Adaptive and Resilient Circuits for Improving Processor Performance, Energy Efficiency, and Yield

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Seminar Focus

Problem

- Variability is a primary challenge in the semiconductor industry
- Degrades processor performance, energy efficiency, & yield

Variability Classifications

1) Simulation tool uncertainties – Mitigated at test
2) Static parameter variations – Mitigated at test
3) Dynamic parameter variations

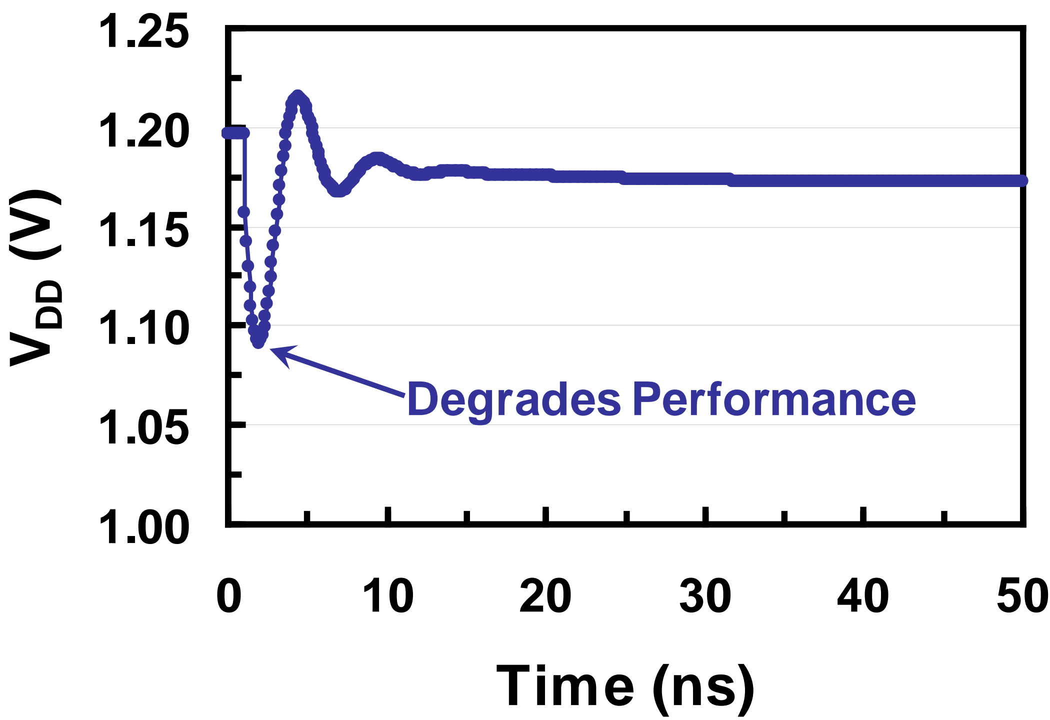
Seminar Focus

1) Dynamic parameter variations
2) Adaptive & resilient circuits for dynamic variation tolerance

Outline

- Sources of Dynamic Parameter Variations
- Impact of Dynamic Variations on Design
- Adaptive & Resilient Circuits
  - Adaptive Designs for Slow-Changing Variations
  - Resilient Designs
  - Adaptive Designs for Fast-Changing Variations
  - Future Adaptive Designs
- Summary

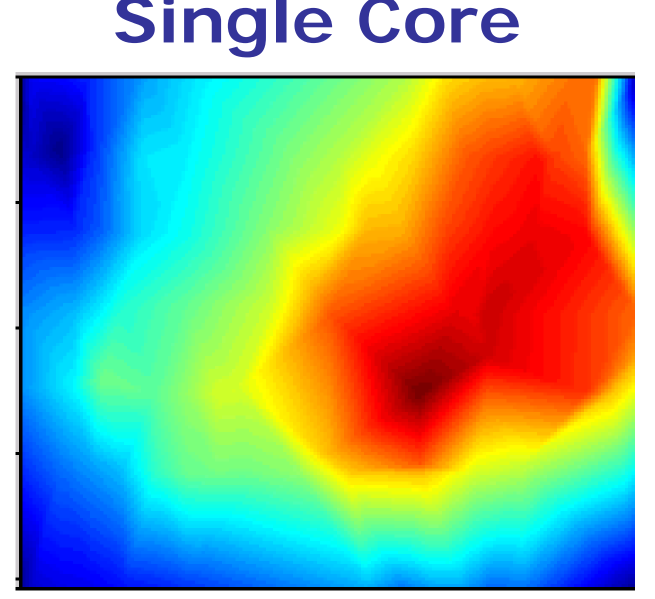
High-Frequency Supply Voltage (V_{DD}) Droops



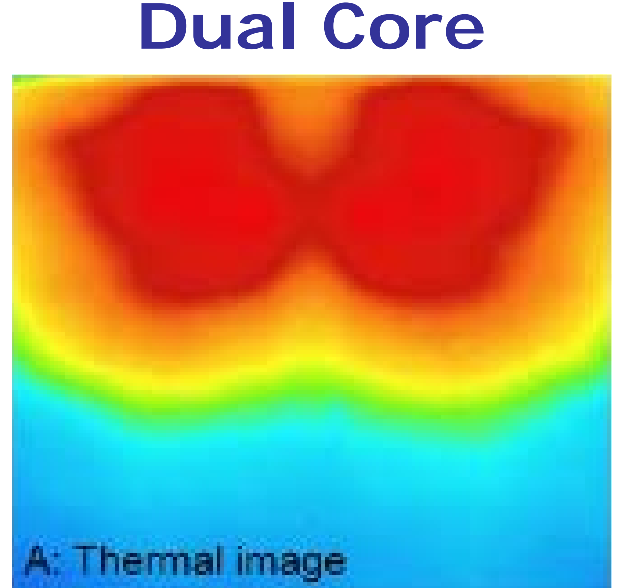
- Abrupt changes in processor activity induce large current transients in the power delivery network
- Primarily a global effect & occurs in nanosecond (ns) time scale
- Infrequent droops degrade performance

Temperature Variations

Single Core



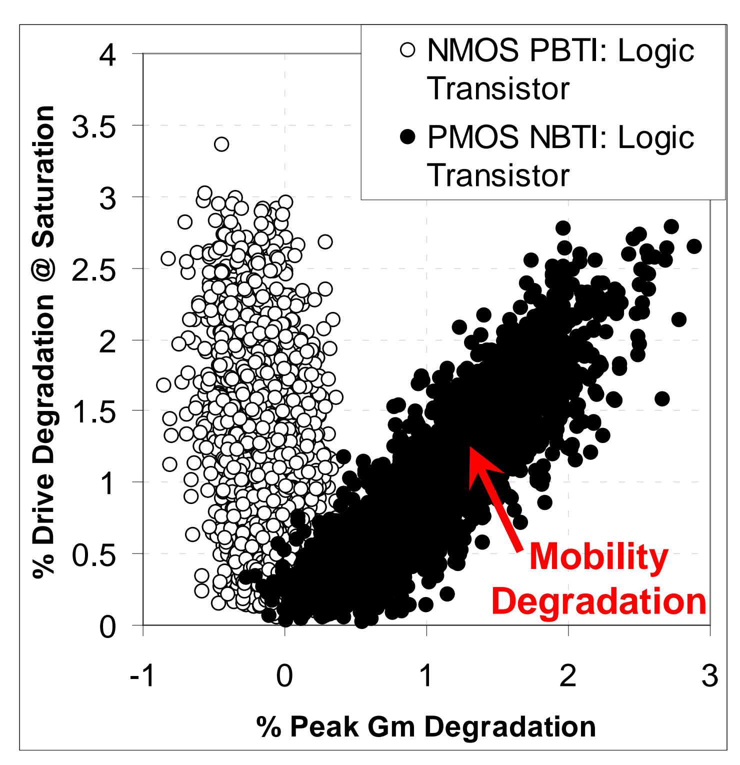
Dual Core

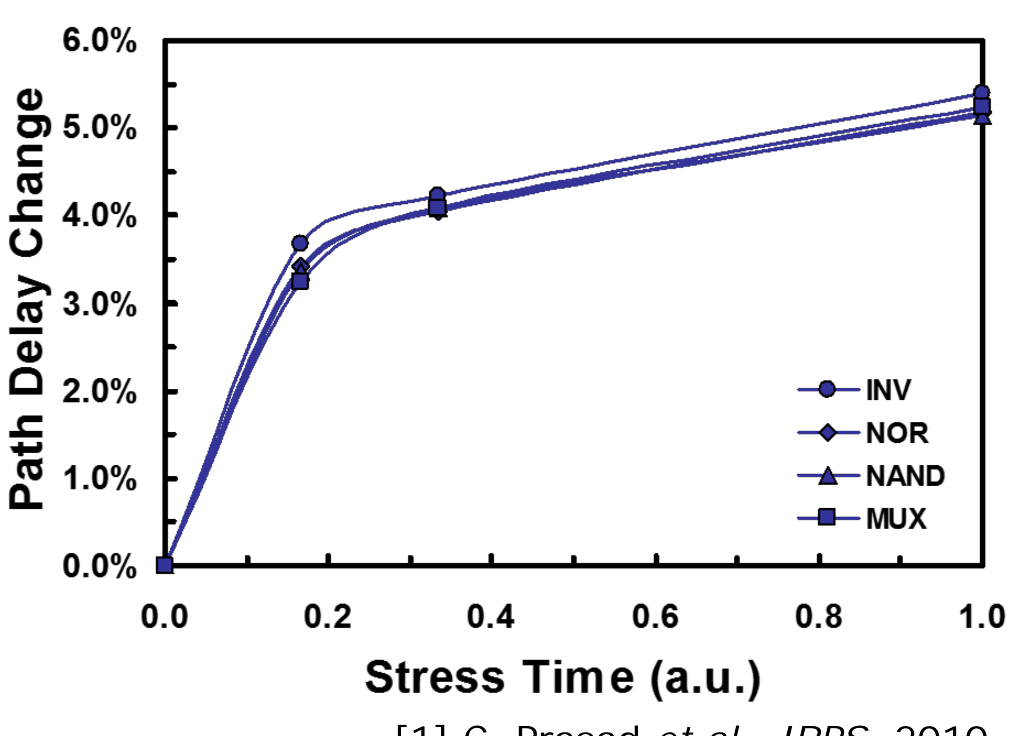


[1] H. F. Hamann *et. al*, *ITHERM*, 2006.

- Changes in processor activity or ambient conditions
- Dynamic time scale: 100μs to 1ms

Bias Temperature Instability (BTI)

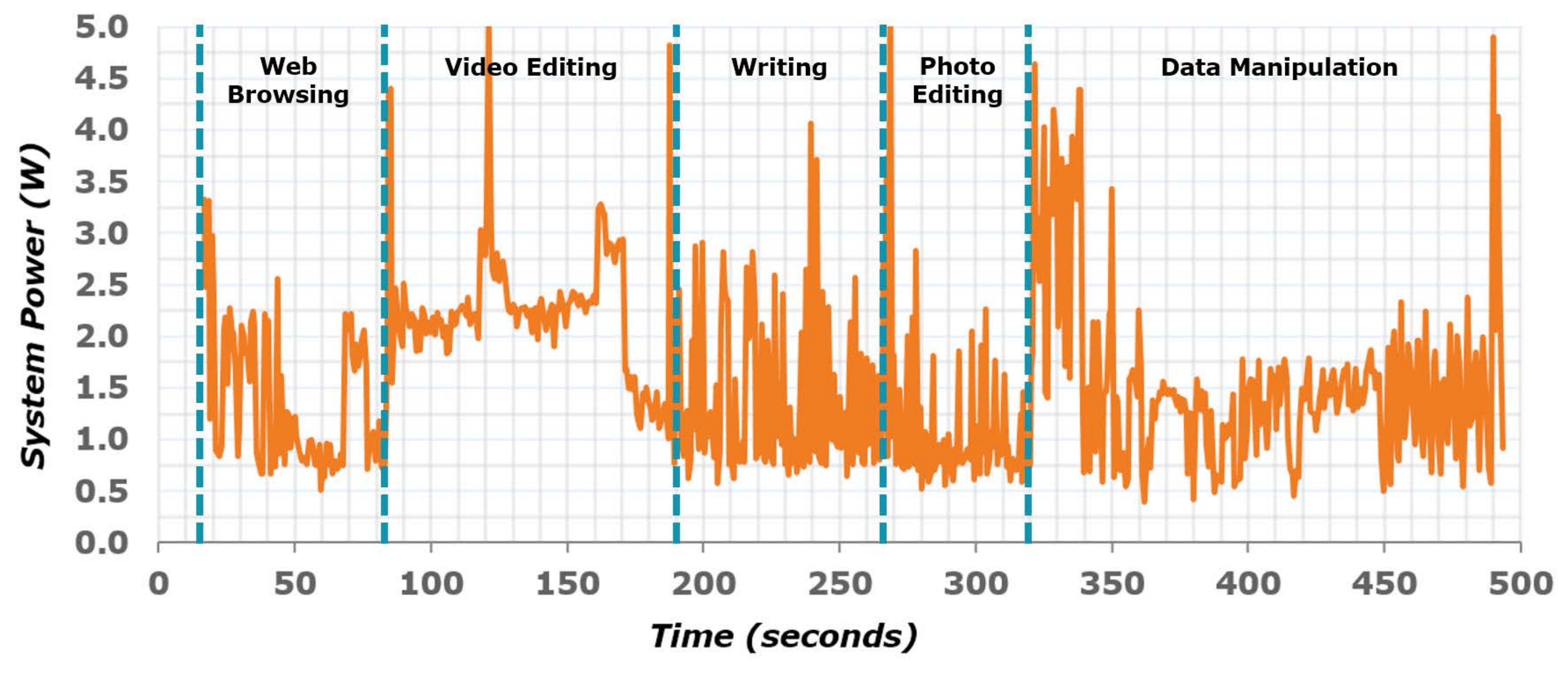




[1] C. Prasad *et al.*, *IRPS*, 2010.
[2] J. Tschanz *et al.*, *Symp. VLSI Circuits*, 2009.

- Interface damage reduces PMOS mobility (negative BTI – NBTI)
- Dielectric traps increase NMOS threshold voltage (positive BTI – PBTI)
- BTI degrades performance at high bias & temperature conditions

Workload Variations



[1] AnandTech, 2017.

- Power significantly depends on the workload

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- Sources of Dynamic Parameter Variations
- Impact of Dynamic Variations on Design
- Adaptive & Resilient Circuits
  - Adaptive Designs for Slow-Changing Variations
  - Resilient Designs
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  - Future Adaptive Designs
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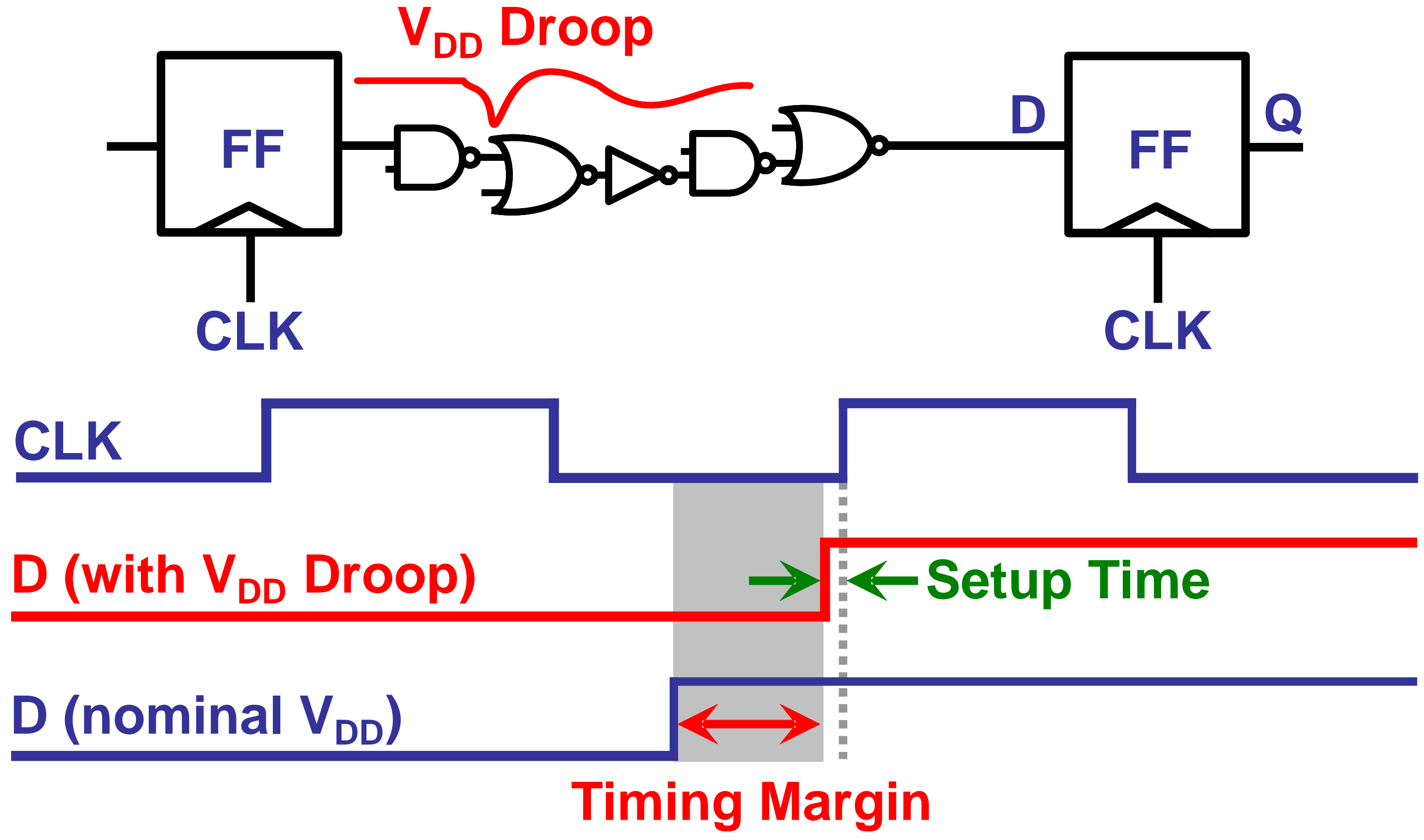
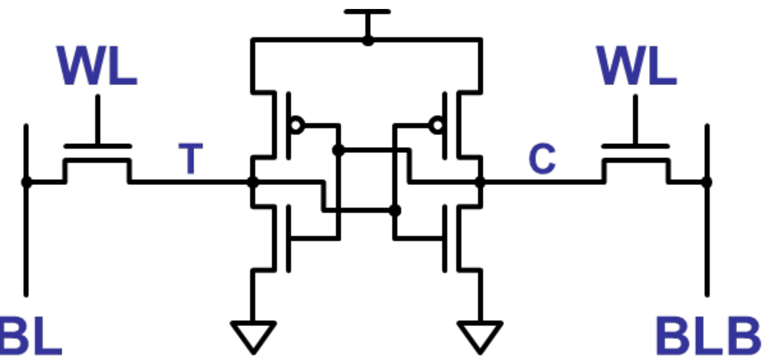
Impact of Dynamic Variations on Logic Design



- Clock frequency (F_{CLK}) or V_{DD} guardbands result in a lower F_{CLK} or a higher V_{DD} to provide extra timing margin for dynamic variations

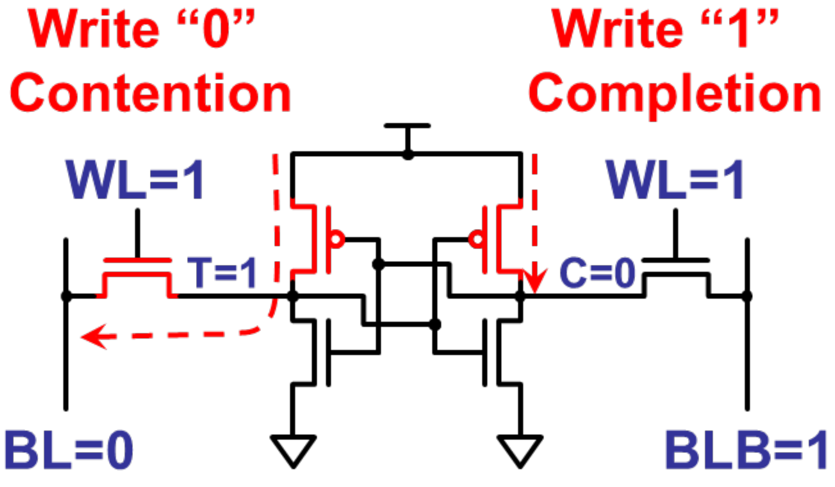
Impact of Dynamic Variations on Memory Design

6-Transistor (6T) Bit-Cell Design



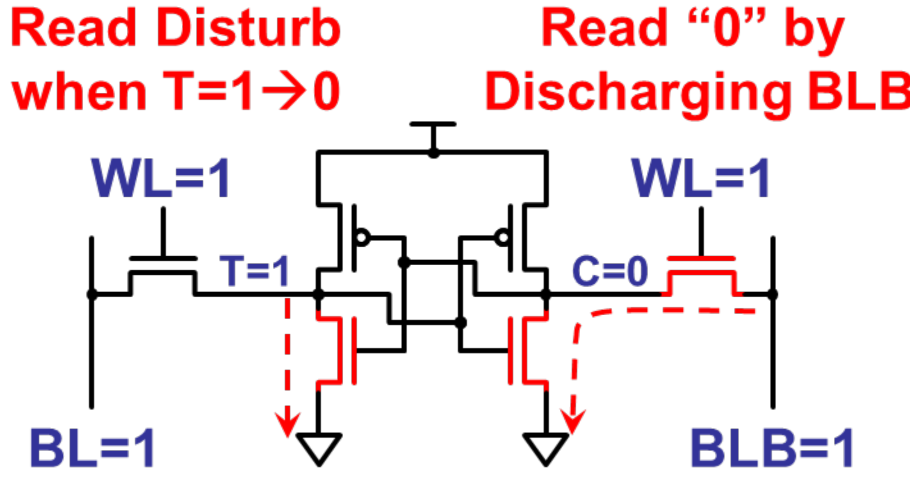
- Modes of operation: Write, read, & retain
- Variations limit the minimum supply voltage (V_{MIN})
- L2 & L3 caches desire the minimum bit-cell area for high density
- Trade-off between bit-cell area & V_{MIN} reduction

6T Bit-Cell Write V_{MIN}



- NFET pass gate writes a strong "0"
- Write V_{MIN} limited by:
  - Contention between NFET pass gate & PFET pull-up
  - PFET pull-up completion

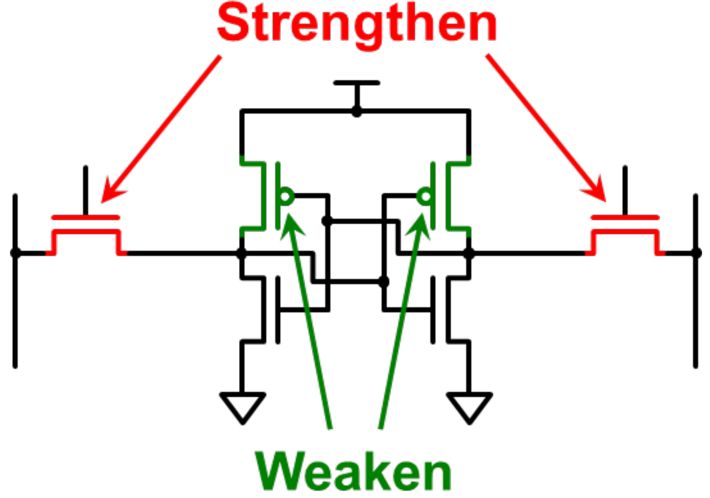
6T Bit-Cell Read V_{MIN}



- NFET pass gate & NFET pull-down discharge BLB voltage
- Read V_{MIN} limited by:
  - Strong NFET pass gate & weak NFET pull-down

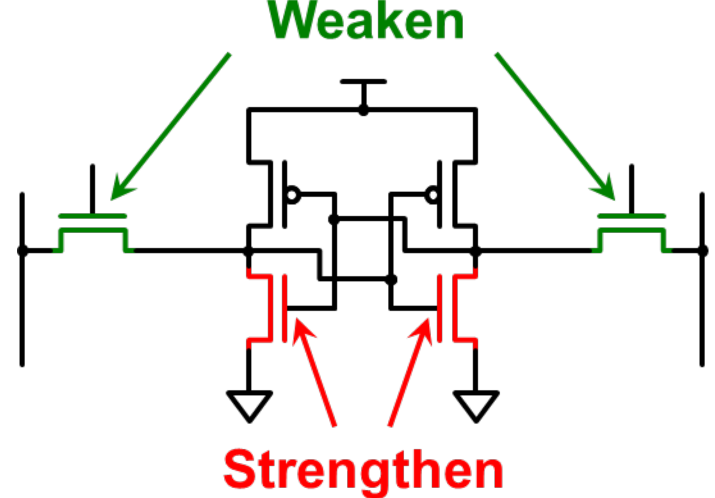
Write & Read-Assist Circuits to Reduce V_{MIN}

Write-Assist Circuits



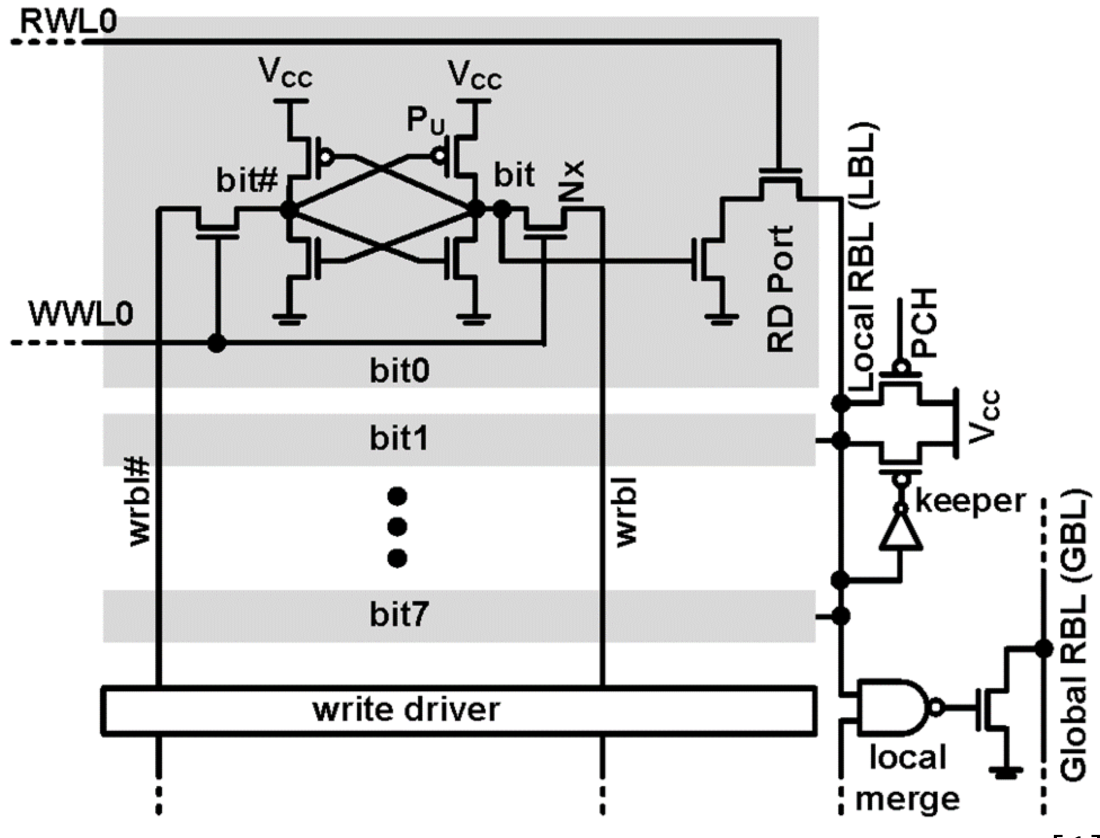
- V_{DD} collapse
- Wordline overdrive
- Negative bit line

Read-Assist Circuits



- V_{DD} boost
- Negative V_{SS} bias
- Wordline underdrive

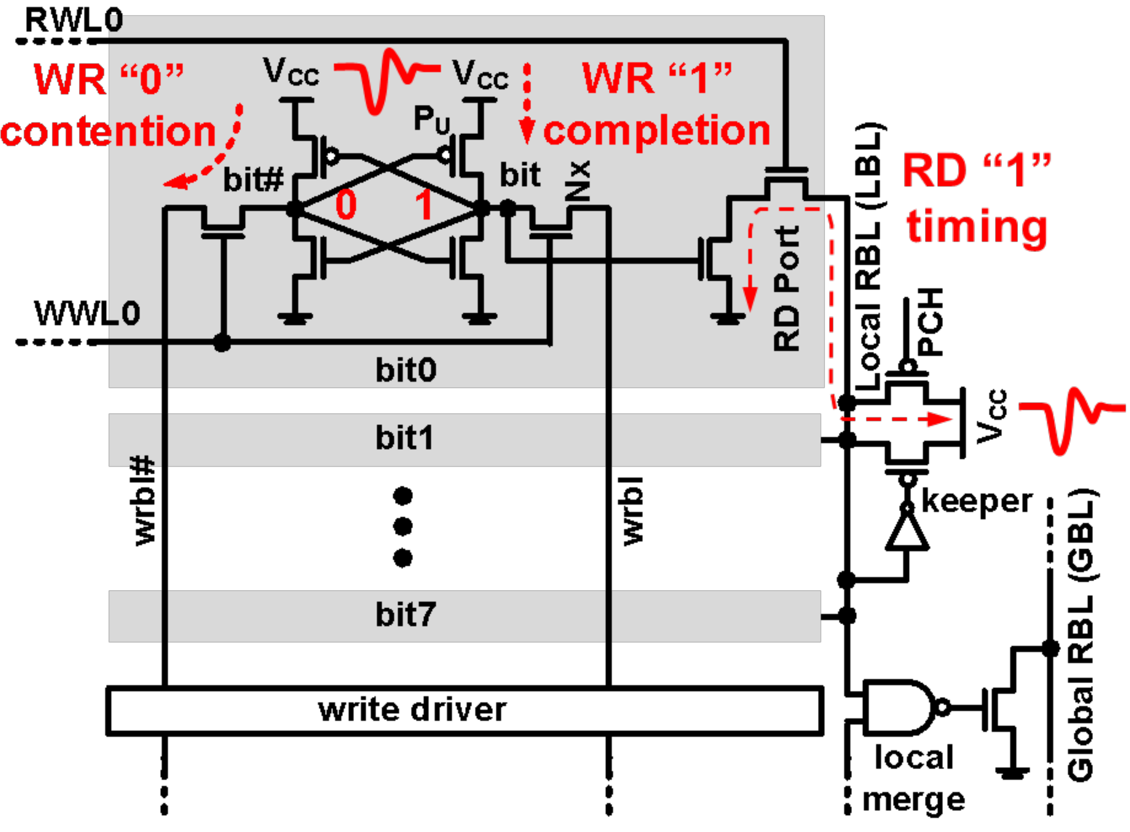
8T Bit-Cell Design



[1] A. Raychowdhury *et al.*, *JSSC*, 2011.

- 8T bit cell decouples the read & write ports, enabling a lower V_{MIN}

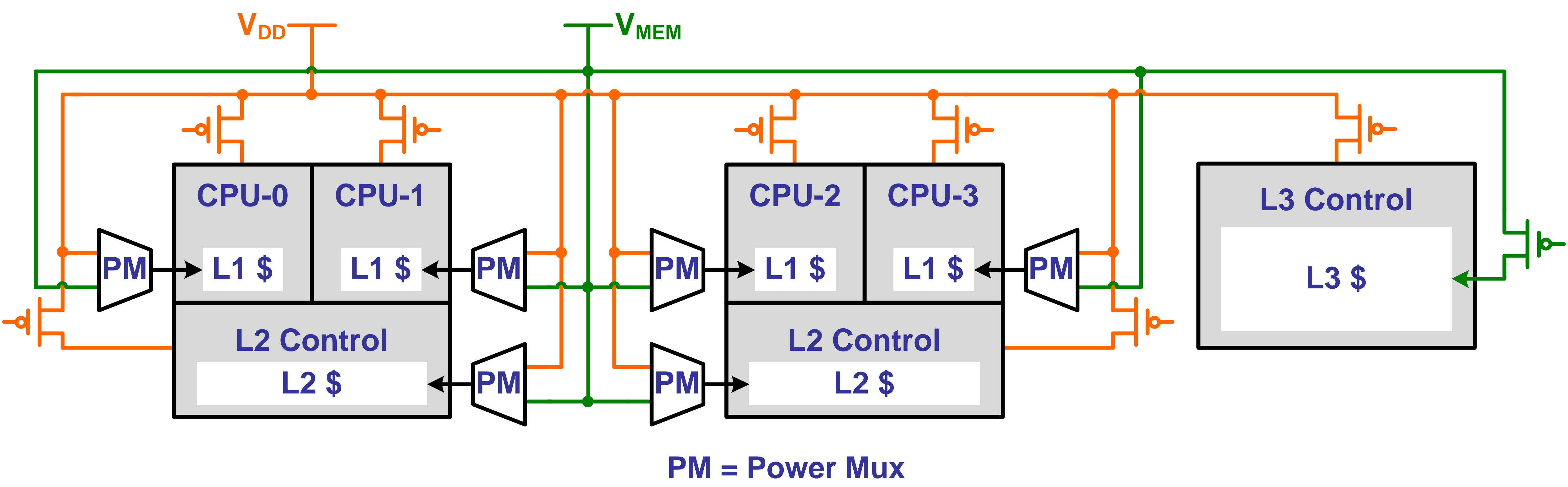
V_{MIN} Guardband for Dynamic Variations



[1] A. Raychowdhury *et al.*, *JSSC*, 2011.

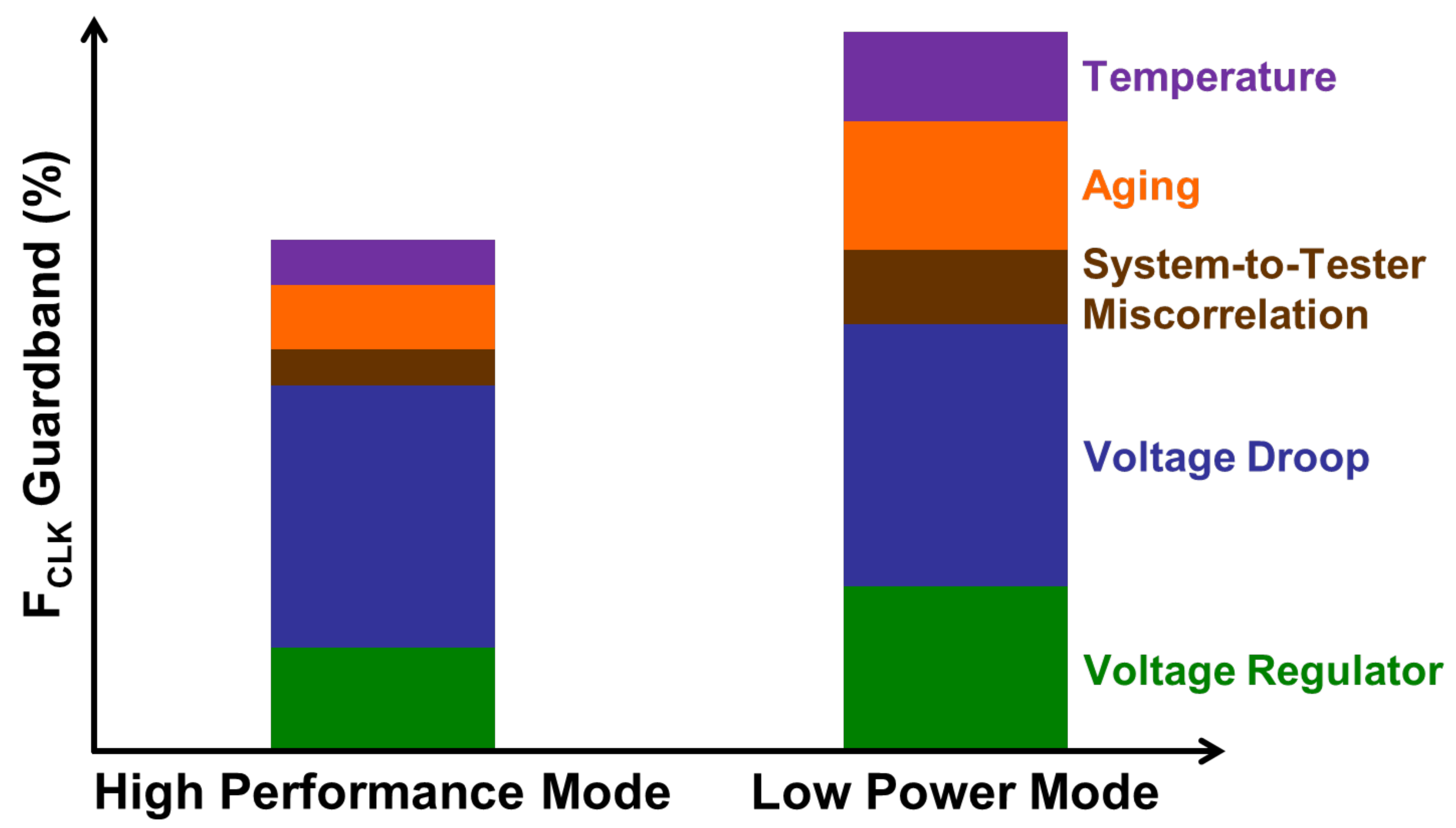
- V_{MIN} guardband guarantees correct read & write operations within the presence of dynamic variations

Separate Voltage Rails for Logic & Memory



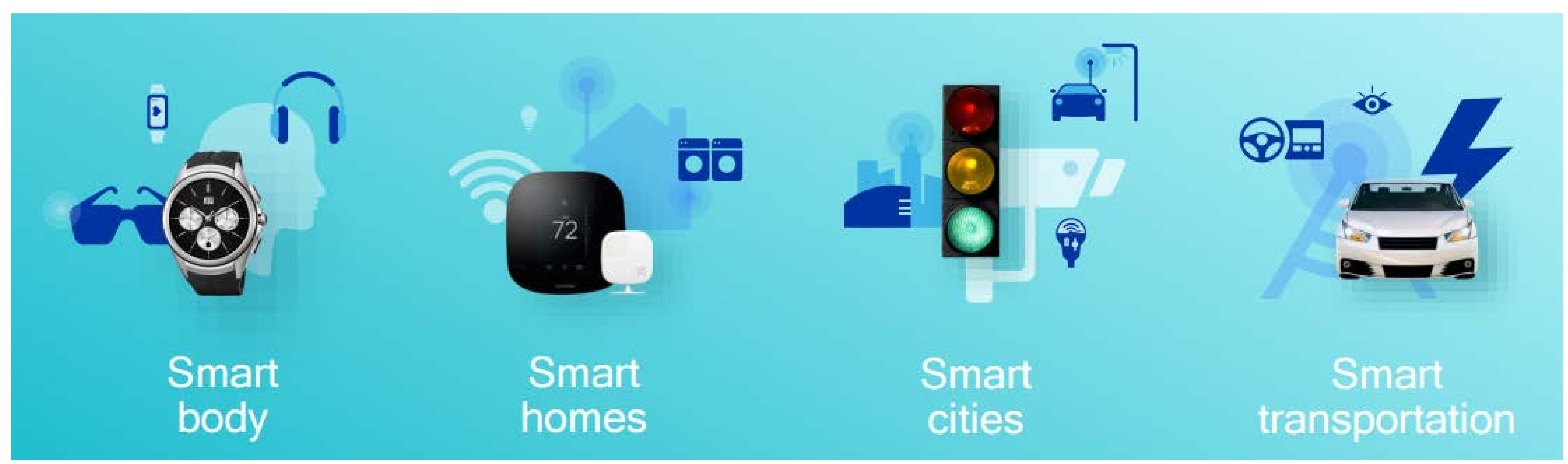
- Logic & memory operate on separate voltage rails at low voltage to enable logic V_{MIN} scaling

Dynamic Variation Guardbands



- Dynamic variations degrade performance, energy efficiency, & yield

Processors for Internet of Things (IoT)



- IoT requirements exacerbate the impact of dynamic variations
  - Low-cost packaging
  - Time-varying energy harvesters
  - Wide range of temperature conditions
  - Long-lifetime requirements

Adaptive Design versus Resilient Design

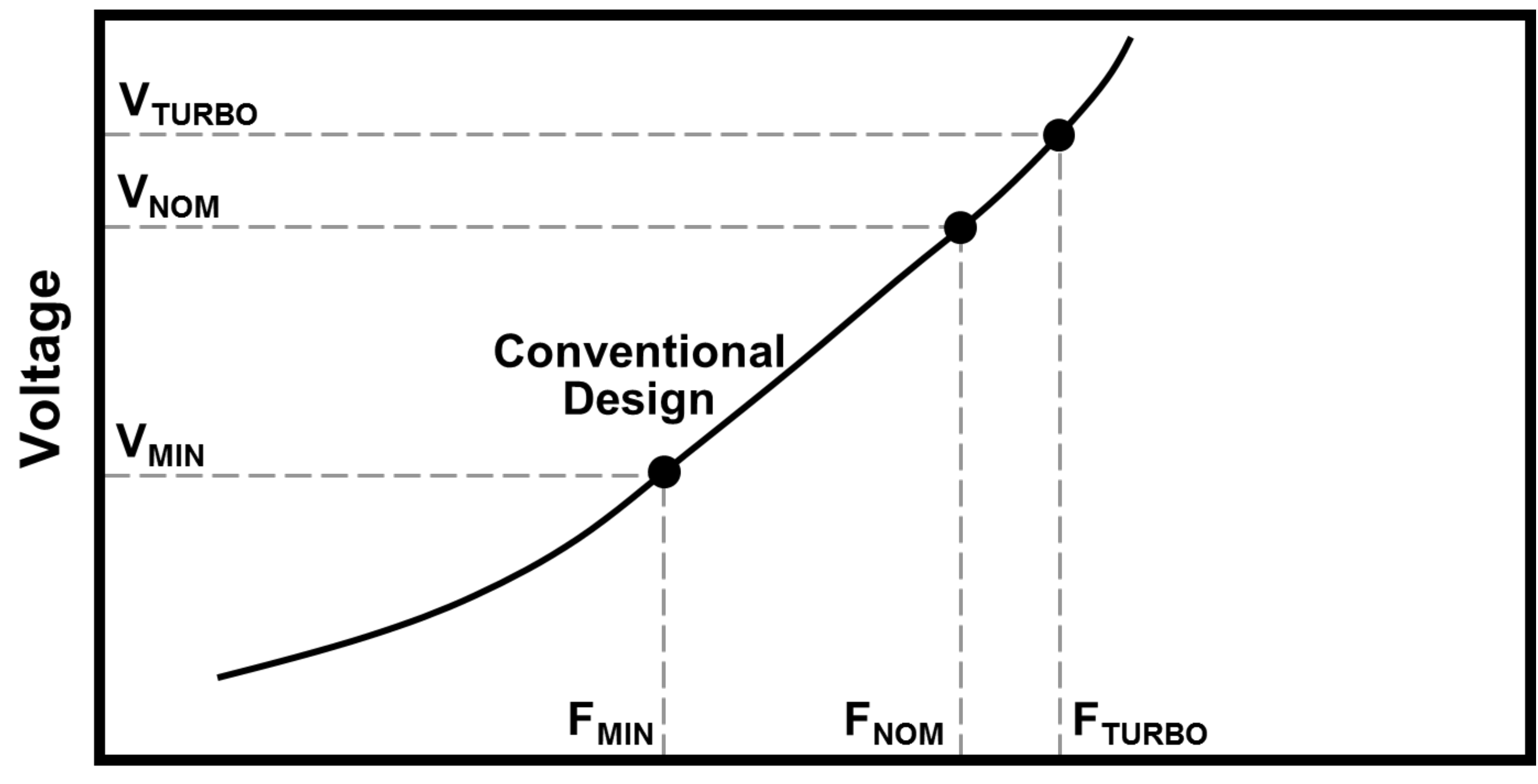
Merriam-Webster Definitions

Adaptation: adjustment to environmental conditions

Resilience: an ability to recover from or adjust easily to misfortune or change

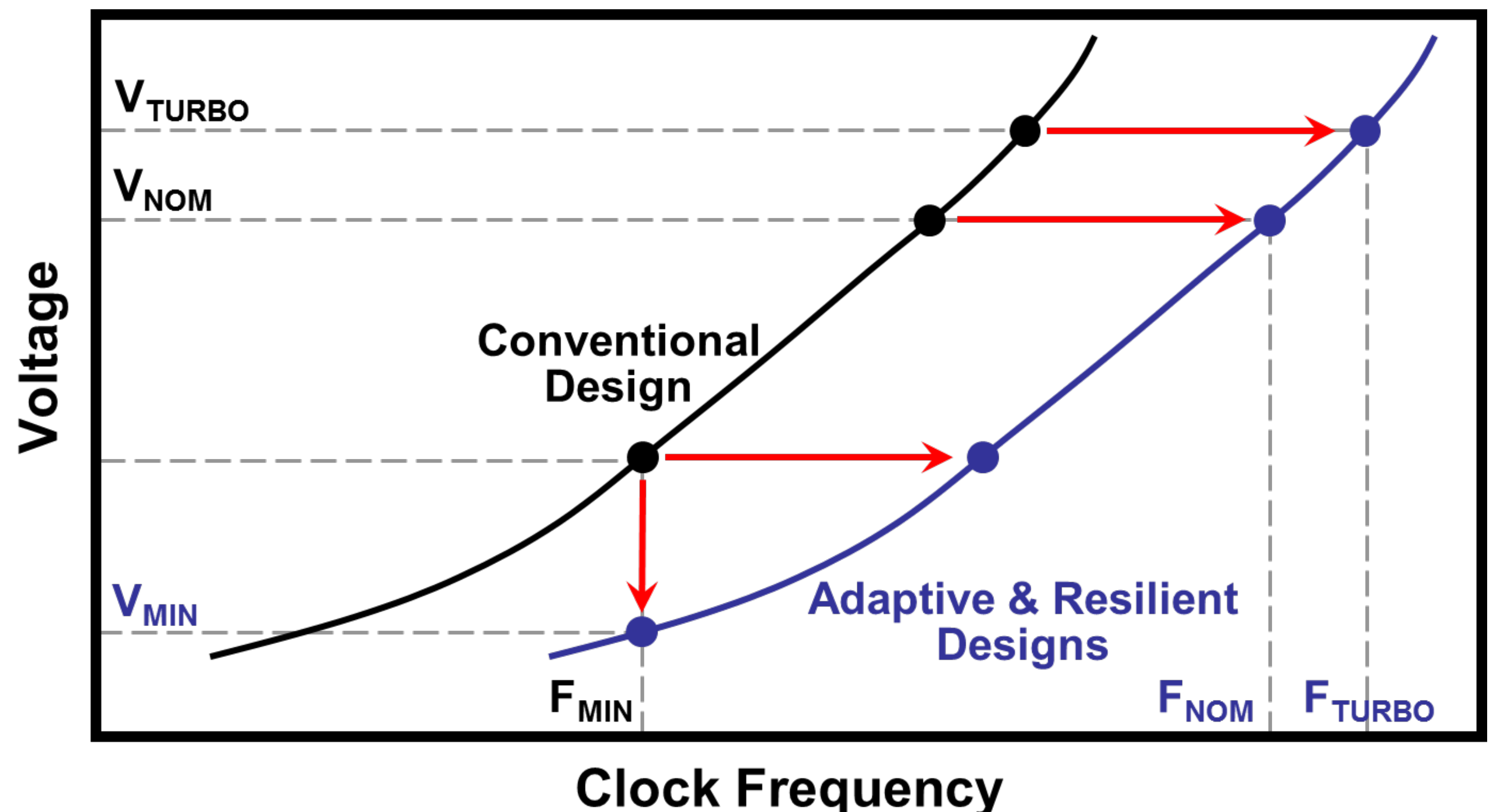
- Adaptive design detects parameter changes & adjusts the operating conditions to avoid errors
- Resilient design detects & corrects errors to maintain correct system operation
- Adaptive & resilient designs mitigate guardbands to improve performance, energy efficiency, & yield

Wide Dynamic Operation Range



- V_{TURBO} & V_{NOM}: Limited by reliability or power constraints
- V_{MIN}: Limited by memory circuit failures

Wide Dynamic Operation Range



- Adaptive & resilient designs expand the operating range

Wide Range of Platforms

Platform	Power	Perf.	Cores	Thermal	Ambient	RAS
Server	High	Very High		Fan	Controlled	Very High
Tablet	Low	High	SoC	Fan-less	Uncontrolled	High
Phone	Very Low	Med	SoC	Fan-less	Uncontrolled	Med
IoT	Ultra Low	Low	SoC	Fan-less	Uncontrolled	Low

- Couple of designs must support many platforms
- Adaptive & resilient designs to satisfy multiple platforms

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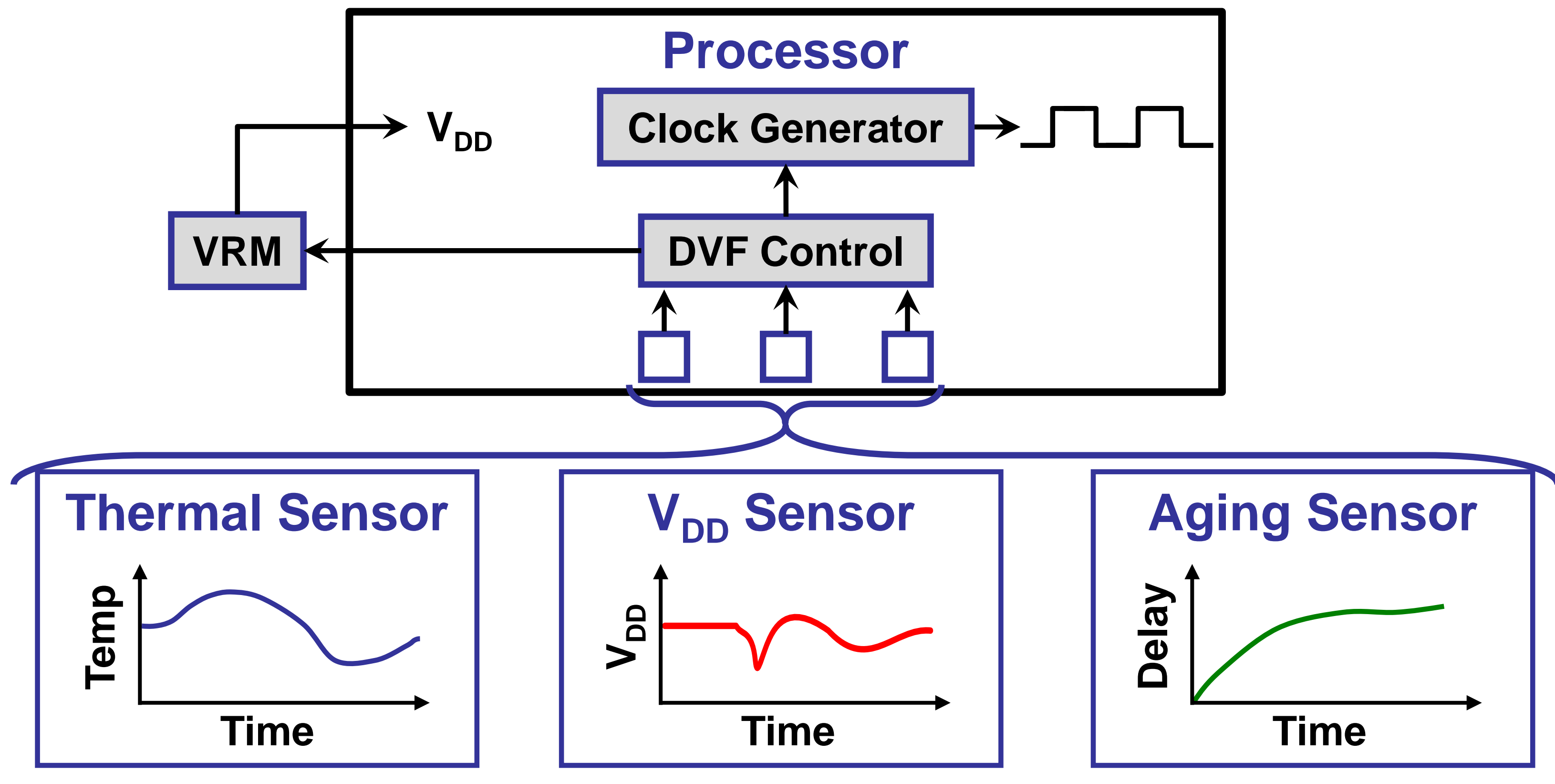
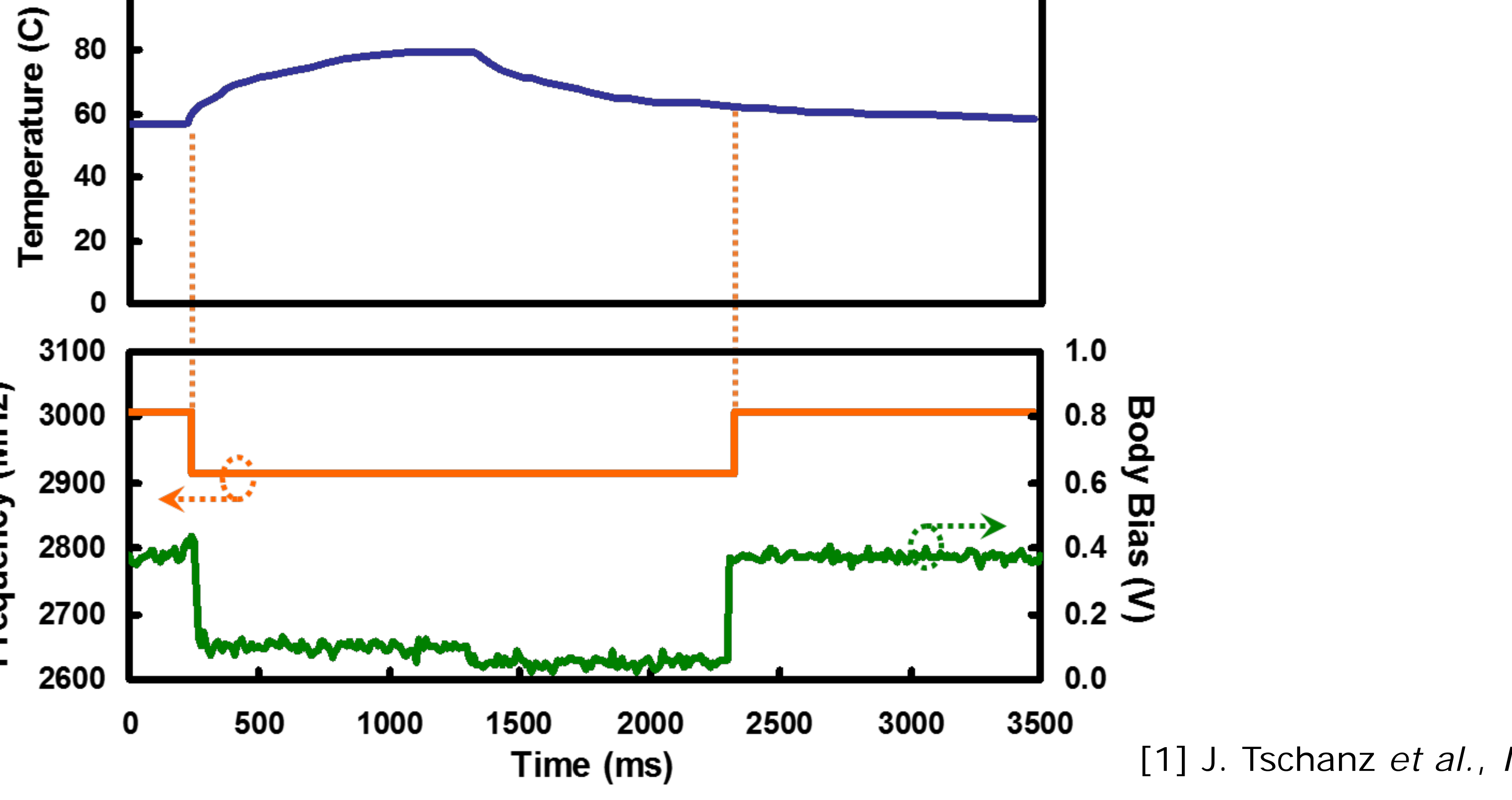
Traditional Adaptive Design



- Detect temperature, V_{DD}, & aging variations
- Adapt F_{CLK} or V_{DD} to avoid timing violations

[1] T. Fisher *et al.*, *JSSC*, 2006.
[2] R. McGowen *et al.*, *JSSC*, 2006.
[3] J. Tschanz *et al.*, *ISSCC*, 2007.
[4] C. Lefurgy *et al.*, *MICRO*, 2011.
[5] A. Grenat *et al.*, *ISSCC*, 2014.
[6] M. Floyd *et al.*, *ISSCCC*, 2017.

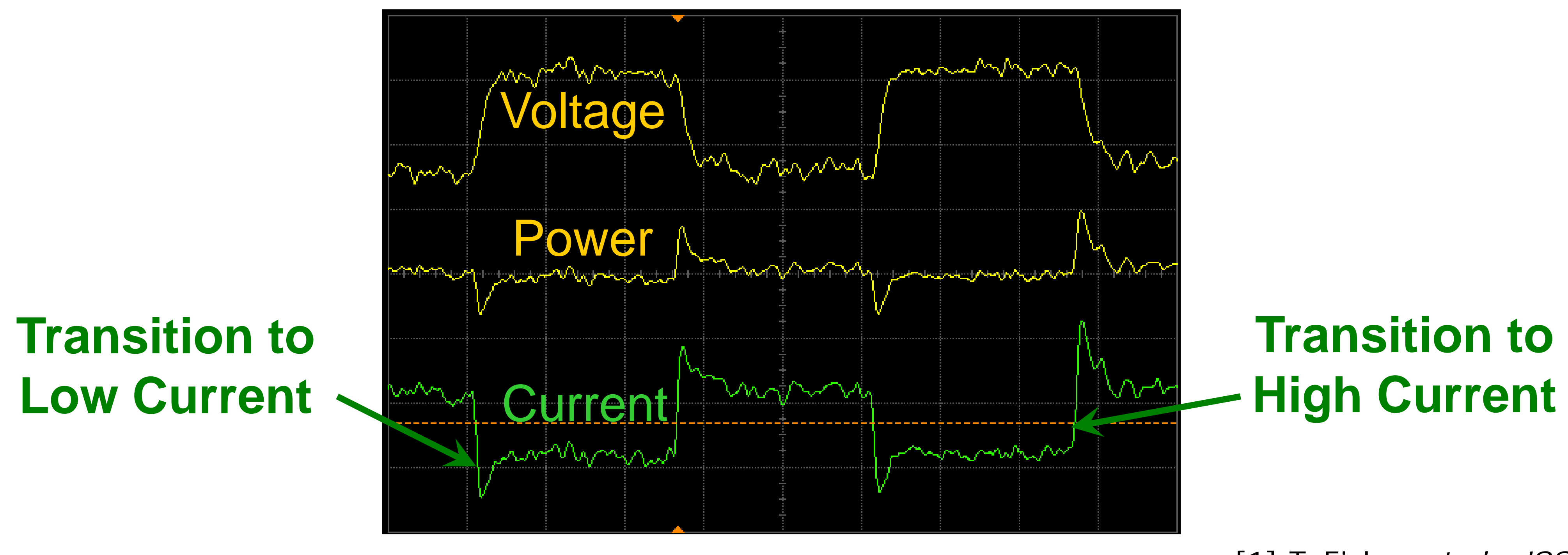
Adapting to Temperature Variations



[1] J. Tschanz *et al.*, *ISSCC*, 2007.

- Adaptive F_{CLK} & body bias ensures correct operation & lower leakage at higher temperatures

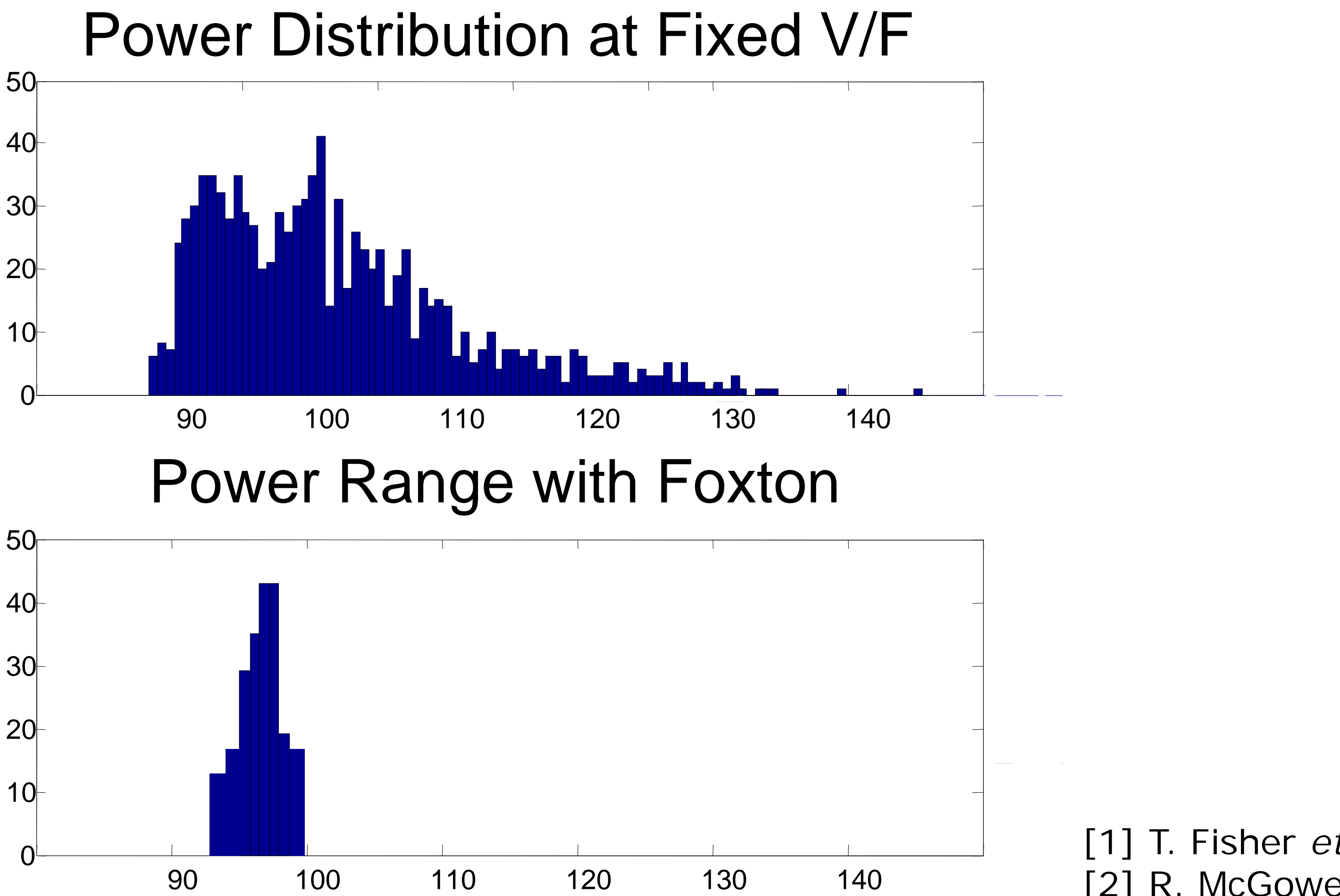
Adapting to Workload Variations



[1] T. Fisher *et al.*, *JSSC*, 2006.
[2] R. McGowen *et al.*, *JSSC*, 2006.

- Adaptive power management design increases performance within a power & thermal envelope

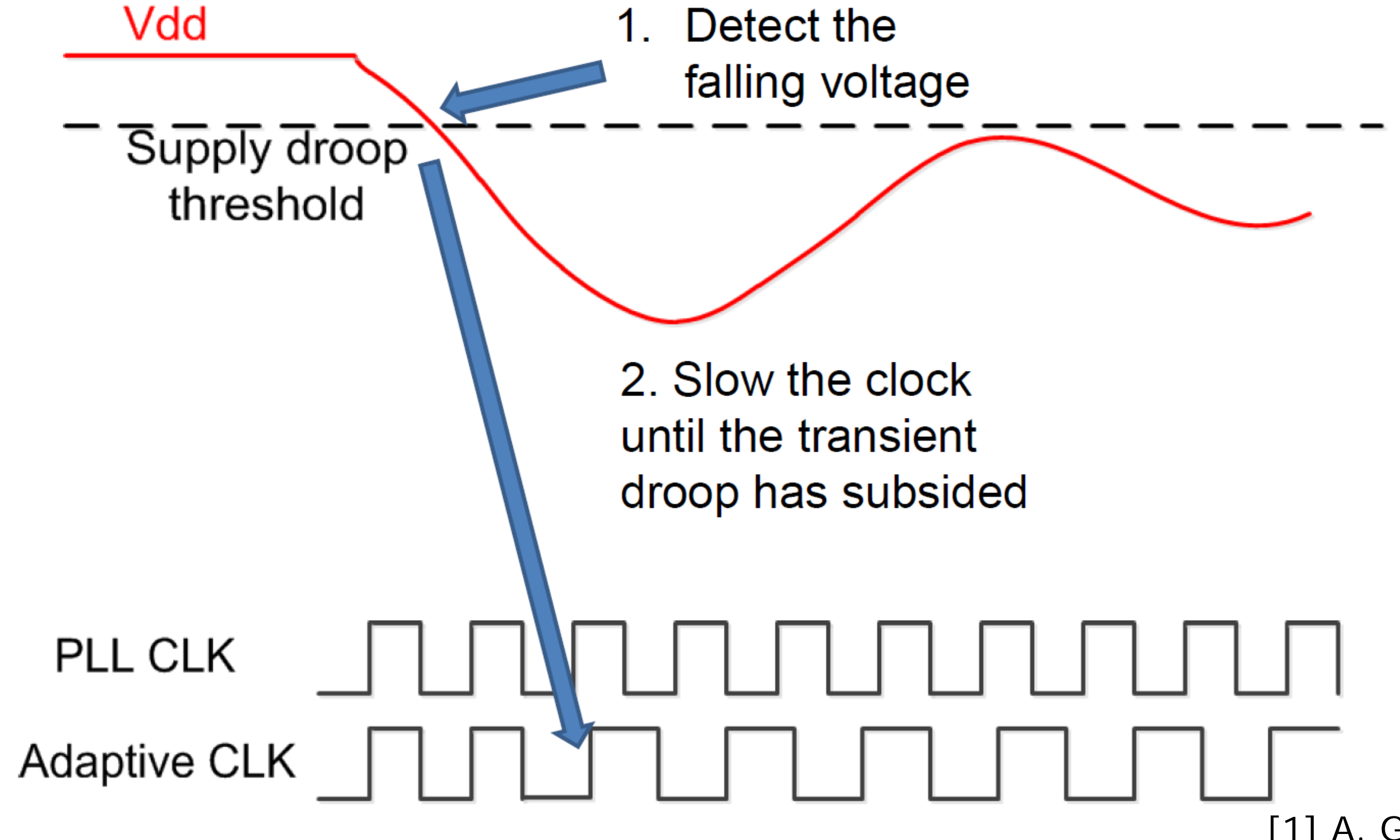
Adapting to Workload Variations



[1] T. Fisher *et al.*, *JSSC*, 2006.
[2] R. McGowen *et al.*, *JSSC*, 2006.

- Dynamic adaptation reduces the processor power variation

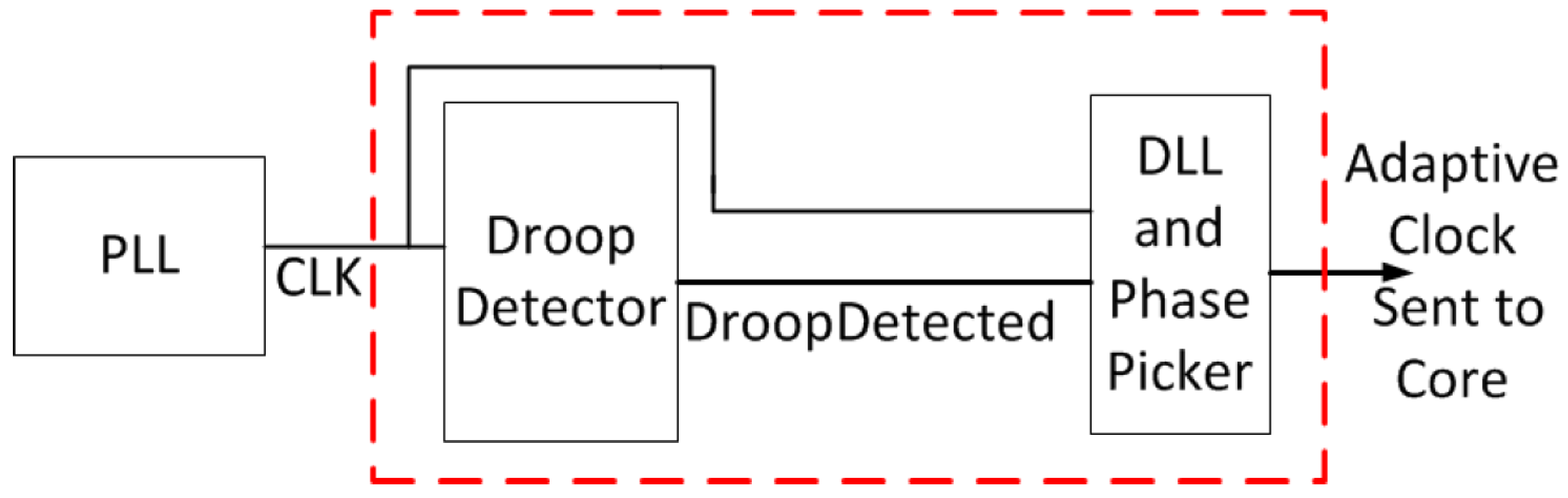
Adaptive Design for V_{DD} Droop Mitigation



[1] A. Grenat *et al.*, *ISSCC*, 2014.
[2] T. Fischer *et al.*, *JSSC*, 2006.

- Detect V_{DD} droop & then adapt by stretching the clock period

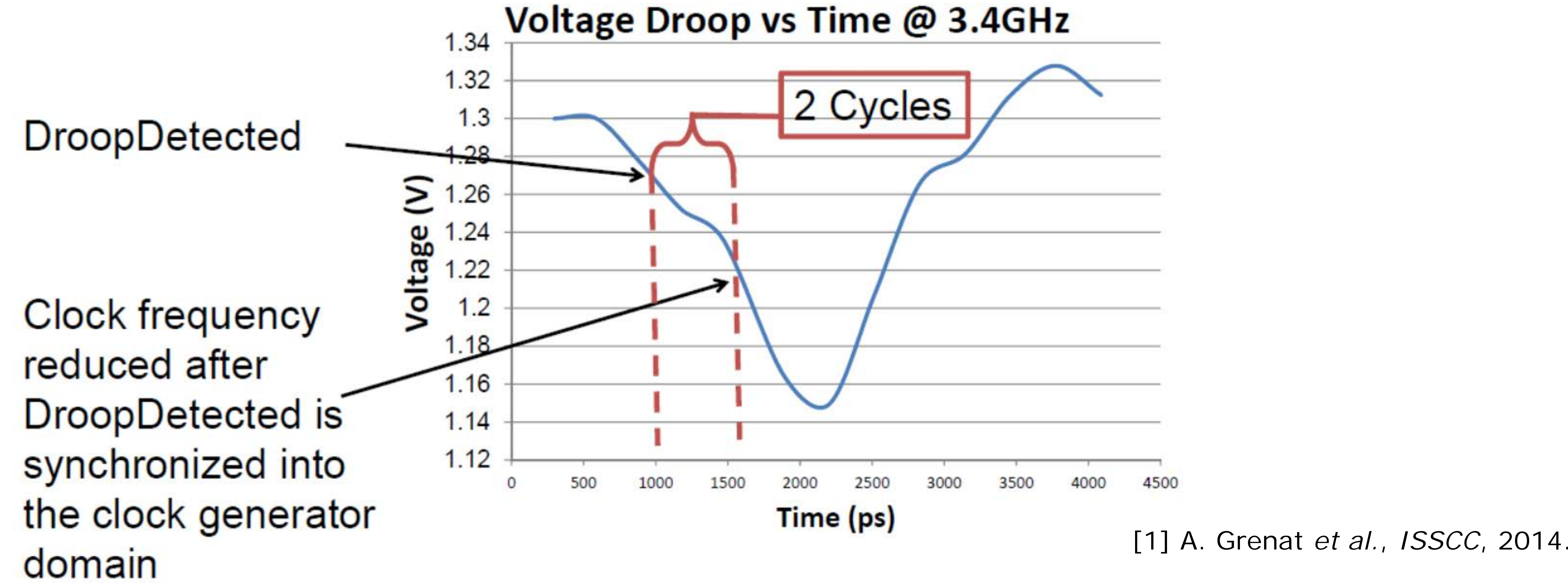
Adaptive Design for V_{DD} Droop Mitigation



[1] A. Grenat *et al.*, *ISSCC*, 2014.

- Adaptive clock design allows 5% resolution in F_{CLK} reduction

Adaptive Design for V_{DD} Droop Mitigation



[1] A. Grenat *et al.*, *ISSCC*, 2014.

- Recovers a portion of the F_{CLK} loss when $F_{CLK} >> F_{DROOP}$
- Response time limits benefits

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Resilient Designs

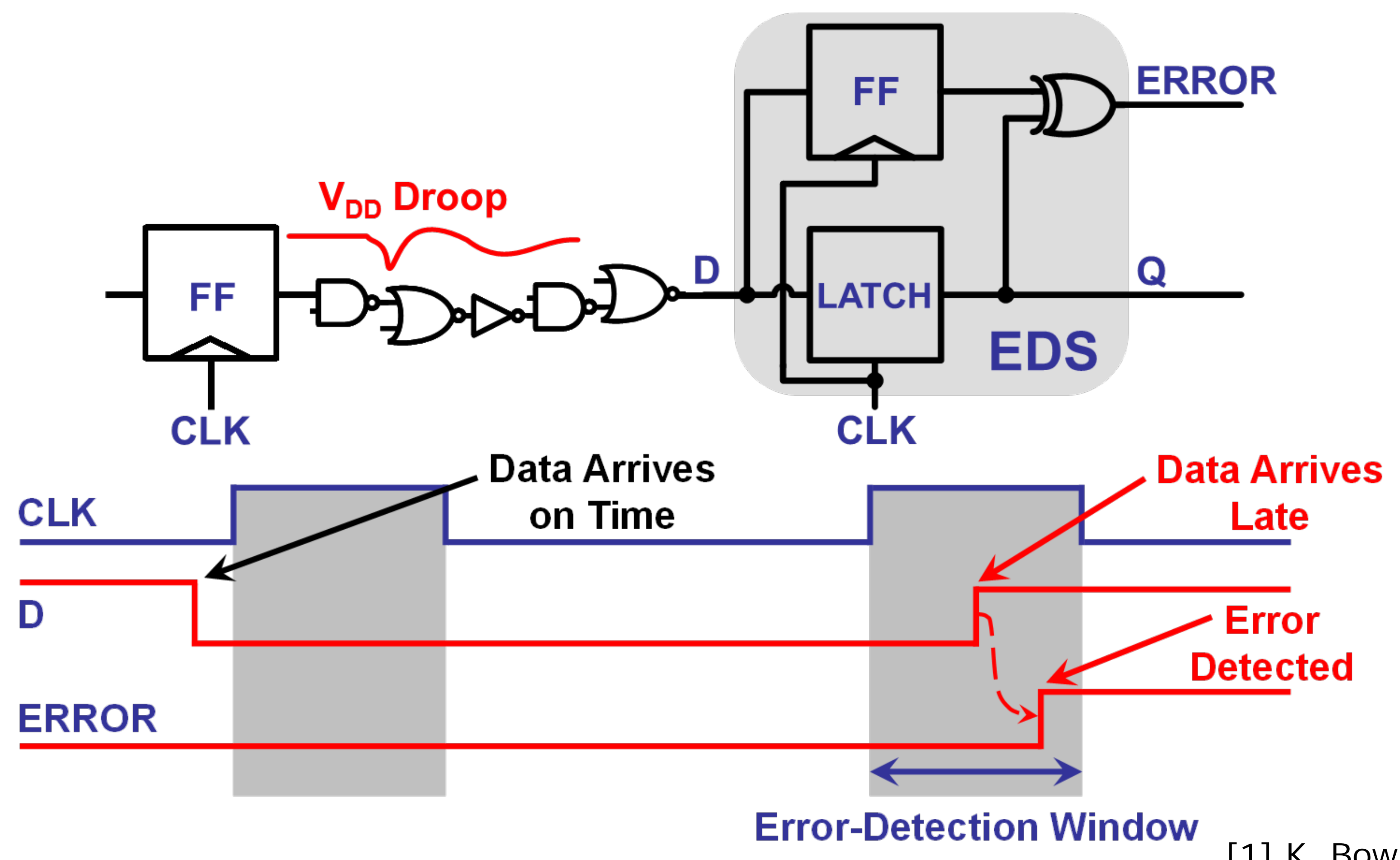
- Operate V_{DD} & F_{CLK} based on nominal conditions
- Resilient circuits detect & correct timing errors due to infrequent dynamic variations
- Throughput & energy benefits result from mitigating dynamic variation guardbands

Error-Detection Circuits

1) Error-Detection Sequential (EDS)

2) Tunable Replica Circuit (TRC)

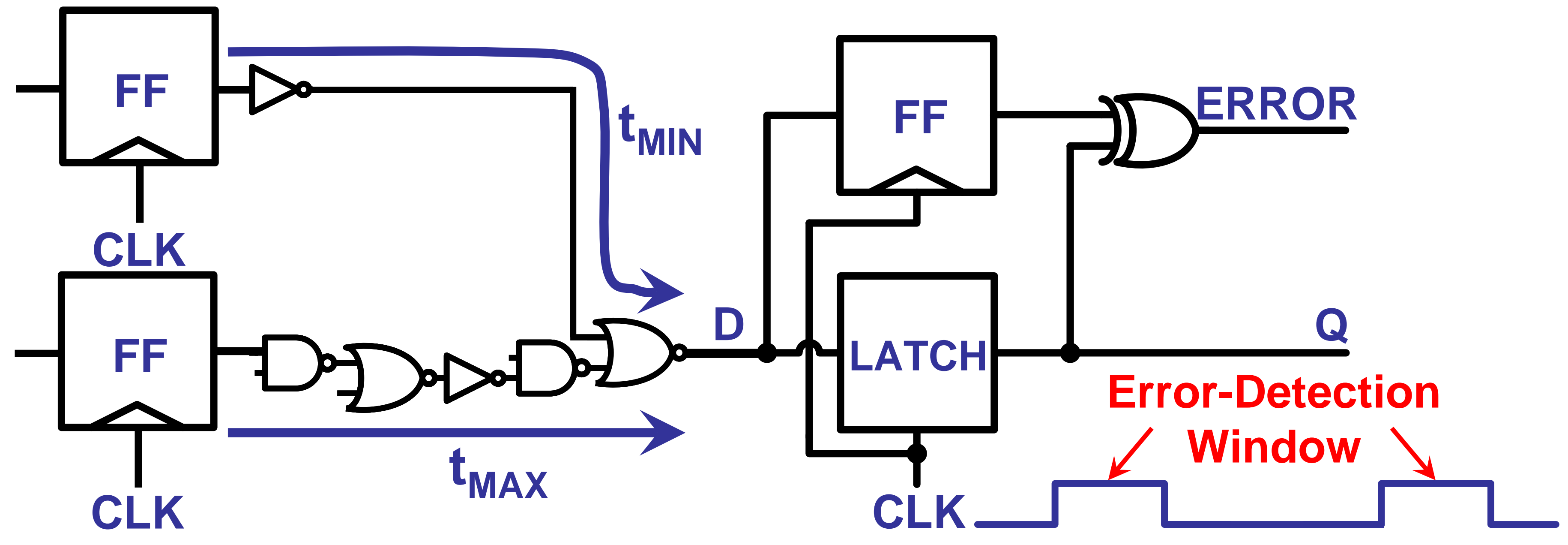
Error-Detection Sequential (EDS)



[1] K. Bowman *et al.*, *JSSC*, 2009.

- Detect timing error within error-detection window

Error-Detection Sequential (EDS)

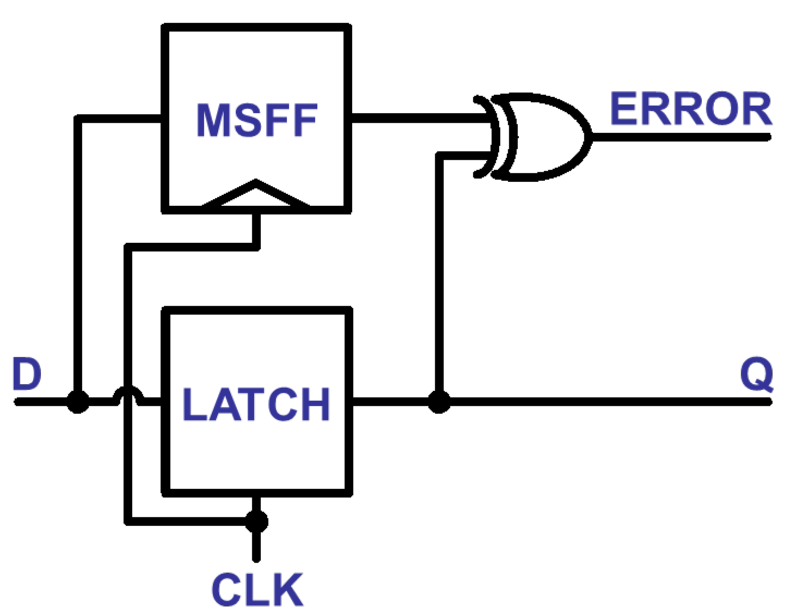


[1] K. Bowman *et al.*, *JSSC*, 2009.

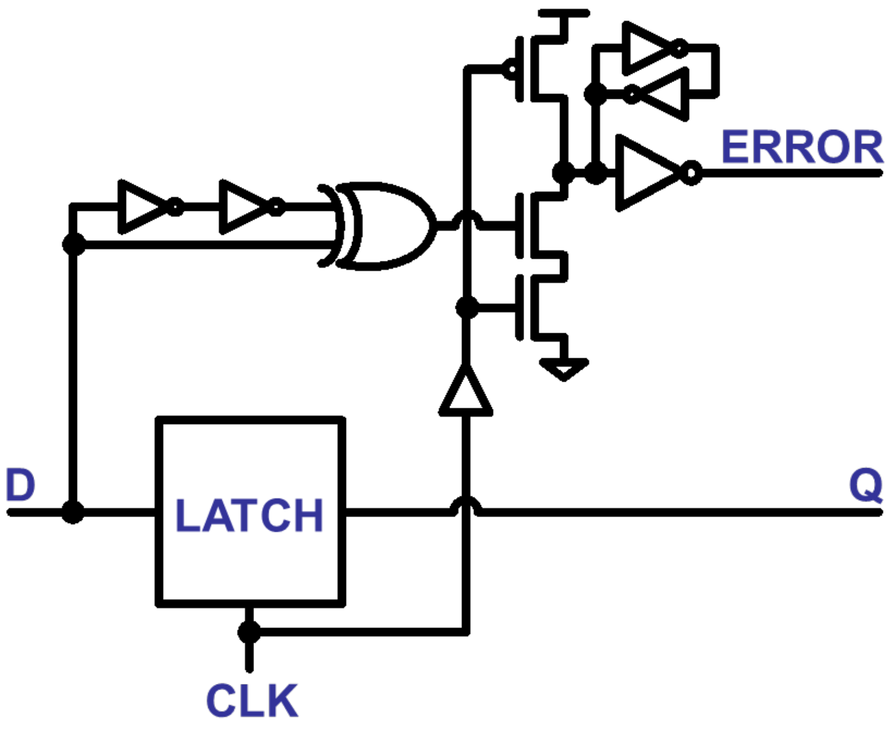
- Min-delay penalty increases by error-detection window
- Clock duty-cycle control maintains a constant high-phase delay during low & high F_{CLK}

Error-Detection Sequential (EDS)

Double-Sampling EDS



Transition-Detector EDS



[1] P. Franco *et al.*, *VLSI Test Symp.*, 1994.
[2] M. Nicolaidis, *VLSI Test Symp.*, 1999.
[3] D. Ernst *et al.*, *MICRO*, 2003.
[4] S. Das *et al.*, *JSCC*, 2009.
[5] K. Bowman *et al.*, *JSSC*, 2009.
[6] D. Bull *et al.*, *JSSC*, 2011.
[7] S. Kim *et al.*, *ISSCC*, 2013.
[8] Z. Hao *et al.*, *IEICE*, 2016.
[9] Y. Zhang *et al.*, *ISSCC*, 2016.

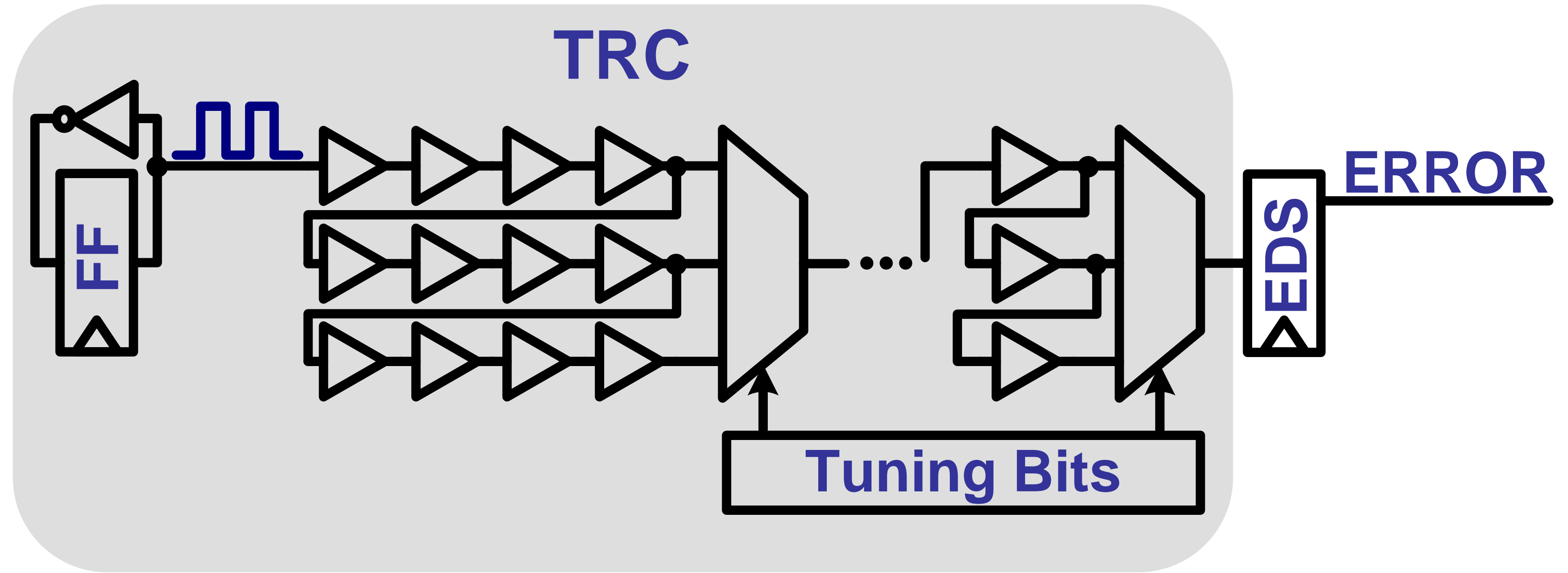
- Many EDS circuit designs in the literature with various trade-offs

Error-Detection Circuits

1) Error-Detection Sequential (EDS)

2) Tunable Replica Circuit (TRC)

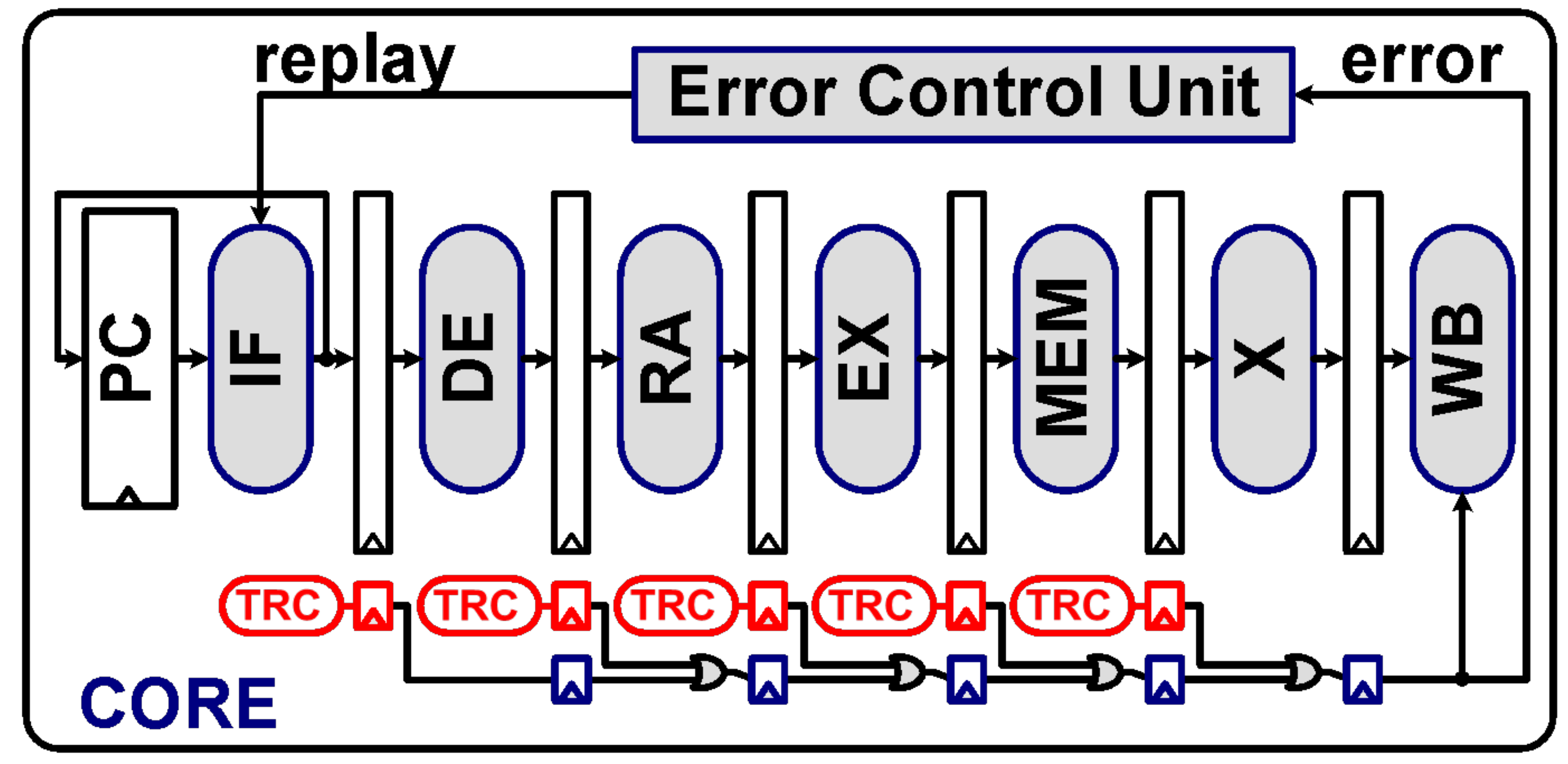
Tunable Replica Circuit (TRC)



[1] K. Bowman *et al.*, *JSSC*, 2011.

- TRC monitors critical-path delays
- Non-intrusive design

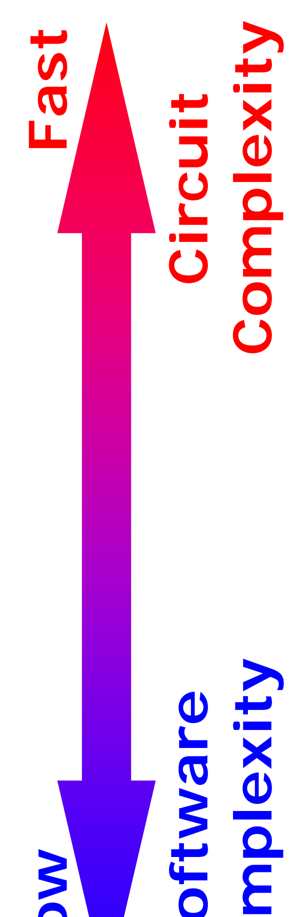
Tunable Replica Circuit (TRC)



[1] K. Bowman *et al.*, *JSSC*, 2011.

- Calibrate TRC to track critical paths per pipeline stage
- TRC error initiates error recovery
- TRC must always fail if any critical path fails

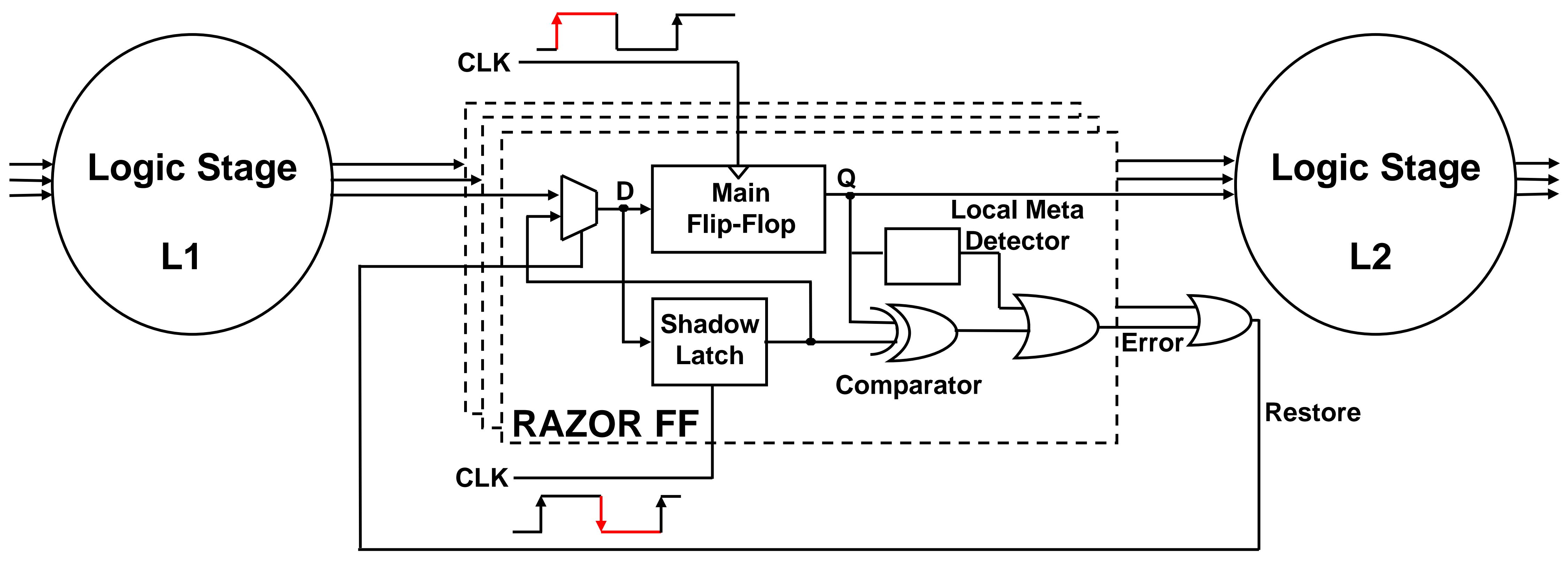
Error Recovery



- Local Recovery [1]-[2]
  - Inject correct value into pipeline
  - Stall for one cycle & continue
- Instruction Replay [3]-[5]
  - Invalidate instructions in pipeline
  - Re-execute errant instruction
- Checkpoint & Rollback
  - Periodically save system state in memory
  - Rollback to last saved state

[1] D. Ernst *et al.*, *MICRO*, 2003.
[2] S. Das *et al.*, *JSSC*, 2006.
[3] S. Das *et al.*, *JSCC*, 2009.
[4] K. Bowman *et al.*, *JSSC*, 2009.
[5] K. Bowman *et al.*, *JSSC*, 2011.

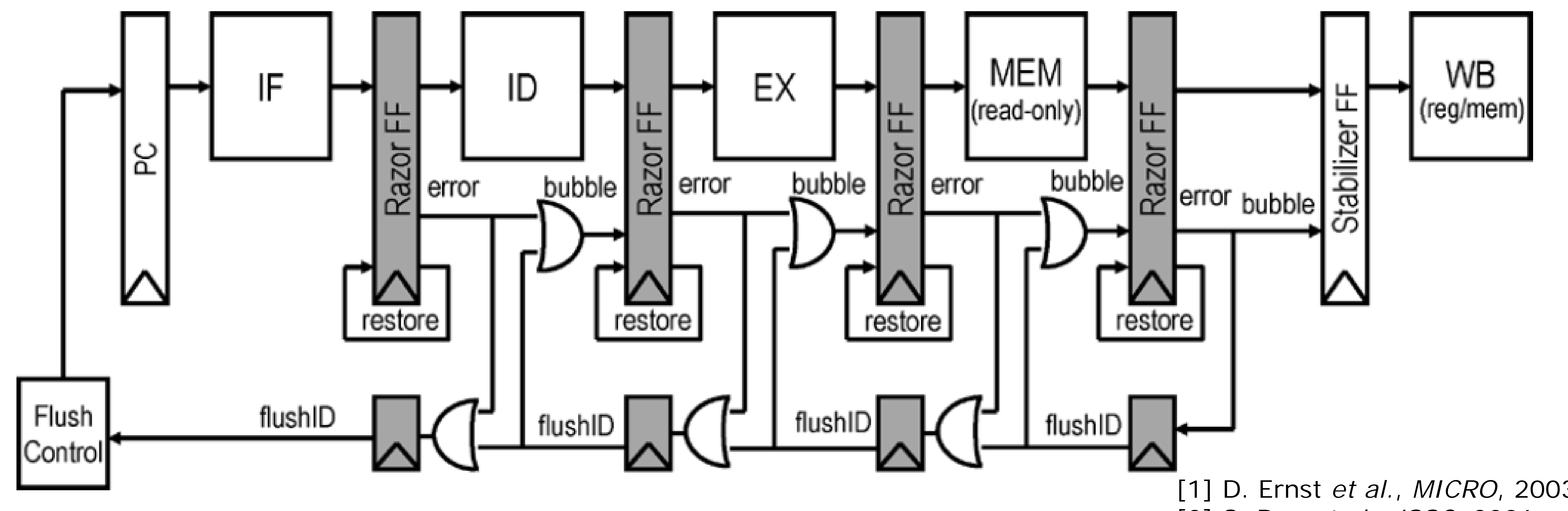
Error Recovery: Local



[1] D. Ernst *et al.*, *MICRO*, 2003.
[2] S. Das *et al.*, *JSSC*, 2006.

- Errors generate the pipeline restore to recover the correct value into the main flip-flop on the next cycle

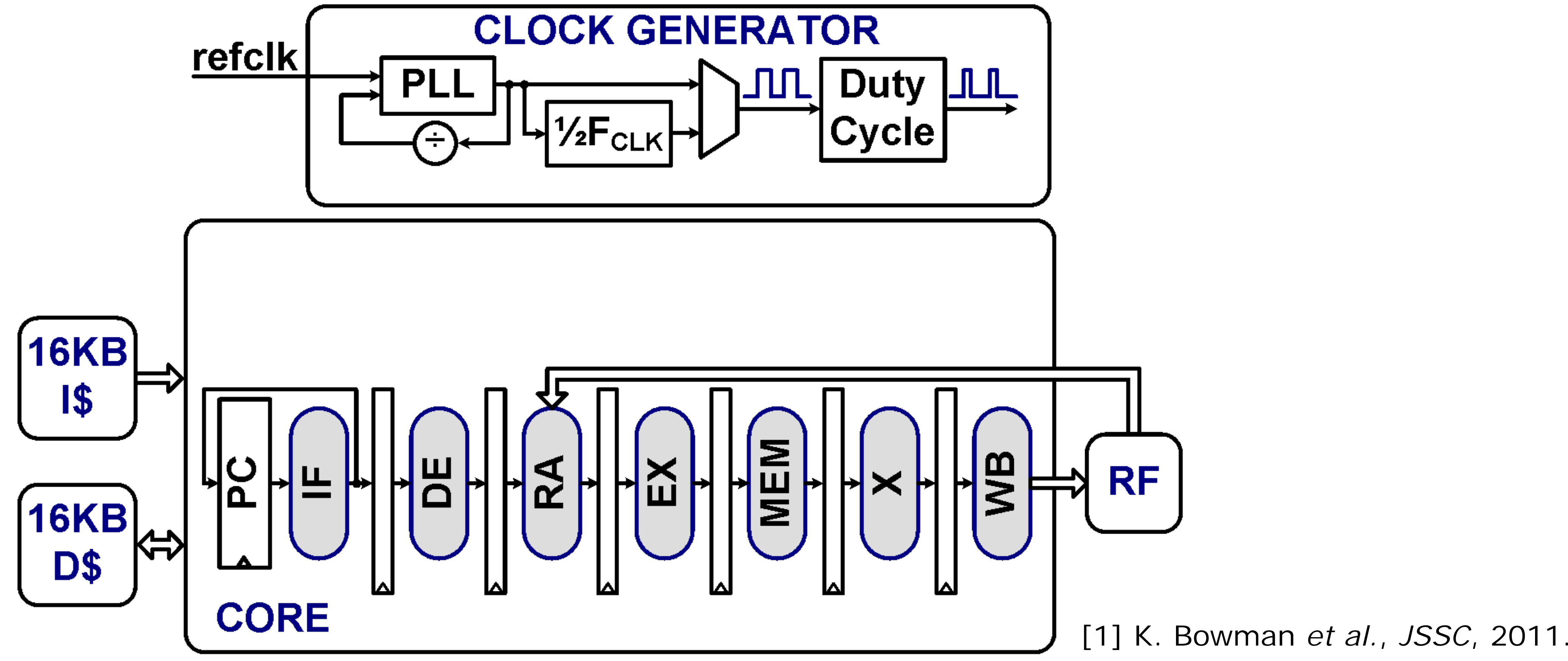
Error Recovery: Local



[1] D. Ernst *et al.*, *MICRO*, 2003.
[2] S. Das *et al.*, *JSSC*, 2006.

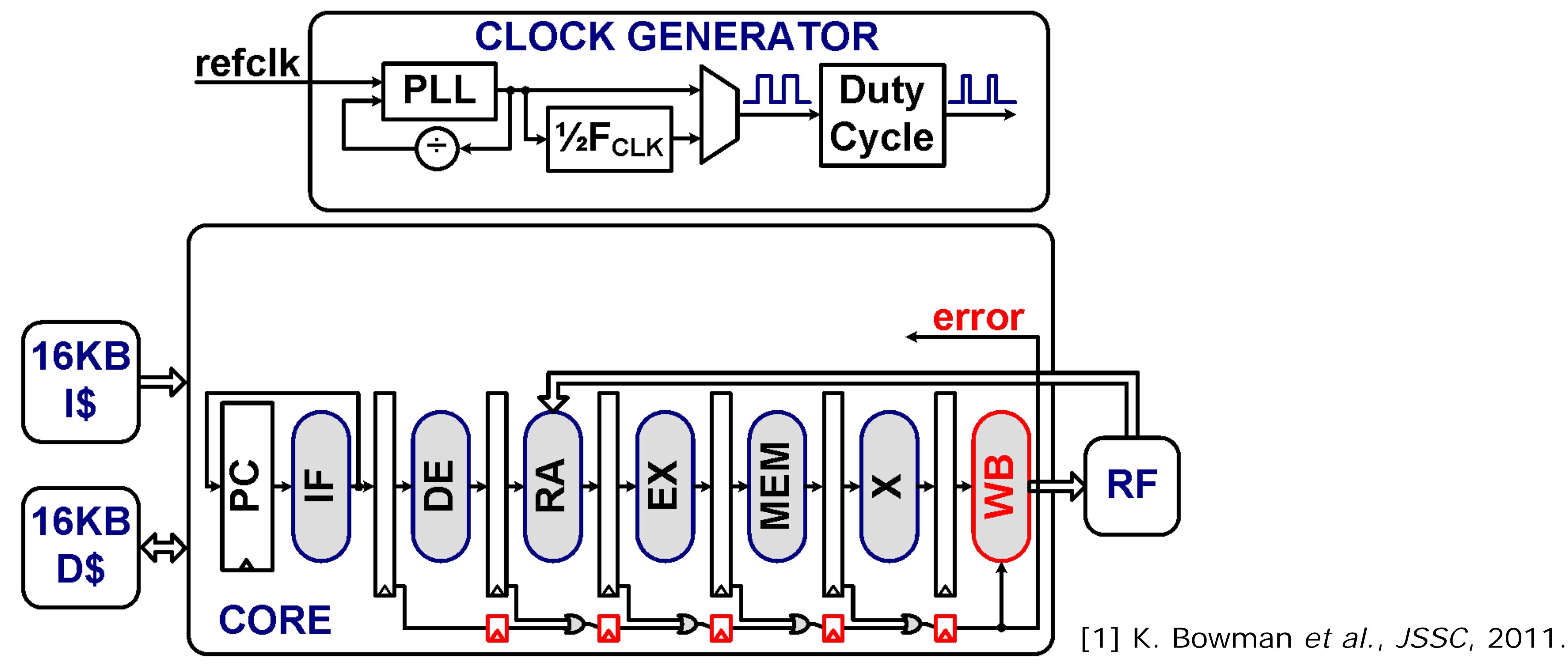
- Pipeline stage errors invalidate computation in subsequent pipeline stages & trigger an instruction flush
- Errant instruction correctly executes to allow forward progress

Error Recovery: Instruction-Replay at ½F_{CLK}



[1] K. Bowman *et al.*, *JSSC*, 2011.

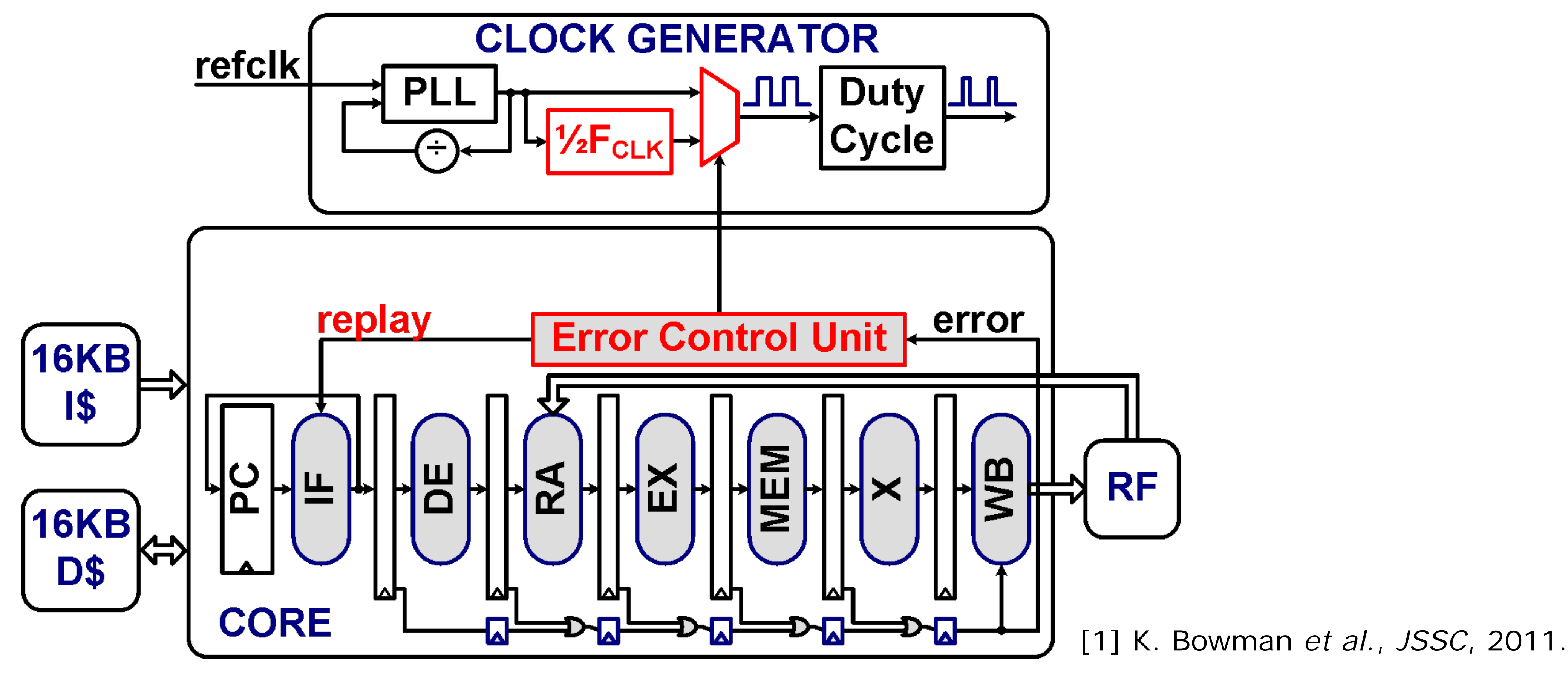
Error Recovery: Instruction-Replay at ½F_{CLK}



[1] K. Bowman *et al.*, *JSSC*, 2011.

- Pipeline errors propagate to the write-back (WB) stage to invalidate erroneous instructions

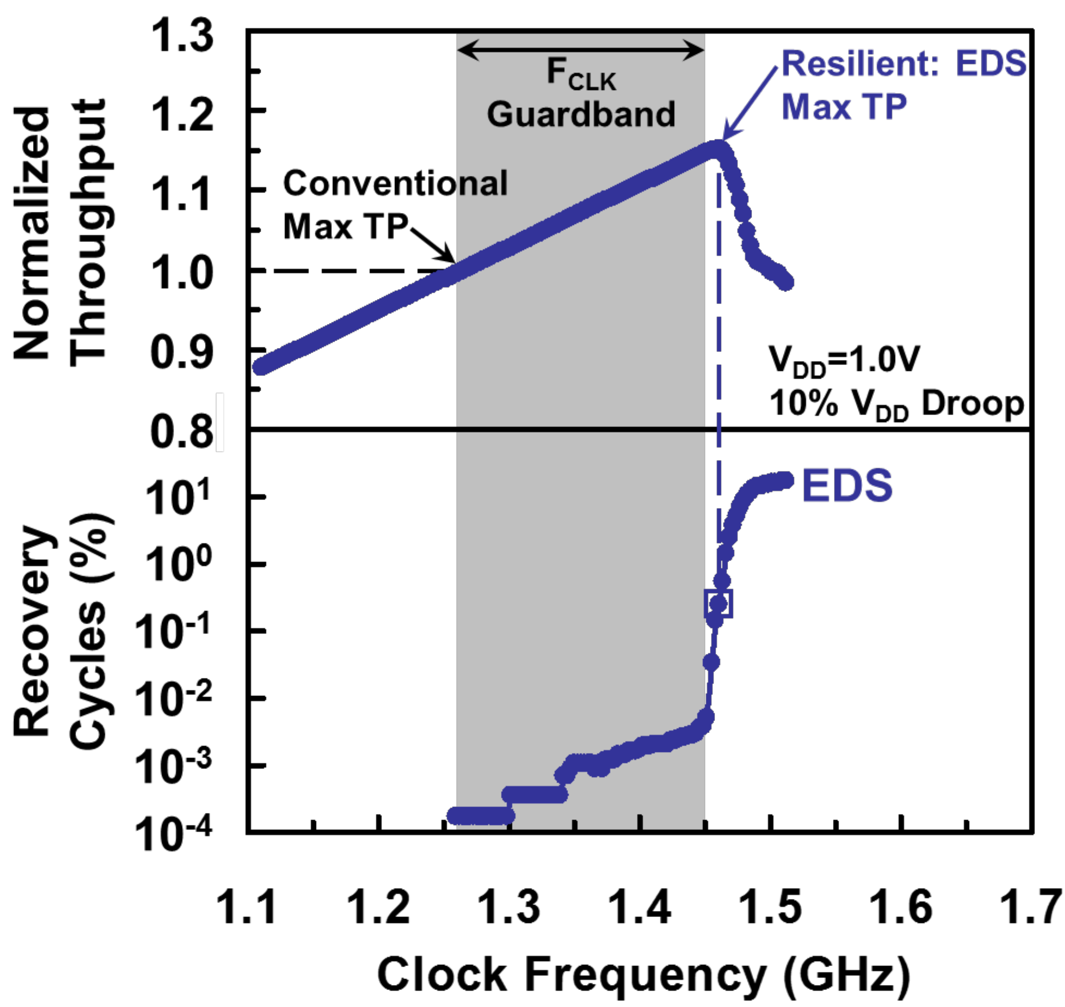
Error Recovery: Instruction-Replay at ½F_{CLK}



[1] K. Bowman *et al.*, *JSSC*, 2011.

- Error-control unit (ECU) enables recovery
- Clock high-phase delay remains unchanged at ½F_{CLK}

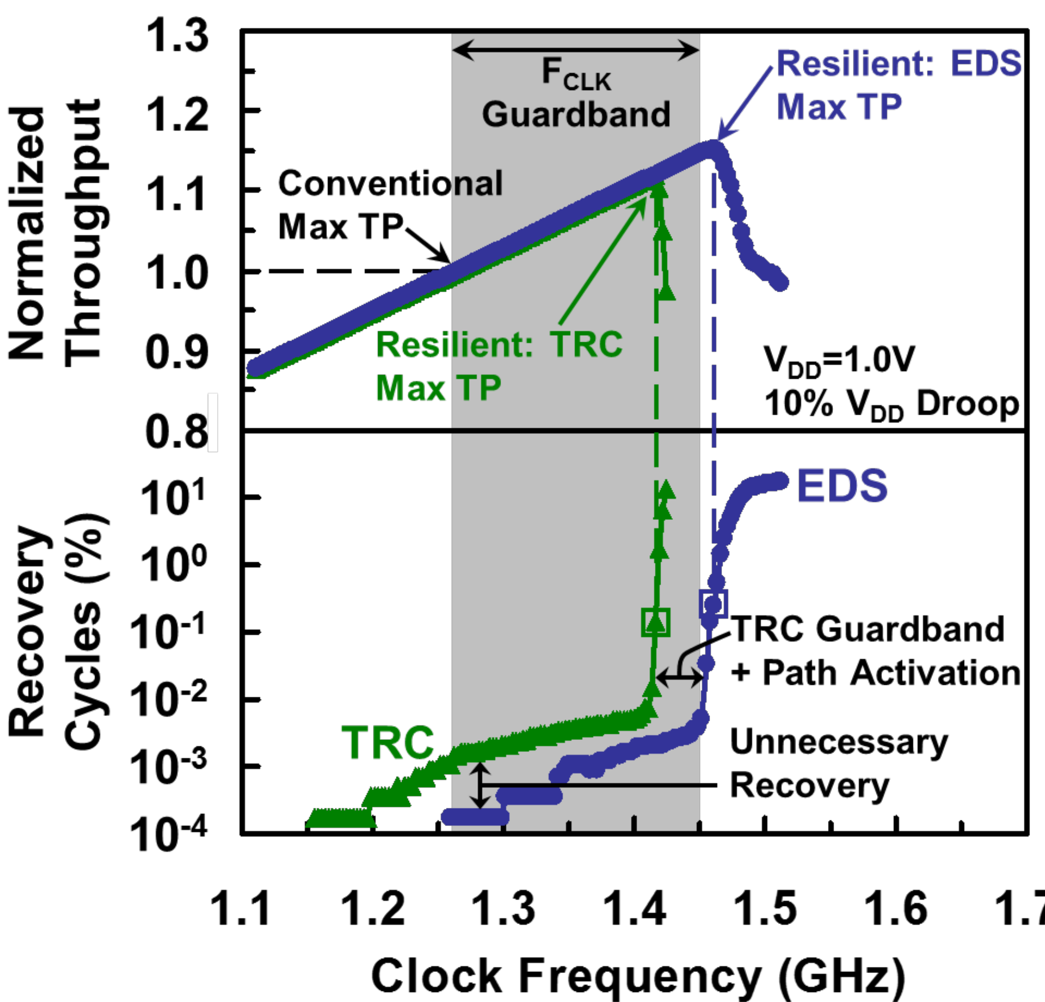
Measured Throughput (TP) versus F_{CLK}



[1] K. Bowman *et al.*, *JSSC*, 2011.

- 16% TP gain with EDS

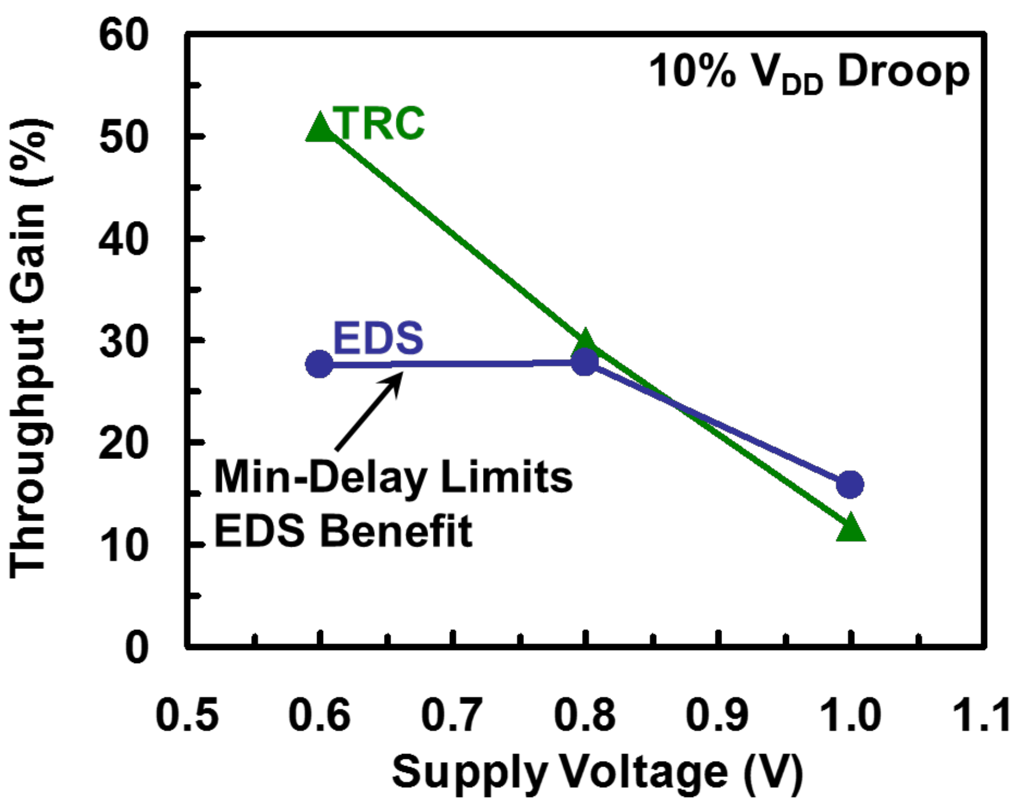
Measured Throughput (TP) versus F_{CLK}



[1] K. Bowman *et al.*, *JSSC*, 2011.

- 16% TP gain with EDS
- 12% TP gain with TRC

Measured Throughput Gain versus V_{DD}



[1] K. Bowman *et al.*, *JSSC*, 2011.

- TRC TP gains exceed EDS TP gains at low V_{DD}
- Error-detection window determines EDS & TRC TP benefits
- Core min-delay paths limit EDS error-detection window

Adaptive Design versus Resilient Design

- Traditional Adaptive Design:
  - \+ Low overhead
  - — Response time limits benefits

- Resilient Design:
  - \+ Relaxes the response-time constraint
  - — Design complexity for implementing error recovery into a high-performance processor

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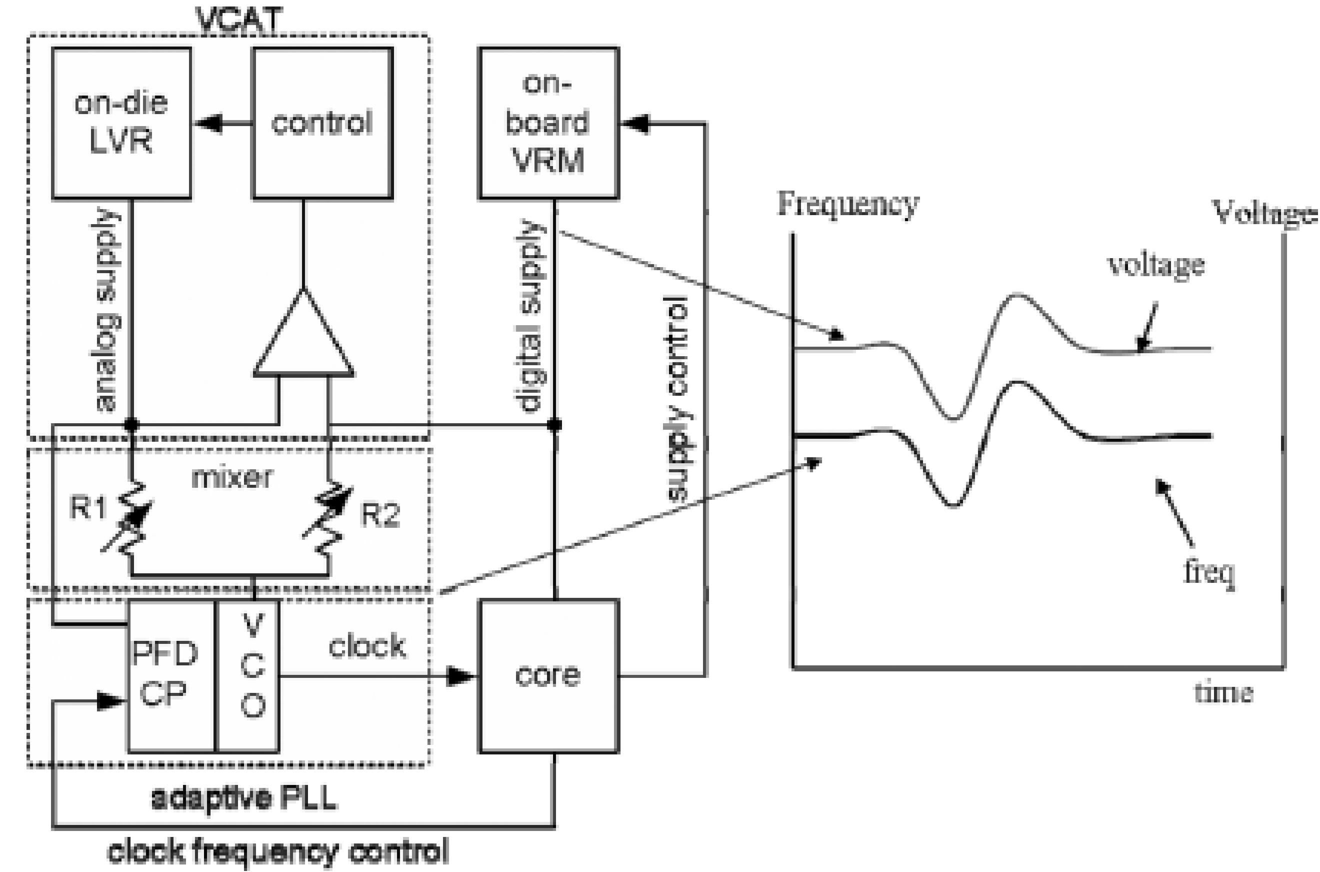
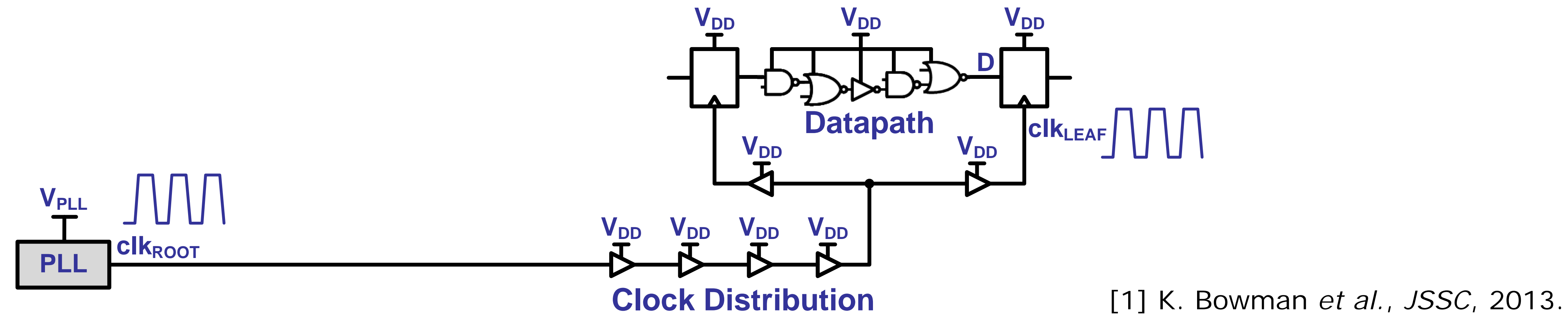
Adaptive Frequency System



[1] N. Kurd *et al.*, *JSSC*, 2009.

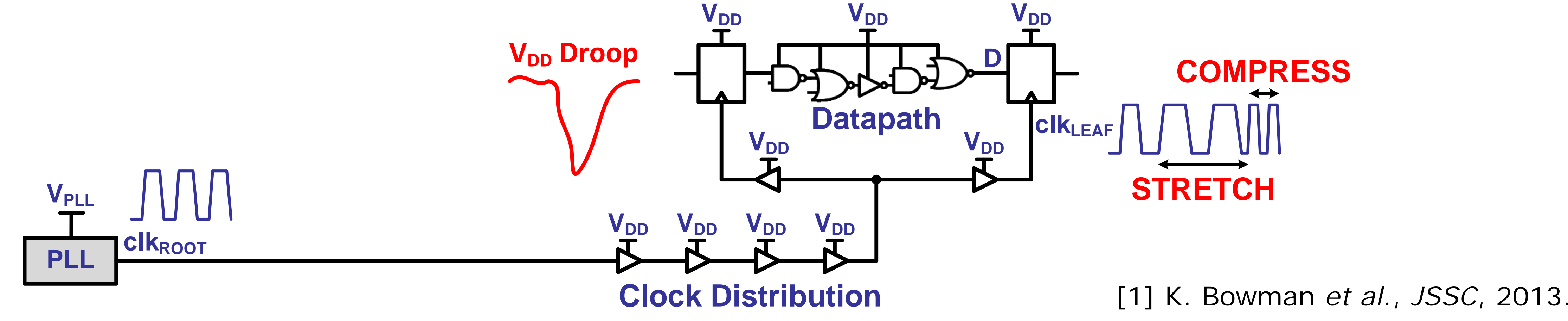
- Adapt PLL clock output with core V_{DD} changes
- Analog circuit complexities limit benefits

Adaptive Clock Distribution (ACD)



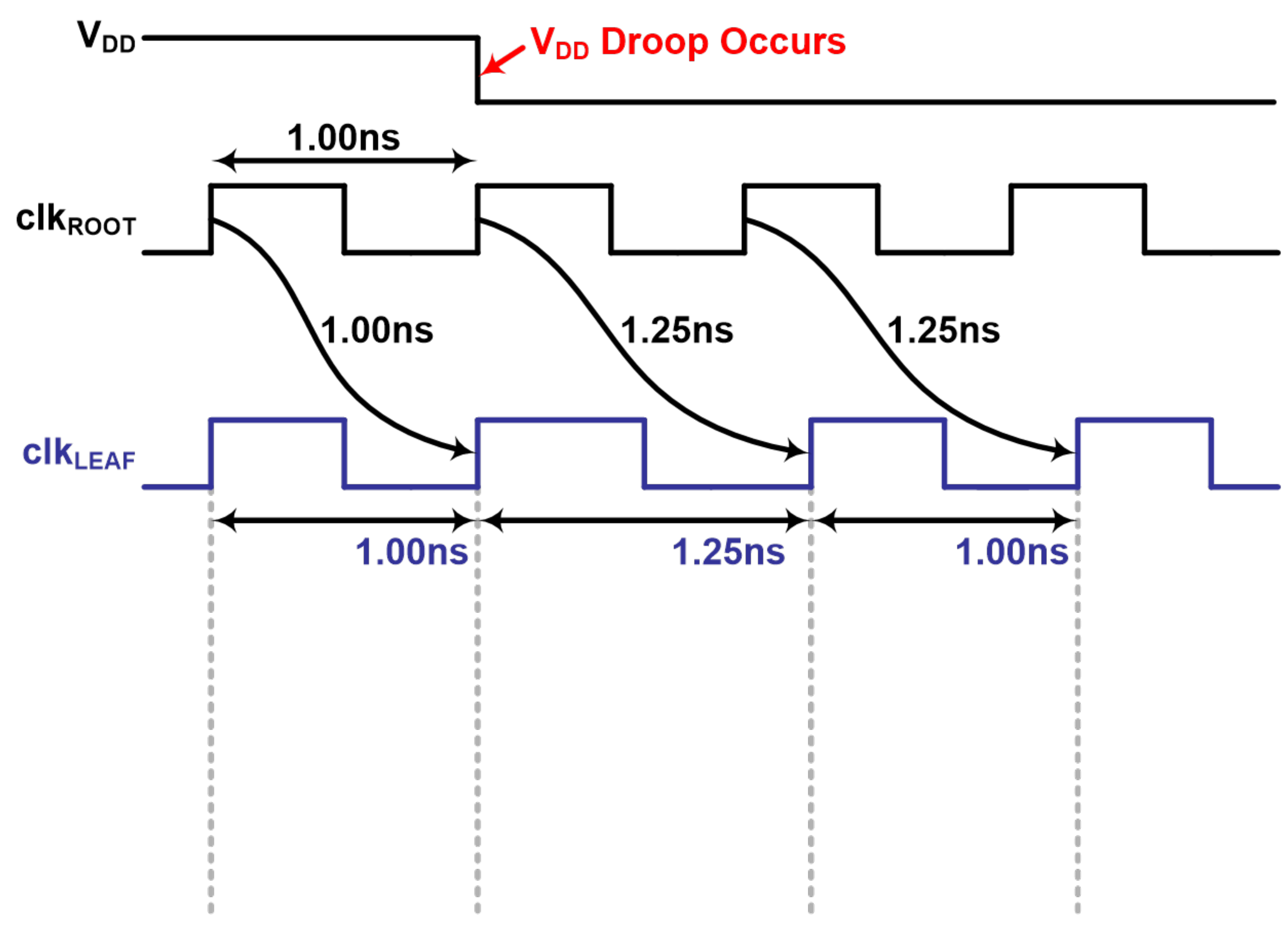
- V_{DD} droops impact datapath & clock distribution timing

Adaptive Clock Distribution (ACD)

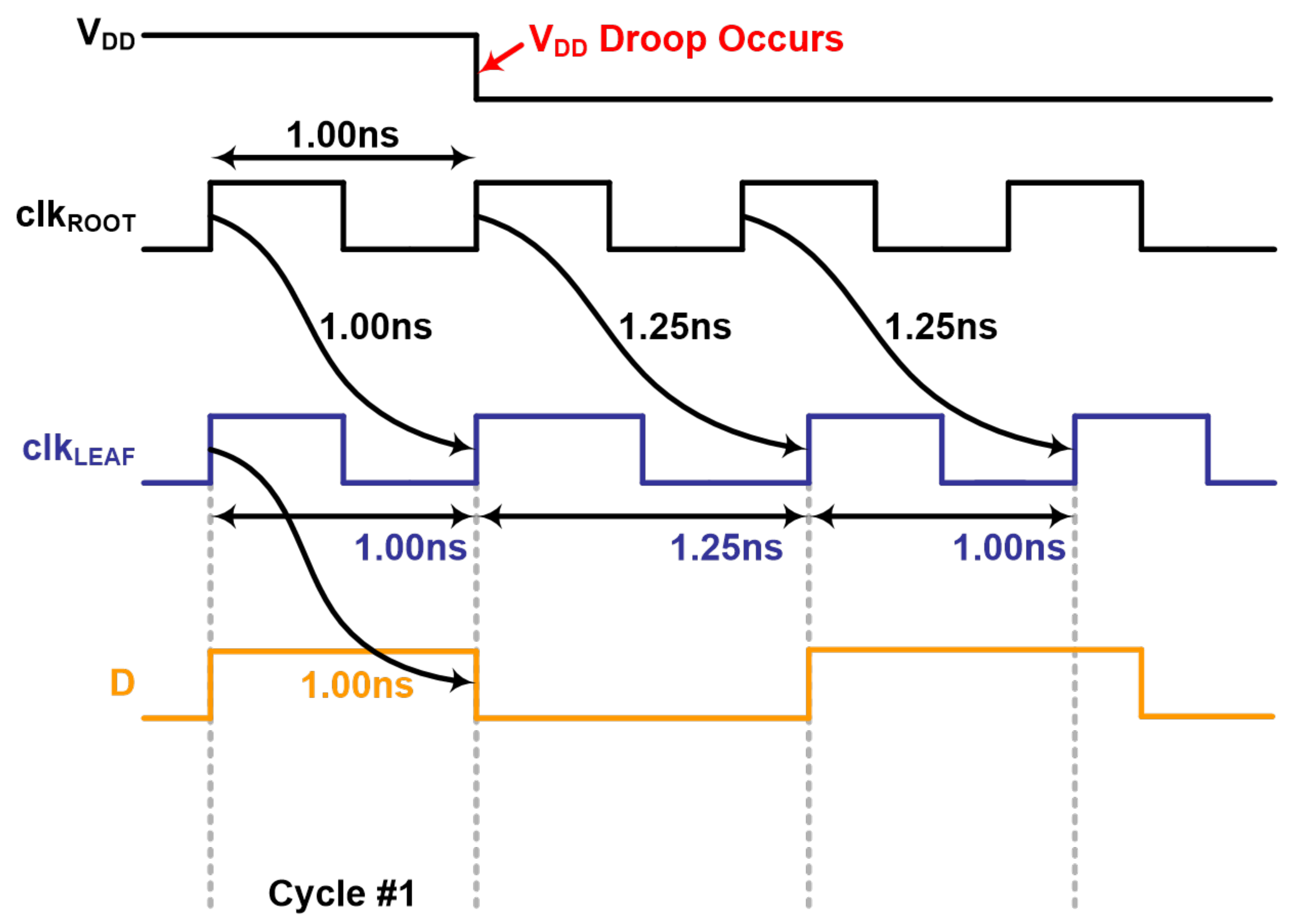


- V_{DD} droops impact datapath & clock distribution timing
- Clock-data compensation temporarily occurs
  - As V_{DD} ramps down, the clock period stretches & compensates for the slower datapath delay
  - As V_{DD} ramps up, the datapath delay is faster & compensates for the clock period compression

Clock-Data Compensation



Clock-Data Compensation



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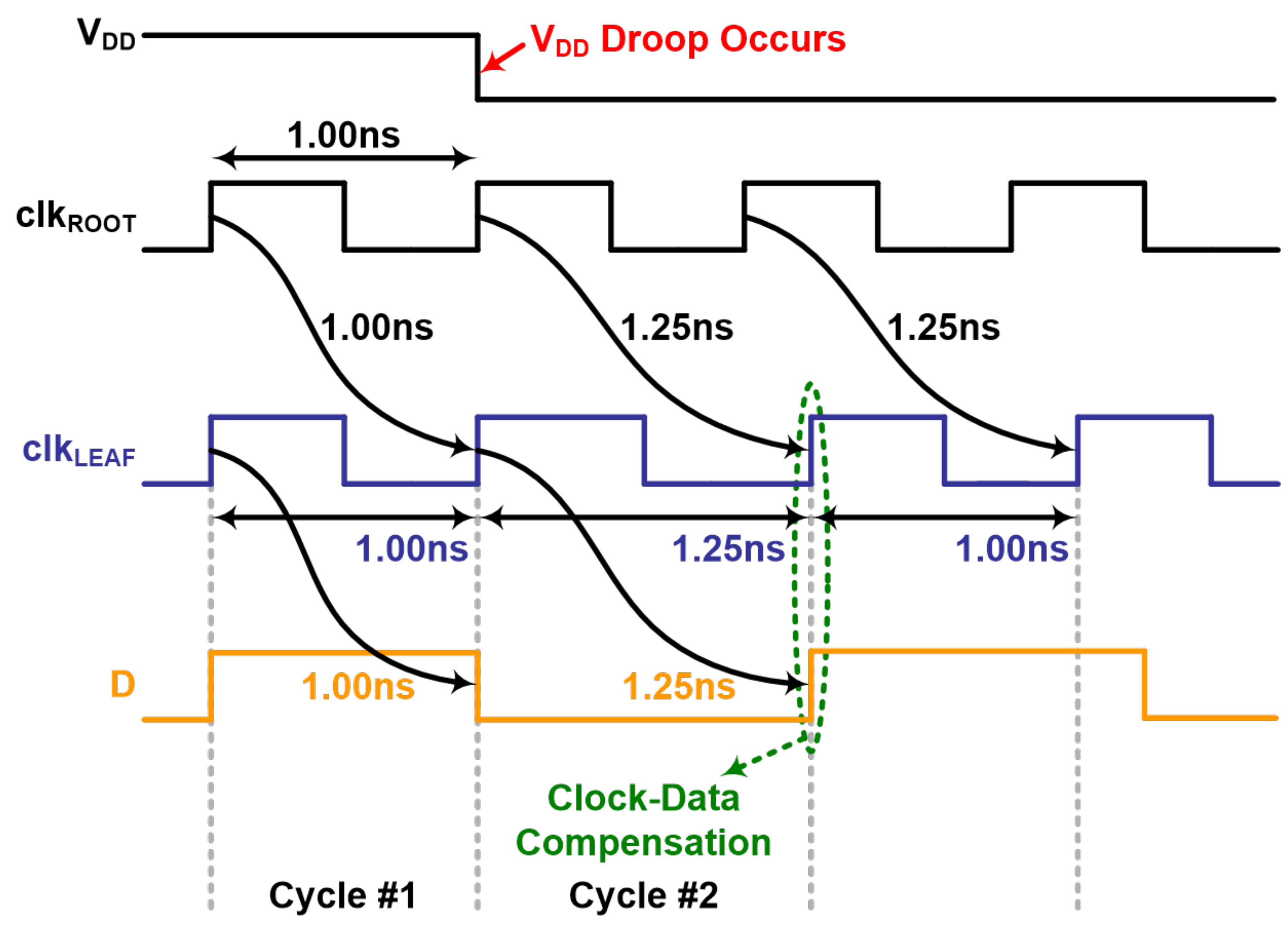
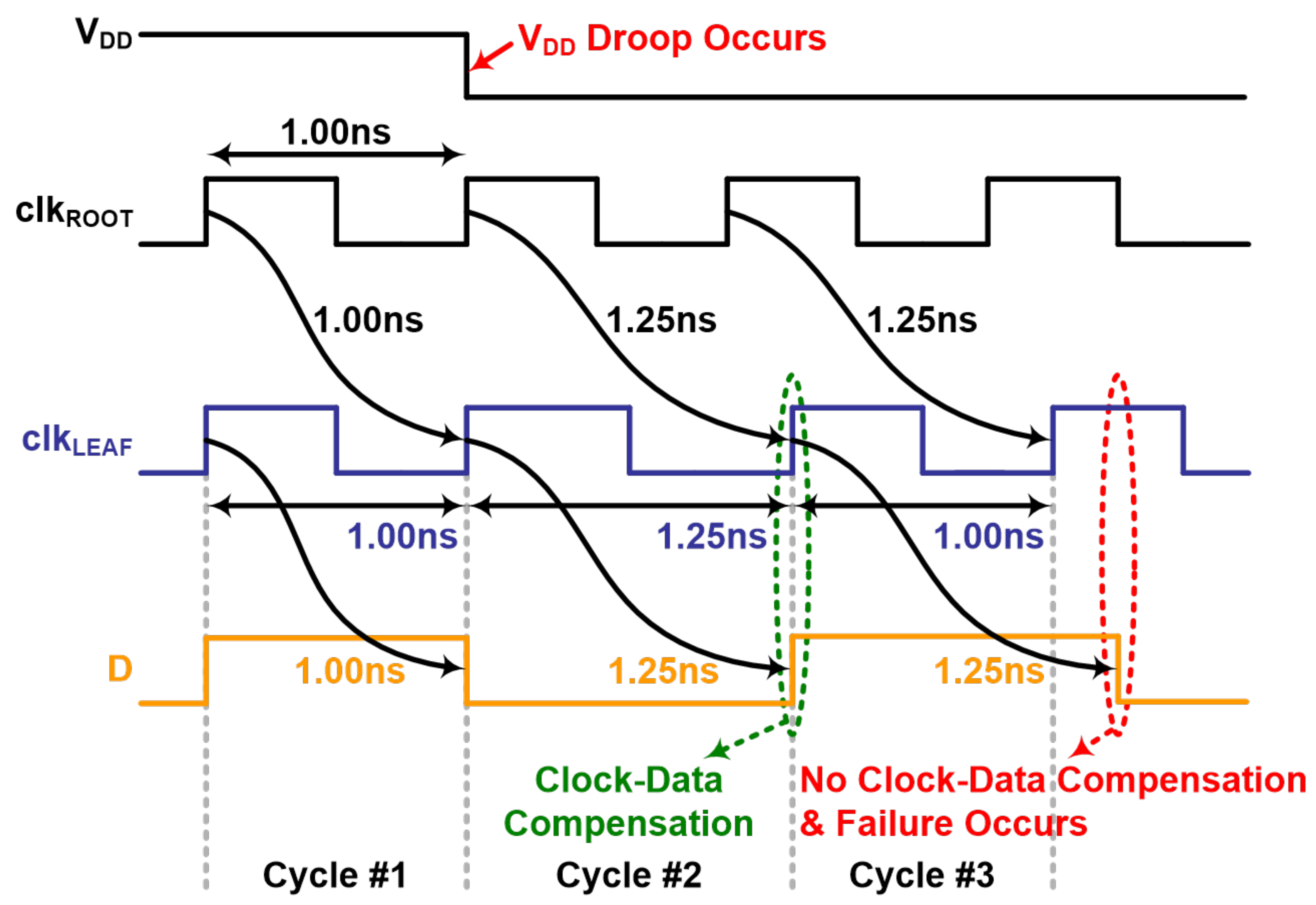
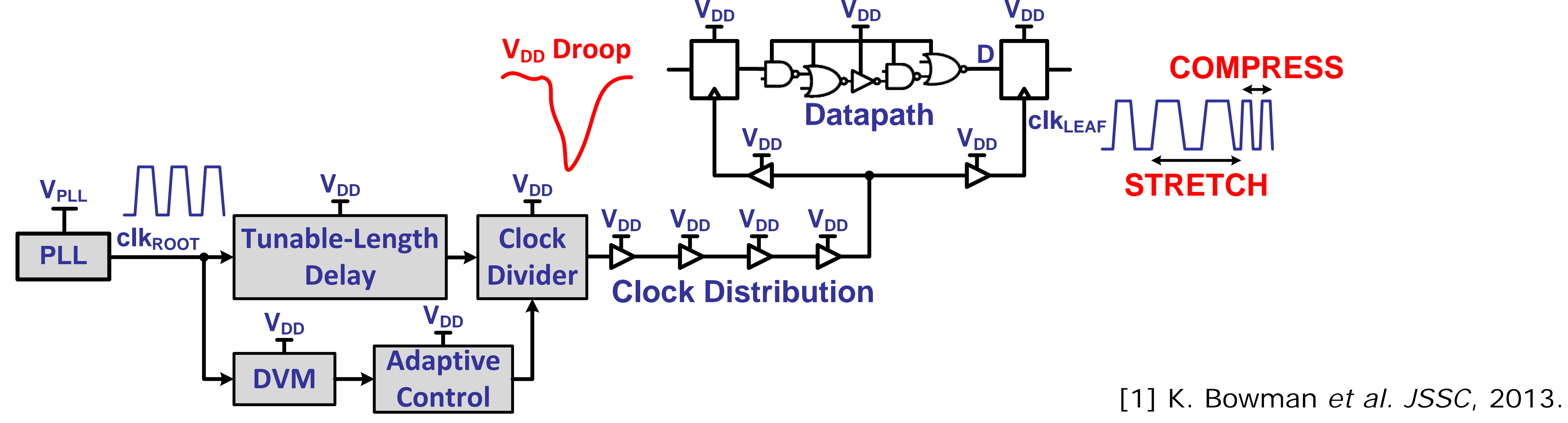


Clock-Data Compensation



Adaptive Clock Distribution (ACD)



[1] K. Bowman *et al. JSSC*, 2013.

- Key Idea: Exploit clock-data delay compensation during a V_{DD} droop to provide a response time for adaptation
- Primary Design Components: Tunable-length delay (TLD), dynamic variation monitor (DVM), adaptive control, & clock divider

Initial ACD Designs [1]-[2]

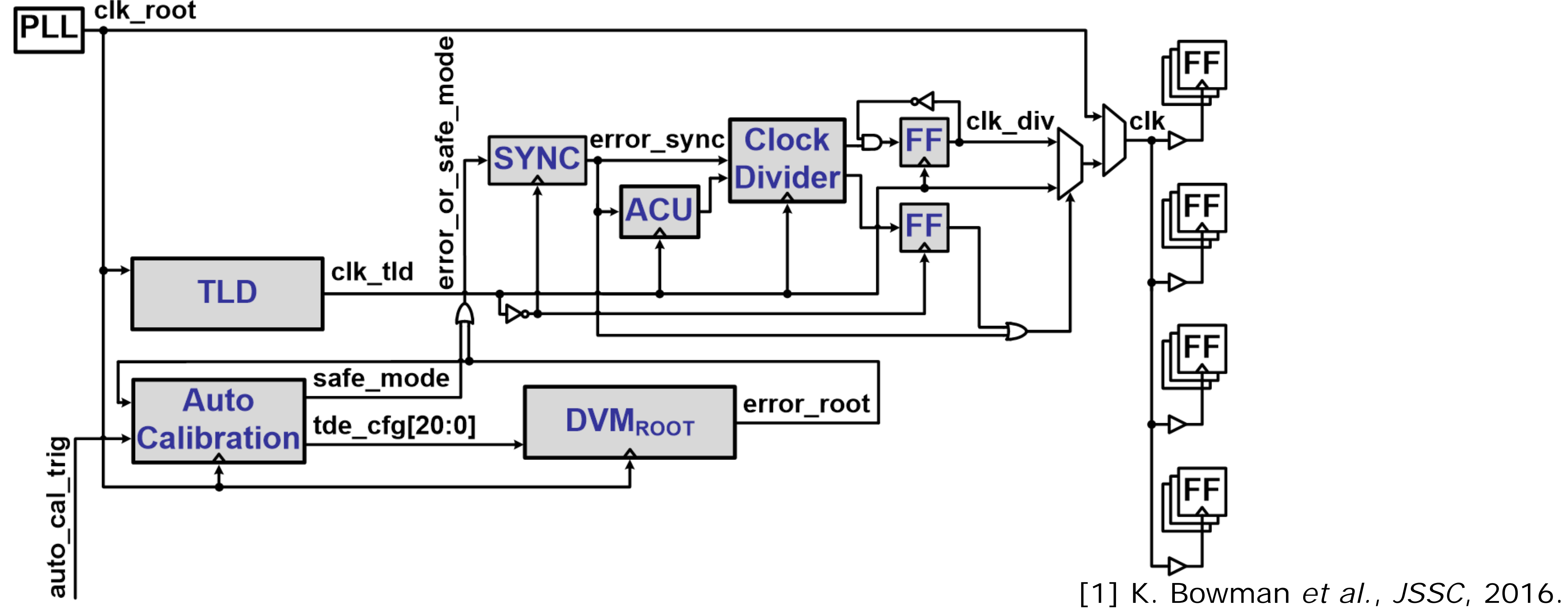
+ Mitigate impact of V_{DD} droops on performance & energy efficiency for a wide range of V_{DD} & F_{CLK}

— DVM requires calibration

- Extensive tester calibration to support a wide range of F_{CLK}, V_{DD}, temperature, & process conditions
- Prohibitively expensive test time for high-volume products

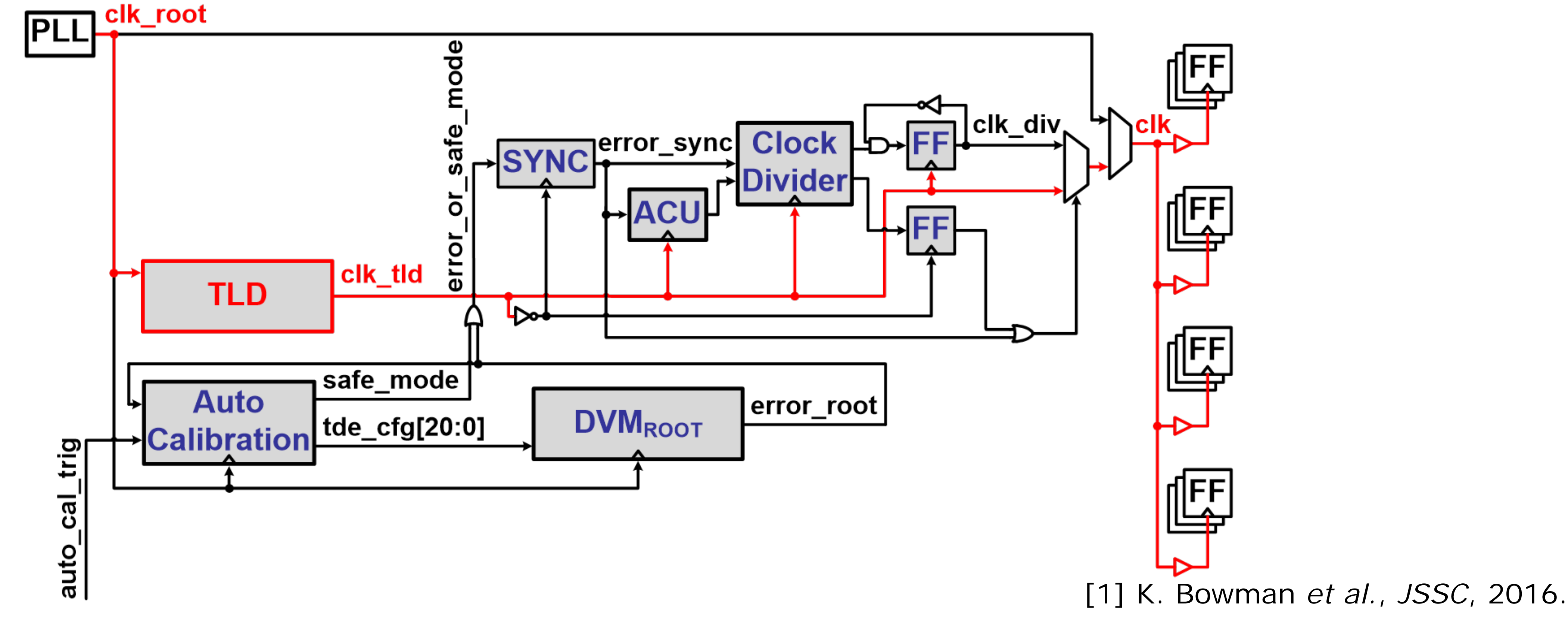
[1] K. Bowman *et al.*, *JSSC*, 2013.
[2] C. Tokunaga *et al.*, *ISSCC*, 2014.

Auto-Calibrating ACD



[1] K. Bowman *et al.*, *JSSC*, 2016.

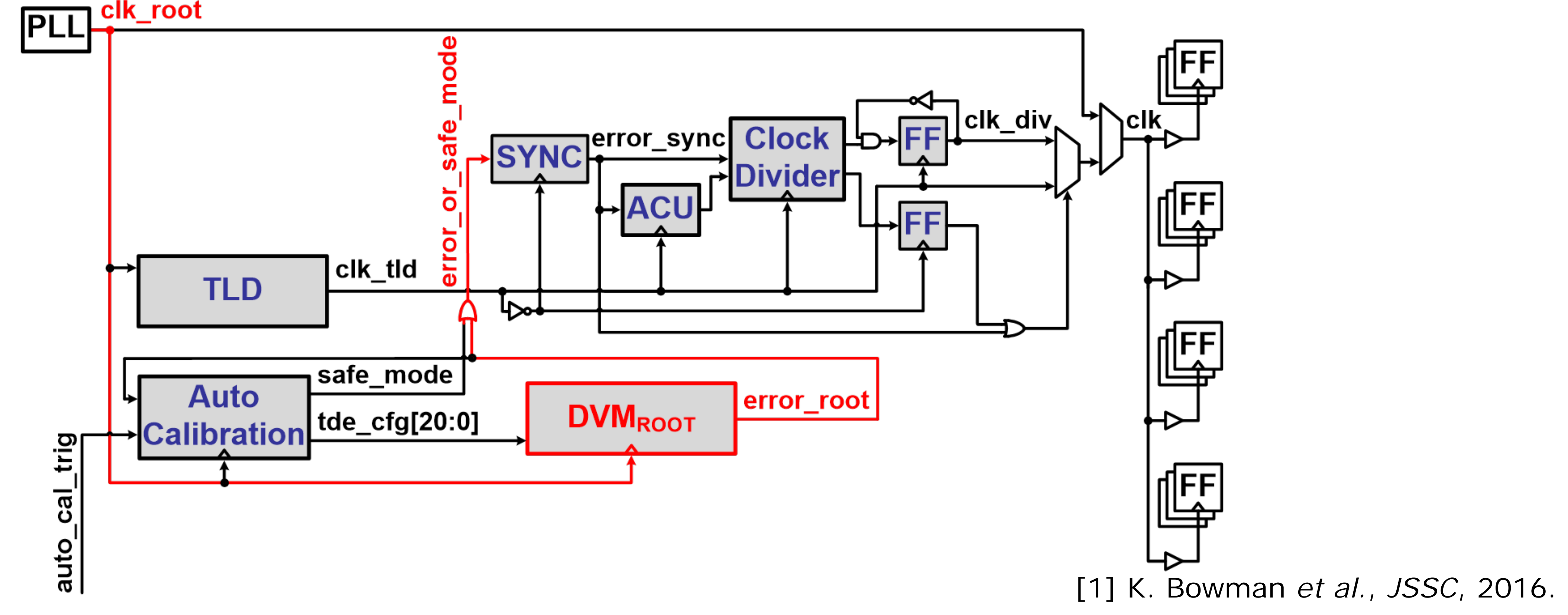
Auto-Calibrating ACD



[1] K. Bowman *et al.*, *JSSC*, 2016.

1) TLD provides the response time

Auto-Calibrating ACD

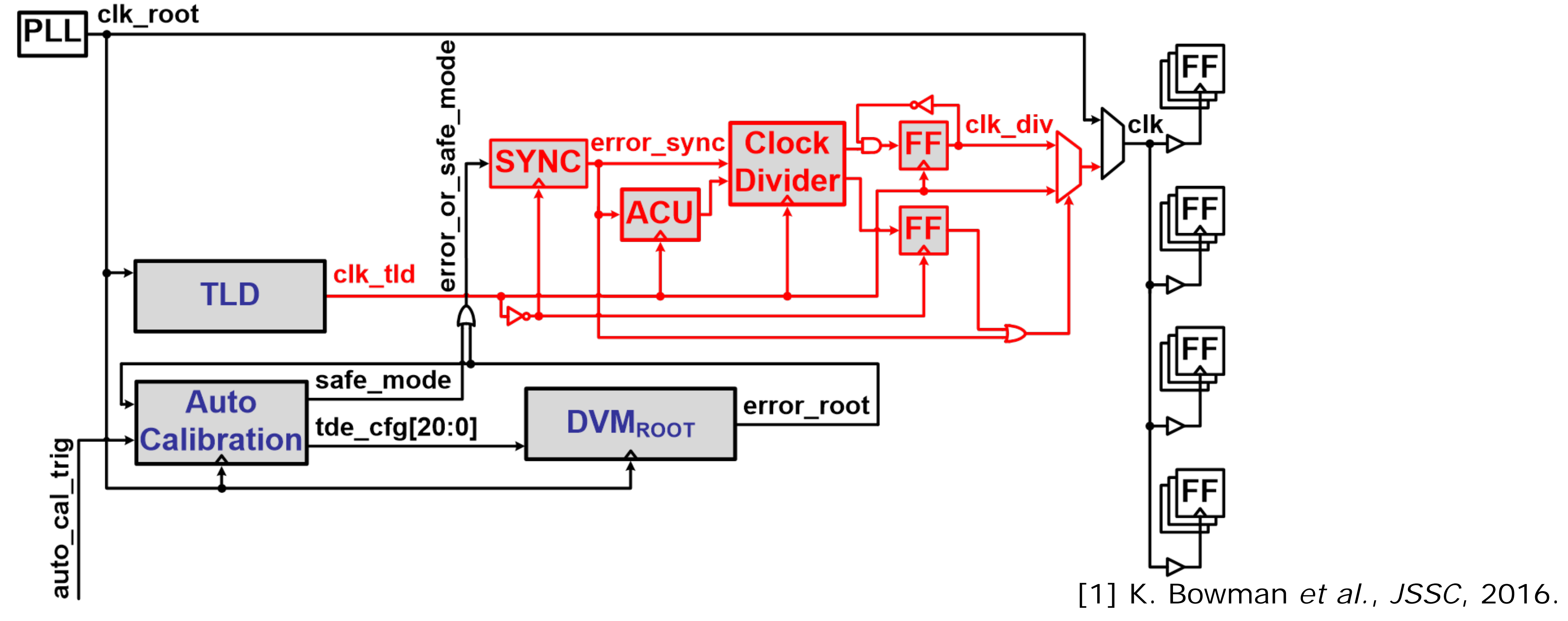


[1] K. Bowman *et al.*, *JSSC*, 2016.

1) TLD provides the response time

2) DVM_{ROOT} detects the onset of a V_{DD} droop

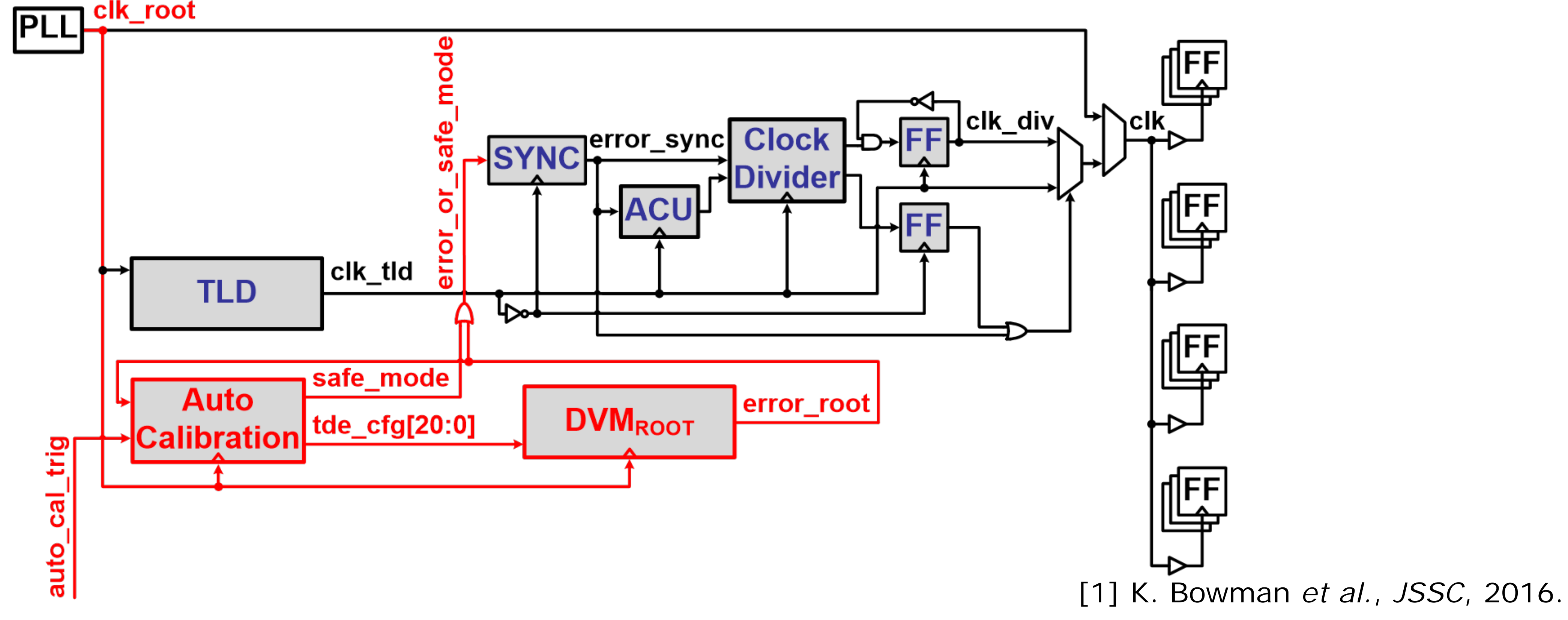
Auto-Calibrating ACD



[1] K. Bowman *et al.*, *JSSC*, 2016.

1) TLD provides the response time
2) DVM_{ROOT} detects the onset of a V_{DD} droop
3) Adaptive control unit (ACU) & clock divider reduce F_{CLK} in half

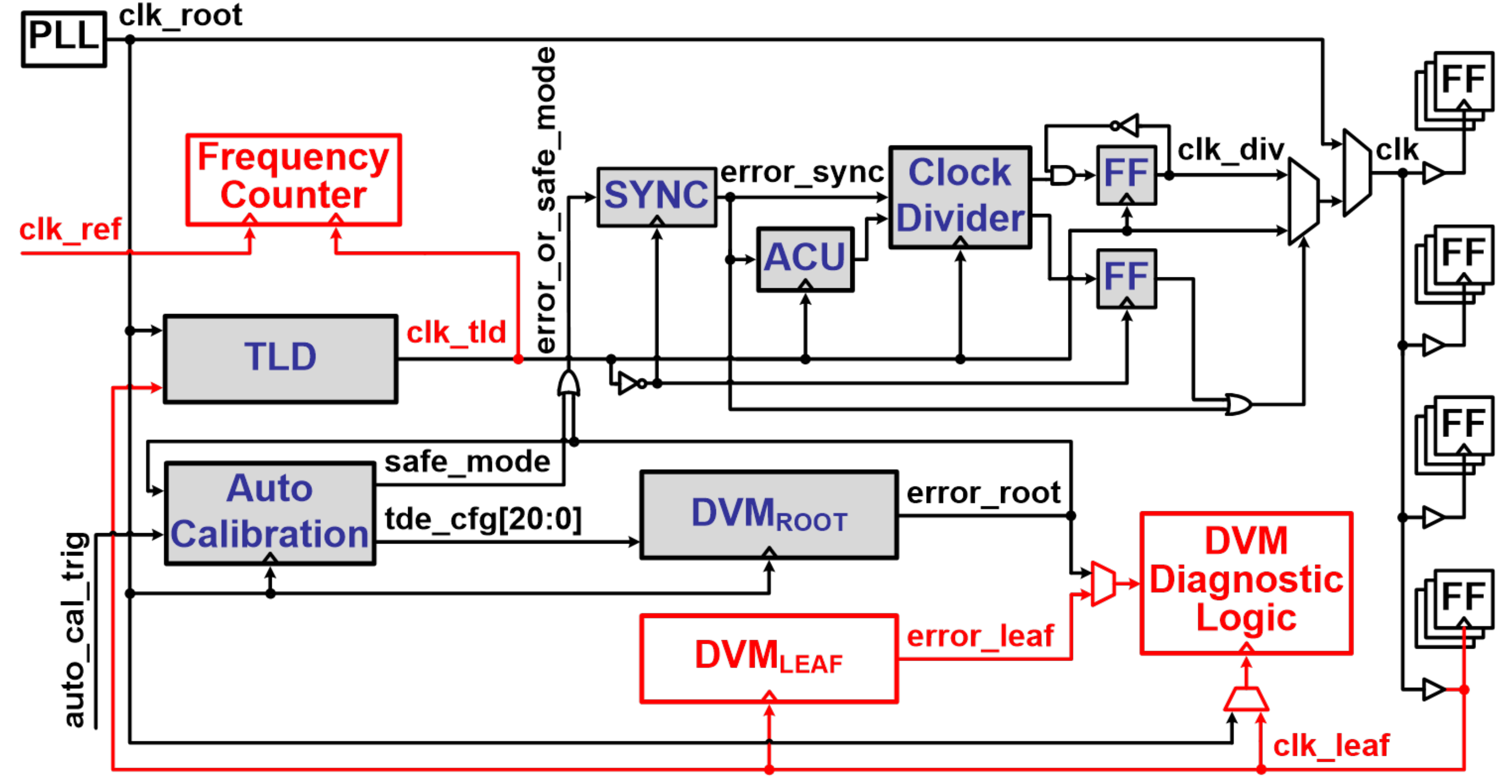
Auto-Calibrating ACD



[1] K. Bowman *et al.*, *JSSC*, 2016.

- Auto-calibration circuit optimally configures the DVM in-field to maximize the ACD benefits

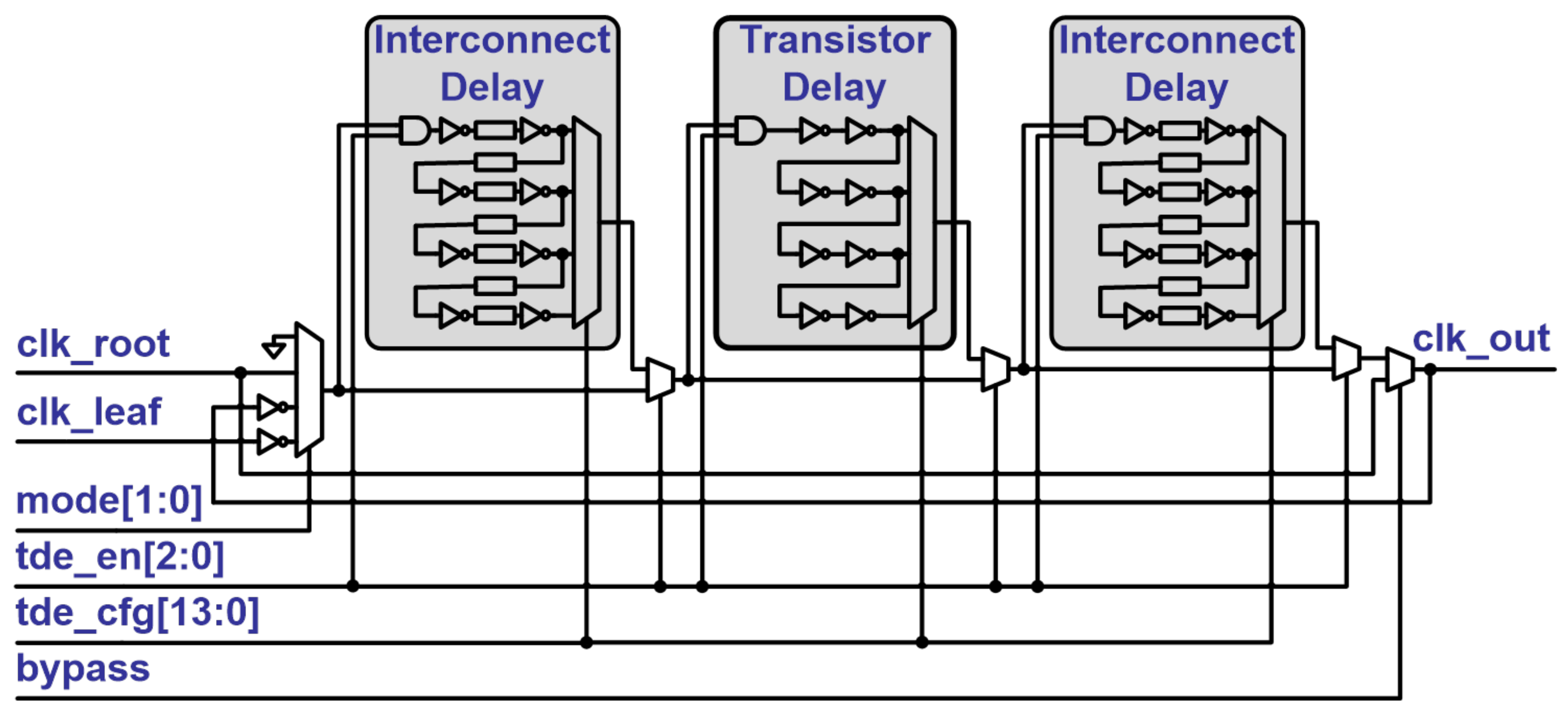
Auto-Calibrating ACD



[1] K. Bowman *et al.*, *JSSC*, 2016.

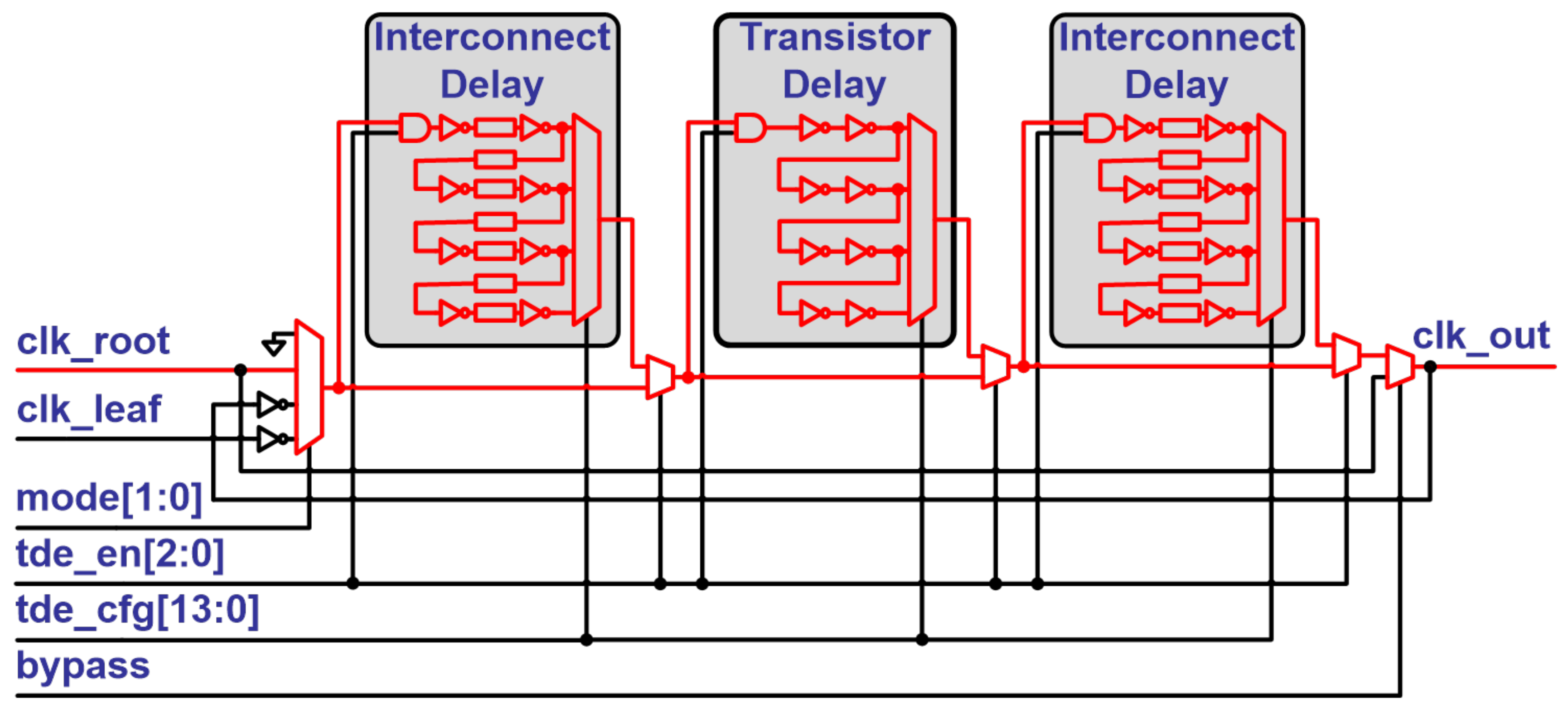
- Frequency counter enables TLD calibration
- DVM_{LEAF} & diagnostic logic allows on-die observability

Tunable-Length Delay (TLD)



[1] K. Bowman *et al.*, *JSSC*, 2016.

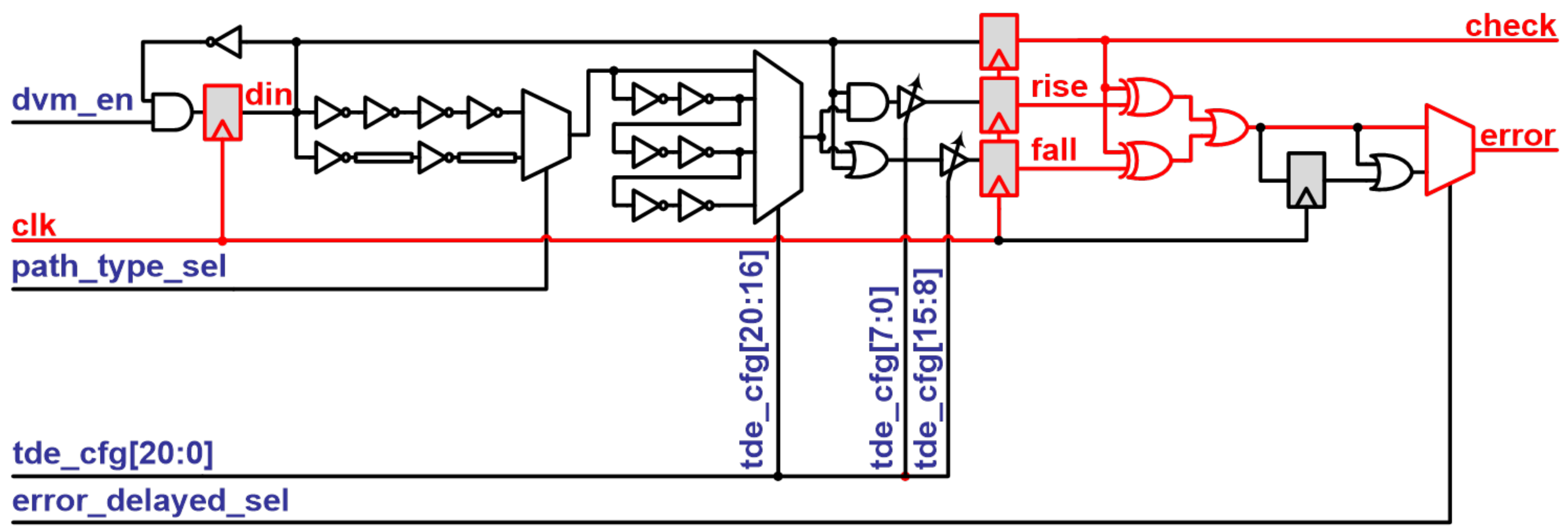
Tunable-Length Delay (TLD)



[1] K. Bowman *et al.*, *JSSC*, 2016.

- Extends delay & changes delay sensitivity to V_{DD}
- Prolongs clock-data delay compensation during V_{DD} droop to provide the response time for adaptation

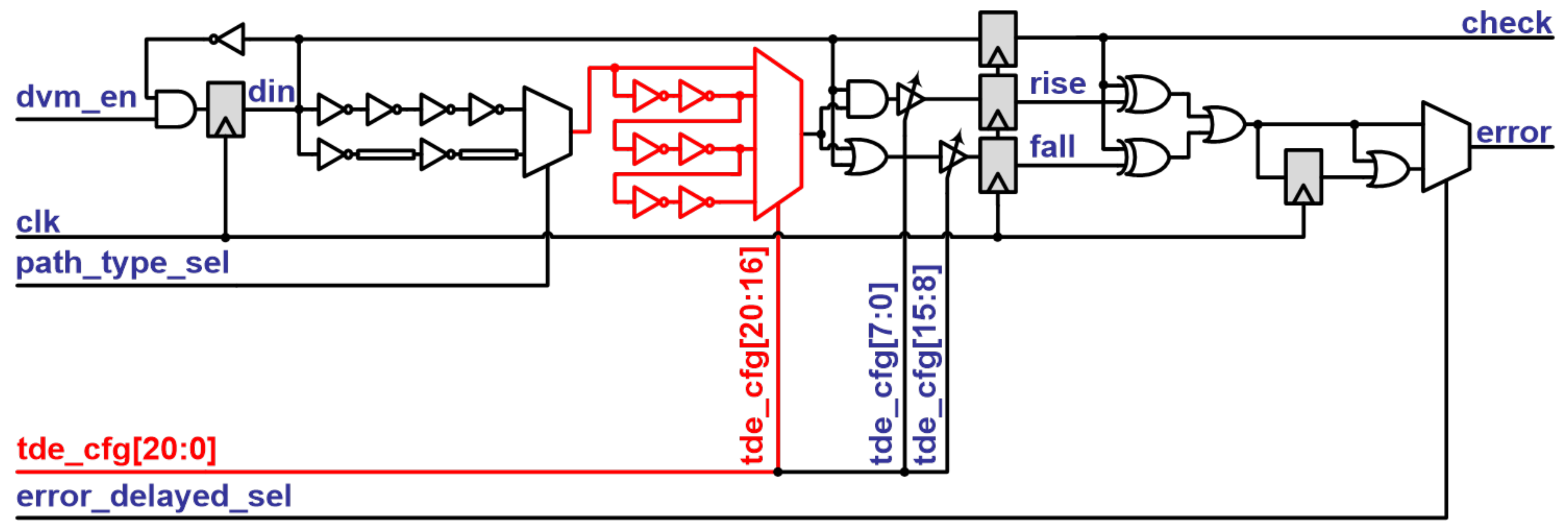
Dynamic Variation Monitor (DVM)



[1] K. Bowman *et al.*, *JSSC*, 2016.

- Measures critical-path timing margin every cycle

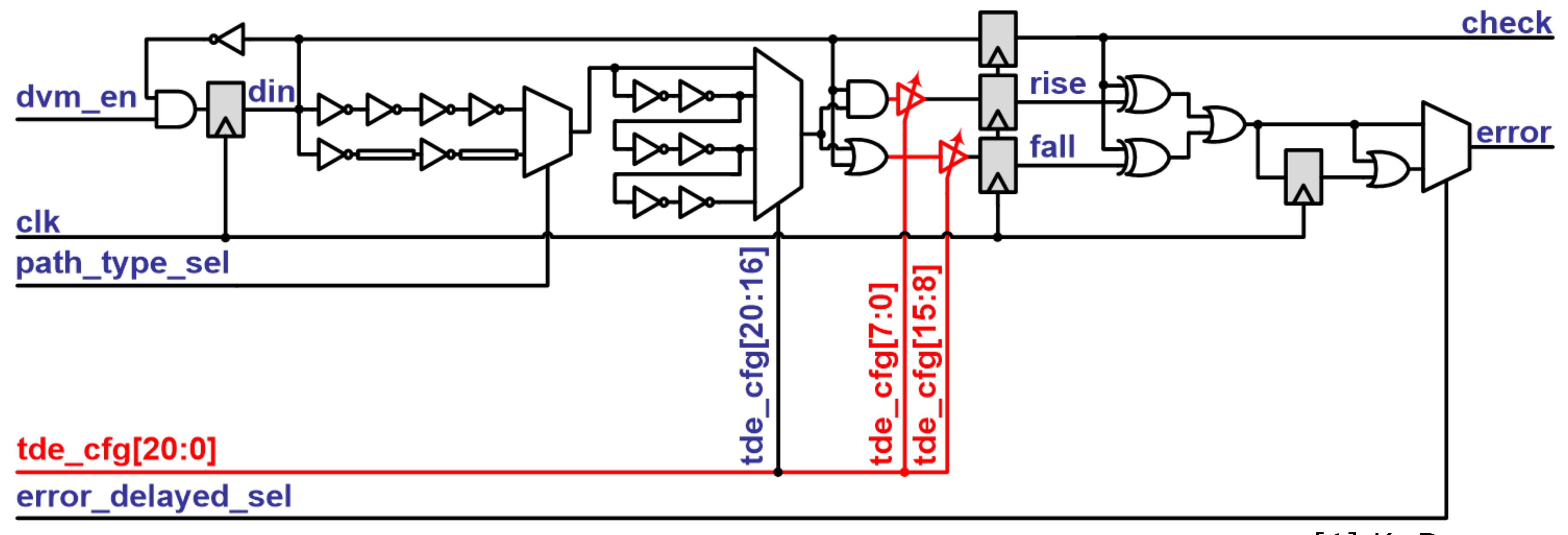
Dynamic Variation Monitor (DVM)



[1] K. Bowman *et al.*, *JSSC*, 2016.

- Measures critical-path timing margin every cycle
- Large tunable-delay elements (TDEs):
  - Provides wide tuning range (± 40% of cycle time)

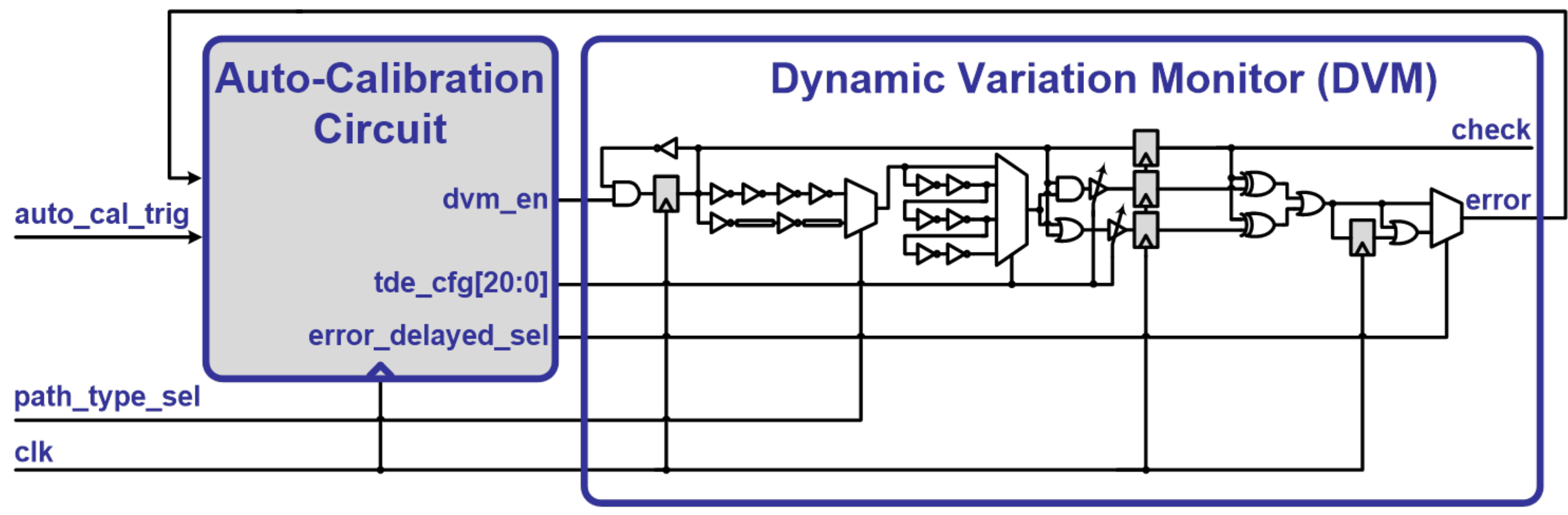
Dynamic Variation Monitor (DVM)



[1] K. Bowman *et al.*, *JSSC*, 2016.

- Measures critical-path timing margin every cycle
- Large tunable-delay elements (TDEs):
  - Provides wide tuning range (± 40% of cycle time)
- Small tunable-delay elements (TDEs):
  - Provides high resolution tuning (<0.5% of cycle time)

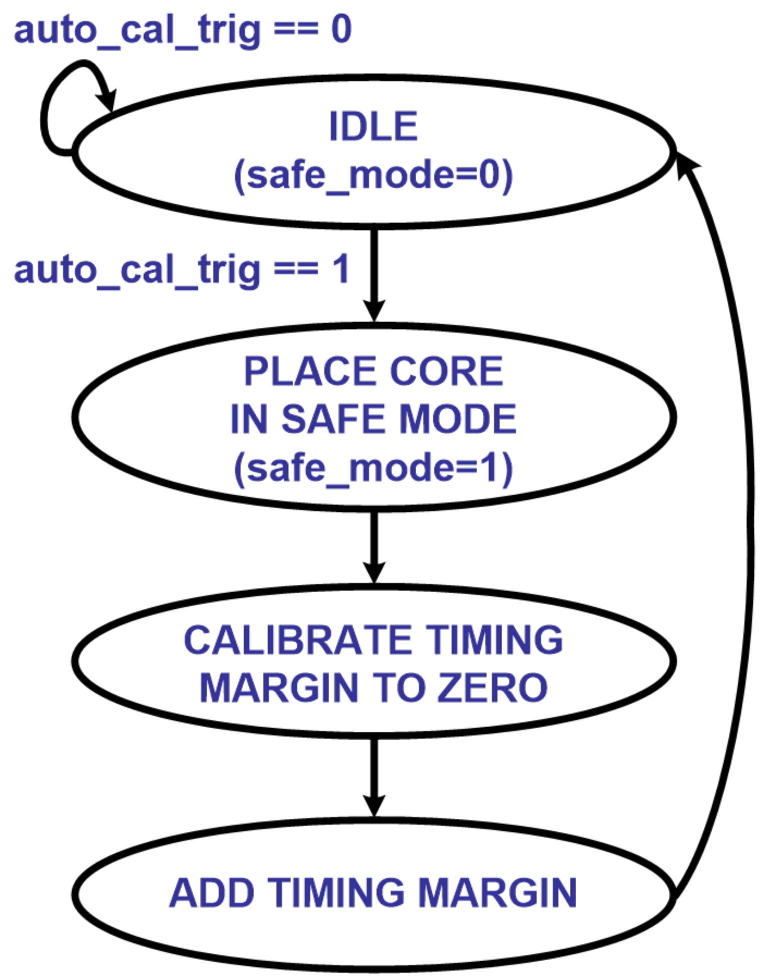
DVM Auto-Calibration Circuit



[1] K. Bowman *et al.*, *JSSC*, 2016.

- Auto-calibration circuit directly interfaces to the DVM
- Enables in-field, low-latency optimal DVM calibration for any F_{CLK}, V_{DD}, or temperature to maximize ACD benefits
- Eliminates lookup tables & reduces ACD calibration time at test

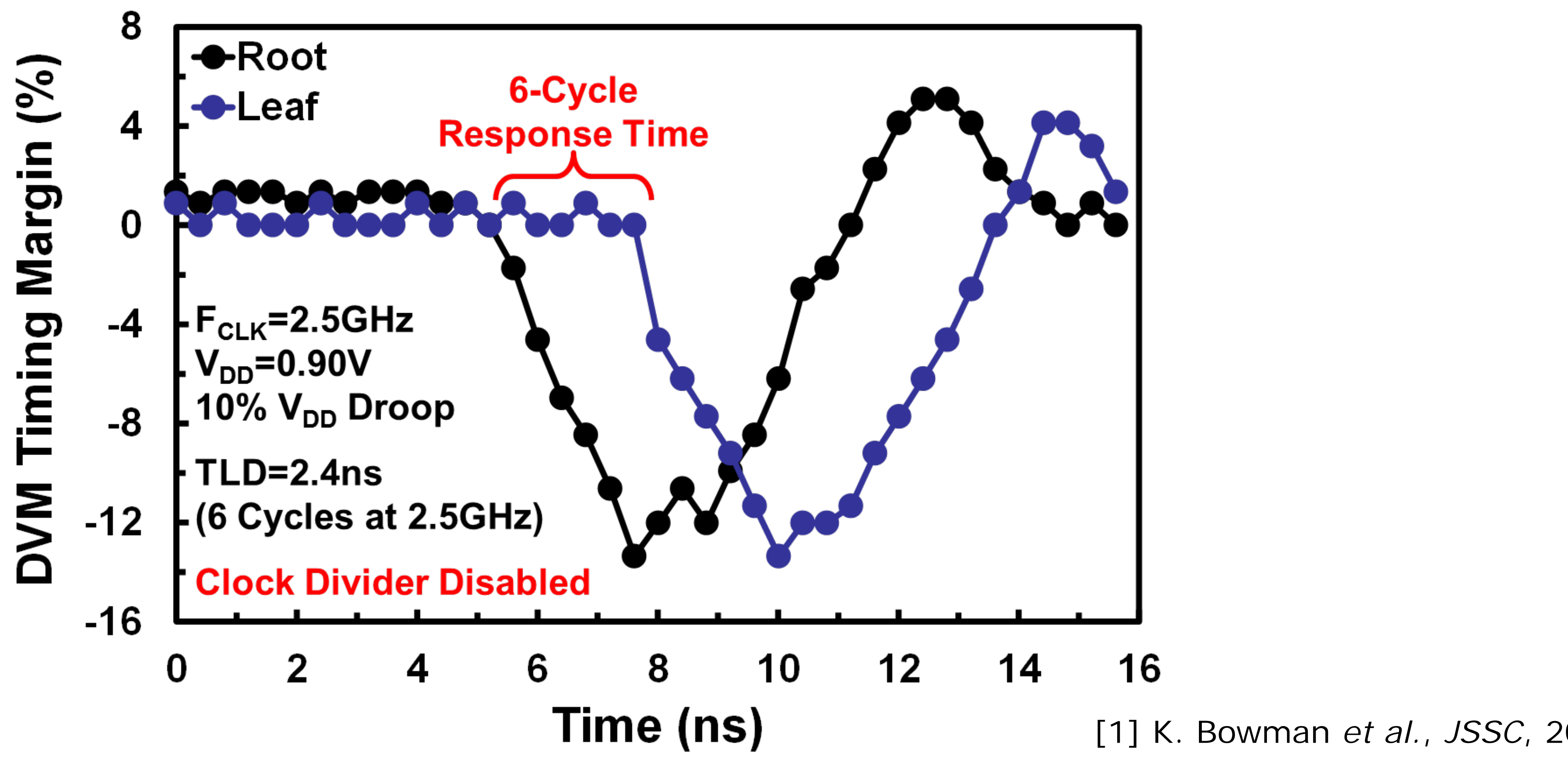
DVM Auto-Calibration Circuit State Diagram



[1] K. Bowman *et al.*, *JSSC*, 2016.

- Calibrates DVM at the current F_{CLK}, V_{DD}, & temperature

Measured Impact of Tunable-Length Delay



[1] K. Bowman *et al.*, *JSSC*, 2016.

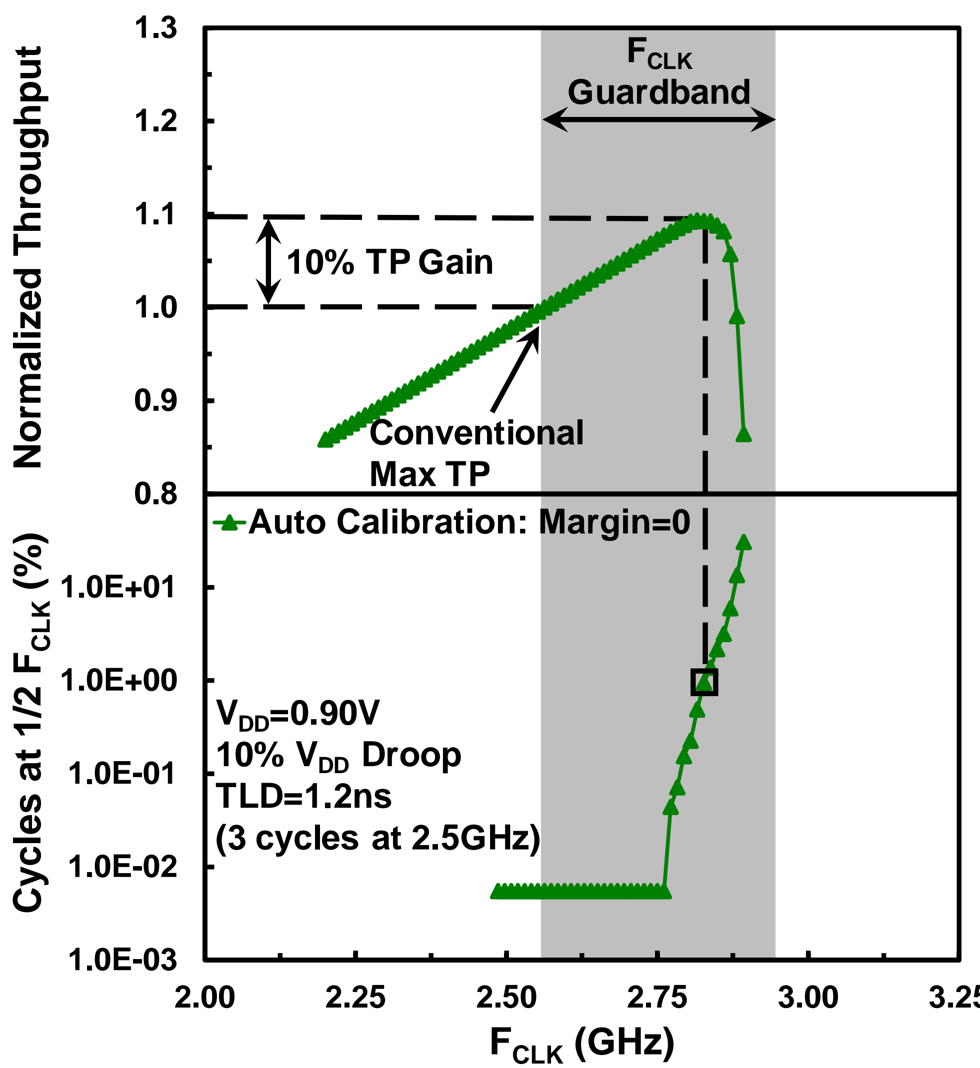
- With F_{CLK}=2.5GHz, a 2.4ns tunable-length delay postpones the critical-path timing-margin degradation by 6 cycles

Clock-Data Compensation Dependencies

- Independent of V_{DD} droop frequency
- Depends on tunable-length delay

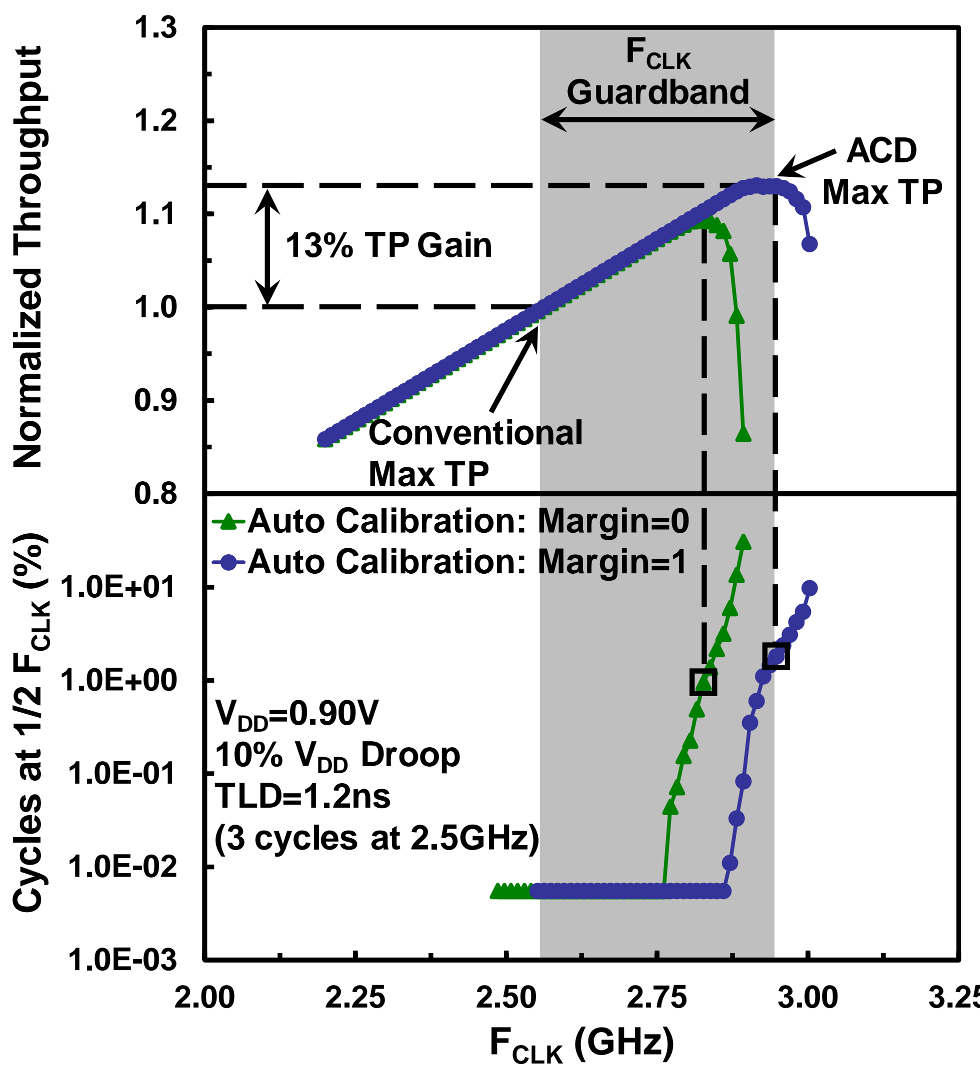
[1] K. Bowman *et al.*, *JSSC*, 2013.

Measured Throughput (TP) versus F_{CLK}



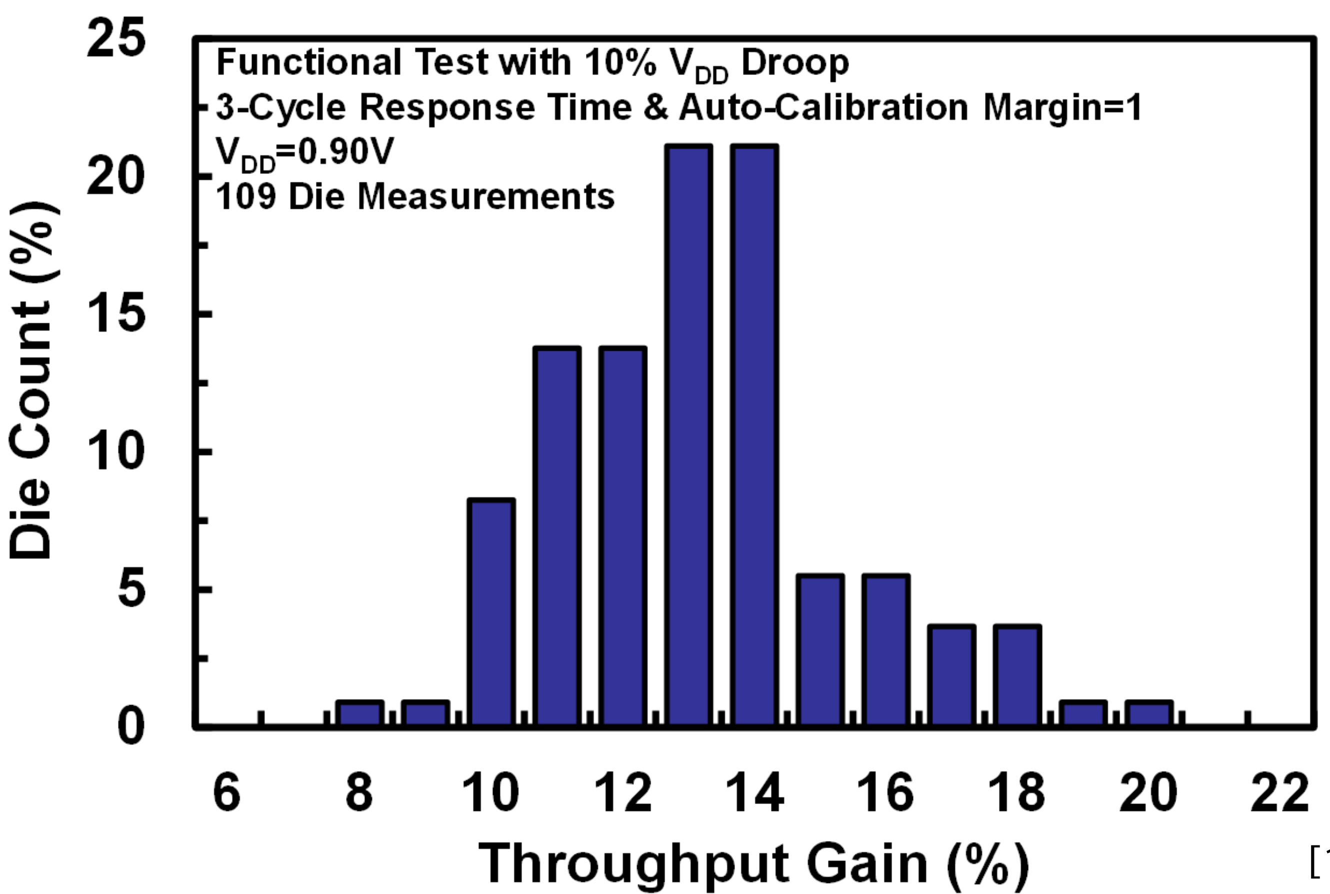
[1] K. Bowman *et al.*, *JSSC*, 2016.

Measured Throughput (TP) versus F_{CLK}



[1] K. Bowman *et al.*, *JSSC*, 2016.

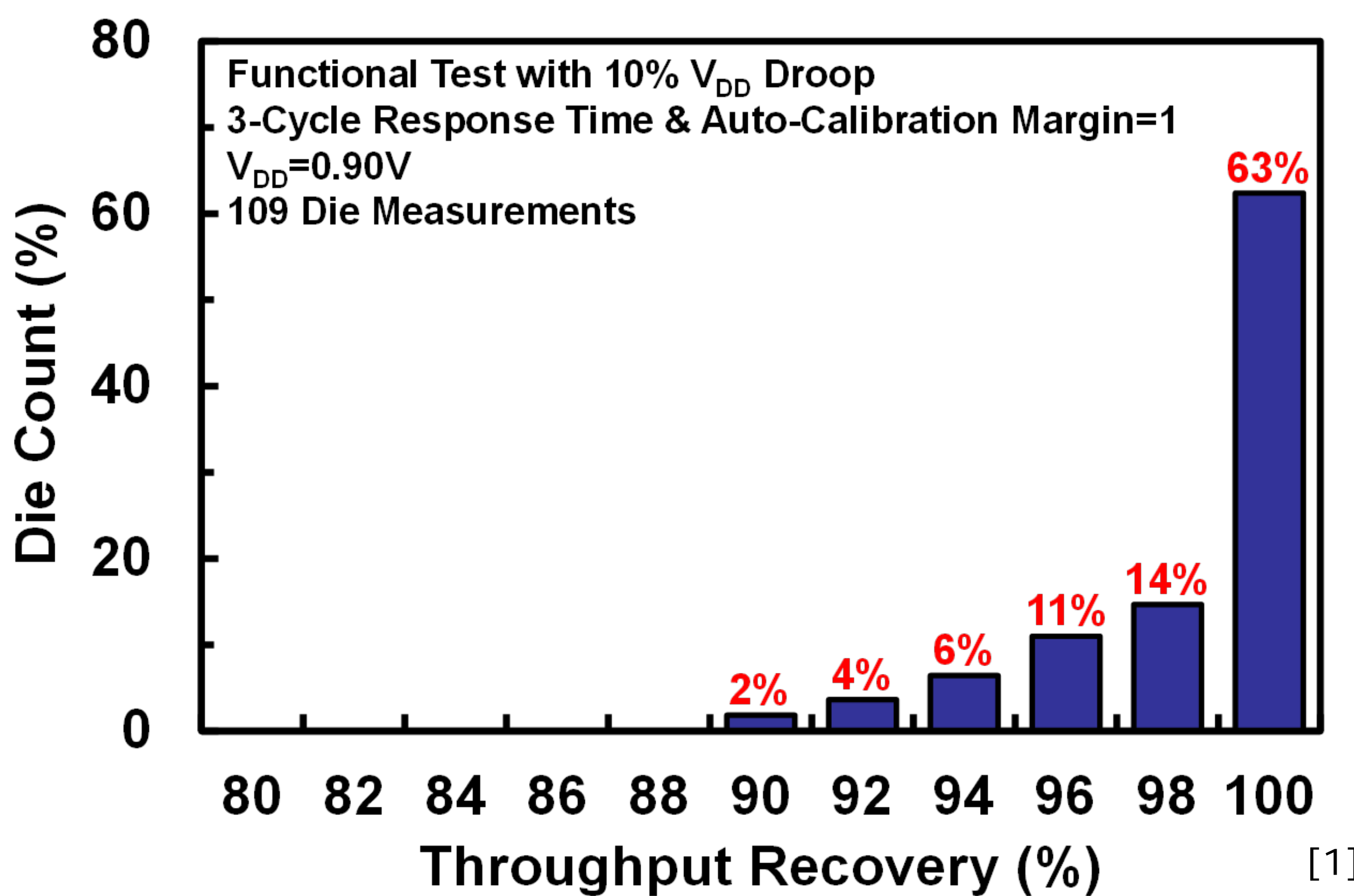
Measured Throughput Gain Distribution



[1] K. Bowman *et al.*, *JSSC*, 2016.

- ACD TP gain ranges from 8% to 20% with a mean of 14%
- ACD TP gain depends on TP loss for conventional design

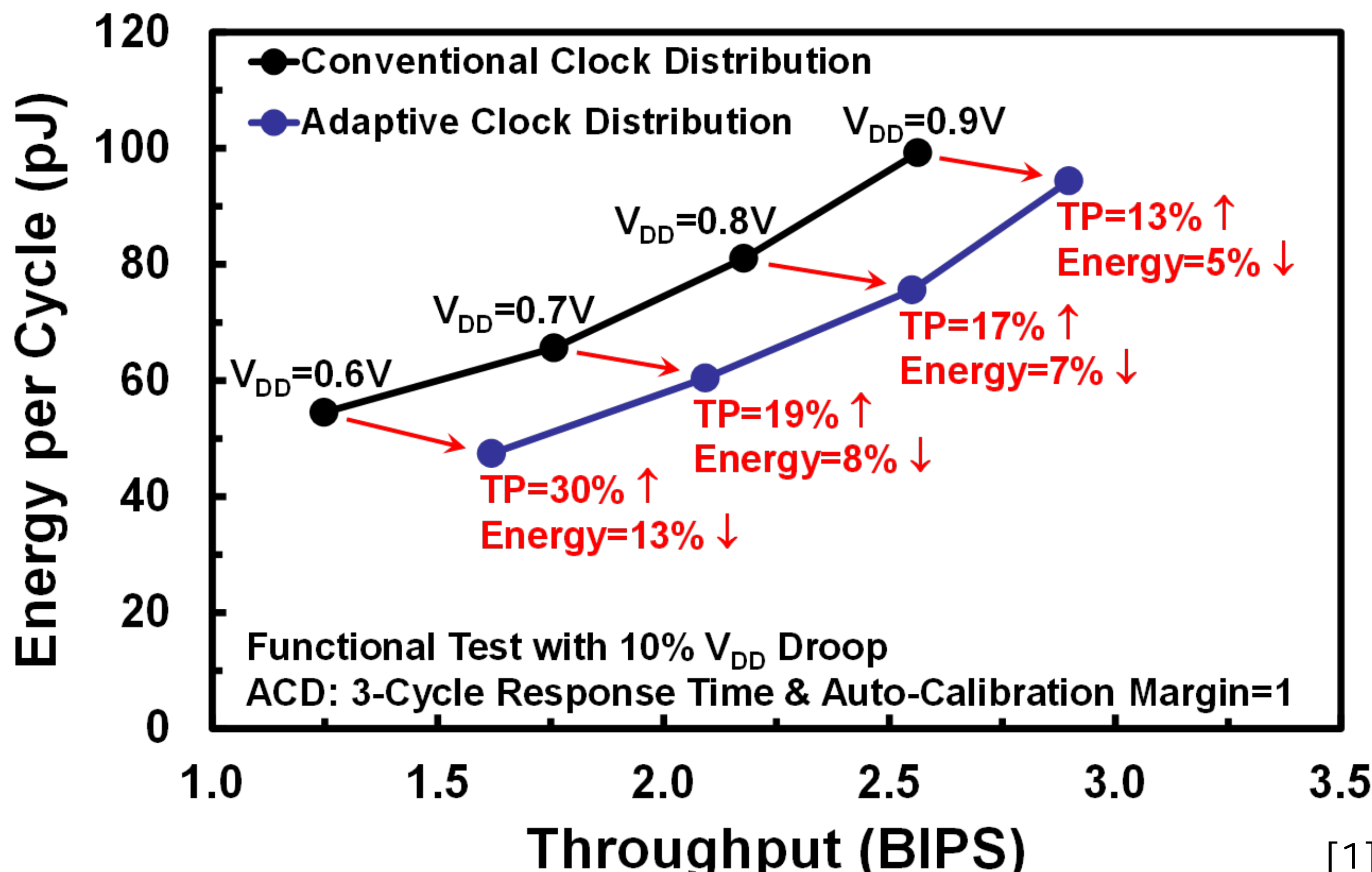
Measured Throughput Recovery Distribution



[1] K. Bowman *et al.*, *JSSC*, 2016.

- Recovers 100% of the throughput loss for 63% of dies
- Recovers 90% of the throughput loss for 100% of dies

Measured Energy versus Throughput



[1] K. Bowman *et al.*, *JSSC*, 2016.

- Throughput gains range from 13% to 30%
- Energy reduction ranges from 5% to 13%

ACD Product Calibration & High-Volume Test

Production Calibration: 2 Steps

1) Performance Test

- Calibrate DVM margin via system-level testing with real applications
- Determine the minimum DVM margin with negligible performance loss

2) Stability Test

- Perform F_{MAX}/V_{MIN} tests to measure ACD benefits with synthetic code to induce the largest V_{DD} droop possible
- Focus is on surviving the worst-case V_{DD} droop events

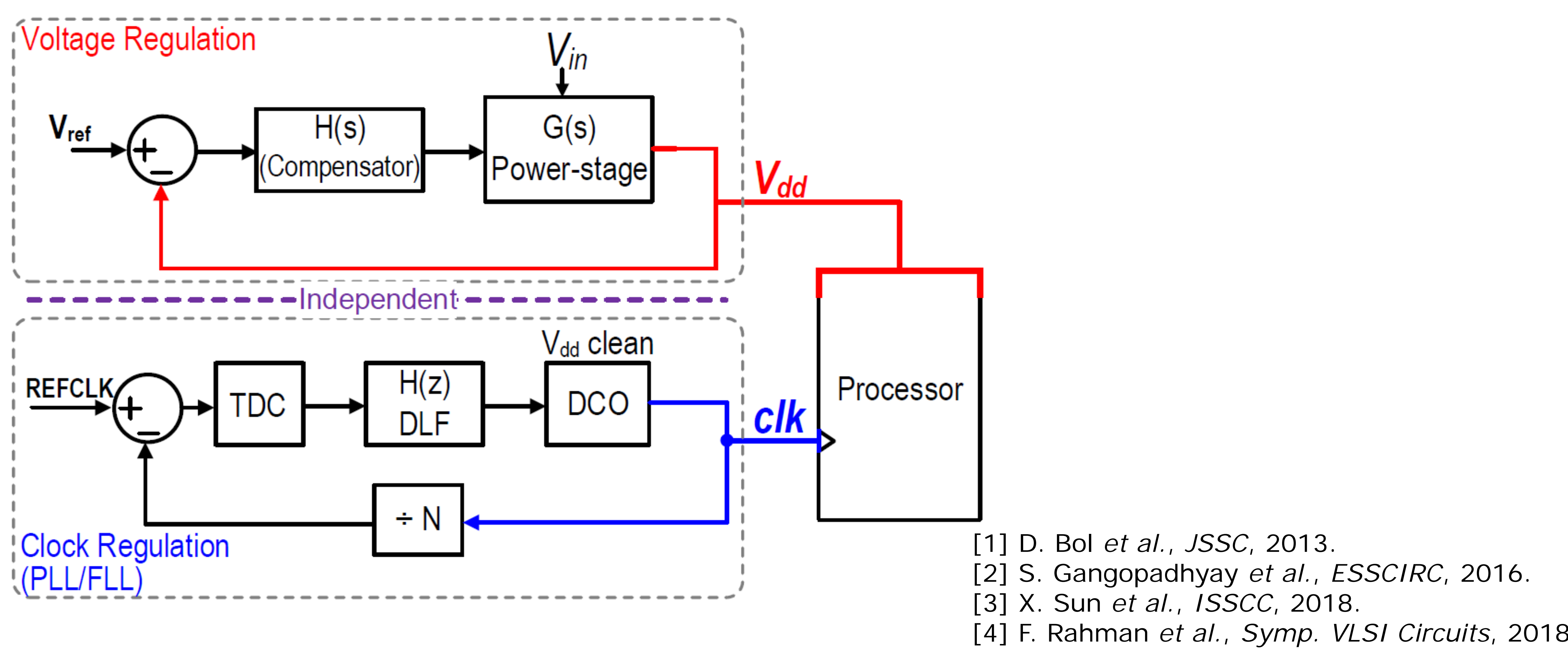
High-Volume Test

- *No calibration required (functional test only)*

Outline

- Sources of Dynamic Parameter Variations
- Impact of Dynamic Variations on Design
- Adaptive & Resilient Circuits
  - Adaptive Designs for Slow-Changing Variations
  - Resilient Designs
  - Adaptive Designs for Fast-Changing Variations
  - Future Adaptive Designs
- Summary

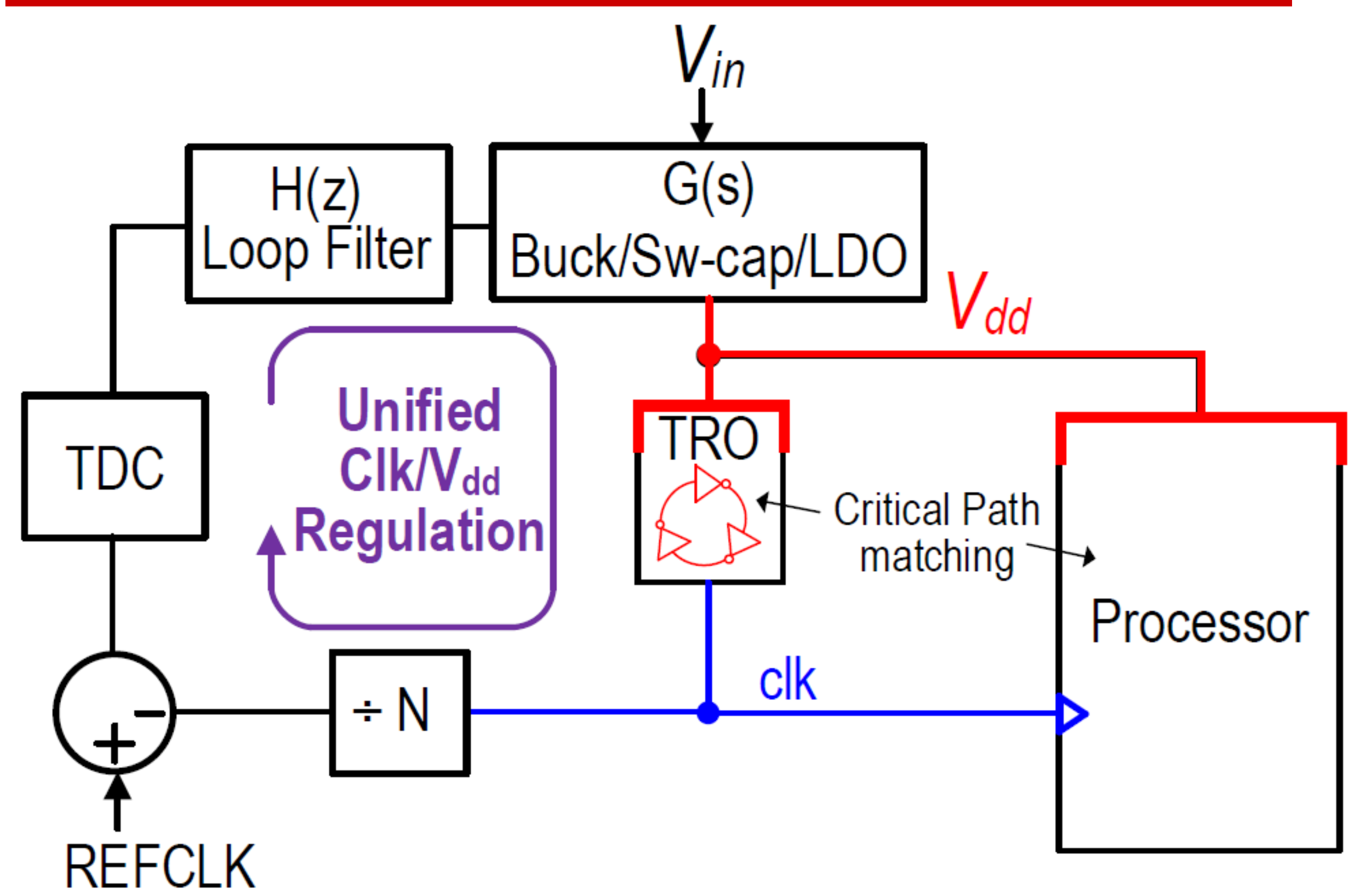
Voltage & Frequency Regulation



[1] D. Bol *et al.*, *JSSC*, 2013.
[2] S. Gangopadhyay *et al.*, *ESSCIRC*, 2016.
[3] X. Sun *et al.*, *ISSCC*, 2018.
[4] F. Rahman *et al.*, *Symp. VLSI Circuits*, 2018.

- Today's processors generate V_{DD} & F_{CLK} in two separate control loops

Unified Voltage & Frequency Regulation



[1] D. Bol *et al.*, *JSSC*, 2013.
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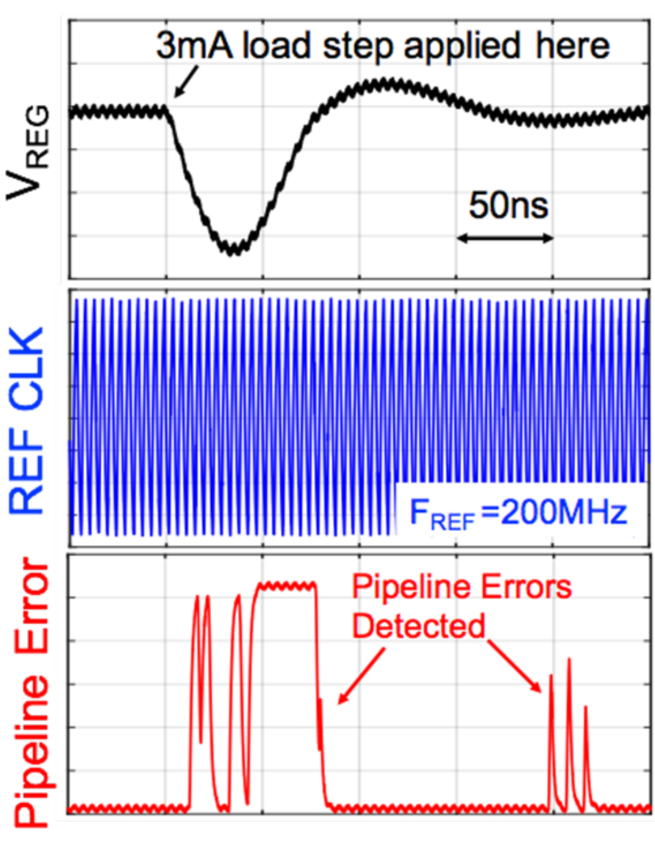
[3] X. Sun *et al.*, *ISSCC*, 2018.
[4] F. Rahman *et al.*, *Symp. VLSI Circuits*, 2018.

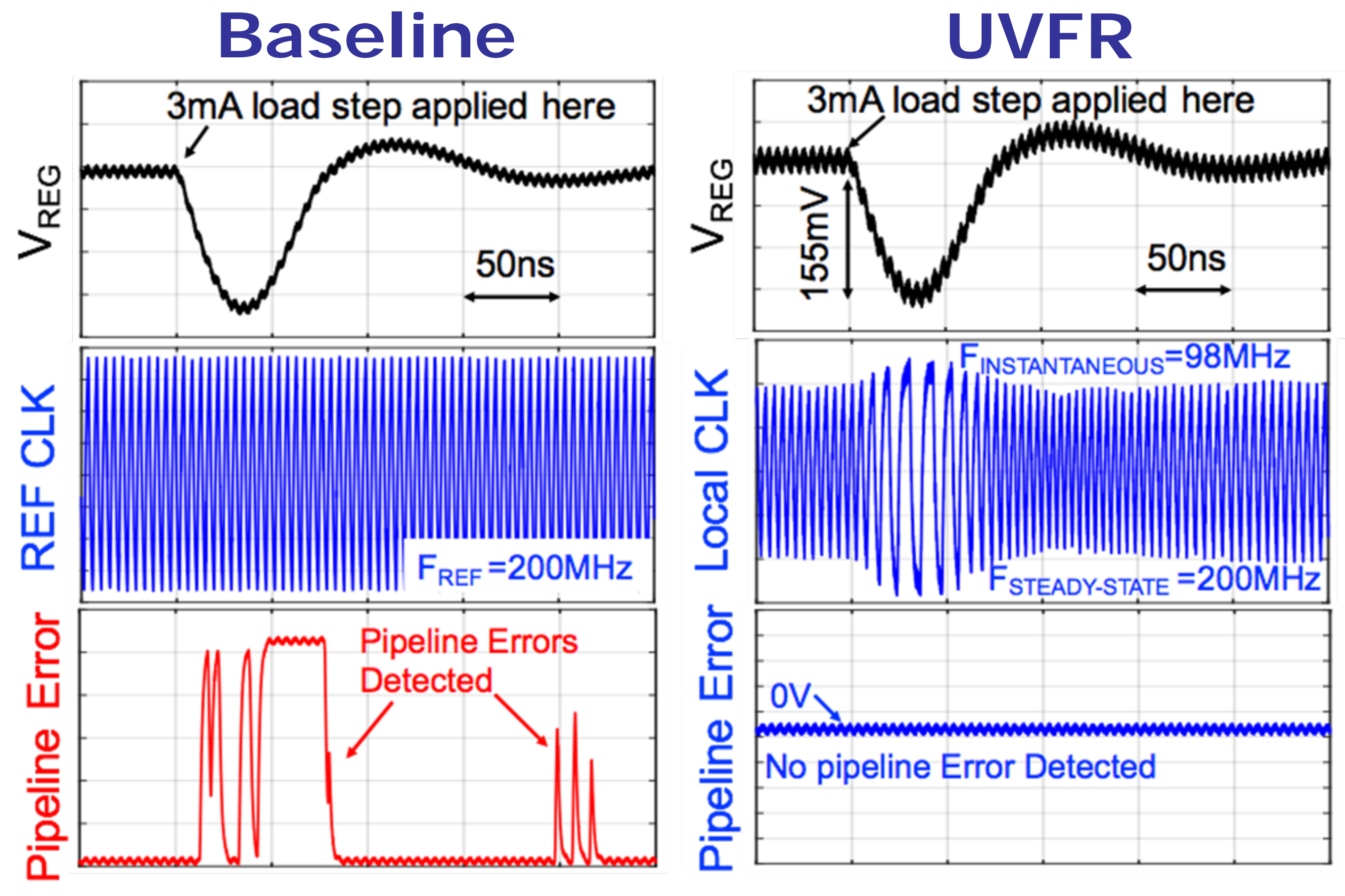
- Generates V_{DD} & F_{CLK} in a single control loop
- *Clock-data compensation is infinite!!!*

Unified Voltage & Frequency Regulation



[1] S. Gangopadhyay *et al.*, *ESSCIRC*, 2016.

Unified Voltage & Frequency Regulation



[1] S. Gangopadhyay *et al.*, *ESSCIRC*, 2016.

- Intrinsically adapts V_{DD} & F_{CLK} to avoid timing-margin violations

Outline

- Sources of Dynamic Parameter Variations
- Impact of Dynamic Variations on Design
- Adaptive & Resilient Circuits
  - Adaptive Designs for Slow-Changing Variations
  - Resilient Designs
  - Adaptive Designs for Fast-Changing Variations
  - Future Adaptive Designs
- Summary

Summary

- Adaptive & resilient circuits mitigate dynamic variation guardbands for higher performance, energy efficiency, & yield
- Traditional Adaptive Design:
  - + Low overhead
  - — Response time limits benefits
- Resilient Design:
  - + Relaxes the response-time constraint
  - — Design complexity for error recovery
- Auto-Calibrating Adaptive Clock Distribution Design:
  - + Low overhead
  - + Mitigates impact of V_{DD} droops while avoiding error recovery & calibration at test
- Unified Voltage & Frequency Regulation:
  - + Generates V_{DD} & F_{CLK} in single control loop with intrinsic adaptation

Q & A

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