Dissecting Design Choices for Power Efficient Continuous-time $\Delta\Sigma$ Converters

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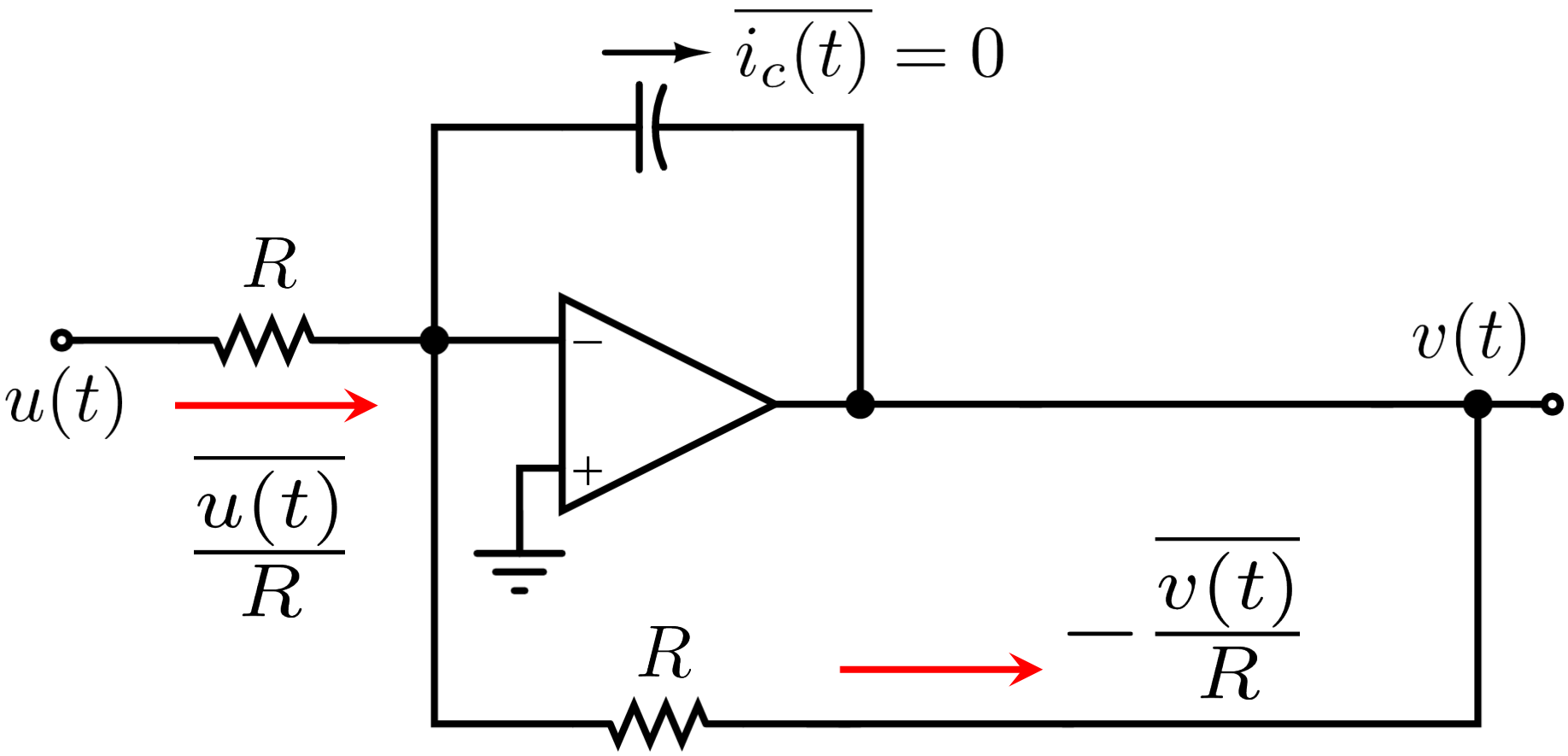
Outline

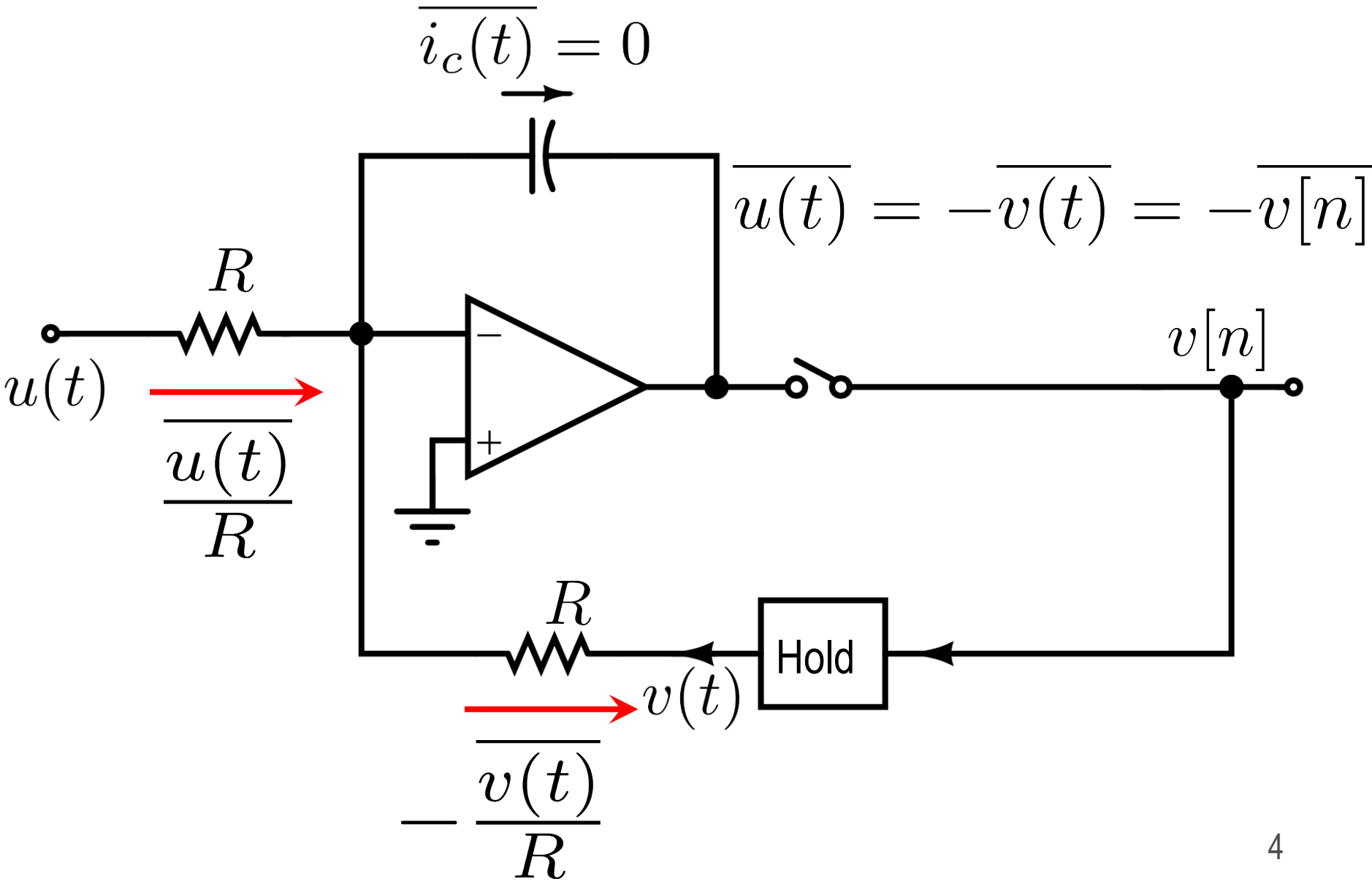
- Introduction
- Architectural design choices
- Circuit techniques for low power
- Design details
- Measured results
- Conclusions

CTΔΣM in 1 minute

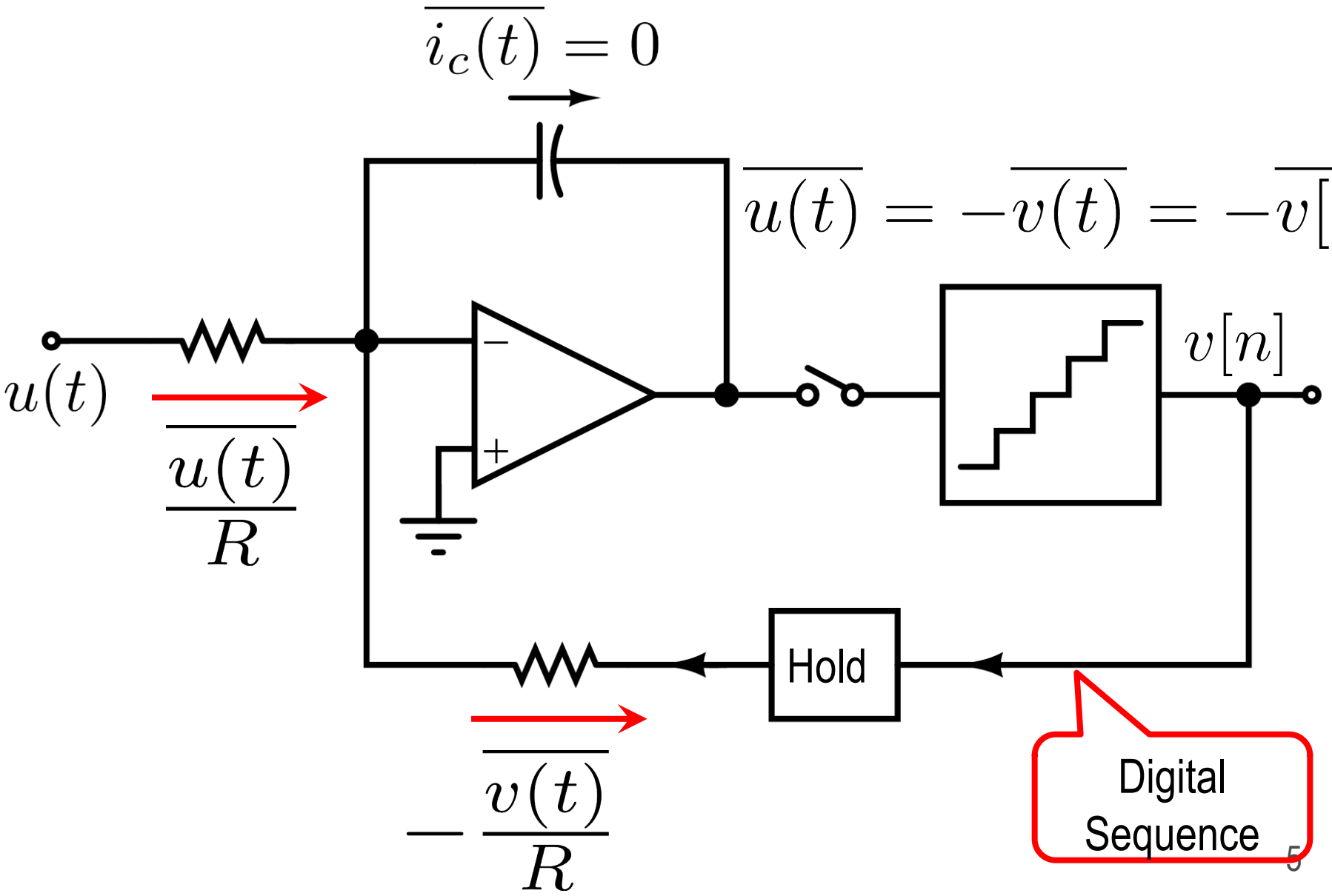


$$\overline{u(t)} = -\overline{v(t)}$$

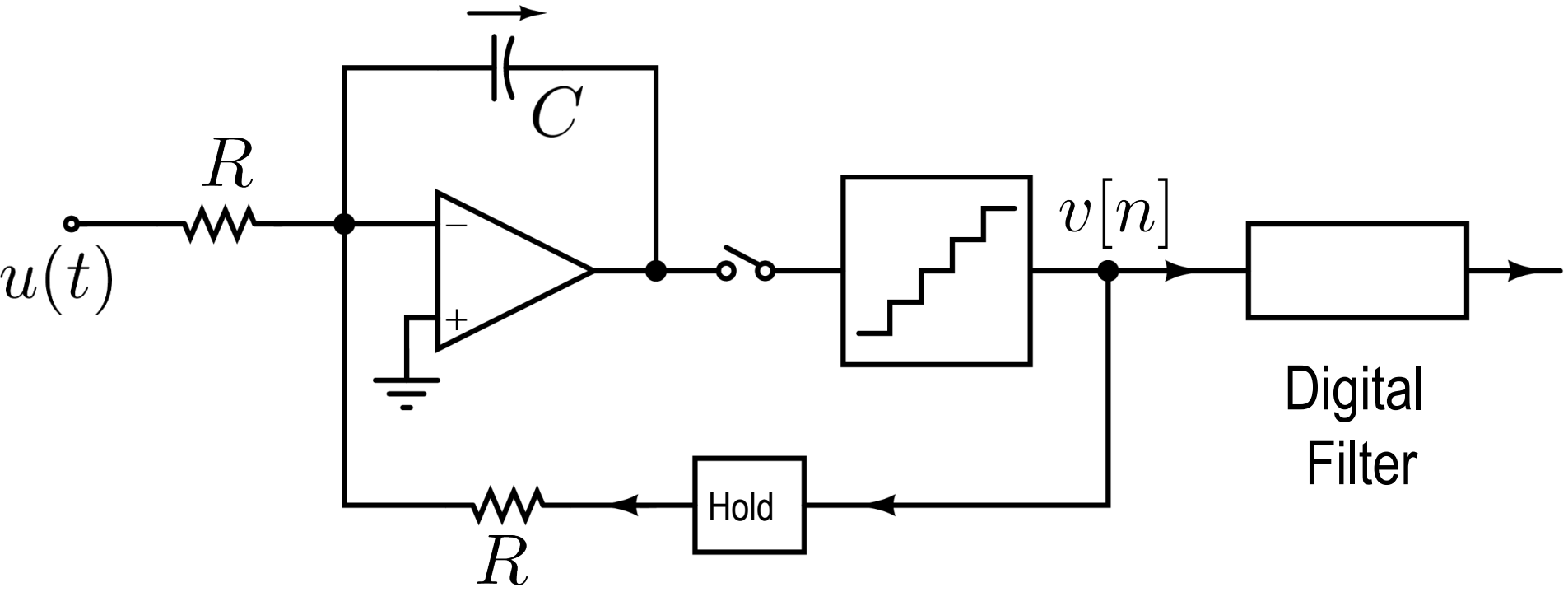
CTΔΣM in 1 minute



CTΔΣM in 1 minute



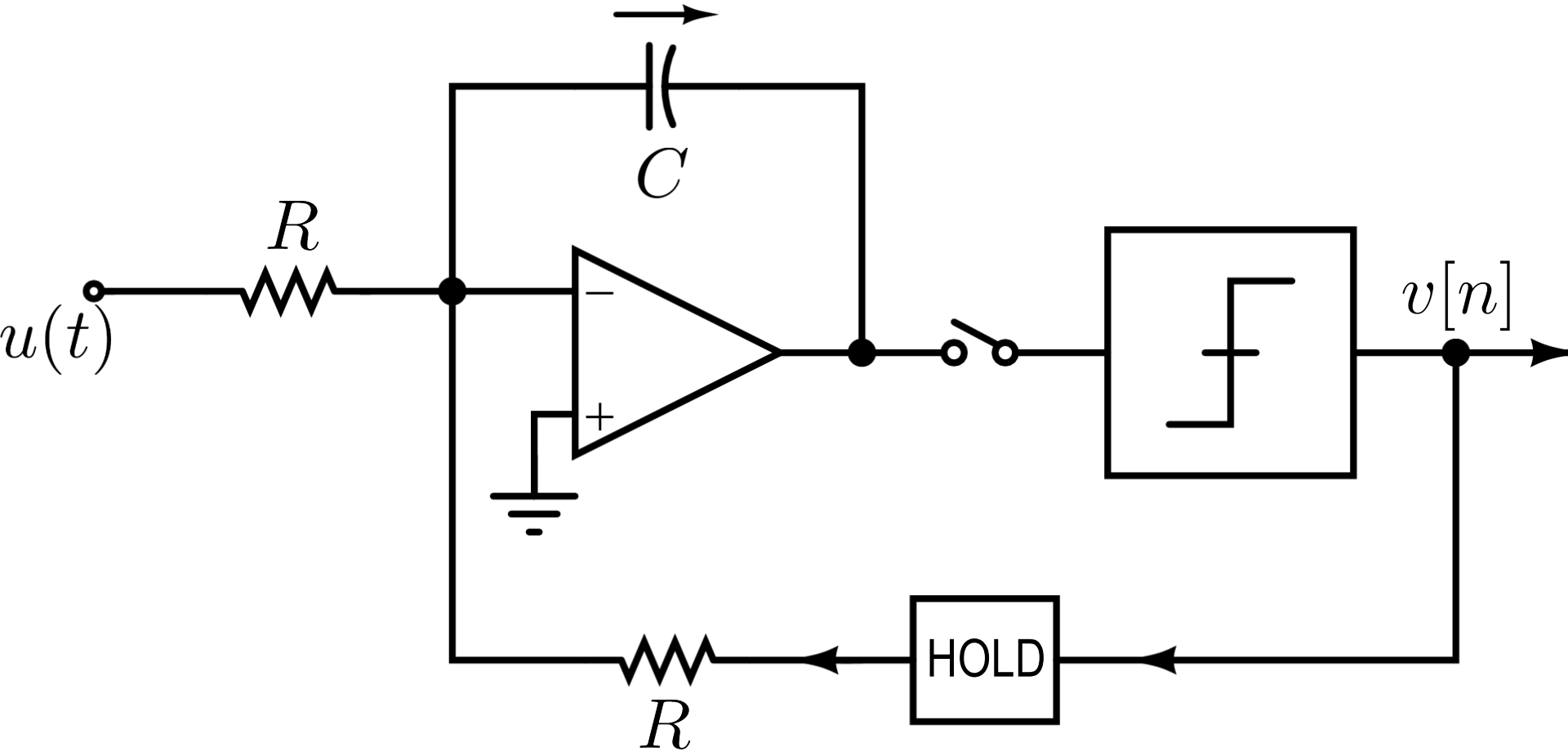
CTΔΣM in 1 minute



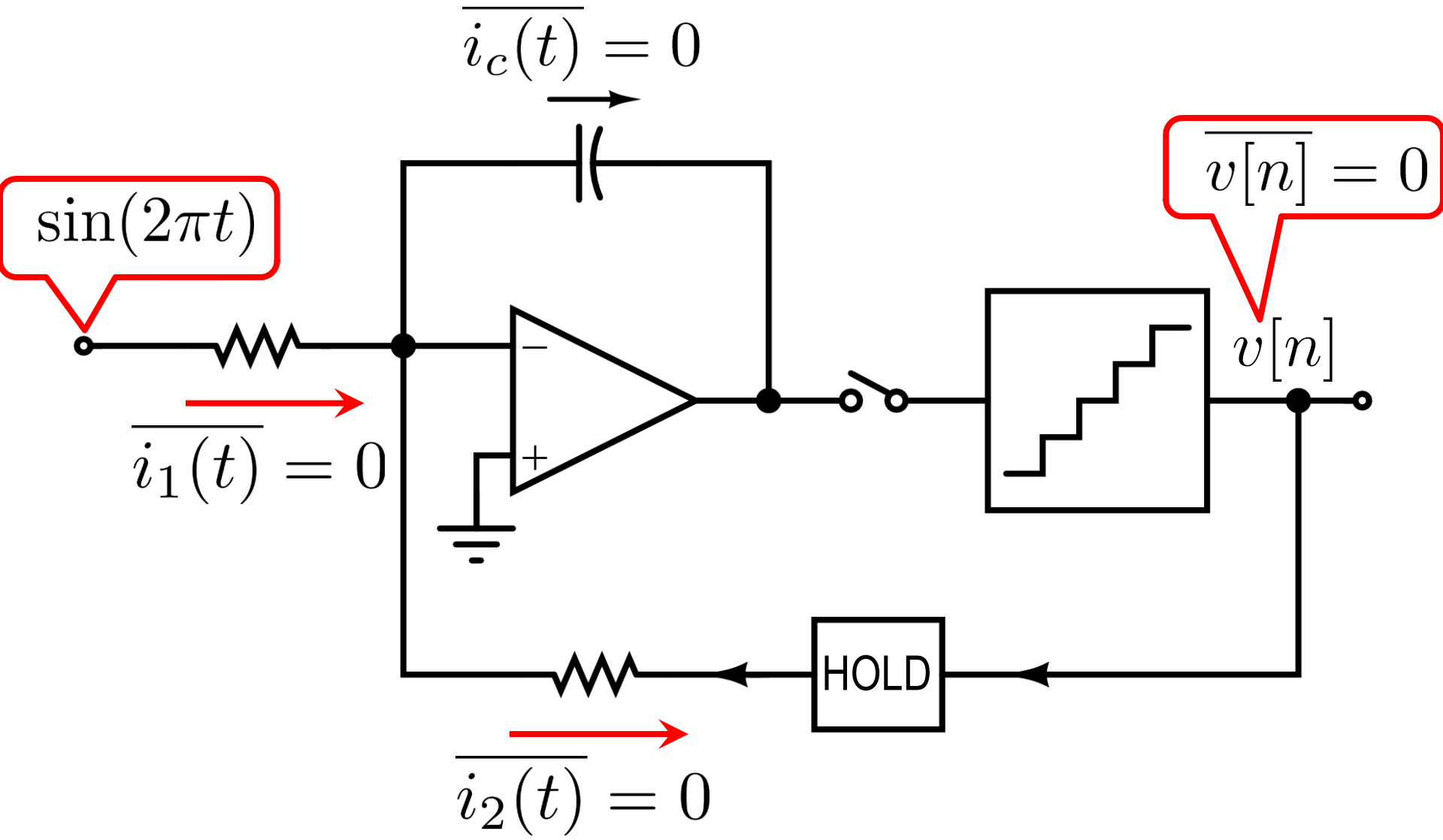
$$\text{Slow } u(t) \longrightarrow \overline{u(t)} \approx u(t)$$

Does the number of quantizer levels matter?

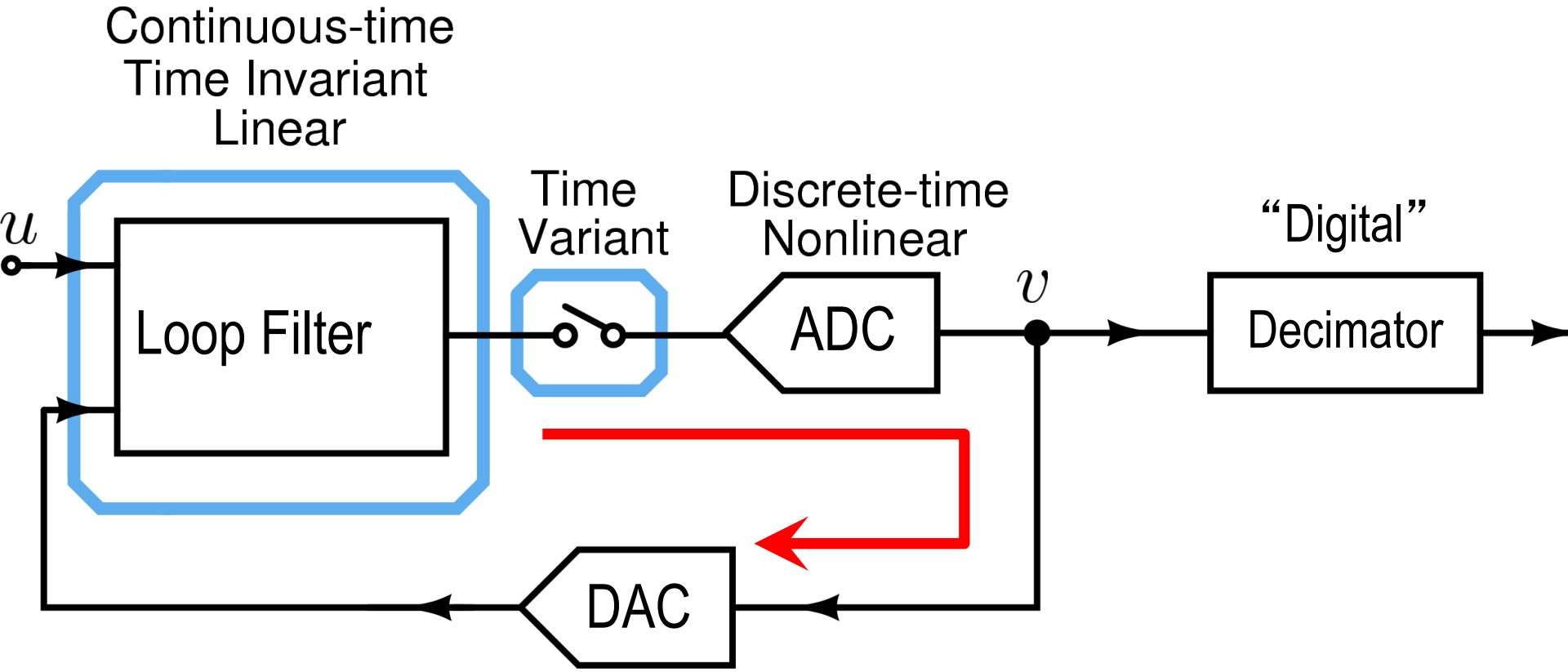
CTΔΣM in 1 minute



CTΔΣM in 1 minute : Antialiasing



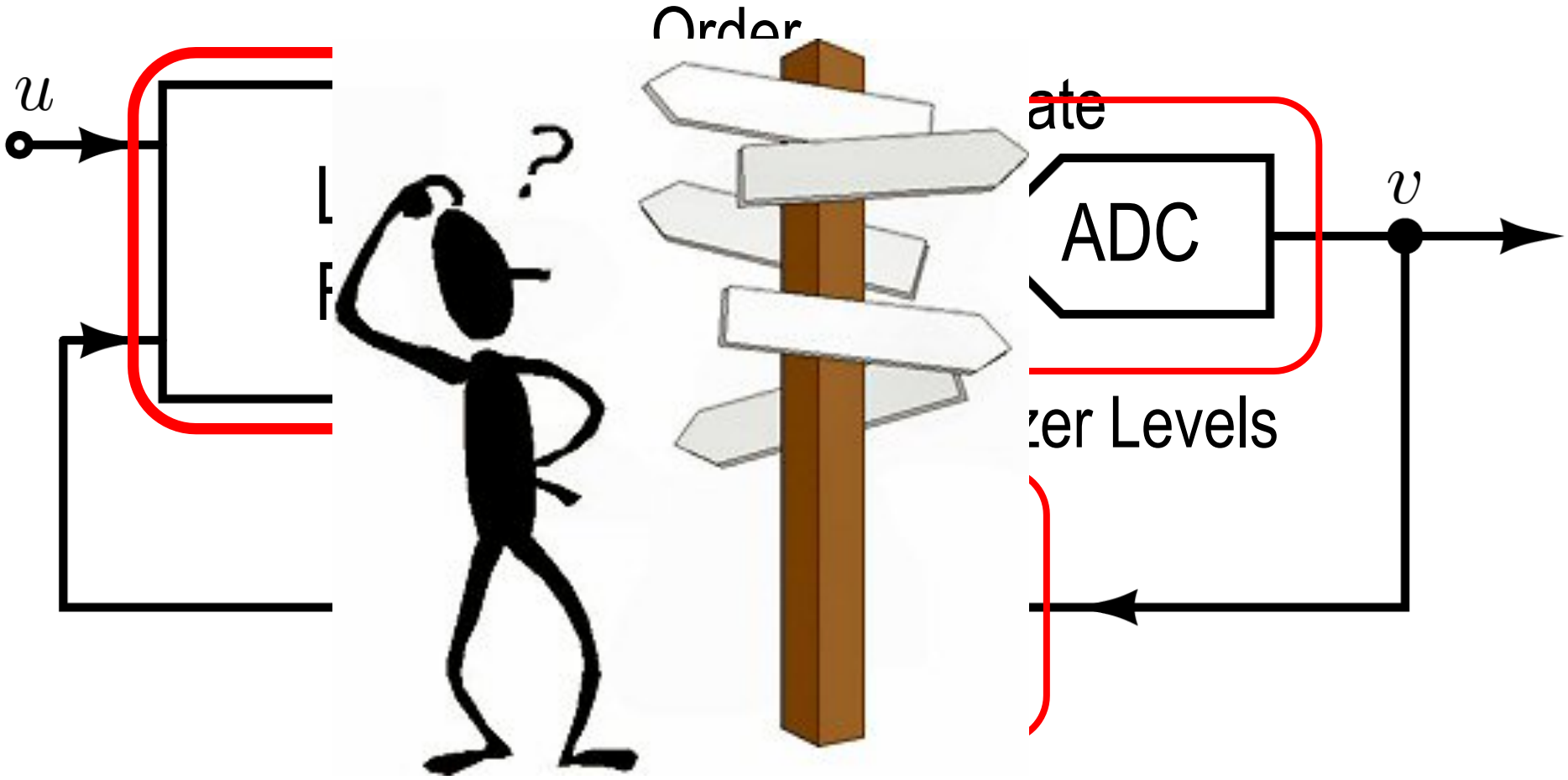
CTΔΣM : A System for all Seasons



Negative Feedback

Industrially and Practically Relevant

(Too) Many Design Choices



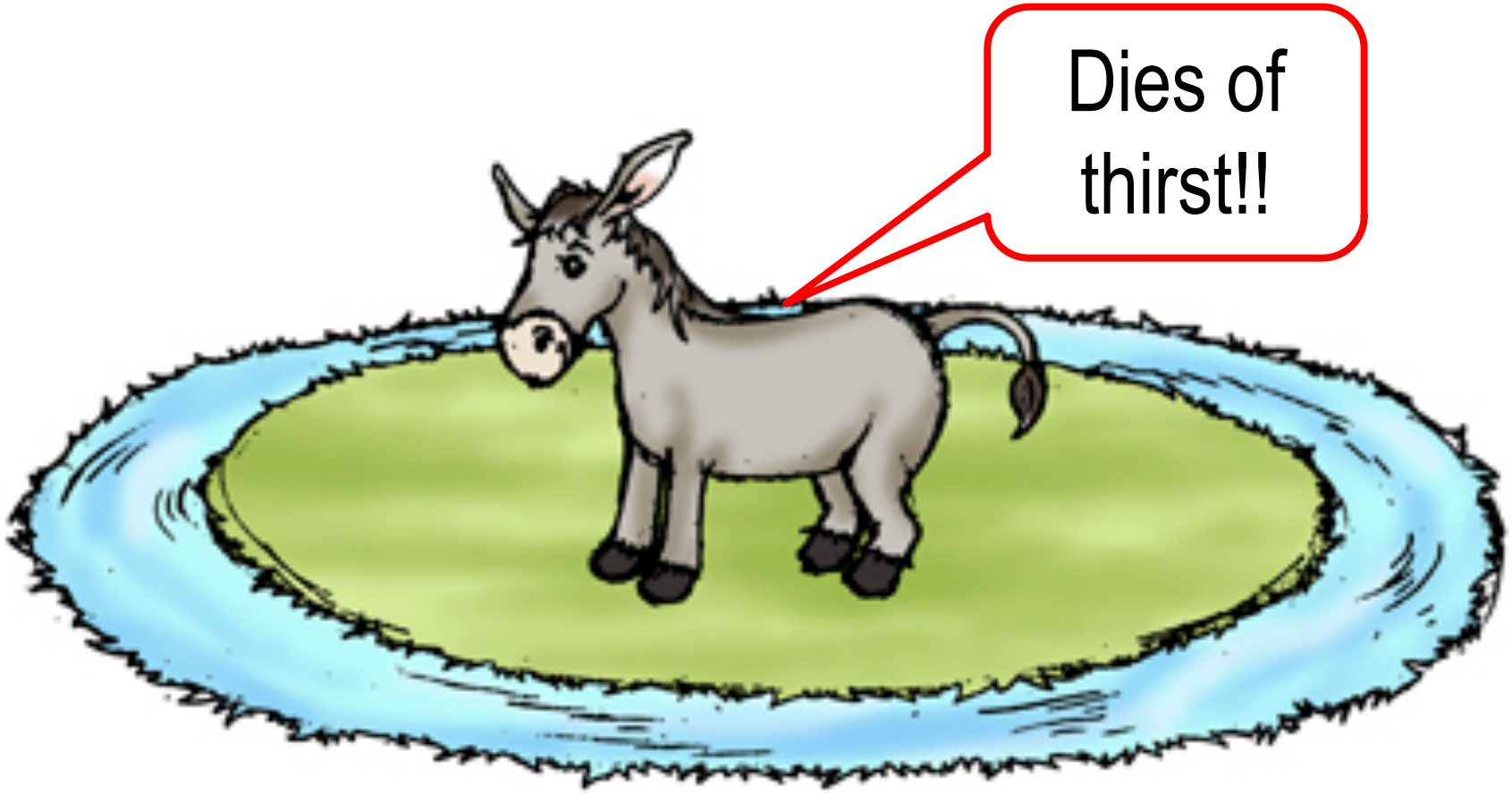
Curse of Too Many Choices

- Single bit quantizer + high OSR
  - Or multibit quantizer + low OSR?
- Flash ADC
  - Or SAR ADC?
- NRZ DAC
  - Or Switched capacitor DAC for low jitter?

Buridan's Ass

Courtesy : Inspirehep.net

$\Delta\Sigma$ Designer …



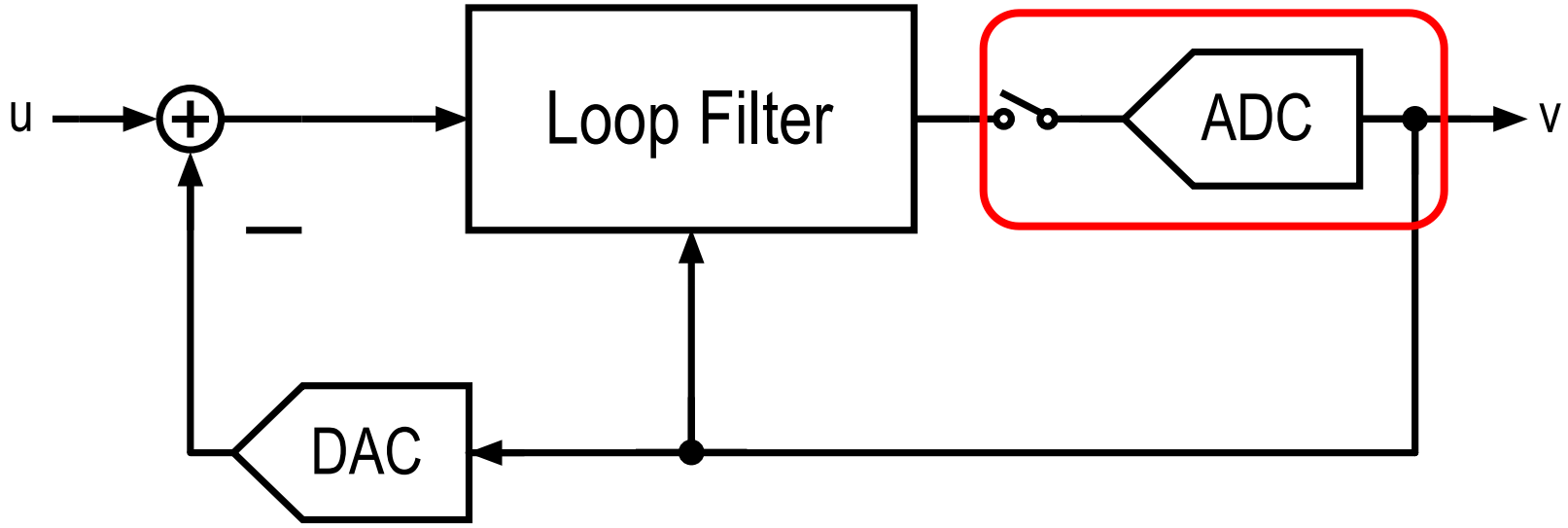
Courtesy : Inspirehep.net

Motivation

- Aim : Audio DSM with > 100 dB DR
  - 0.18μm CMOS technology
  - As low power as possible
- Low distortion (~100 dB) audio $\Delta\Sigma$ converters
  - Typically realized with discrete-time, multi-bit loops

Single-bit versus Multibit Modulators

Quantizer : 1-bit versus 4-bit

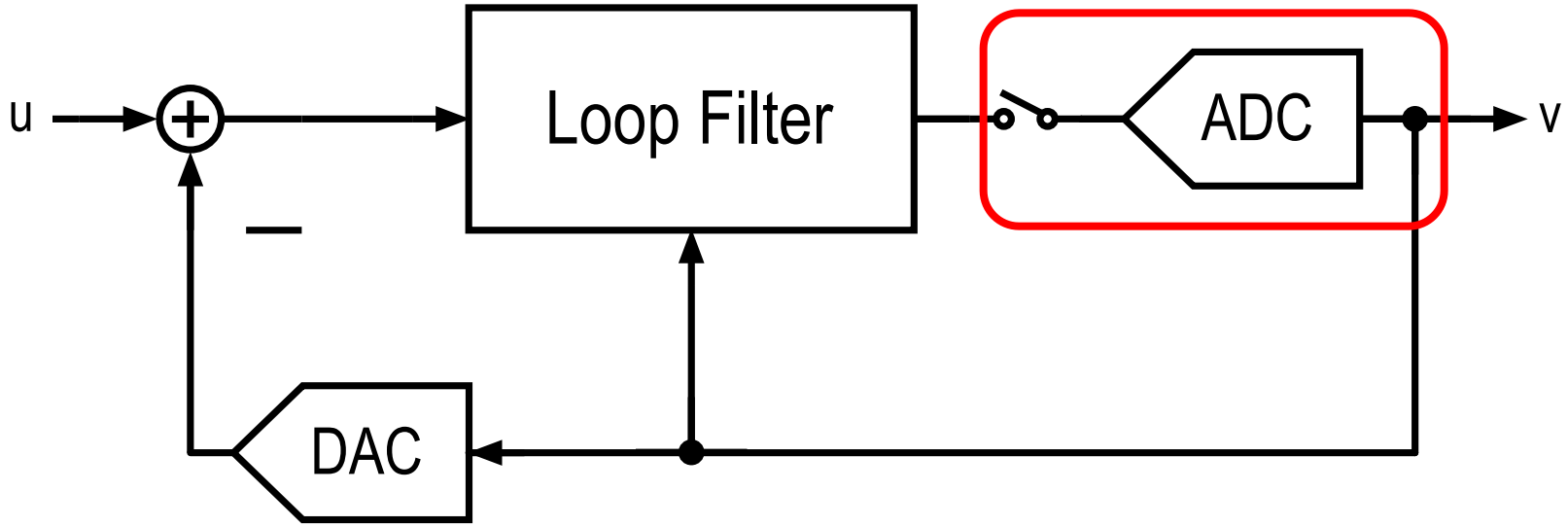


4-bit quantizer needs half the OSR

to achieve same in-band noise

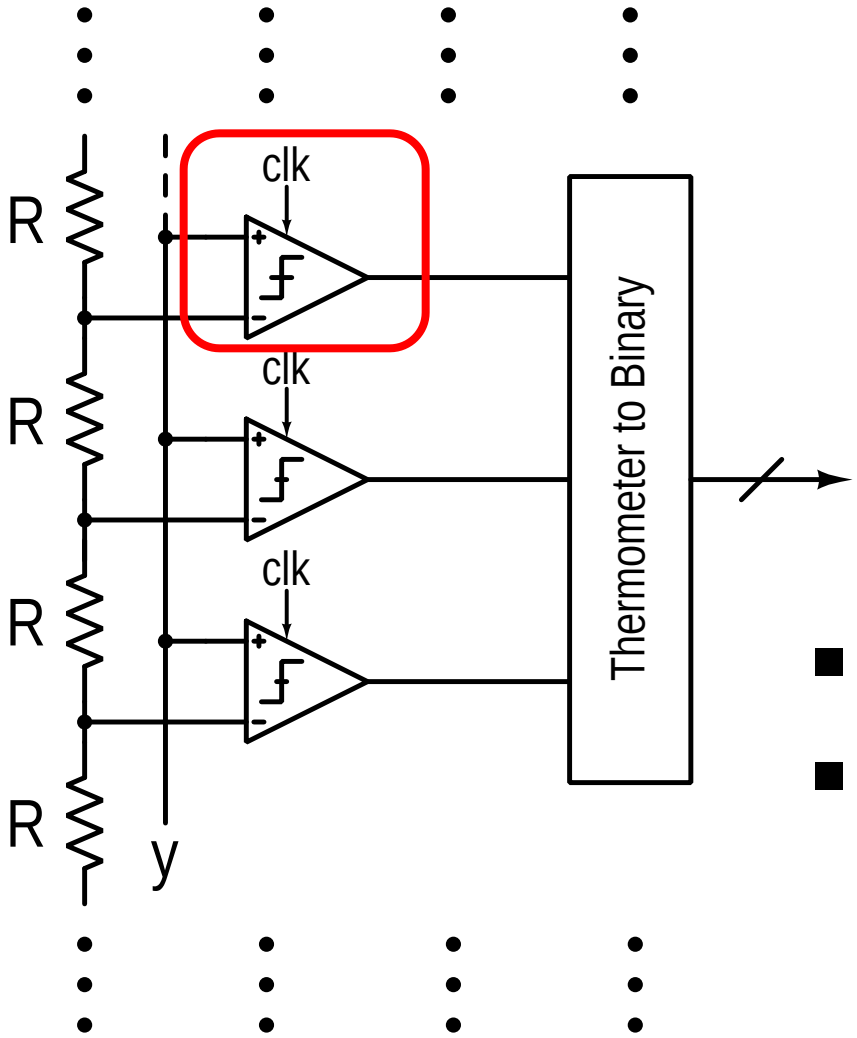
(Baseline : 3rd Order Single-bit DSM, OSR =128)

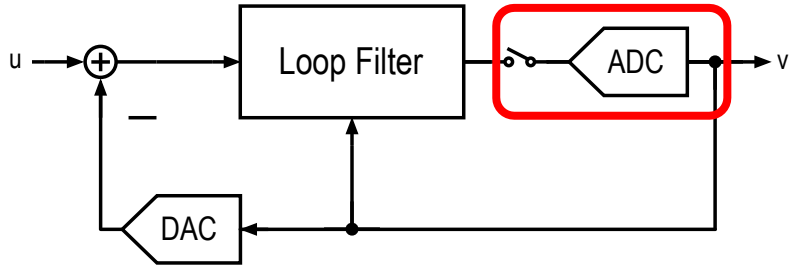
ADC Resolution



- 4 bit ADC
  - 15x more comparators @ 1/2 speed
  - 7x more ADC power, 15x more area
  - 15x loop filter & clock path loading

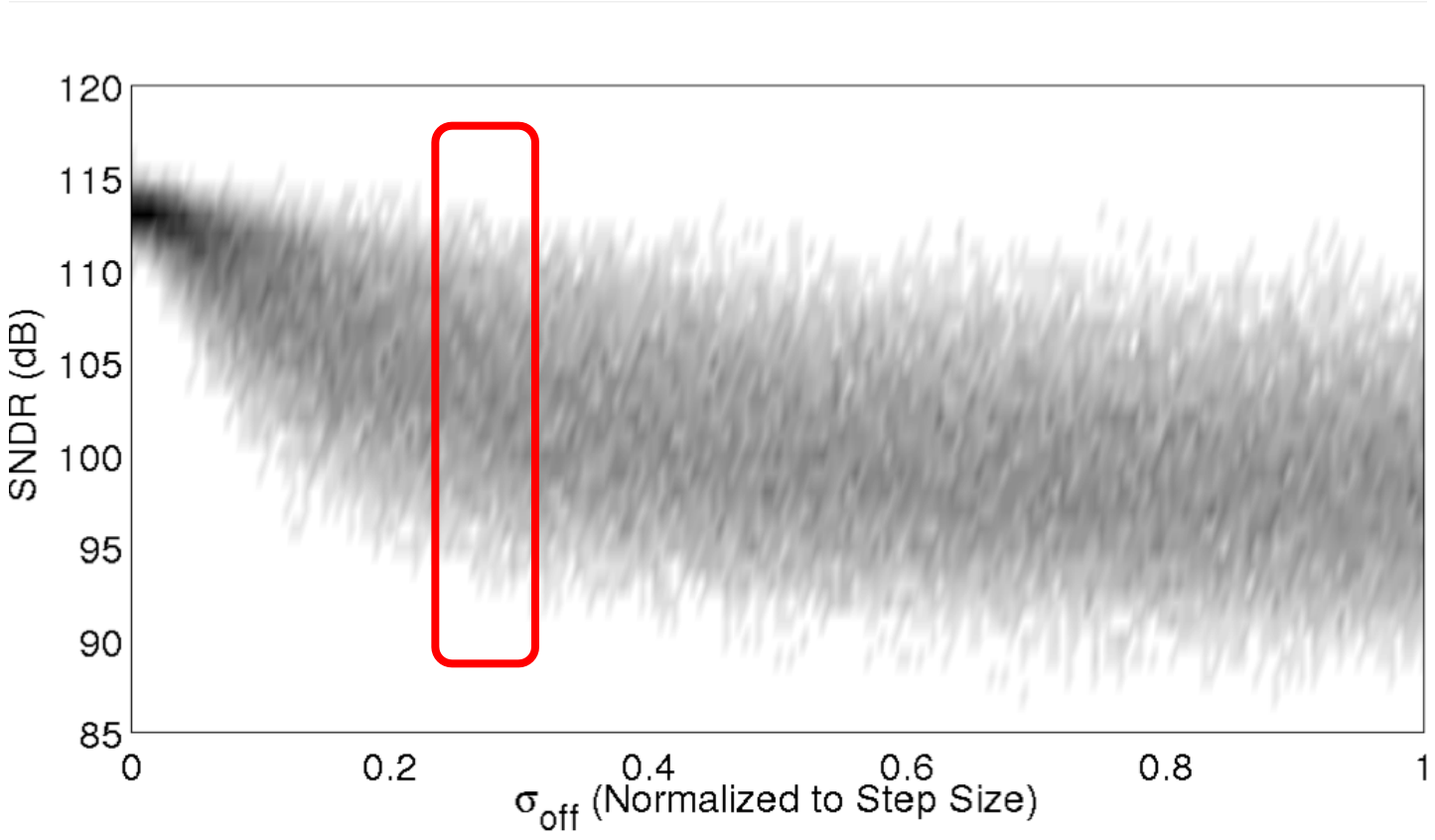
Comparator Random Offset





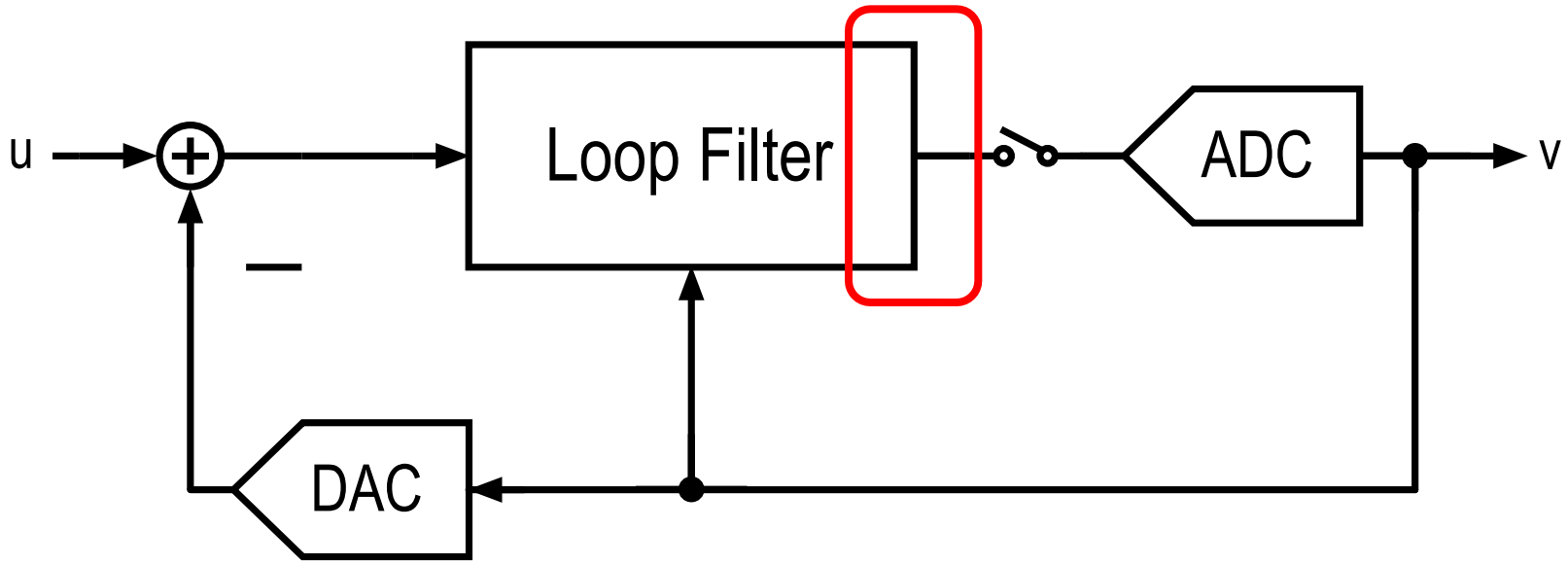
- Increased in-band noise
- Reduced stable amplitude

SNDR with Random Offset



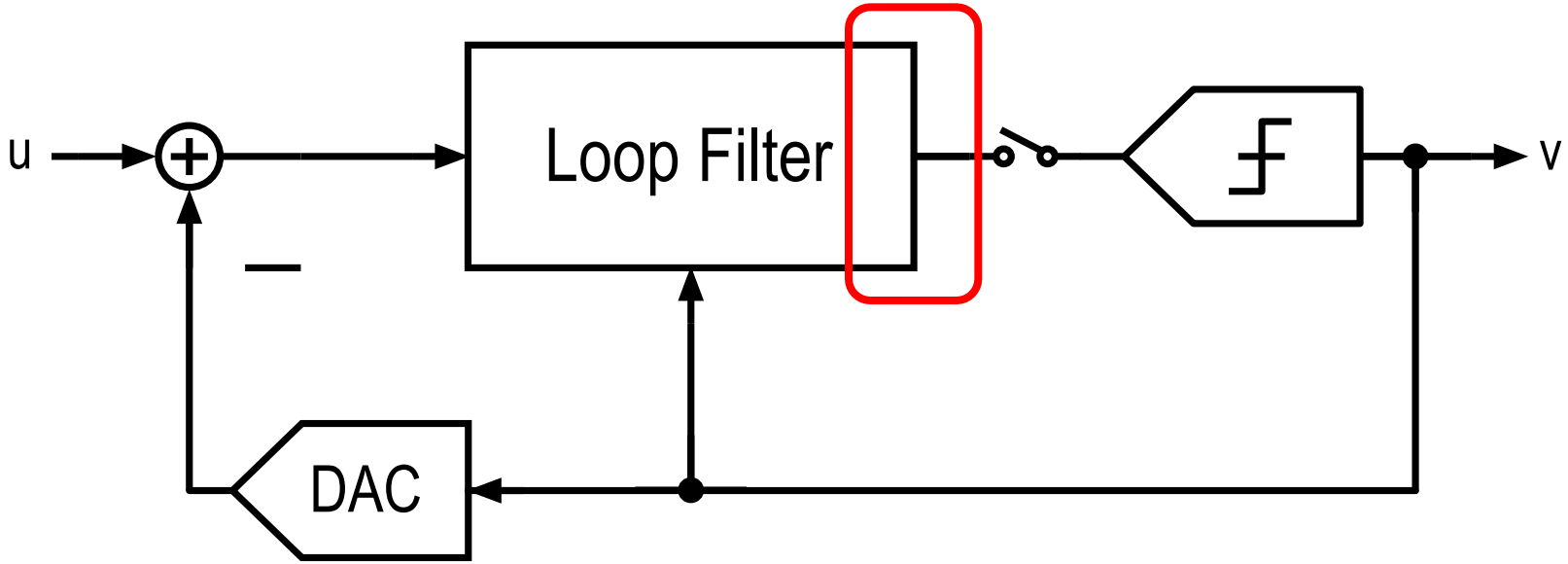
Third-order Modulator 16-level Quantizer

Loop Filter



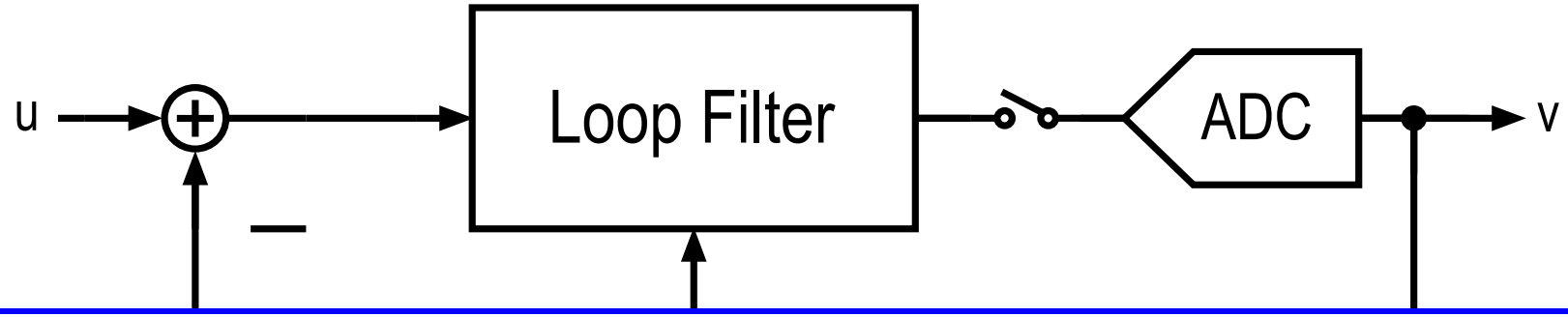
- Loop filter should swing full-scale
- Difficult in high-speed designs

Loop Filter



- Comparator offset is benign
- Driving the 1-bit quantizer
  - Loop filter's last stage simpler to design
  - Particularly useful at high speeds

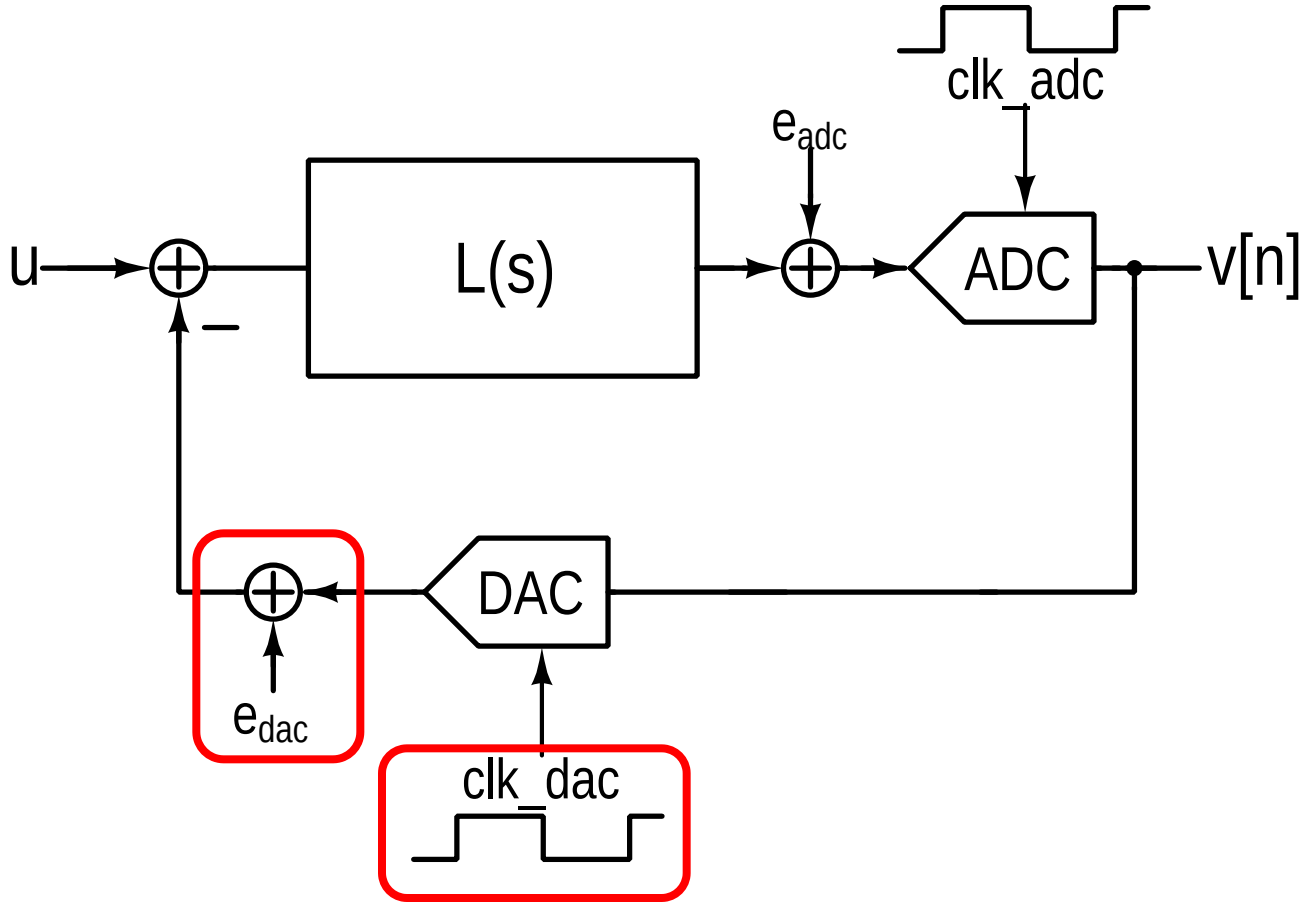
DAC : 1-bit versus 4-bit



A single bit quantizer consumes
lesser power
though it operates at 2x the speed

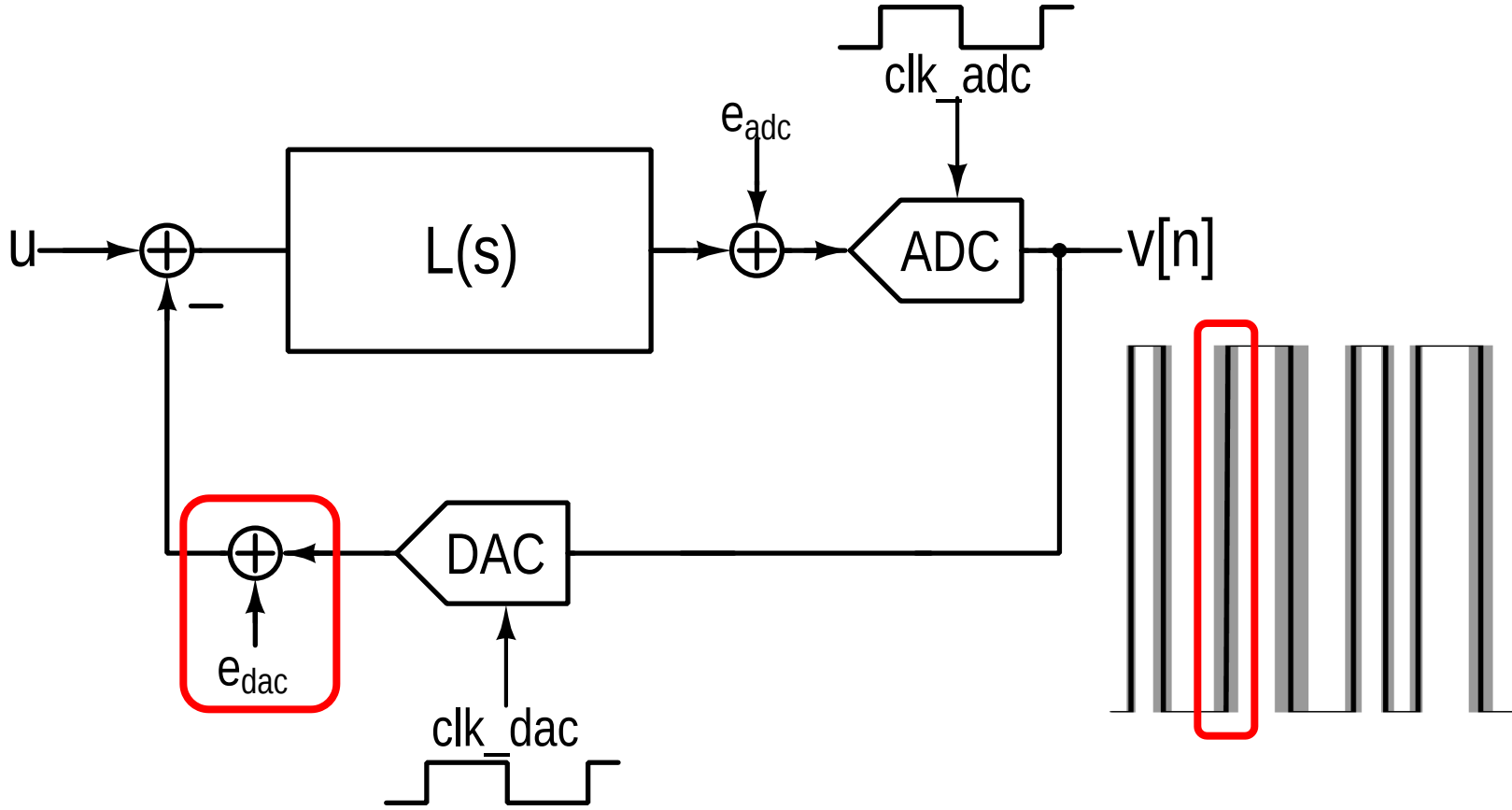
- Needs Dynamic Element Matching
- DEM adds excess delay & power

Single-bit CTDSM Issues : Clock Jitter



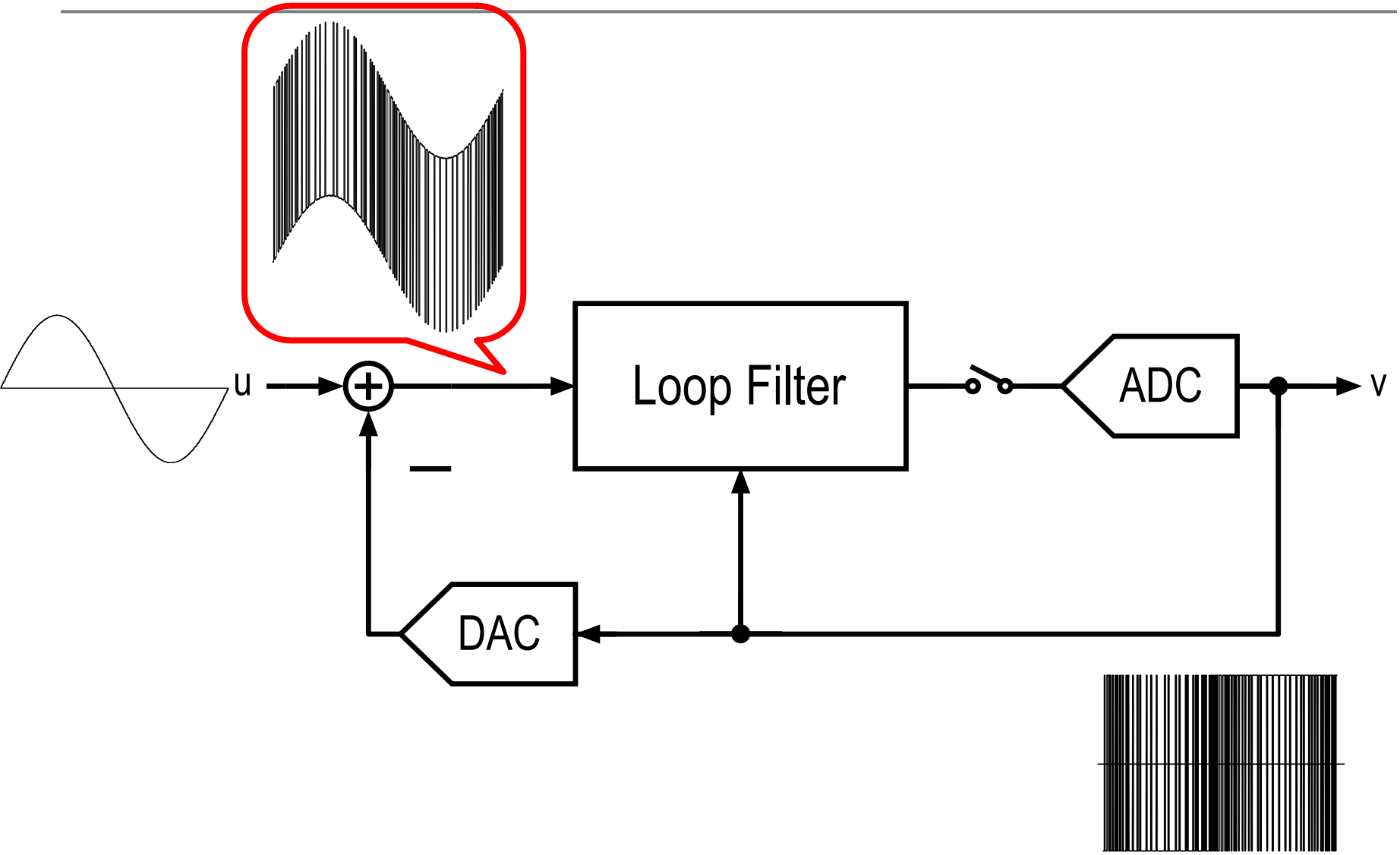
Jittery clock → equivalent to error at the input

Single-bit CTDSM Issues : Clock Jitter

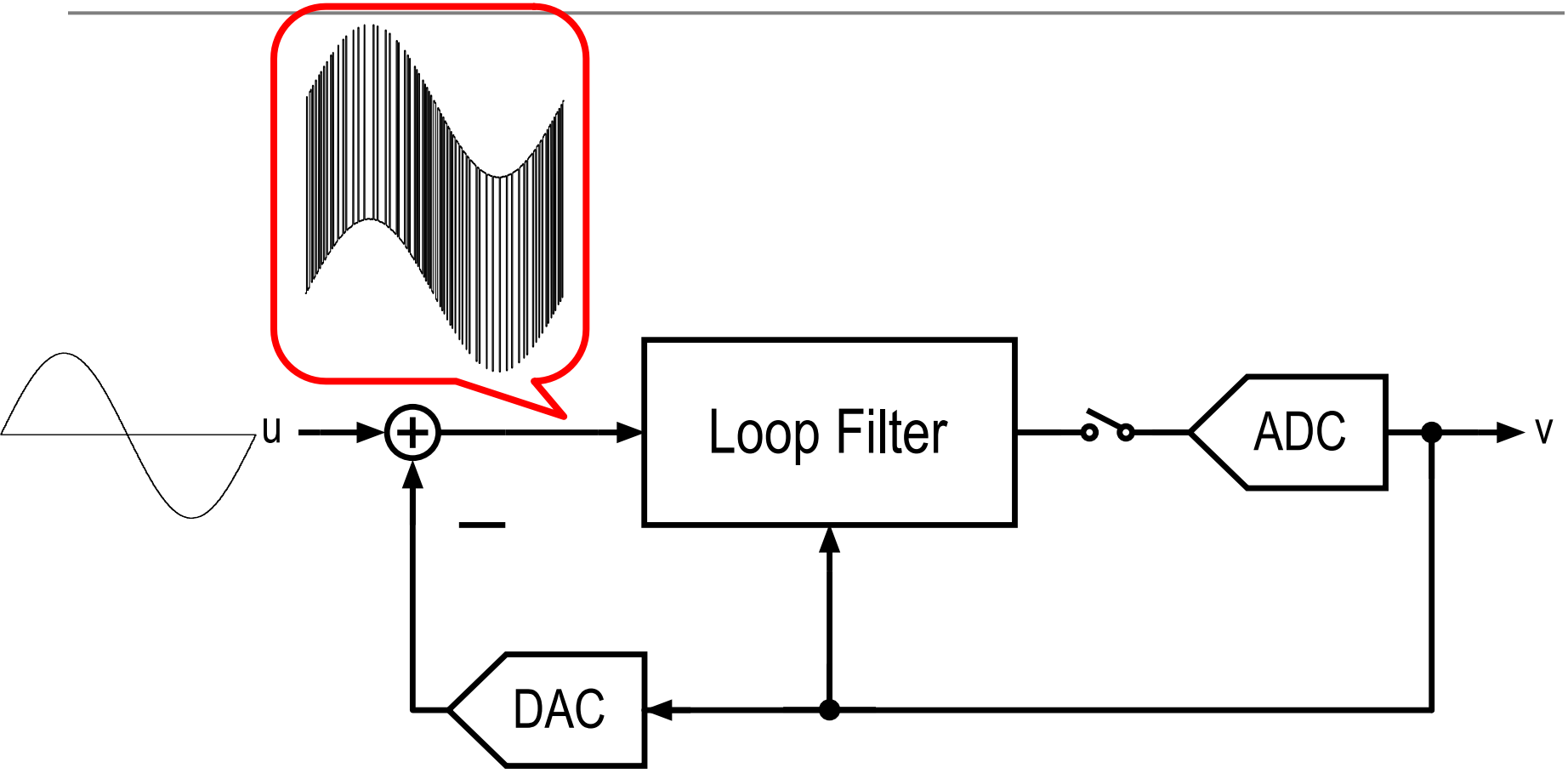


Large jitter error → rail-to-rail feedback waveform

Single-bit CTDSM Issues : Filter Linearity



Single-bit CTDSM Issues : Filter Linearity

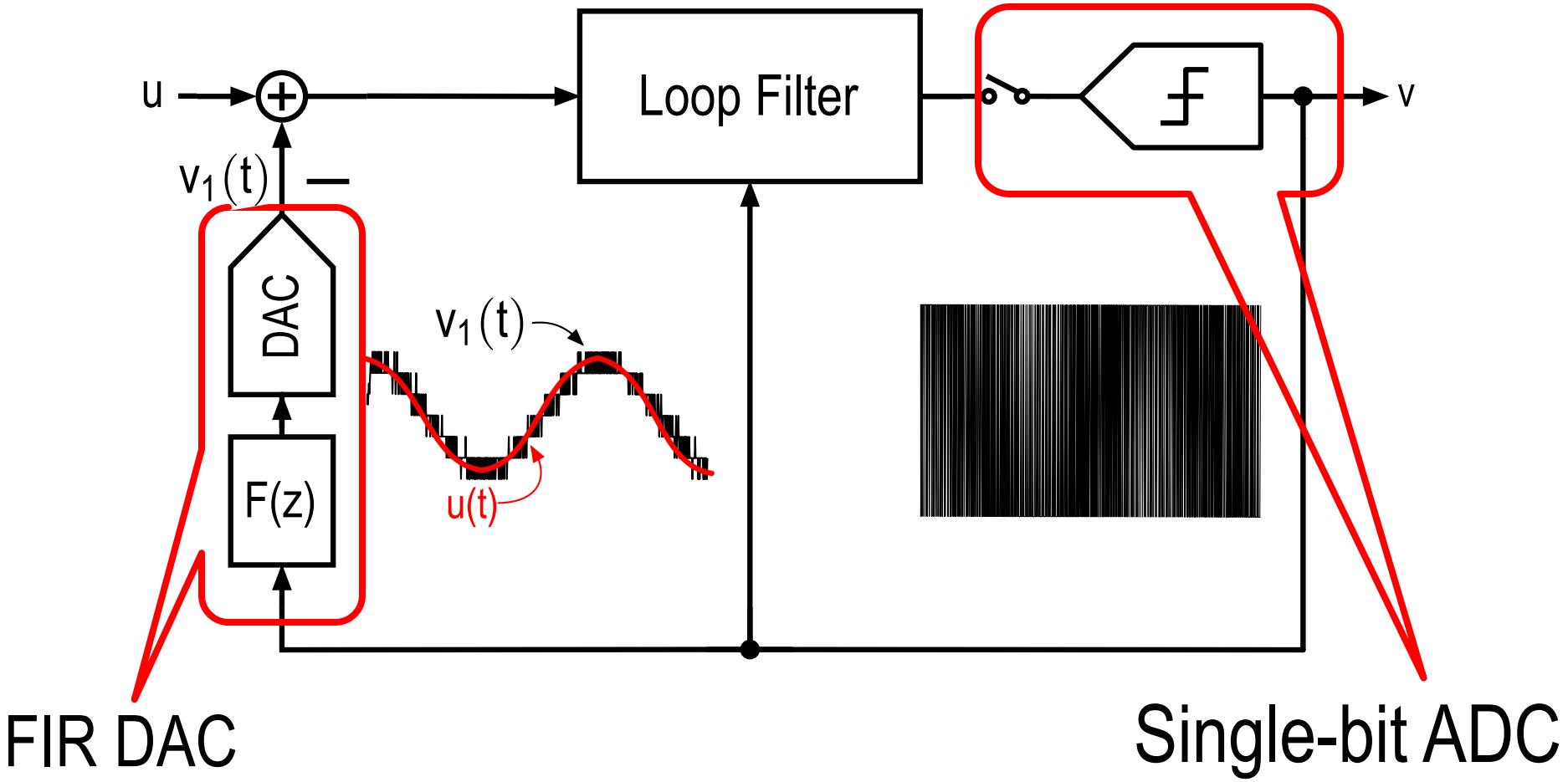


Increased loop filter power dissipation needed to achieve linearity

Summary so far …

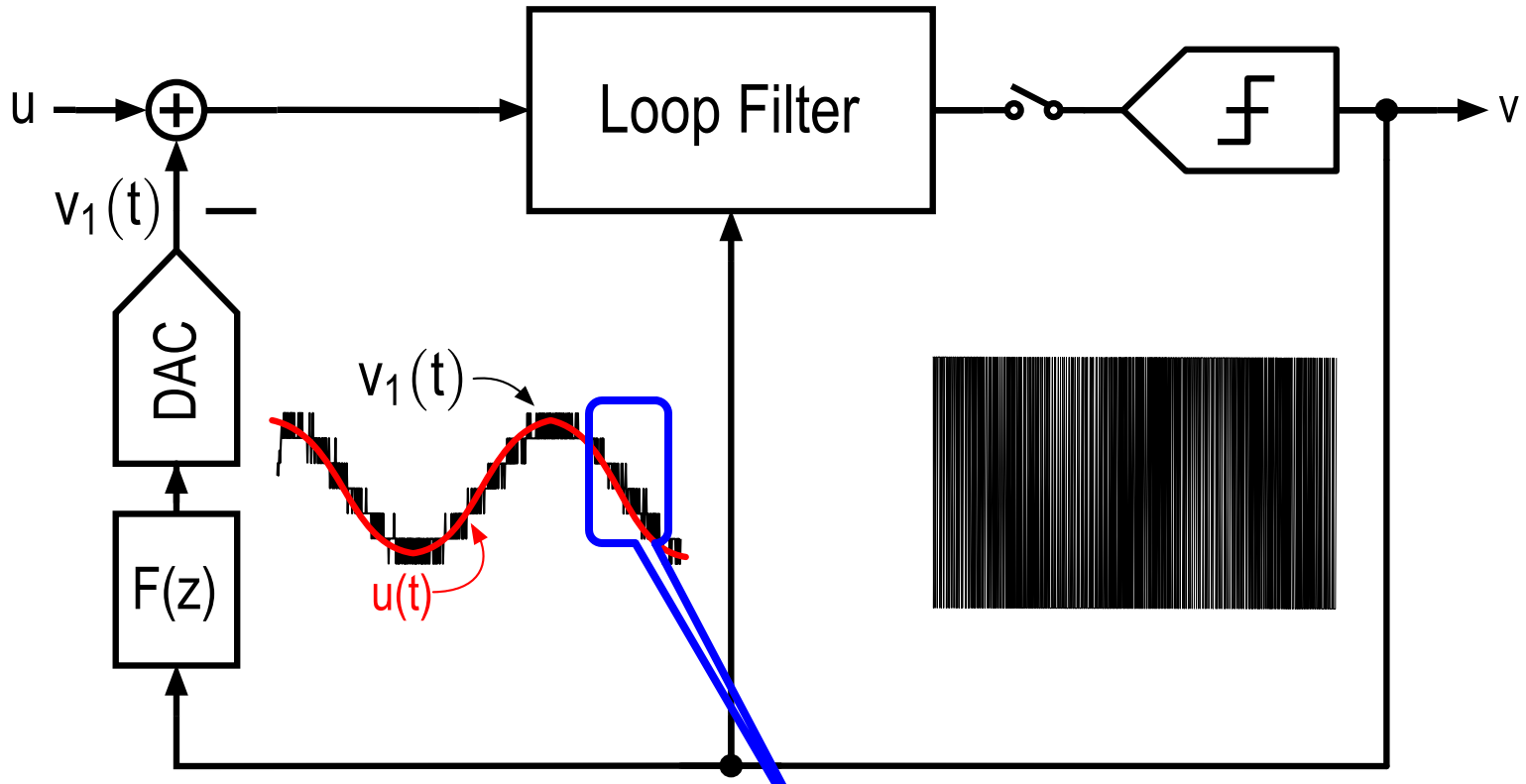
- Single bit operation
  - Very efficient quantizer
  - Easy to drive
  - Sensitive to clock jitter
  - Loop filter needs to handle large swings
    - Increased power dissipation

Improved Single-bit CTDSM : FIR Feedback



FIR filter in the feedback path

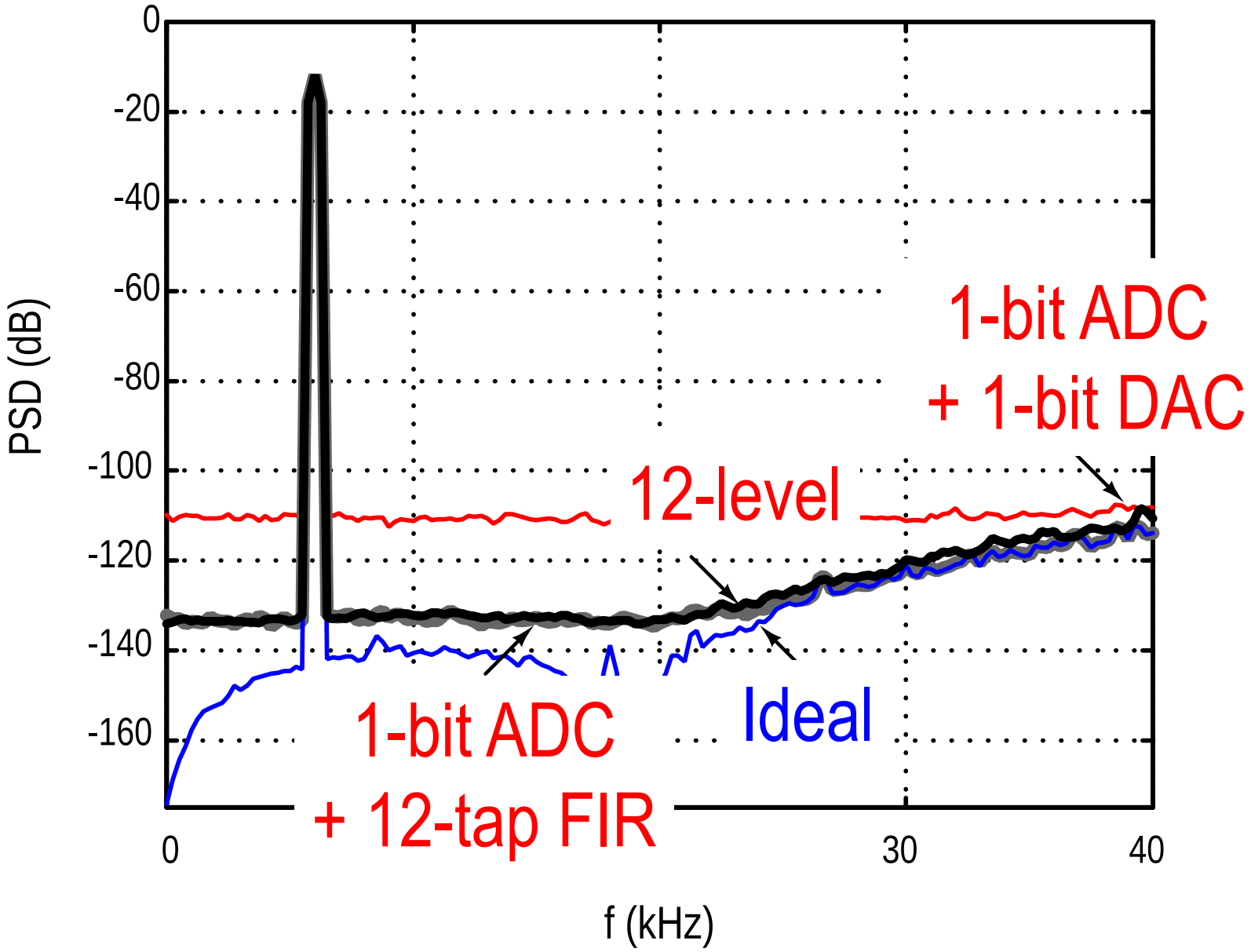
Improved 1-bit CTDSM : FIR Feedback



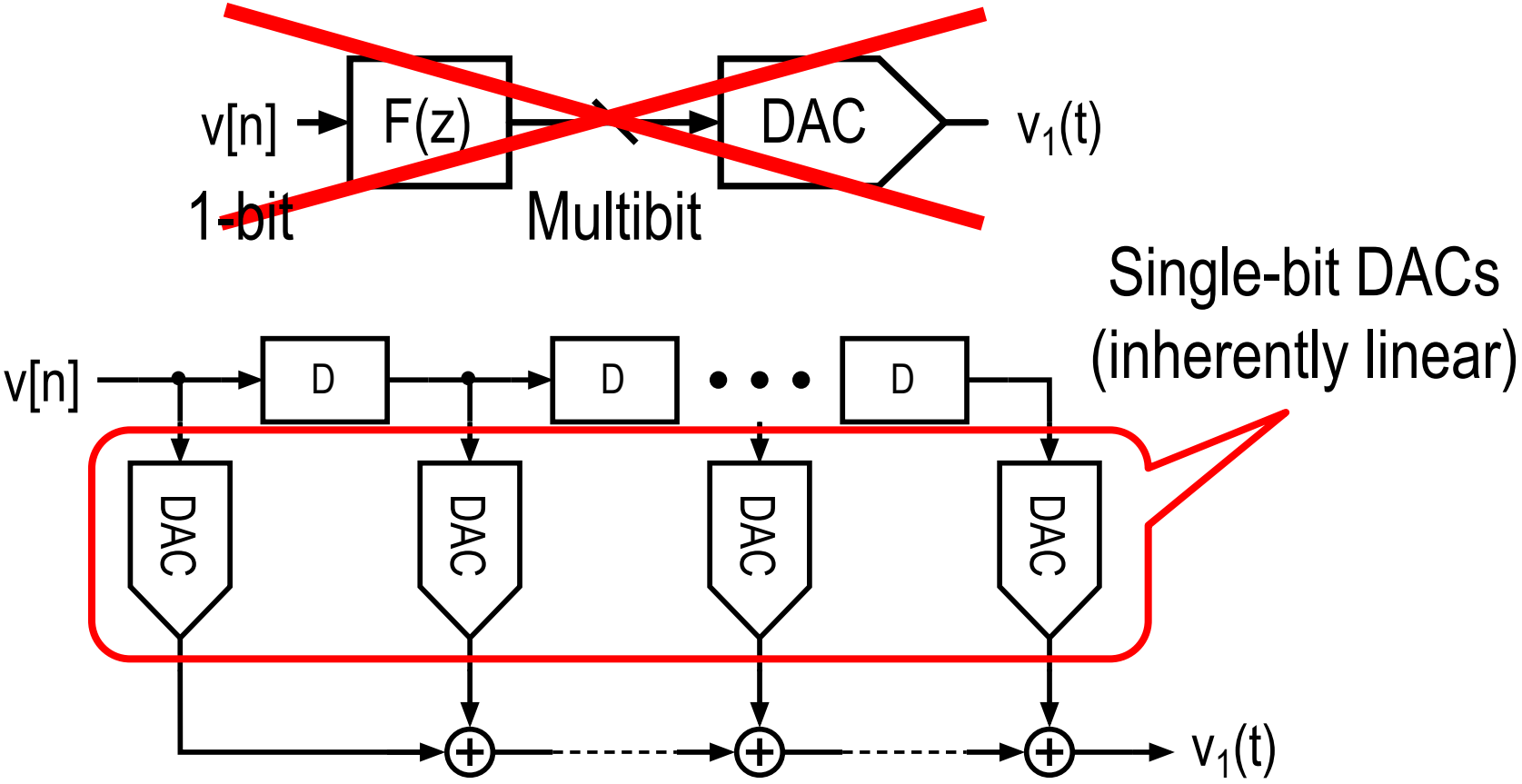
Height of steps → Greatly reduced

→ Reduced jitter sensitivity

Improved 1-bit CTDSM : FIR Feedback



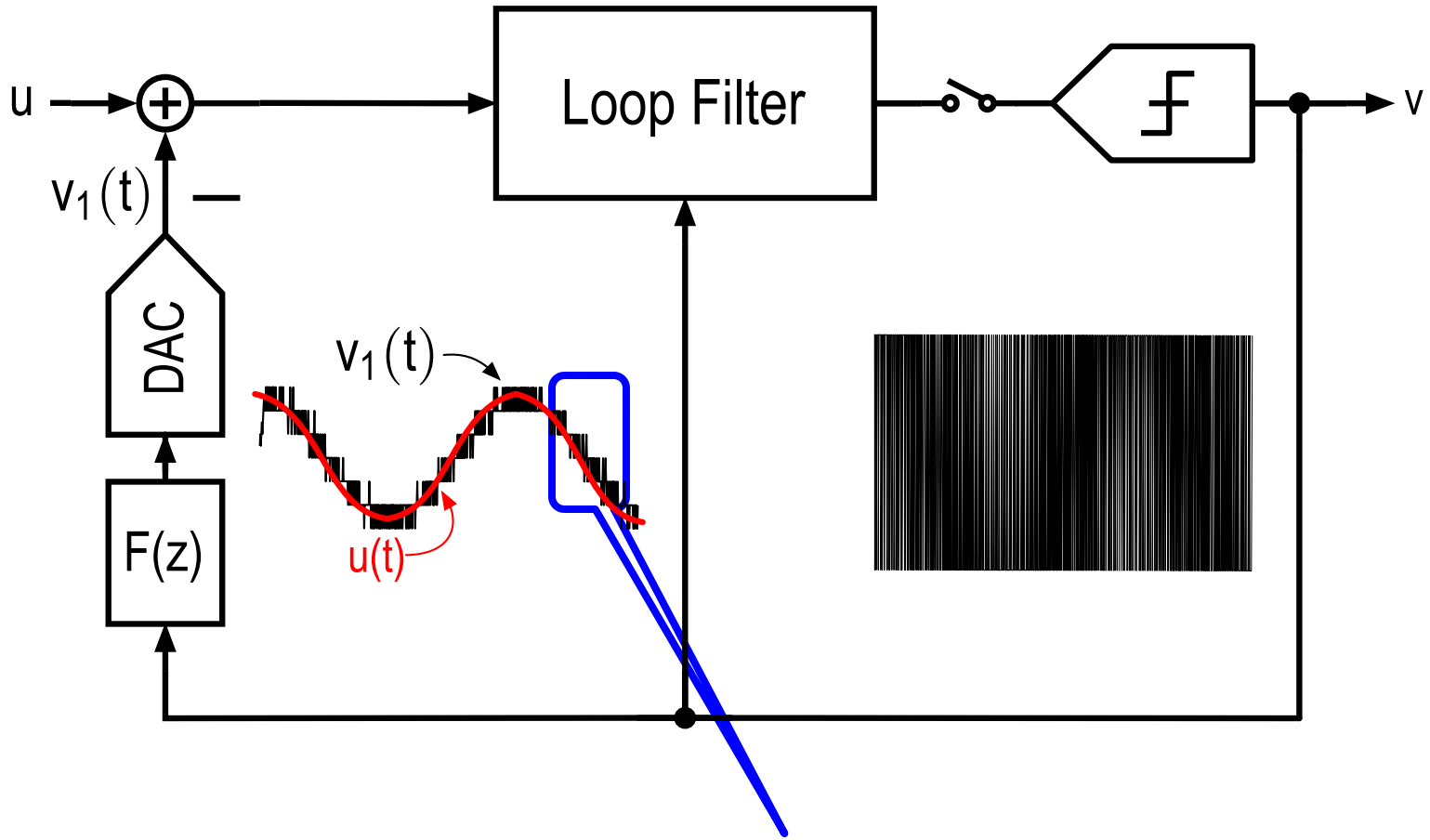
FIR DAC and Element Mismatch



Semi-digital Implementation

Mismatch does not lead to non-linearity

Improved 1-bit CTDSM : FIR Feedback



$u(t)-v_1(t)$ → very small

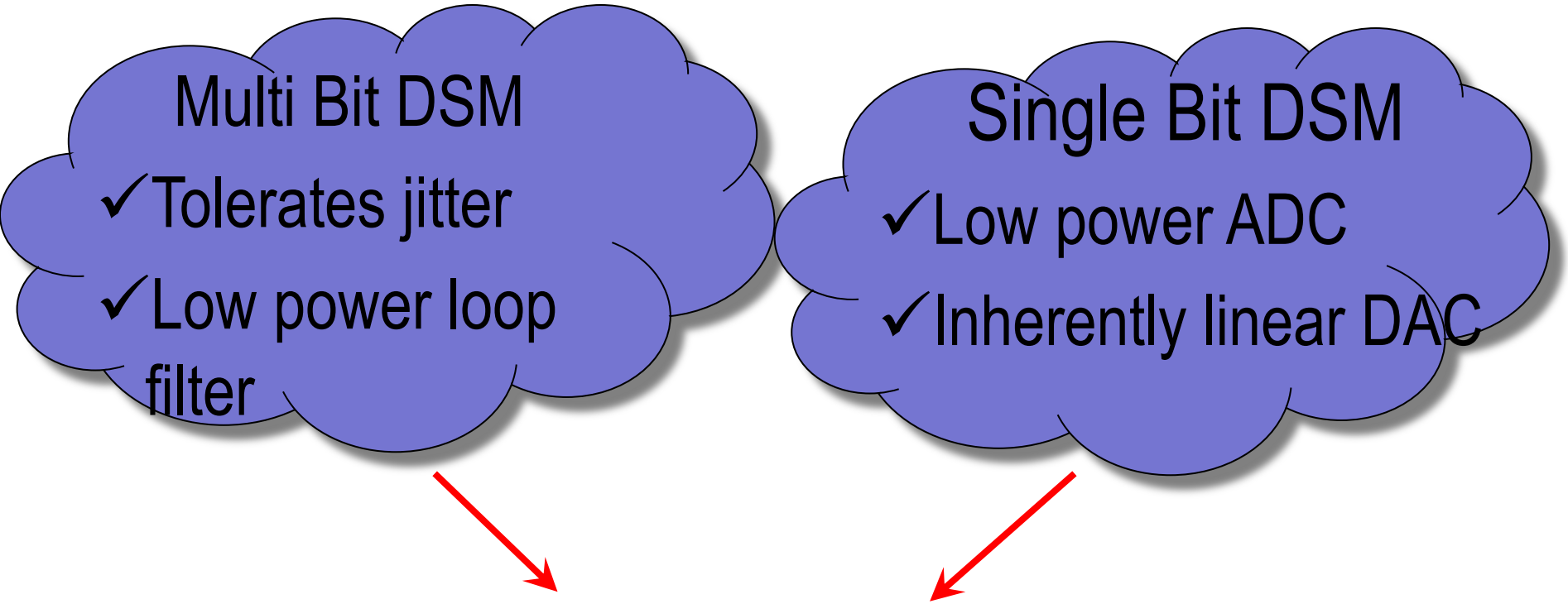
→ Improved loop filter linearity

Summary so far …

- Single bit ADC + FIR DAC
  - Low power ADC, easy to drive
  - Inherently linear DAC, no DEM
  - Low jitter sensitivity
  - Improved loop filter linearity

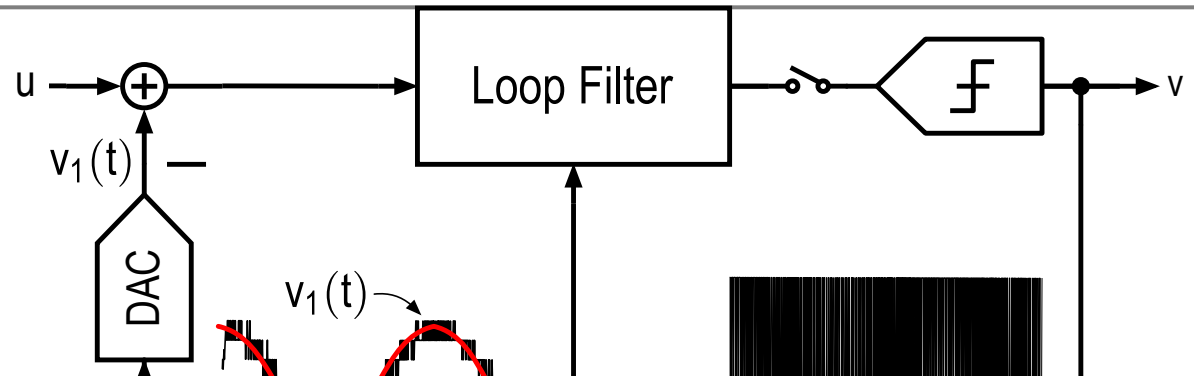
Benefits of single-bit operation

Key Takeaway



Single-bit ADC + FIR DAC combines benefits of 1-bit and multi-bit operation

Single-bit ADC + FIR DAC



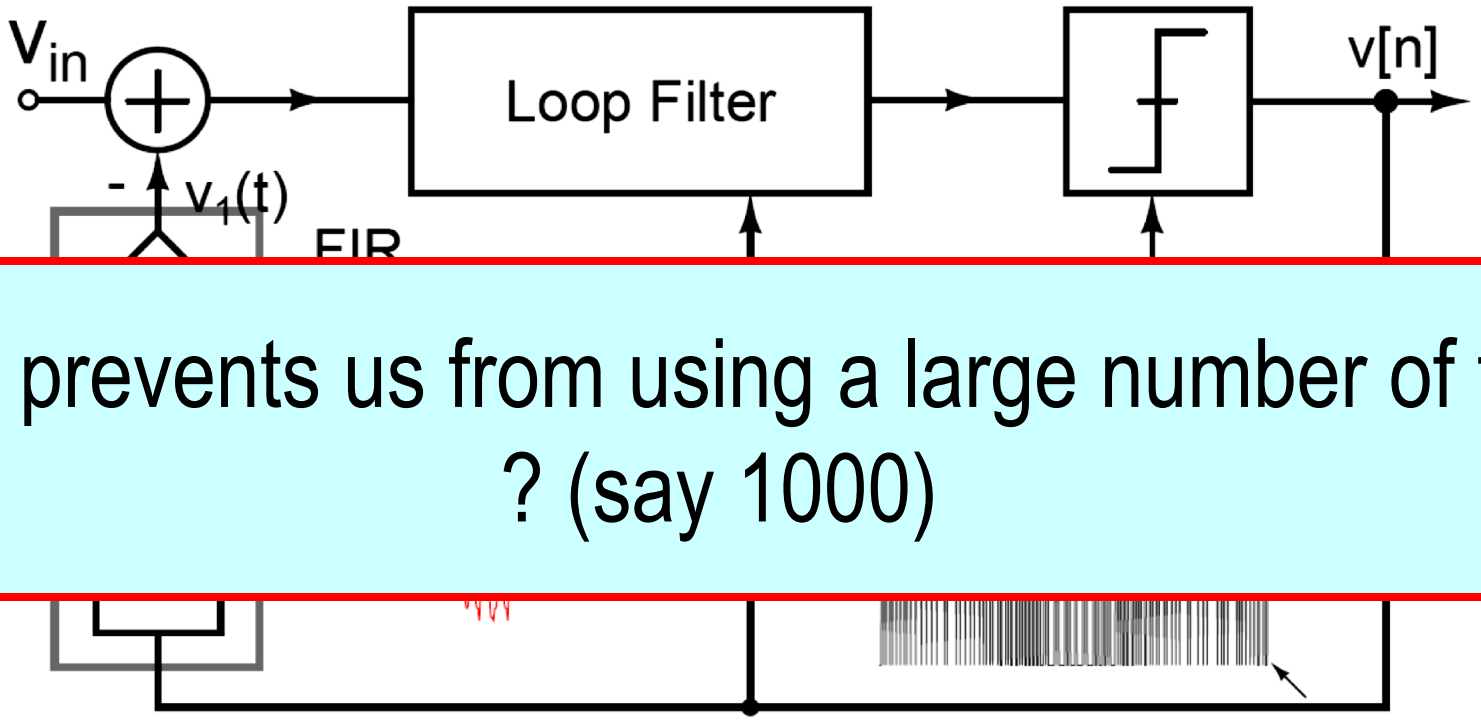
(G)old Idea :
B.Putter, ISSCC 2003; O.Oliaei, TCAS-II 2003

- but dormant for a long while – why?
  - (?) Multibit & DEM well established by 2003
  - (?) More difficult to understand
  - (?) Stability

FIR DAC Summary

- Low power loop ADC
- Simple DAC – no DEM
- Multilevel feedback waveform
  - Improved loop filter linearity
  - Reduced clock jitter sensitivity
- Performance benefits of a multibit quantizer
  - But with low power

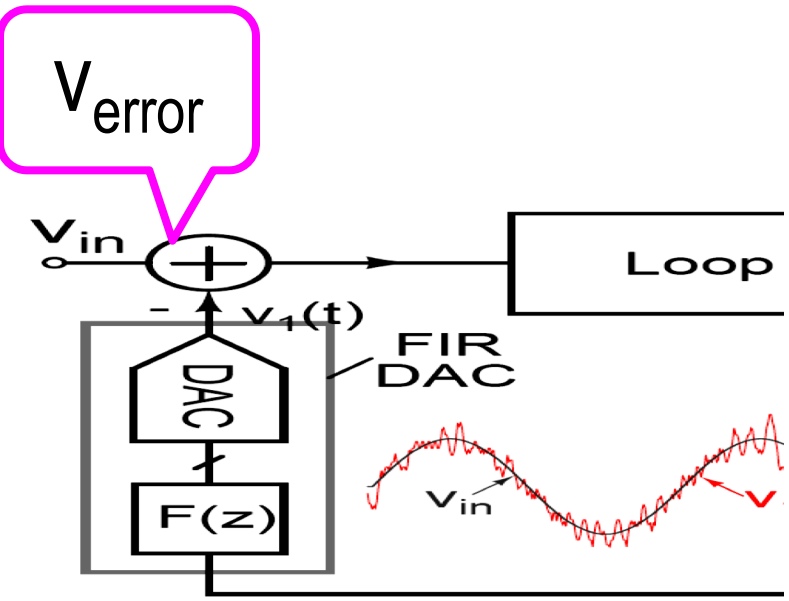
FIR DAC : Number of taps

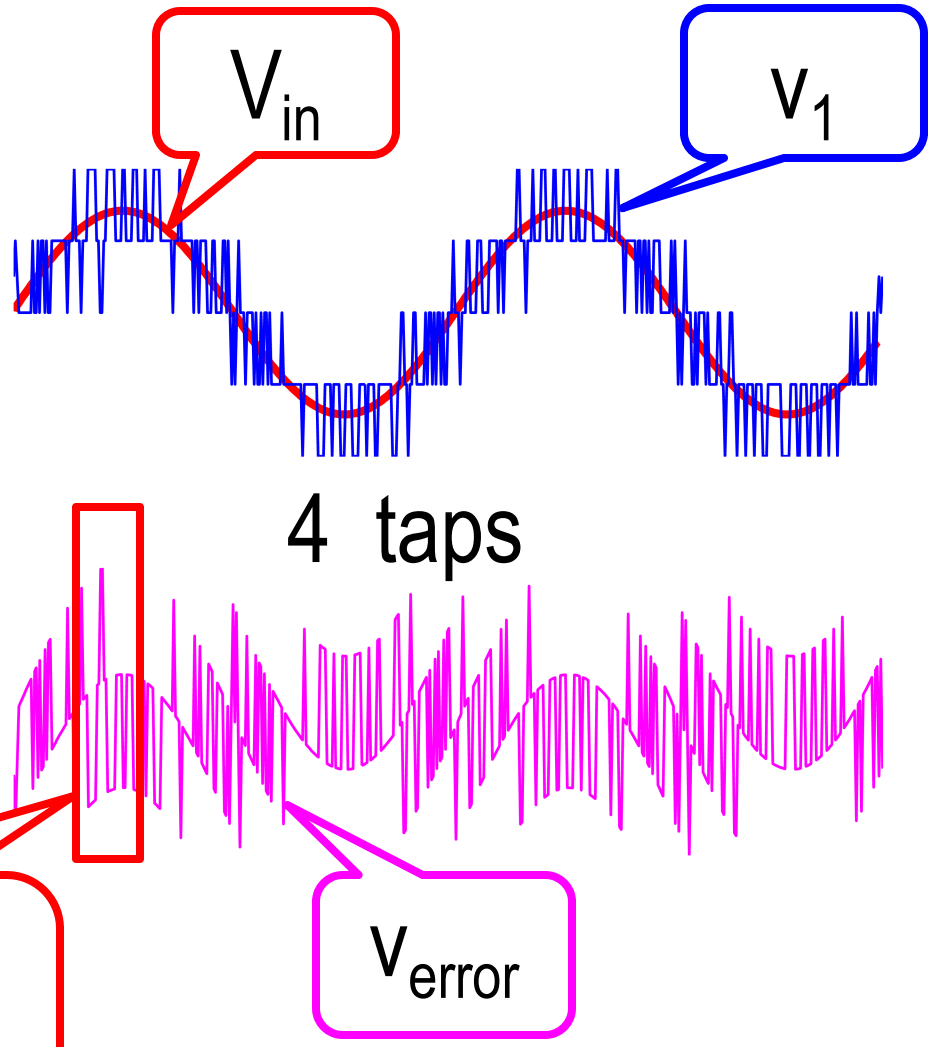


What prevents us from using a large number of taps ? (say 1000)

- More FIR taps → Better filtering
- →Reduced clock jitter sensitivity, better linearity

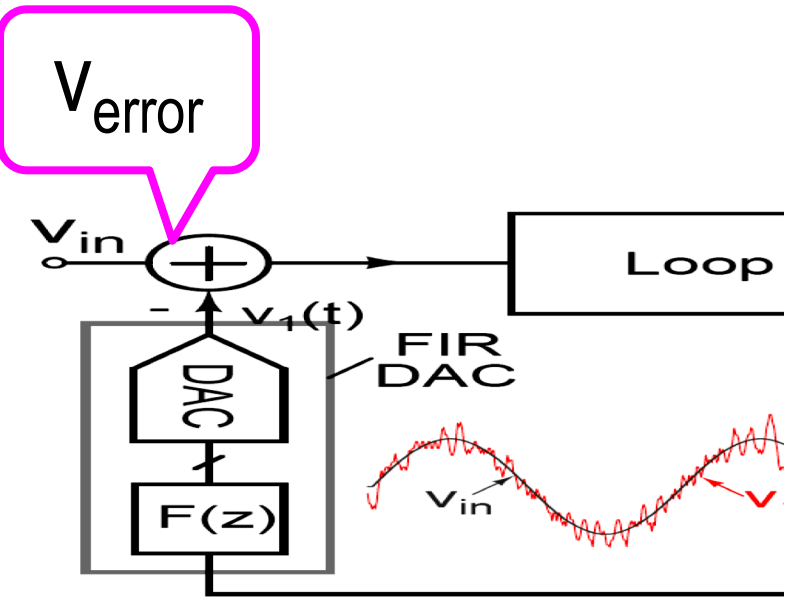
Increasing FIR Length

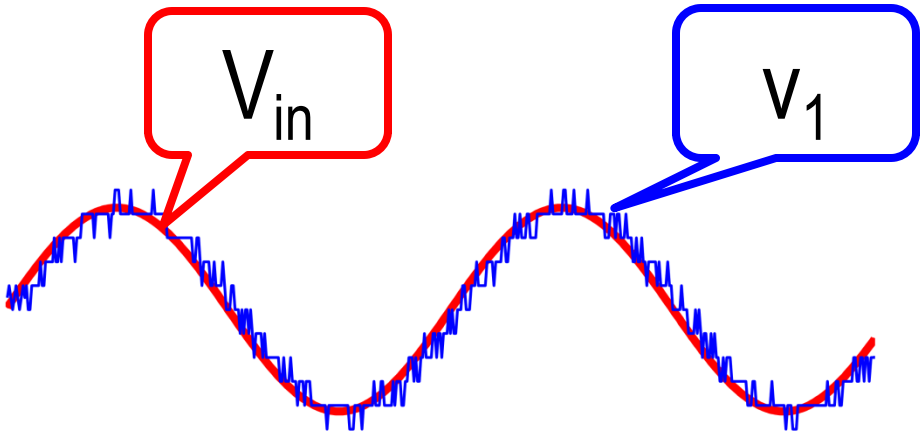




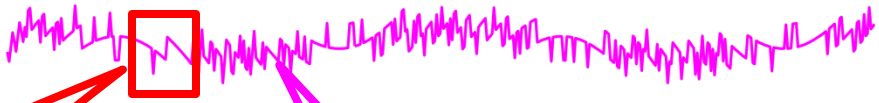
Large v_{error} due to inadequate filtering of shaped quantization noise

Increasing FIR Length





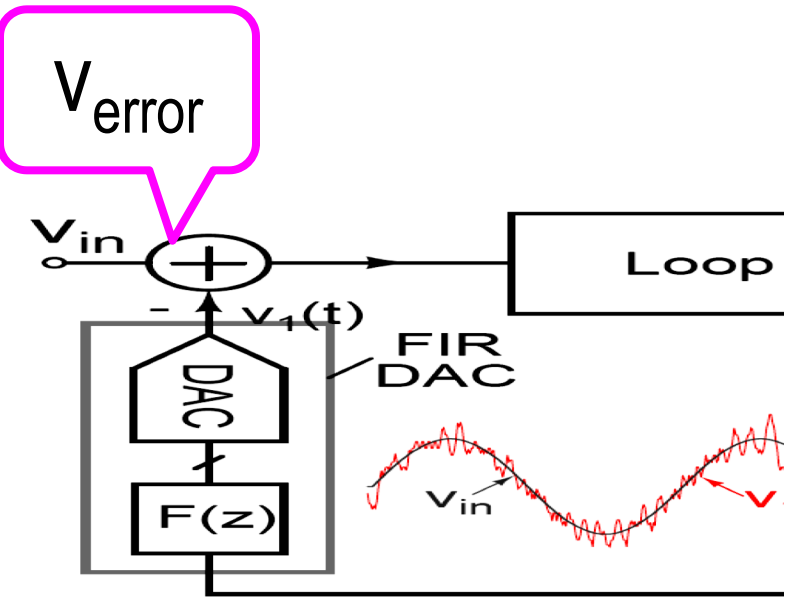
12 taps

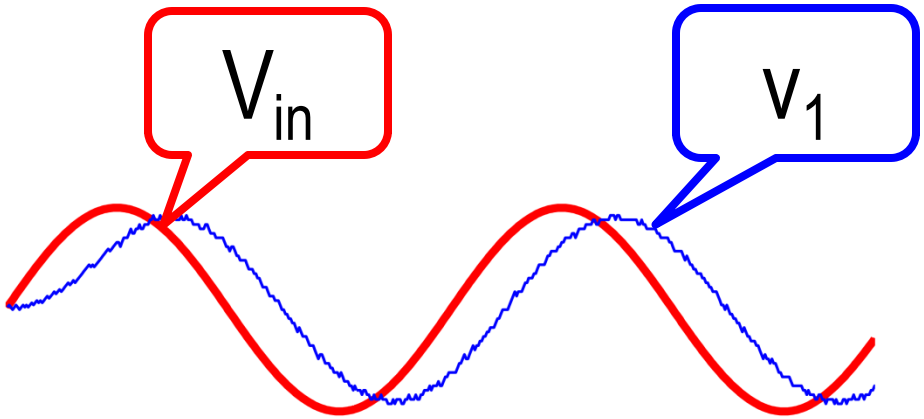


Smaller v_{error} due to better filtering

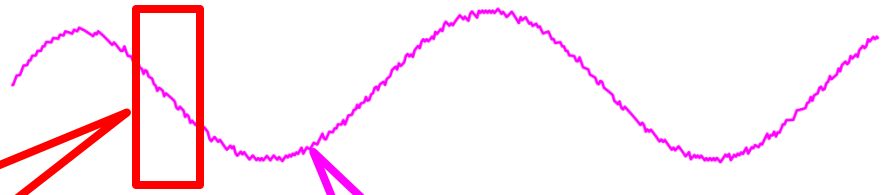
V_{error}

Increasing FIR Length





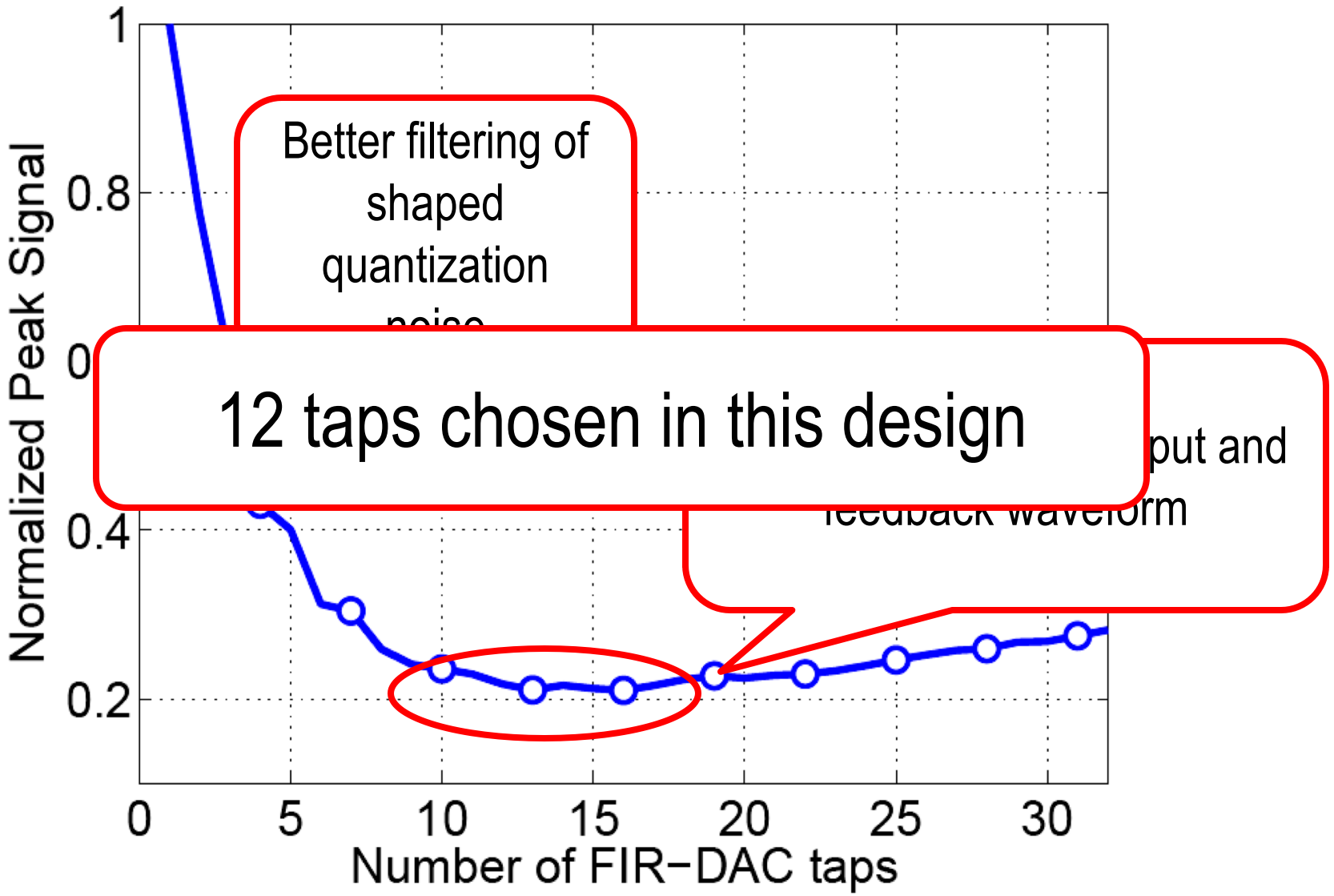
64 taps



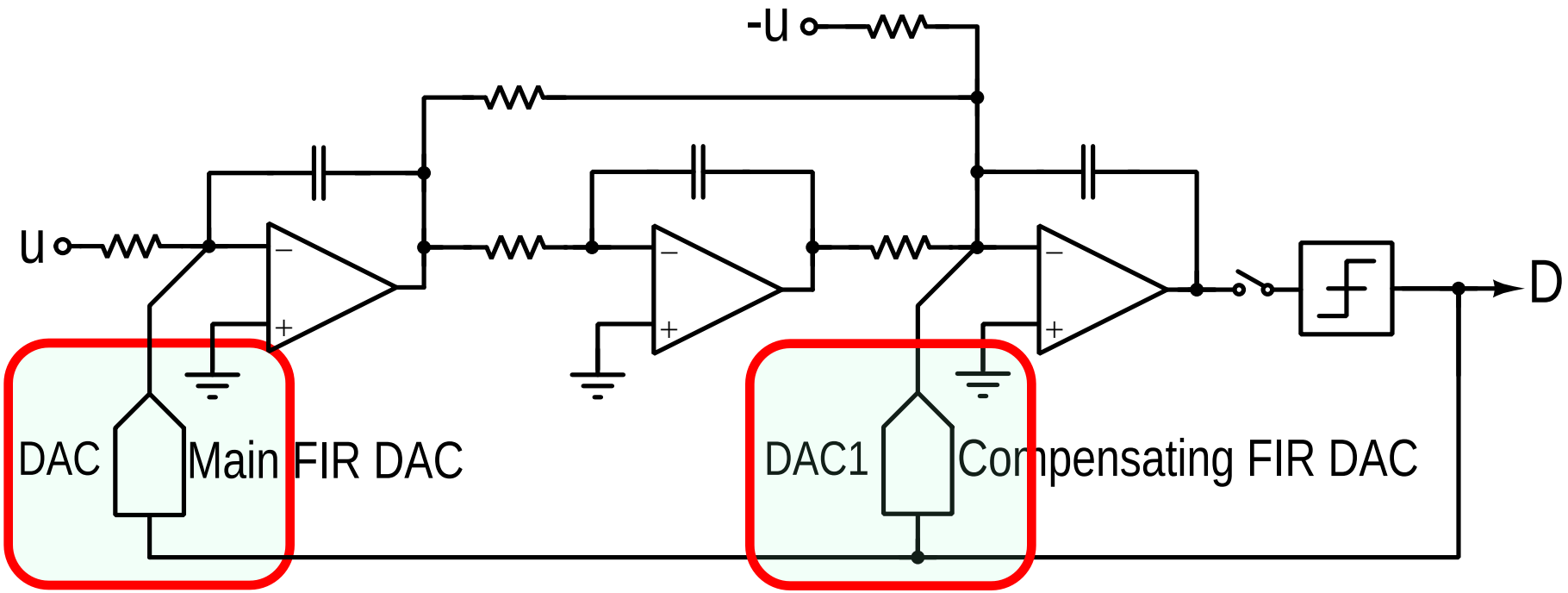
Large v_{error} due to higher phase shift

V_{error}

Error Signal Magnitude



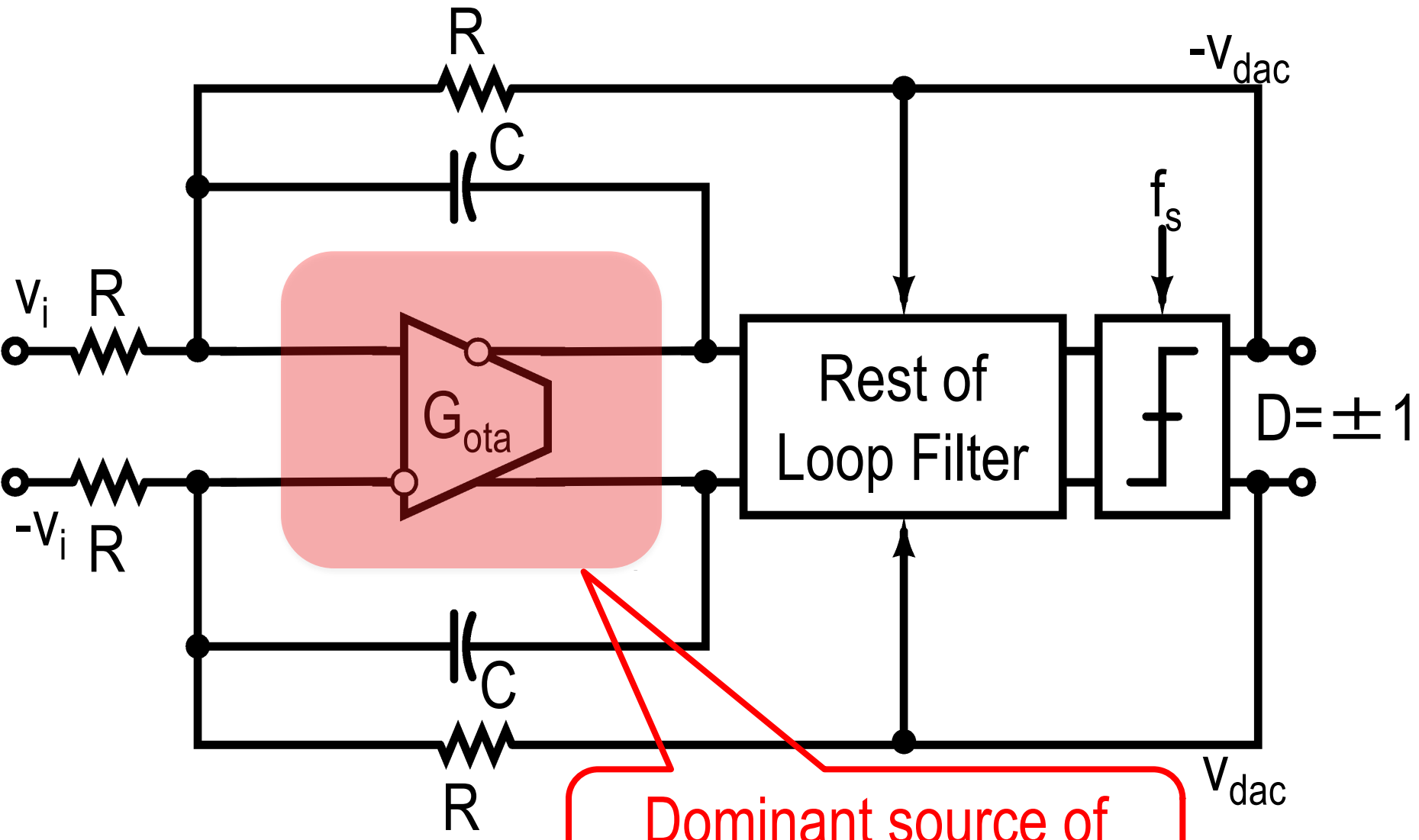
Modulator Architecture



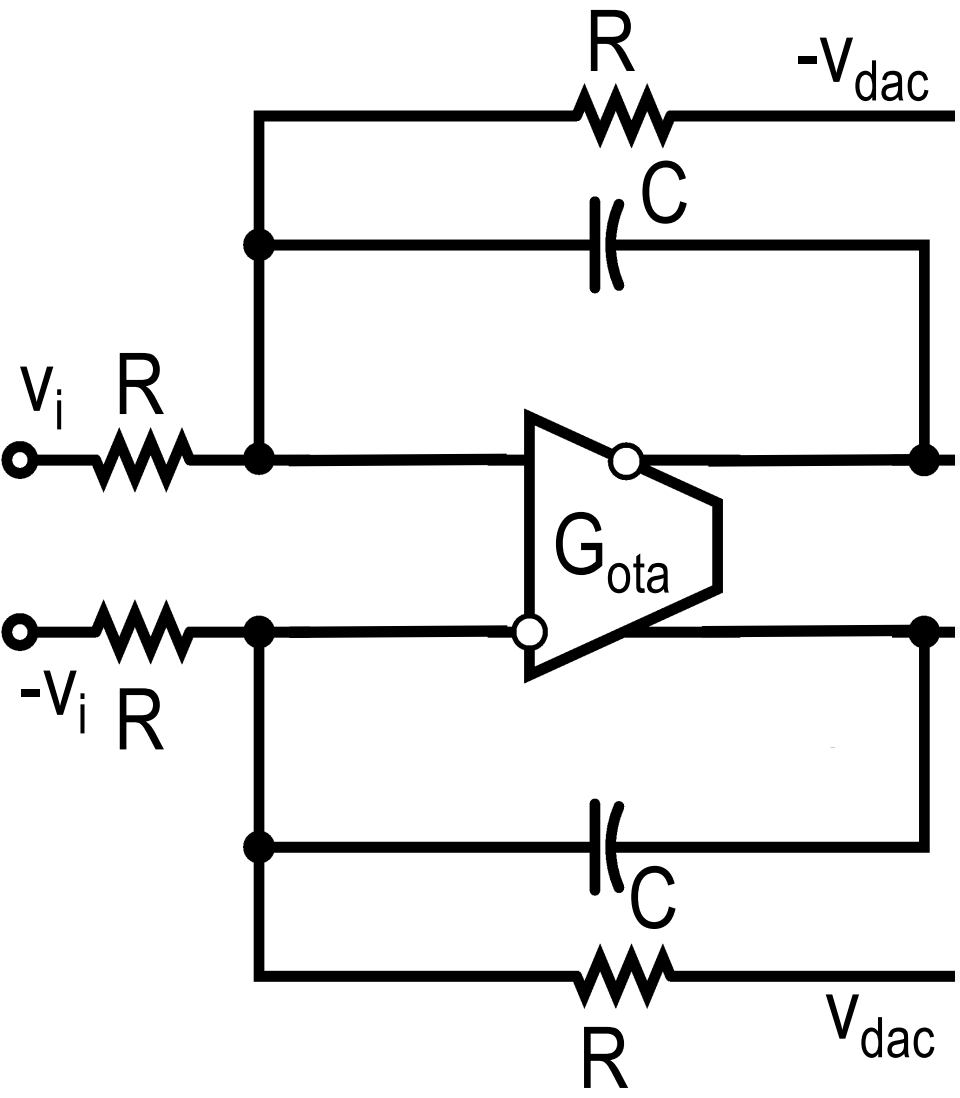
Third Order CIFF-B Prototype

FIR Feedback : More Benefits

1/f Noise in CTDSMs



1/f Noise Mitigation in CTDSMs



Brute Force Solution

- Increase device sizes

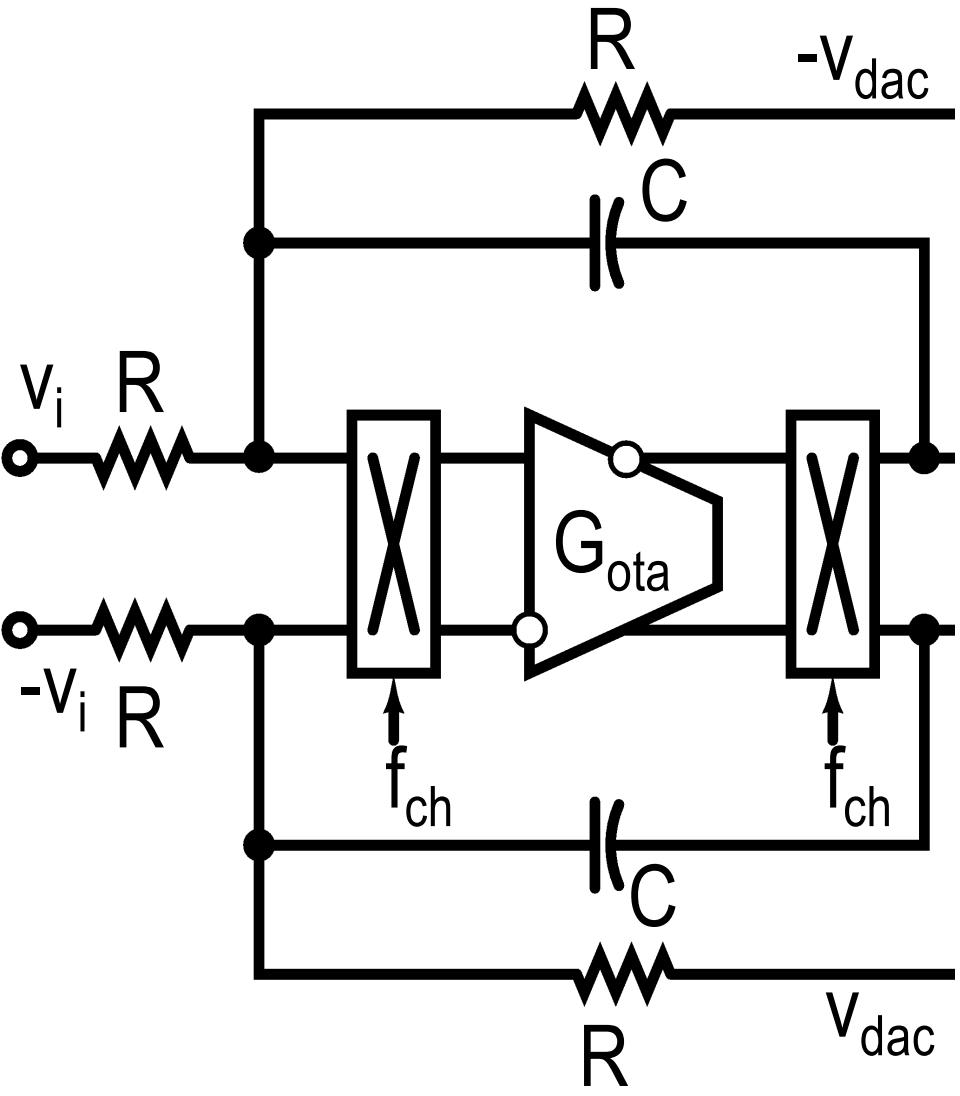
→ Increased parasitics

→ Reduced loop gain

→ Higher distortion

→ Higher area

1/f Noise Mitigation in CTDSMs

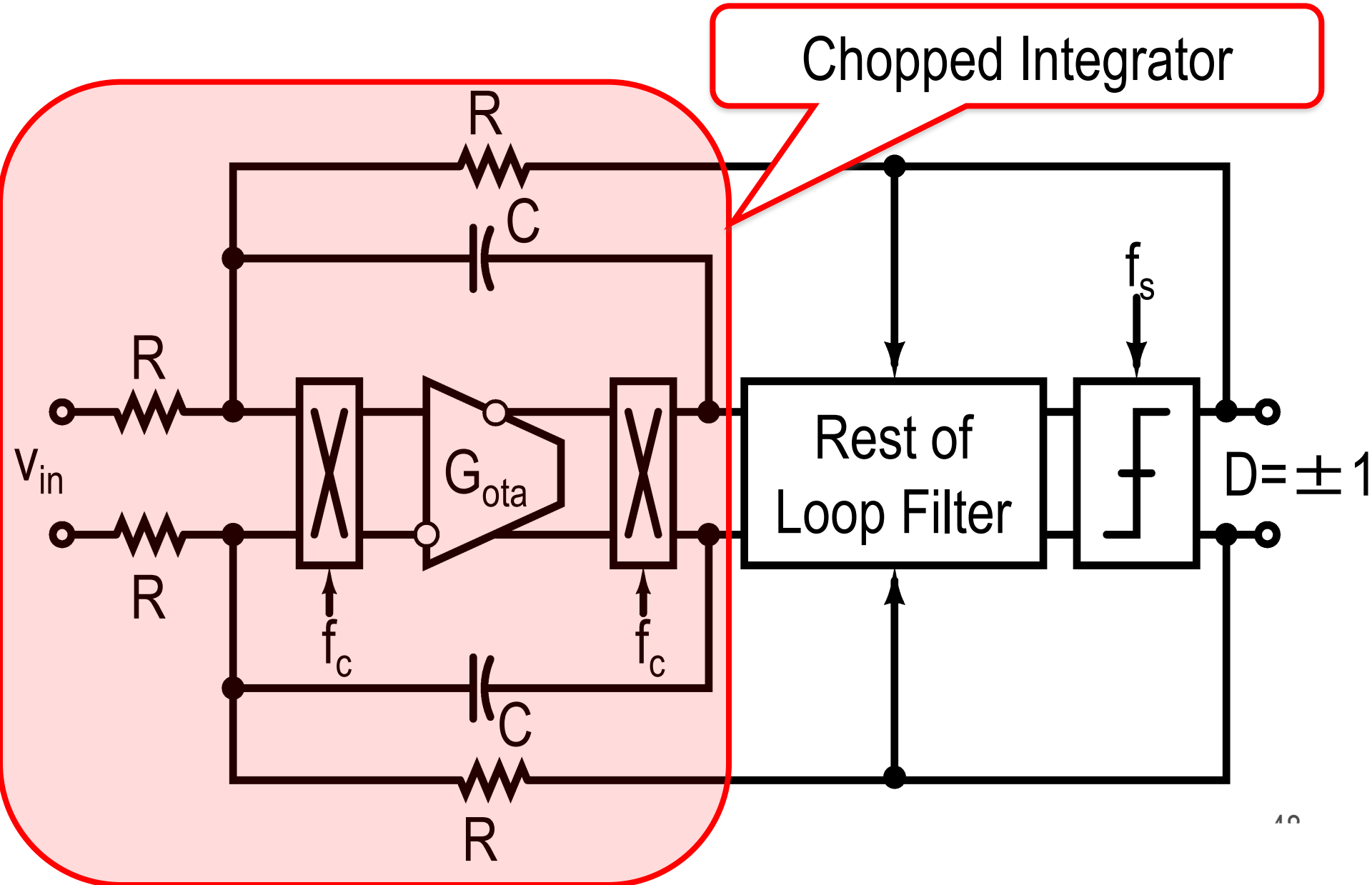


Chopping

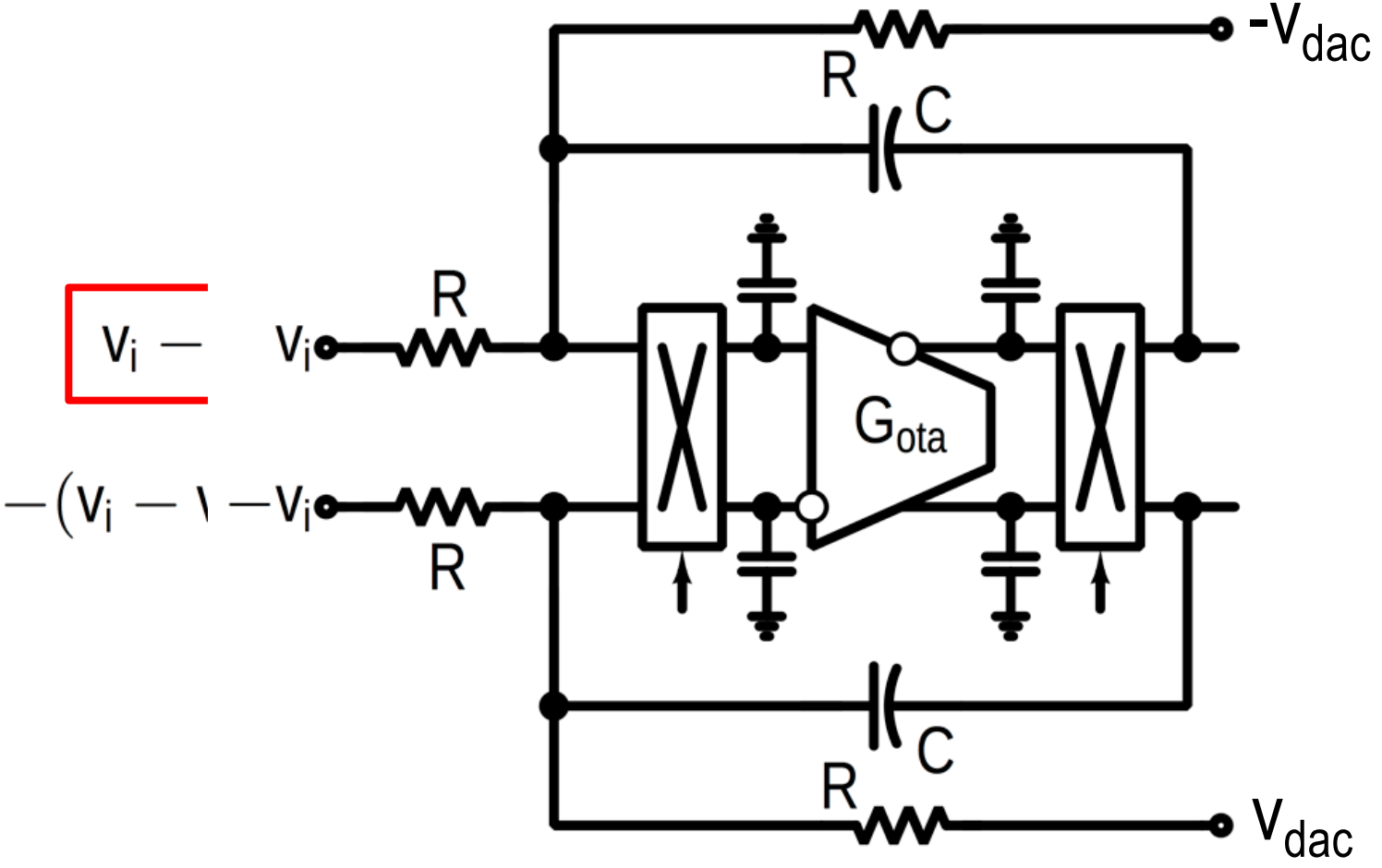
- Modulates 1/f noise out of the signal band

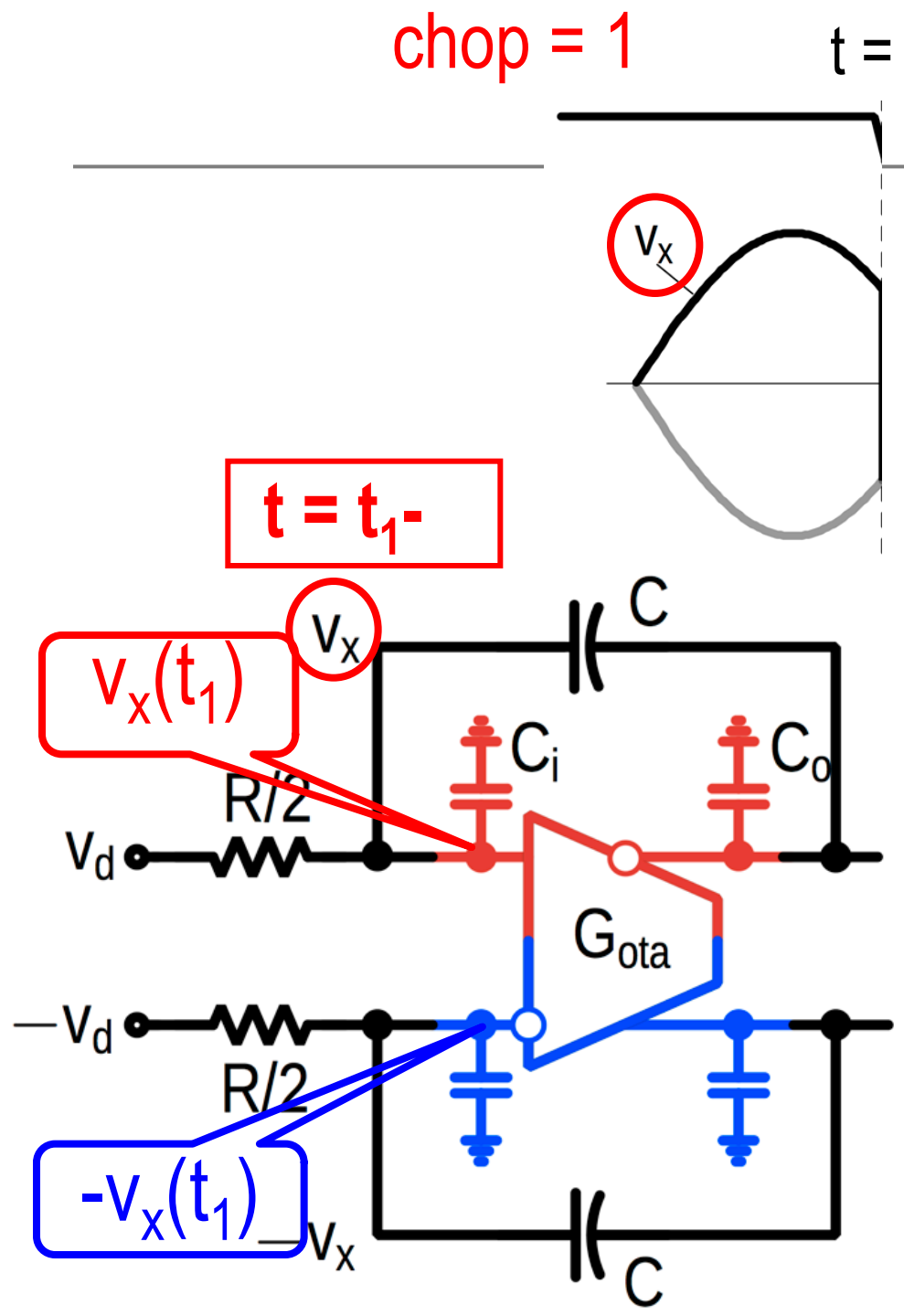
Chopping in CT ΔΣ-Modulators

Chopping in a CTΔΣM



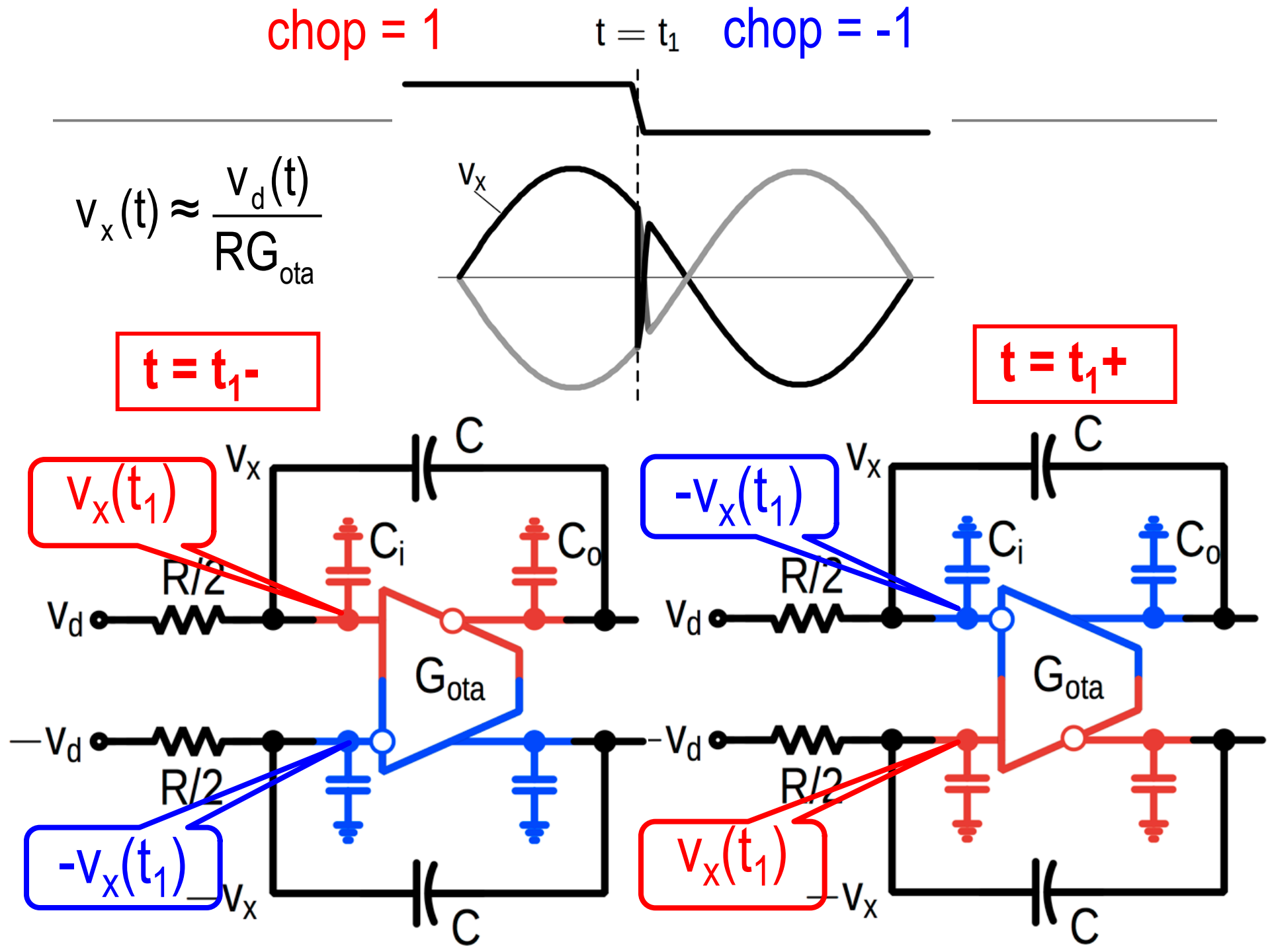
Chopping in a CTΔΣM



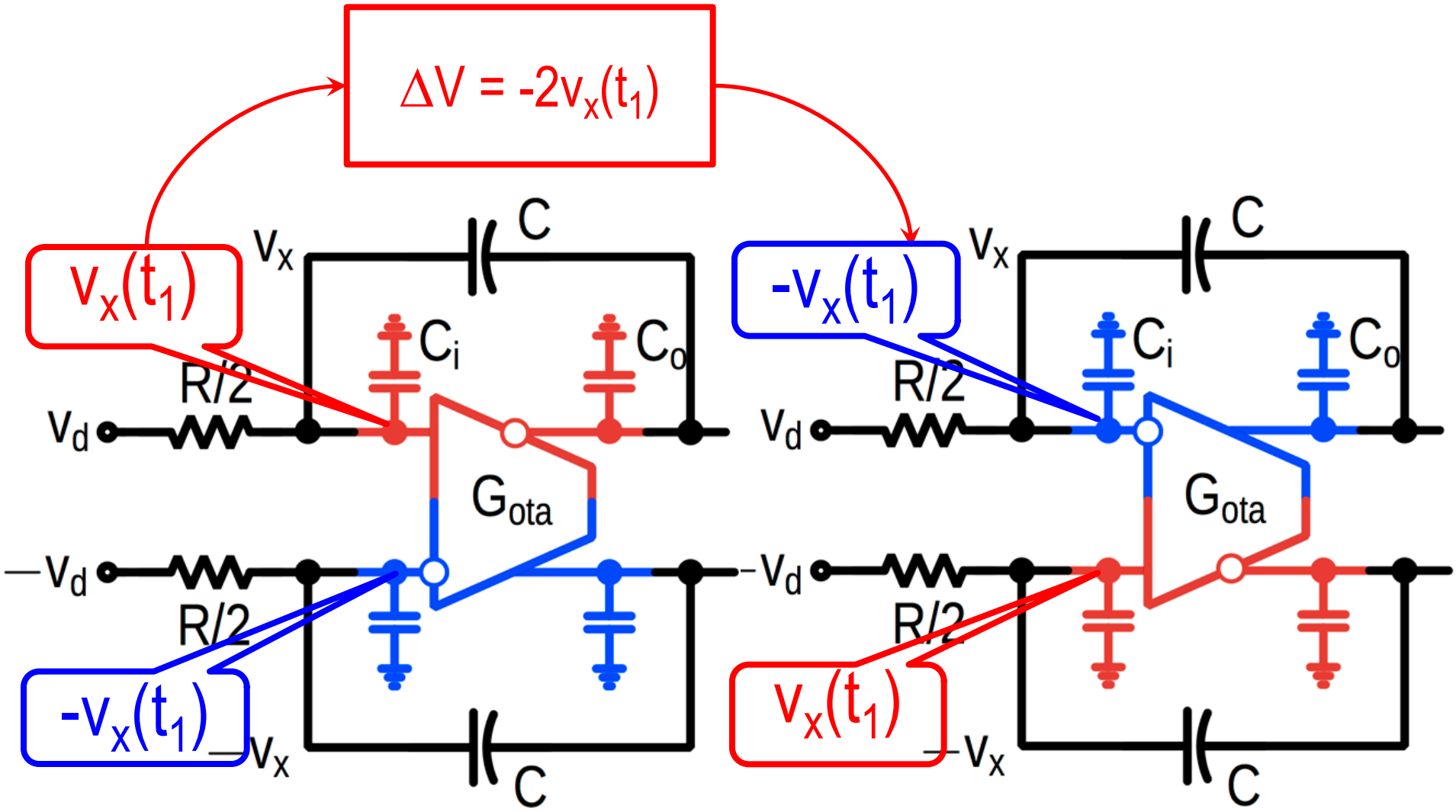


$$v_x(t) \approx \frac{v_d(t)}{RG_{ota}}$$

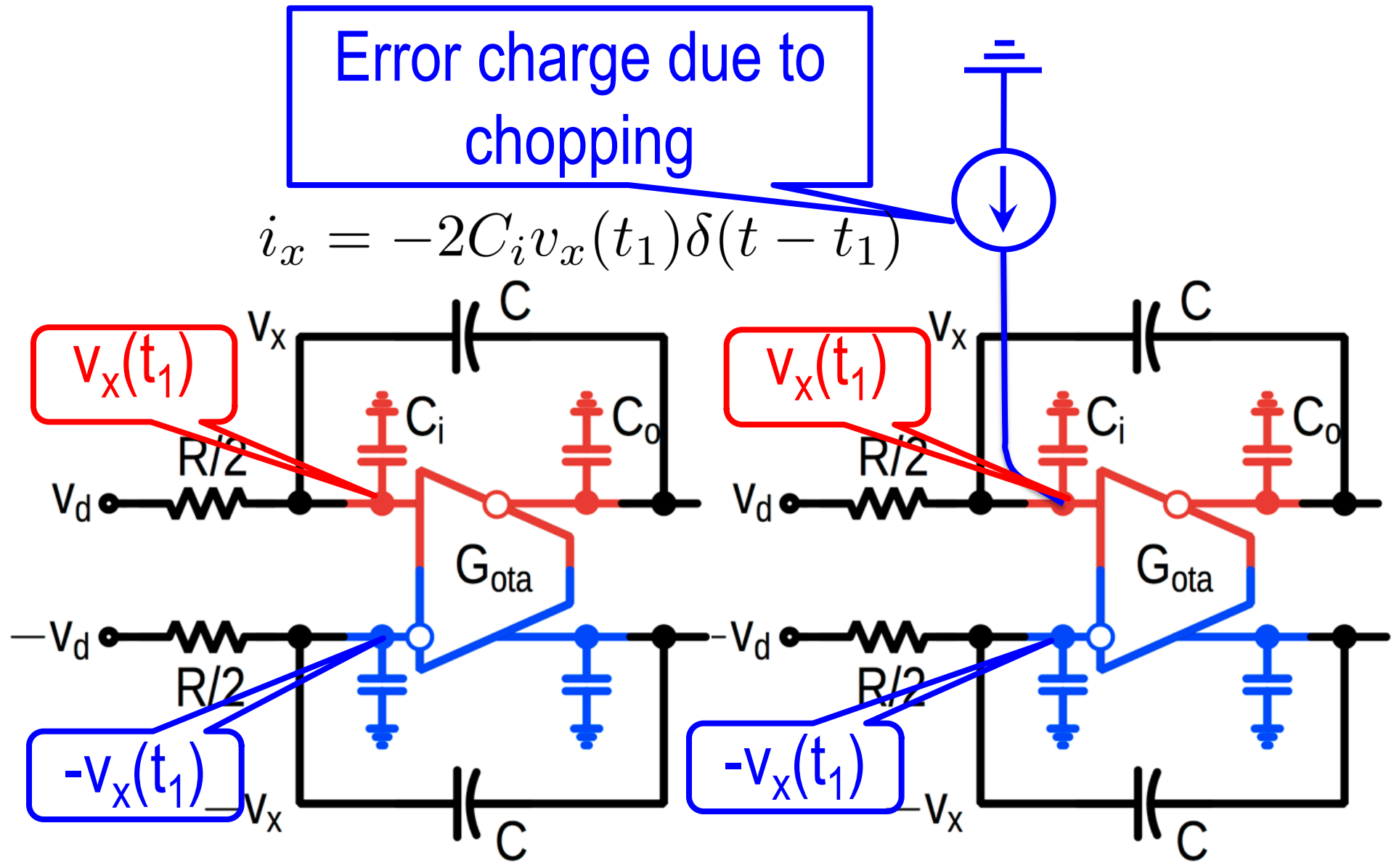
Chopping transition at $t = t_1$


chop = 1
t = t1
chop = -1
vx(t) ≈ vd(t) / RGota
vx
t = t1-
t = t1+
C
vx
Ci
Co
R/2
vd
Gota
-vd
-vx(t1)
vx(t1)
-vx

At **EVERY** transition of the chopping clock



At EVERY transition of the chopping clock



Error Model of a Chopped Integrator

$$i_x = -2C_i v_x(t_1)\delta(t - t_1)$$

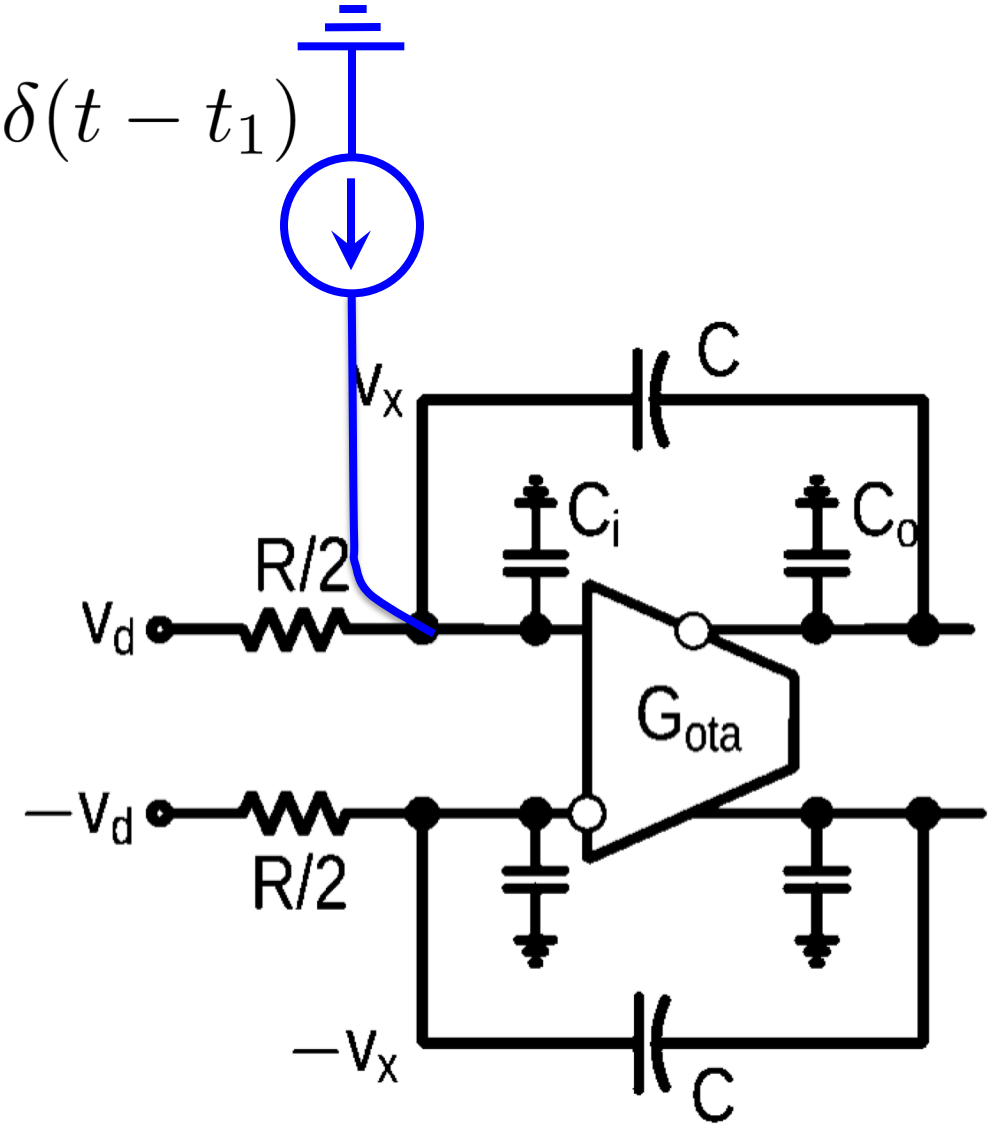
OTA input parasitic

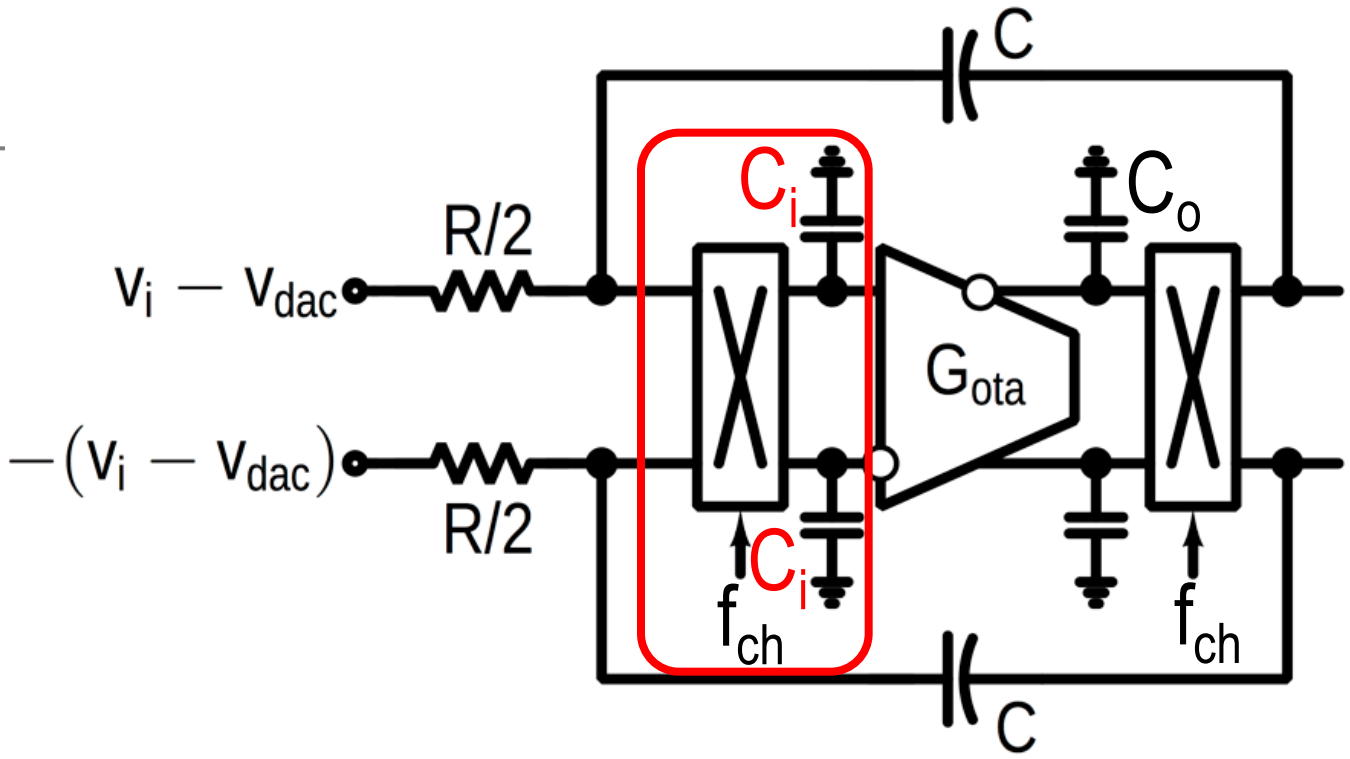
Virtual Ground

Voltage

Sampled at chopping edge

$$v_x \approx \frac{v_d}{RG_{ota}}$$

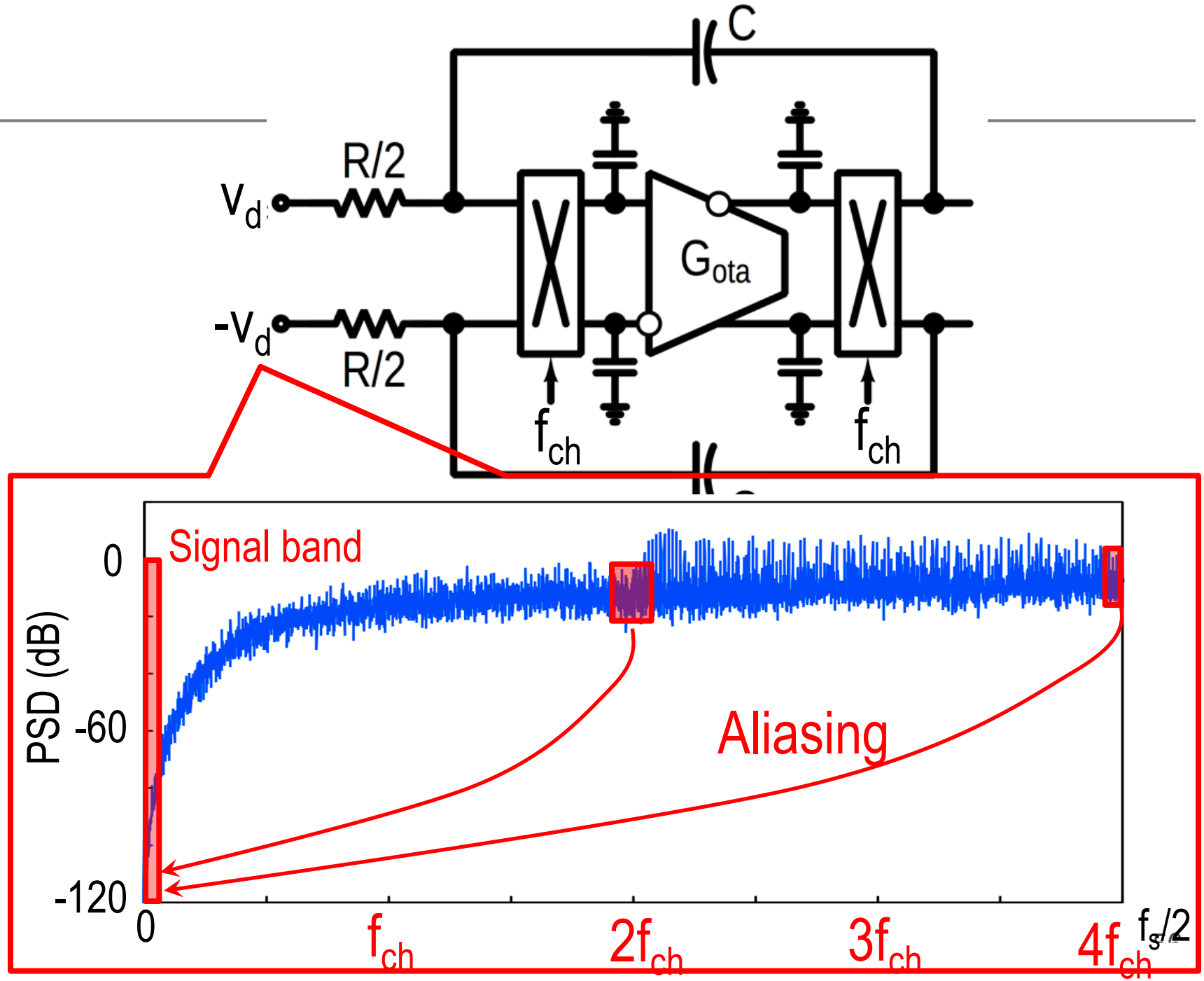


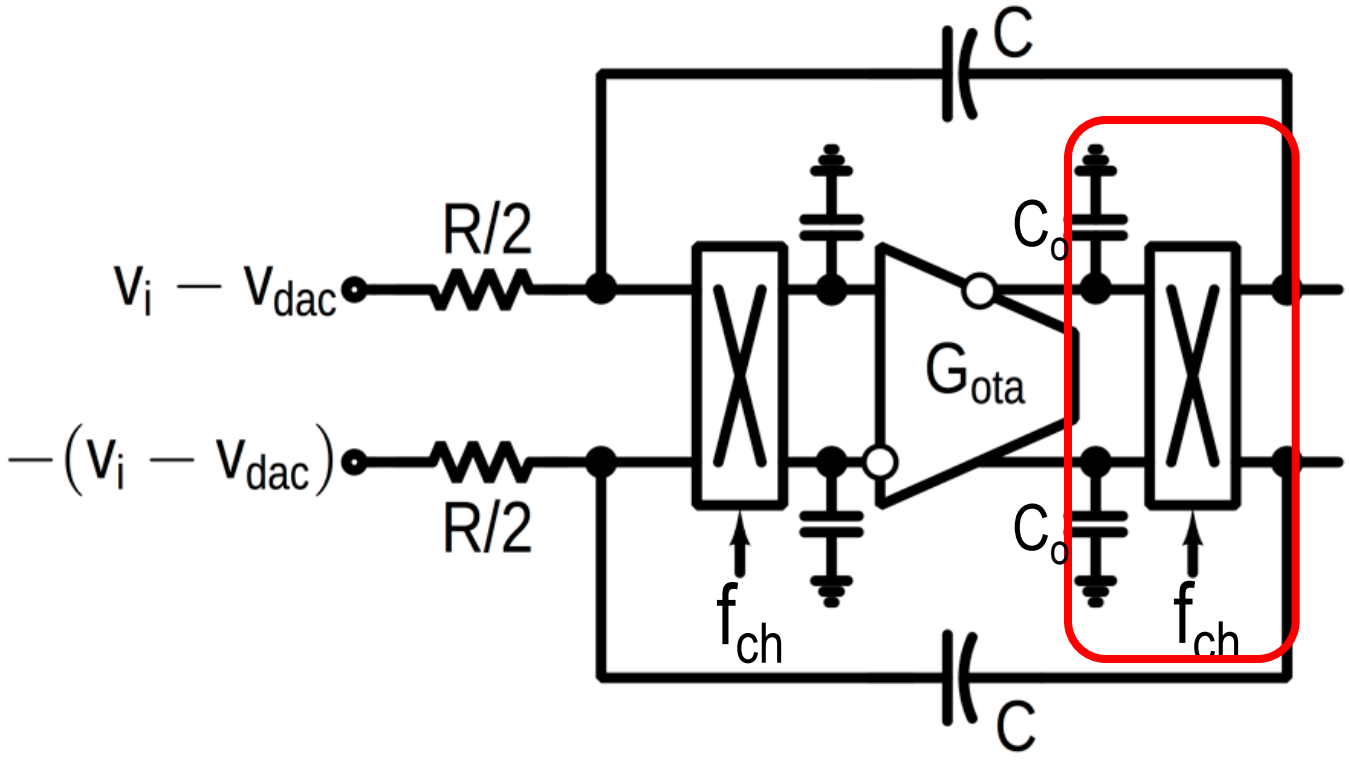


Error current injected at **every edge** of f_{ch}

→Sampling the virtual ground at $2f_{ch}$

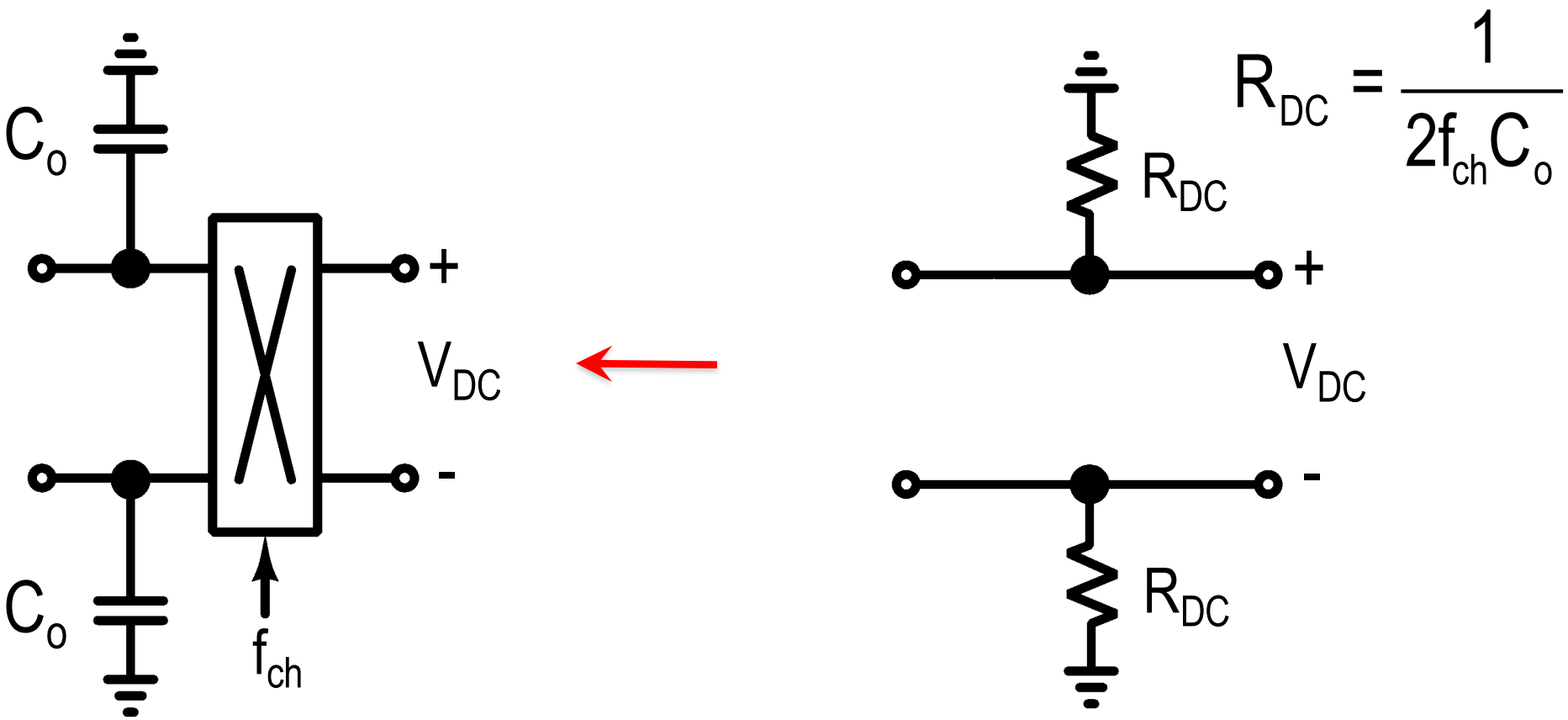
→Error proportional to C_i/RG_{ota}


C
R/2
V_d
$-V_d$
R/2
G_{ota}
f_{ch}
f_{ch}
Signal band
0
PSD (dB)
-60
-120
Aliasing
0
f_{ch}
$2f_{ch}$
$3f_{ch}$
$4f_{ch}$
$f_s/2$



Output parasitic switched at **every edge** of f_{ch}

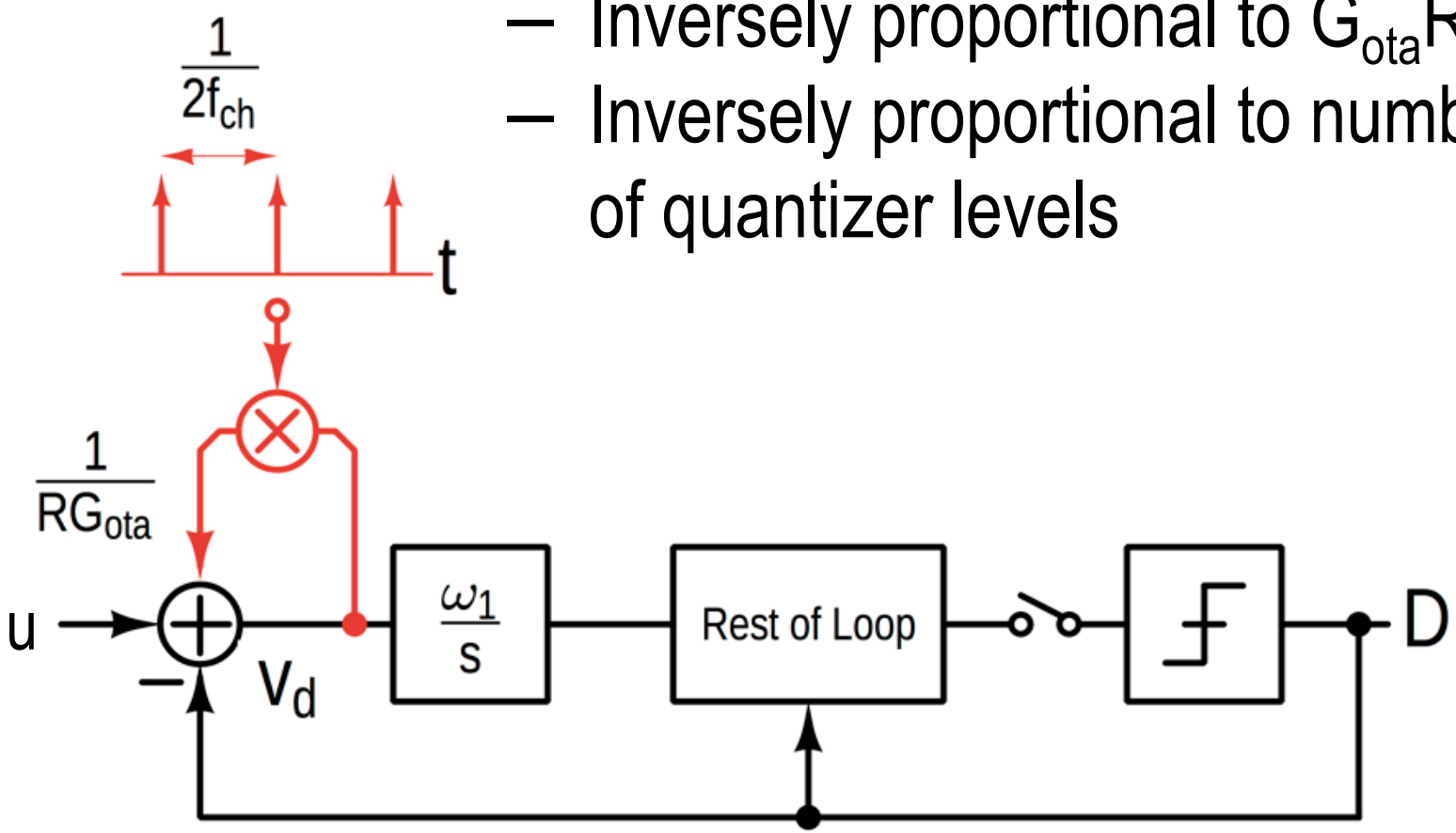
Chopped C_o : Equivalent Resistor



Reduced Integrator DC Gain

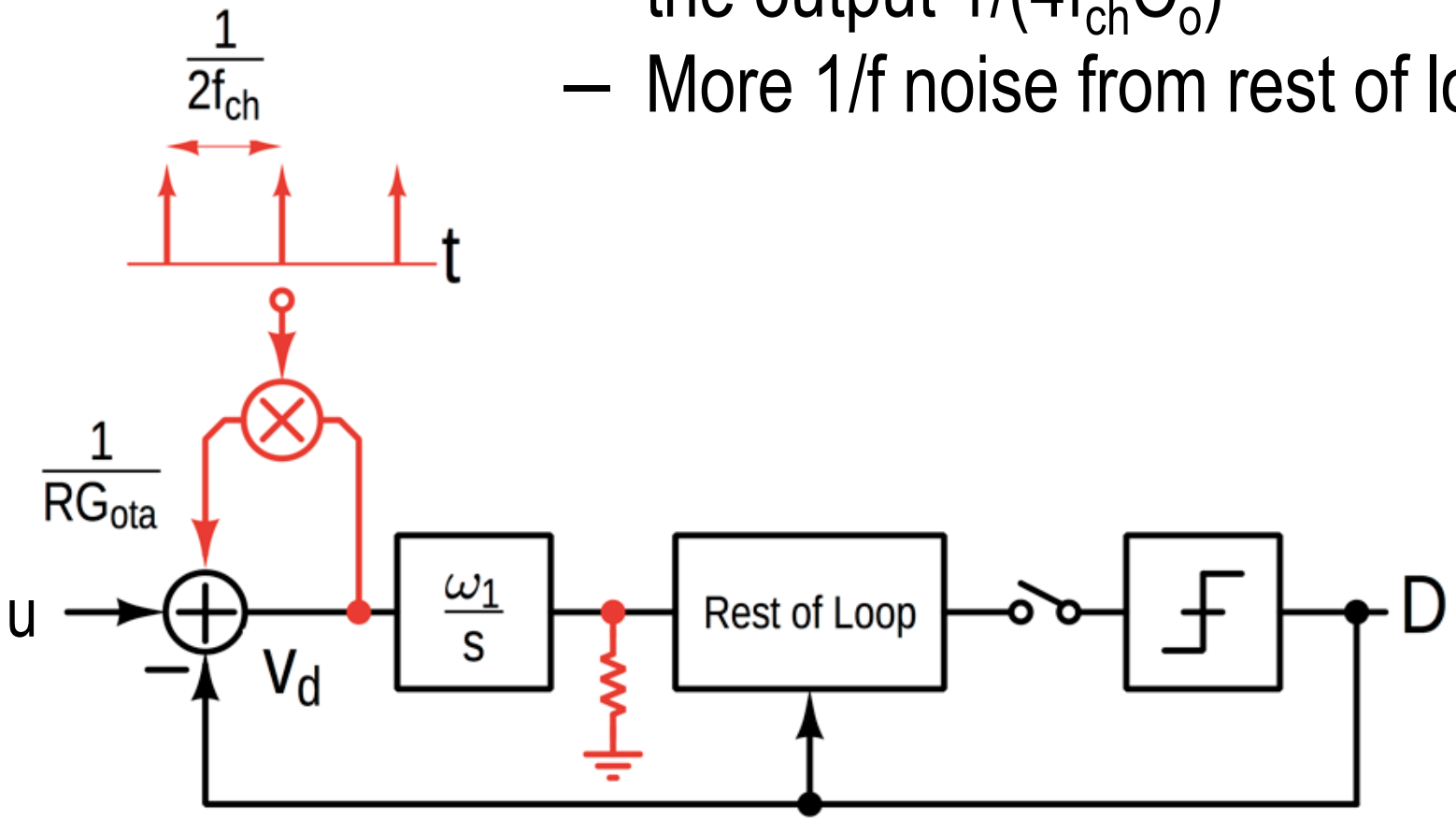
Chopping in CTDSMs : Summary

- Aliases shaped noise from multiples of $2f_{ch}$
  - Inversely proportional to $G_{ota}R$
  - Inversely proportional to number of quantizer levels



Chopping in CTDSMs : Summary

- Reduced integrator gain
  - Switched capacitor resistor at the output $1/(4f_{ch}C_o)$
  - More 1/f noise from rest of loop



Chopping in CTDSMs : Summary

Solutions

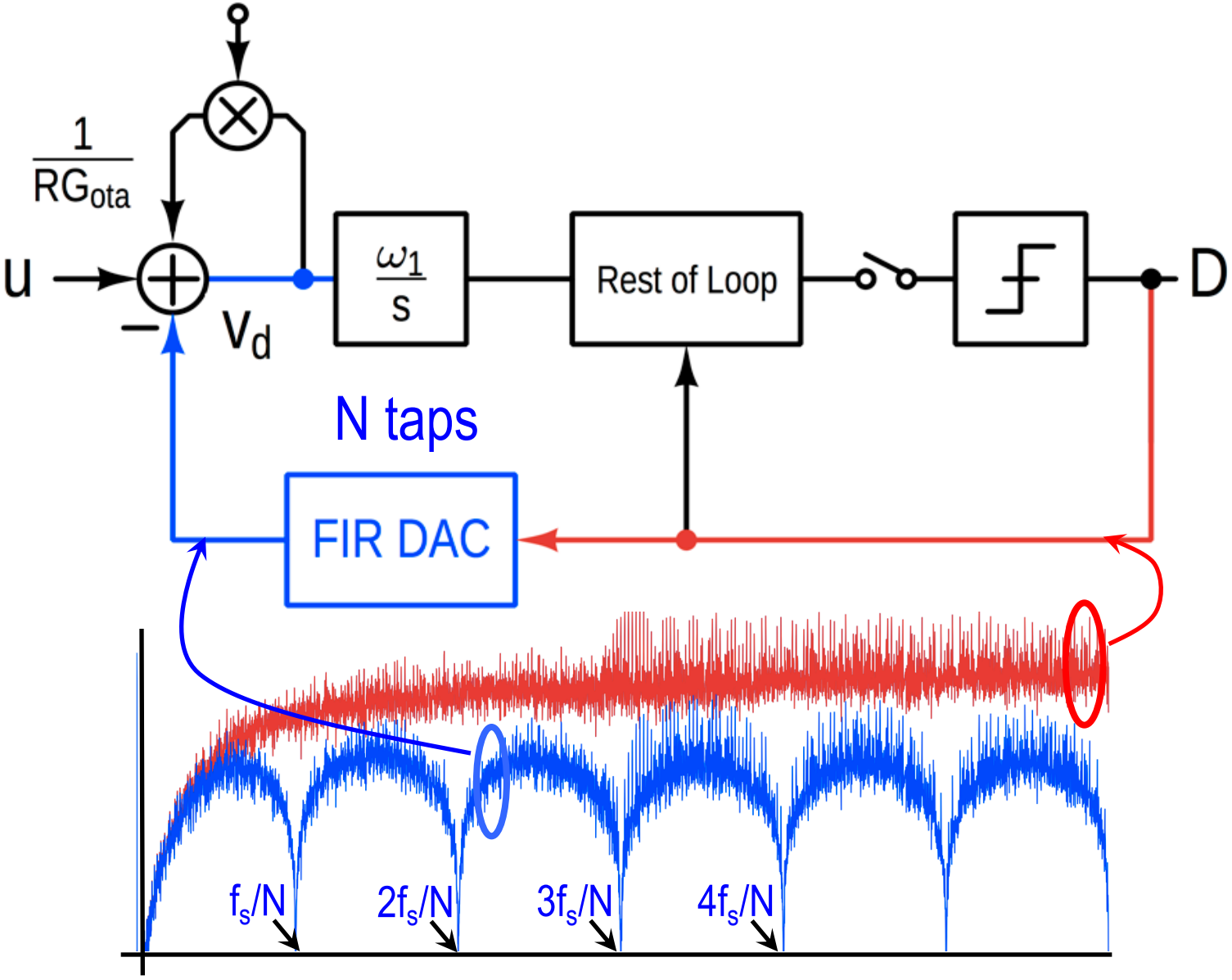
Increase $G_{ota}R$

✗ 20dB reduction of alias noise dissipates 10x power

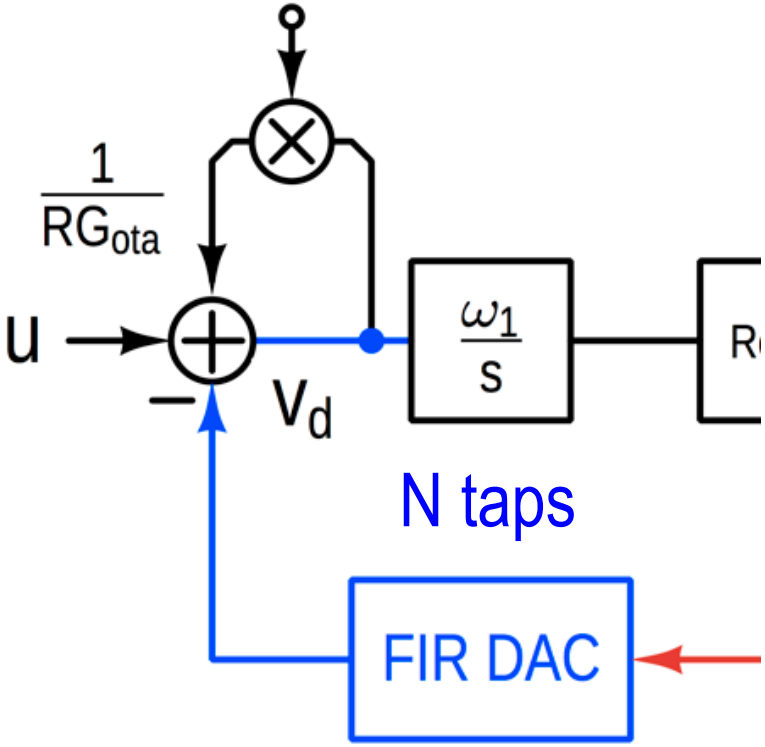
Increase number of quantizer levels

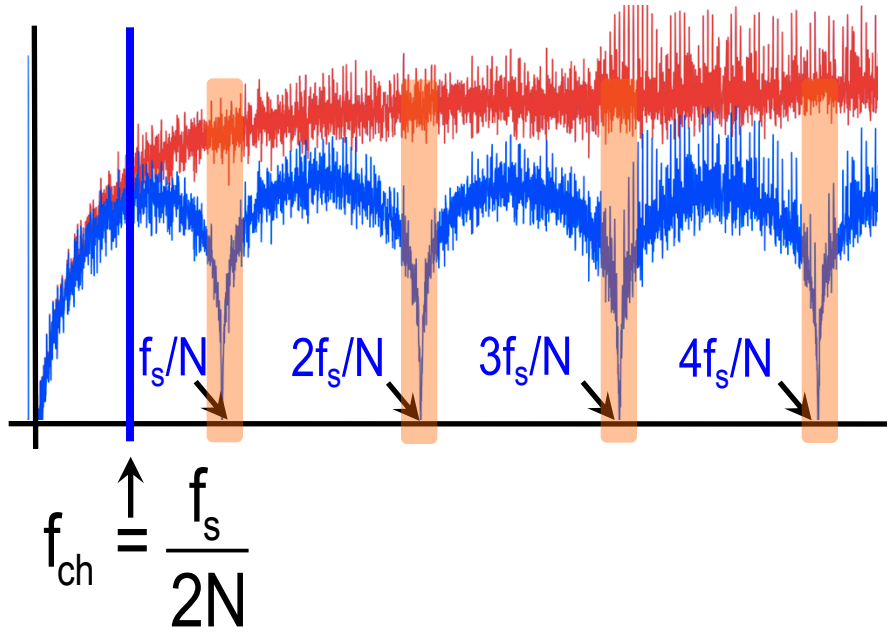
✗ 20dB reduction of alias noise needs 10x the number of levels

FIR Feedback DAC



FIR Feedback and Chopping



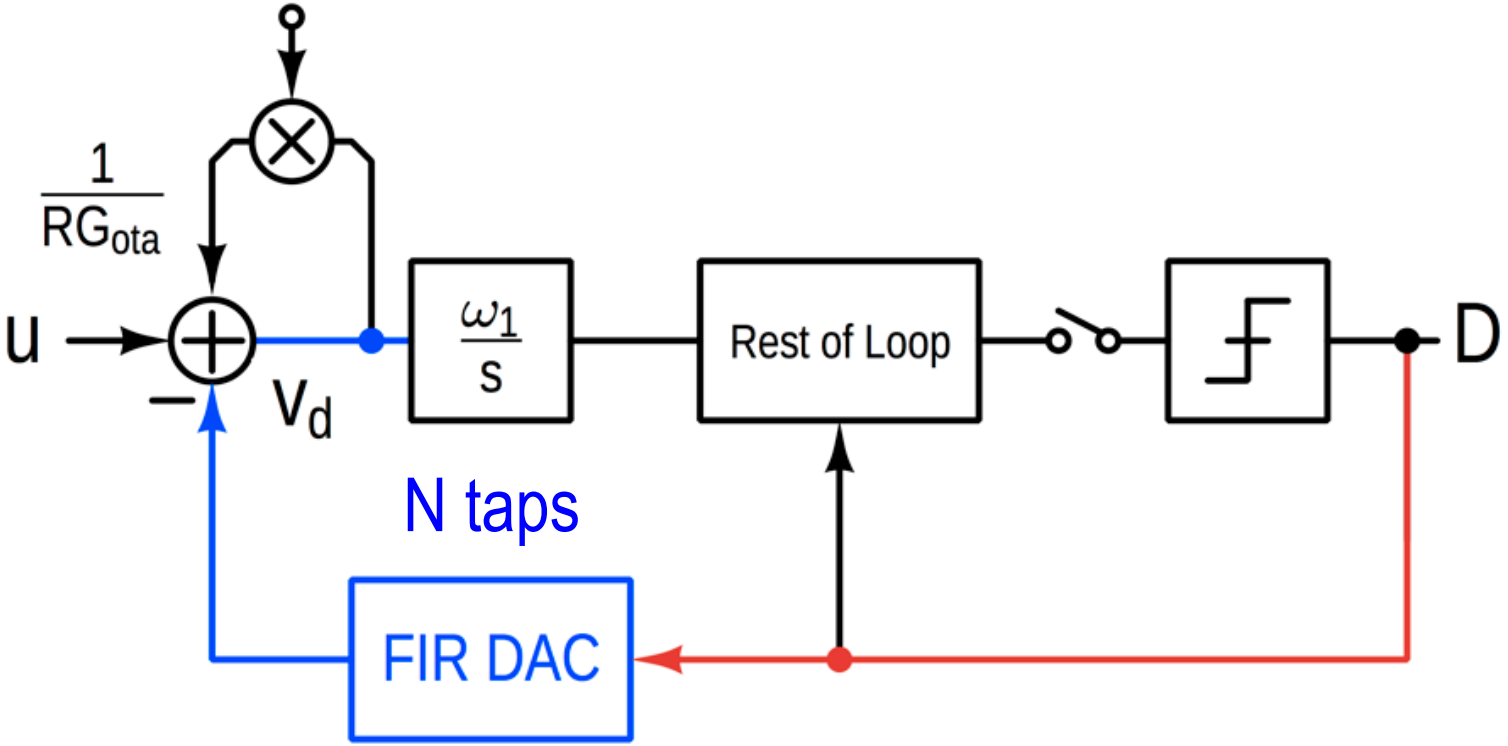


Chopping frequency chosen as $f_s/2N$

→ Nulls at multiples of $2f_{ch}$

→ Reduced aliasing of shaped noise

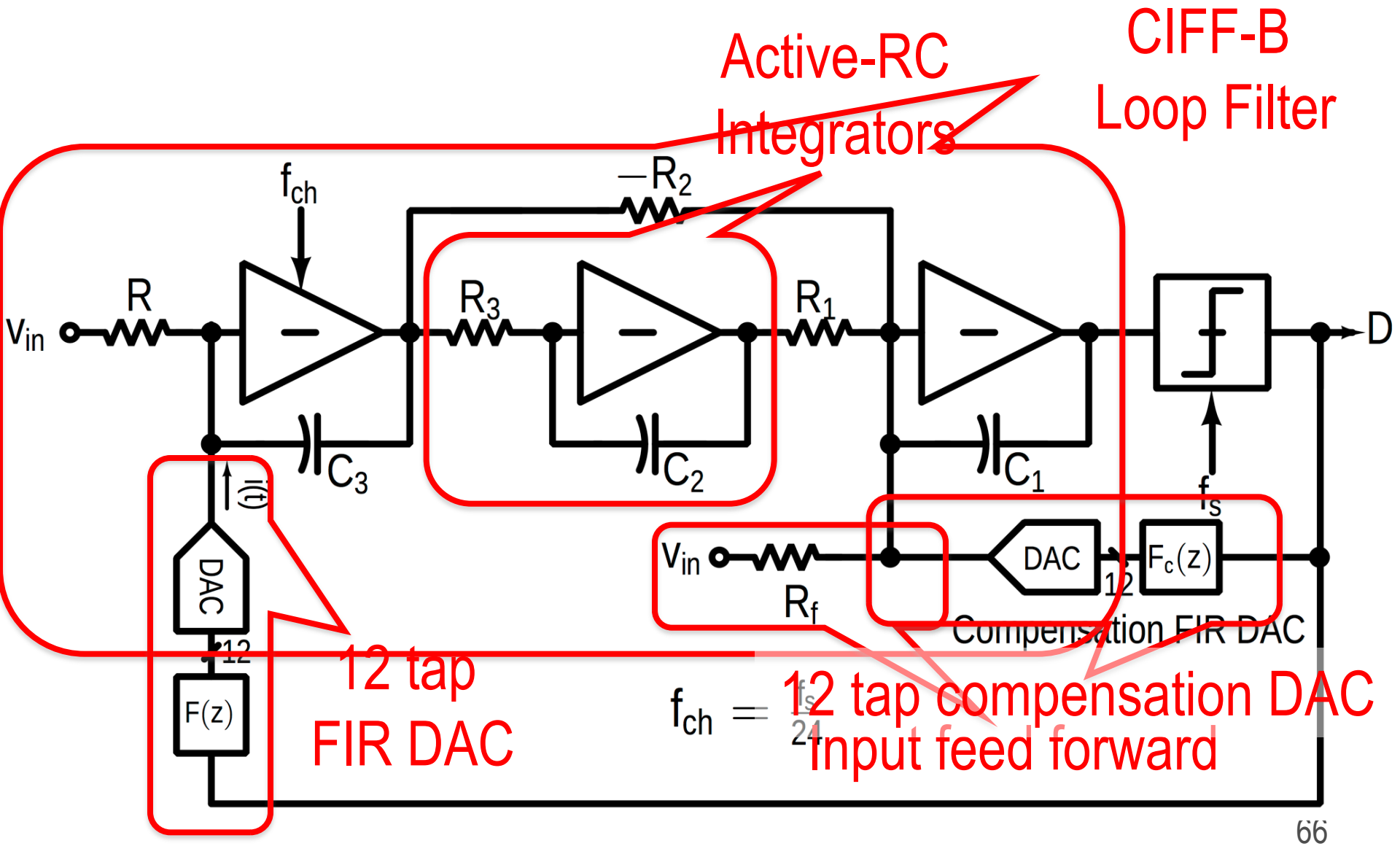
1-bit quantizer & FIR Feedback : Summary



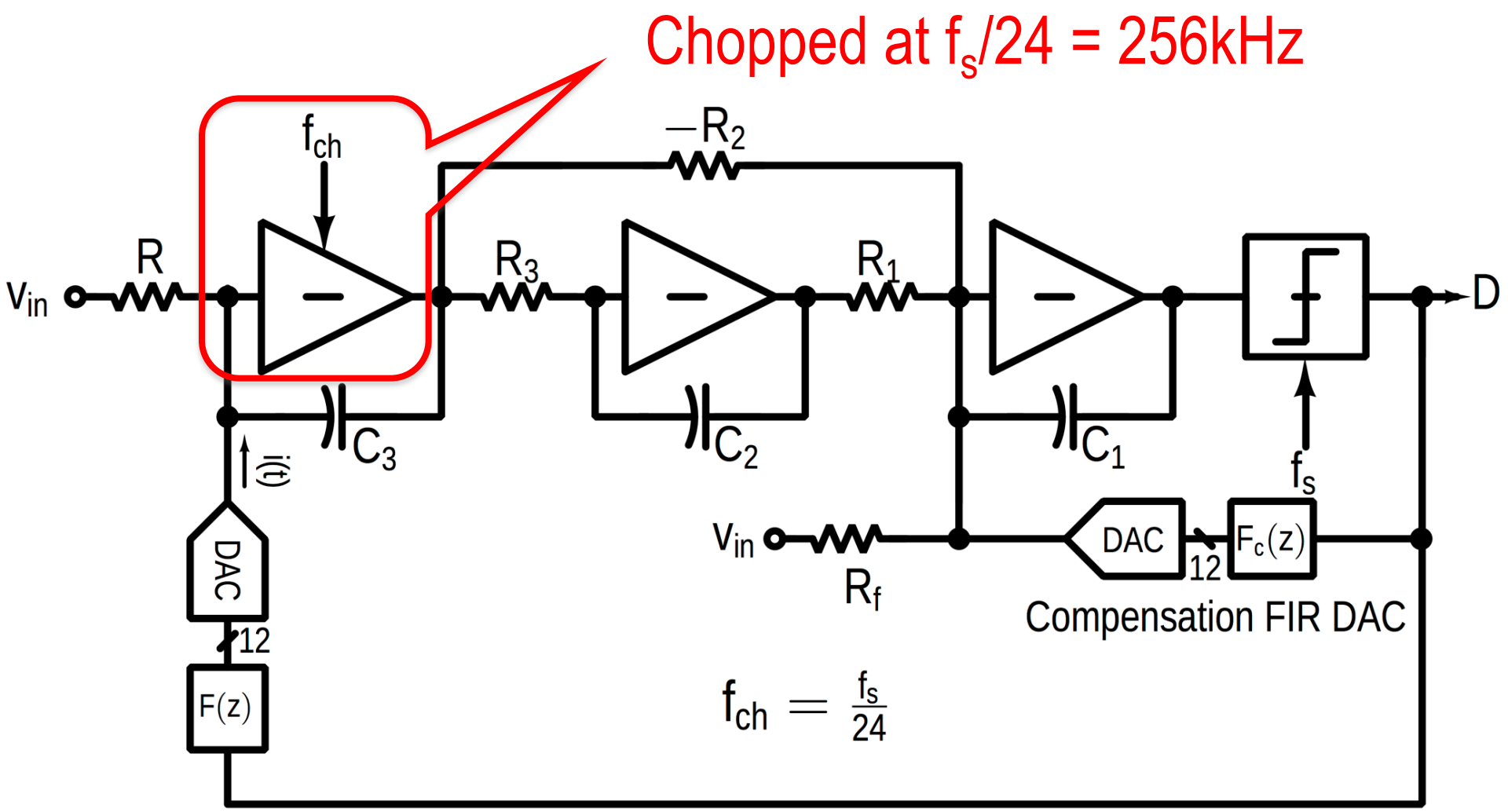
- ✓ Reduced jitter sensitivity
- ✓ Improved integrator linearity
- ✓ Reduced chopping artifacts
- ✓ Inherently linear DAC

Architecture and Circuit Design

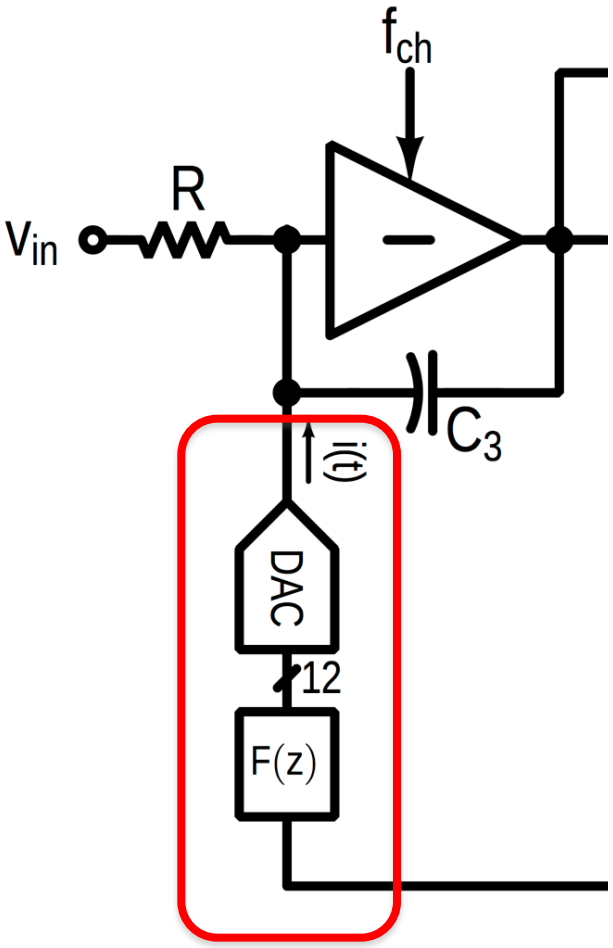
3rd Order CTDSM Architecture



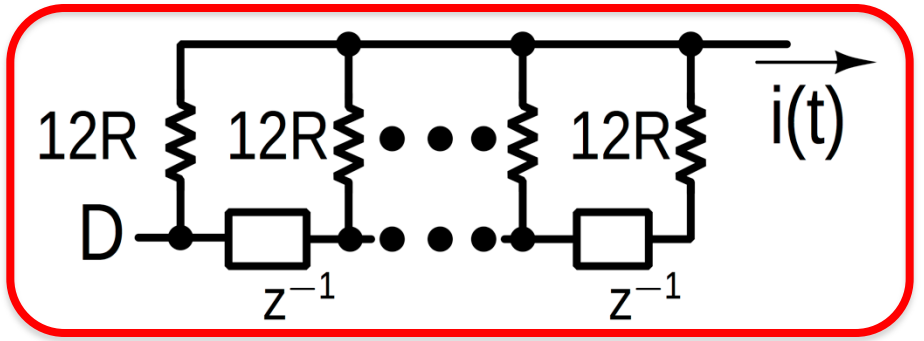
3rd Order CTDSM Architecture

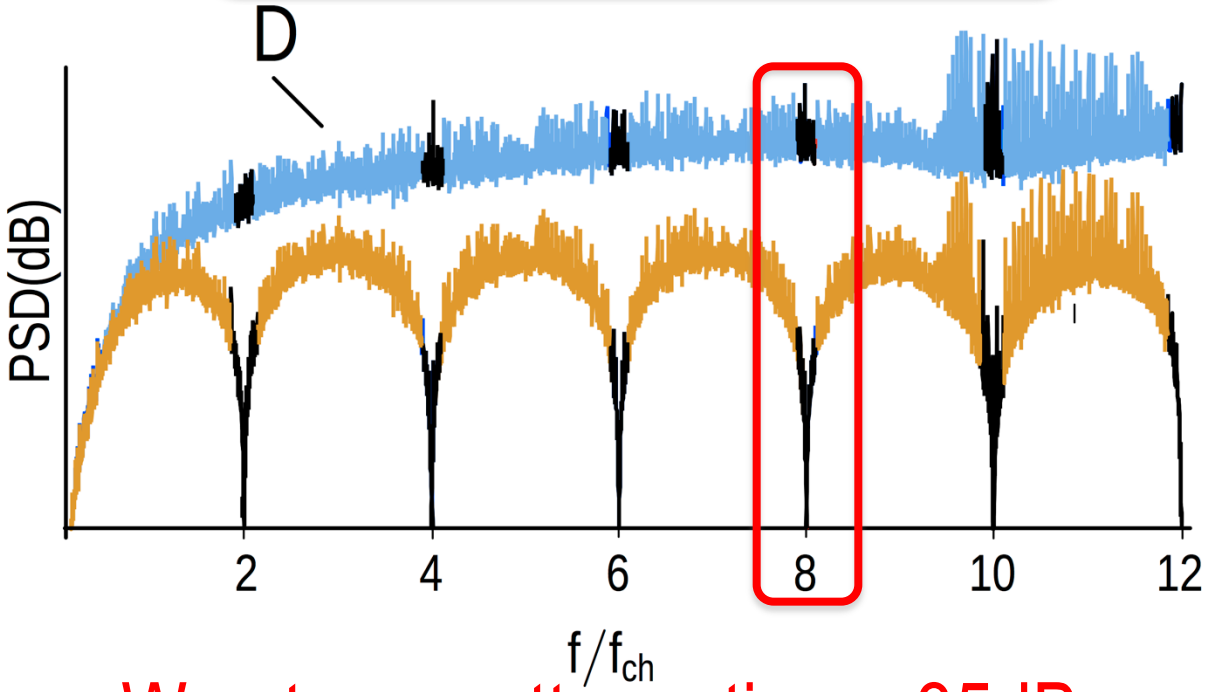


3rd Order CTDSM Architecture



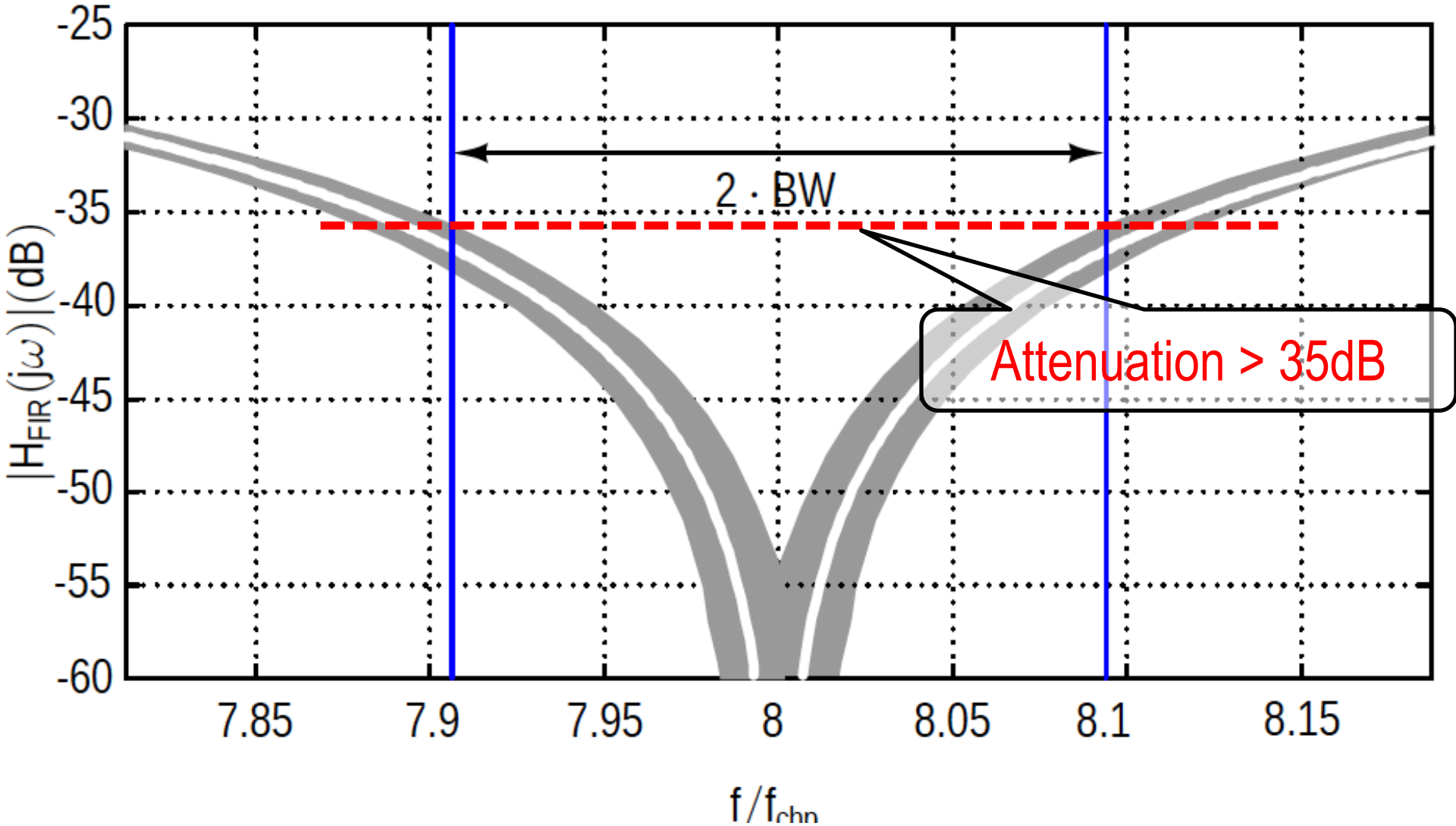
Semidigital Implementation





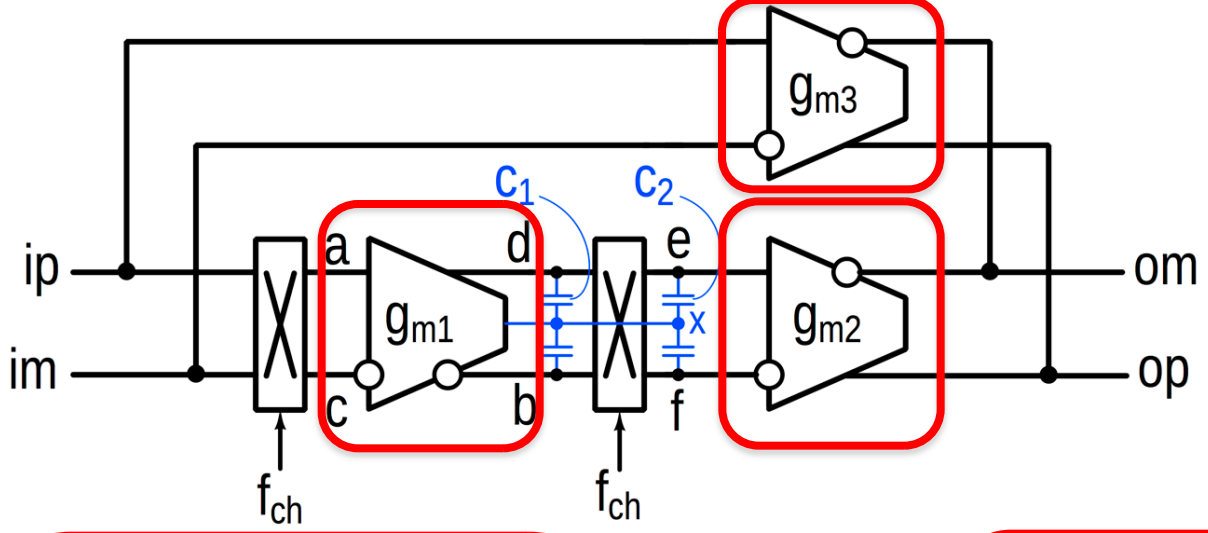
Worst case attenuation > 35dB

Monte Carlo : 1% random tap mismatch

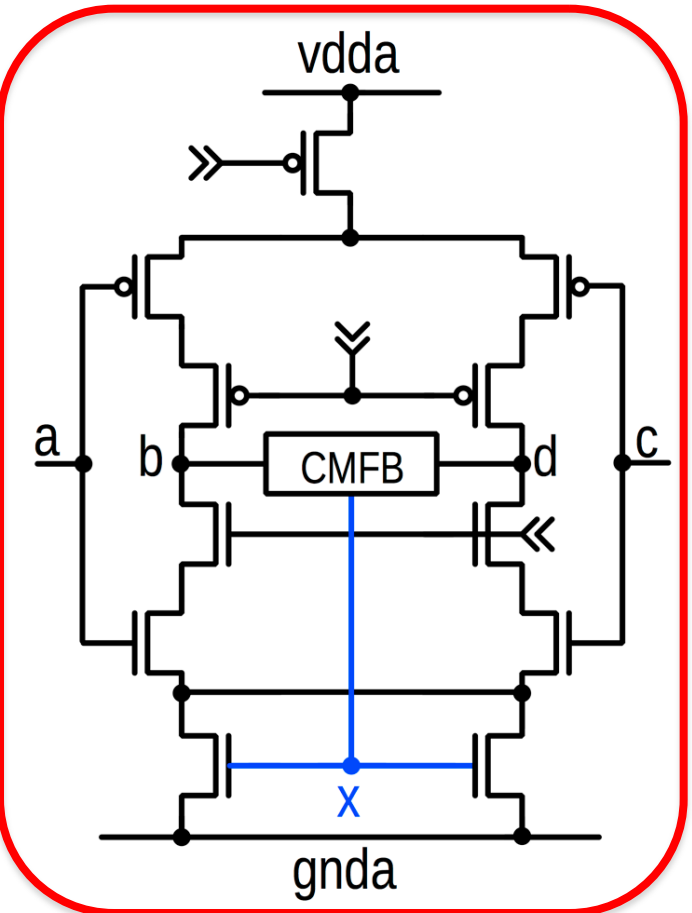


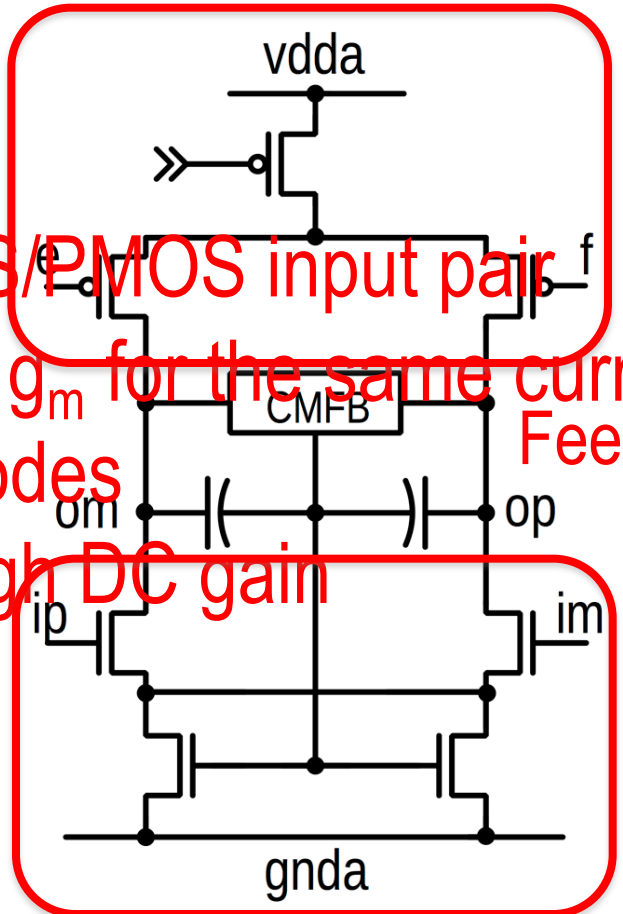
OTA Design

2 Stage Feedforward Compensated OTA



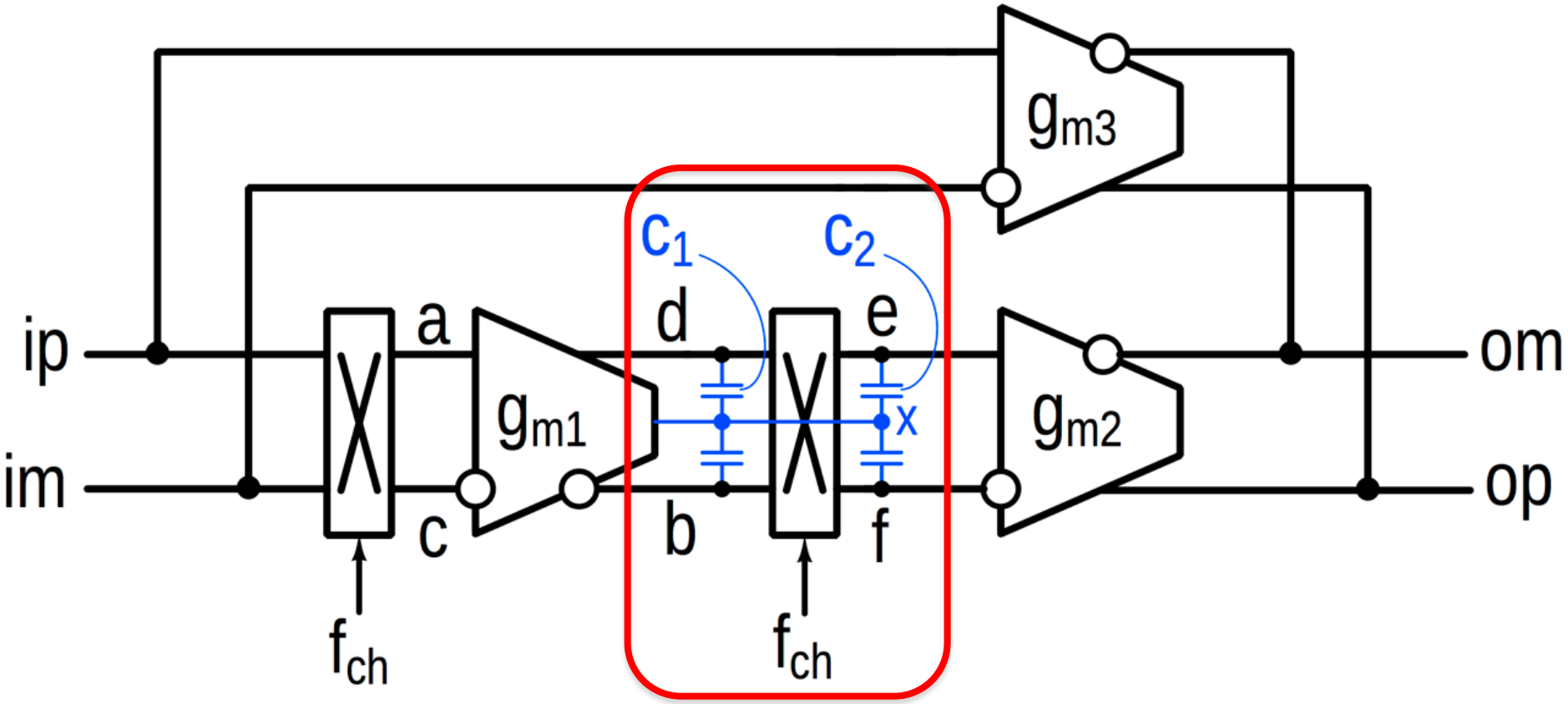
2nd Stage





NMOS/PMOS input pair
→ 2x g_m for the same current

Feedforward Cascodes
→ High DC gain



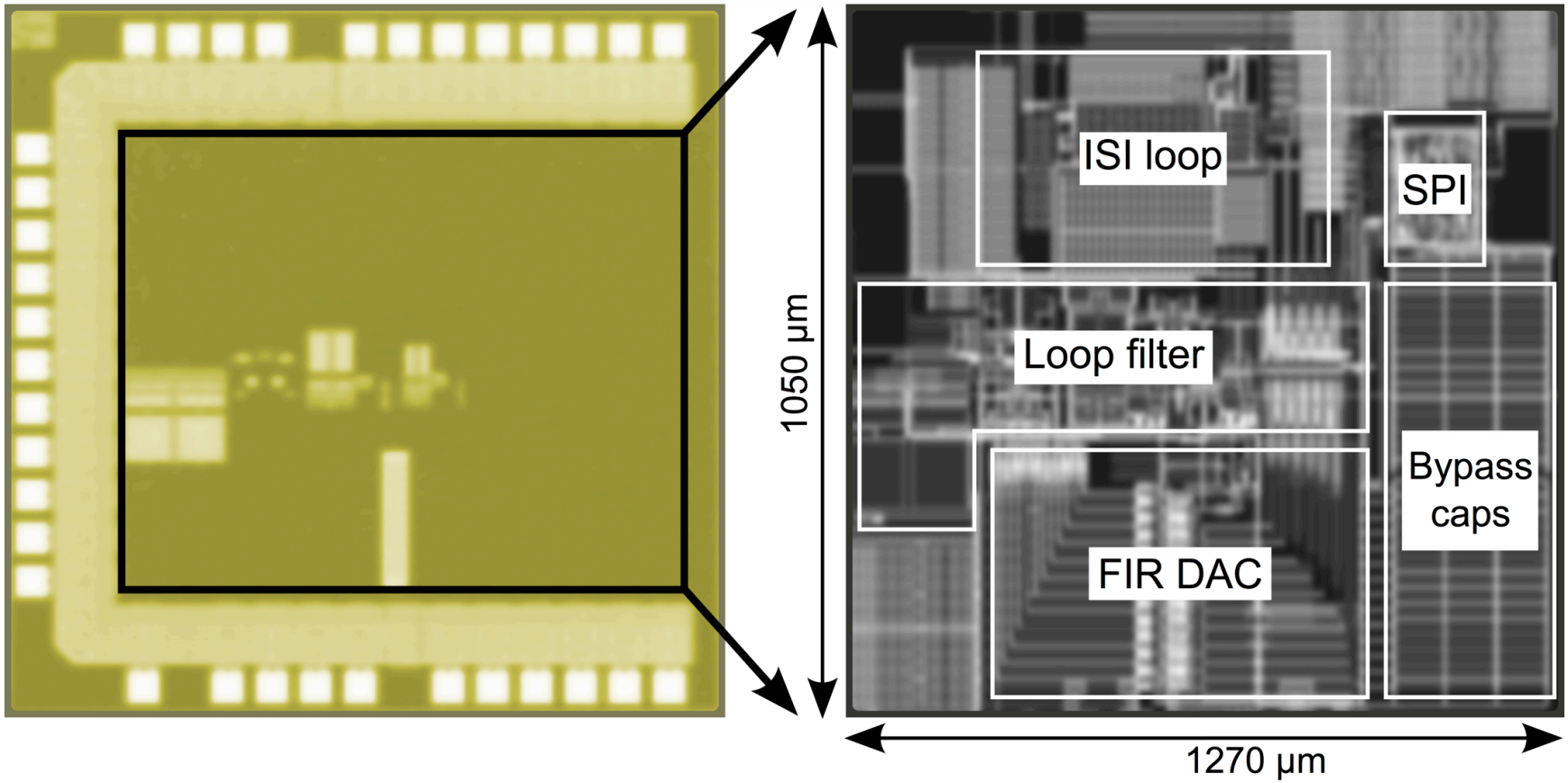
CMFB compensation capacitors

Small fraction (c_1) inside chopper

→ Compensation during chop transitions

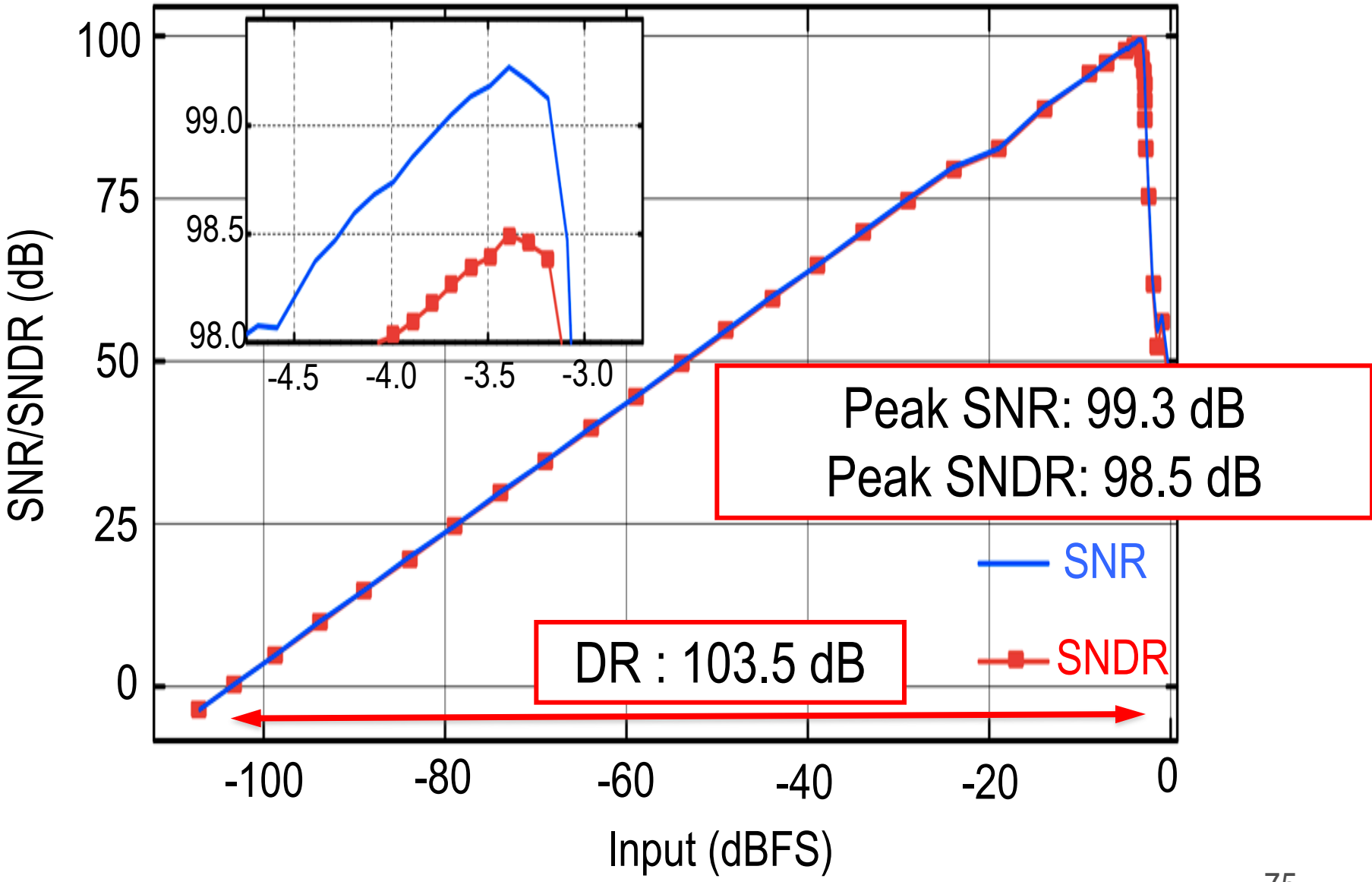
Measurement Results

Die Photo & Layout Snapshot

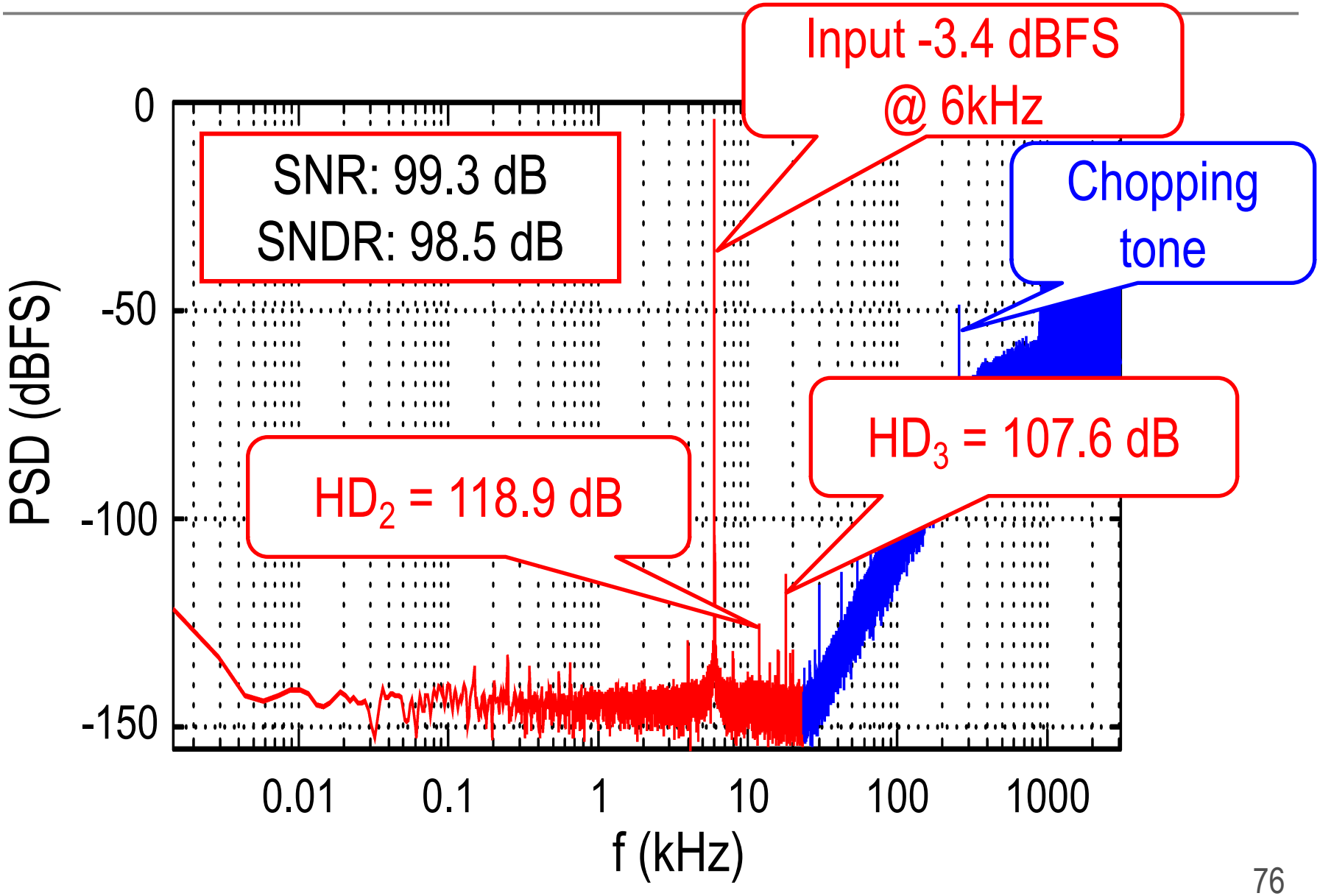


UMC 180nm CMOS process
(Europractice)

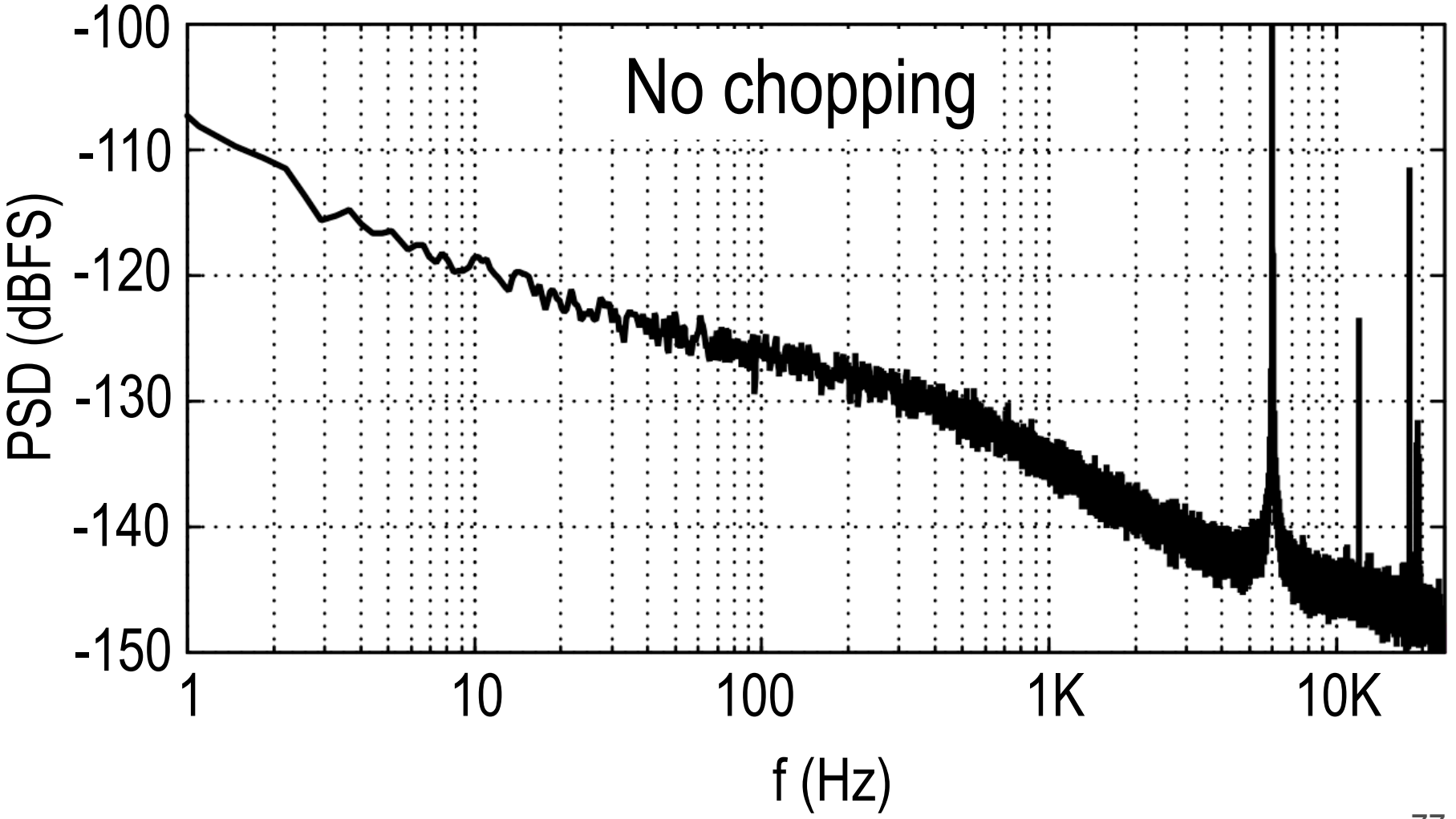
Dynamic Range Plot



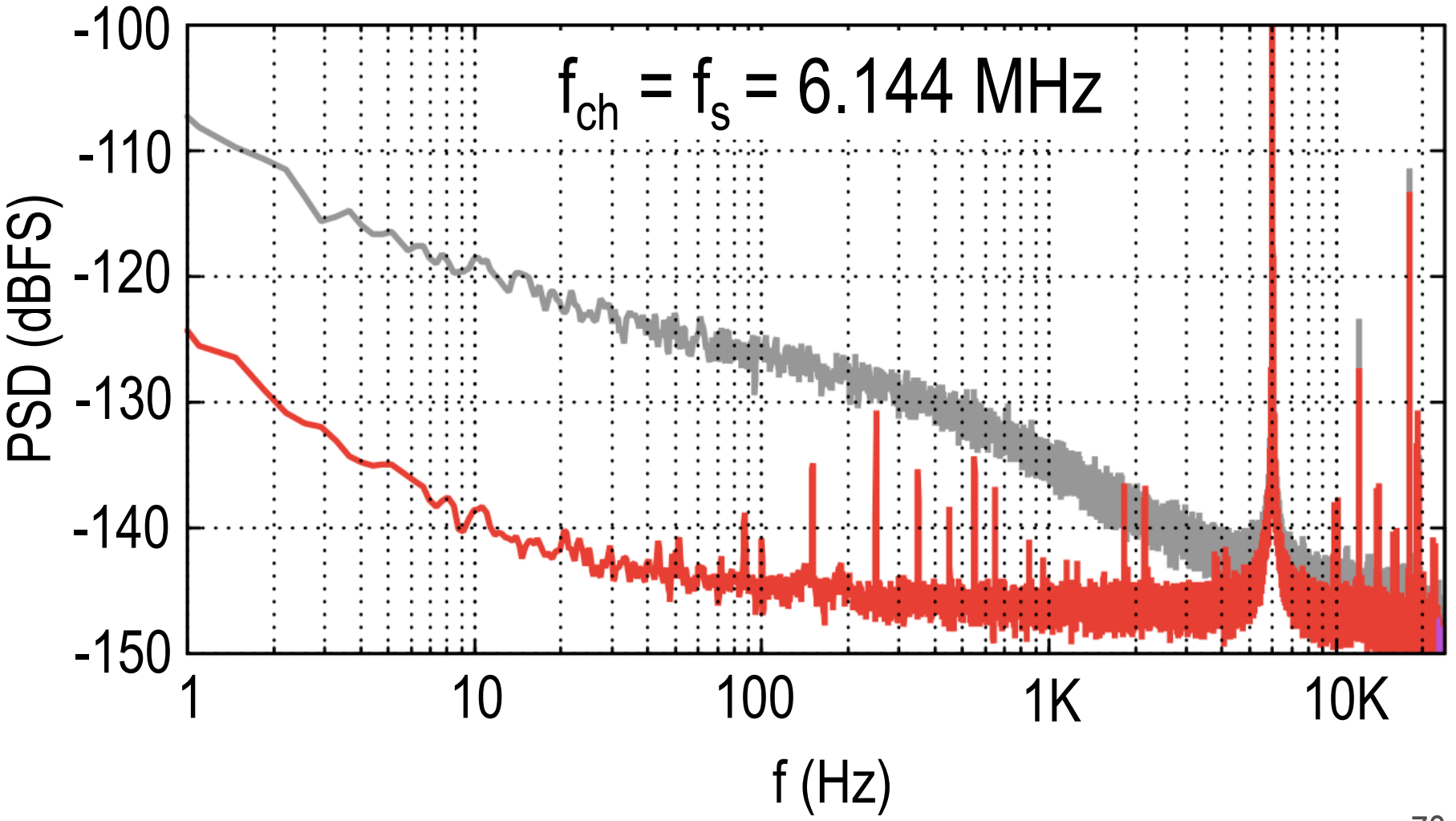
PSD at Peak SNDR



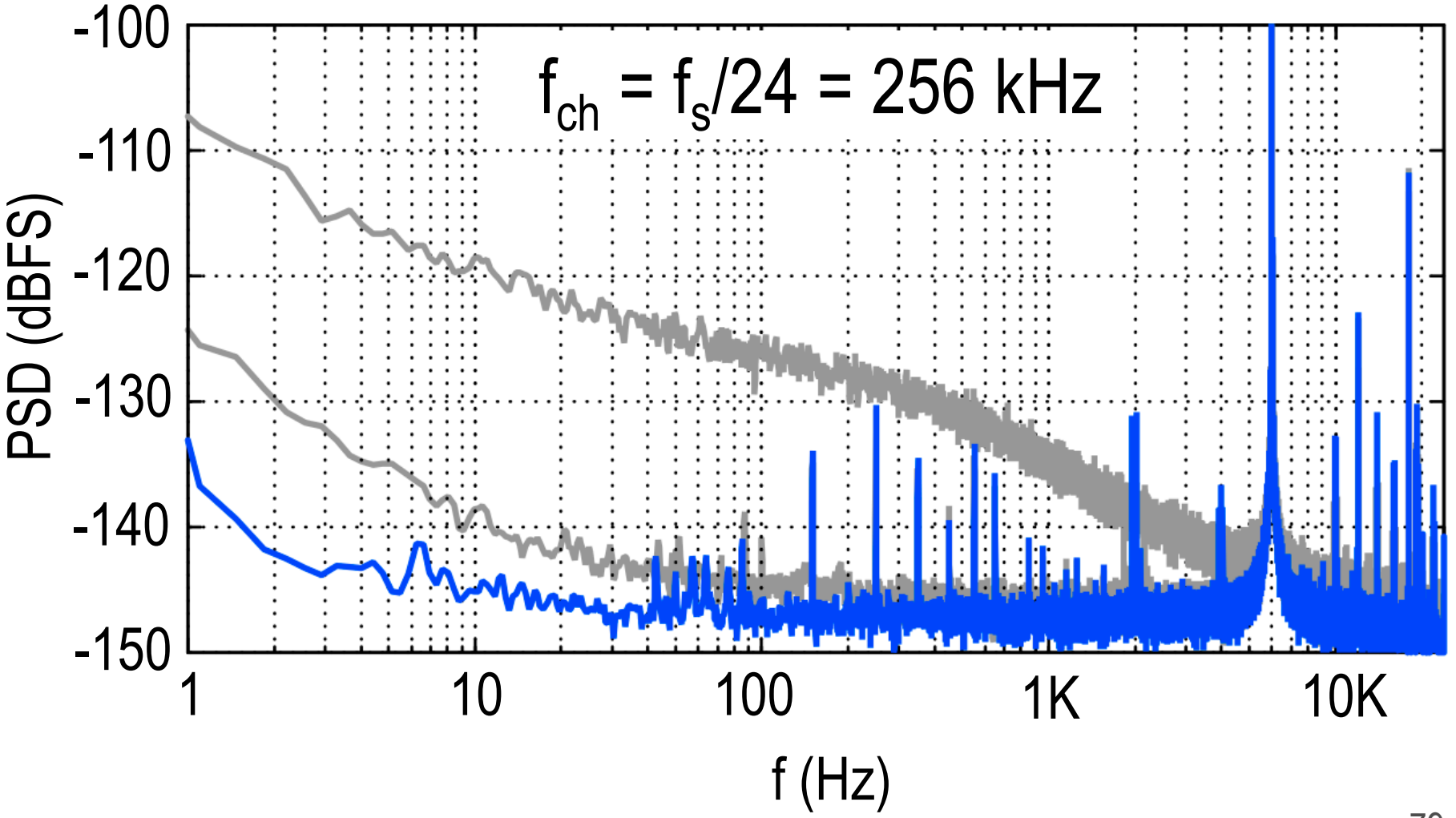
Low Frequency PSD



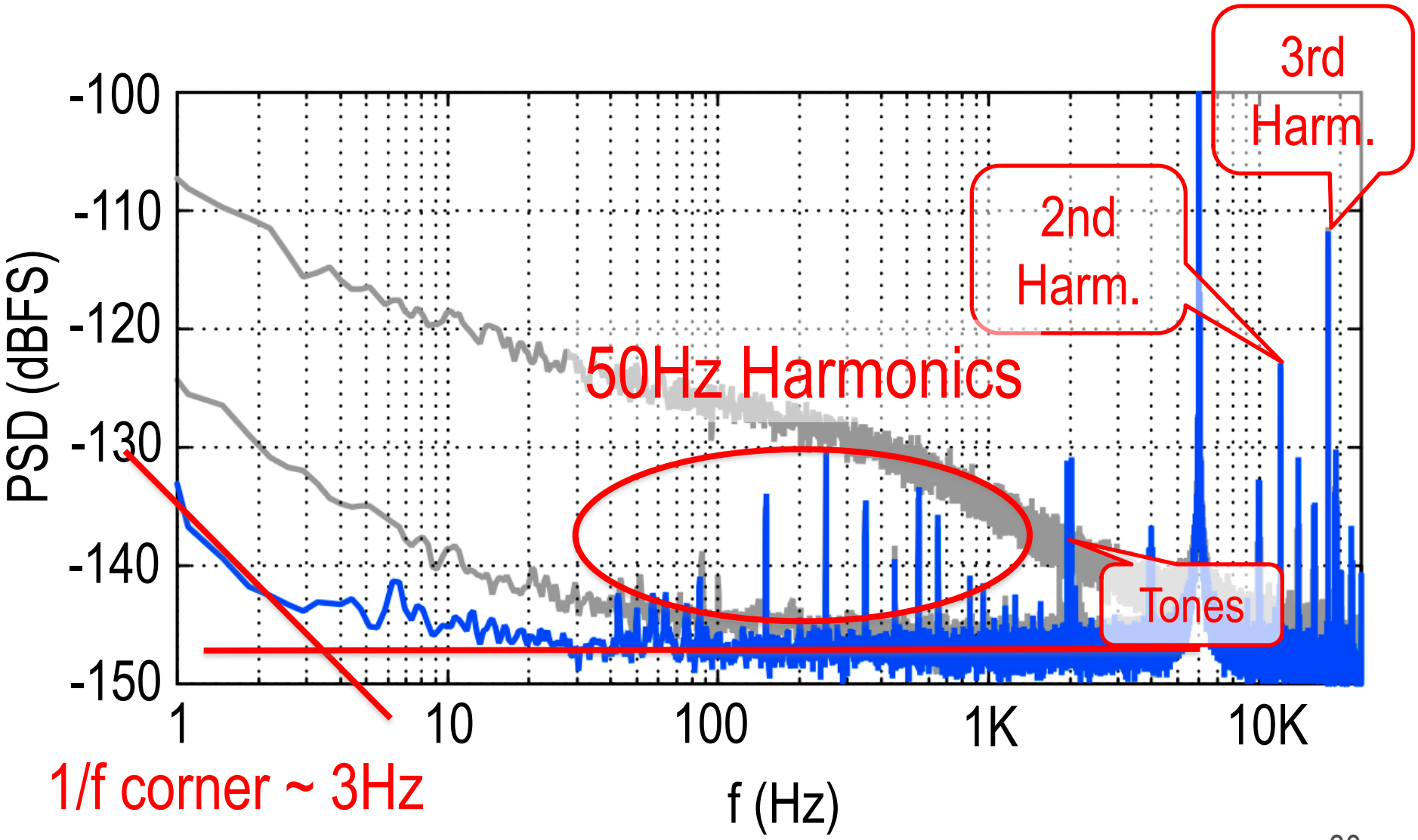
Low Frequency PSD



Low Frequency PSD

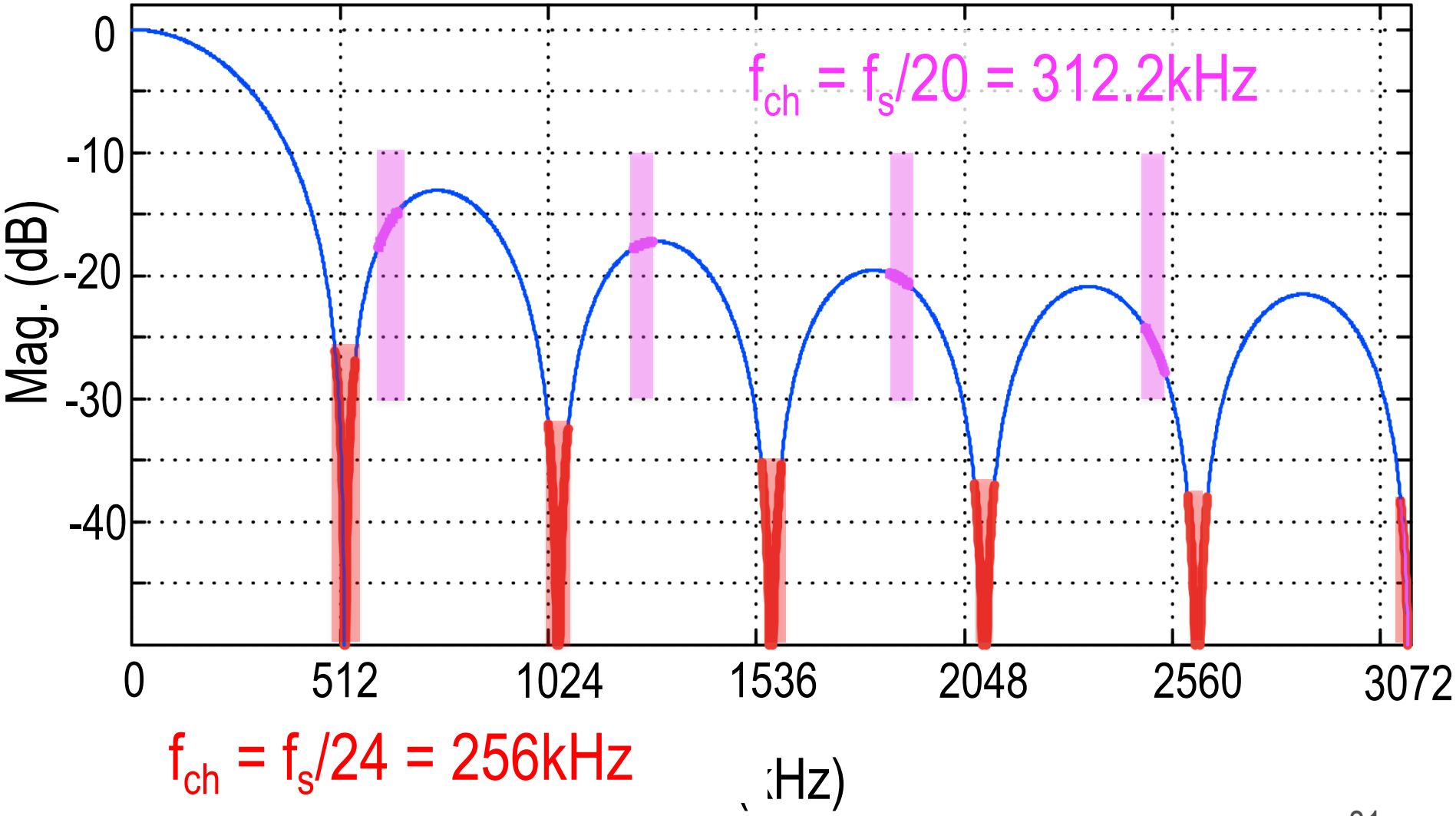


Low Frequency PSD

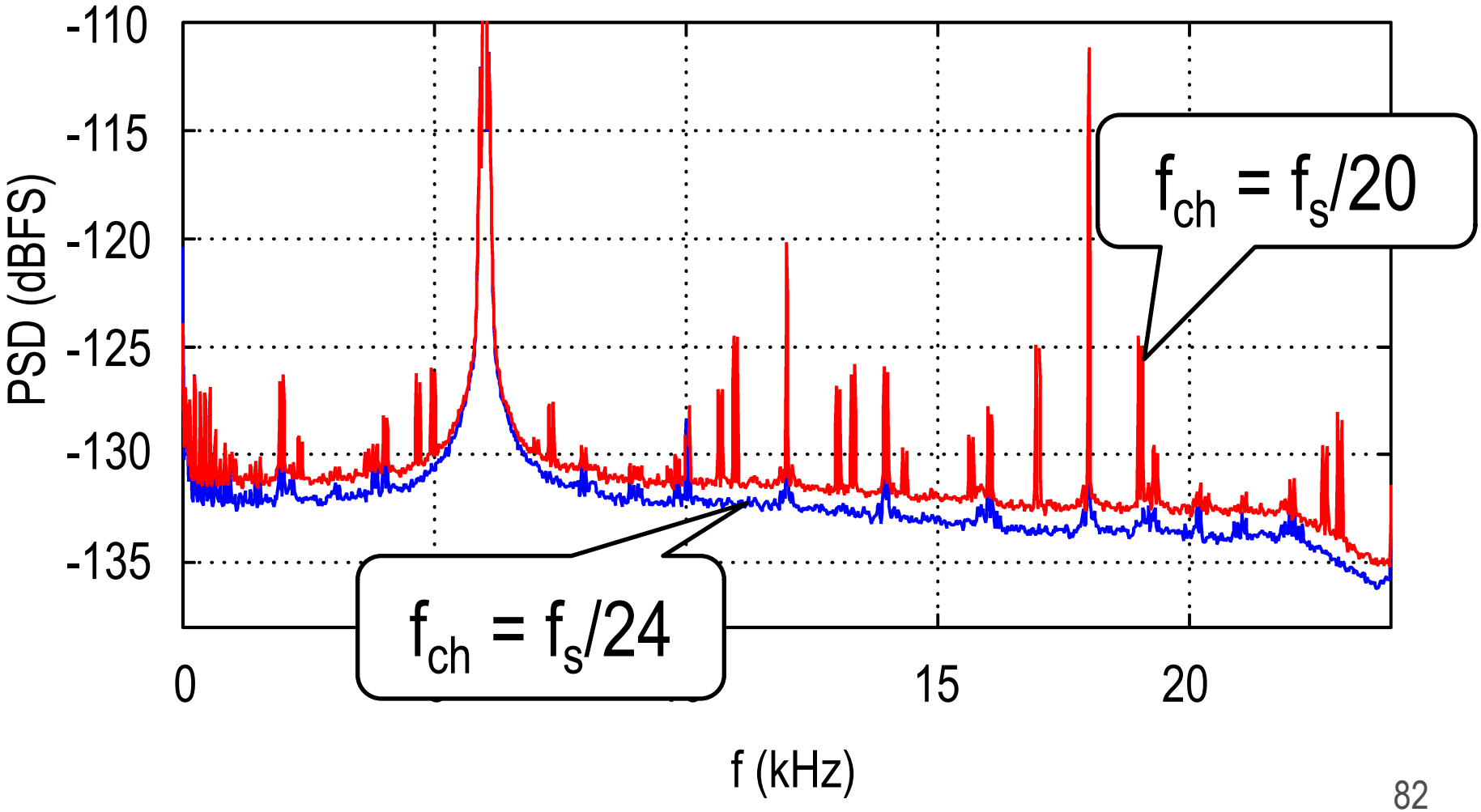


Effect of changing f_{ch}

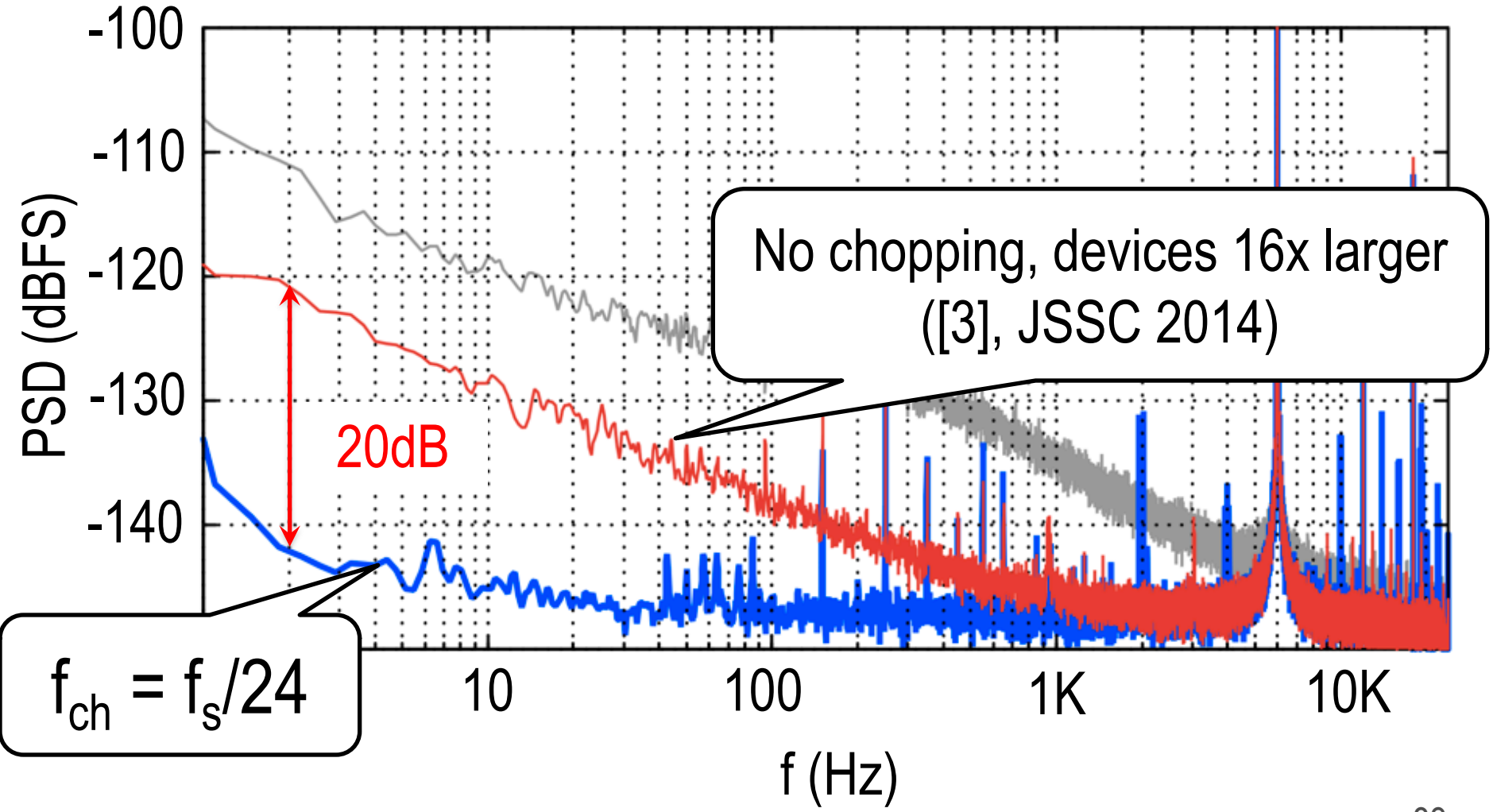
Increased Aliasing



PSD Comparison : $f_c = f_s/24$ & $f_s/20$



PSD Comparison



Performance Summary and Comparison

	This work	[3] JSSC 2014	[4] ISSCC 2008	[5] VLSI 2015	[6] ASSCC 2014
BW (kHz)	**24**	24	20	24	24
Feature Size (nm)	**180**	180	45	65	28
Supply (V)	**1.8**	1.8	1.1	1.1	1.1
Power (μW)	**280**	280	1200	121	9900
Peak SNDR (dB)	**98.5**	98.2	76.5	85	98.5
DR (dB)	**103.6**	103	91.7	88	100.6
SFDR (dB)	**107.6**	106	80.5	90	102.6
Chop Freq. (kHz)	**256**	-	46	-	-
FoM_{SNDR} (fJ/lvl)	**85**	88	500	173.4	342
$FoM_{Schreier}$ (dB)	**177.8**	177.5	148.5	168	172

A Tale of 4 ADCs

- Multi-bit (4-bit ADC in the loop)
  - ESSCIRC 2007, JSSC 2008
- Single-bit ADC with linearity enhancement
  - ESSCIRC 2009, JSSC 2010
- Single-bit ADC + 12-tap FIR DAC
  - ASSCC 2013, JSSC 2014
- Single-bit ADC + 12-tap FIR DAC + Chopping
  - ISSCC 2016, JSSC 2017
- Same process, same design group

Multi-bit Modulator

- Third order CIFF loop
- 4-bit flash ADC
- OSR = 64 (Clock Rate = 3.072 MHz)
- NRZ Resistive DAC
- Data Weighted Averaging

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 43, NO. 2, FEBRUARY 2008

A Power Optimized Continuous-Time $\Delta\Sigma$ ADC for Audio Applications

Shanthi Pavan, Nagendra Krishnapura, Ramalingam Pandarinathan, and Prabu Sankar

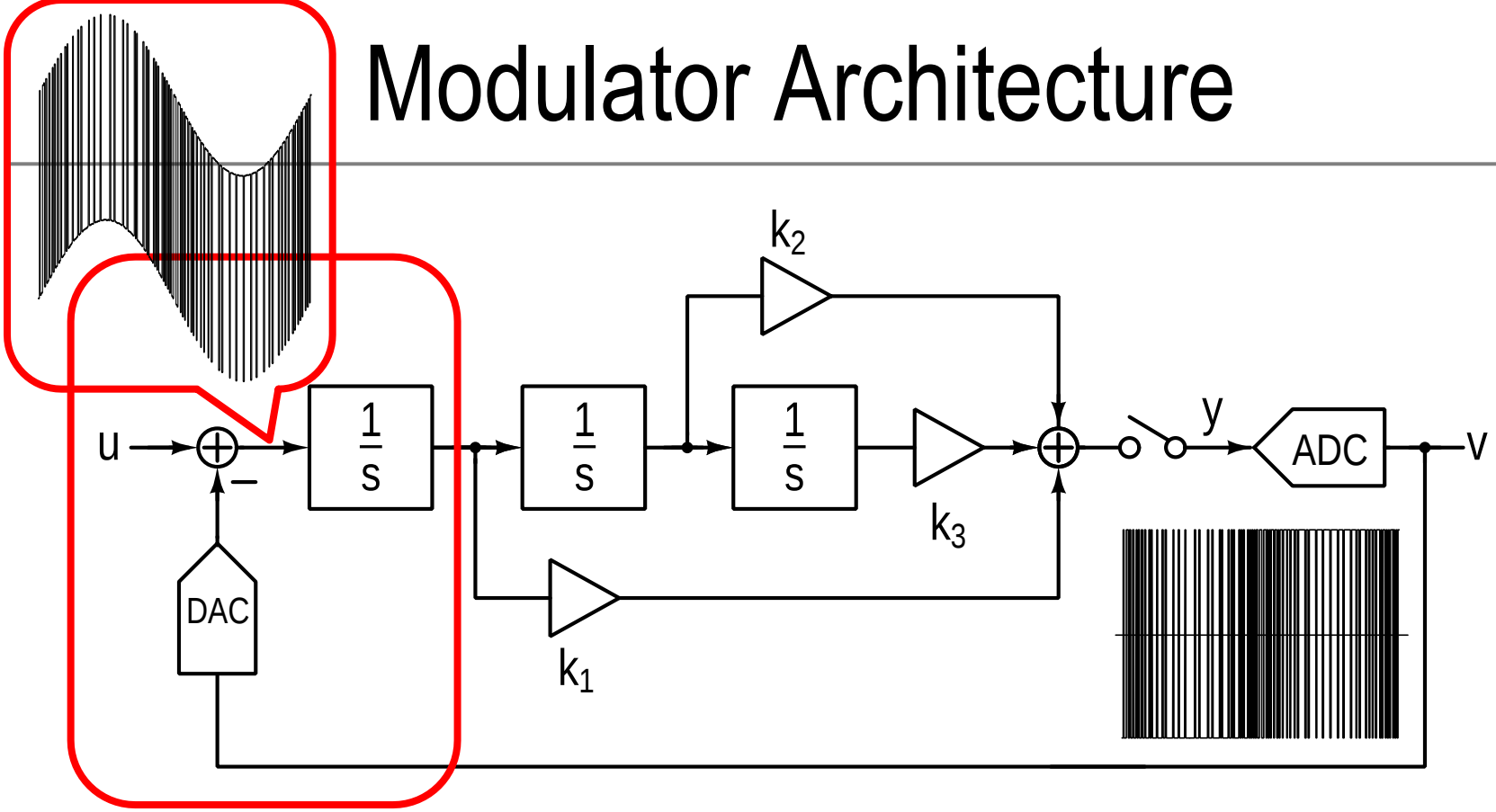
Single-bit Modulator

- Third order CIFF loop
- 1-bit ADC
- OSR = 128 (Clock Rate = 6.144 MHz)
- NRZ Resistive DAC

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 45, NO. 7, JULY 2010

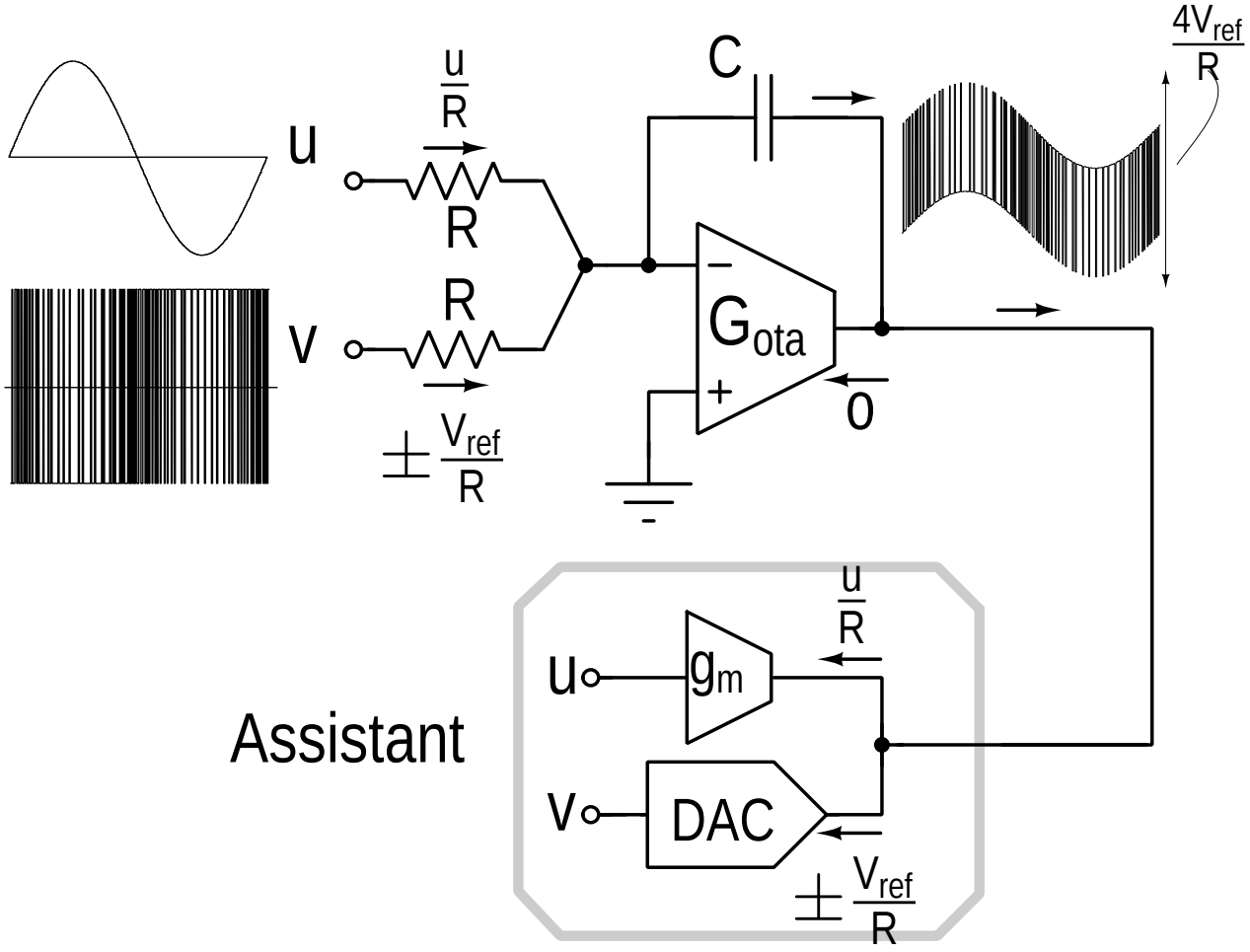
Power Reduction in Continuous-Time Delta-Sigma Modulators Using the Assisted Opamp Technique

Modulator Architecture



First integrator has to be very linear

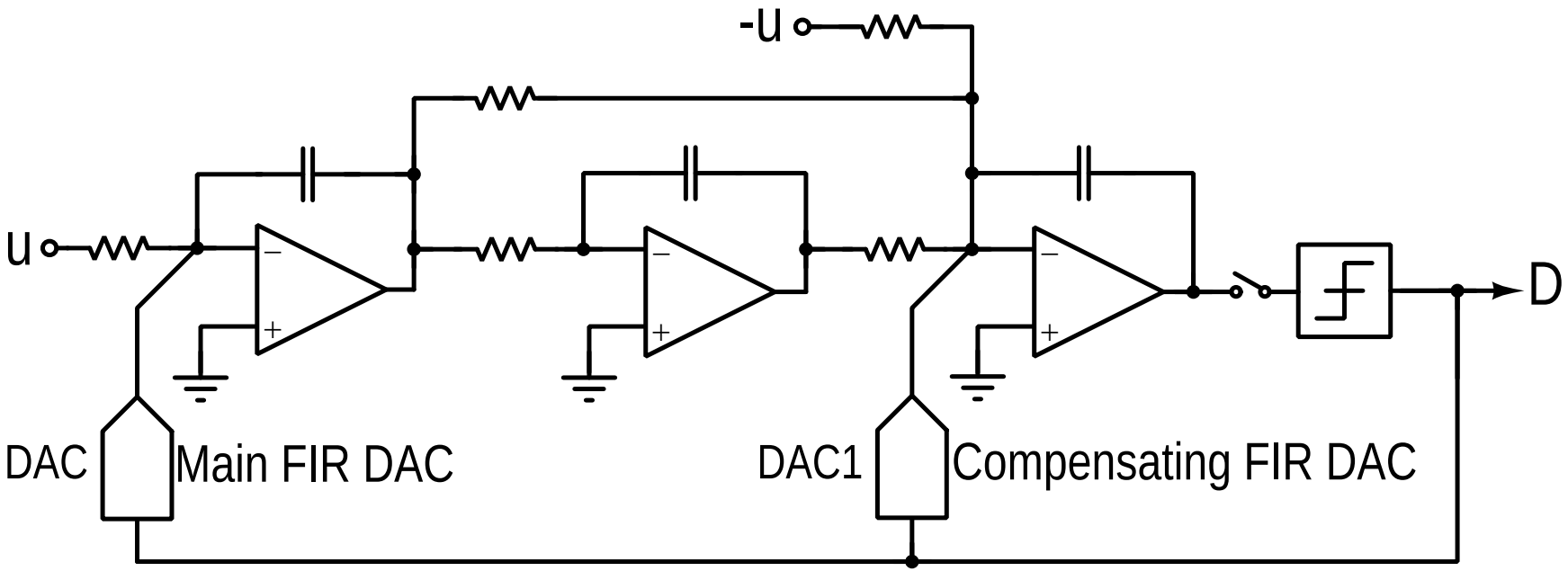
The Assisted-Opamp Integrator



1-bit + FIR DAC Based Modulator

- Third order CIFF-B loop
- 1-bit ADC + 12-tap FIR DAC
- OSR = 128 (Clock Rate = 6.144 MHz)
- NRZ Resistive DAC

Modulator Architecture



IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 49, NO. 11, NOVEMBER 2014

Low Power Design Techniques for Single-Bit Audio Continuous-Time Delta Sigma ADCs Using FIR Feedback

Amrith Sukumaran and Shanthi Pavan, *Senior Member, IEEE*

1-bit + FIR DAC + Chopping

- Third order CIFF-B loop
- 1-bit ADC + 12-tap FIR DAC
- OSR = 128 (Clock Rate = 6.144 MHz)
- NRZ Resistive DAC
- First integrator chopped at $f_s/24$
- ISSCC 2016

Performance Summary and Comparison

	1-bit + FIR + chopping	1-bit ADC + FIR DAC	1-bit ADC	4-bit ADC
BW (kHz)	24	24	24	24
Feature Size (nm)	180	180	180	180
Supply (V)	1.8	1.8	1.8	1.8
Power (μW)	280	280	110	121
Peak SNDR (dB)	98.5	98.2	88	90.8
DR (dB)	103.6	103	91.7	88
SFDR (dB)	107.6	106	95	94
FoM_{SNDR} (fJ/lvl)	85	88	111	89
$FoM_{Schreier}$ (dB)	177.8	177.5	171.4	173.7

Conclusions

- FIR feedback
  - ✓Simple 1-bit ADC
  - ✓Reduced ADC power and area
  - ✓Simplified clock distribution
  - ✓Inherently linear DAC → No DEM
  - ✓Relaxes integrator linearity and jitter requirements
  - ✓Chopping for free
  - ✓Combines benefits of 1-bit and multi-bit operation
  - ✓Highest Schreier FoM reported