Dissecting Design Choices for Power Efficient Continuous-time $\Delta \Sigma$ Converters

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Outline

• Introduction
• Architectural design choices
• Circuit techniques for low power
• Design details
• Measured results
• Conclusions
CTΔΣM in 1 minute

\[
\overline{u(t)} = -\overline{v(t)}
\]
CTΔΣM in 1 minute

\[ i_c(t) = 0 \]

\[ u(t) = -v(t) = -v[n] \]

\[ \frac{u(t)}{R} \]

\[ \frac{v(t)}{R} \]

\[ \text{Hold} \]
$i_c(t) = 0$

$u(t) = -v(t) = -v[n]$

$\frac{u(t)}{R}$

$\frac{v(t)}{R}$

Digital Sequence
CTΔΣM in 1 minute

\[ u(t) \rightarrow R \rightarrow C \rightarrow \text{Comparator} \rightarrow \text{Hold} \rightarrow v[n] \rightarrow \text{Digital Filter} \]

Slow \( u(t) \rightarrow \overline{u(t)} \approx u(t) \)

Does the number of quantizer levels matter?
CTΔΣM in 1 minute

\[ u(t) \rightarrow R \rightarrow (C) \rightarrow \text{operator} \rightarrow R \rightarrow \text{HOLD} \rightarrow v[n] \]
CTΔΣM in 1 minute: Antialiasing

\[ i_c(t) = 0 \]

\[ \sin(2\pi t) \]

\[ i_1(t) = 0 \]

\[ v[n] = 0 \]

\[ i_2(t) = 0 \]
CTΔΣM : A System for all Seasons

Continuous-time
Time Invariant
Linear

Loop Filter

Time Variant

Discrete-time
Nonlinear

ADC

DAC

“Digital”

Decimator

Negative Feedback

Industrially and Practically Relevant
(Too) Many Design Choices

- ADC
- DAC
- Loop Filter
- Order
- Quantizer Levels
- Sampling rate
Curse of Too Many Choices

• Single bit quantizer + high OSR
  – Or multibit quantizer + low OSR?

• Flash ADC
  – Or SAR ADC?

• NRZ DAC
  – Or Switched capacitor DAC for low jitter?
Buridan’s Ass

Dies of starvation

Courtesy: Inspirehep.net
Dies of thirst!!
Motivation

• Aim: Audio DSM with > 100 dB DR
  – 0.18µm CMOS technology
  – As low power as possible

• Low distortion (~100 dB) audio ΔΣ converters
  – Typically realized with discrete-time, multi-bit loops
Single-bit versus Multibit Modulators
Quantizer : 1-bit versus 4-bit

4-bit quantizer needs half the OSR to achieve same in-band noise
(Baseline : 3\textsuperscript{rd} Order Single-bit DSM, OSR = 128)
ADC Resolution

- 4 bit ADC
  - 15x more comparators @ 1/2 speed
  - 7x more ADC power, 15x more area
  - 15x loop filter & clock path loading
Comparator Random Offset

- Increased in-band noise
- Reduced stable amplitude
SNDR with Random Offset

Third-order Modulator 16-level Quantizer
Loop Filter

- Loop filter should swing full-scale
- Difficult in high-speed designs
- Comparator offset is benign
- Driving the 1-bit quantizer
  - Loop filter’s last stage simpler to design
  - Particularly useful at high speeds
DAC: 1-bit versus 4-bit

A single bit quantizer consumes lesser power though it operates at 2x the speed

- Needs Dynamic Element Matching
- DEM adds excess delay & power
Single-bit CTDSM Issues: Clock Jitter

Jittery clock $\rightarrow$ equivalent to error at the input
Single-bit CTDSM Issues: Clock Jitter

Large jitter error $\Rightarrow$ rail-to-rail feedback waveform
Single-bit CTDSM Issues: Filter Linearity
Single-bit CTDSM Issues: Filter Linearity

Increased loop filter power dissipation needed to achieve linearity
Summary so far …

- Single bit operation
  - Very efficient quantizer
  - Easy to drive
  - Sensitive to clock jitter
  - Loop filter needs to handle large swings
    - Increased power dissipation
Improved Single-bit CTDSM: FIR Feedback

FIR filter in the feedback path
Improved 1-bit CTDSM : FIR Feedback

Height of steps $\rightarrow$ Greatly reduced
$\rightarrow$ Reduced jitter sensitivity
Improved 1-bit CTDSM : FIR Feedback

**Graph Description:**
- **PSD (dB)** is plotted on the vertical axis.
- **f (kHz)** is plotted on the horizontal axis.
- The graph compares the performance of different configurations:
  - **1-bit ADC + 1-bit DAC**
  - **12-level**
  - **1-bit ADC + 12-tap FIR**
  - **Ideal**
FIR DAC and Element Mismatch

Mismatch does not lead to non-linearity

Semi-digital Implementation
Mismatch does not lead to non-linearity
Improved 1-bit CTDSM: FIR Feedback

\[ u(t) - v_1(t) \rightarrow \text{very small} \]

\[ \rightarrow \text{Improved loop filter linearity} \]
Summary so far ...

- Single bit ADC + FIR DAC
  - Low power ADC, easy to drive
  - Inherently linear DAC, no DEM
  - Low jitter sensitivity
  - Improved loop filter linearity

Benefits of single bit operation
Key Takeaway

Multi Bit DSM
✓ Tolerates jitter
✓ Low power loop filter

Single Bit DSM
✓ Low power ADC
✓ Inherently linear DAC

Single-bit ADC + FIR DAC combines benefits of 1-bit and multi-bit operation
Single-bit ADC + FIR DAC

- but dormant for a long while – why?
  - (?) Multibit & DEM well established by 2003
  - (?) More difficult to understand
  - (?) Stability

(G)old Idea:
B.Putter, ISSCC 2003; O.Oliaei, TCAS-II 2003
FIR DAC Summary

- Low power loop ADC
- Simple DAC – no DEM
- Multilevel feedback waveform
  - Improved loop filter linearity
  - Reduced clock jitter sensitivity
- Performance benefits of a multibit quantizer
  - But with low power
FIR DAC: Number of taps

What prevents us from using a large number of taps? (say 1000)

- More FIR taps → Better filtering
- → Reduced clock jitter sensitivity, better linearity
Increasing FIR Length

Large $v_{\text{error}}$ due to inadequate filtering of shaped quantization noise
Increasing FIR Length

Smaller $v_{\text{error}}$ due to better filtering
Increasing FIR Length

$$V_{\text{error}}$$

$$V_{\text{in}}$$

$$V_1$$

Large $$v_{\text{error}}$$ due to higher phase shift

64 taps
Error Signal Magnitude

Better filtering of shaped quantization noise

12 taps chosen in this design
Modulator Architecture

Third Order CIFF-B Prototype
FIR Feedback : More Benefits
1/f Noise in CTDSMs

Dominant source of 1/f noise
1/f Noise Mitigation in CTDSMs

Brute Force Solution
- Increase device sizes
  → Increased parasitics
  → Reduced loop gain
  → Higher distortion
  → Higher area
1/f Noise Mitigation in CTDSMs

- **Chopping**
  - Modulates 1/f noise out of the signal band
Chopping in CT $\Delta\Sigma$-Modulators
Chopping in a CTΔΣM

Chopped Integrator

Rest of Loop Filter

D = ±1

Chopped Integrator

\[ R \]

\[ C \]

\[ f_c \]

\[ f_s \]

\[ V_{in} \]
Chopping in a CTΔΣM
Chopping transition at $t = t_1$

$$v_x(t) \approx \frac{v_d(t)}{RG_{ota}}$$

Chopping transition at $t = t_1$
\[ v_x(t) \approx \frac{v_d(t)}{RG_{ota}} \]

For \( t = t_1^- \):
\[ v_x(t_1) = \frac{v_d(t_1^-)}{RG_{ota}} \]

For \( t = t_1^+ \):
\[ v_x(t_1) = -\frac{v_d(t_1^+)}{RG_{ota}} \]
At EVERY transition of the chopping clock

\[ \Delta V = -2v_x(t_1) \]
At EVERY transition of the chopping clock

Error charge due to chopping

\[ i_x = -2C_i v_x(t_1) \delta(t - t_1) \]
Error Model of a Chopped Integrator

\[ i_x = -2C_i v_x(t_1) \delta(t - t_1) \]

\[ v_x \approx \frac{v_d}{RG_{ota}} \]
Error current injected at every edge of $f_{ch}$

→ Sampling the virtual ground at $2f_{ch}$

→ Error proportional to $C_i/RG_{ota}$
Aliasing
Signal band

PSD (dB)

$0$

$-60$

$-120$

$0$

$f_{ch}$

$2f_{ch}$

$3f_{ch}$

$4f_{ch}$

$\frac{f_s}{2}$
Output parasitic switched at every edge of $f_{ch}$
Chopped $C_o$ : Equivalent Resistor

Reduced Integrator DC Gain

$$R_{DC} = \frac{1}{2f_{ch}C_o}$$
Chopping in CTDSMs: Summary

- Aliases shaped noise from multiples of $2f_{ch}$
  - Inversely proportional to $G_{ota}R$
  - Inversely proportional to number of quantizer levels
Chopping in CTDSMs: Summary

- Reduced integrator gain
  - Switched capacitor resistor at the output \(1/(4f_{ch}C_o)\)
  - More 1/f noise from rest of loop
Chopping in CTDSMs: Summary

Solutions

Increase $G_{\text{otaR}}$

✗ 20dB reduction of alias noise dissipates 10x power

Increase number of quantizer levels

✗ 20dB reduction of alias noise needs 10x the number of levels
FIR Feedback DAC

\[ \frac{1}{RG_{ota}} \]

\[ u \rightarrow + \rightarrow V_d \rightarrow - \rightarrow FIR DAC \]

\[ \frac{\omega_1}{s} \]

Rest of Loop

N taps

f_s/N, 2f_s/N, 3f_s/N, 4f_s/N
FIR Feedback and Chopping

Chopping frequency chosen as \( f_s/2N \)

\[ f_{ch} = \frac{f_s}{2N} \]

→ Nulls at multiples of \( 2f_{ch} \)

→ Reduced aliasing of shaped noise
1-bit quantizer & FIR Feedback: Summary

- Reduced jitter sensitivity
- Improved integrator linearity
- Reduced chopping artifacts
- Inherently linear DAC

Diagram:
- \( \frac{1}{RG_{ota}} \)
- \( \omega_1 / s \)
- FIR DAC
- Rest of Loop
- D
- u
- V_d
- N taps

Diagram notes:
- Input u
- Output D
- Feedback path with FIR DAC
Architecture and Circuit Design
3rd Order CTDSM Architecture

- Active-RC Integrators
- CIFF-B Loop Filter
- 12 tap FIR DAC
- 12 tap compensation DAC
- Input feed forward

\[ f_{ch} = \frac{f_s}{24} \]
3rd Order CTDSM Architecture

Chopped at $f_s/24 = 256\text{kHz}$
3rd Order CTDSM Architecture

Semidigital Implementation

Worst case attenuation > 35dB
Monte Carlo: 1% random tap mismatch

\[ |H_{FR}(i\omega)| (\text{dB}) \]

-25
-30
-35
-40
-45
-50
-55
-60

\[ f/f_{\text{ch}} \]

7.85 7.9 7.95 8 8.05 8.1 8.15

2 \cdot \text{BW}

Attenuation > 35dB
OTA Design
2 Stage Feedforward Compensated OTA

2\textsuperscript{nd} Stage

NMOS/PMOS input pair → 2x $g_m$ for the same current

Cascodes → High DC gain
CMFB compensation capacitors
Small fraction ($c_1$) inside chopper
→ Compensation during chop transitions
Measurement Results
Die Photo & Layout Snapshot

UMC 180nm CMOS process
(Europractice)
Dynamic Range Plot

Peak SNR: 99.3 dB
Peak SNDR: 98.5 dB
DR : 103.5 dB
PSD at Peak SNDR

**SNR:** 99.3 dB  
**SNDR:** 98.5 dB

**Input -3.4 dBFS @ 6kHz**

**HD₂ = 118.9 dB**  
**HD₃ = 107.6 dB**  
**Chopping tone**
Low Frequency PSD

No chopping

PSD (dBFS)

f (Hz)
Low Frequency PSD

$f_{ch} = f_s = 6.144$ MHz
Low Frequency PSD

\[ f_{\text{ch}} = \frac{f_s}{24} = 256 \text{ kHz} \]
Low Frequency PSD

1/f corner ~ 3Hz

50Hz Harmonics

2nd Harm.

3rd Harm.

Tones
Effect of changing $f_{ch}$

**Increased Aliasing**

$f_{ch} = f_s/20 = 312.2\text{kHz}$

$f_{ch} = f_s/24 = 256\text{kHz}$
PSD Comparison: $f_c = \frac{f_s}{24} \& \frac{f_s}{20}$

$P_{sd} \text{(dBFS)}$

$f (kHz)$

$f_{ch} = \frac{f_s}{20}$

$f_{ch} = \frac{f_s}{24}$
PSD Comparison

No chopping, devices 16x larger ([3], JSSC 2014)

$\frac{f_{\text{ch}}}{f_s} = \frac{24}{f_s}$
## Performance Summary and Comparison

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<thead>
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<tbody>
<tr>
<td>BW (kHz)</td>
<td>24</td>
<td>24</td>
<td>20</td>
<td>24</td>
<td>24</td>
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<tr>
<td>Feature Size (nm)</td>
<td>180</td>
<td>180</td>
<td>45</td>
<td>65</td>
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<tr>
<td>Supply (V)</td>
<td>1.8</td>
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<td>1.1</td>
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<tr>
<td>Power (µW)</td>
<td>280</td>
<td>280</td>
<td>1200</td>
<td>121</td>
<td>9900</td>
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<tr>
<td>Peak SNDR (dB)</td>
<td>98.5</td>
<td>98.2</td>
<td>76.5</td>
<td>85</td>
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<td>DR (dB)</td>
<td>103.6</td>
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<td>91.7</td>
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<td>SFDR (dB)</td>
<td>107.6</td>
<td>106</td>
<td>80.5</td>
<td>90</td>
<td>102.6</td>
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<td>Chop Freq. (kHz)</td>
<td>256</td>
<td>-</td>
<td>46</td>
<td>-</td>
<td>-</td>
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<tr>
<td>FoM_{SNDR} (fJ/lvl)</td>
<td>85</td>
<td>88</td>
<td>500</td>
<td>173.4</td>
<td>342</td>
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<td>FoM_{Schreier} (dB)</td>
<td>177.8</td>
<td>177.5</td>
<td>148.5</td>
<td>168</td>
<td>172</td>
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A Tale of 4 ADCs

- Multi-bit (4-bit ADC in the loop)
  - ESSCIRC 2007, JSSC 2008

- Single-bit ADC with linearity enhancement
  - ESSCIRC 2009, JSSC 2010

- Single-bit ADC + 12-tap FIR DAC
  - ASSCC 2013, JSSC 2014

- Single-bit ADC + 12-tap FIR DAC + Chopping
  - ISSCC 2016, JSSC 2017

- Same process, same design group
Multi-bit Modulator

- Third order CIFF loop
- 4-bit flash ADC
- OSR = 64 (Clock Rate = 3.072 MHz)
- NRZ Resistive DAC
- Data Weighted Averaging

IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 43, NO. 2, FEBRUARY 2008

A Power Optimized Continuous-Time ΔΣ ADC for Audio Applications

Shanthi Pavan, Nagendra Krishnapura, Ramalingam Pandarinathan, and Prabu Sankar
Single-bit Modulator

• Third order CIFF loop
• 1-bit ADC
• OSR = 128 (Clock Rate = 6.144 MHz)
• NRZ Resistive DAC

Power Reduction in Continuous-Time Delta-Sigma Modulators Using the Assisted Opamp Technique
First integrator has to be very linear
The Assisted-Opamp Integrator

Assistant
1-bit + FIR DAC Based Modulator

- Third order CIFF-B loop
- 1-bit ADC + 12-tap FIR DAC
- OSR = 128 (Clock Rate = 6.144 MHz)
- NRZ Resistive DAC
Low Power Design Techniques for Single-Bit Audio Continuous-Time Delta Sigma ADCs Using FIR Feedback

Amrith Sukumaran and Shanthi Pavan, Senior Member, IEEE
1-bit + FIR DAC + Chopping

• Third order CIFF-B loop
• 1-bit ADC + 12-tap FIR DAC
• OSR = 128 (Clock Rate = 6.144 MHz)
• NRZ Resistive DAC
• First integrator chopped at $f_s/24$
• ISSCC 2016
### Performance Summary and Comparison

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Conclusions

- FIR feedback
  - Simple 1-bit ADC
  - Reduced ADC power and area
  - Simplified clock distribution
  - Inherently linear DAC → No DEM
  - Relaxes integrator linearity and jitter requirements
  - Chopping for free
  - Combines benefits of 1-bit and multi-bit operation
  - Highest Schreier FoM reported