ANALOG DEVICES

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Mixed-signal technologies for ultra-wide band signal processing systems

GABRIELE MANGANARO

Agenda

- Motivation / Applications
- Process Technology
- ADC architectures
- Integration
- Signal Chain Linearization
- Conclusion

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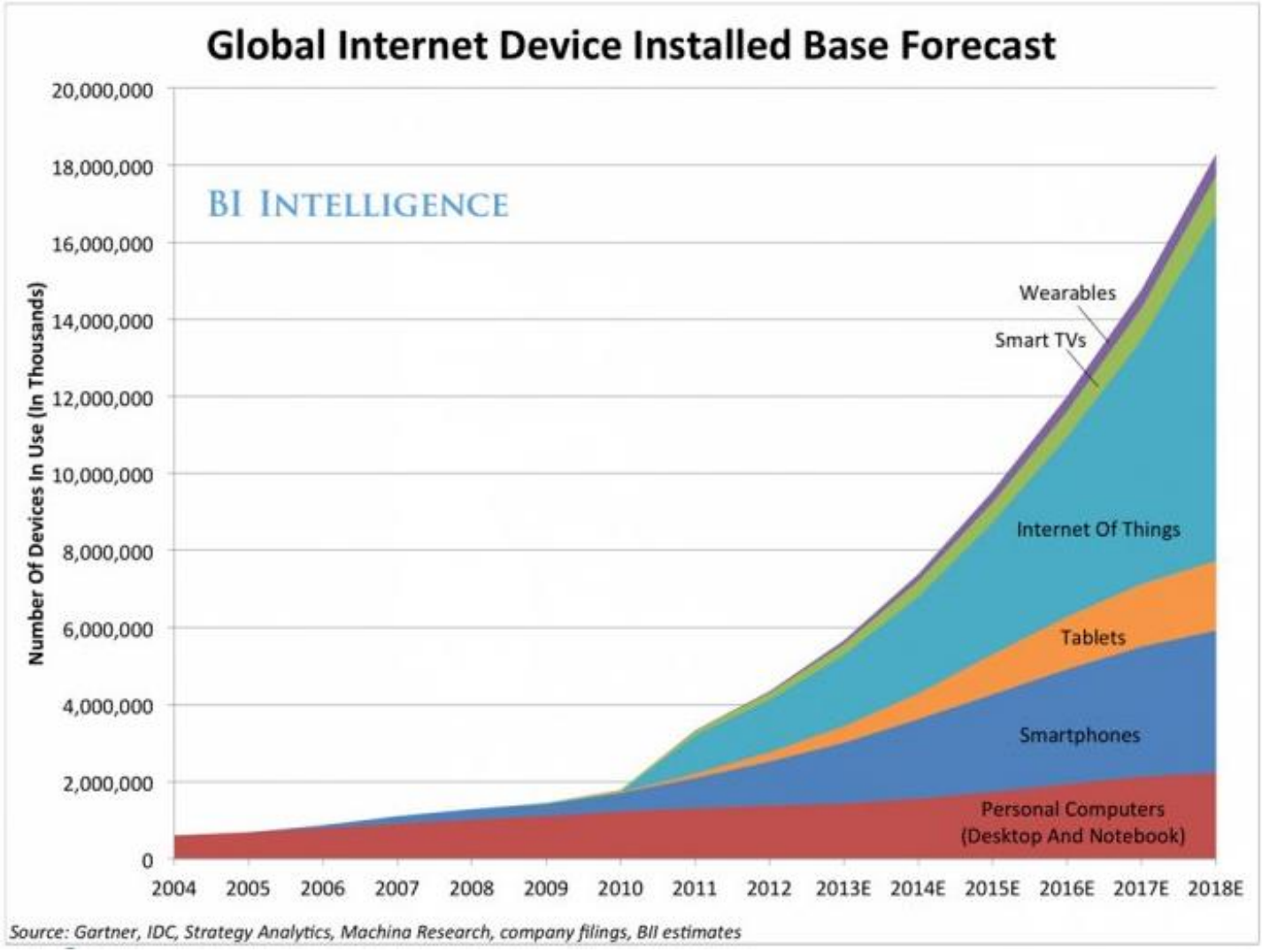
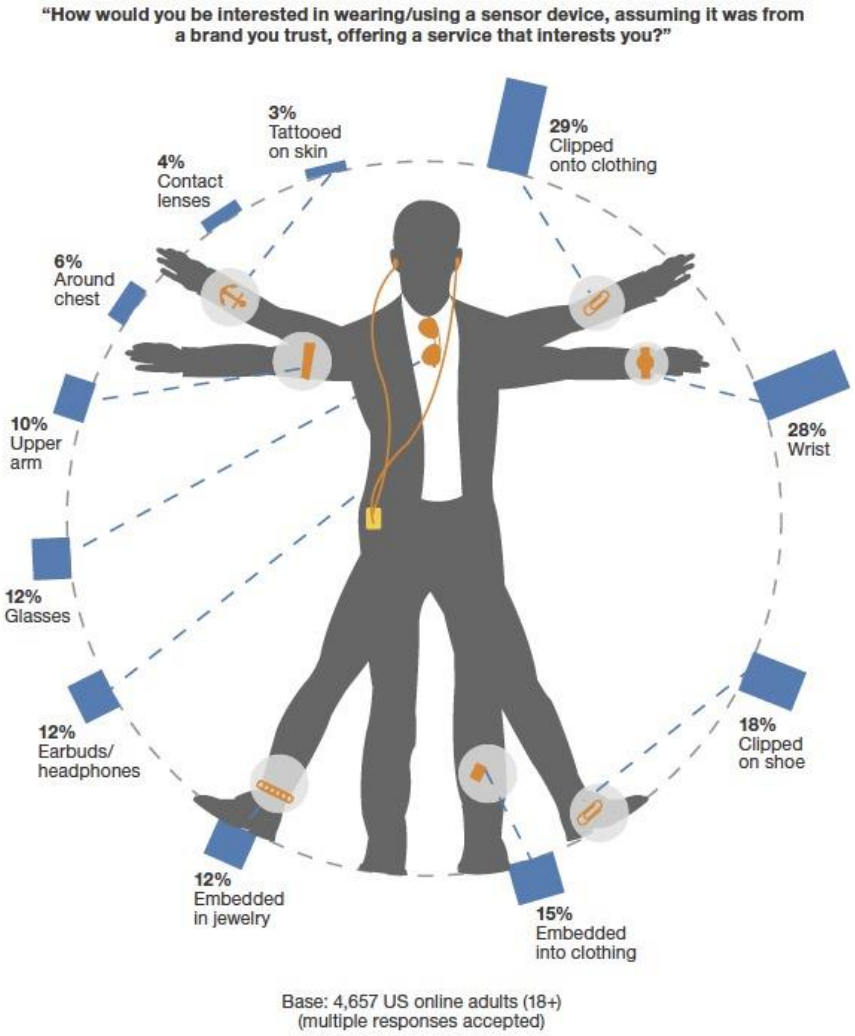
Motivation / Applications

Application drivers: mobility, pervasive computing, ...



Source: Gartner, IDC, Strategy Analytics, Machina Research, company filings, BII estimates



Source: North American Technographics® Consumer Technology Survey, 2013

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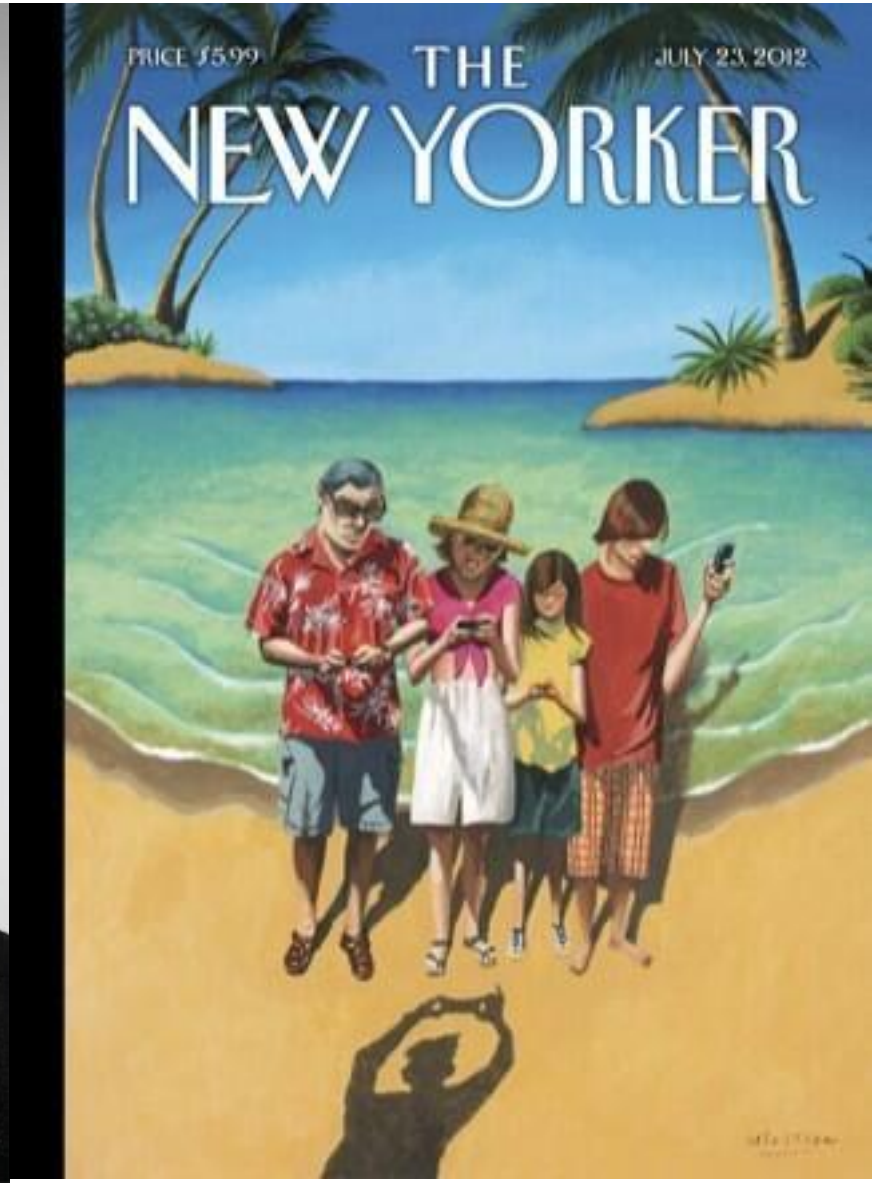
“We wanted flying cars, instead we got 140 characters” – Founders Fund (P. Thiel)



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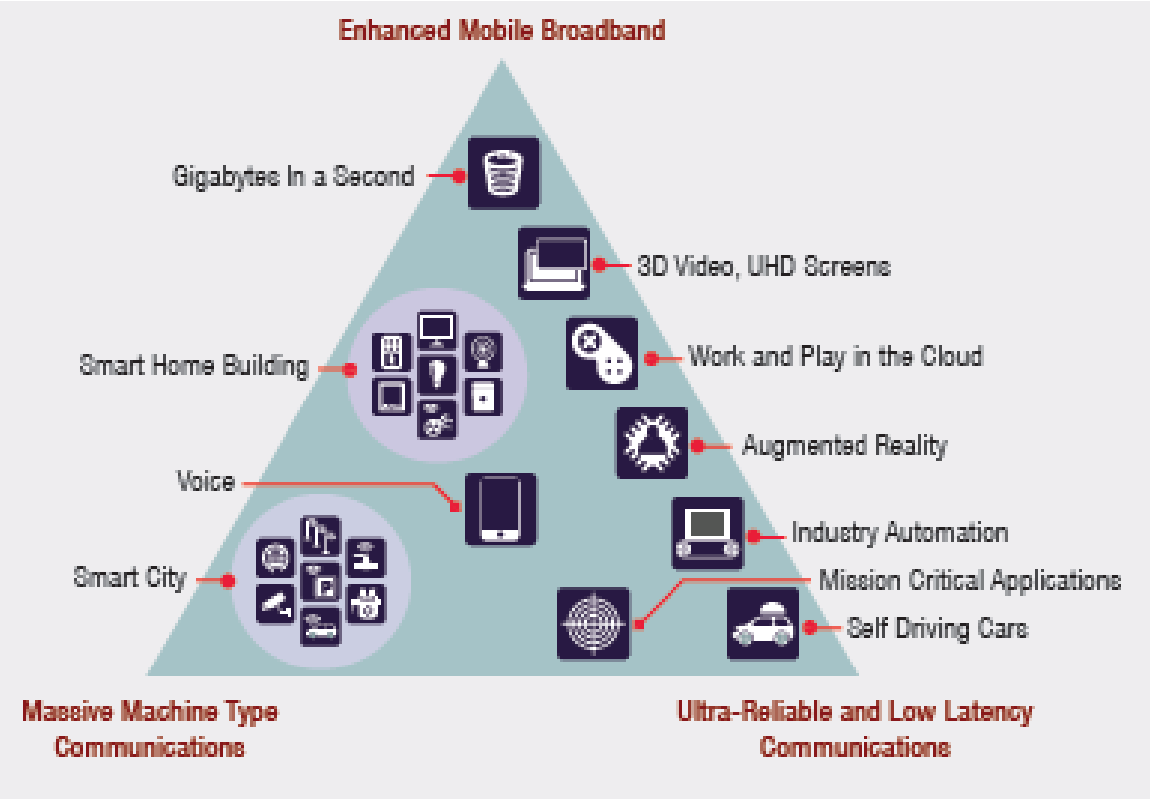
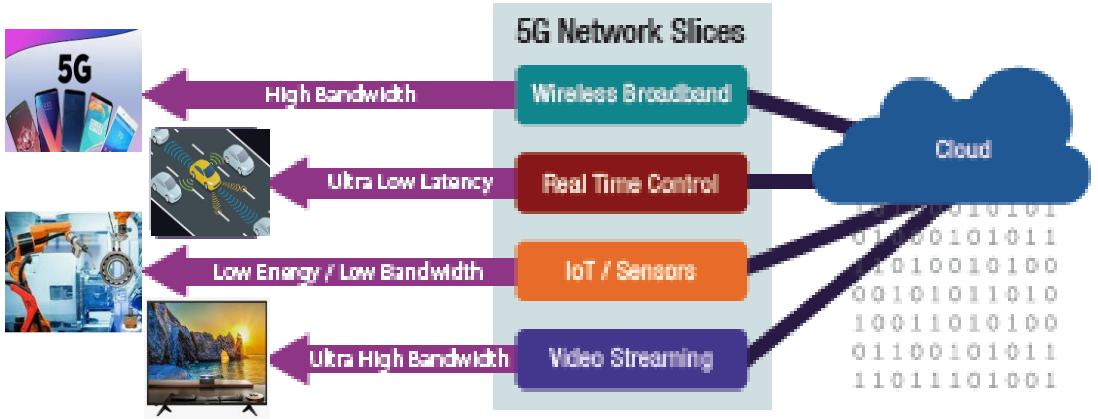
Wireless communication: 5G





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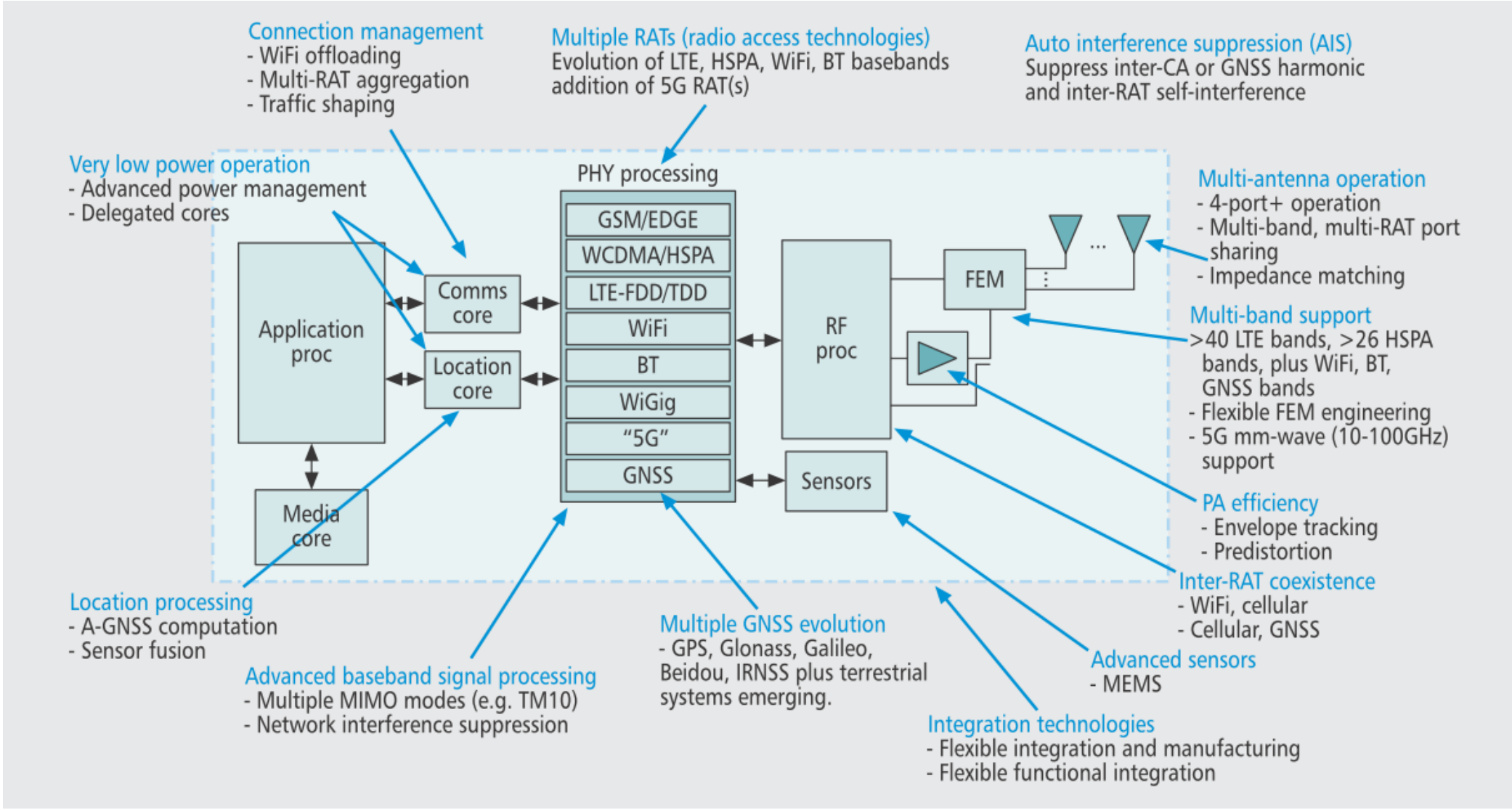
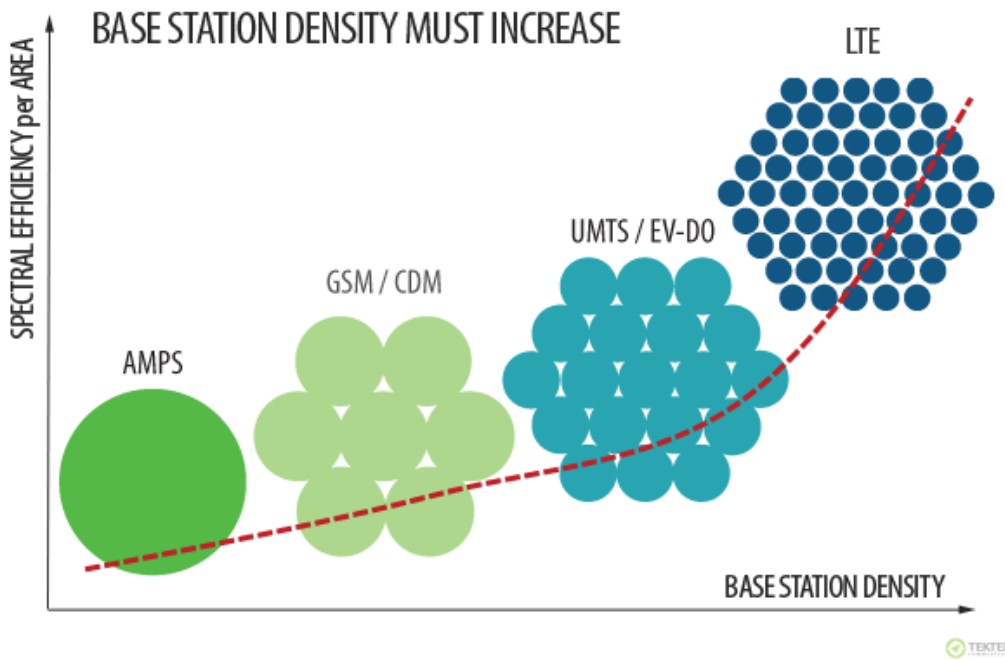
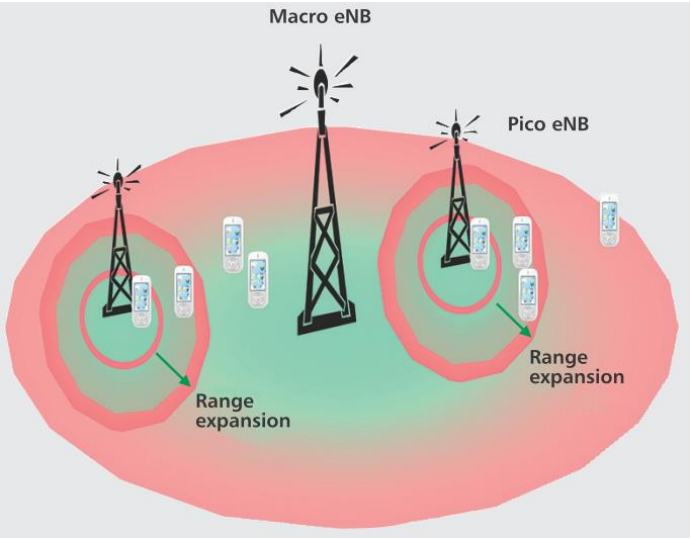
Wireless communication: 5G

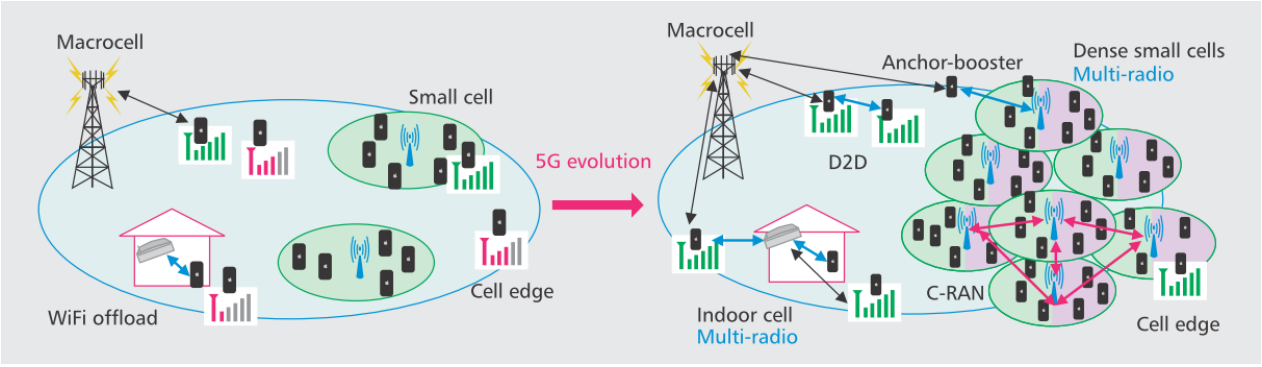


B. Bangerter et al., "Networks and devices for the 5G era", IEEE Communication Magazine, 2014

Densification/Range Extension

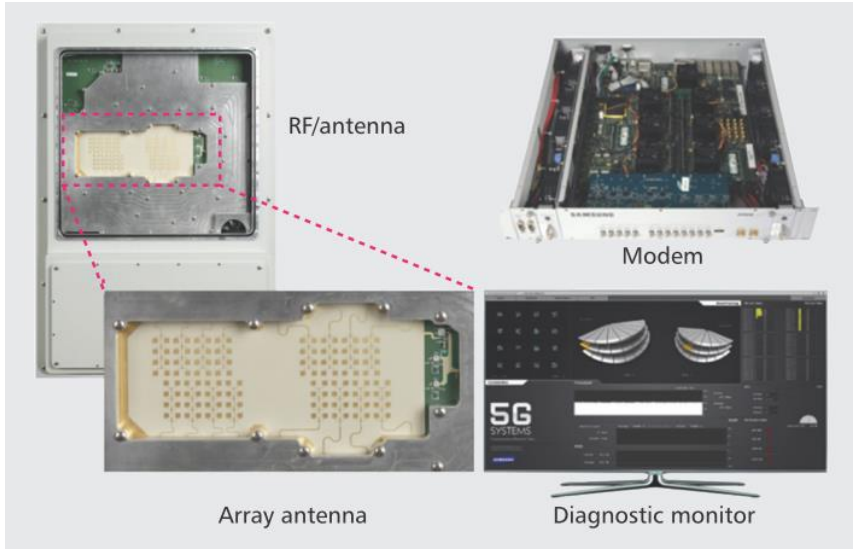


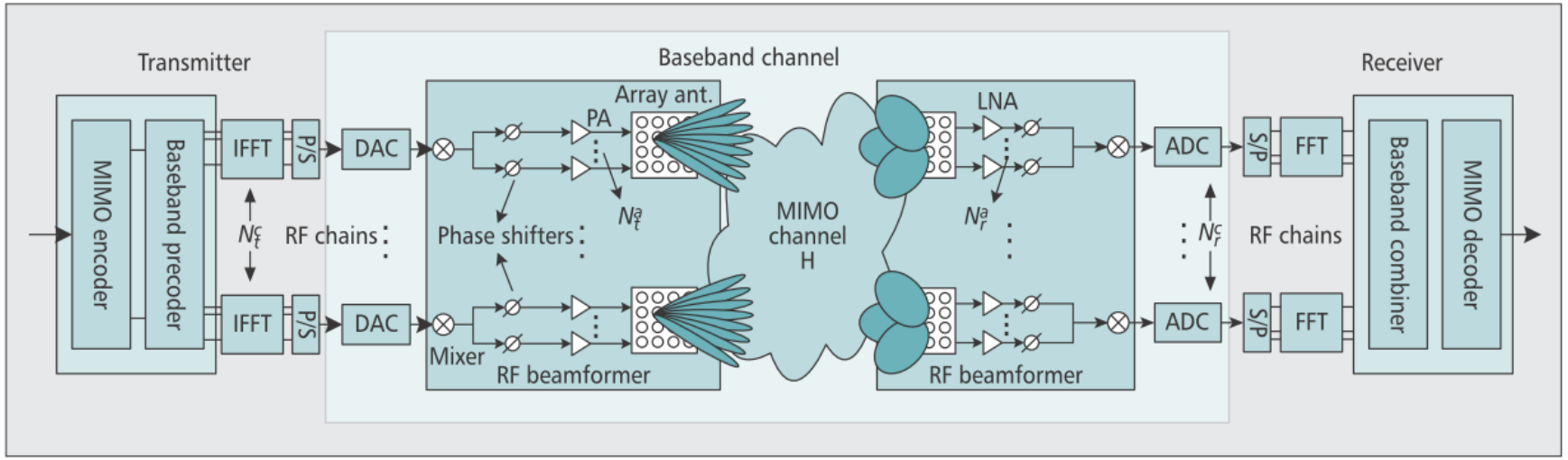




B. Bangerter et al., “Networks and devices for the 5G era”, IEEE Communication Magazine, 2014

Massive MIMO / Beamforming

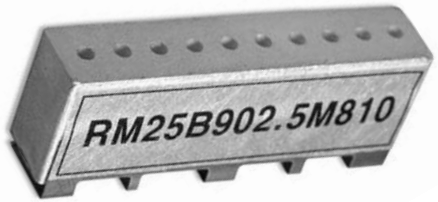




W. Roh et al., “Millimeter-wave beamforming as an enabling technology for 5G cellular…”, IEEE Communication Magazine, 2014

The $$ stuff that does not want to scale: duplexer & other filters

SAW
(photo lithography)



Ceramic Monoblock
(mechanical)

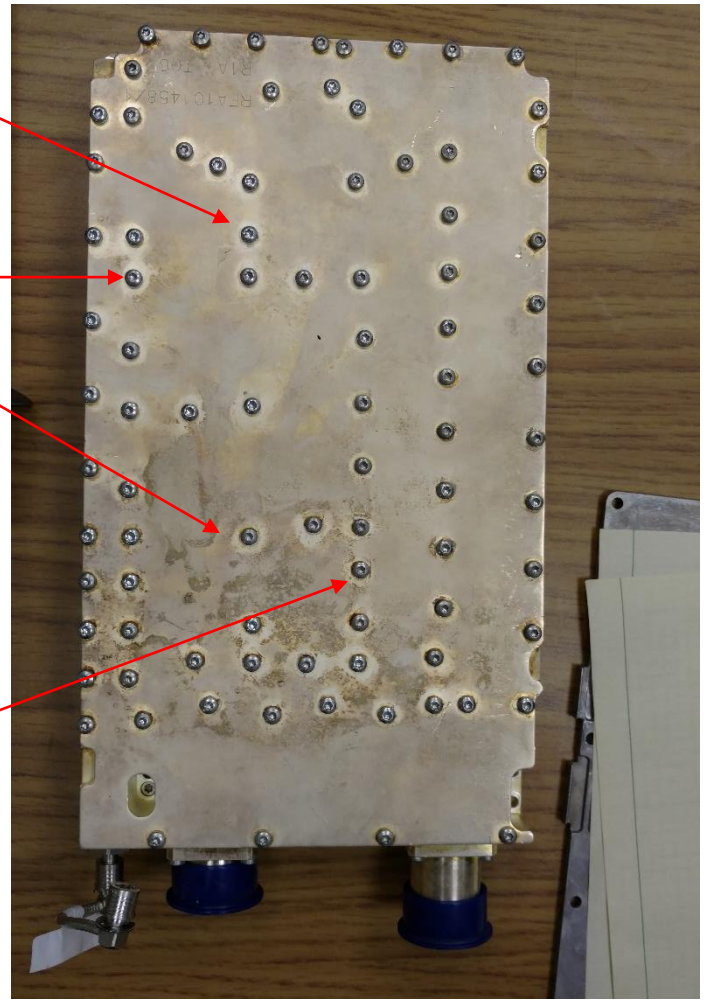
Cavity (GHz)
(manual assembly)

$$size \propto performance \qquad size \propto \frac{1}{frequency}$$

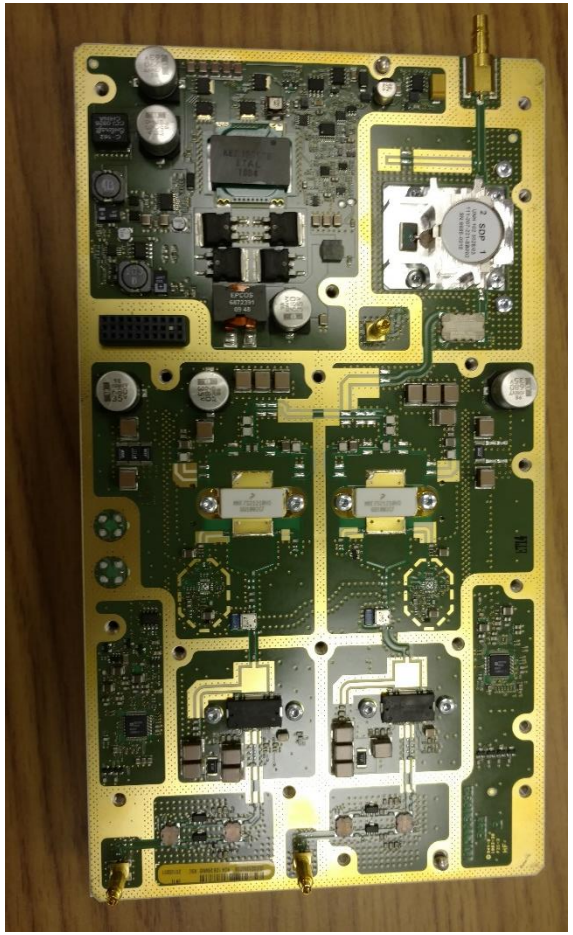
$$cost \propto size$$

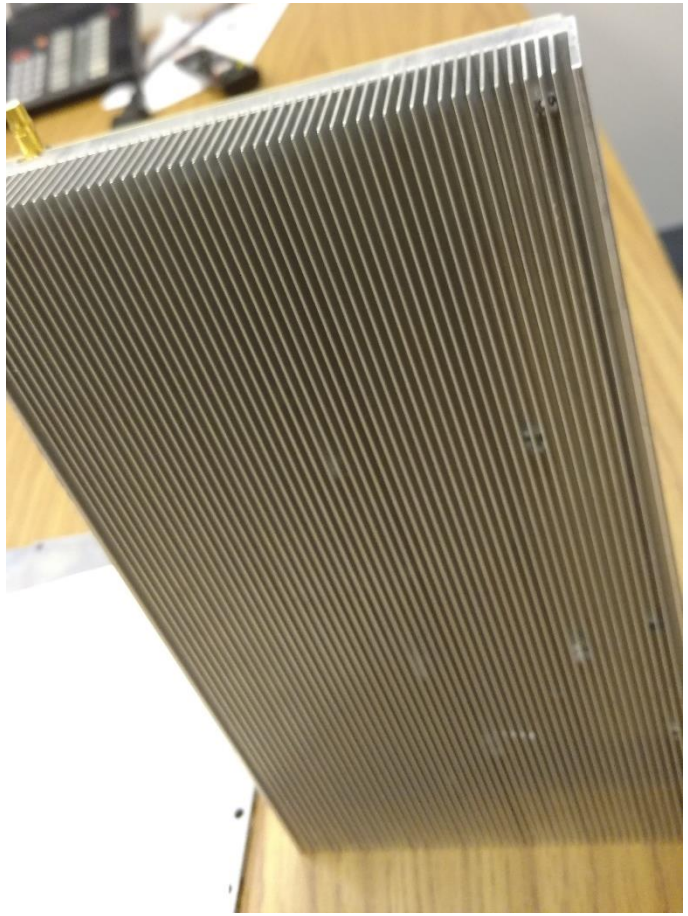
An actual BTS's duplexer

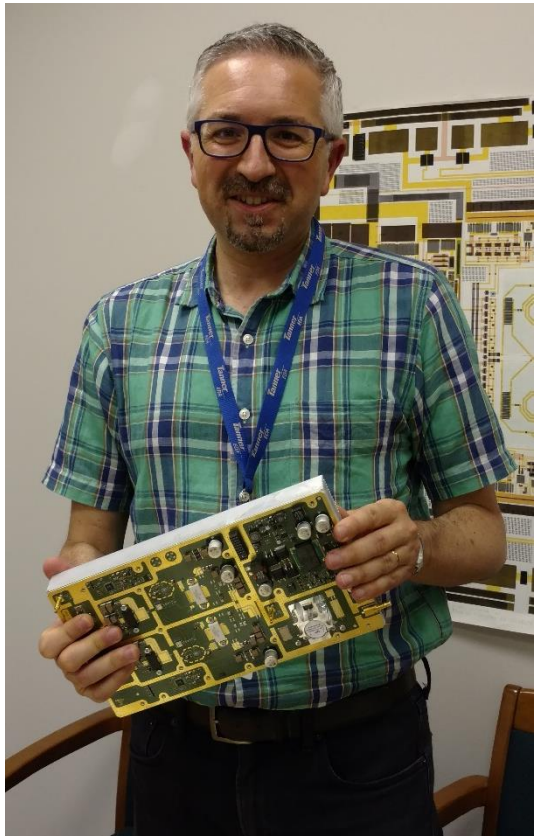
Tuning screws!!!



An actual power amplifier

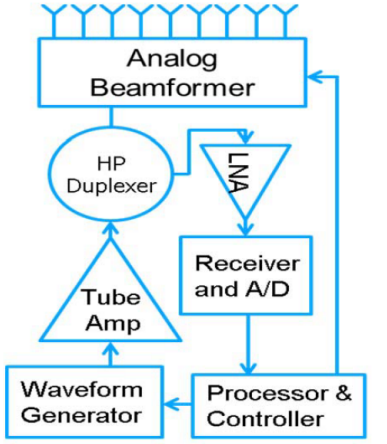






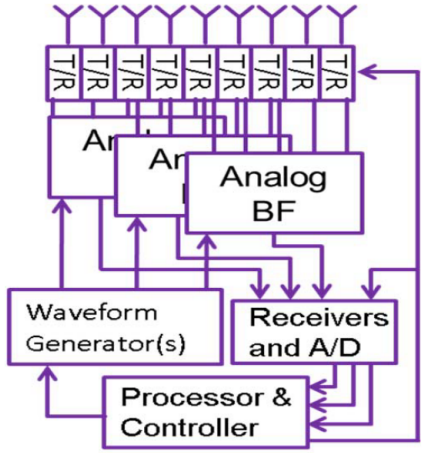
Phased array system evolution

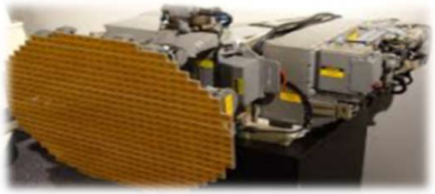
Classical



- All Analog Beamforming
- Centralized Receivers & Exciters
  - Low electronics content:

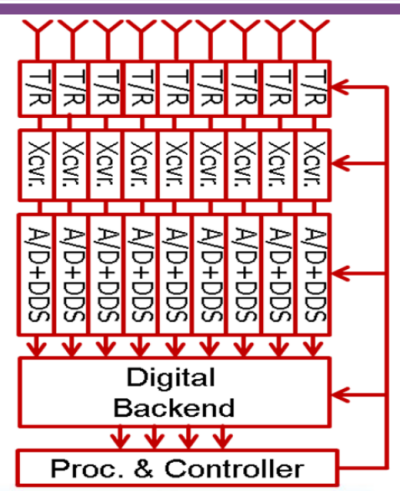
Hybrid Solution





- Sub-array Architecture
  - Analog/Digital Beamforming
- Distributed Receivers & Exciters
  - At Subarray Level

All Digital



- Every Element Digital Beamforming
  - No Analog Beamforming
- Distributed Receivers & Exciters
  - At a per element level

C. Fulton, et al., “Digital phased array systems: challenges and opportunities,” Proceedings of the IEEE, Vol. 104, Issue 3, Feb. 2016.

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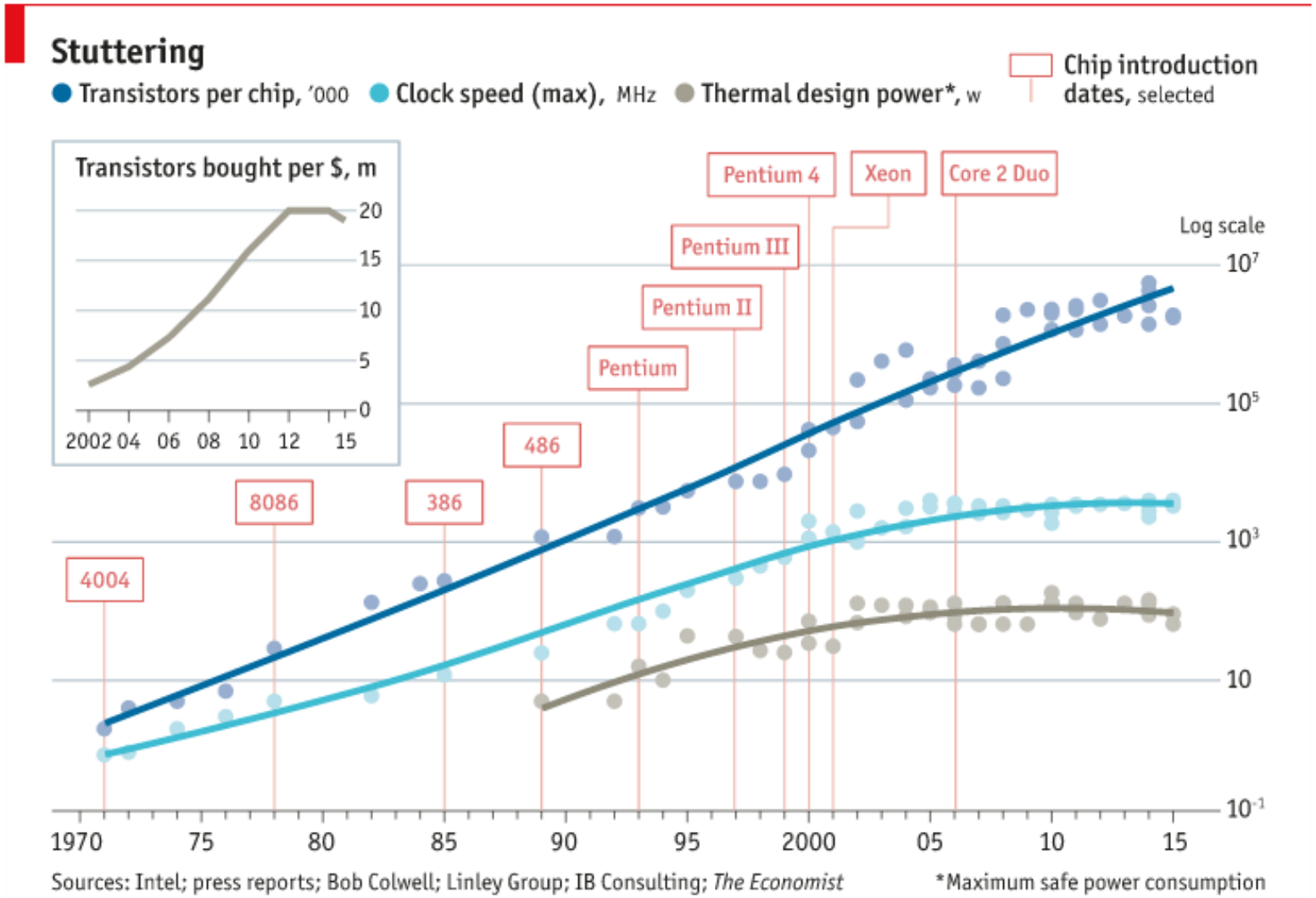
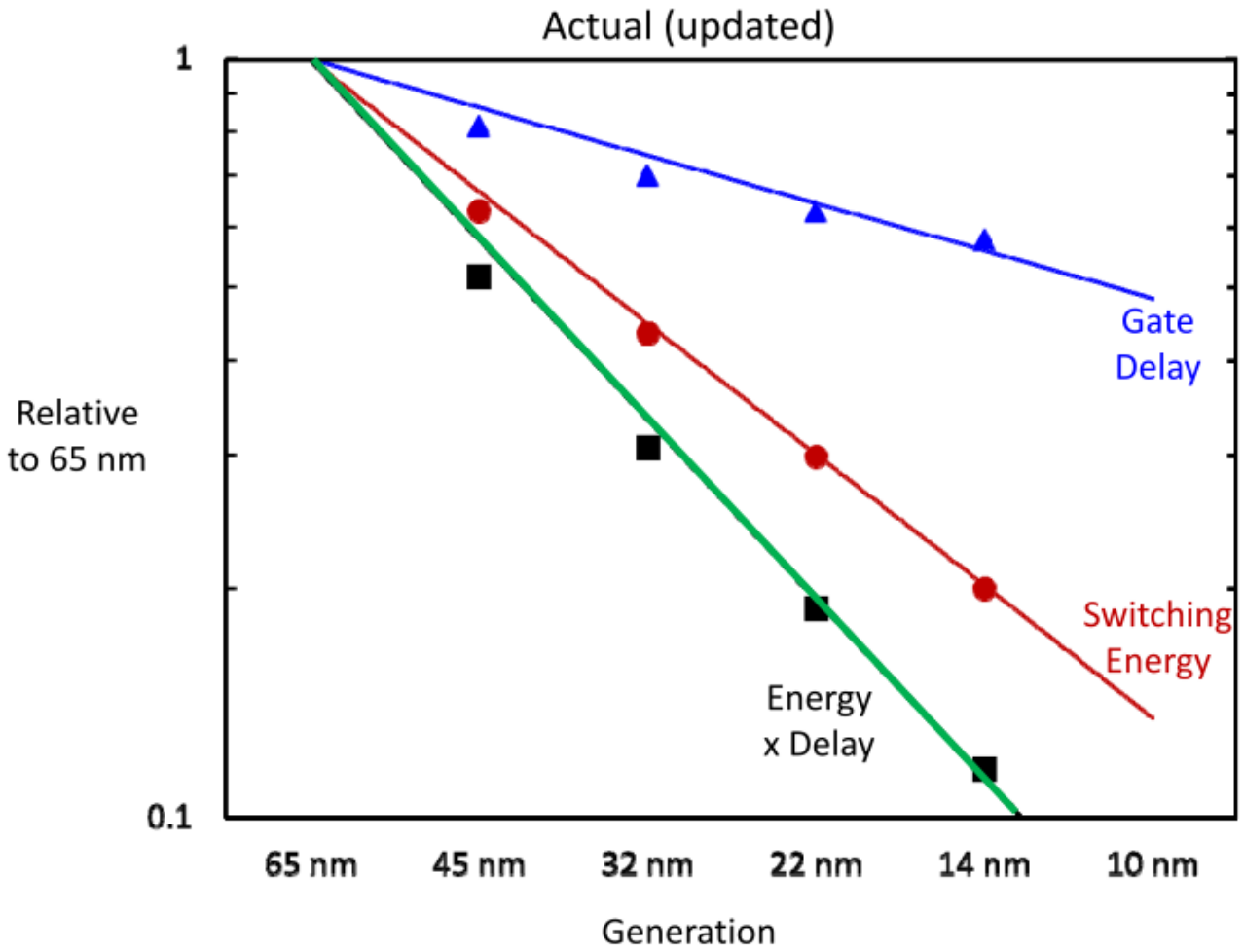
Process Technology

Moore’s law

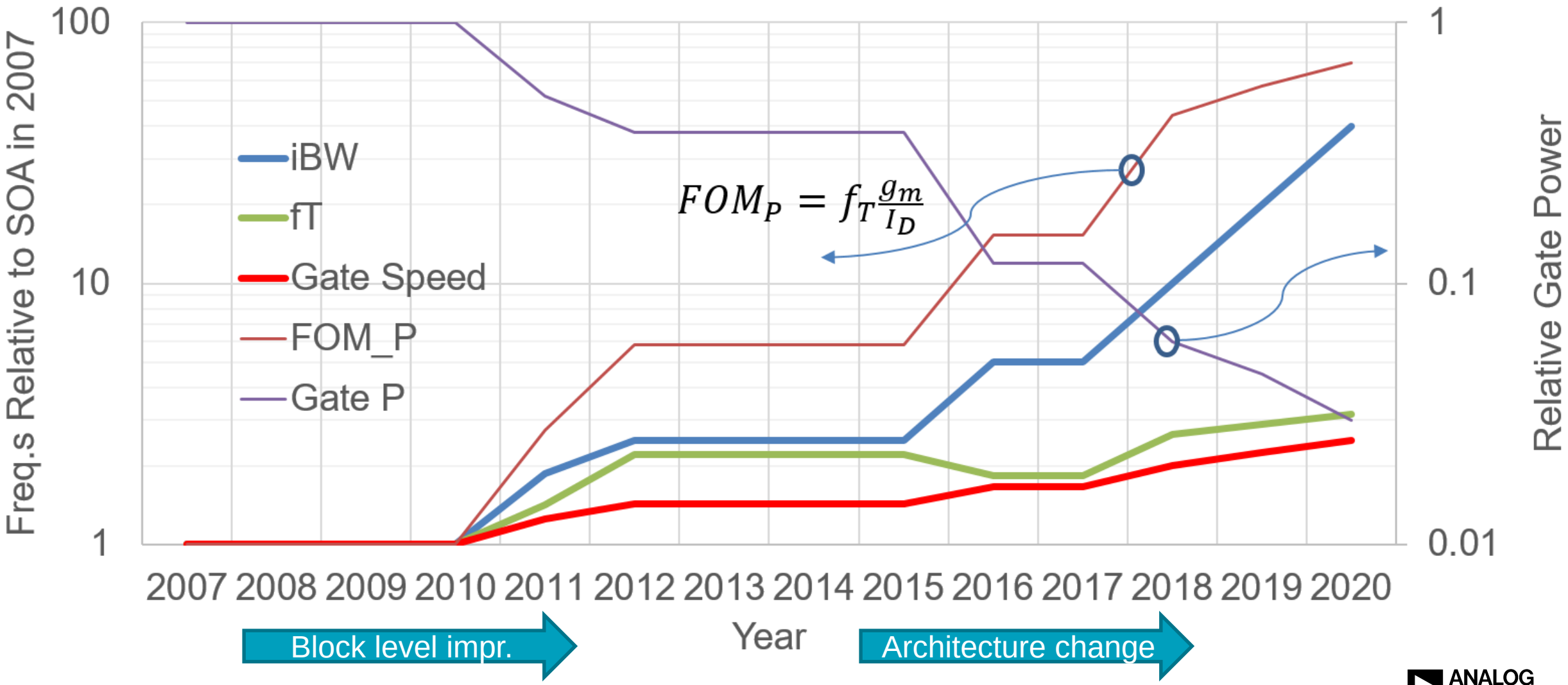


Higher digital power efficiency, but not (much) higher device speed!



Source: W.M.Holt, "Moore's Law: A path going forward", ISSCC 2016

Application pull: Wireless Infrastructure (BTS) bandwidth demand versus MS CMOS capability



G. Manganaro, “Emerging data converter architectures and techniques,” IEEE CICC, 2018.

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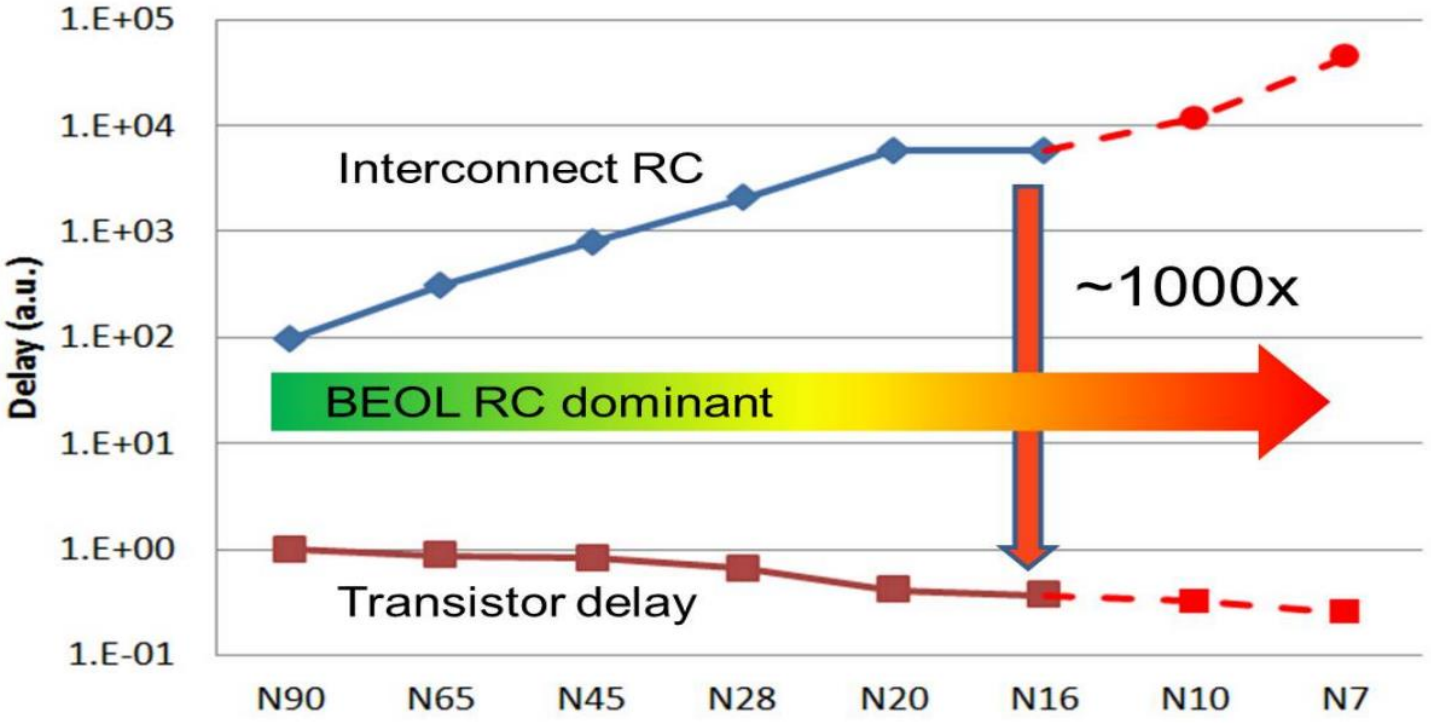
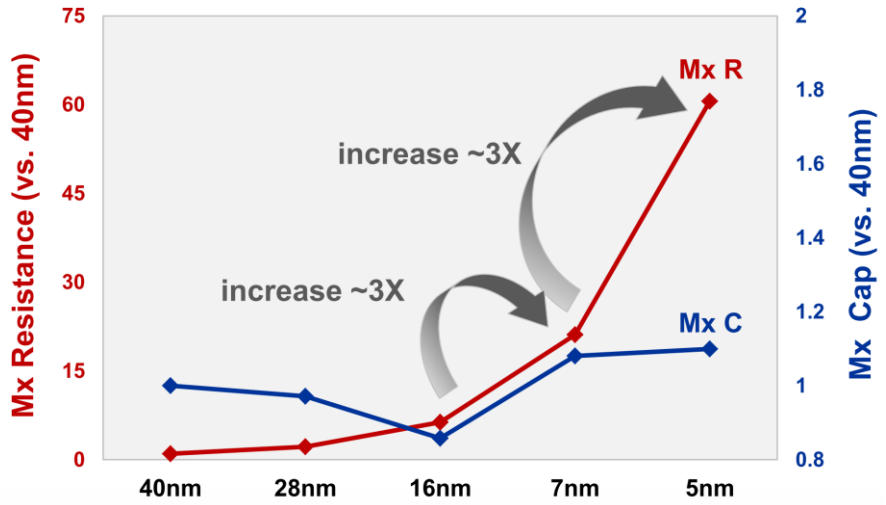
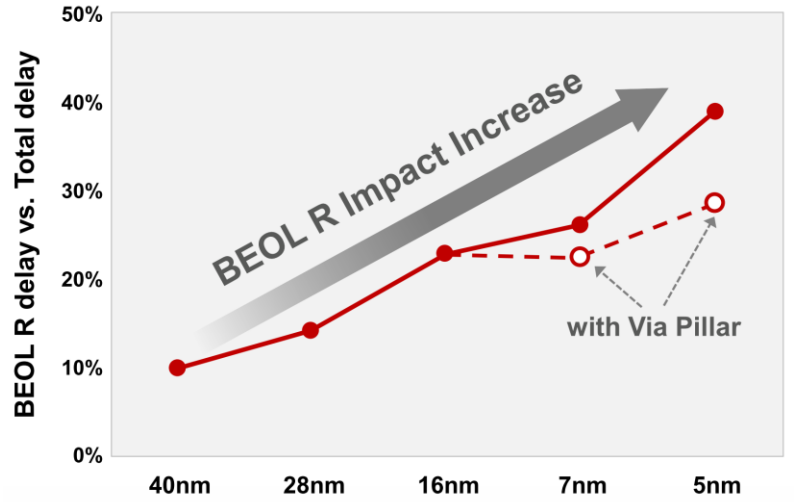
Die interconnects are the biggest bottleneck



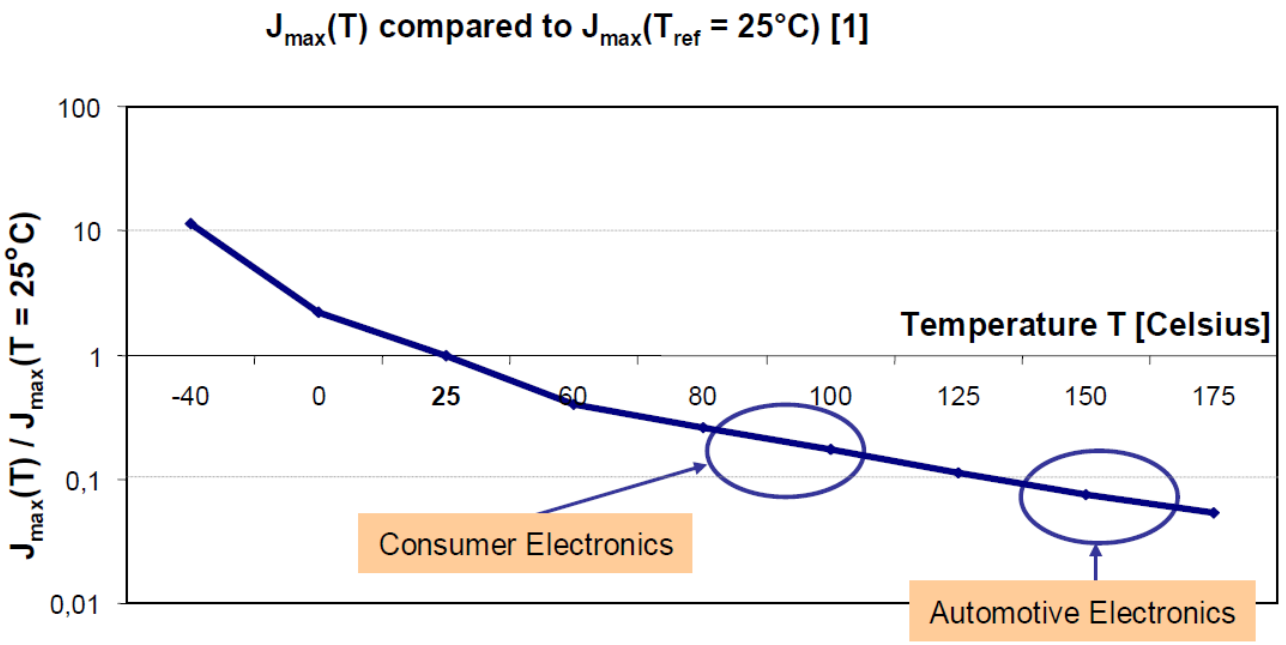
Source: G. Yeap (Qualcomm), IEEE Electron Devices Meeting (IEDM), 2013

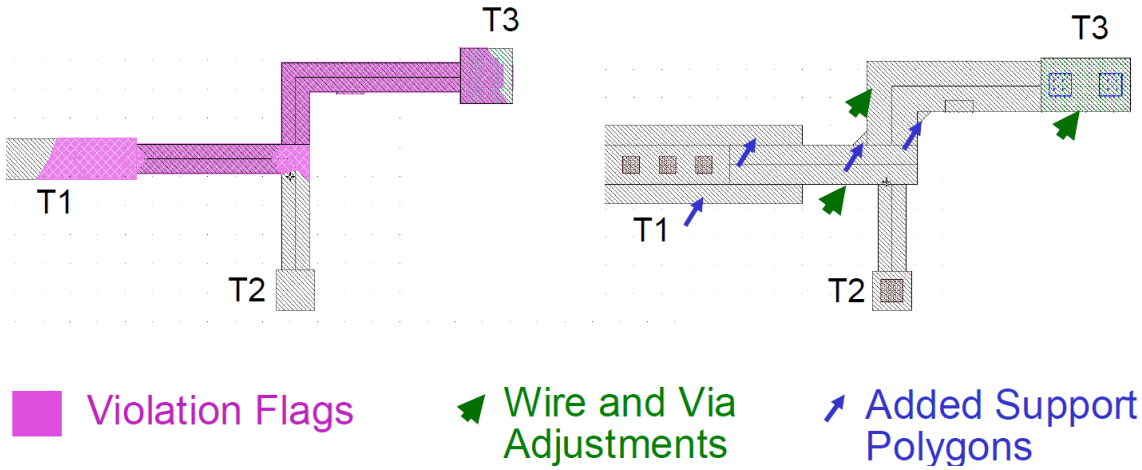




C. Hou (TSMC), ISSCC 2017 & L. Lu (TSMC), ISPD 2017

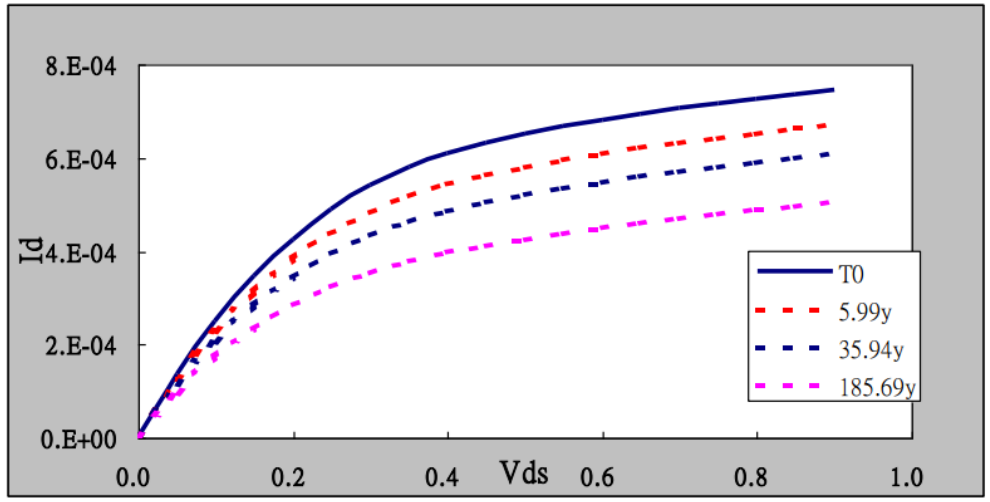
Electromigration

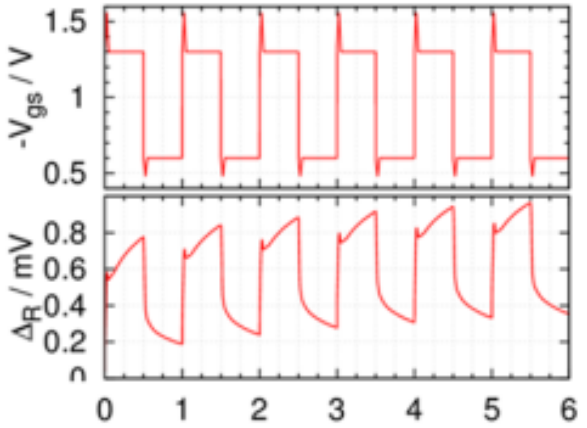




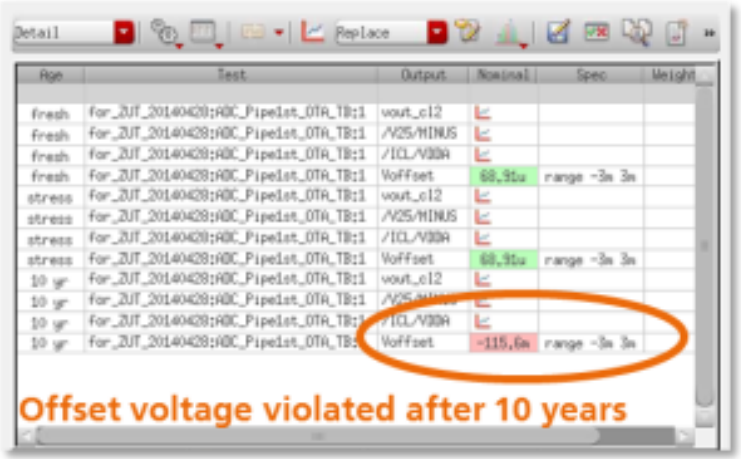
The maximum permissible current density of an aluminum metallization, calculated at e.g. 25°C, is reduced significantly when the temperature of the interconnect rises

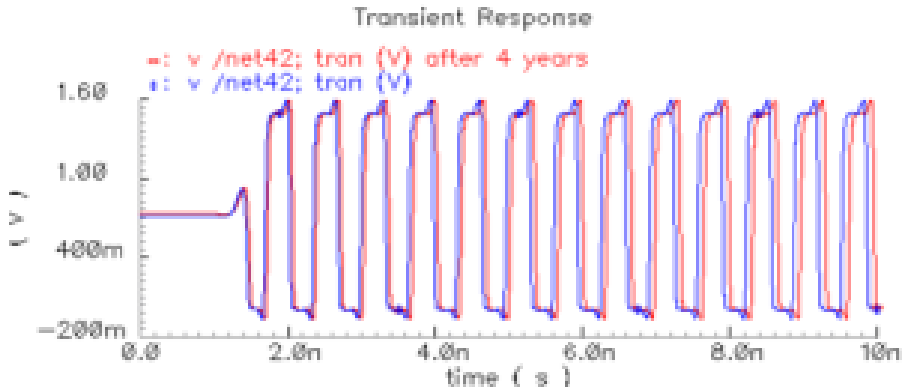
Device Aging





Vt shift due to NBTI degradation

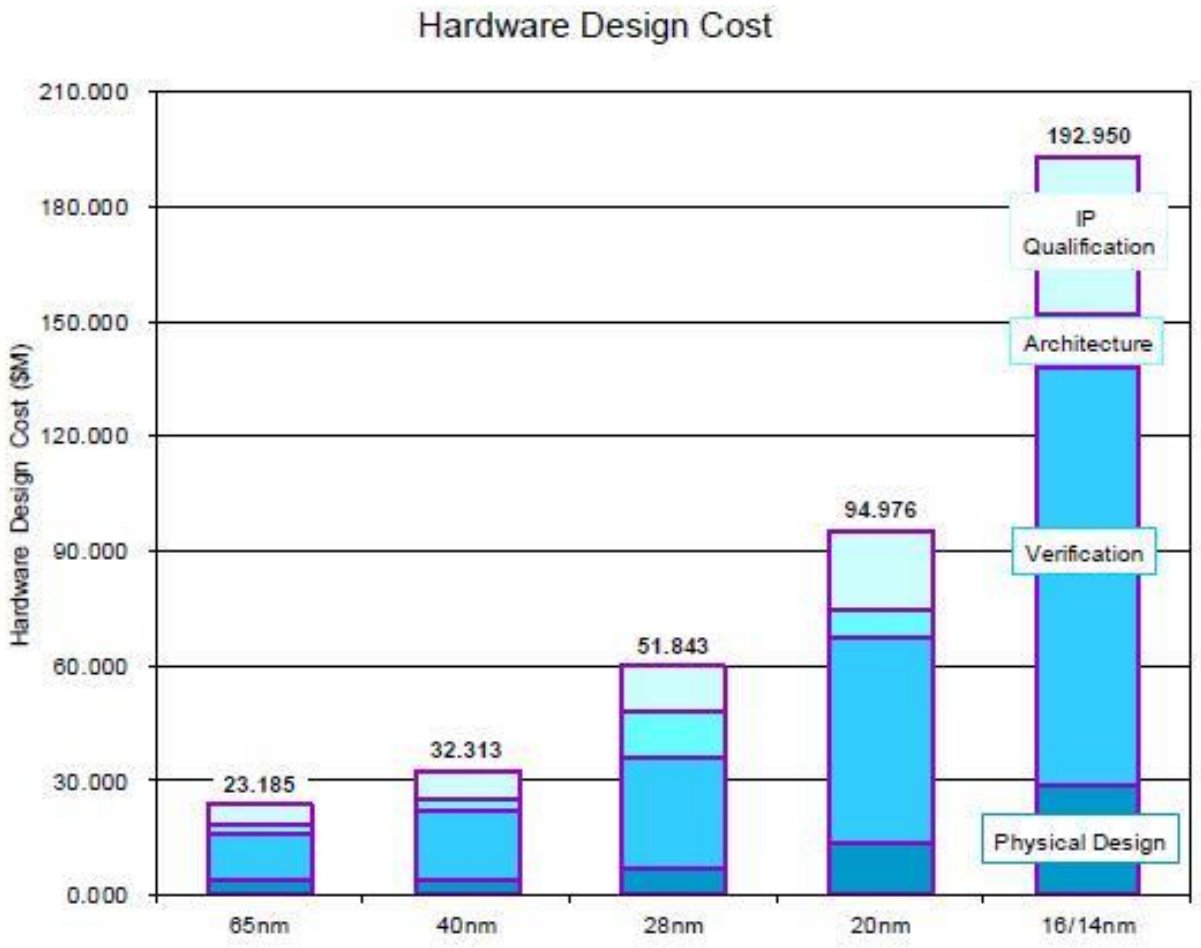




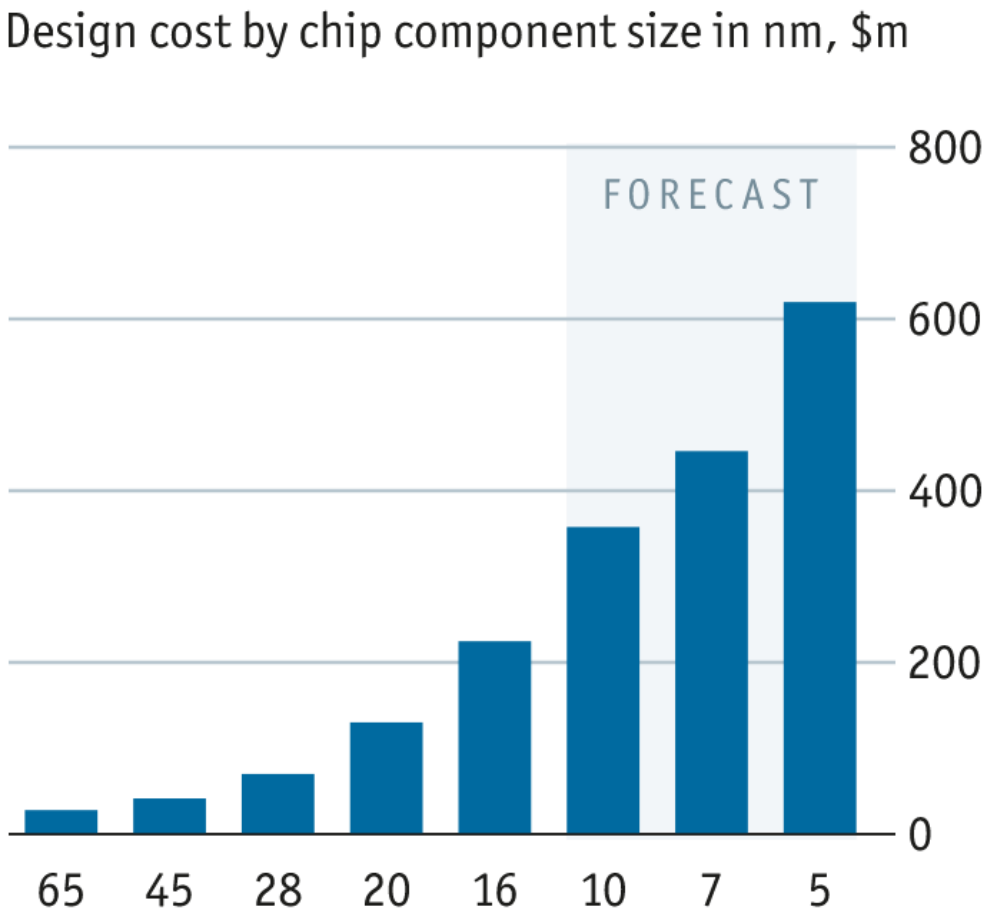
Frequency shift after 4 years of op.

Source: Fraunhofer Institute for Integrated Circuits

Complexity drives development cost



Source: International Business Strategies, Inc 2013 report



Source: IB Consulting

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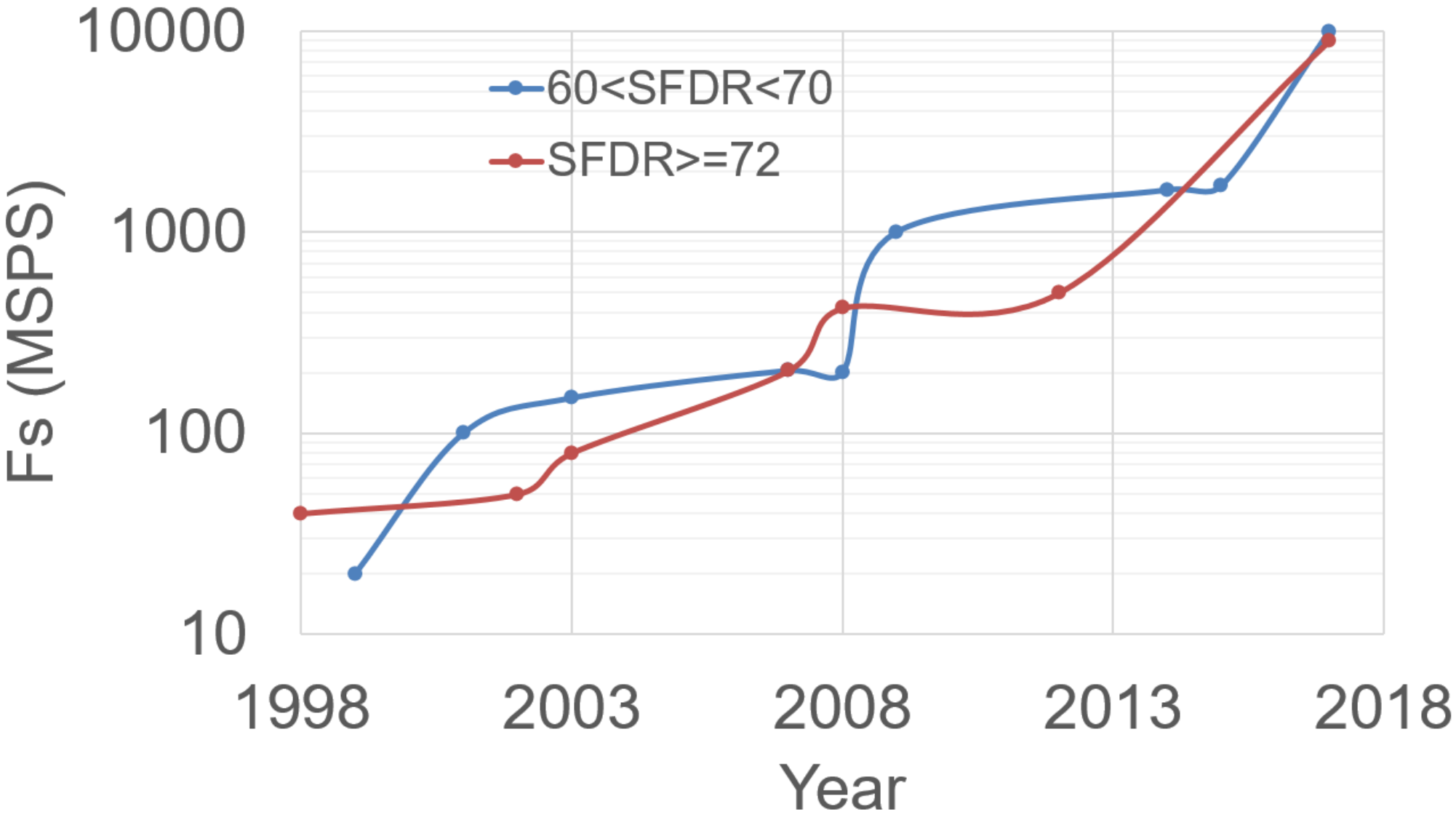
ADC architectures

Technology progression: 12b/14b High Speed (HS) ADC progression



G. Manganaro, “Emerging data converter architectures and techniques,” IEEE CICC, 2018.

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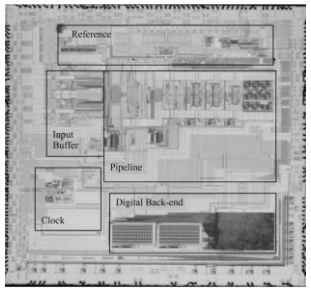
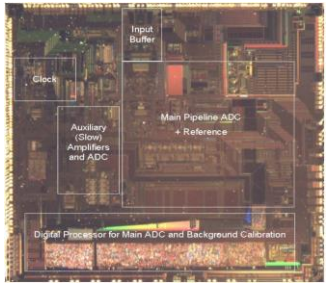
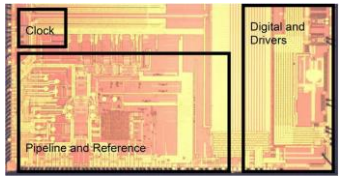
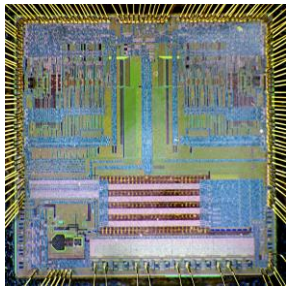
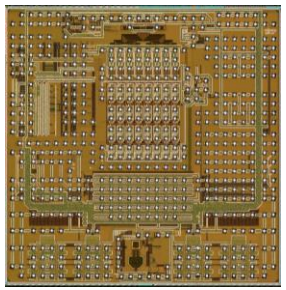
Analog/Digital composition for HS ADC cores







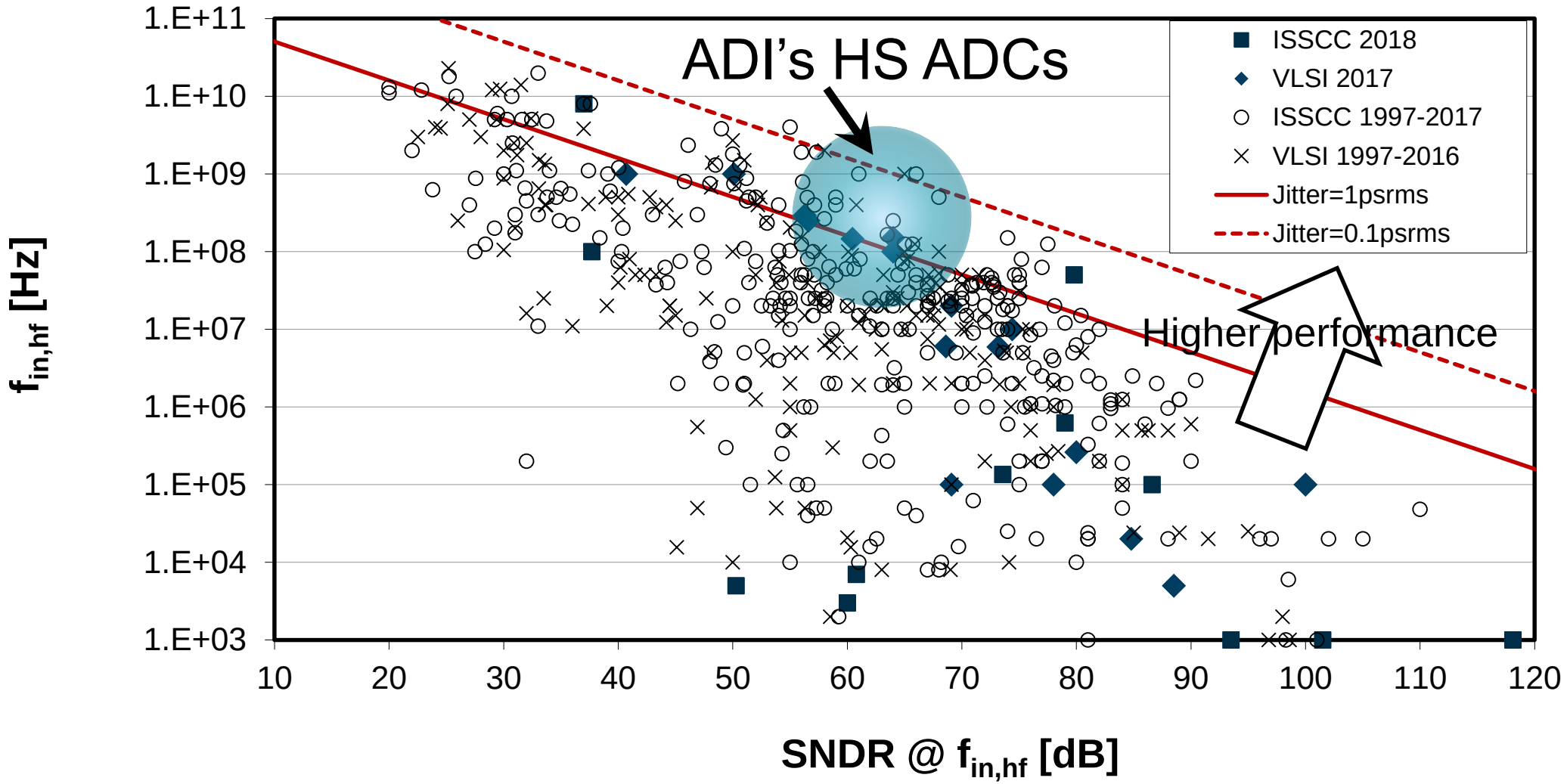




2006 2007 2008 2009 2010 2011 2012 2013 2014 2015 2016 2017 2018 Release to Market

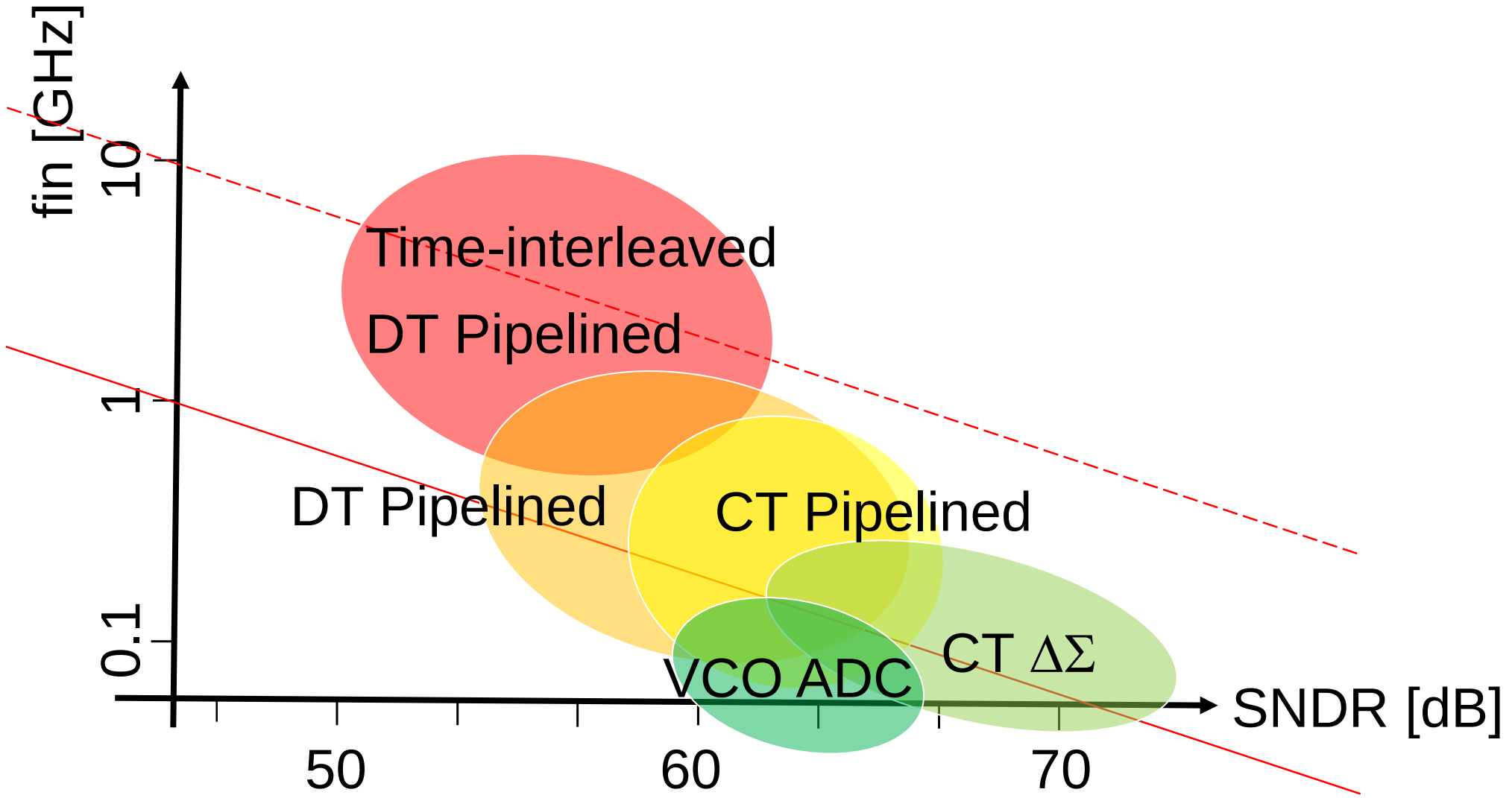
14b/125MSPS	16b/250MSPS	14b/1.25GSPS	14b/3GSPS	12b/10GSPS
0.35u BiCMOS	0.18u BiCMOS	65nm CMOS	28nm CMOS	28nm CMOS
85%A/15%D	80%A/20%D	75%A/25%D	70%A/30%D	60%A/40%D

Architectures (no one fits all): ADC “Aperture plot” (i.e. Bandwidth vs. Dyn Range or sample rate vs. resolution)



Created using data available at https://web.stanford.edu/~murmann/adcsurvey.html (Prof. B. Murmann’s ADC performance survey)

ADI's ADC architectures: one cannot fit all



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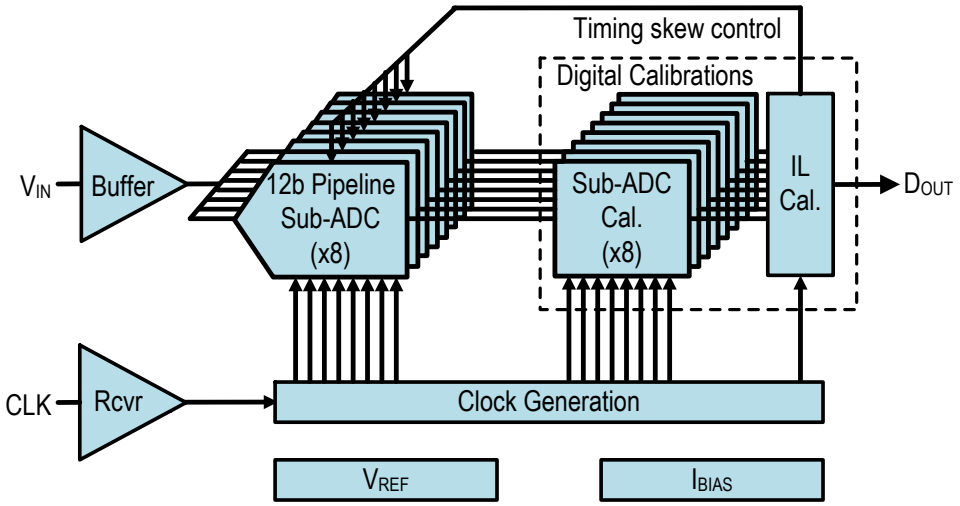
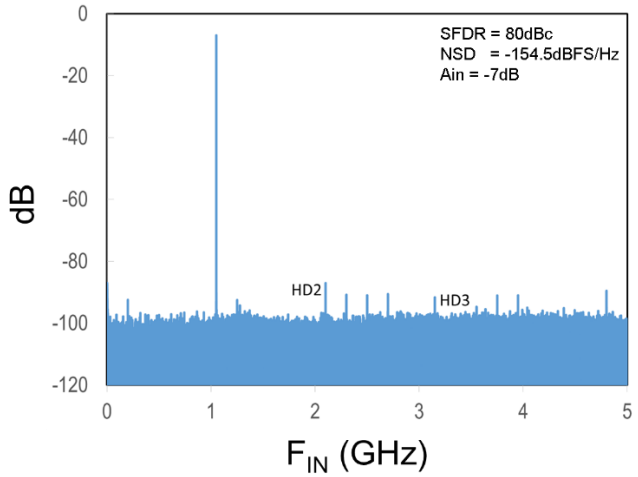
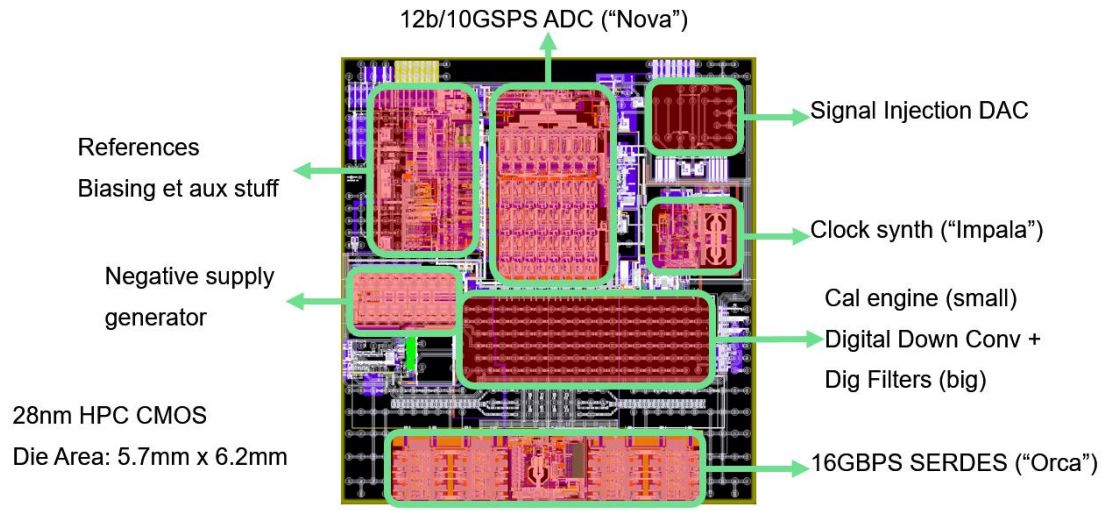
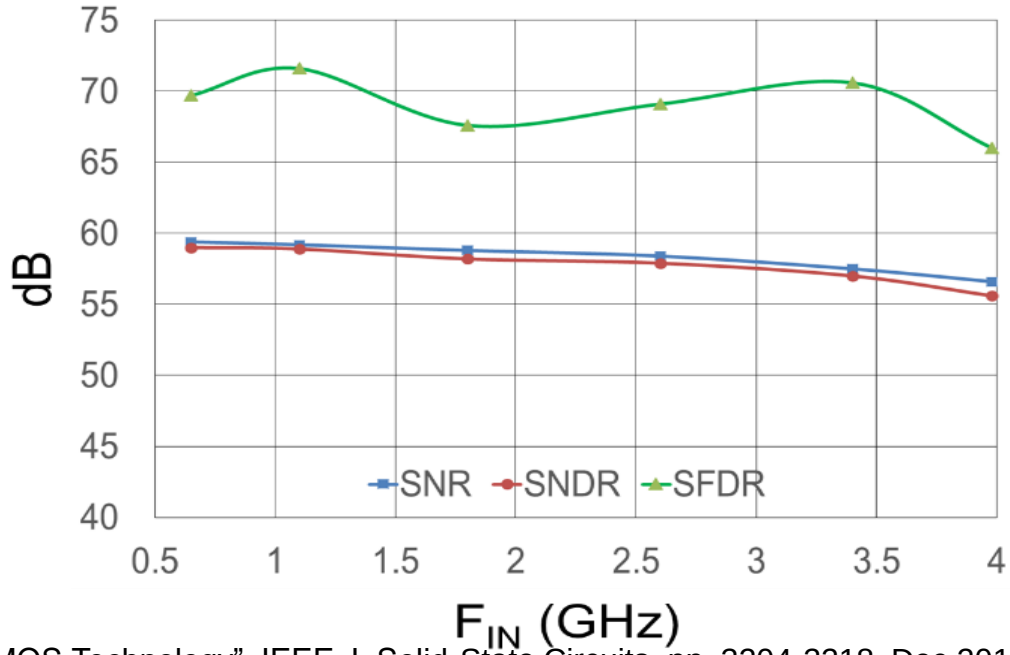
12b/10GSPS ADC: 8x interleaved Analog to Digital converter



Resolution	12b
F_{SAMPLE}	10GS/s
SNR	56dB
SNDR	55dB
SFDR	66dB
Input fin	4GHz
Power	2.9W
FOMS_HF	147dB
BW	7.4GHz
DR	60dB
$NSD_{small-signal}$	-157dBFS/Hz
Technology	28nm

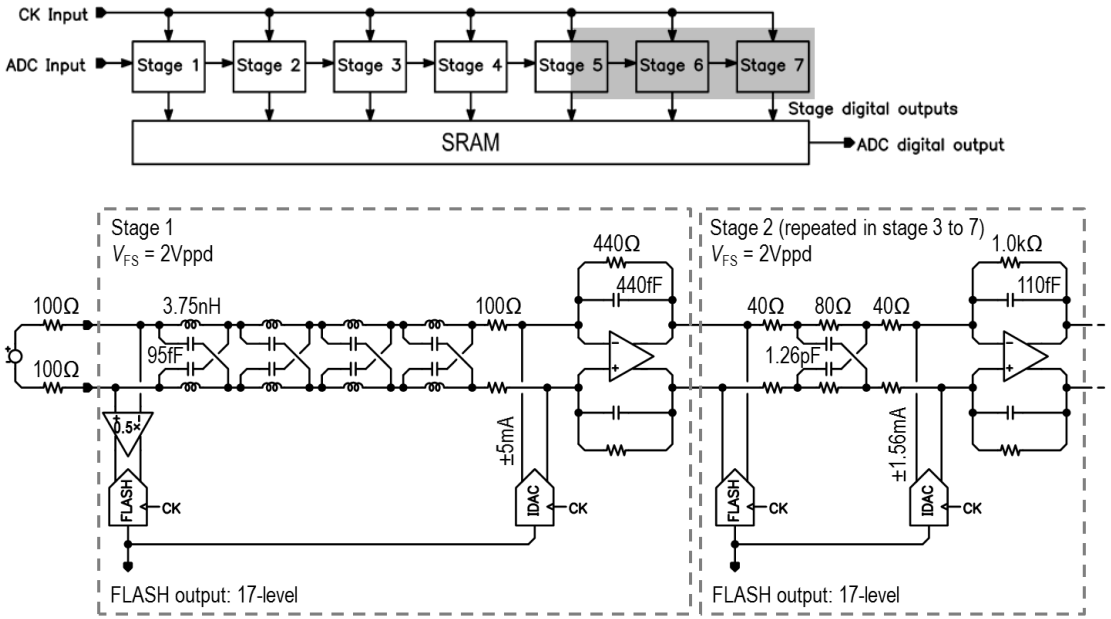


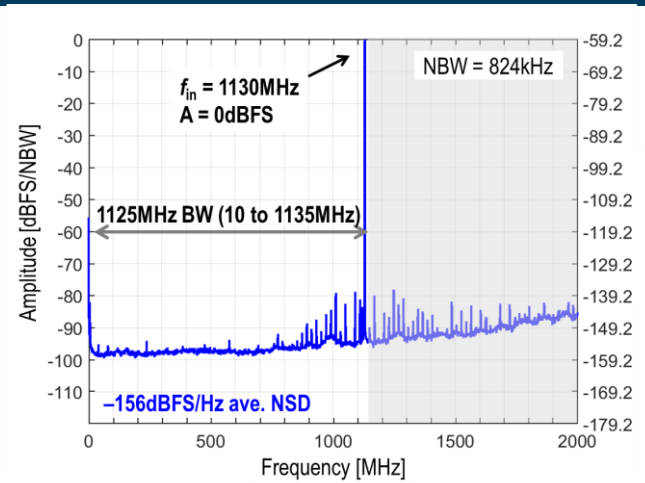


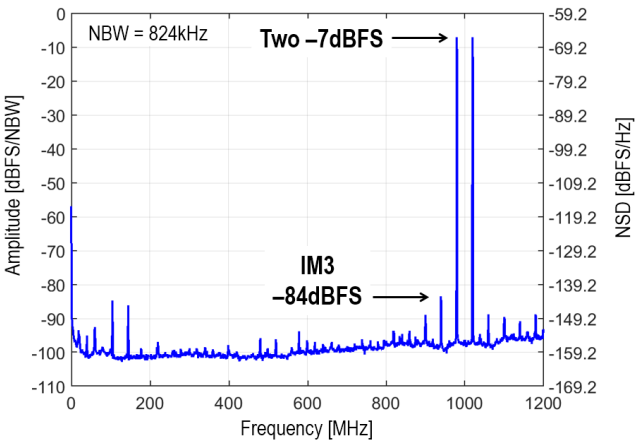


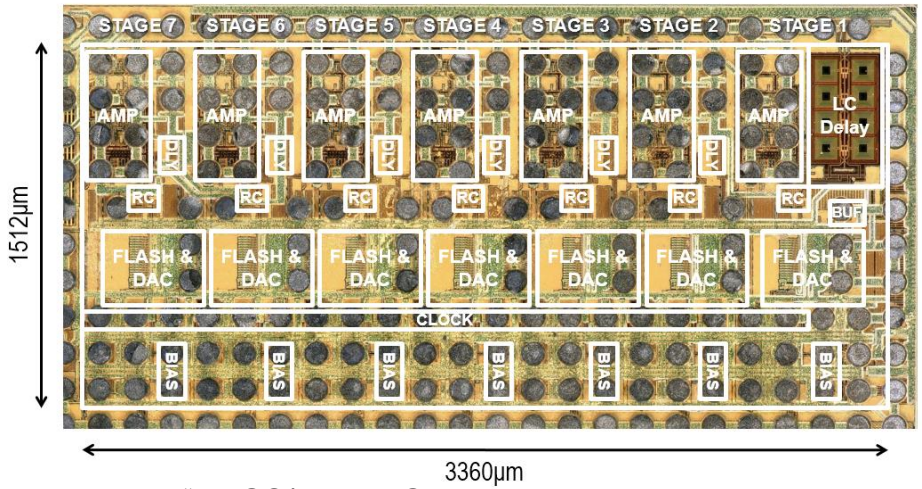
S. Devarajan, et al., “A 12b 10GS/s Interleaved Pipeline ADC in 28nm CMOS Technology”, IEEE J. Solid-State Circuits, pp. 3204-3218, Dec 2017

CT pipelined ADCs

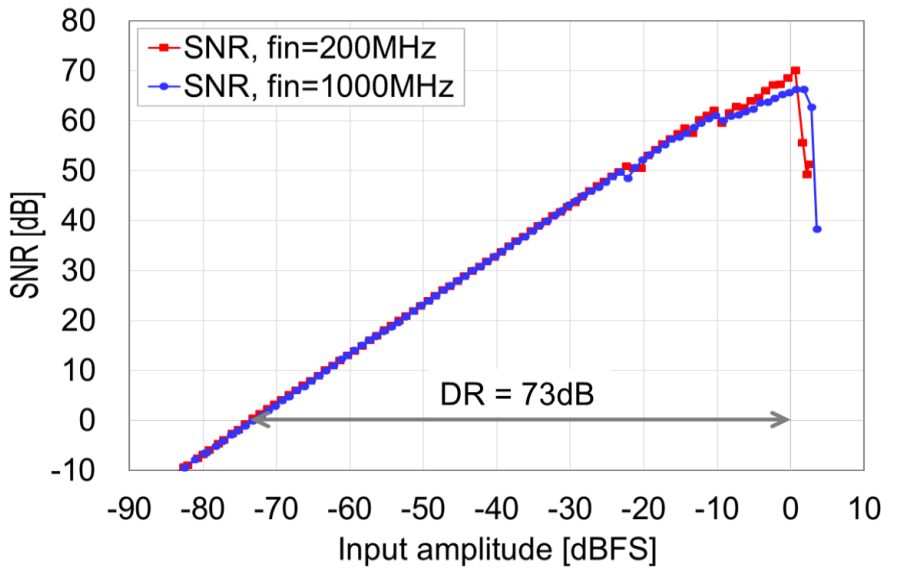








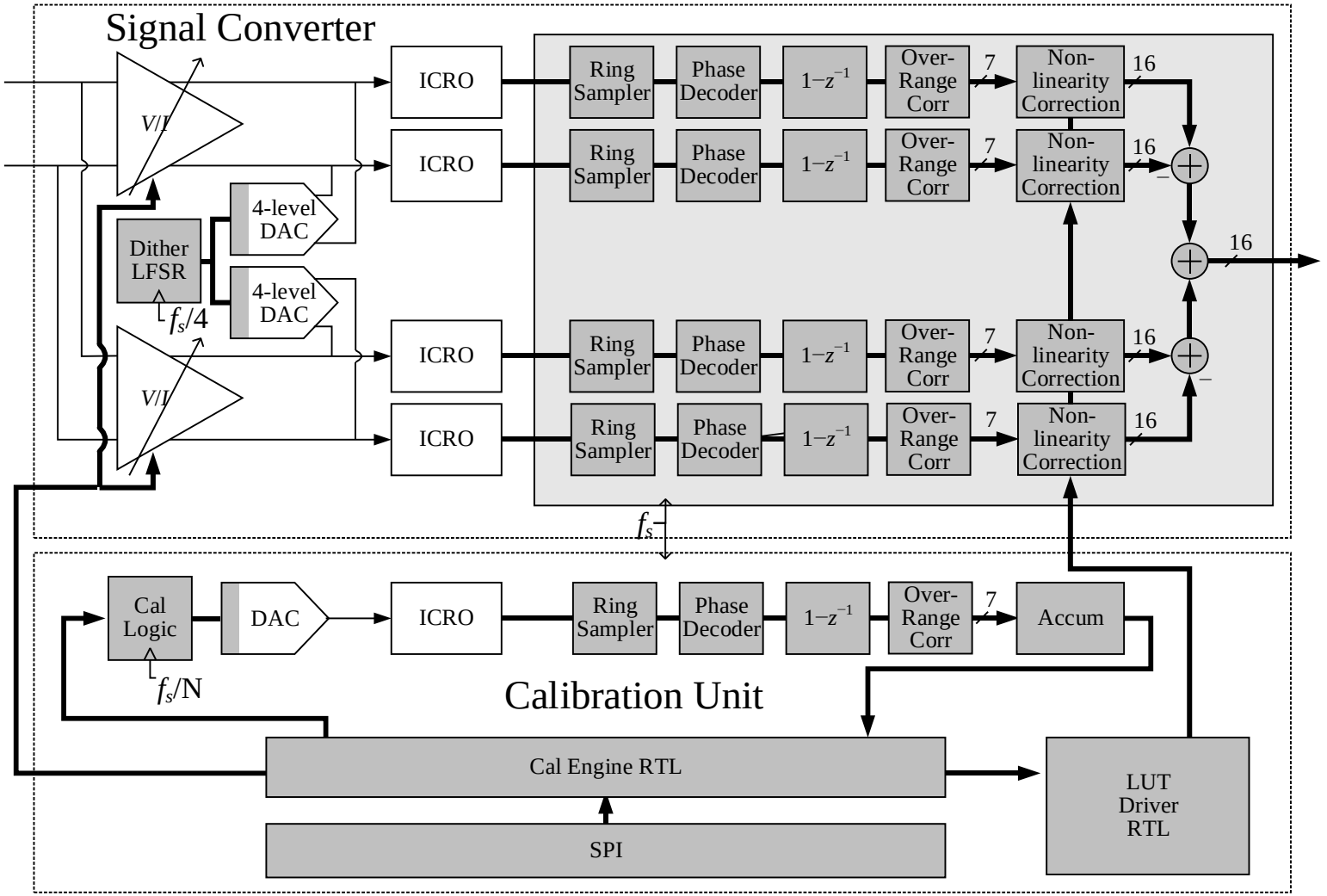
	This work
Architecture	CT pipeline
Inherent Anti-aliasing	Yes
Process Technology	28nm CMOS
f_S [GHz]	9
Raw BW = f_S / (2 OSR) [MHz]	1125
App BW = f_S / (2 App OSR) [MHz]	1125
App OSR	4.0
Small-signal NSD = DR + 10 log10(BW) [dBFS/Hz]	–164
Large-signal NSD (low f) = SNR + 10 log10(BW) [dBFS/Hz]	–160
Large-signal NSD (high f) = SNR + 10 log10(BW) [dBFS/Hz]	–156
IM3 [dBFS]	–84
HD2 [dBFS]	–79
HD3 [dBFS]	–86
SFDR [dB]	73
Area [mm^2]	5.1
Power [mW]	2330
FOM_S = DR+10log$_{10}$(BW/P) [dB]	160



H. Shibata, et al., “A 9GS/s 1.125GHz BW oversampling continuous-time pipeline ADC achieving -164 dBFS/Hz NSD”, IEEE J. Solid-State Circuits, pp. 3219-3234, Dec 2017

VCOADC

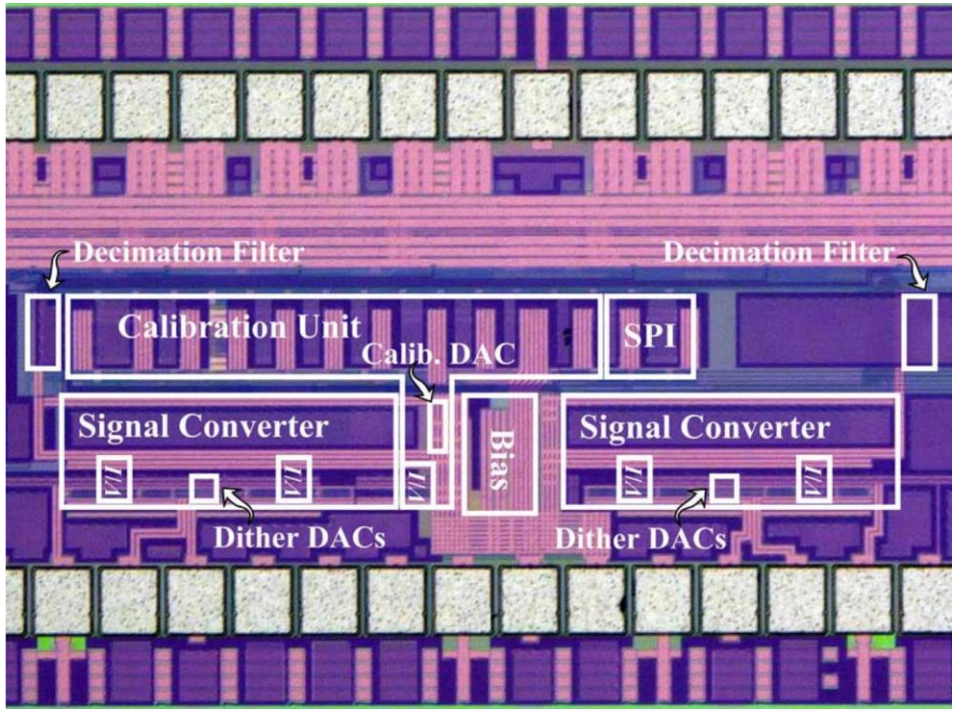
- Variable gain V/I
- Reconfigurable
  - f_s =1.1-2.2Gsps
  - BW=10-20-50MHz
  - NSD=-147 to -154dBFS
  - Power=7-30mW/adc
- SFDR > 85dBc
- Calibration:
  - Background calibration of replica ADC signal path.
  - All calibration engine logic included with ADC IP, no uController required
  - Continuous calibration or on-demand
  - Calibration period=15-30uS
- Manual layout for high-speed signal path, P&R for calibration engine only



G. Taylor and I. Galton, “A mostly digital variable rate continuous-time delta-sigma modulator ADC”, IEEE J. Solid-State Circuits, pp.2634-2646, Dec 2010

Why VCOADC?

- Area is 5-10x smaller than other ADCs with similar specs
- CT front end-> drive-able
- Mostly digital->Scalable



G. Taylor and I. Galton, “A mostly digital variable rate continuous-time delta-sigma modulator ADC”, IEEE J. Solid-State Circuits, pp.2634-2646, Dec 2010

ANALOG DEVICES

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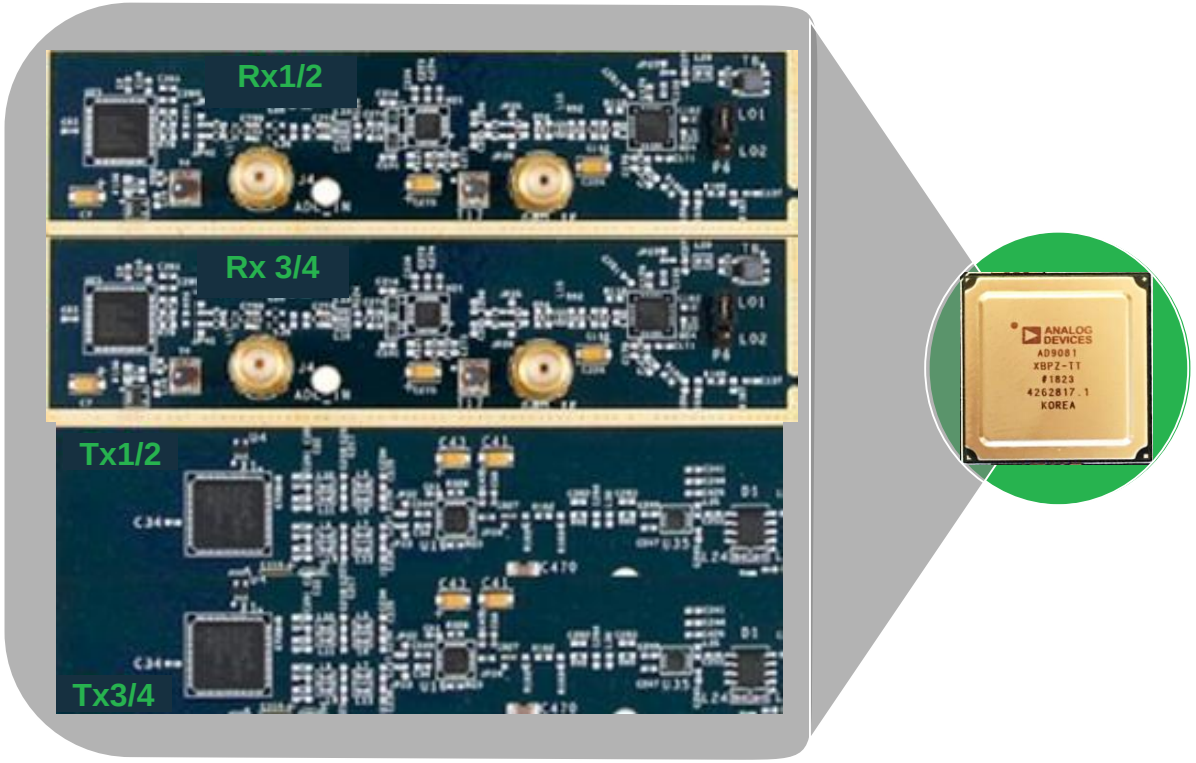
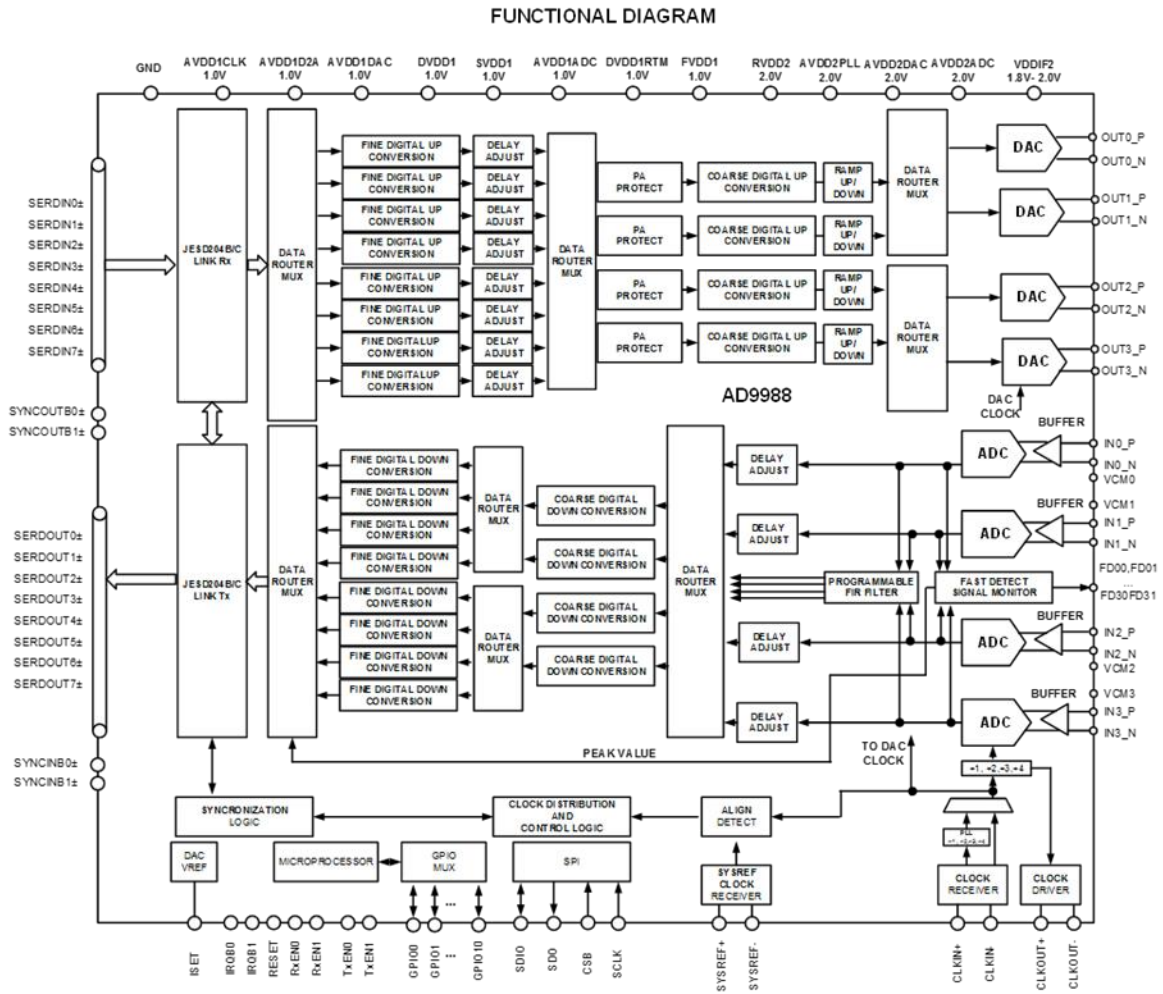
Integrated Systems: SoCs/SiPs with Mixed-Signal + Embedded DSP Capability

quad Tx / quad-dual Rx fully integrated wideband MxFE





ANALOG DEVICES
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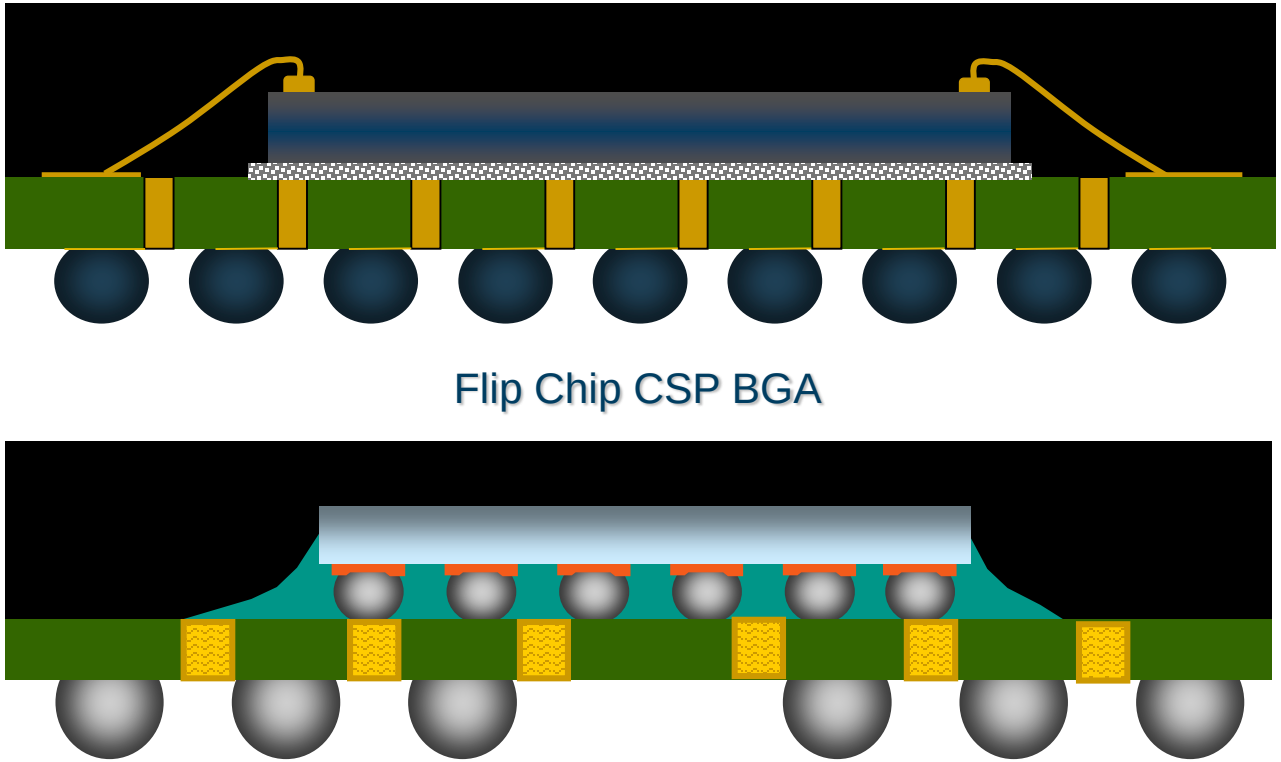
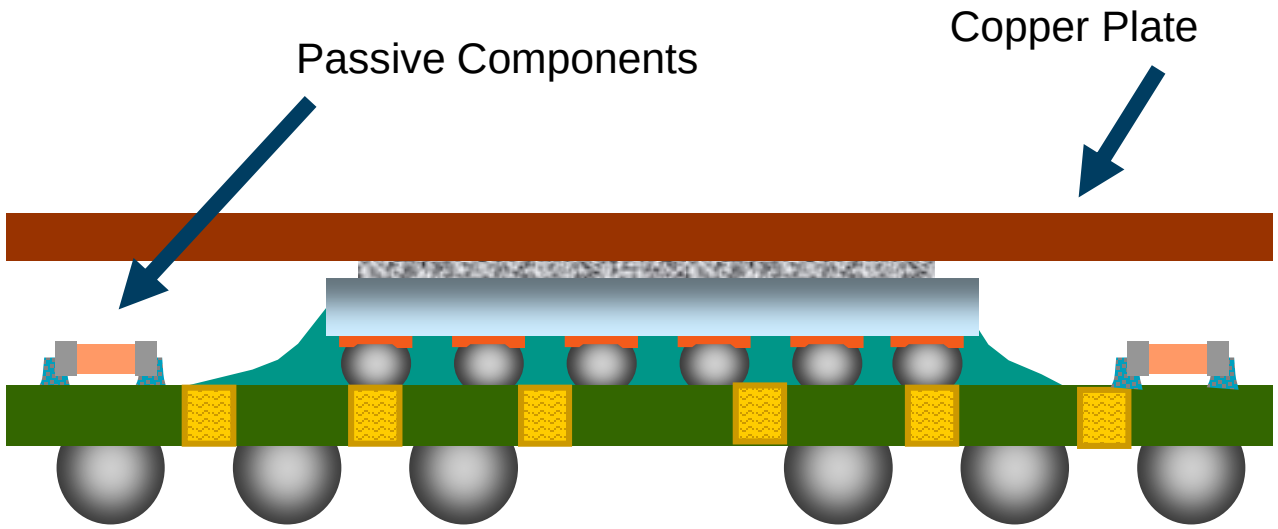
Flip Chip Chip Scale Package BGA

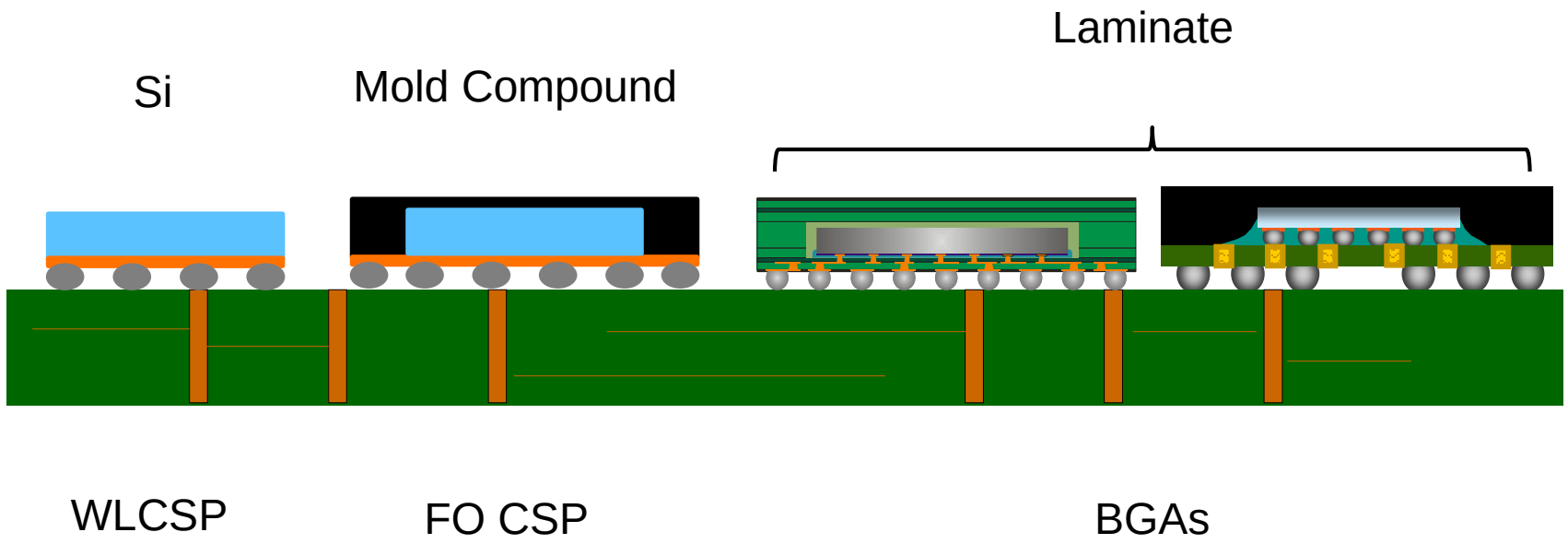


Flip Chip CSP BGA

Flip Chip – Thermally Enhanced BGA

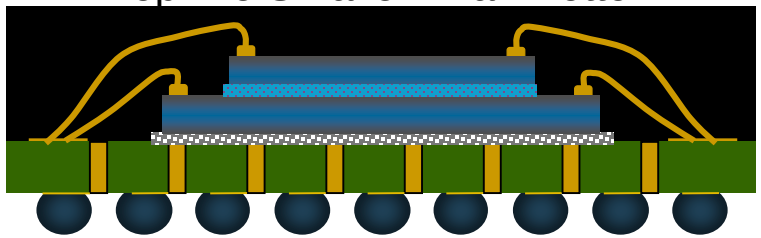


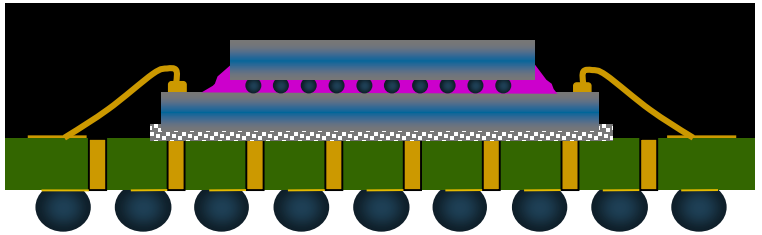
Higher frequency performance



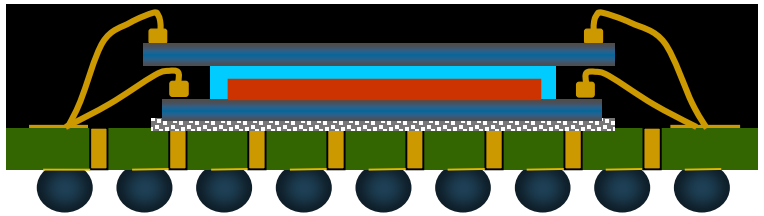
3D Packaging

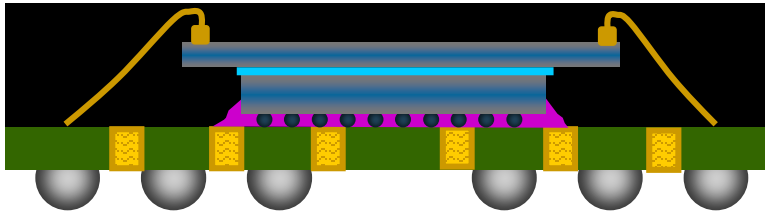
“Pyramid”
Top Die Smaller Than Bottom





Top Die Same Size or Larger
Than Bottom

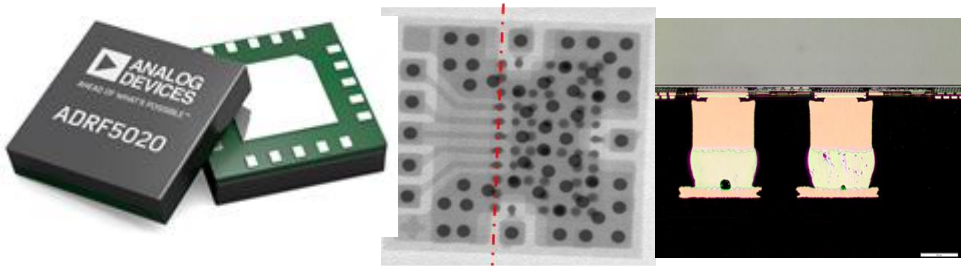




Wirebond Versions

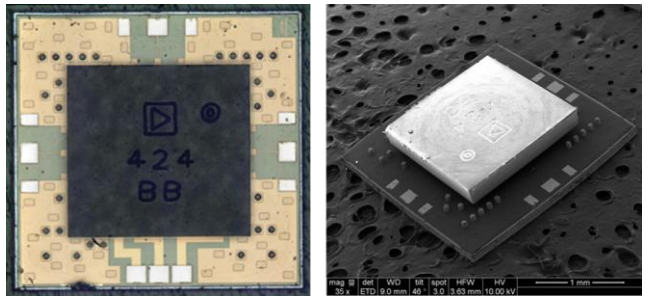
Bumped Die Flip Chip Versions

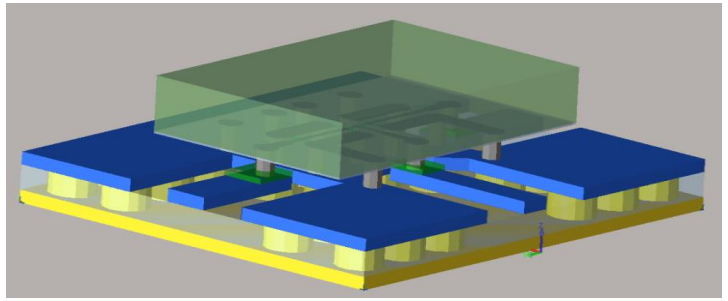
mmWave front-end modules



FlipChip on Laminate (LGA)

Die-On-Carrier (DOC)
“Die-like” RF Product





Bumped Flip Chip (SMT Assembly)

ANALOG DEVICES
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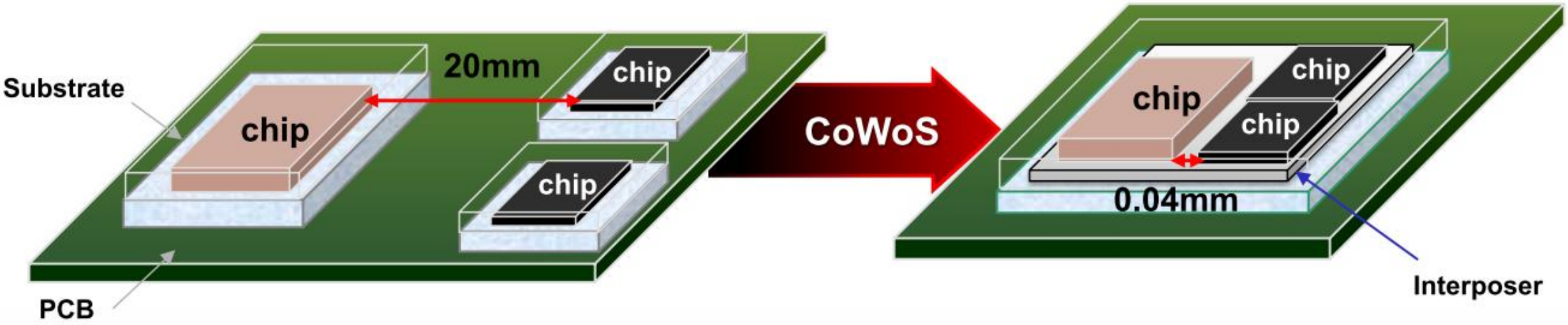
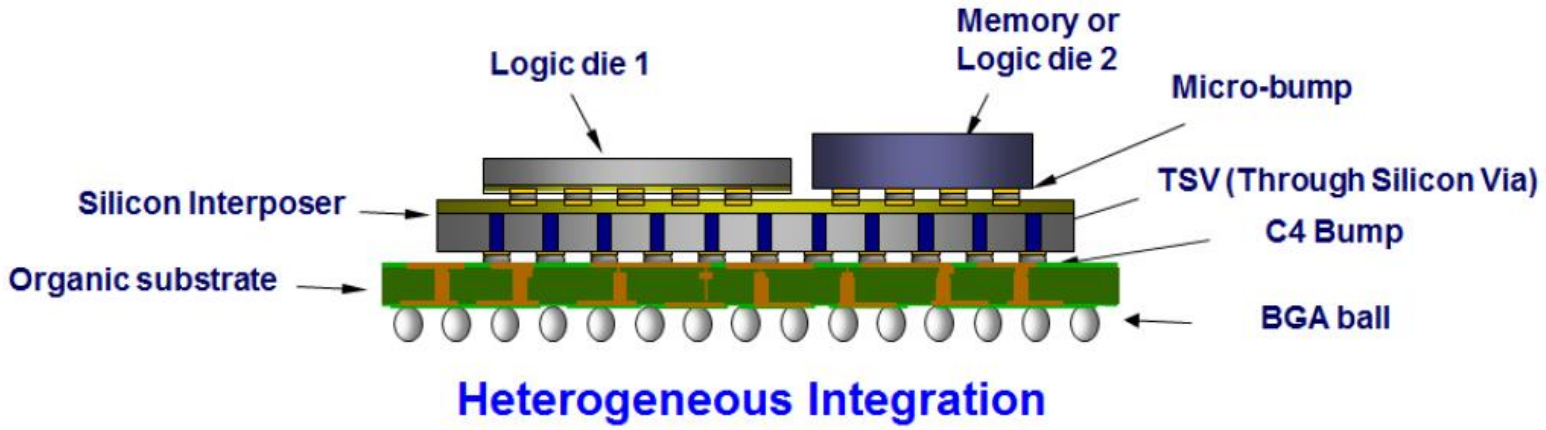
Interposer Systems in a Package





TSMC's CoWoS® (Chip-on-Wafer-on-Substrate) Services, https://www.tsmc.com/english/dedicatedFoundry/services/cowos.htm

P. Gupta and S. S. Iyer, "Goodbye, Motherboard. Hello, Silicon-Interconnect Fabric", IEEE Spectrum, Sept 2019

ANALOG DEVICES

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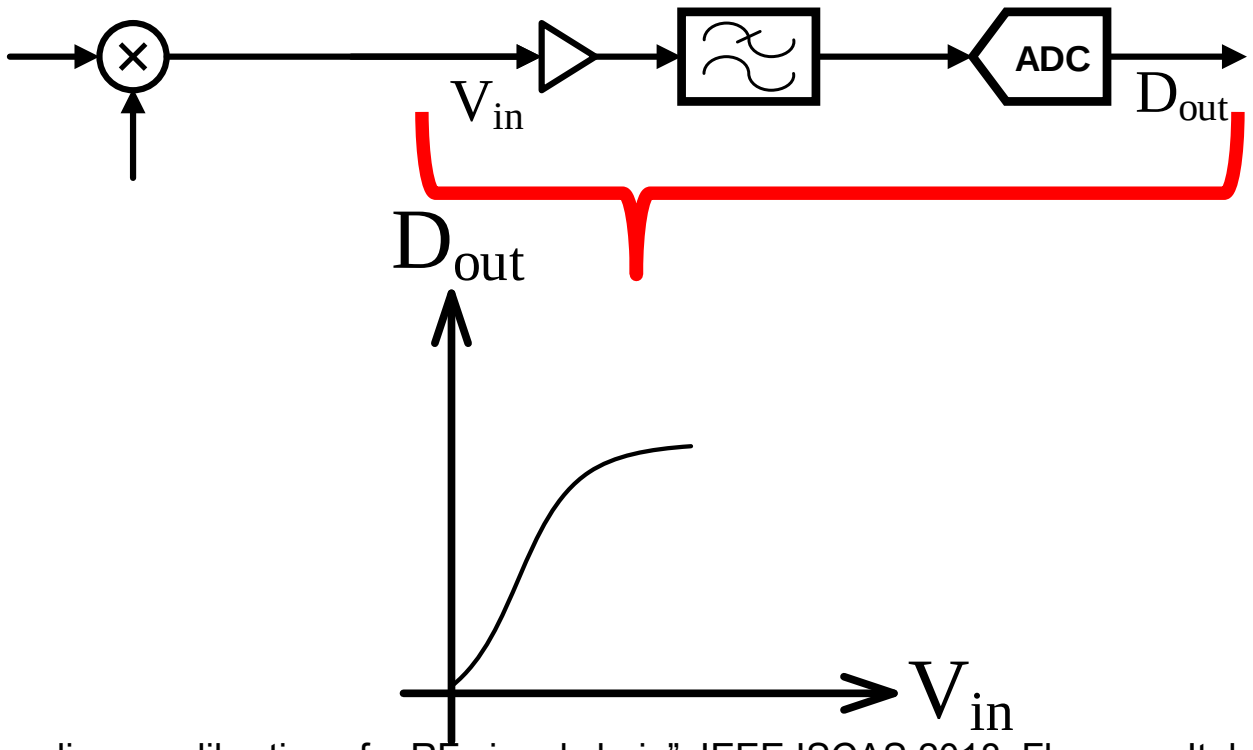
Algorithmic Capability: System-level Linearization

Non-linear Correction for Rx Signal Chain



N. Rakuljic et al., “In-situ nonlinear calibration of a RF signal chain”, IEEE ISCAS 2018, Florence, Italy, 2018

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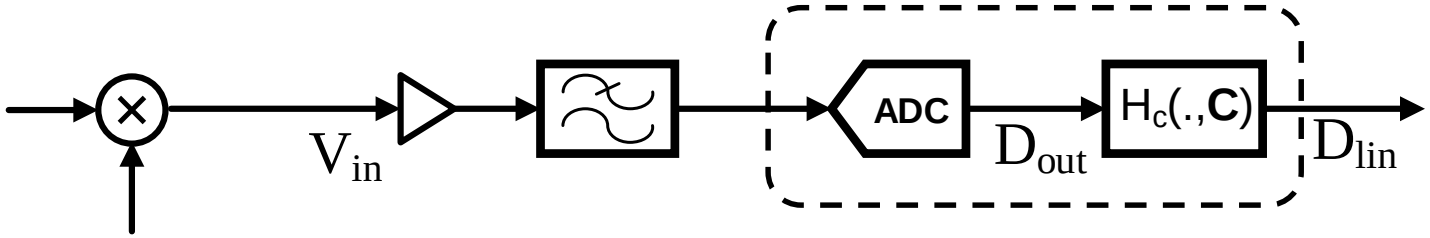
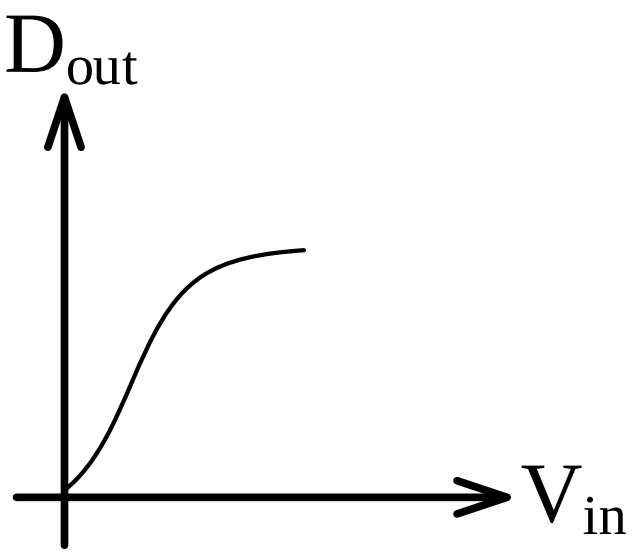
Non-linear Correction for Rx Signal Chain





ANALOG DEVICES
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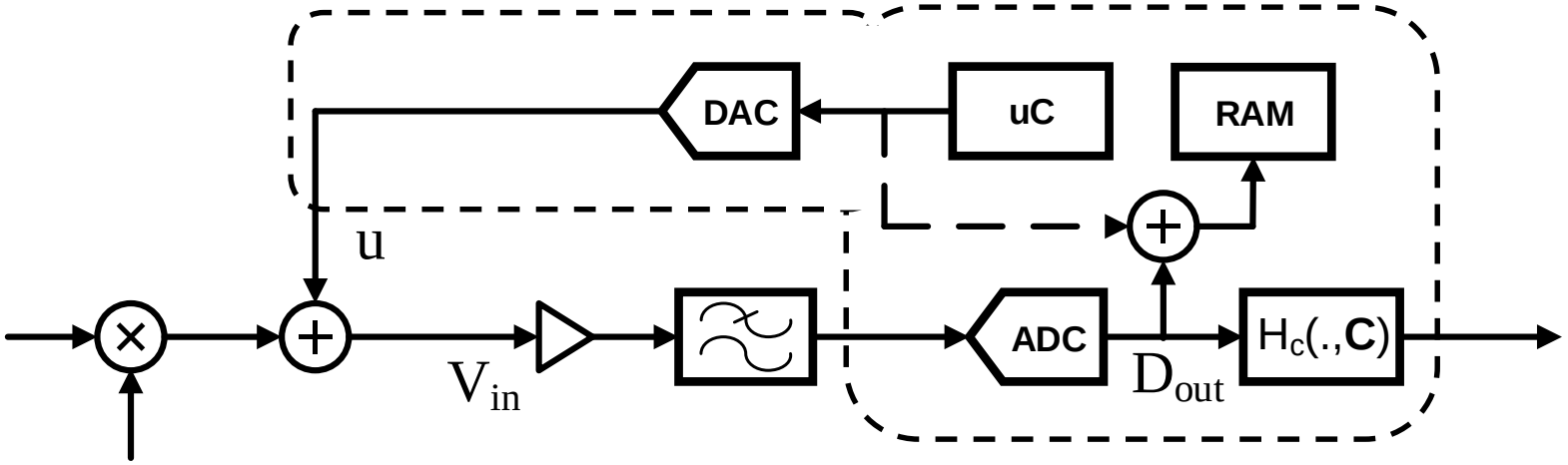
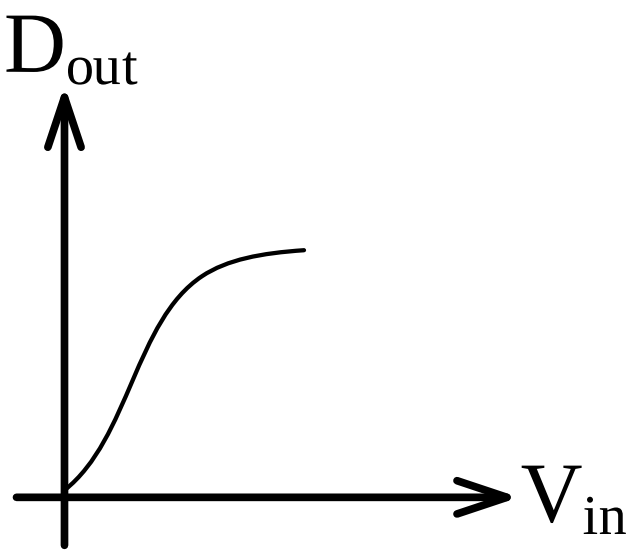
Non-linear Correction for Rx Signal Chain





ANALOG DEVICES
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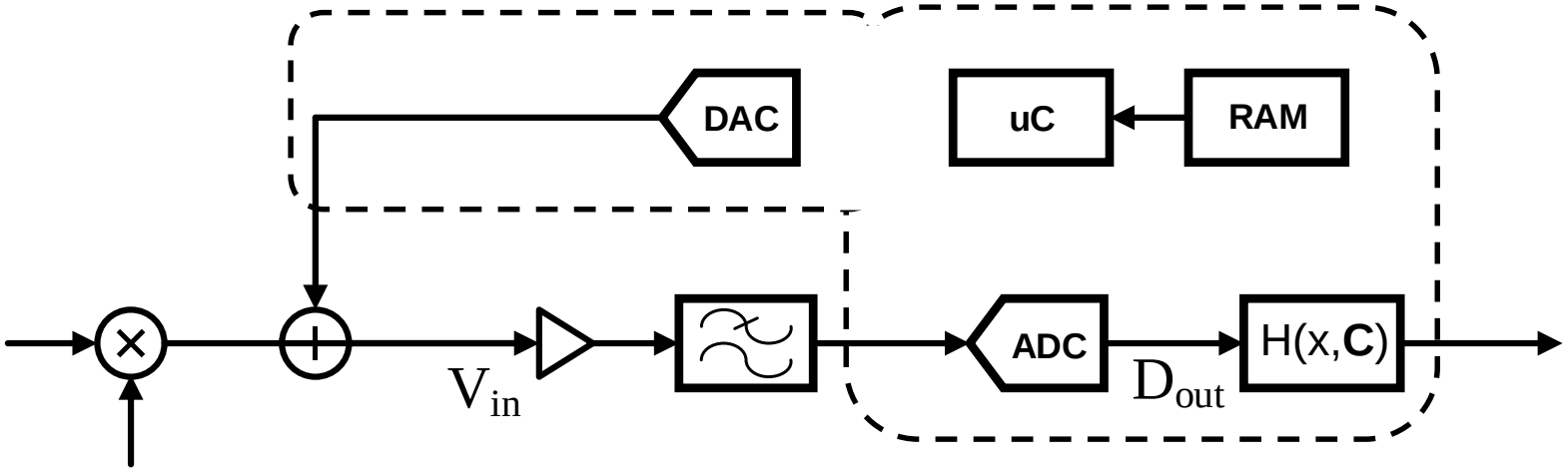
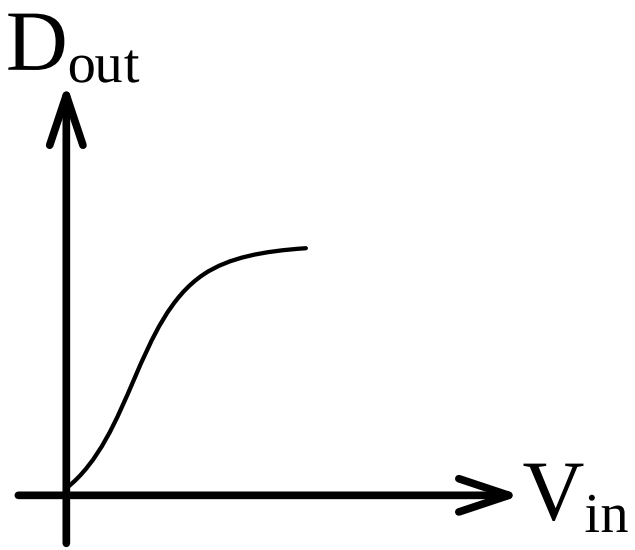
Non-linear Correction for Rx Signal Chain





ANALOG DEVICES
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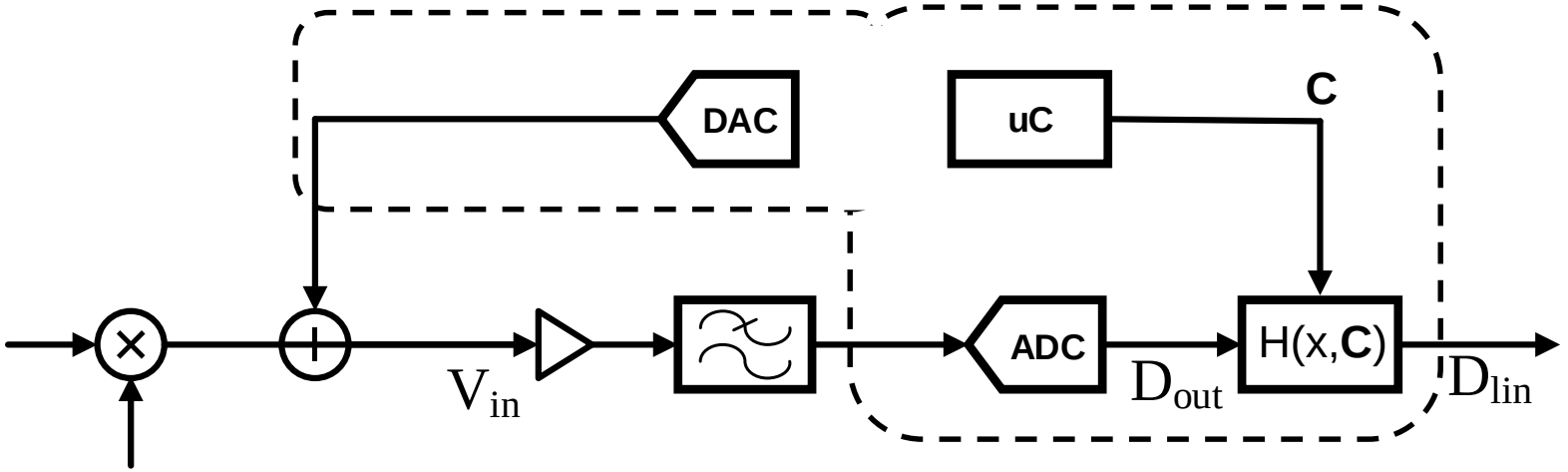
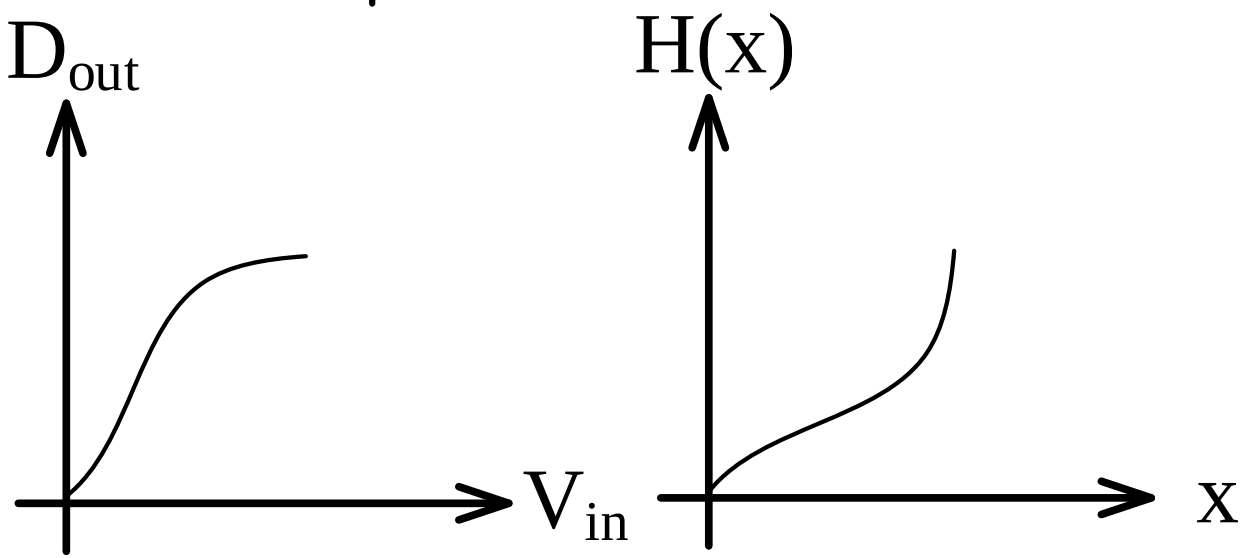
Non-linear Correction for Rx Signal Chain





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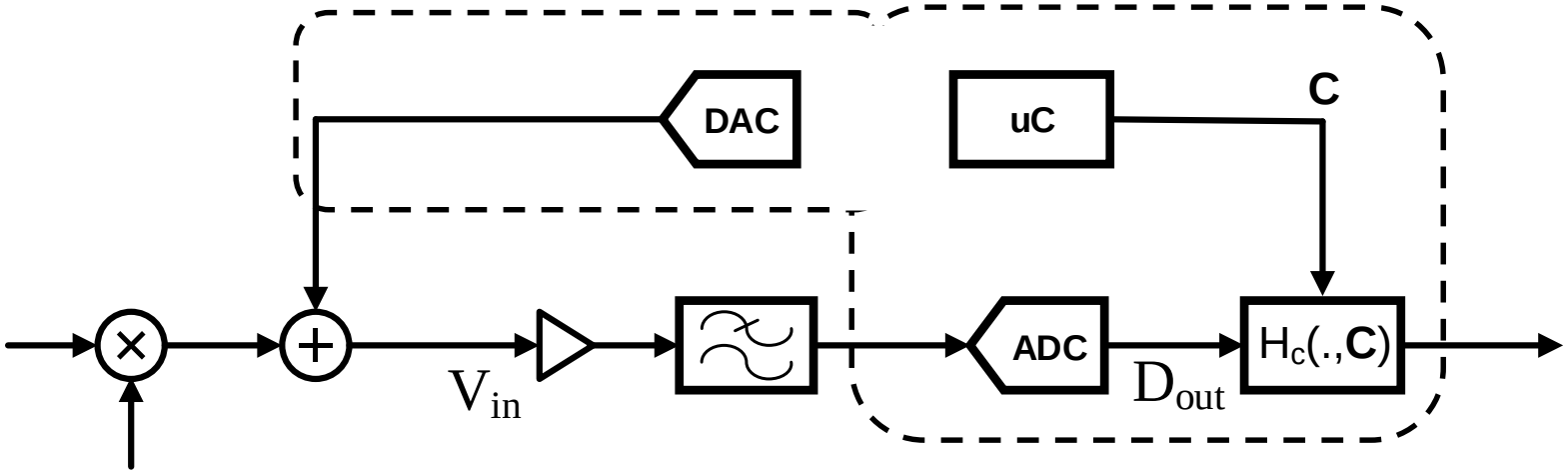
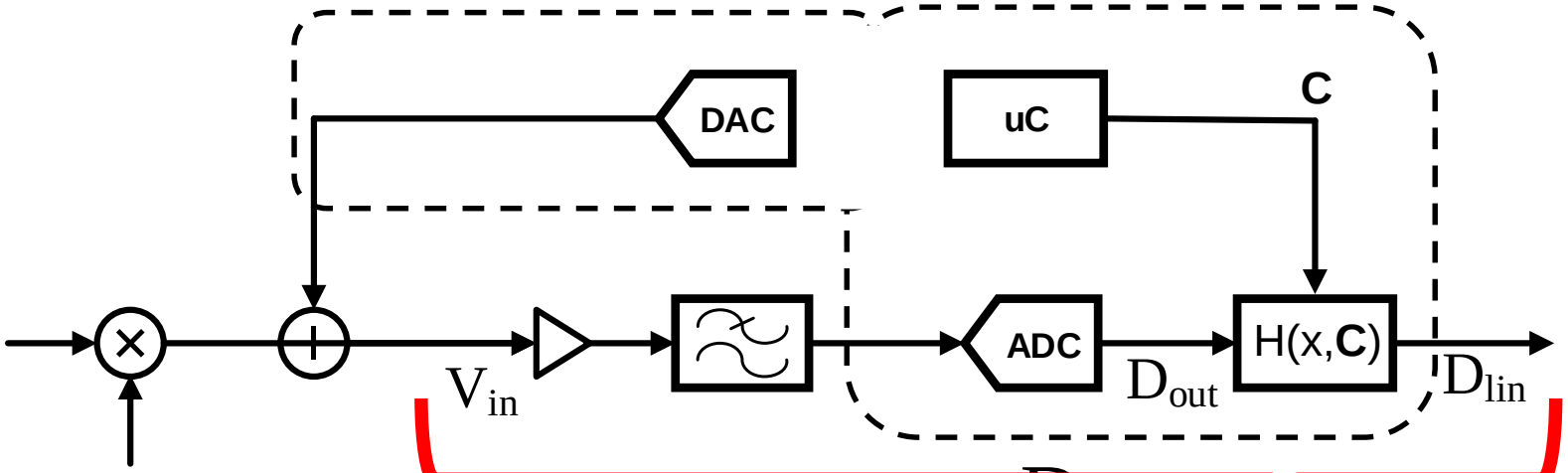
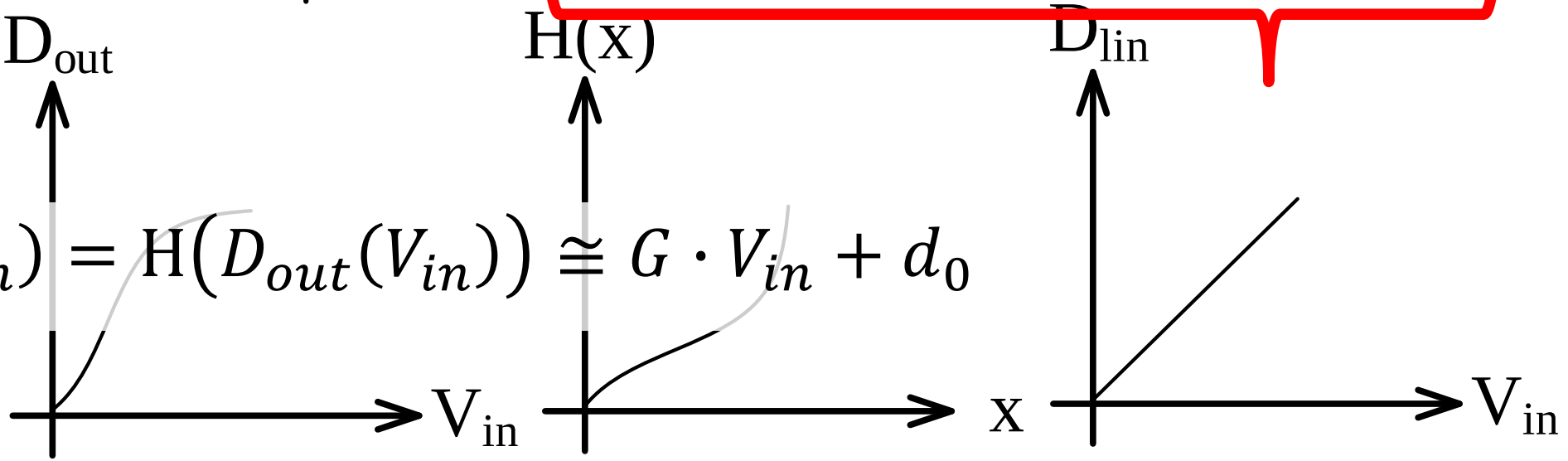
Non-linear Correction for Rx Signal Chain



Non-linear Correction for Rx Signal Chain



$$D_{lin}(V_{in}) = \mathrm{H}\left(D_{out}(V_{in})\right) \cong G \cdot V_{in} + d_0$$



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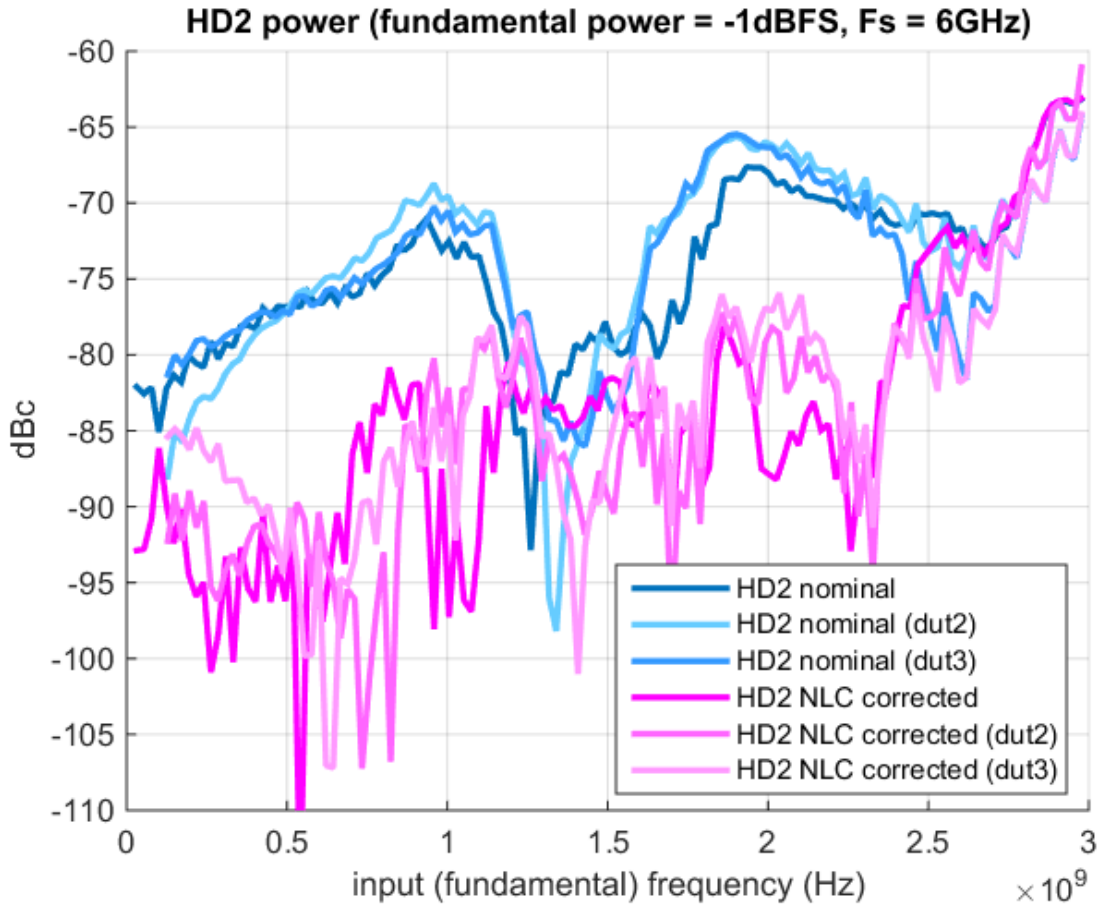
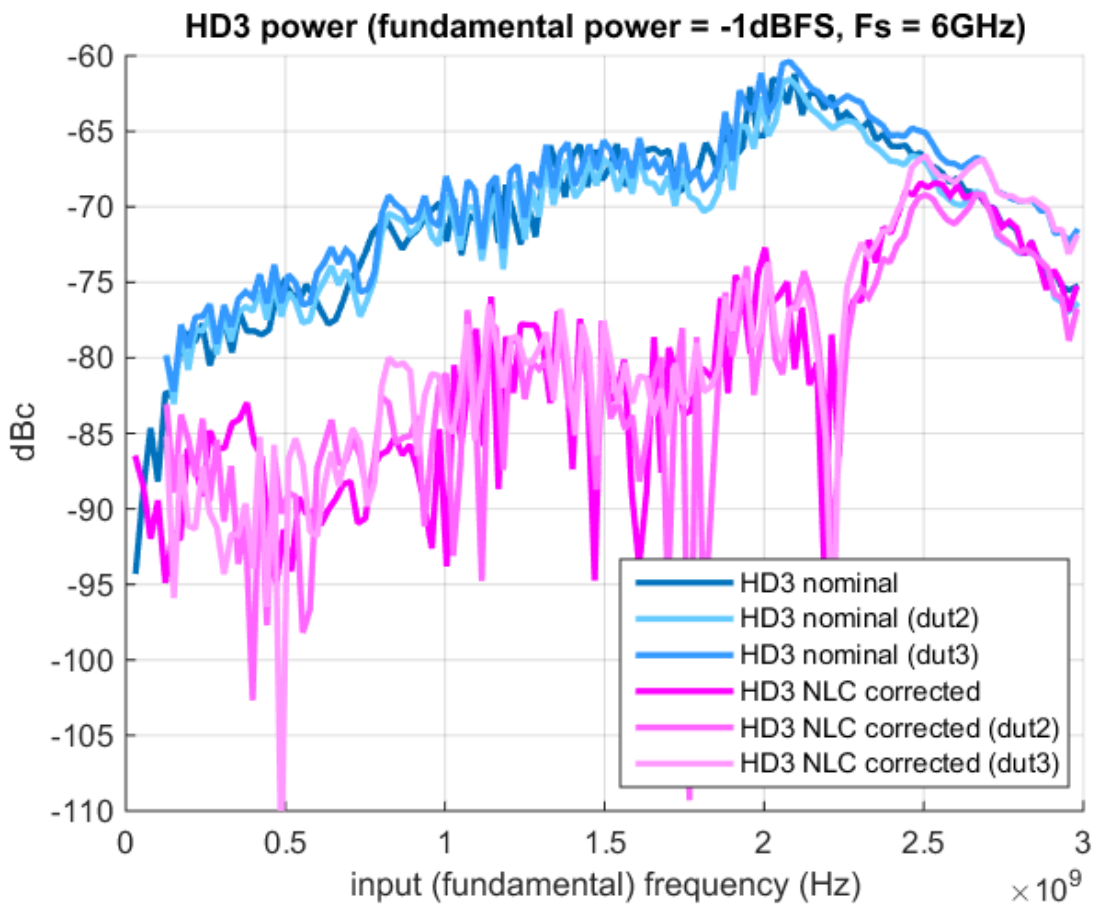
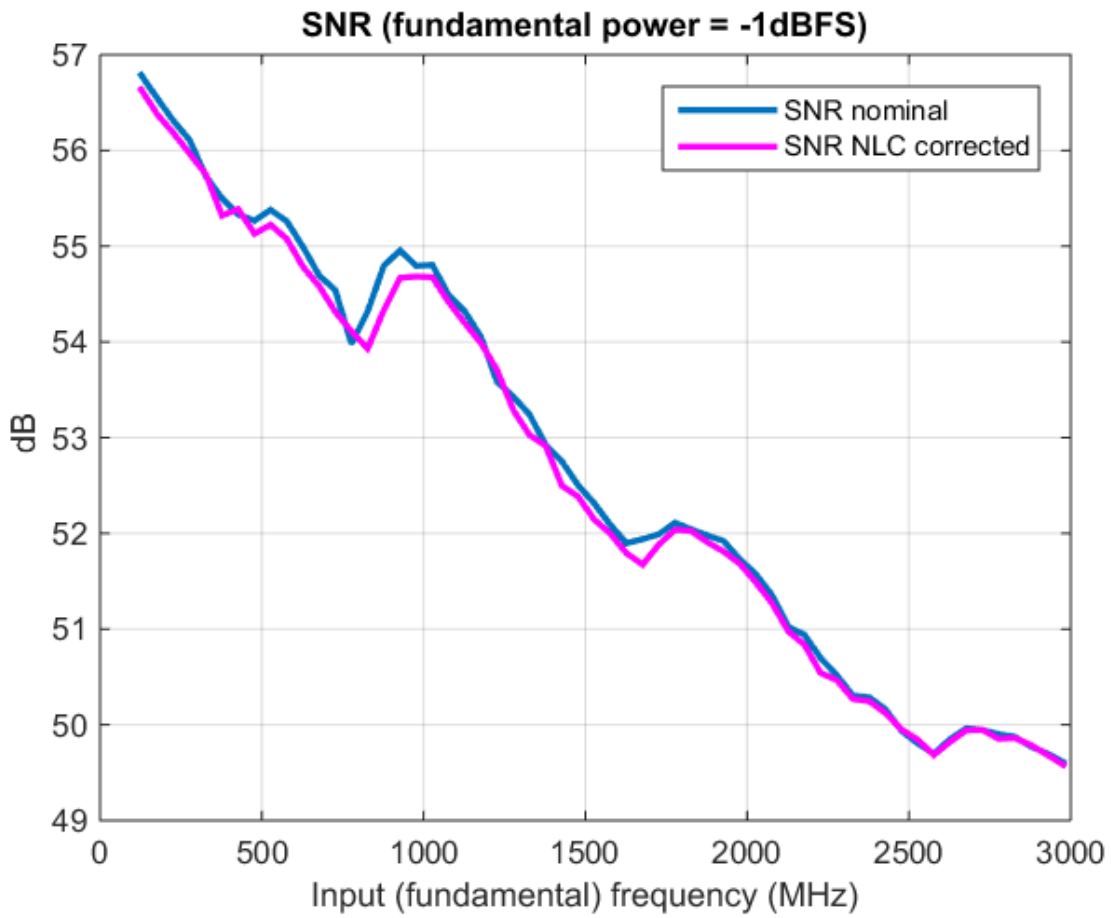
Fs=6GSPS Lab Data: HD2 & HD3 correction

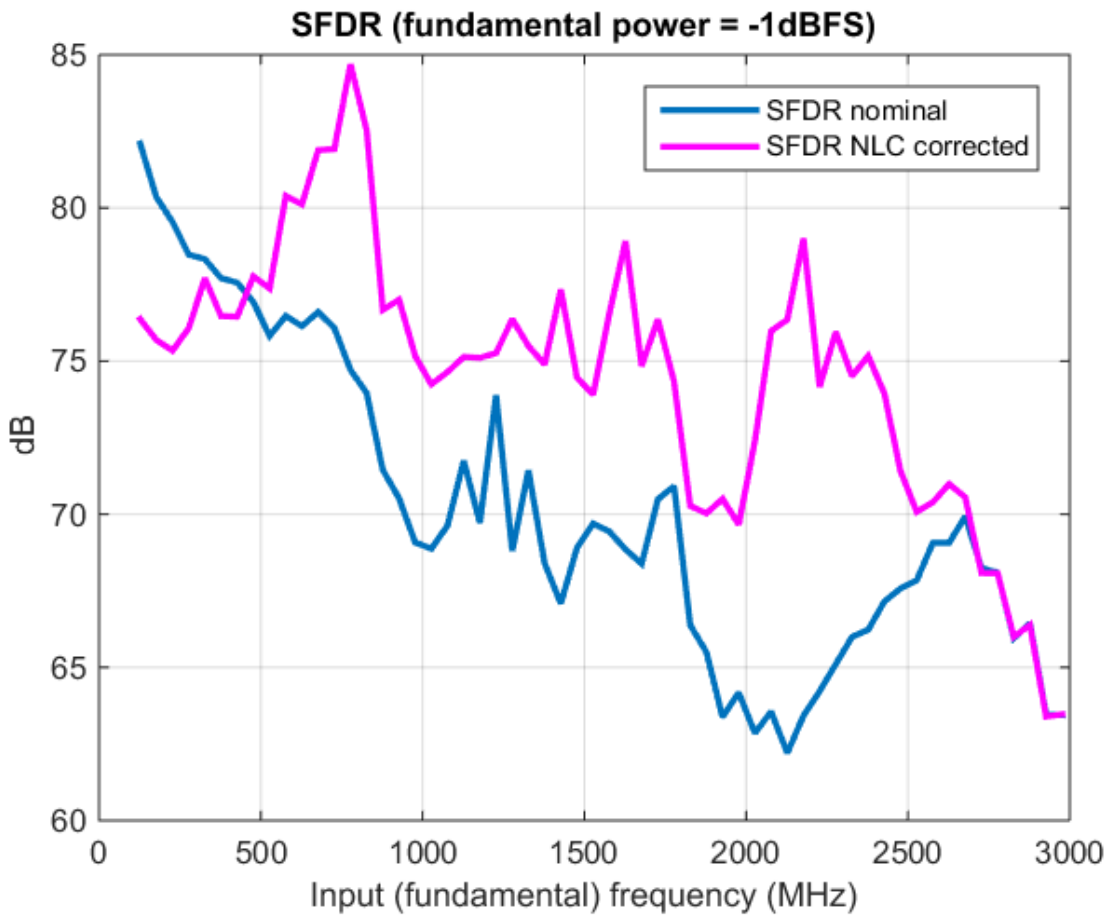




N. Rakuljic et al., “In-situ nonlinear calibration of a RF signal chain”, IEEE ISCAS 2018, Florence, Italy, 2018

Fs=6GSPS Lab Data: SNR and SFDR

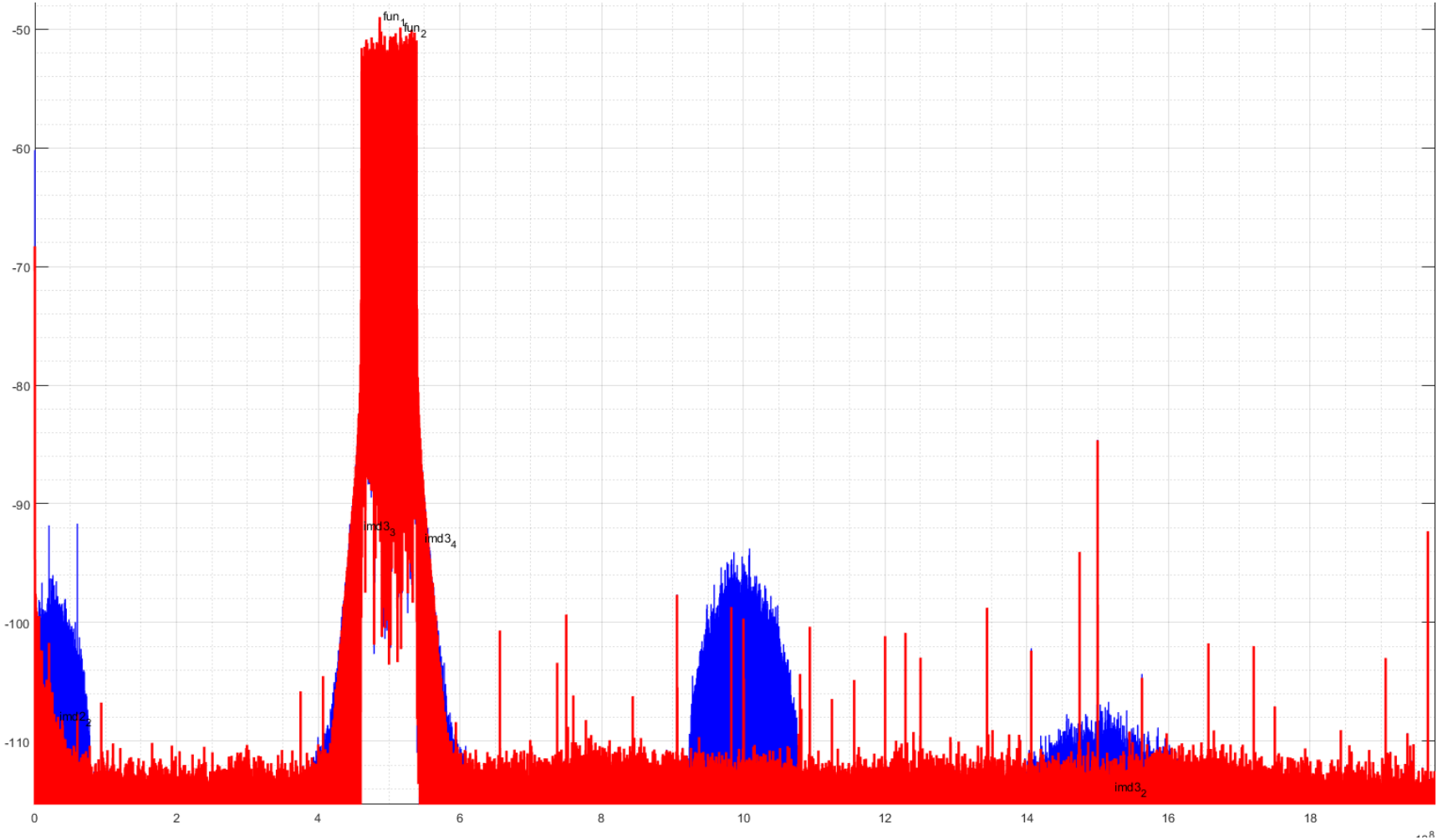




N. Rakuljic et al., “In-situ nonlinear calibration of a RF signal chain”, IEEE ISCAS 2018, Florence, Italy, 2018

Wi-Fi 6 (802.11AX) Test Signal (500M)

- Test signal shown at right
- Before LinearX™ correction in blue
- After LinearX™ correction in red (tonal spurs are common to both)
- Training was done using a different wideband training signal spanning 400 – 600M



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Conclusion

Conclusion

A comprehensive approach is required to address the multiple important design constraints:

- Heat removal
- Devices' reliability and aging
- Process technology
- Packaging
- Data interfaces
- Performance/band/power consumption
- Area/costs

QUESTIONS!?