Integrated True-Time-Delay based Large-Scale Arrays for Spatially Diverse Applications

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Oct 18, 2019

Outline

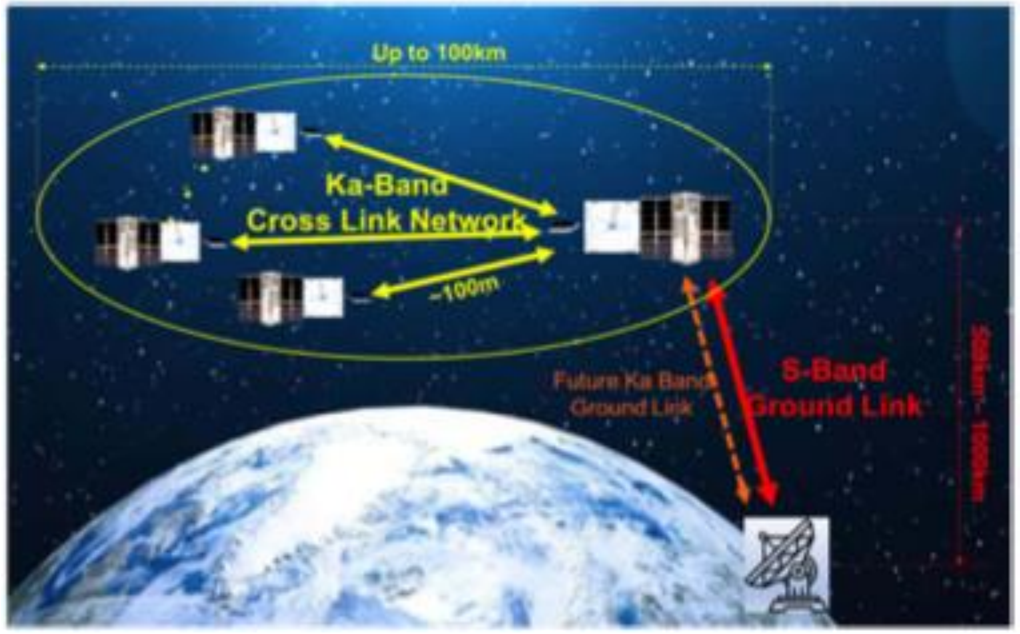
- Motivation
- Background
- Proposed Discrete-Time Delay-Compensation
  - ☐ True-time-delay beamforming for wide modulated BW and large arrays
  - ☐ Spatial interference cancellation with wideband NULL
- Conclusions

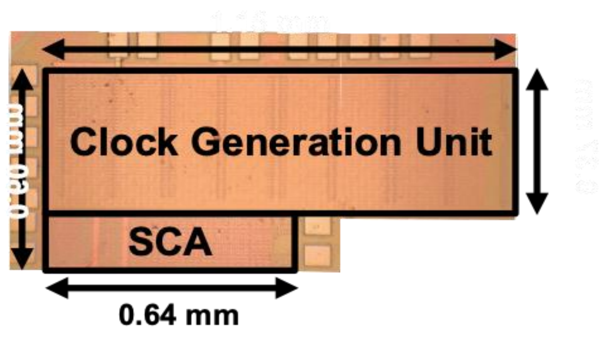
Motivation

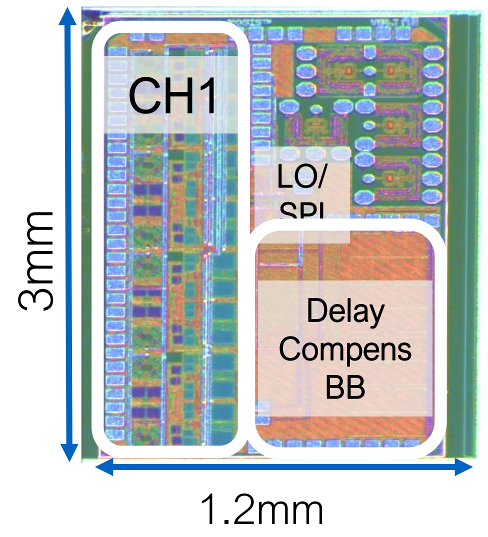
Communications

Key challenges

- Network of CubeSat crosslinks
- Swarm-to-ground communication
- Network Scaling
- Local ranging up to 100 km
- Low-power edge computing





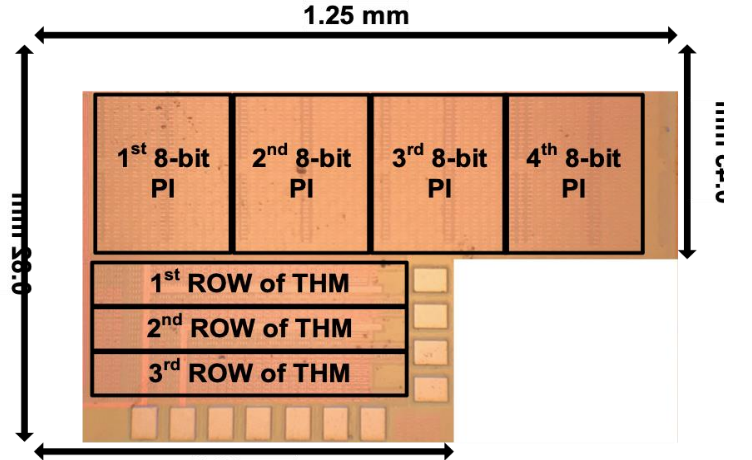


True-time-Delay Beamforming

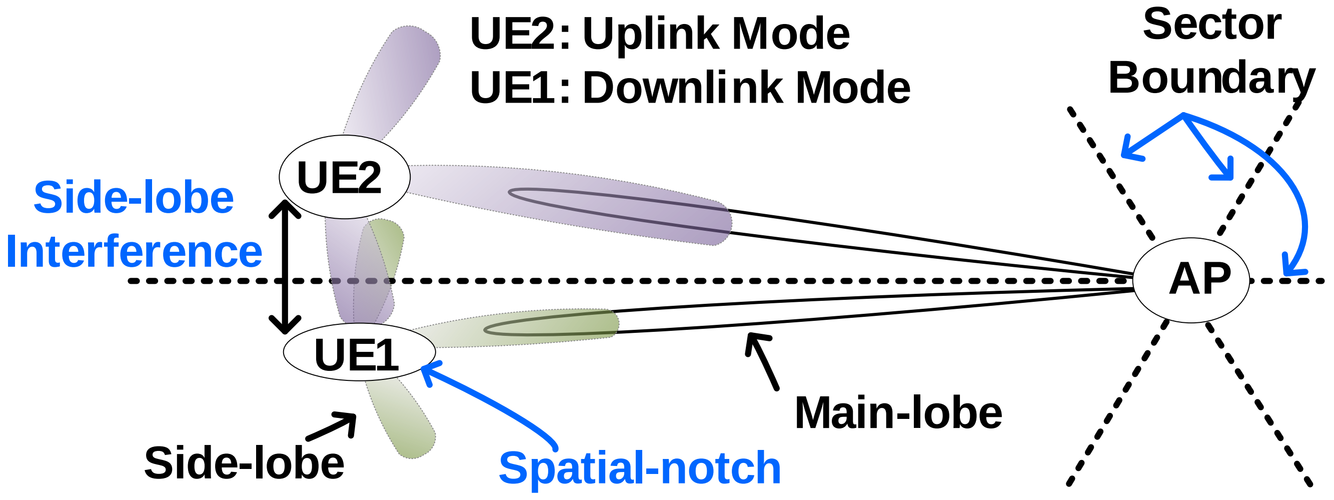
- mmWave links among CubeSats
  - True-time-delay beamforming (ongoing)
  - Single/multiple spatial interference cancellation → near-far problem
  - Closed-loop DoA estimation (ongoing)

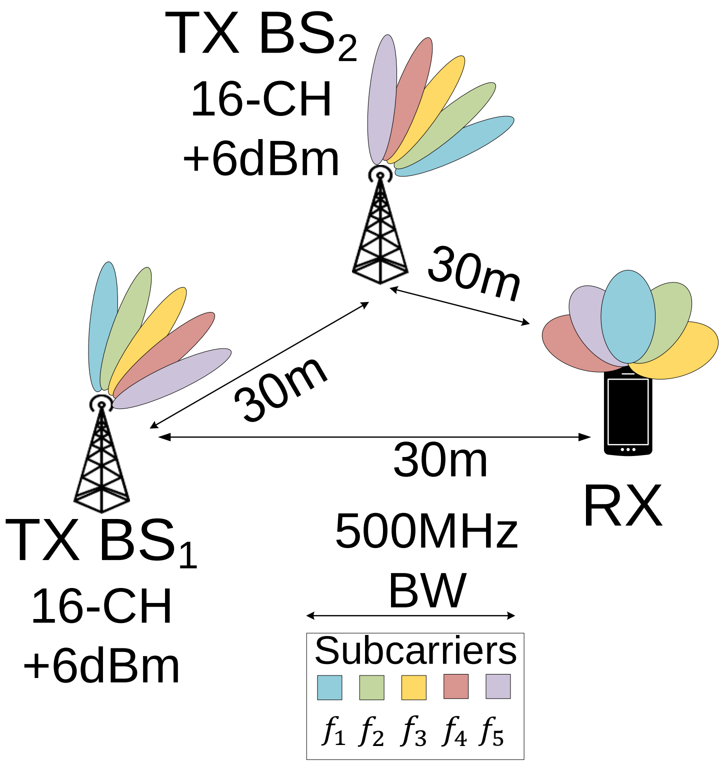
Motivation

Spatial Interference Cancellation (SpICa)



Spatial Int. Canc. w/ Wideband Null





- ❖Dense small cells
- ❖Aggressive frequency re-use
- ❖MIMO
- ❖Co-channel (same frequency)
- ❖Inter-sectoral interference

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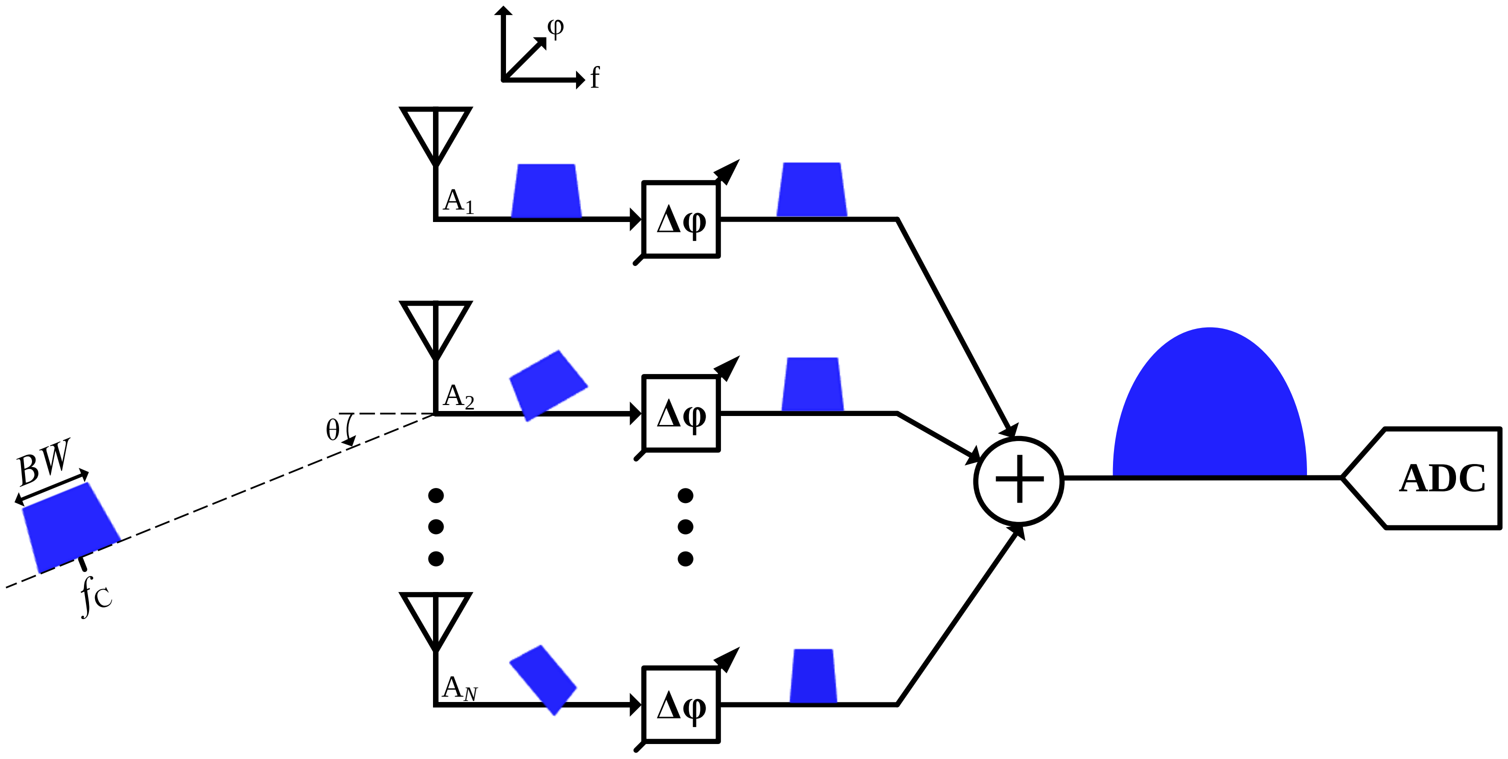
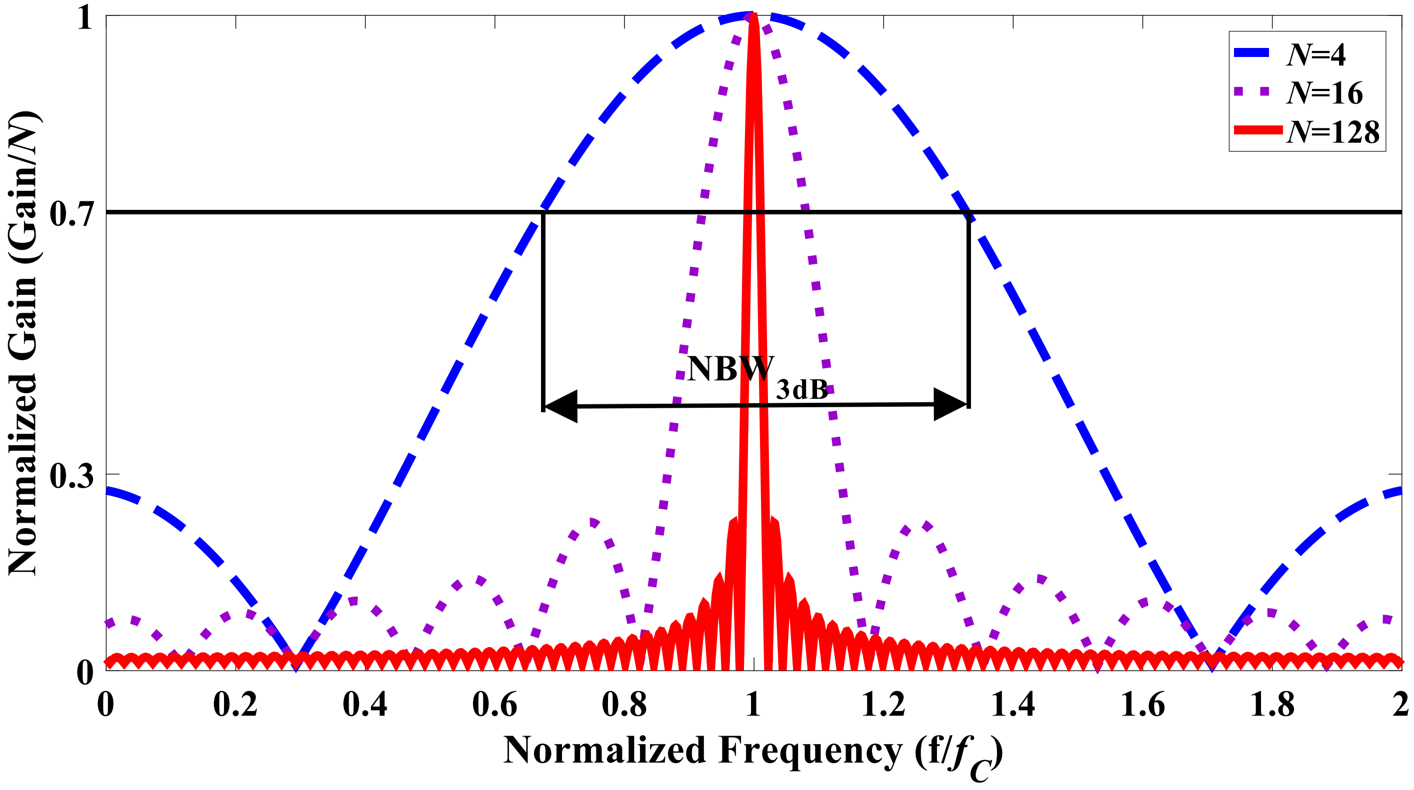
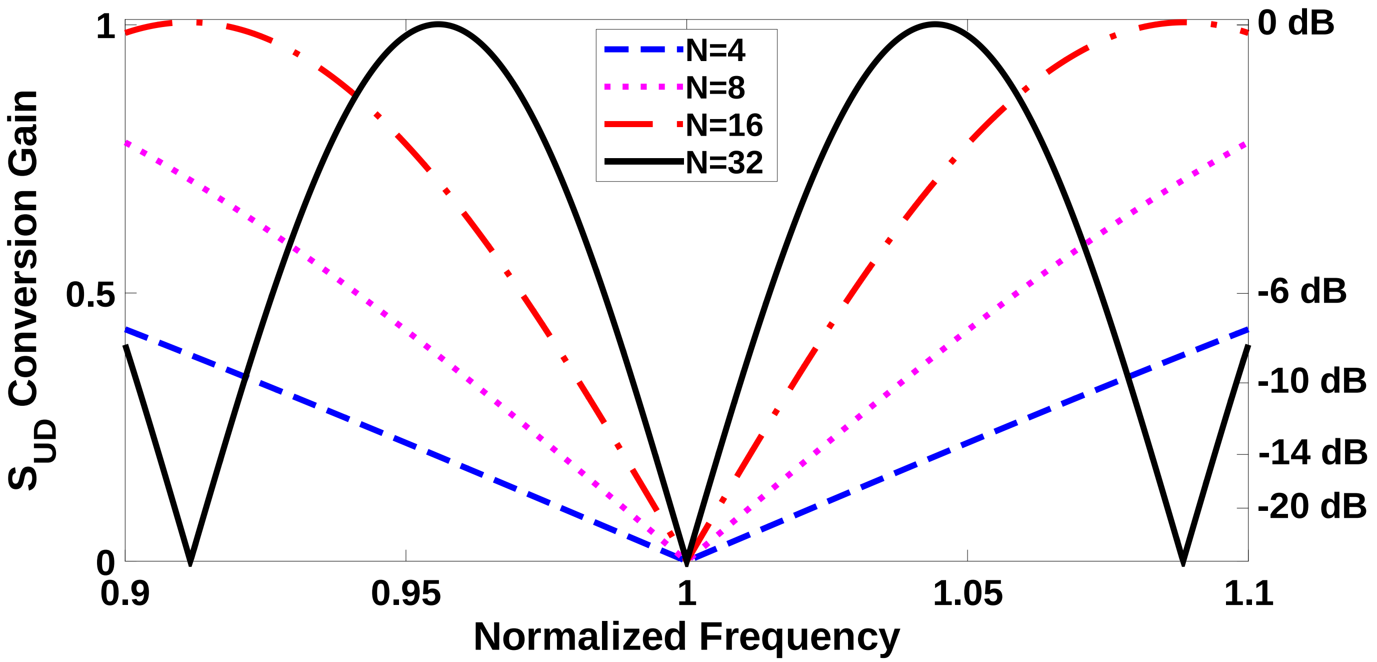
RF/Analog Phase Shift Beamforming





- ❖Valid phase shift approximation for narrow-band signal
- ❖Large antenna arrays suffer from lower normalized 3dB bandwidth (NBW_{3dB})
- ❖Bandpass filtering results in signal distortion and performance degradation
- ❖Easy to implement

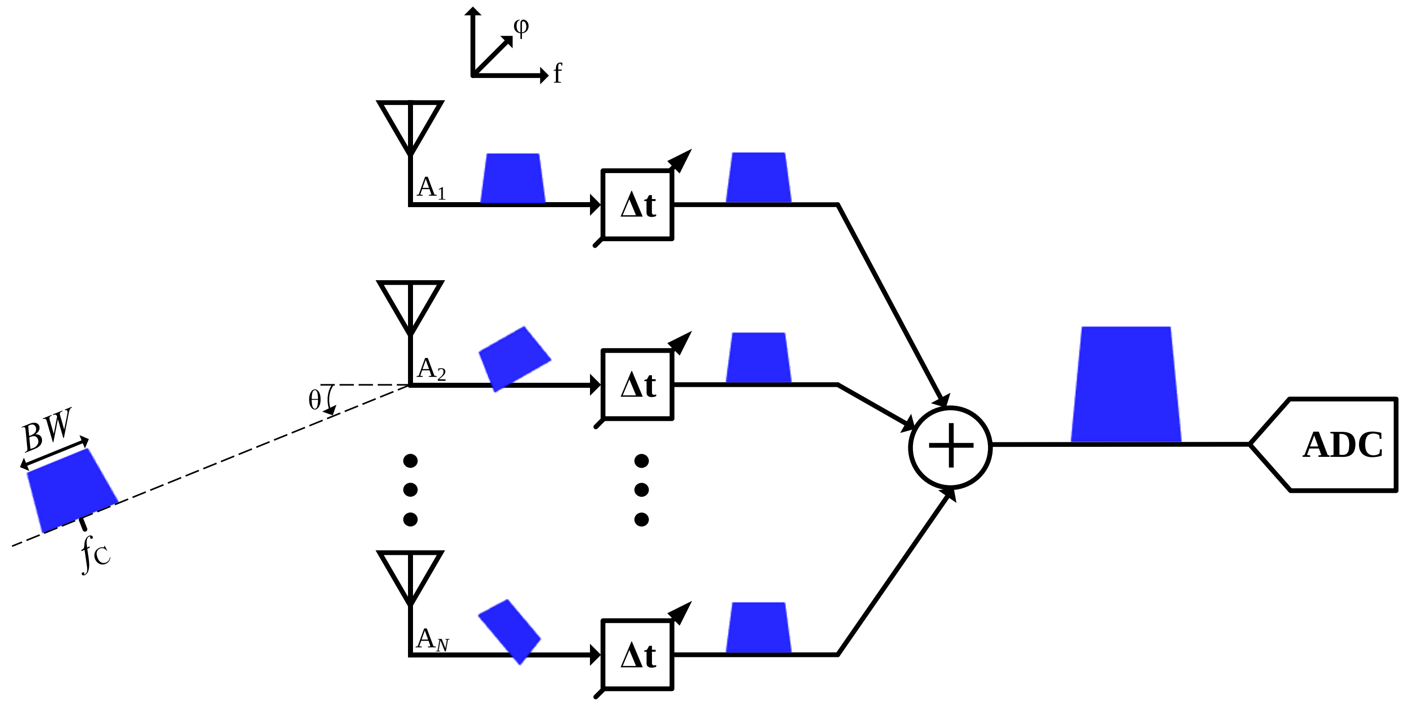
Leakage in Phase-Shifter based Phased Arrays

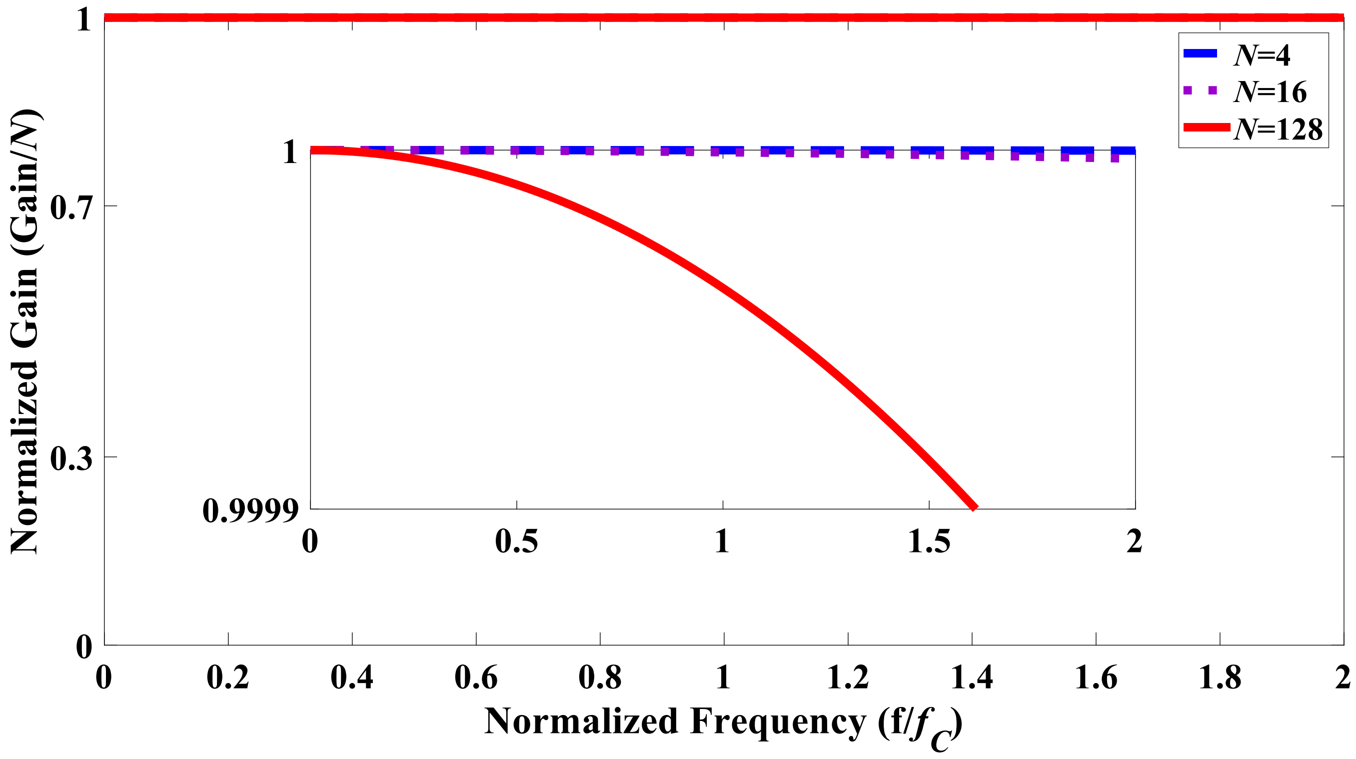


- Cancellation of undesired signal (S_{UD})
- Leakage is dependent on:
  Bandwidth (BW),
  Center frequency (fc),
  Number of elements, (N).

Apps	f_c (GHz)	BW (MHz)	N	S_{UD} Max Conversion Gain in PS-Based SpICa (dB)
802.11ay	60	8640	4	-7.1
802.11ac	5	160	8	-14.0
5G NR n261	28	800	16	-9.1
5G NR n71	0.6	20	32	-5.1

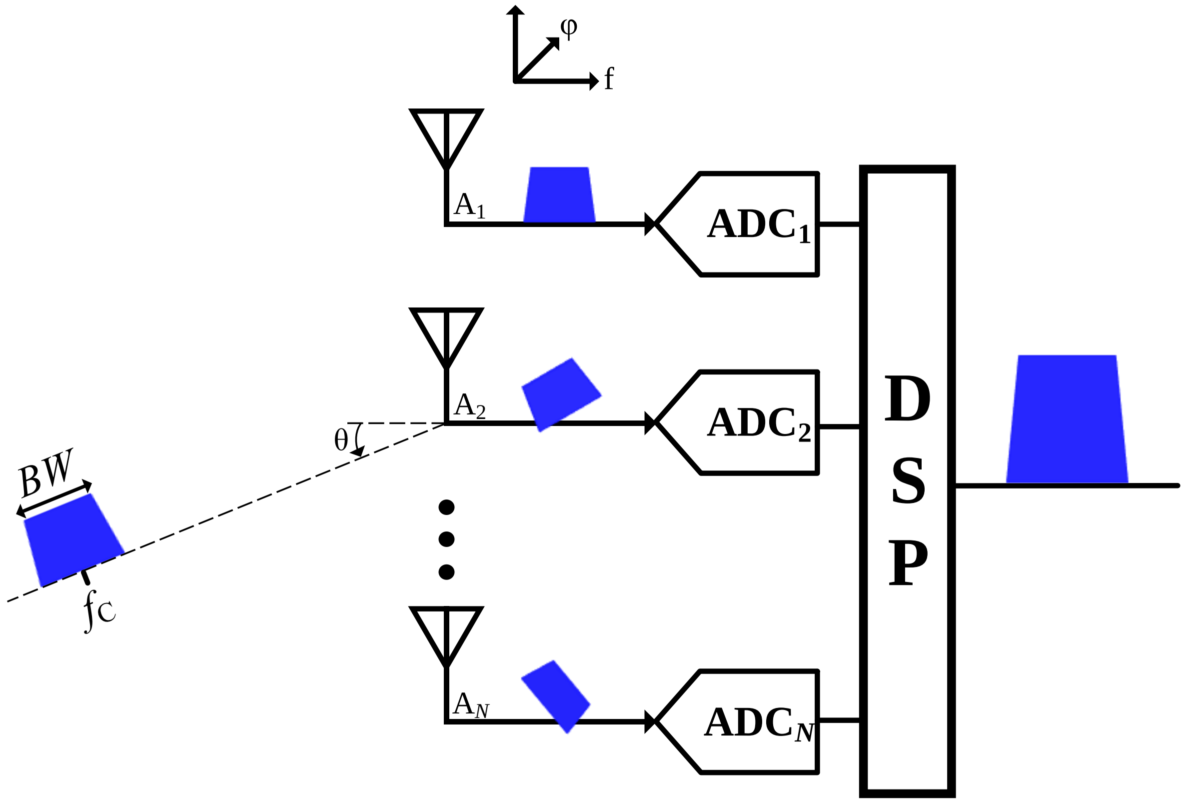
RF TTD Beamforming

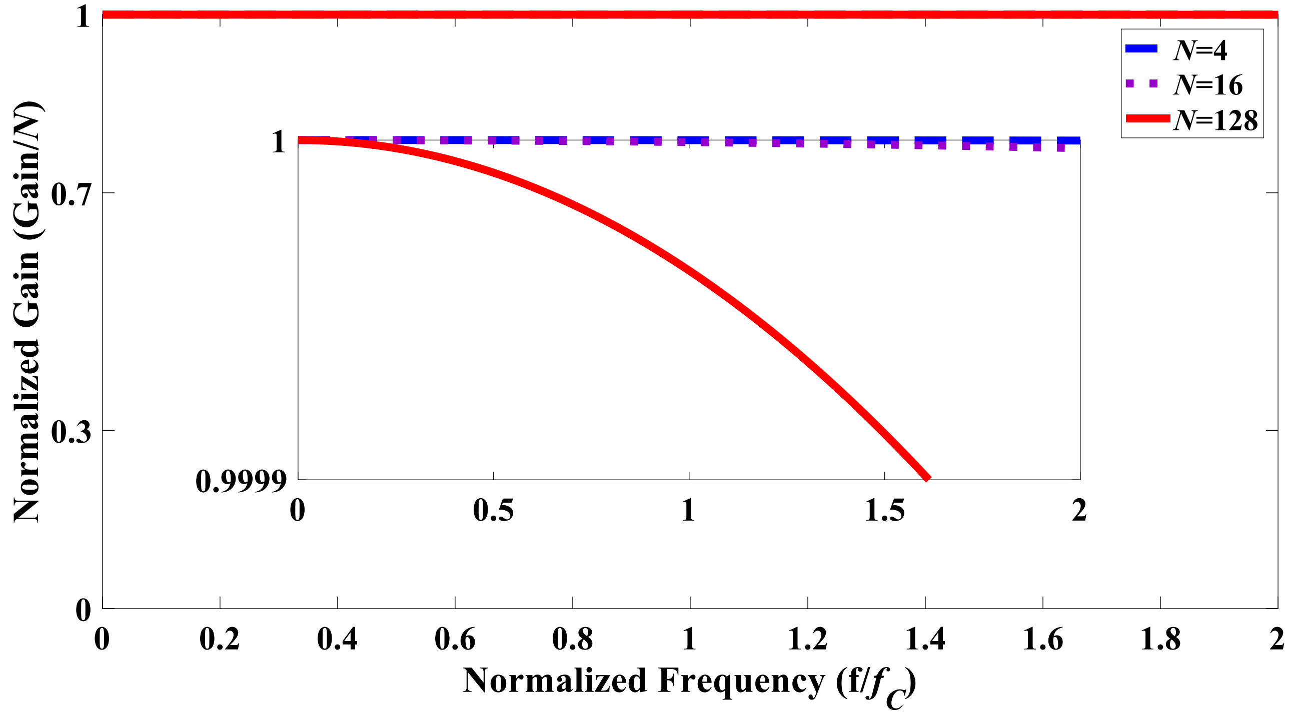




- ❖No frequency-dependency in beamforming gain
- ❖Mismatched components at RF
- ❖Power hungry RF active delay implementations
- ❖Femto-second resolutions at mmWave frequencies
- ❖Limited range of delay elements

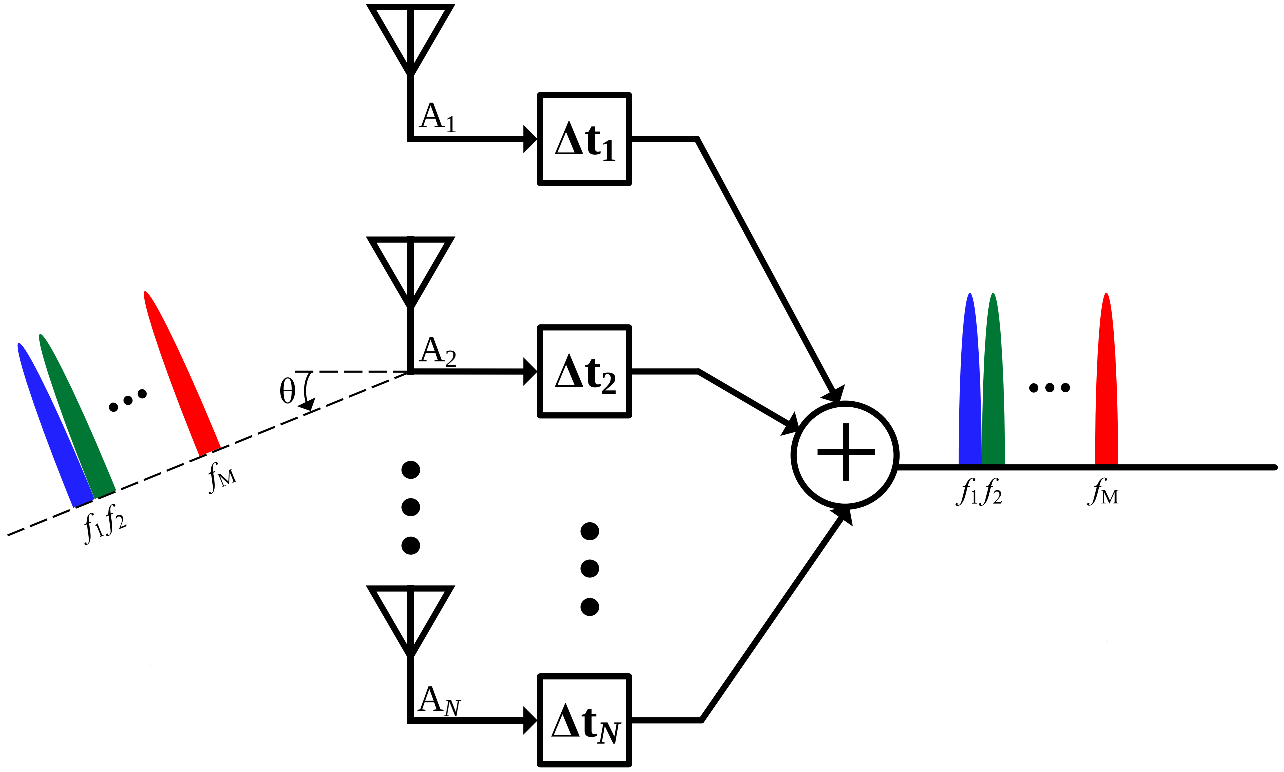
Digital TTD Beamforming

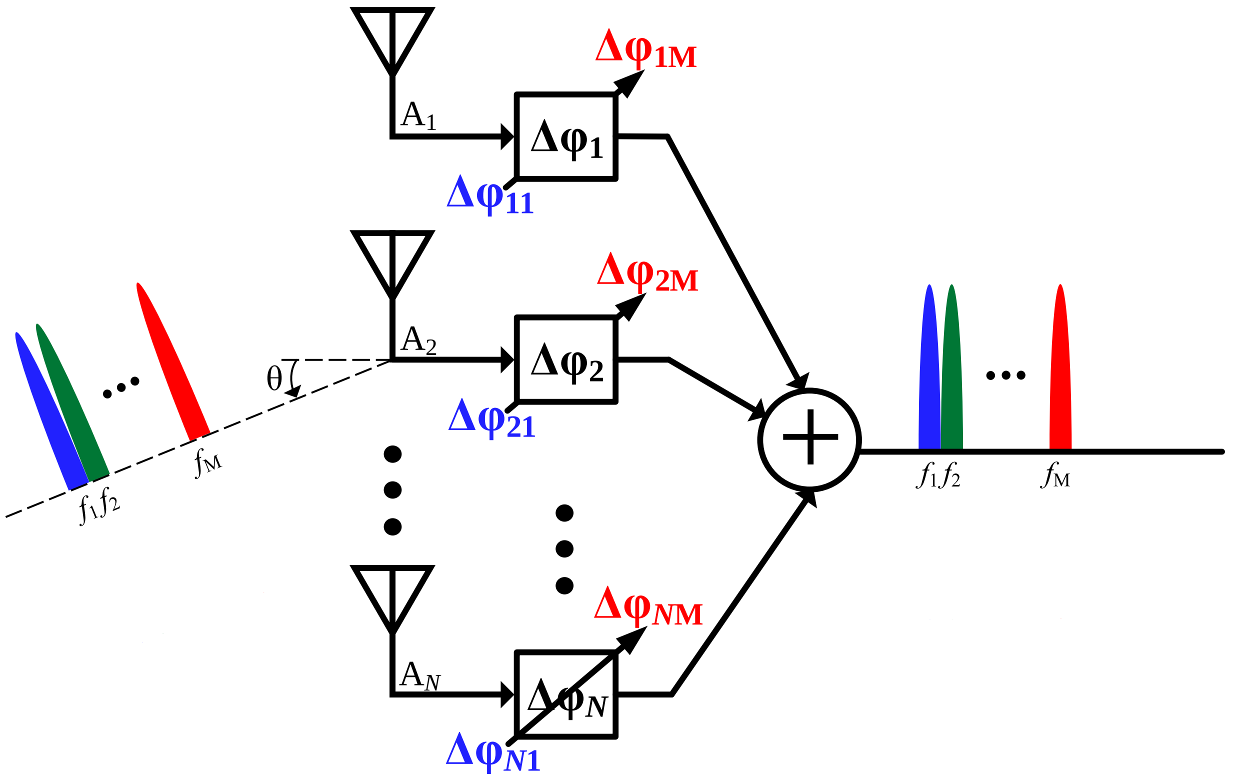




- ❖Higher ADC dynamic range due to no RF/Analog spatial processing
- ❖*N* Power hungry ADCs
- ❖No frequency-dependency in beamforming gain

TTD vs Phase Shift Wideband Beamforming





❖ Phase shift
- Variable phase shift for different sub-carriers

❖ TTD
- Constant time delay for the entire bandwidth

Cancellation requirements w/ TTD-based arrays

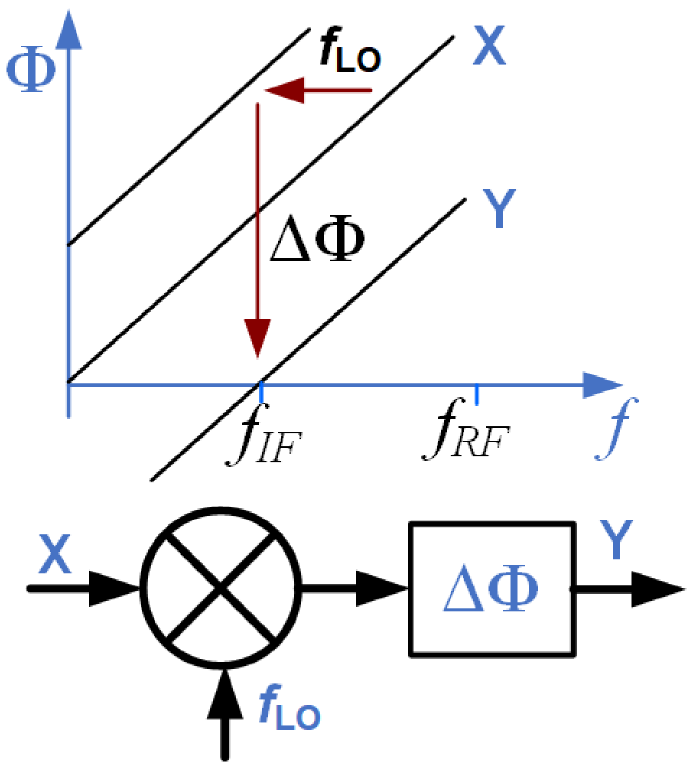
Apps	**f_c (GHz)**	**BW (GHz)**	**N**	**BB TTD Implementation Requirements**				**RF TTD Requirements**
				Δt_{UD} Inter-element Range (ps)	Overall Range $(N-1)\cdot\Delta t_{UD}$ (ps)	$\Delta\varphi_{UD}$ Resolution for 40 dB SpICa (°)	Δt_{UD} Resolution for 40 dB SpICa (ps)	Δt_{UD} resolution for 40 dB SpICa (ps)
802.11ay	60	8640	4	8.3	25	1.2	**0.395**	**0.053**
802.11ac	5	160	8	100.0	700	0.9	**15.17**	**0.48**
5G NR n261	28	800	16	17.9	268	0.6	**2.153**	**0.060**
5G NR n71	0.6	20	32	833.3	25833	0.4	**60.97**	**2.00**

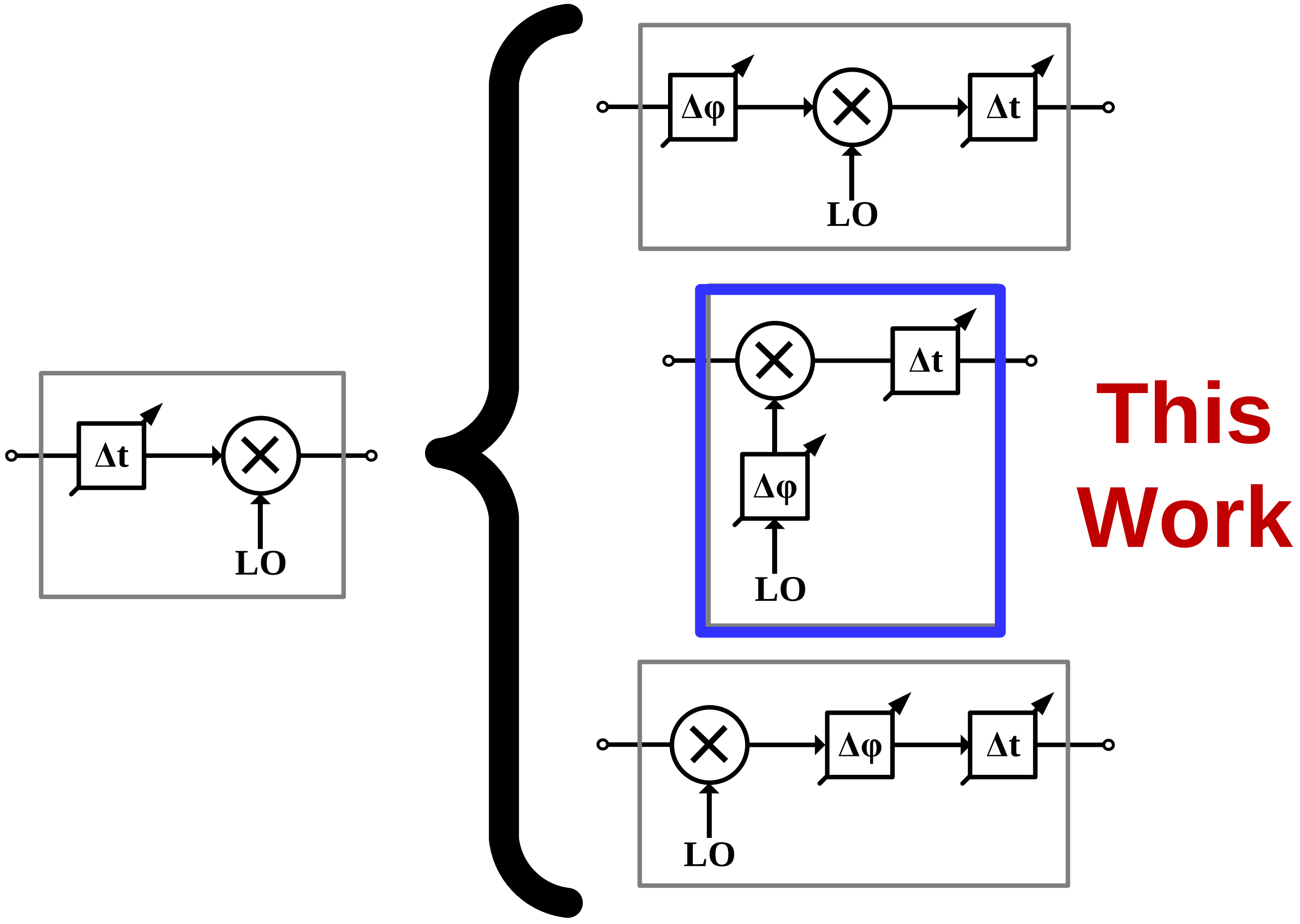
❖TTD requirement in baseband is significantly relaxed

❖Needs a resolution of 2ps (BB TTD) instead of 60fs (RF TTD) at 28GHz.

❖This makes it attractive to do TTD based SpICa at Baseband

Delay Compensation Methods





This Work

RF/IF/LO phase shift
→ single frequency

IF Time Delay + RF/LO Phase Shift
→ multiple frequencies

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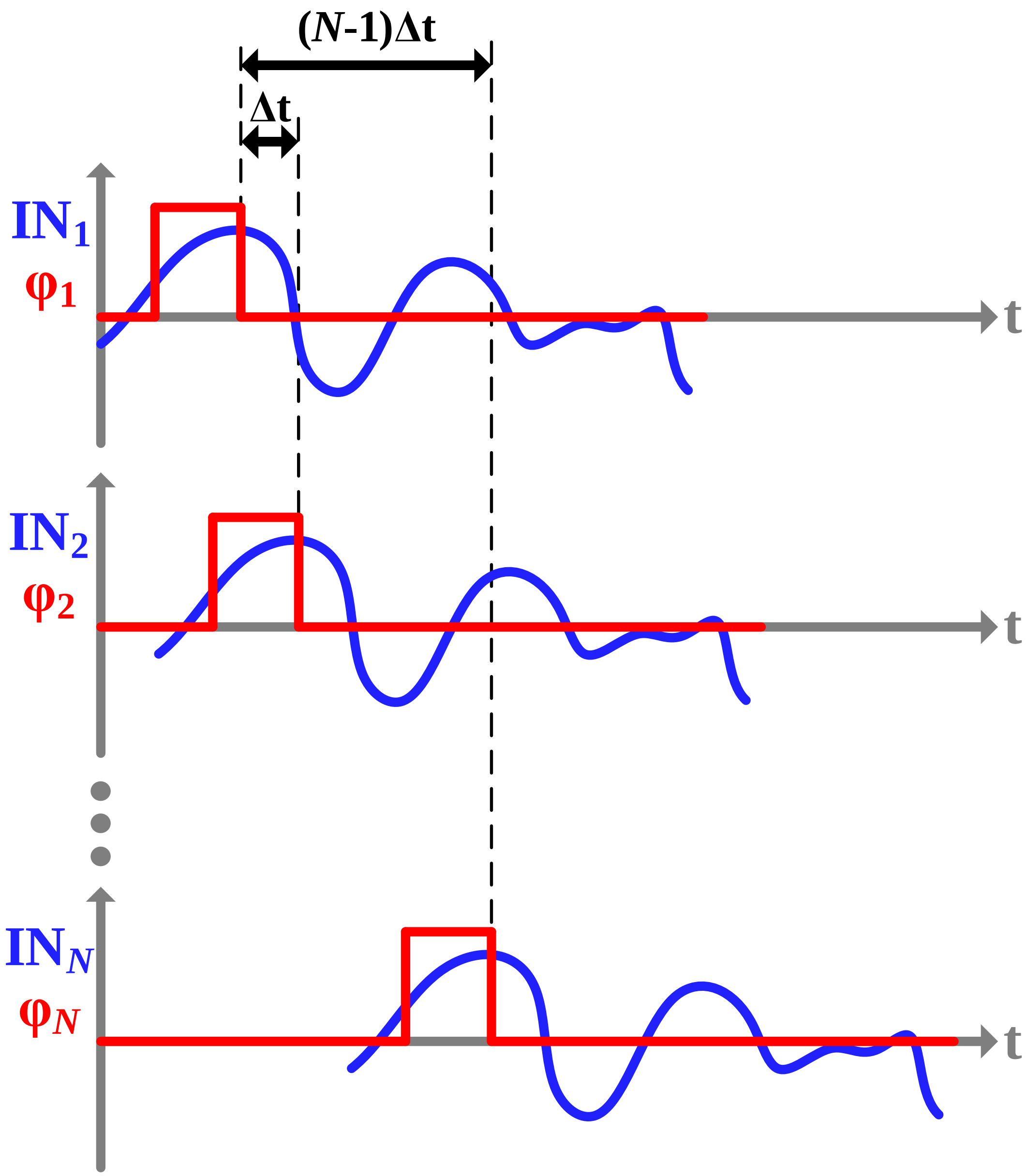
- ❖ Conclusions

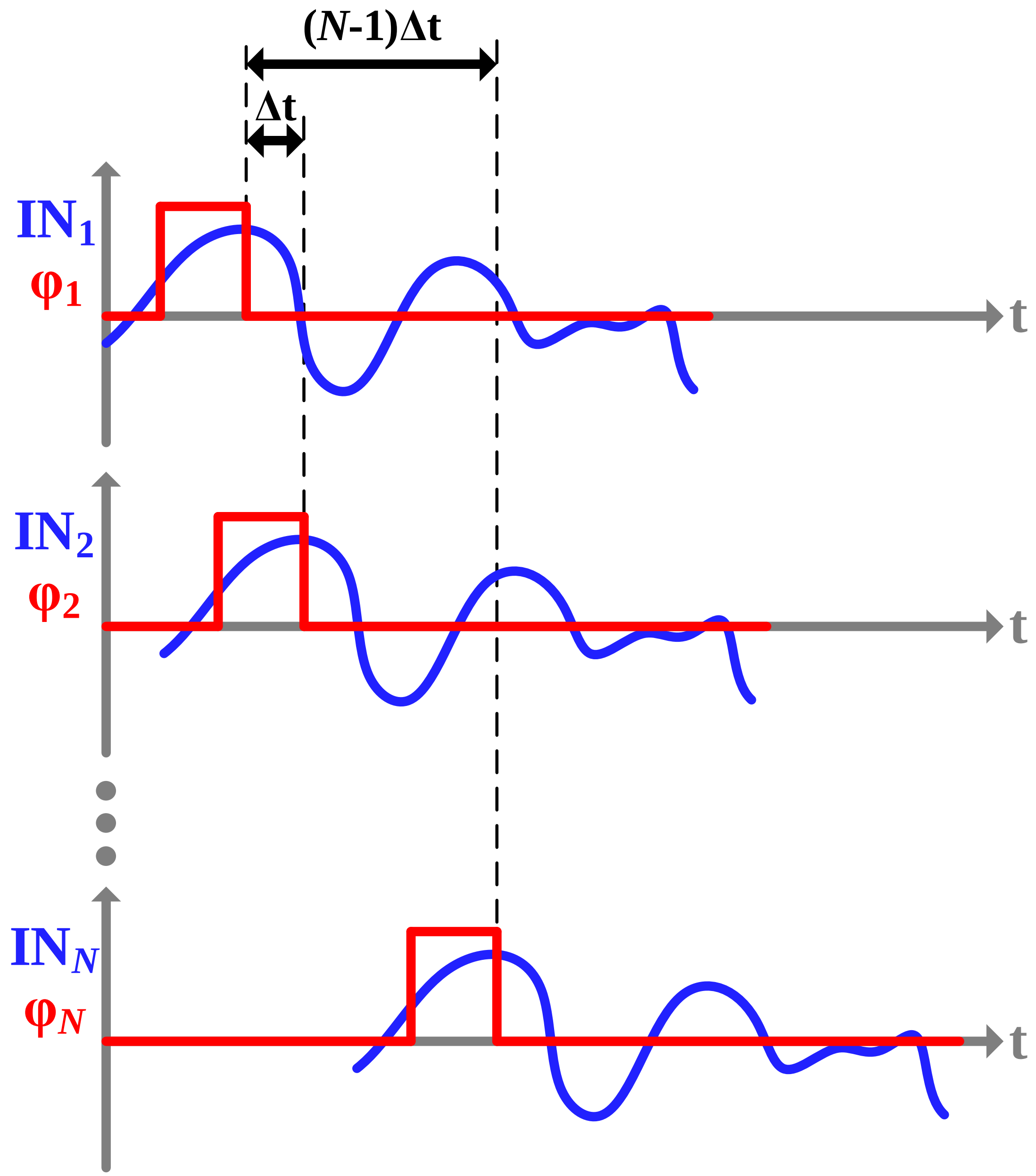
Discrete-time Delay Compensation Technique



- ❖Discrete time implementation
- ❖Introducing delay in signal path is HARD
- ❖Introduce the delay in the CLOCK PATH
- ❖Digitally controlled delay compensation
- ❖Scalable

Discrete-time Beamforming

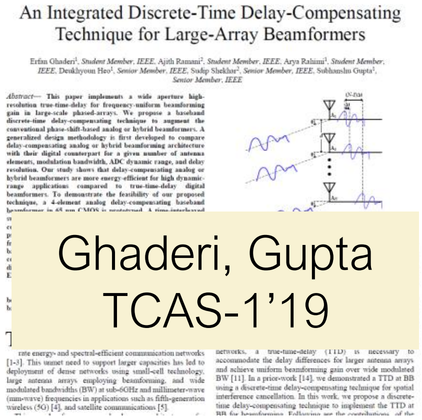
Time alignment – delay compensation



- ❖Discrete time implementation
- ❖NOT in the signal path
- ❖Minimum number of ADCs
- ❖Digitally controlled delay compensation
- ❖Scalable

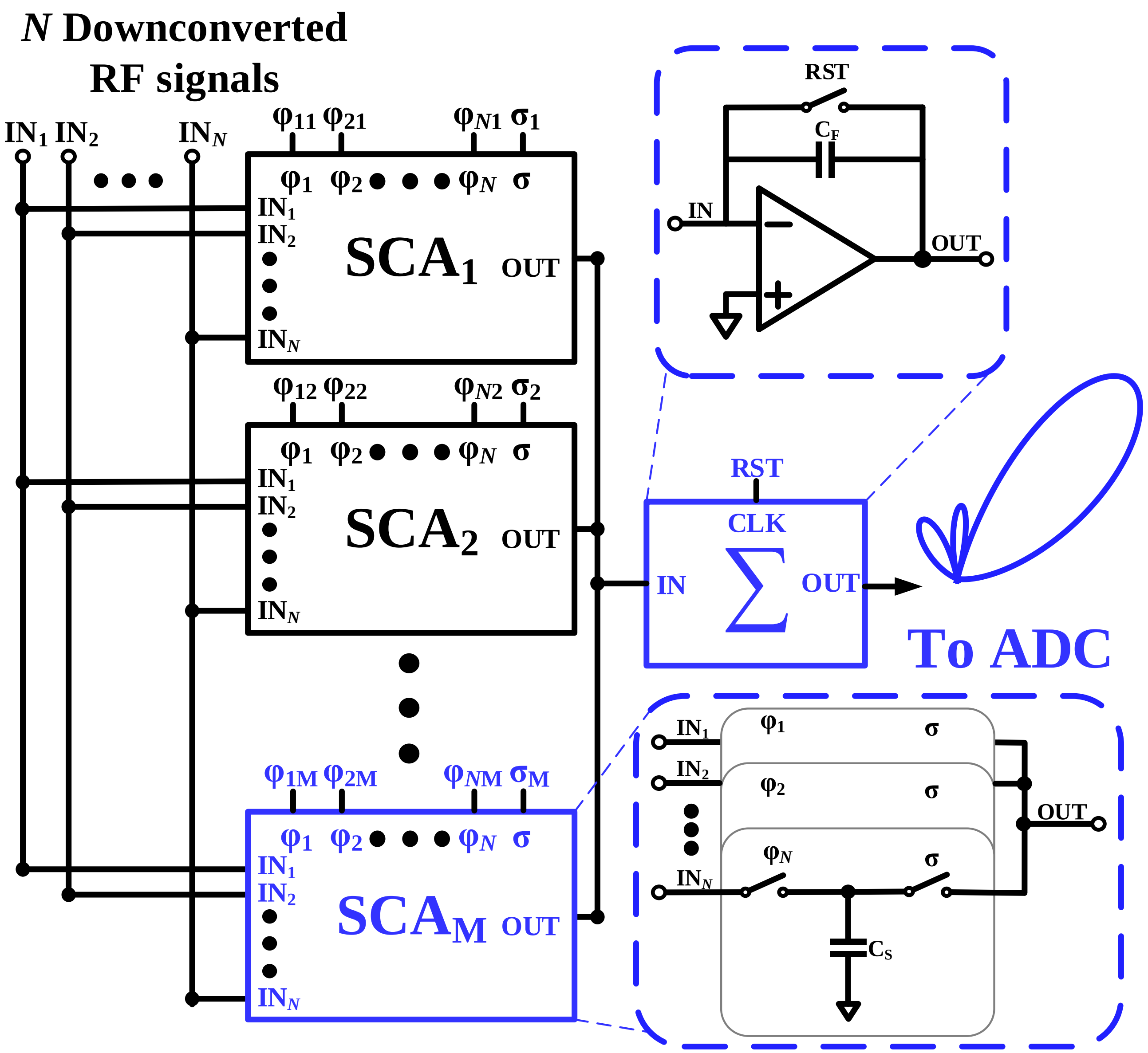
Proposed Discrete-Time BMFRM Arch.

Analog Discrete-time Beamforming



An Integrated Discrete-Time Delay-Compensating Technique for Large-Array Beamformers

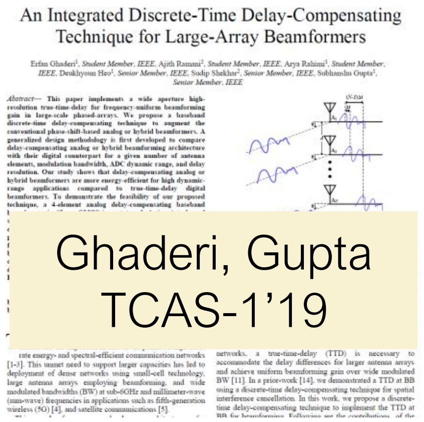
Ghaderi, Gupta
TCAS-1’19



- ❖Non-Uniform-Sampling based switched-capacitor array
- ❖NOT in the signal path
- ❖<u>1 ADC per beam</u>
- ❖Digitally controlled delay compensation
- ❖Scalable
- ❖High clocking power consumption

Discrete-time Delay Compensating Arch.

Clocking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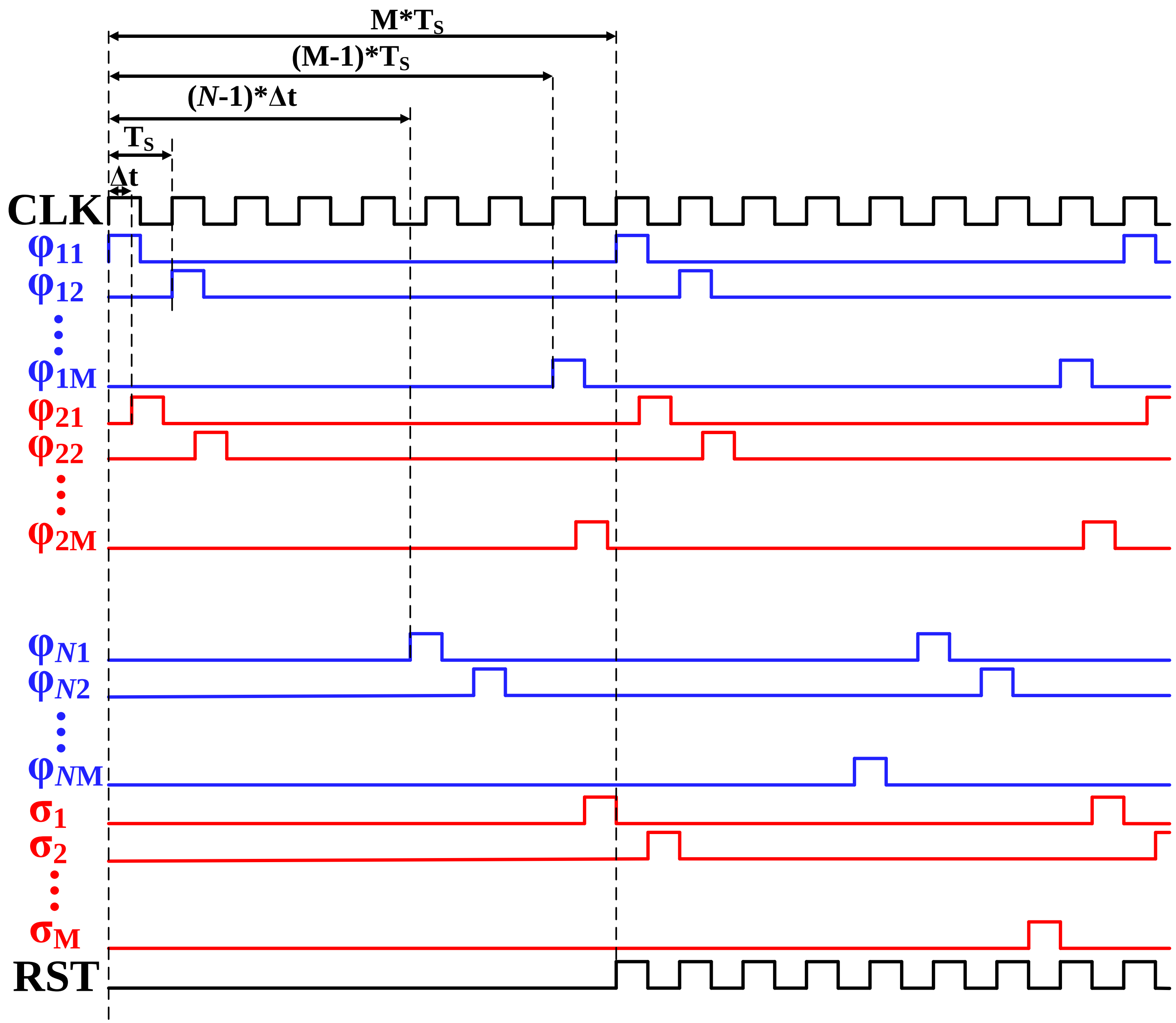
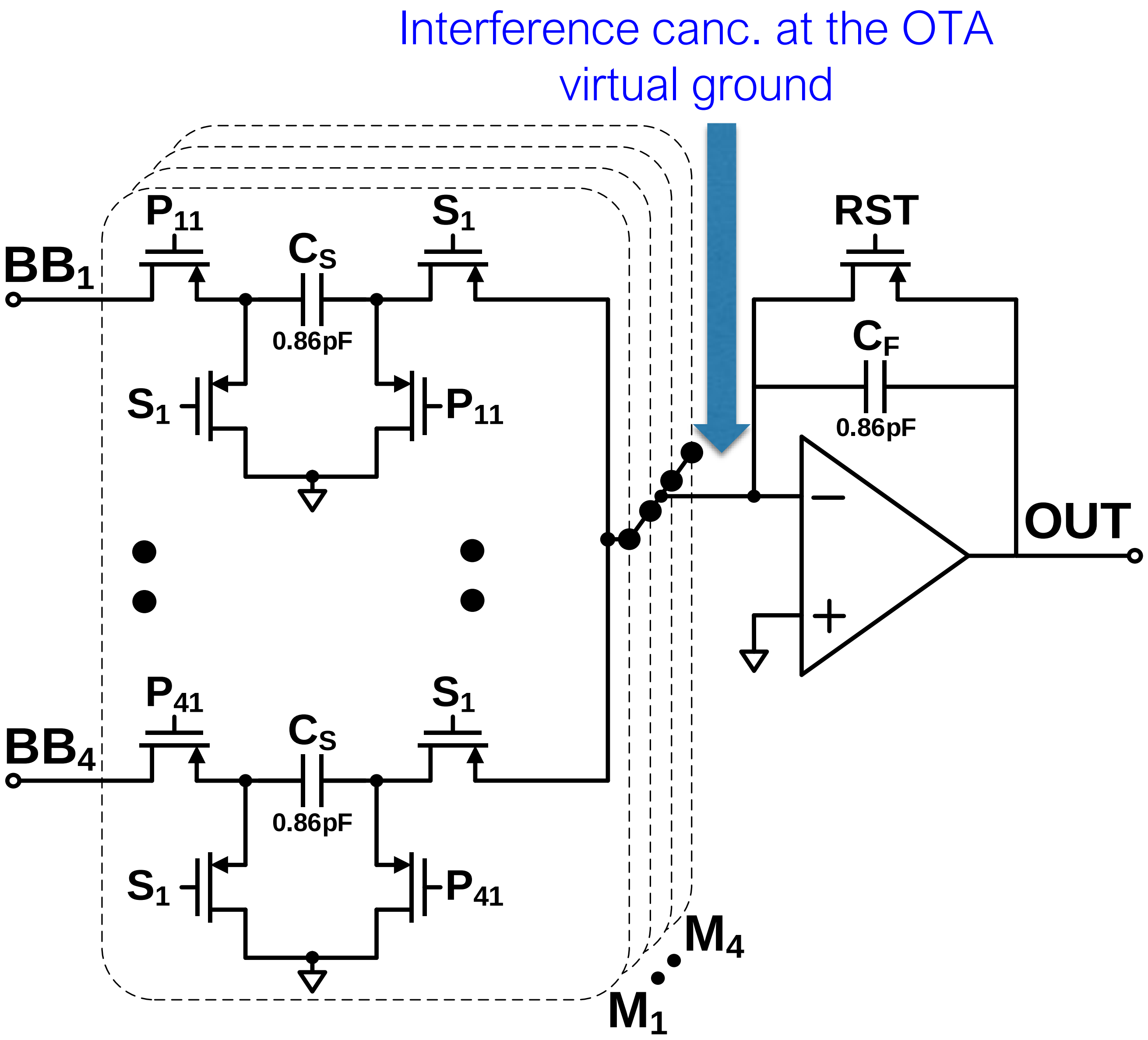


- ❖Delay compensation through phase interpolation
- ❖M-levels of interleaving for covering larger delay ranges
- ❖$f_s = 1 / T_s = 2 {*} f_{BW}$

$$\Delta t_{max} = (N - 1)\cdot\Delta t|_{\theta=\pm 60}$$

$$= \frac{\sqrt{3}}{2}\cdot(N - 1)\cdot\frac{d}{\lambda_C}\cdot\frac{1}{f_C}$$

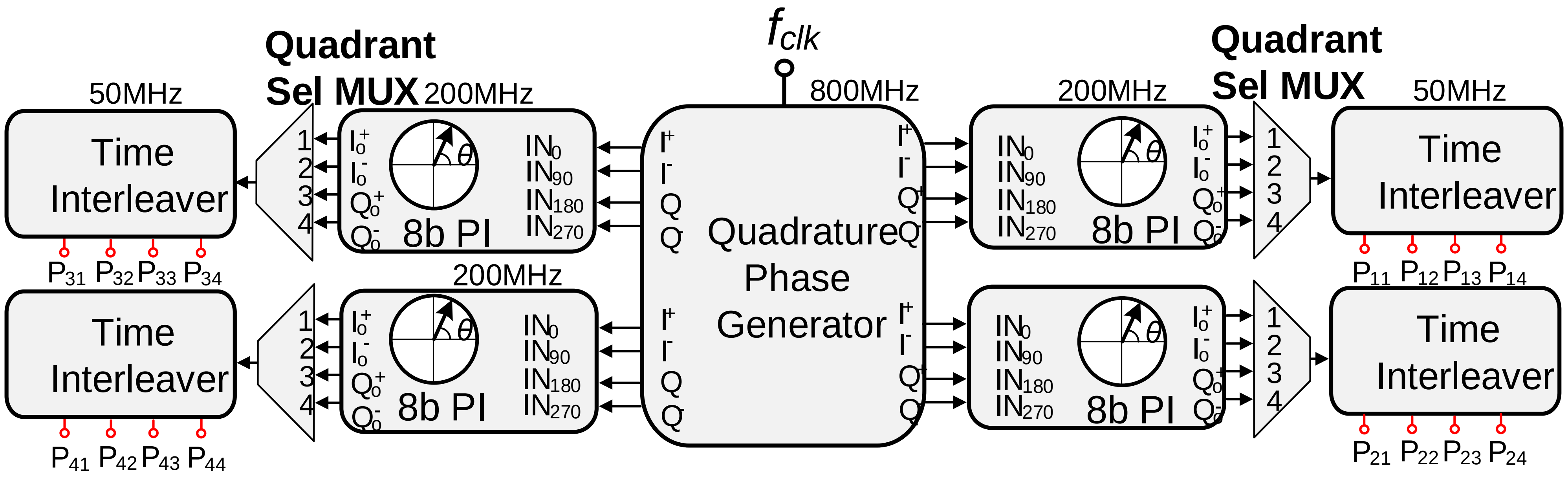
Switched-Capacitor Adder (SCA)

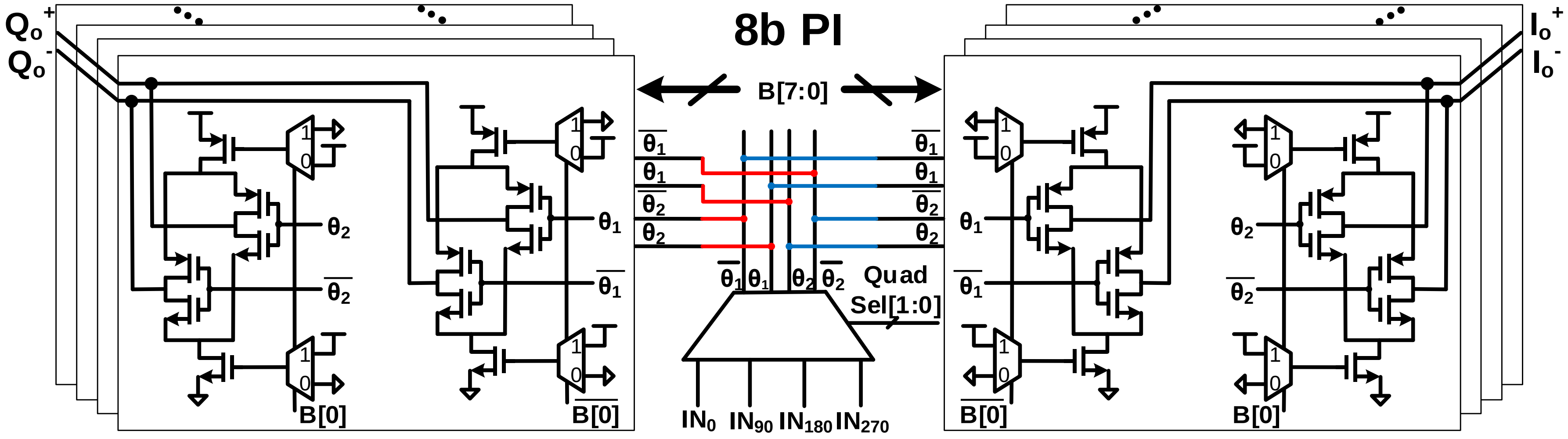


- ❖Parasitic insensitive topology
- ❖Wide bandwidth OTA with 3mW /200 MHz 3dB BW
- ❖Interference cancellation at the virtual ground node → output swing and linearity requirement easy to meet
- ❖Sampling cap designed to meet thermal noise for 10-bit resolution.
- ❖β is limited when using multiple elements

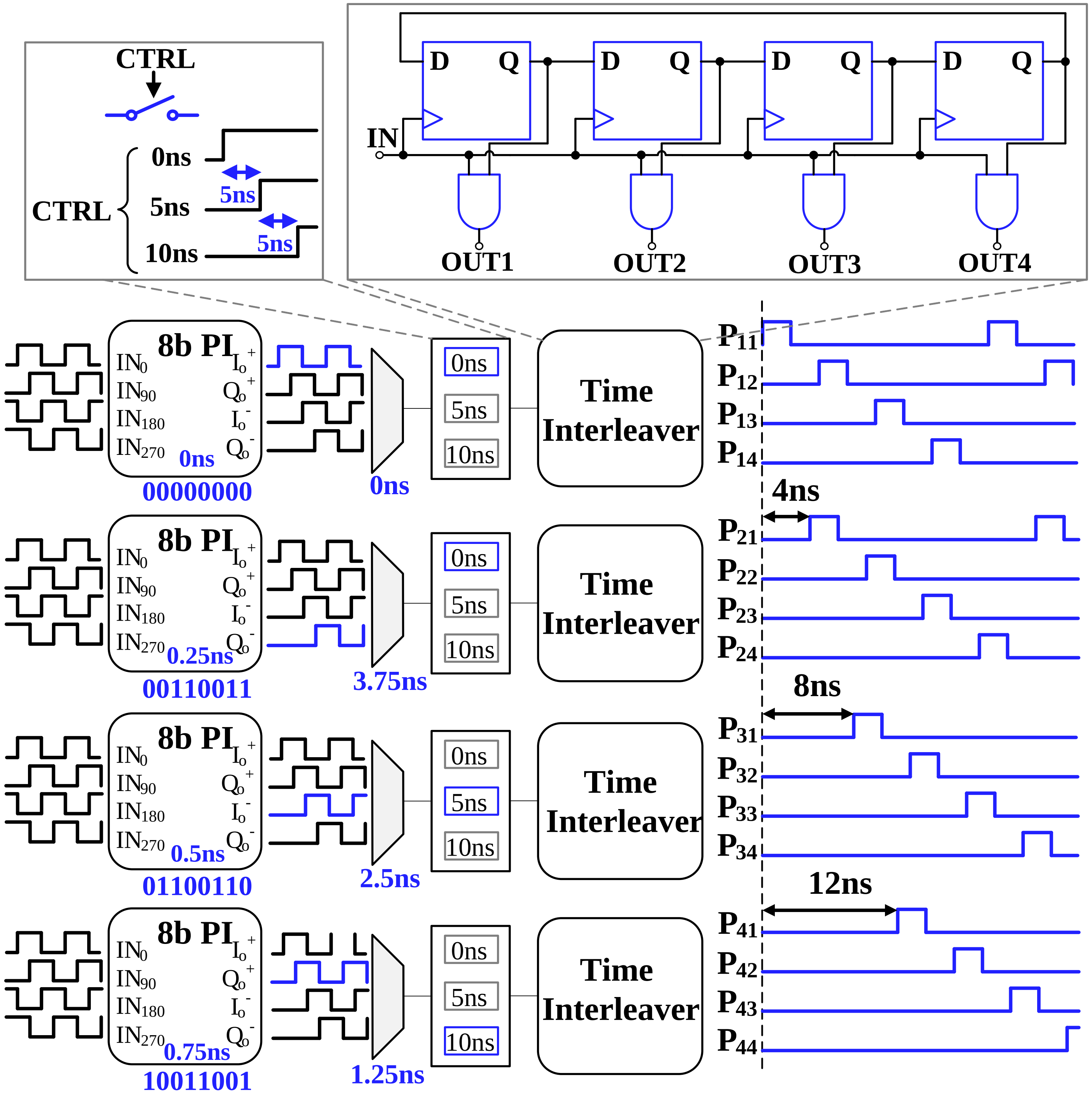
Clock Generation Unit

Proposed Time Interleaver with 8-bit Phase Interpolator

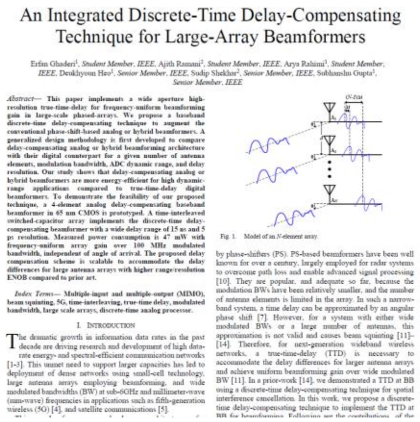




Example Delay Compensating for 4ns



- ❖ States of the time-interleaver and important phases for delay compensation of 4 ns between consecutive antennas.
- ❖ 4-phases with 12.5% ON-time from a time interleaver
- ❖ Delay of 15ns and resolution of 5ps deliberately chosen for both communication and future initial access modes

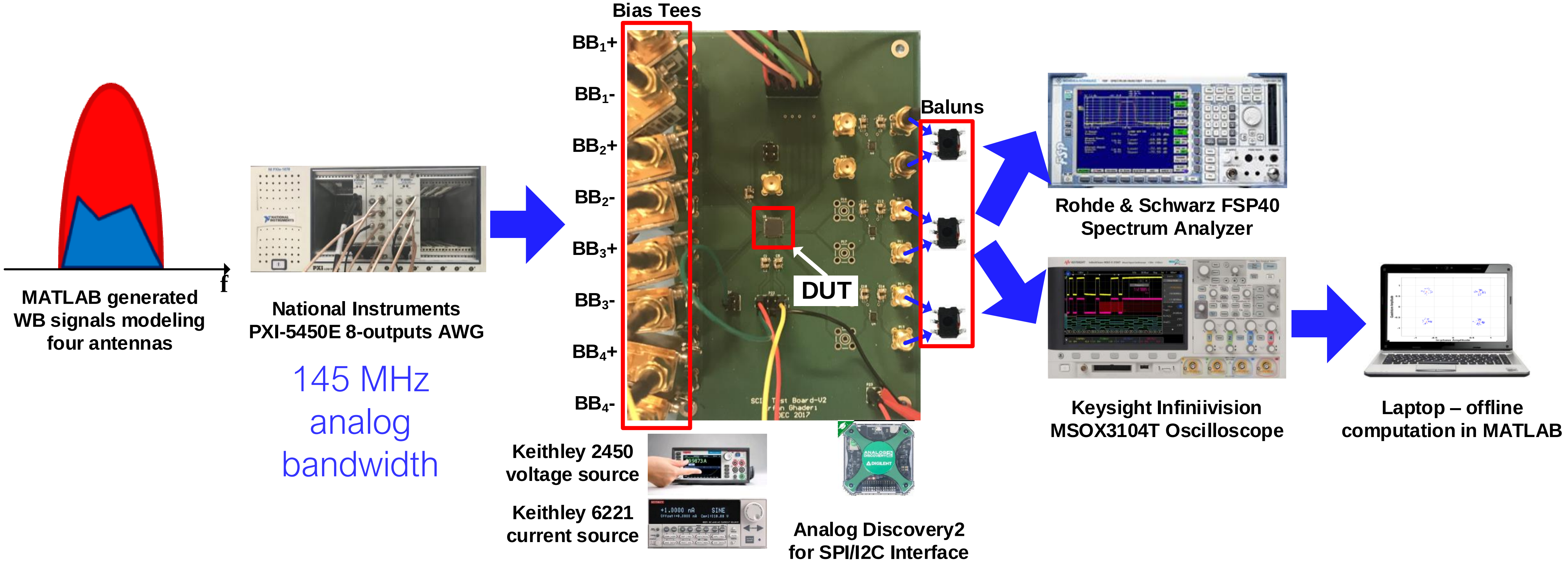


An Integrated Discrete-Time Delay-Compensating Technique for Large-Array Beamformers

Erfan Ghaderi[1], *Student Member, IEEE*, Ajith Ramani[2], *Student Member, IEEE*, Arya Rahimi[1], *Student Member, IEEE*, Deukhyoun Heo[1], *Senior Member, IEEE*, Sudip Shekhar[2], *Senior Member, IEEE*, Subhanshu Gupta[1], *Senior Member, IEEE*

Discrete-time Delay Compensating Arch.

Test Setup



MATLAB generated WB signals modeling four antennas

National Instruments PXI-5450E 8-outputs AWG

145 MHz analog bandwidth

Bias Tees

BB$_1$+

BB$_1$-

BB$_2$+

BB$_2$-

BB$_3$+

BB$_3$-

BB$_4$+

BB$_4$-

DUT

Baluns

Rohde & Schwarz FSP40 Spectrum Analyzer

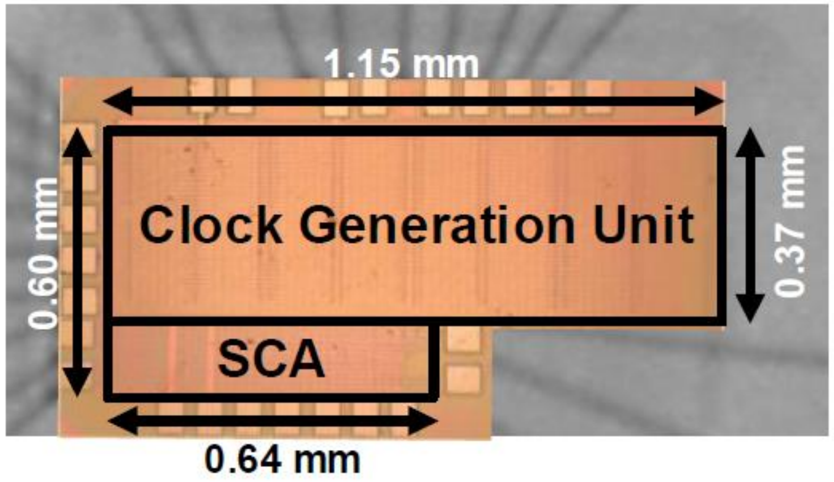
Keysight Infiniivision MSOX3104T Oscilloscope

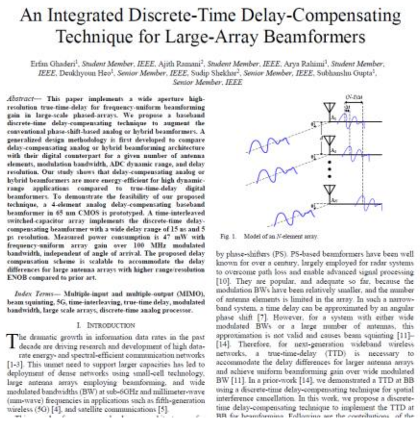
Laptop – offline computation in MATLAB

Keithley 2450 voltage source

Keithley 6221 current source

Analog Discovery2 for SPI/I2C Interface





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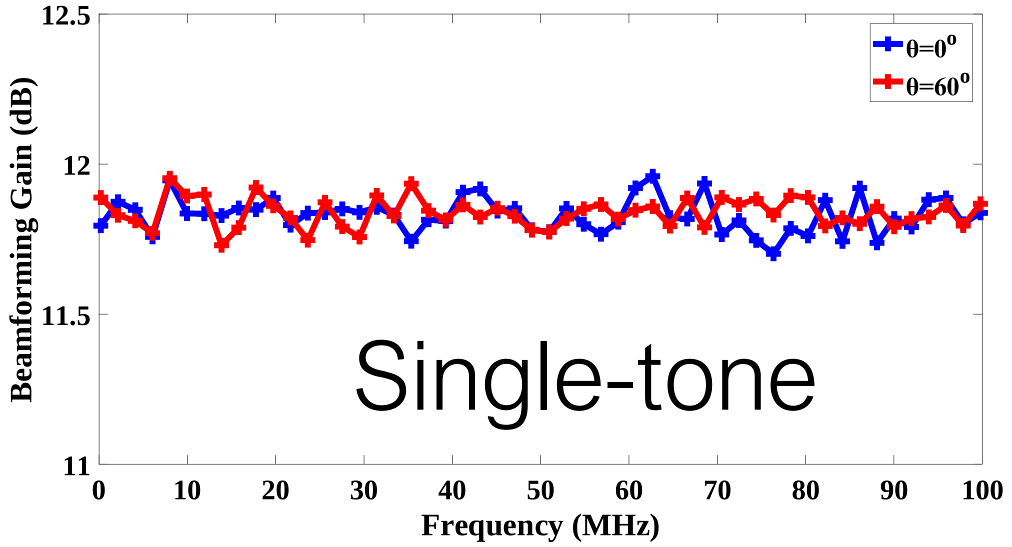
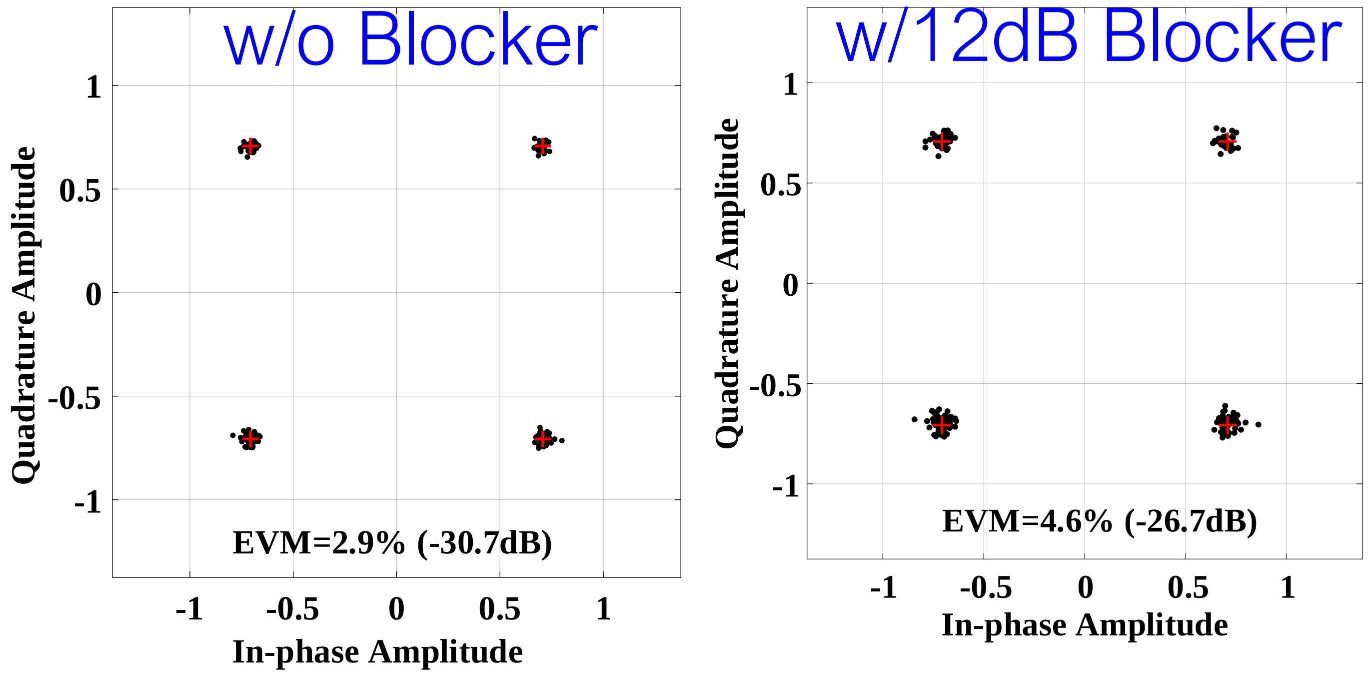
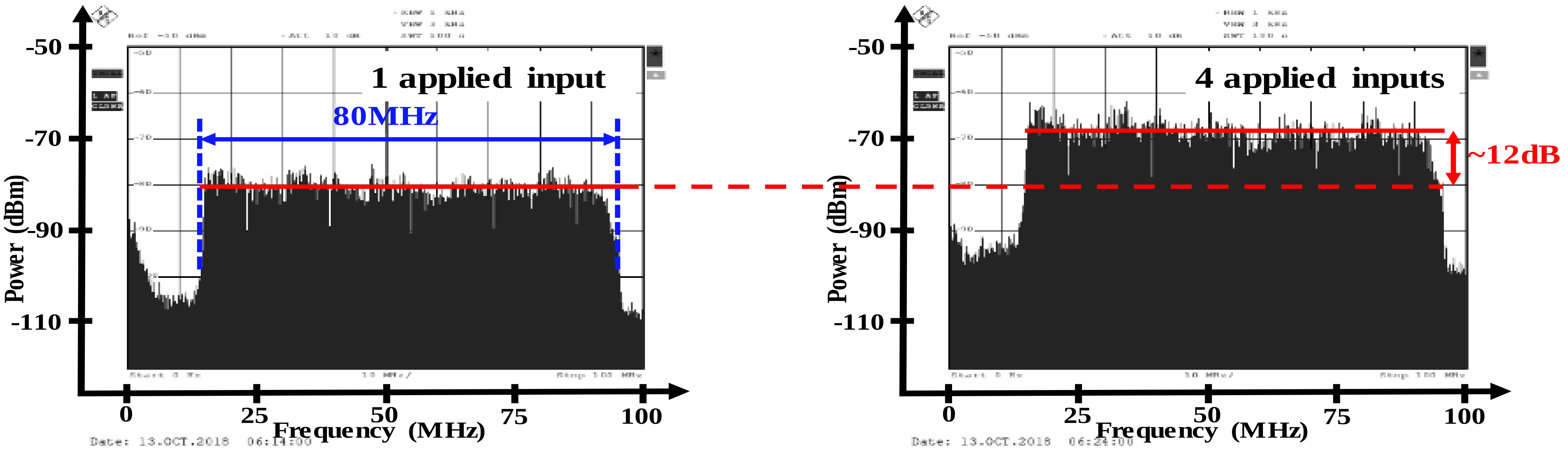
Discrete-time Delay Compensating Arch.

Results

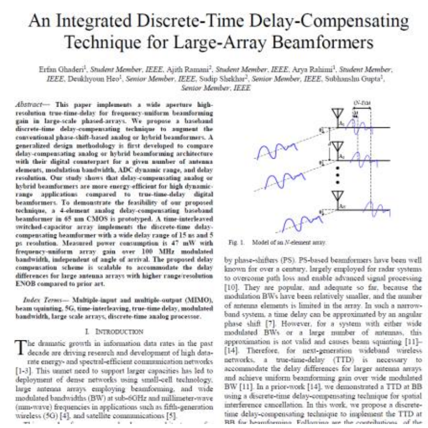






Discrete-time Delay Compensating Arch.

Measurement Results (sample)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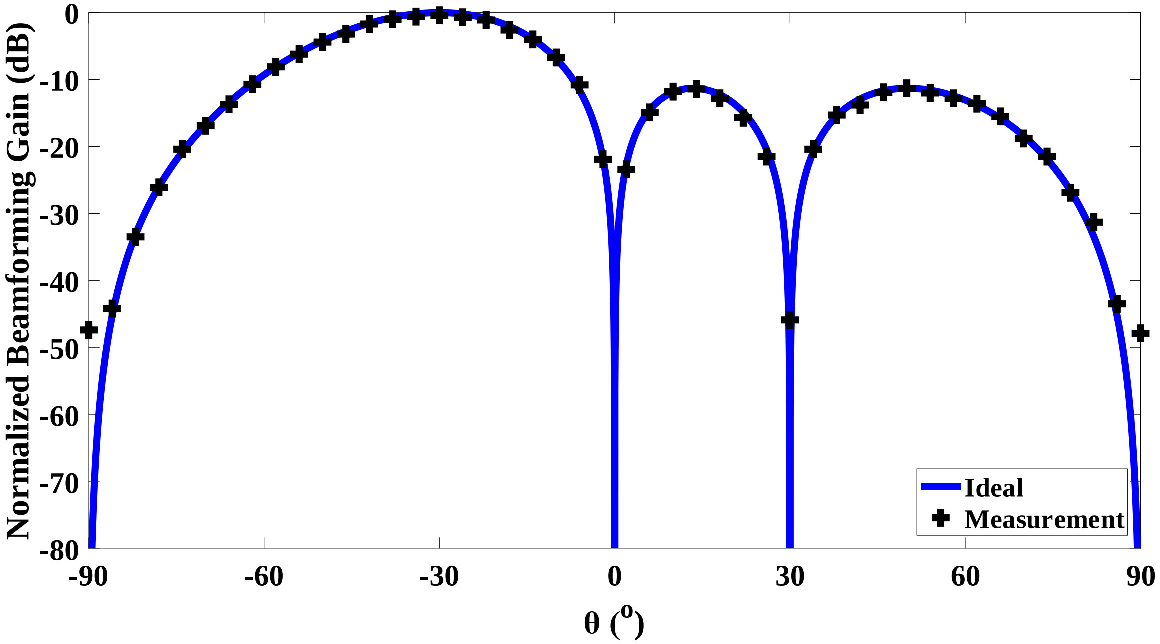
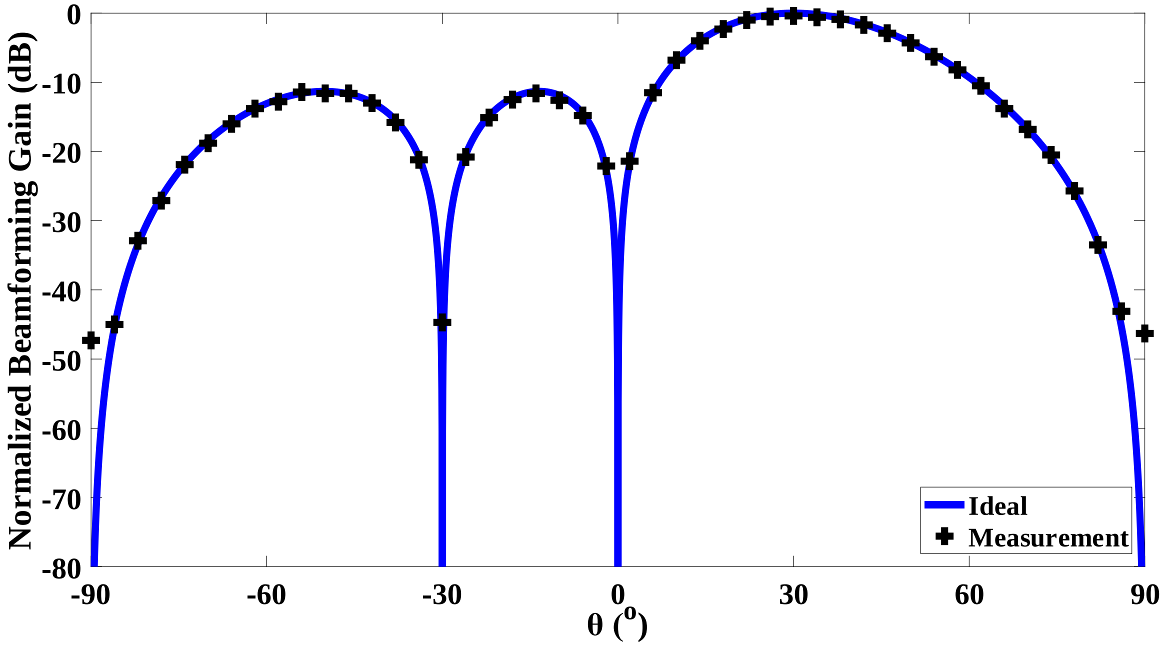
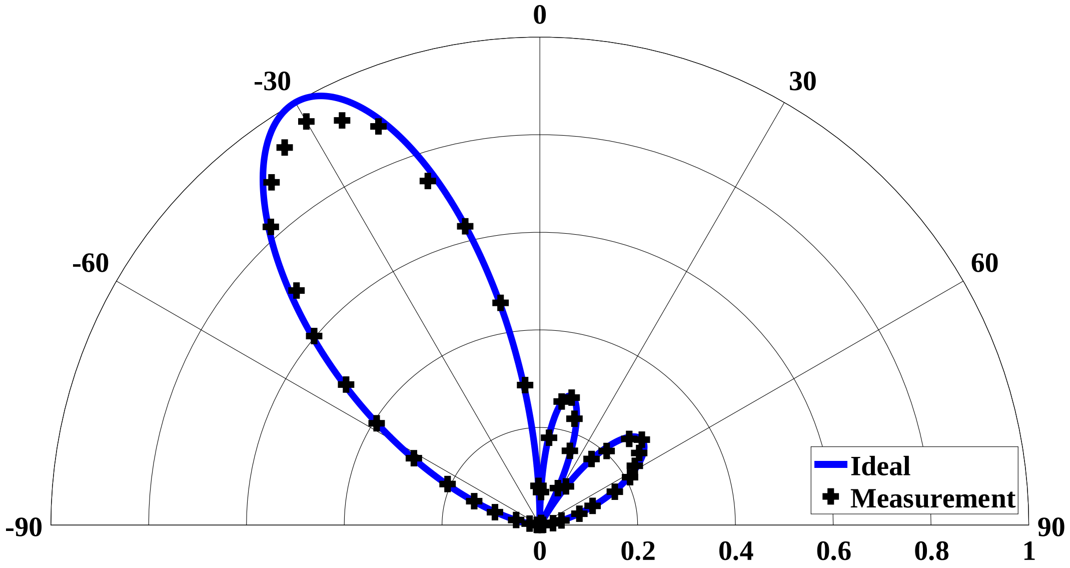
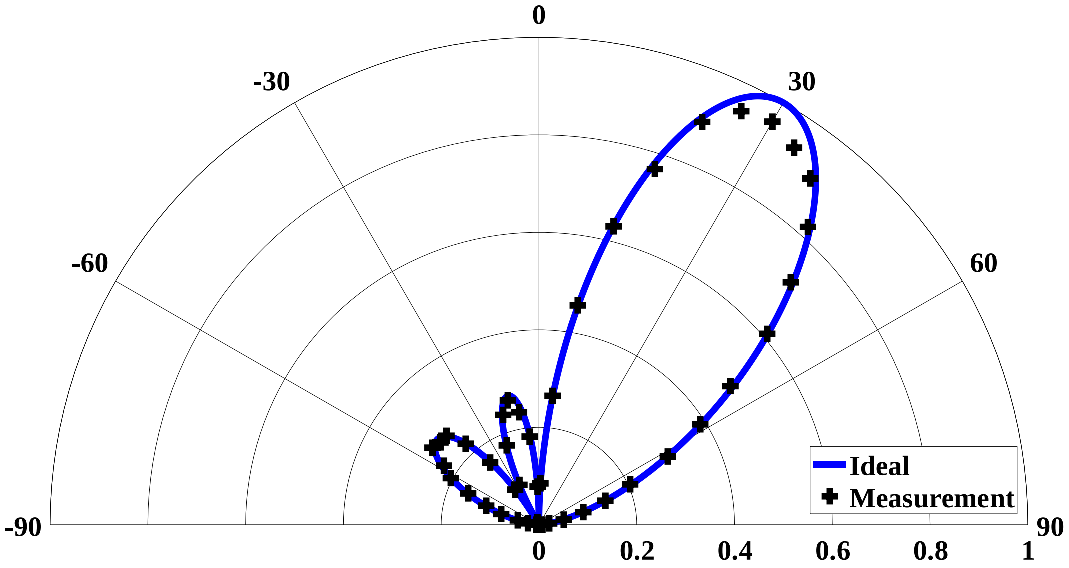


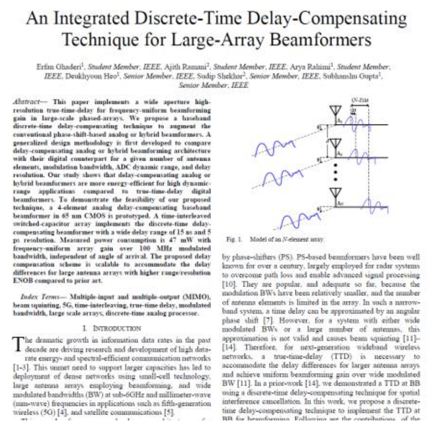






Discrete-time Delay Compensating Arch.

Comparison w/ state-of-the-art



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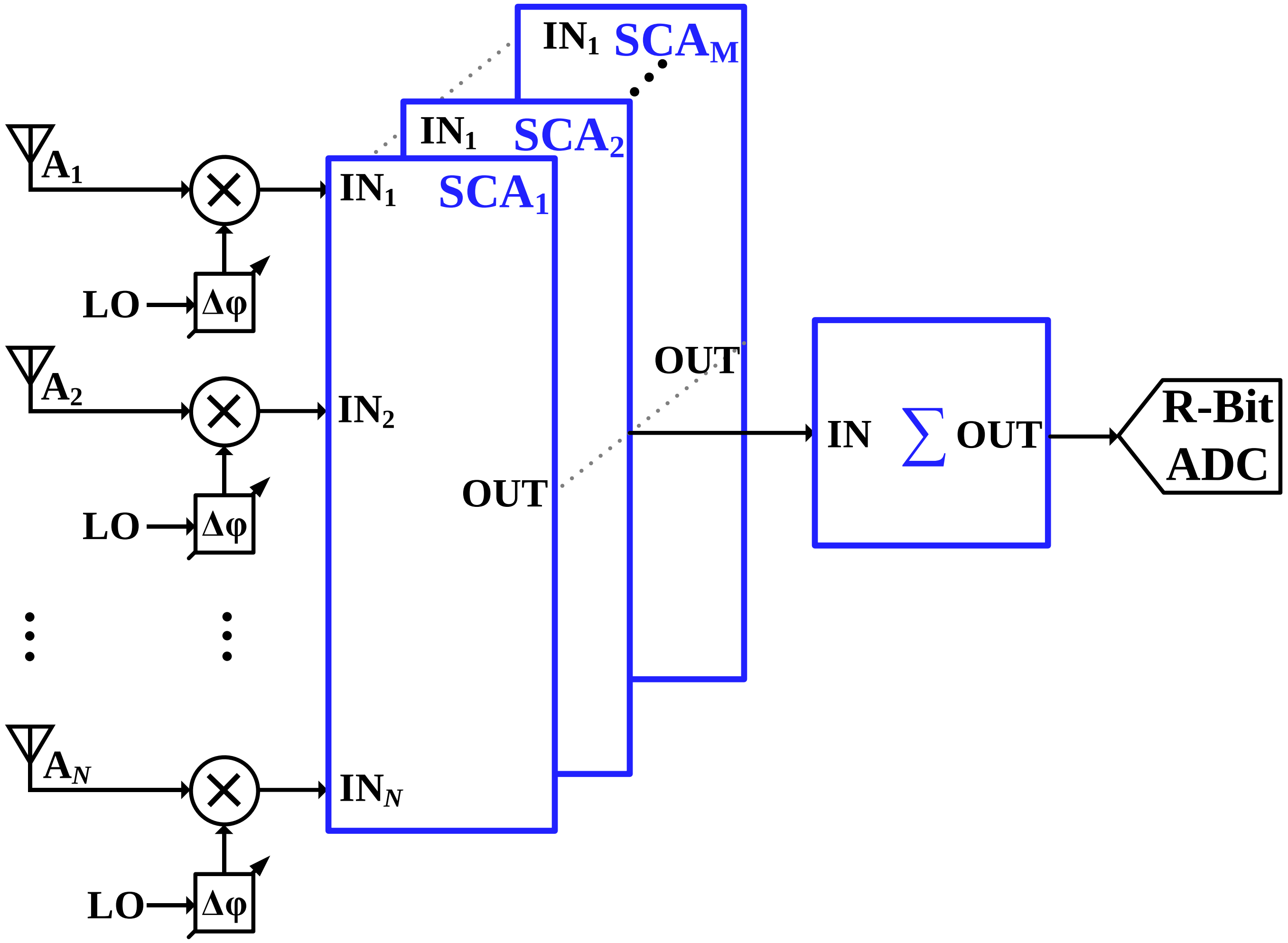
	RFIC2018	JSSC2017	IMS2015	JSSC2015	RFIC2018	**Proposed Work**
Approach	LC delay[a]	Gm-C	Delay line[a]	Gm-C	Delta-Sigma	**BB True-Time-Delay compensation**
# Channel	-	-	-	4	16	**4**
# Beam	-	-	-	1	4	**3**
Tech. (nm)	BiCMOS (130)	CMOS (130)	CMOS (130)	CMOS (140)	CMOS (40)	**CMOS (65)**
VDD (V)	2.5	1.4	1.2	1.5		**1.0**
Delay Range (ps)	508	1450	400	550	7500	**15000**
Delay Resolution (ps)	4	10	5	13	500	**5**
ENOB Log$_2$(Range/Res)	7.0	7.2	6.3	5.4	4	**11.6**
Frequency Range (MHz)	18000	1900	19000	1500	100	**~100 (BB)**
Area (mm^2)	5.45	0.6	4	1	0.29	**0.57 (active)**
Power	285mW[a]	112-364mW[b]	2.6-6mW[a]	450mW[b]	453mW	**Analog: 3mW/100MHz** **Clock: 44mW** **Total: 47mW**

[a] just delay implementation, [b] RF-FE included

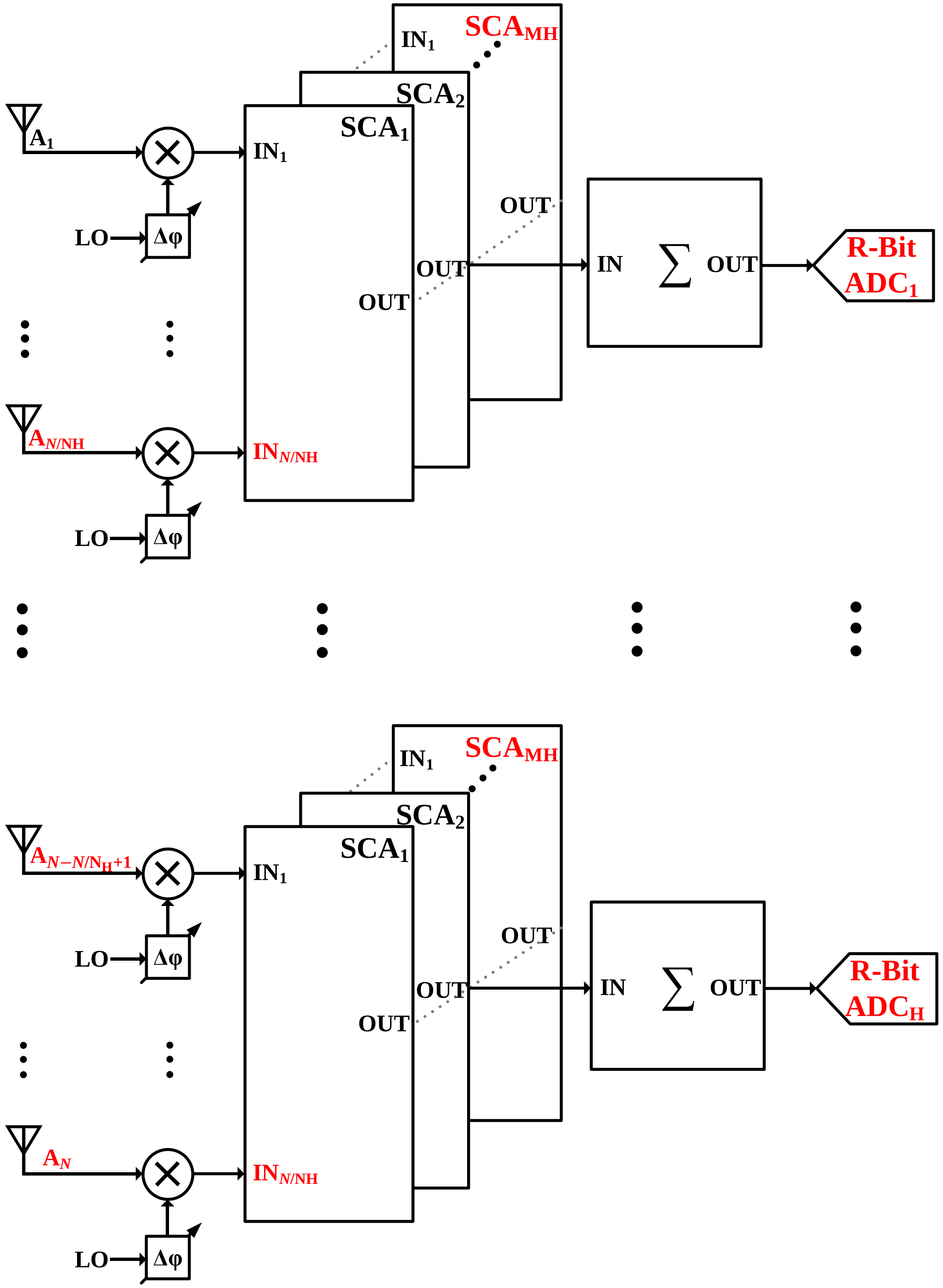
Discrete-time Delay Compensating Arch.



- Large # of elements, wider BW → higher gain-bandwidth OTA
- Example target system: 1500 elements, 3ns scan range, 6-bit resolution, 500MHz BW
- Increasing *N* increases *M* and digital power consumption
- Analog beamforming cannot support large array or BW
- Solution:
- Hybrid Beamforming

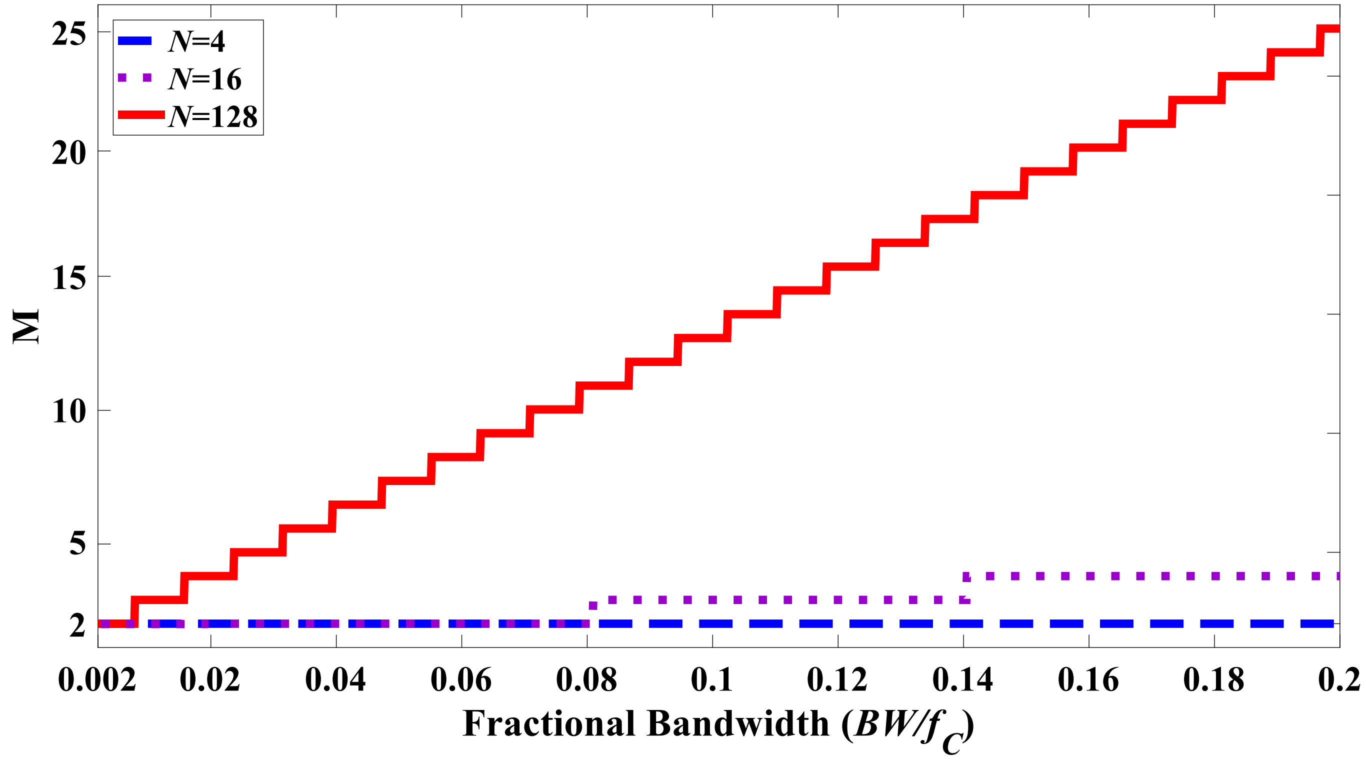
Discrete-time Delay Compensating Arch.

Hybrid Beamforming



- ❖Dividing the large array into smaller sub-arrays
- ❖Relaxing sub-array’s analog requirement
- ❖Energy-efficient compared to digital beamformer
- ❖Higher latency
- ❖Can the TTD-element be used towards decreasing this latency?

Parametric Modeling of TTD Beamformers



$$\Delta t_{max} = (N-1)\cdot\Delta t|_{\theta=\pm 60} = \frac{\sqrt{3}}{2}\cdot(N-1)\cdot\frac{d}{\lambda_C}\cdot\frac{1}{f_C}$$

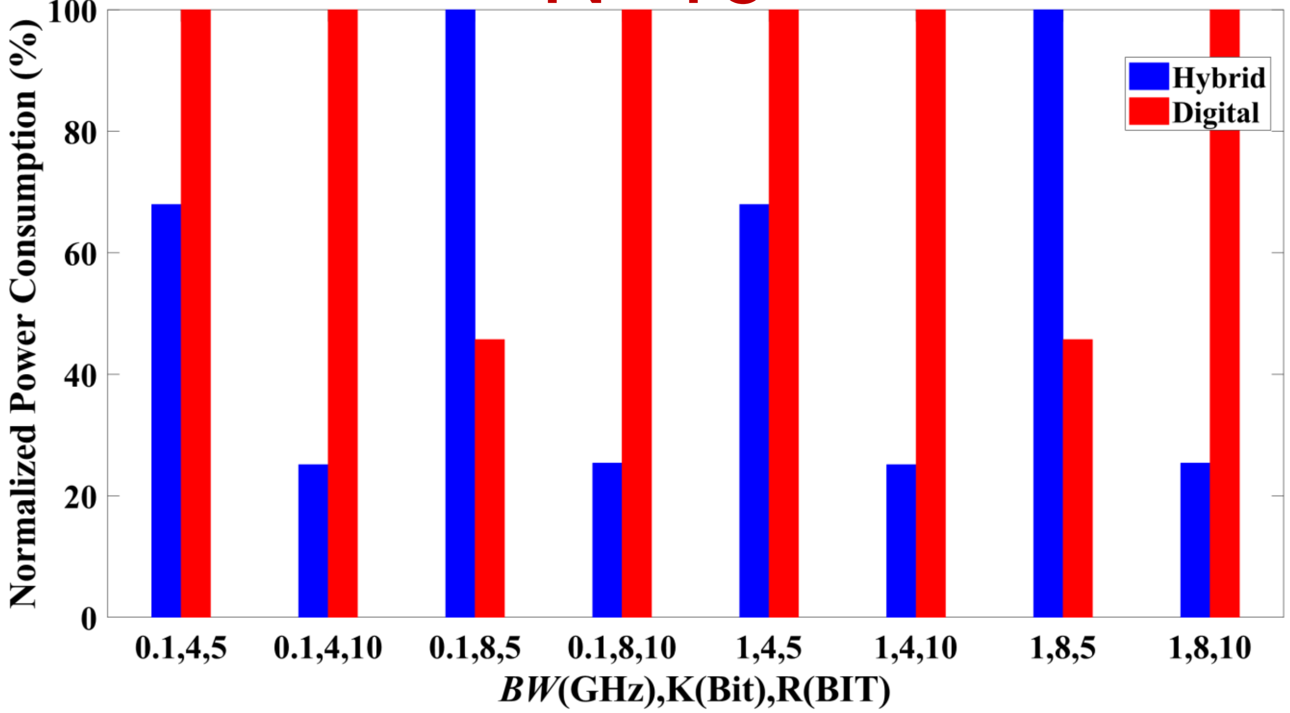
$$T_{C-max} = (M-1)\cdot T_S = (M-1)/f_S$$

$$M \geq 1 + \left(\frac{d}{\lambda_C/2}\right)\cdot\frac{\sqrt{3}}{2}\cdot(N-1)\cdot\left(\frac{BW}{f_C}\right)$$

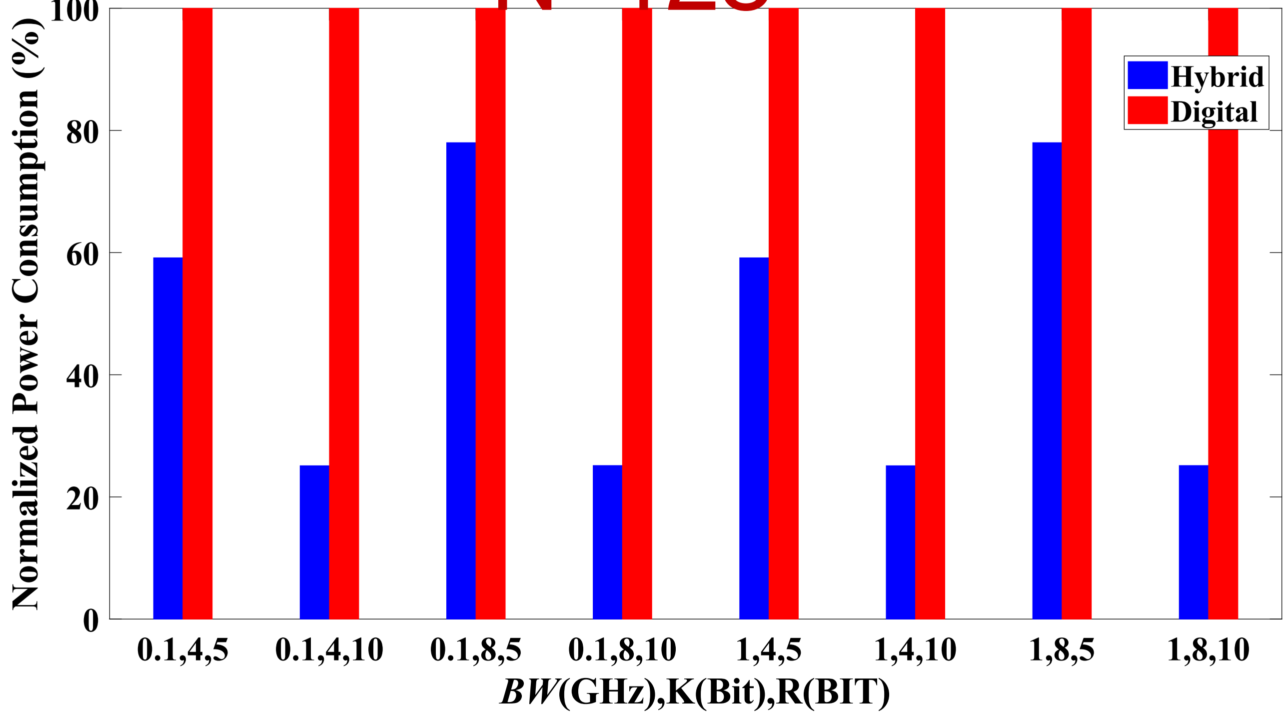
- ❖ Parameterize:
  - ❑ delay between first and last antennas,
  - ❑ fractional bandwidth,
  - ❑ # of interleaving levels,
  - ❑ ADC/PI resolution,
  - ❑ area and power consumption
- ❖ ±90° coverage
- ❖ M-levels of interleaving
- ❖ Conform to Nyquist sampling

Parametric Modeling of TTD Beamformers

N=16



N=128



- ❖R-bit ADC, K-bit phase interpolation
- ❖Larger arrays or moderate to high ADC resolution: Hybrid
- ❖Smaller arrays or lower ADC resolution: Digital

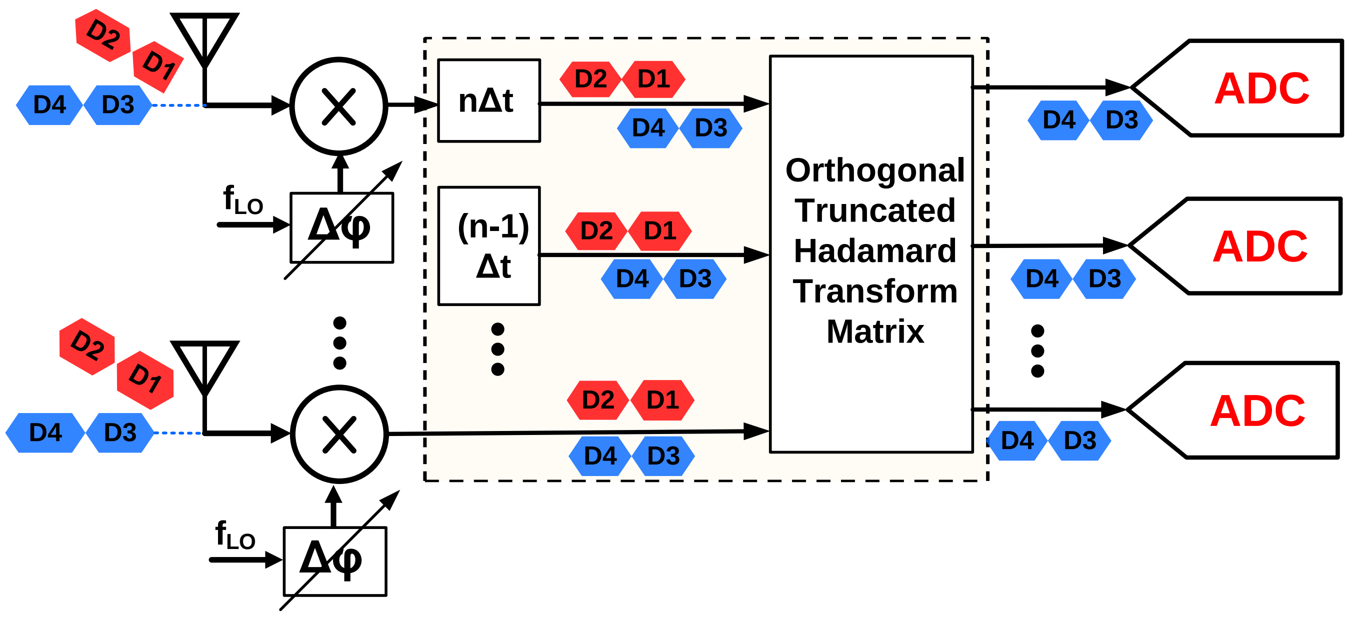
$$P_{PI,8\text{-bit}} = 44\text{mW} / 200\text{ MHz}$$
$$P_{ADC,5\text{-bit}} = 1.2\text{mW} / 250\text{ MHz}$$
$$P_{OTA} = 3\text{mW}/100\text{MHz}$$

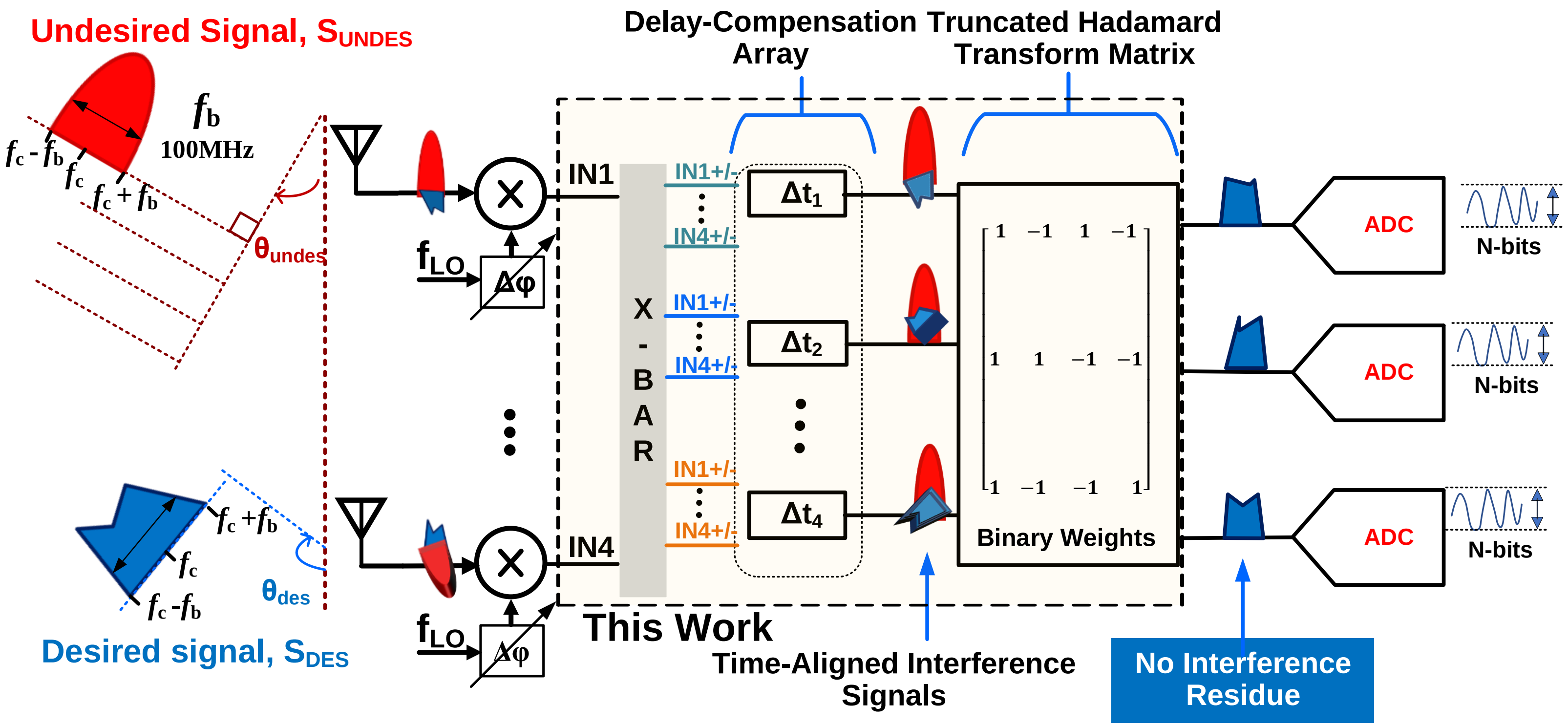
Outline

- ❖ Motivation
- ❖ Background
- ❖ Proposed Discrete-Time Delay-Compensation
  - ☐ True-time-delay beamforming for wide modulated BW and large arrays
  - ☐ Spatial interference cancellation with wideband NULL
- ❖ Conclusions

Spatial Interference Cancellation

SpICa: Proposed Architecture

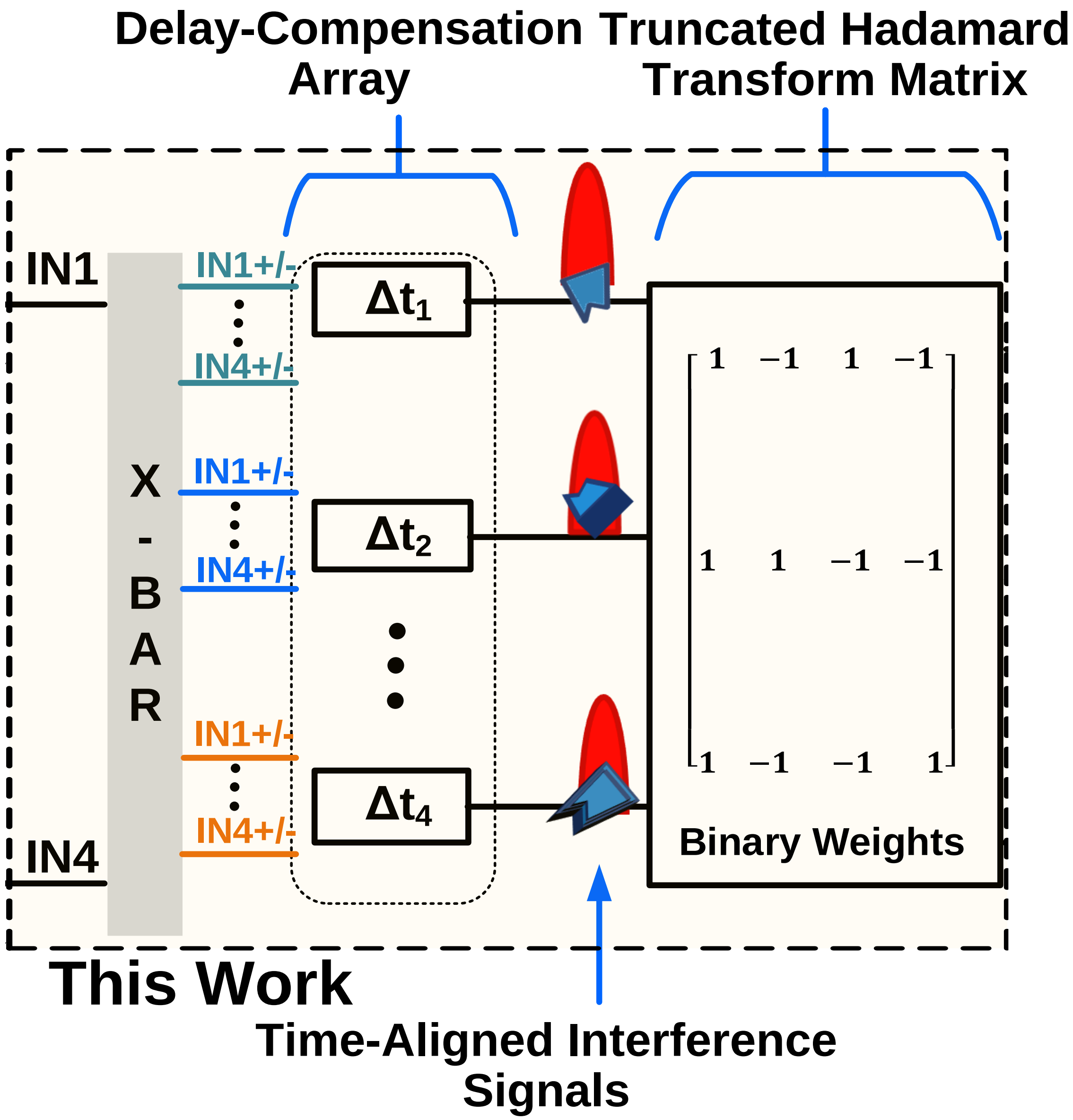




- Wideband interference cancellation
- Lower ADC dynamic range → power consumption
- Easy Hadamard Matrix implementation using differential solution
- Higher clocking power

SpICa: Concept

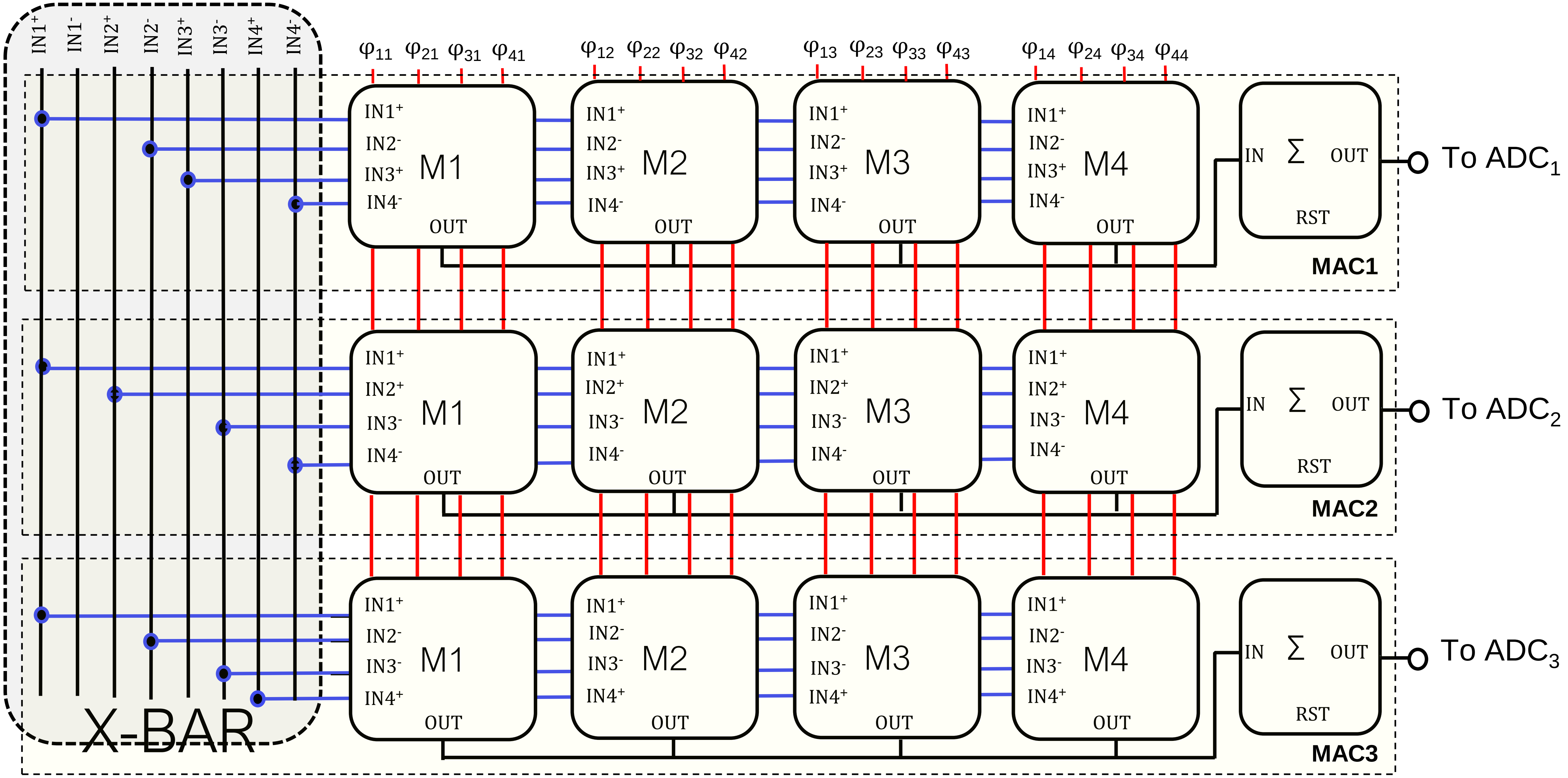
Truncated Hadamard Transform Matrix



- ❖Identical to Hadamard Transform with first row (all 1's) deleted
- ❖Comprises only +1, -1
- ❖N-1 outputs
- ❖Differential implementation requires NO extra hardware
- ❖Scalable

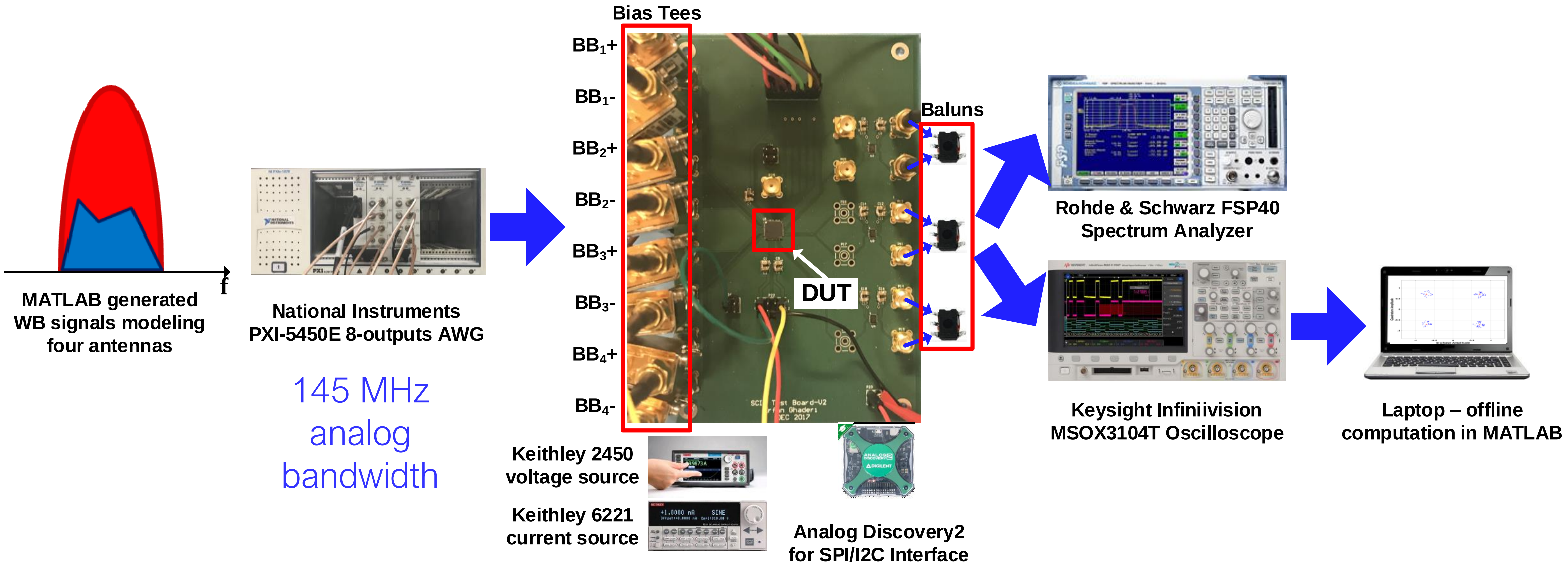
SpICa: Circuits

Proposed Multiply-Accumulate (MAC)



Discrete-time Delay Compensating Arch.

Test Setup



MATLAB generated WB signals modeling four antennas

National Instruments PXI-5450E 8-outputs AWG

145 MHz analog bandwidth

Keithley 2450 voltage source

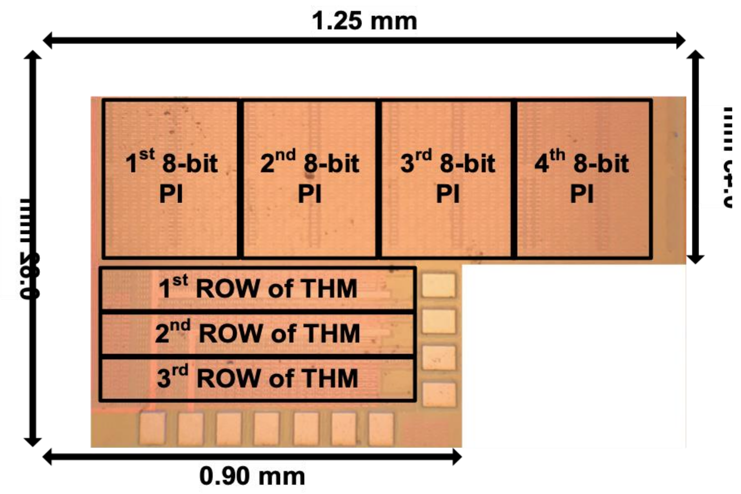
Keithley 6221 current source

Analog Discovery2 for SPI/I2C Interface

Rohde & Schwarz FSP40 Spectrum Analyzer

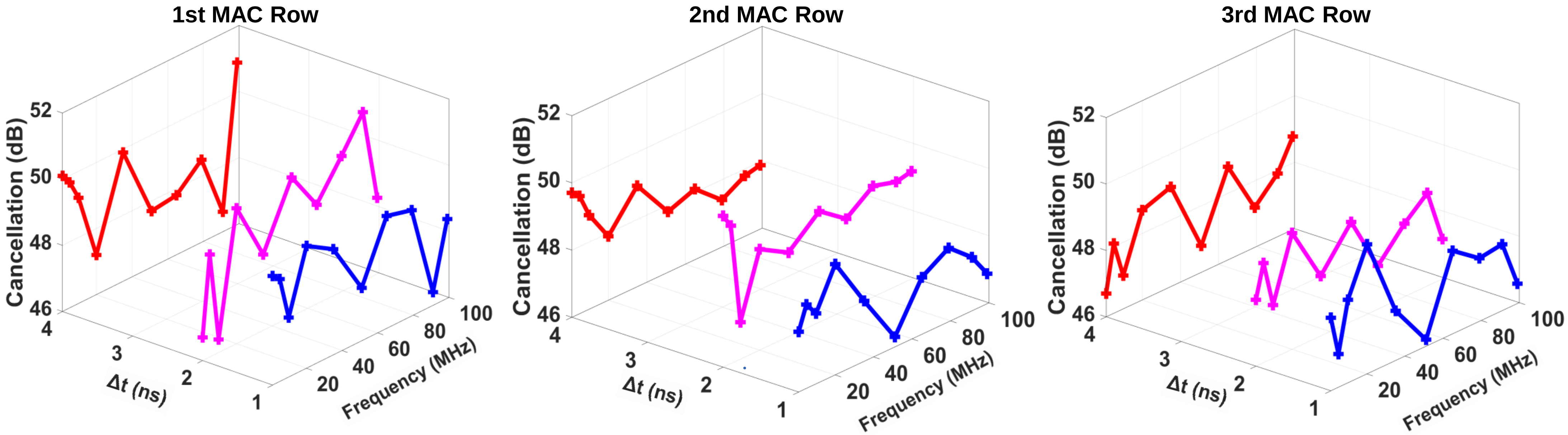
Keysight Infiniivision MSOX3104T Oscilloscope

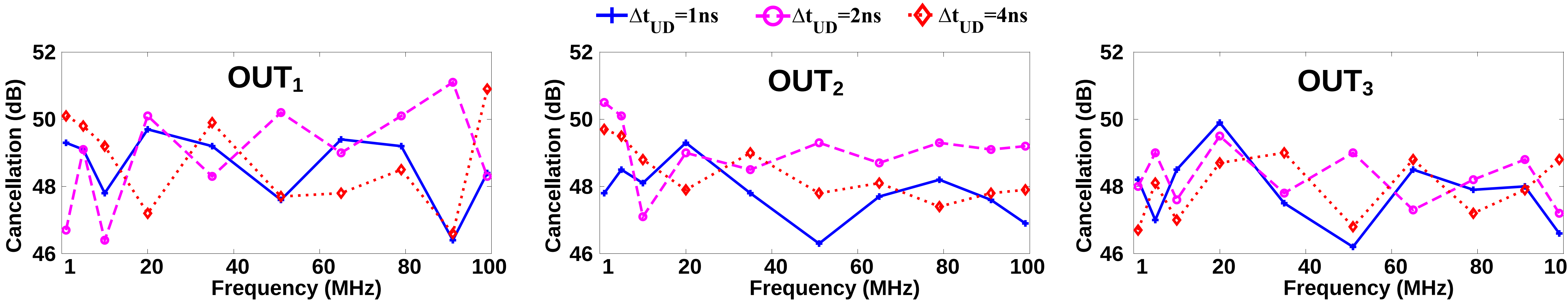
Laptop – offline computation in MATLAB



SpICa: Measurement Results

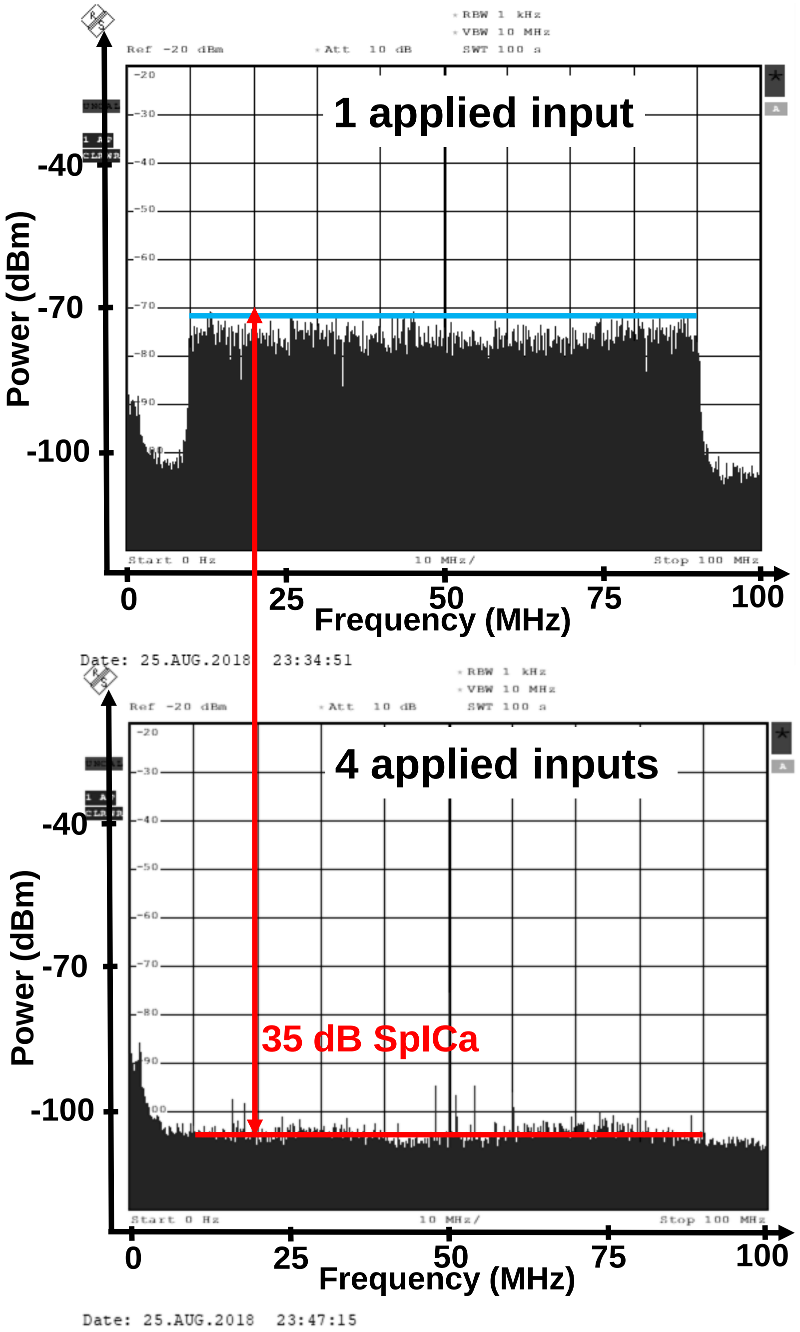
SpICa for Single-tone Input from 1 to 100MHz for varying Δt_d

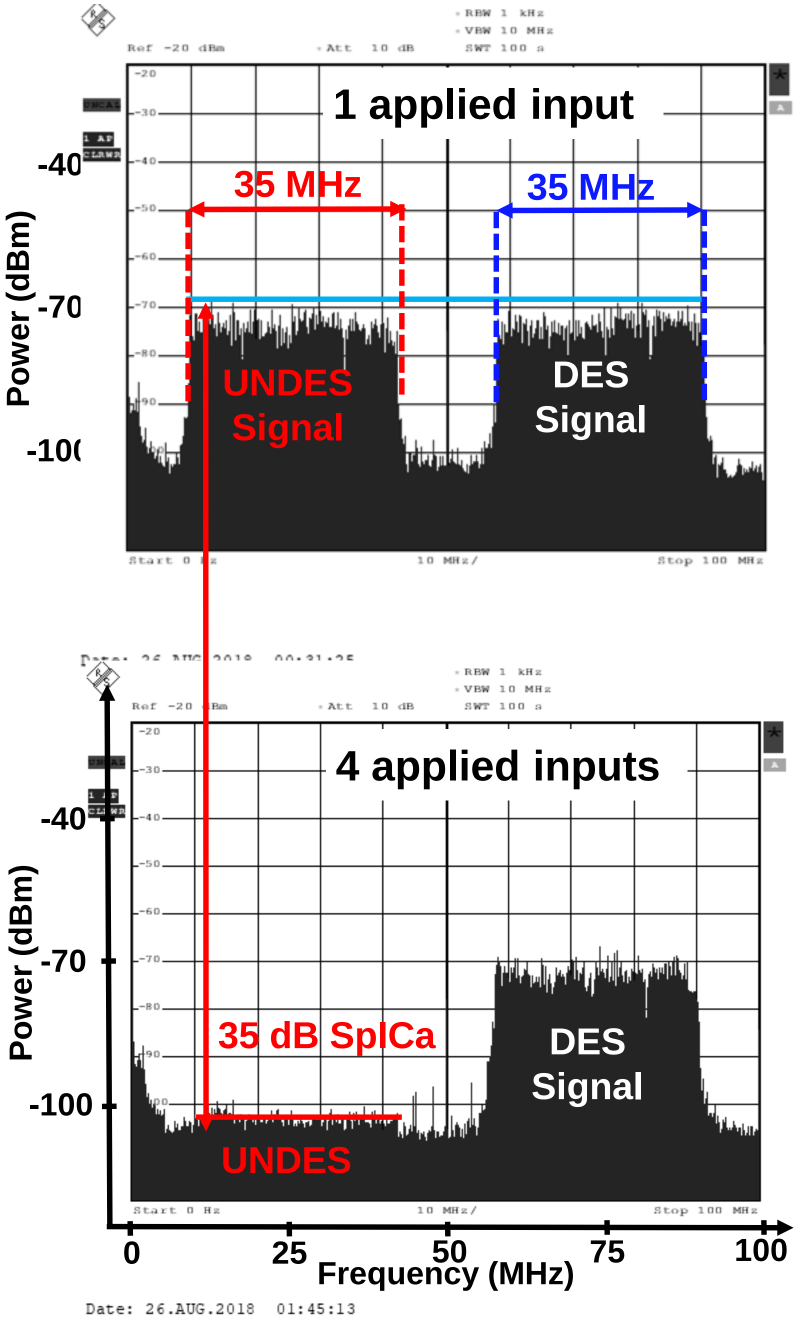


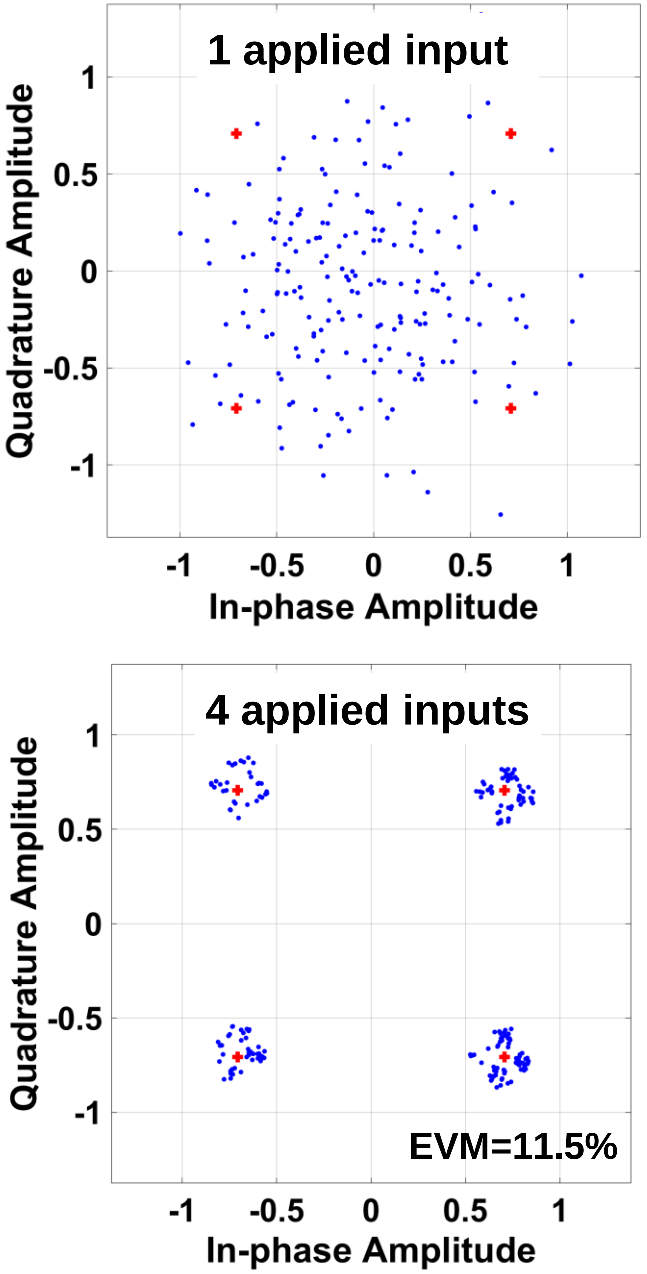


SpICa: Measurement Results

Modulated BW Interference Cancellation







SpICa: Comparison with state of the art

		JSSC2017 [3]	ISSCC2019 [4]	RFIC2016 [6]	ISSCC2013 [7]	ISSCC2017 [8]	**This Work**
# Elements		4 inputs, 4 outputs	4 inputs, 4 outputs	4 input, 1 output	4 inputs, 1 output	8 inputs, 8 outputs	**4 inputs, 3 outputs**
Tech. (nm)		CMOS 65	CMOS SOI 45	CMOS 65	CMOS 65	CMOS 65	**CMOS 65**
VDD (V)		1.2	NR	1.3-1.5	1.2	1.2	**1.0**
Resolution (Amp/Phase)		Phase: 6.5-b (3.8°) Amp: 3.9-b	NR	6-b I/Q	Phase: 3-b	14-b	**8-b (5ps) Overall delay range: 15ns**
BB Power		Not Available (RF+BB implementation)	Not Applicable (RF only implementation)	Not Applicable (RF only implementation)	36mW/40MHz[1]	91mW/350kHz	**Analog: 8mW Clock: 44mW Total: 52mW**
Area (mm^2)		2.25	23.4	3.8	2.25	3.24	**0.9**
P_{IN1dB}[2] (dBm)		Not Available	-27.3[3]	Not Available	-5[3]	Not Available	**4.7[3]**
P_{IIP3}[2] (dBm)		-29[3, 4, 5]	-15[4,6]	Not Available	0-2.6	Not Available	**10.6**
Noise Performance		3.4-5.8 dB[5] (Noise Figure)	4.3-6.3 dB (Noise Figure)	9.5 dB[5] (Noise Figure)	3-6 dB (Noise Figure)	Not Available	**330 μV_{rms} (Output-referred)**
SpICa Frequency		0.3-0.7GHz	900MHz @28GHz	100MHz @10GHz	40MHz @2.4GHz	350kHz	**1-100MHz**
NB-SpICa[7]	Cancellation (dB)	20	50-62	20	< 38	84	**46-51**
	Range (MHz)	320	900[9]	100	40	0.35	**99**
Modulated -SpICa	Cancellation (dB)	–	20[8]	–	–	Not Available	**>35**
	BW		500 MHz[10]			135 kHz	**80 MHz**

Outline

- Motivation
- Background
- Preliminary Work
  - ☐ True-time-delay beamforming for wide modulated BW and large arrays
  - ☐ Spatial interference cancellation with wideband NULL
- Conclusions

Conclusions

- ❖Demonstrated digitally-tunable delay-compensating technique with 5ps resolution and 15ns range for precision beamforming.
- ❖ SpICa with wideband null covering 100% fractional BW
- ❖Frequency-independent gain over a bandwidth of 100MHz (extended in ongoing works to 500MHz) with <50mW power consumption.
- ❖Future work will
  - ❑ Demonstrate discrete-time delay compensating technique for wide modulated bandwidths
  - ❑ Low-latency initial access
  - ❑ mmWave Testbed with closed-loop optimization for TTD arrays

Acknowledgements

- Graduate students at Systems-on-Chip and ARMAG Lab
- National Science Foundation (Award #1705026) for partial support
- Dr. Deuk Heo at WSU, Dr. Sudip Shekhar at UBC, Dr. Akbar Sayeed at UWisc
- Dr. Danijela Cabric, Han Yan, and Veljko at UCLA
- MOSIS and CMC for partial support in chip fabrication
- Xilinx for hardware donation
- Keysight and National Instruments for testbed support through university loan programs
- Cadence and Mentor for CAD support