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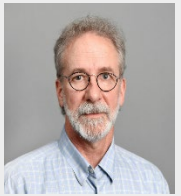
Virtual, November 23-25, 2020
CAS

Gs/s Analog-to-Digital Converters in sub-16nm Process Technologies



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NXP
SECURE CONNECTIONS FOR A SMARTER WORLD

- **The need for (and challenges of) Gs/s ADCs in sub-16nm process technologies**

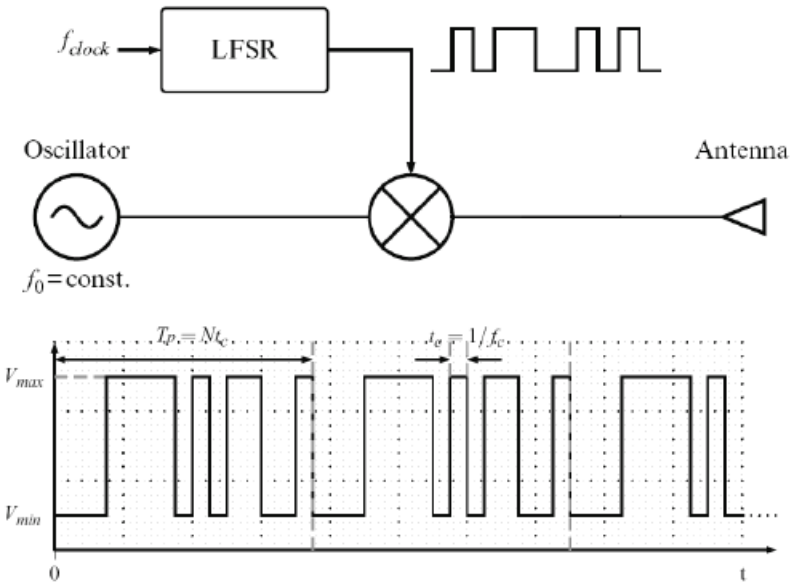
- **Status → where are we now? where to we need to go?**

- **Example implementatons**

Digitally Modulated Radar (DMR)

What is it?

- In a DMR-based automotive radar system, a (digital) Pseudo-Random Binary Sequence (PRBS) is used to modulate the phase of a (~79GHz) continuous-wave signal which is then transmitted as the range finding signal.
- The PRBS is designed to enable both unambiguous range (sequence length) and range resolution (pulse width → bandwidth) while also (potentially) providing excellent immunity to interference.
- The reflected signal is then received and processed (i.e. correlated and accumulated) to determine the range and velocity (FFT) of the target.



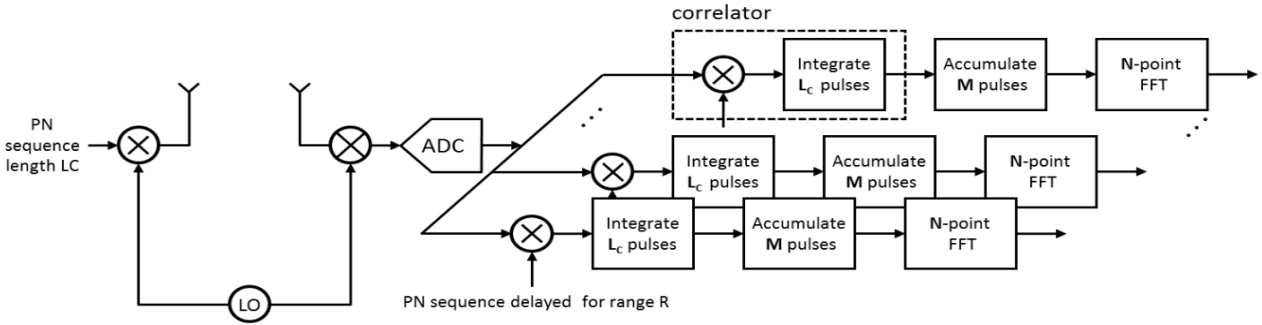
simplified DMR transmitter and PRBS diagrams*

*D. Guermandi, et al "A 79-GHz 2x2 MIMO PMCW Radar SOC in 28nm CMOS," IEEE JSSC, Oct. 2017

Digitally Modulated Radar (DMR)

Why is it good?

- Waveform generation is very simple → no fast-settling, highly-linear frequency synthesizers are required as with FMCW-based radar systems
- Since the PRBS codes that are used to modulate the carrier are designed to be essentially random and to have nearly perfect correlation properties, excellent range resolution and potential immunity to interference can be achieved.
- MIMO (Multiple-Input, Multiple-Output) and Beamforming techniques can be readily applied to a DMR-based system to improve range and angular resolution respectively.
- Receiver is predominantly digital (see diagram below) and requires extensive high-speed signal processing (e.g. correlator, accumulator, FFT, etc.), and provides significant (~70+dB) of processing gain and can also be readily implemented in a FinFET process technology.

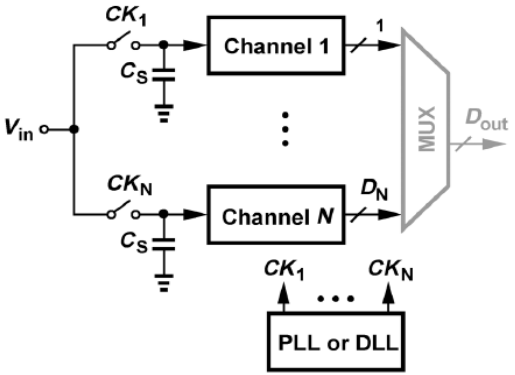


*D. Guermandi, et al "A 79-GHz 2x2 MIMO PMCW Radar SOC in 28nm CMOS," IEEE JSSC, Oct. 2017

Digitally Modulated Radar (DMR)

Is there a catch? (…there's always a catch)

- Since the achievable performance/accuracy of a DMR-based automotive radar is directly proportional to the bandwidth (more is better) of the range finding signals, the ADC that samples the received PRBS signals is required to have very-wide bandwidth (e.g. 2GHz to 5GHz depending upon the system requirements and implementation compared to 10MHz to 20MHz for a FMCW-based system) and correspondingly high sample rate (4Gs/s to 10Gs/s)…**but that's why DMR-based radars are so interesting!**
- A (~10-b) time-interleaved ADC architecture with associated clock issues (e.g. jitter, skew, etc.), low supply voltage, etc. will almost certainly be required…
- Because the Gs/s ADC output is correlated in real time with the PBRS that was used to modulate the 79GHz carrier phase, extremely high-speed (GHz) digital signal processing is also needed…



→ **<u>ADC and signal processing should both be implemented in the same sub-16nm technology!</u>**

- **The need for (and challenges of) Gs/s ADCs in sub-16nm process technologies**

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ADC benchmarking → background

- analog-to-digital converters (ADCs) are (almost) universally compared based upon figures of merit (FoM) of one kind or another.
- for high-speed ADCs, the most commonly used is the *Walden FoM (a.k.a. EQ)

$$EQ = \frac{P}{2^{ENOB}\, 2F_{BW}}$$

where P is power, ENOB is the effective number of bits, and F_{BW} is the input bandwidth

- EQ is essentially a measure of the energy per conversion step (in pico-Joules (pJ))

  → <u>lower is better for this FoM</u>

- the following charts plot EQ versus ENOB and EQ versus F_{BW} for a number of university designed ADCs and a number of industry designed ADCs

* R. H. Walden, “Analog-to-digital converter survey and analysis,” IEEE J. Sel. Areas Commun., Vol. 17, no. 4, pp. 530-550, 1999

…a word (or two) about FoMs for ADCs used in automotive applications:

critical ADC requirements in rank order (especially for automotive applications):

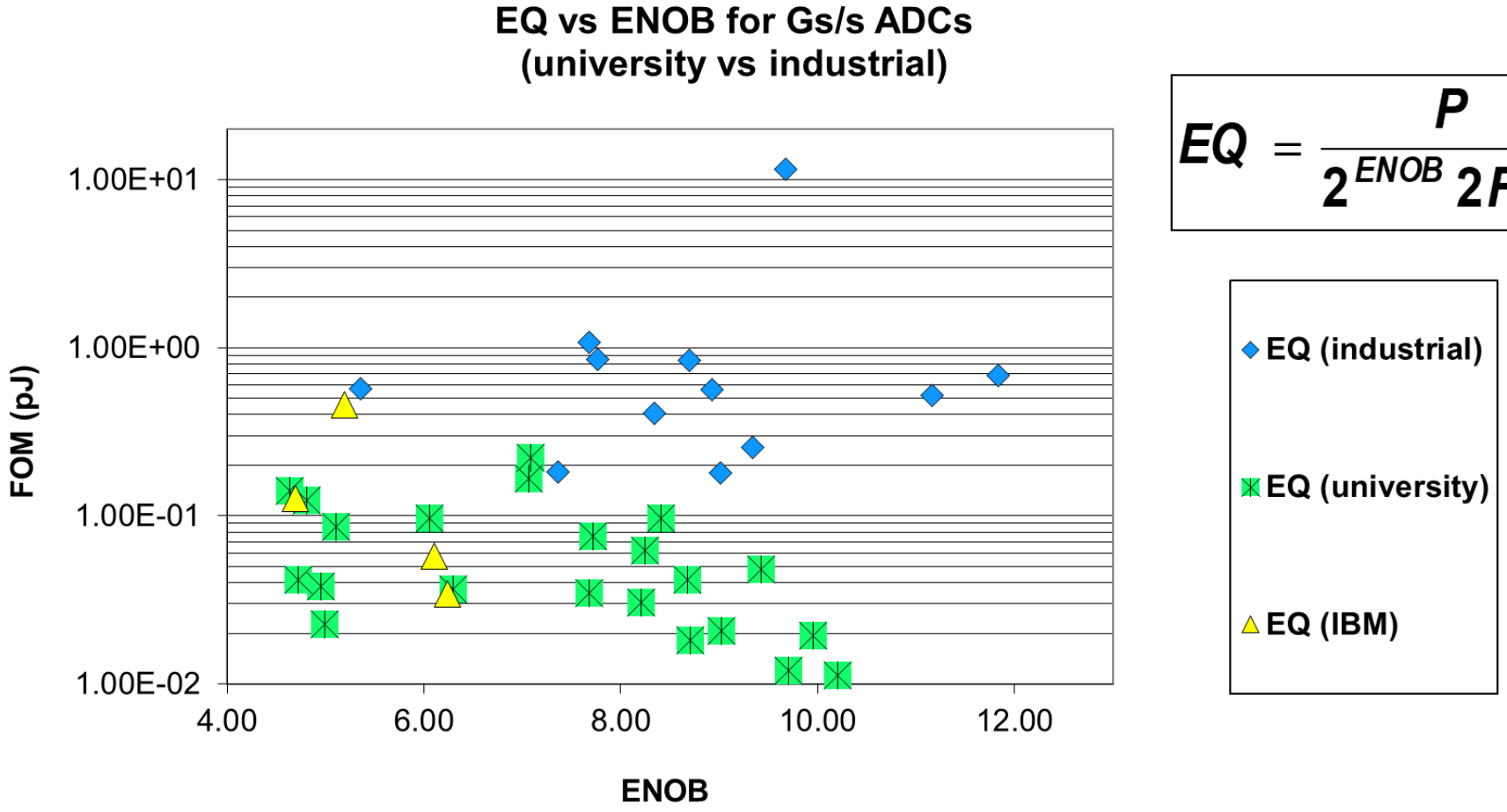
1. **does the ADC actually work as required in the application? (specifications like IFDR, OEV, ADV, etc. do NOT show up in an any FoM (EVER))**

2. **is the ADC manufacturable in high-volume production with automotive temperature ranges and reliability requirements?**

3. **is the ADC a cost effective solution for the application?**

→ if the first 3 requirements are met – then FoMs can be considered as a basis of ADC comparison

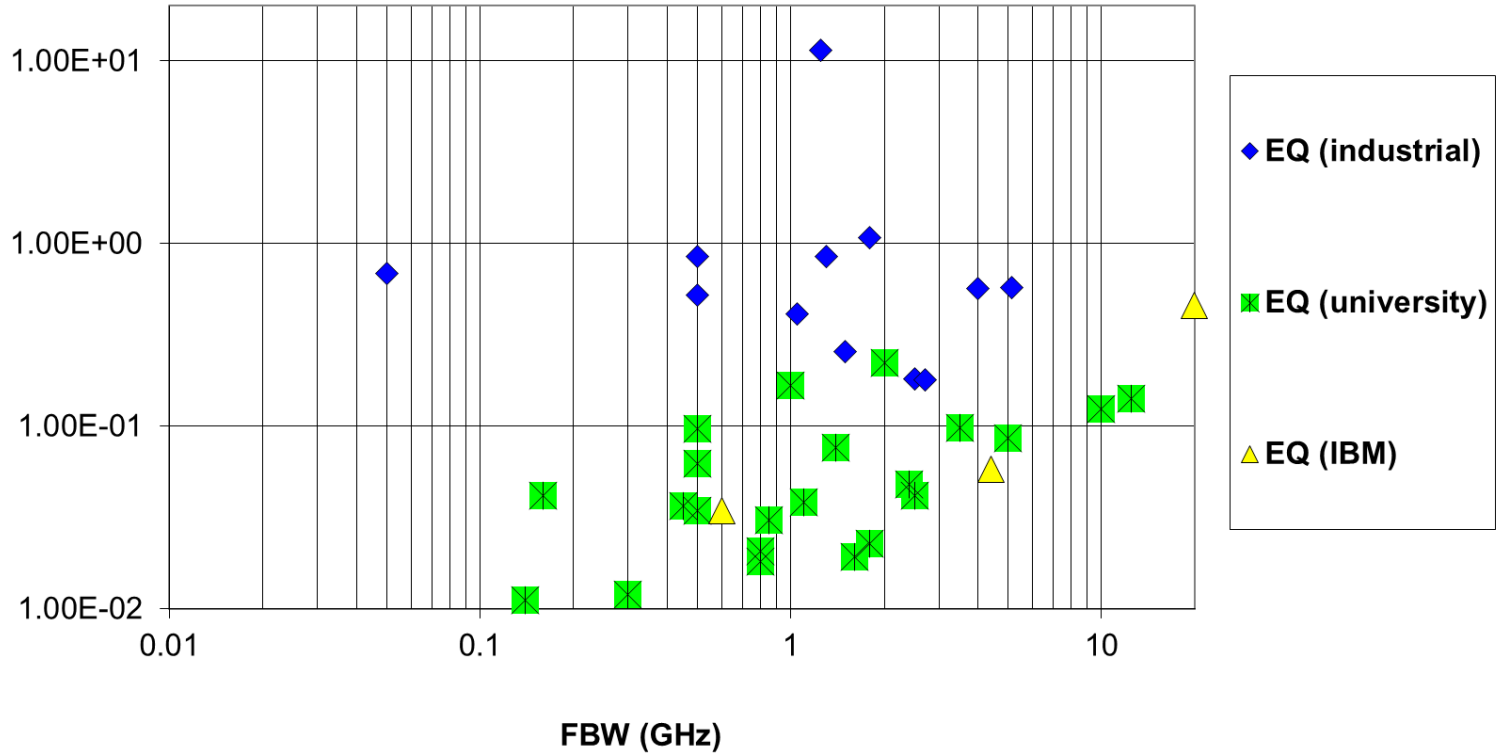
→ ADC performance is widely/aggressively published in the IEEE literature (i.e. ISSCC, VLSI Symposium, etc.)



$$EQ = \frac{P}{2^{ENOB}\, 2F_{BW}}$$

EQ vs F_{BW} for Gs/s ADCs (university vs. industrial)

$$EQ = \frac{P}{2^{ENOB}\, 2F_{BW}}$$



Summary/Concerns:

- Universities are producing overwhelming majority of the published Gs/s ADCs with the best FoMs

  but…
  - only 3 of the published ADCs shown have been implemented in 16nm and none in sub-16nm technologies
  - there are a few in 28nm, but most are 40nm or higher
  - universities focus primarily on FoM in order get their research published
- Industry needs sub-16nm Gs/s ADCs with specific application-based requirements (e.g. low cost, high-yield, IFDR, etc.) **and** excellent FoMs

  but…
  - from Marcel Pelgrom* "…industry contributions (to ISSCC) have dropped to 30%, and in absolute numbers, the 1974 level has been passed - in the downward direction"
  - Why? because industrial companies working on their own are typically more short-term financially driven and are usually not willing/able to invest sufficiently in long-term internal research

*Marcel Pelgrom, "Industry Research," IEEE Solid-State Circuits Magazine, Fall 2019

- **The need for (and challenges of) Gs/s ADCs in sub-16nm process technologies**

- **Status → where are we now? where to we need to go?**

- **<u>Example implementatons:</u>**
  - **time-interleaved**
  - **time-based**
  - **hybrid**

time-interleaved example*: 24 to 72Gs/s, 8-b ADC in 14-nm CMOS

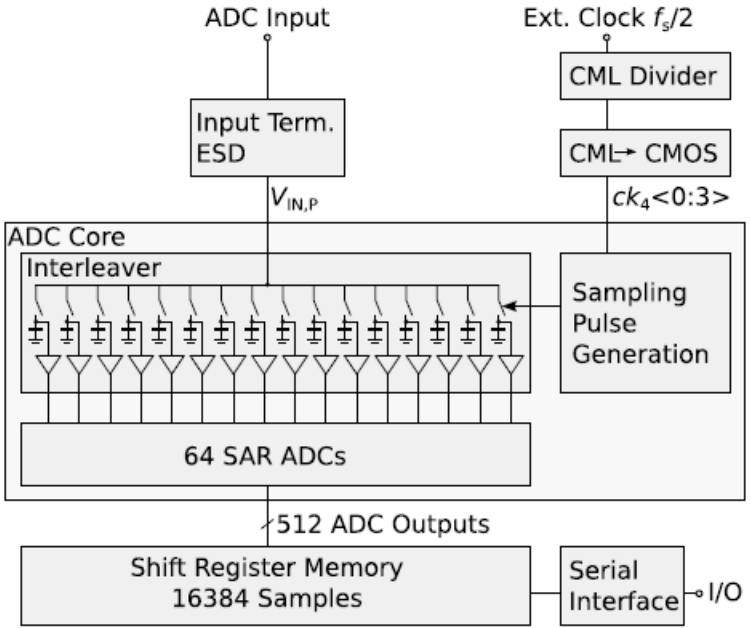


Fig. 1. ADC overview.

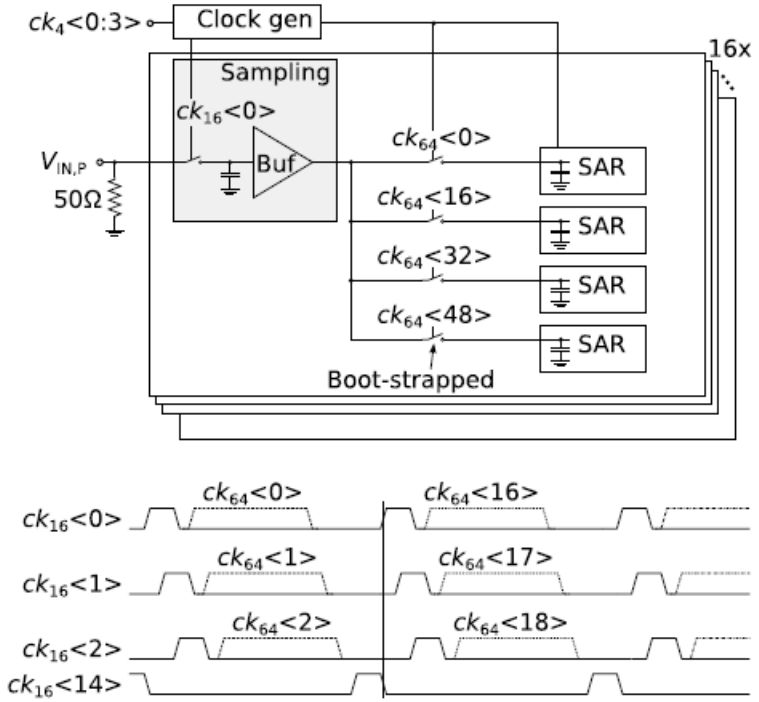


Fig. 2. Overview of the interleaver with input clock waveforms.

*L. Kull, et al, “A 24–72-GS/s 8-b Time-Interleaved SAR ADC With 2.0–3.3-pJ/Conversion and >30 dB SNDR at Nyquist in 14-nm CMOS FinFET, IEEE JSSC Dec. 2018

measured performance:

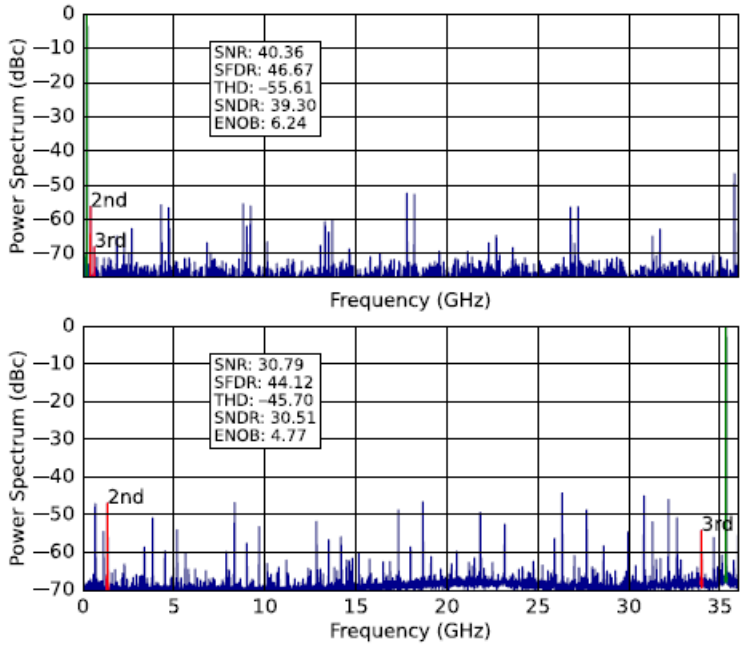


Fig. 15. Power spectrum density at low and high input frequencies, both measured at 72 GS/s.

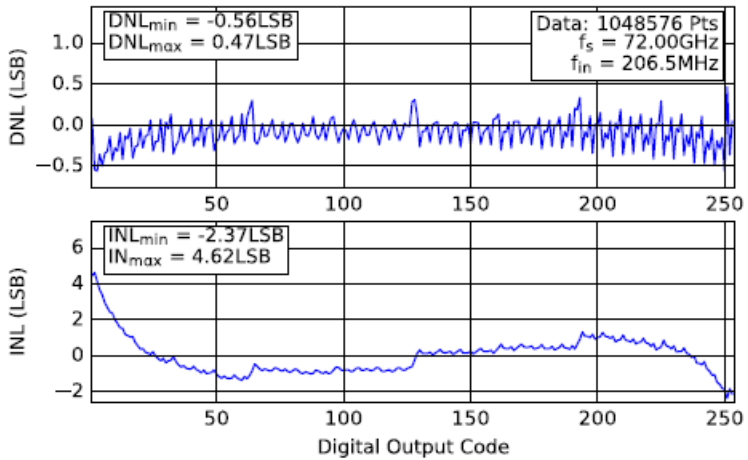


Fig. 16. INL and DNL.

*L. Kull, et al, “A 24–72-GS/s 8-b Time-Interleaved SAR ADC With 2.0–3.3-pJ/Conversion and >30 dB SNDR at Nyquist in 14-nm CMOS FinFET, IEEE JSSC Dec. 2018

time-based example*: 1Gs/s, 2.3mW, 8-b ADC in 65nm CMOS

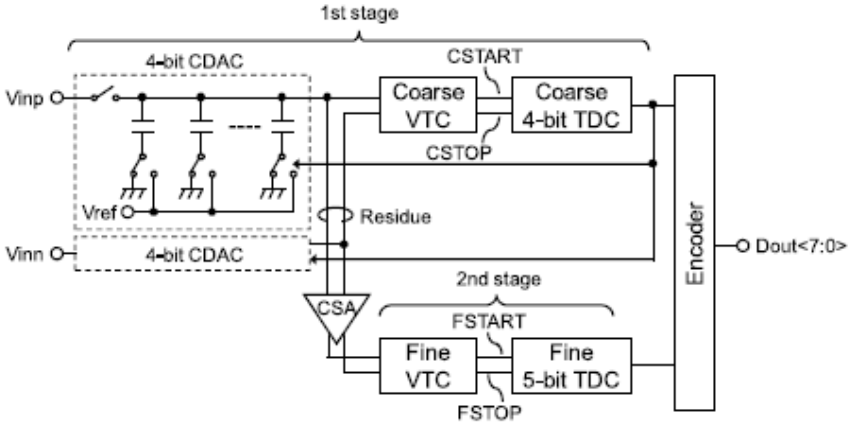
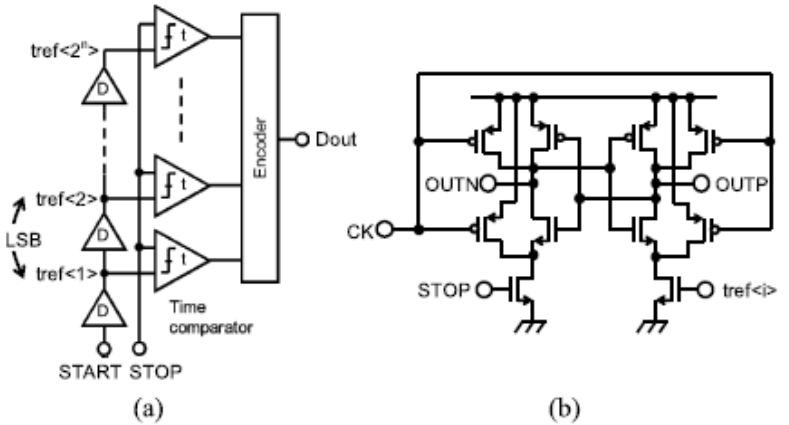


Fig. 6. Schematic of 8-bit fully time-based two-step ADC.



3. Schematic of (a) time-domain quantizer and (b) time comparator.

*K. Ohhata, “A 2.3-mW, 1-GHz, 8-bit Fully Time-Based Two-Step ADC Using a High-Linearity Dynamic VTC,” IEEE JSSC, July 2019

measured performance:

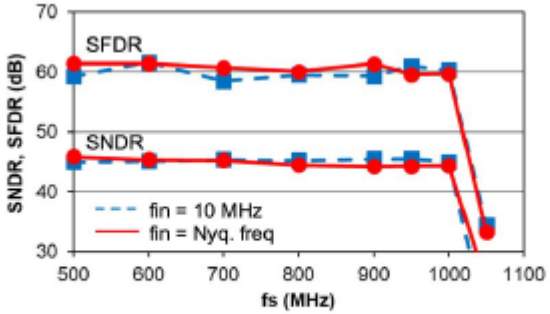


Fig. 29. Measured sampling frequency dependences of SNDR and SFDR.

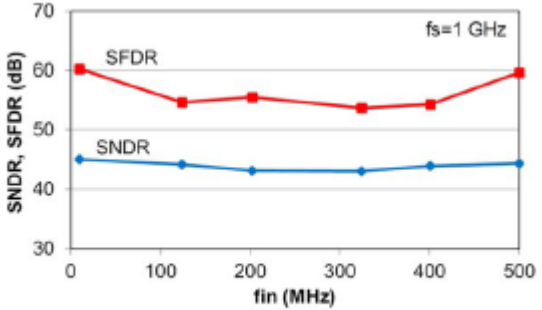
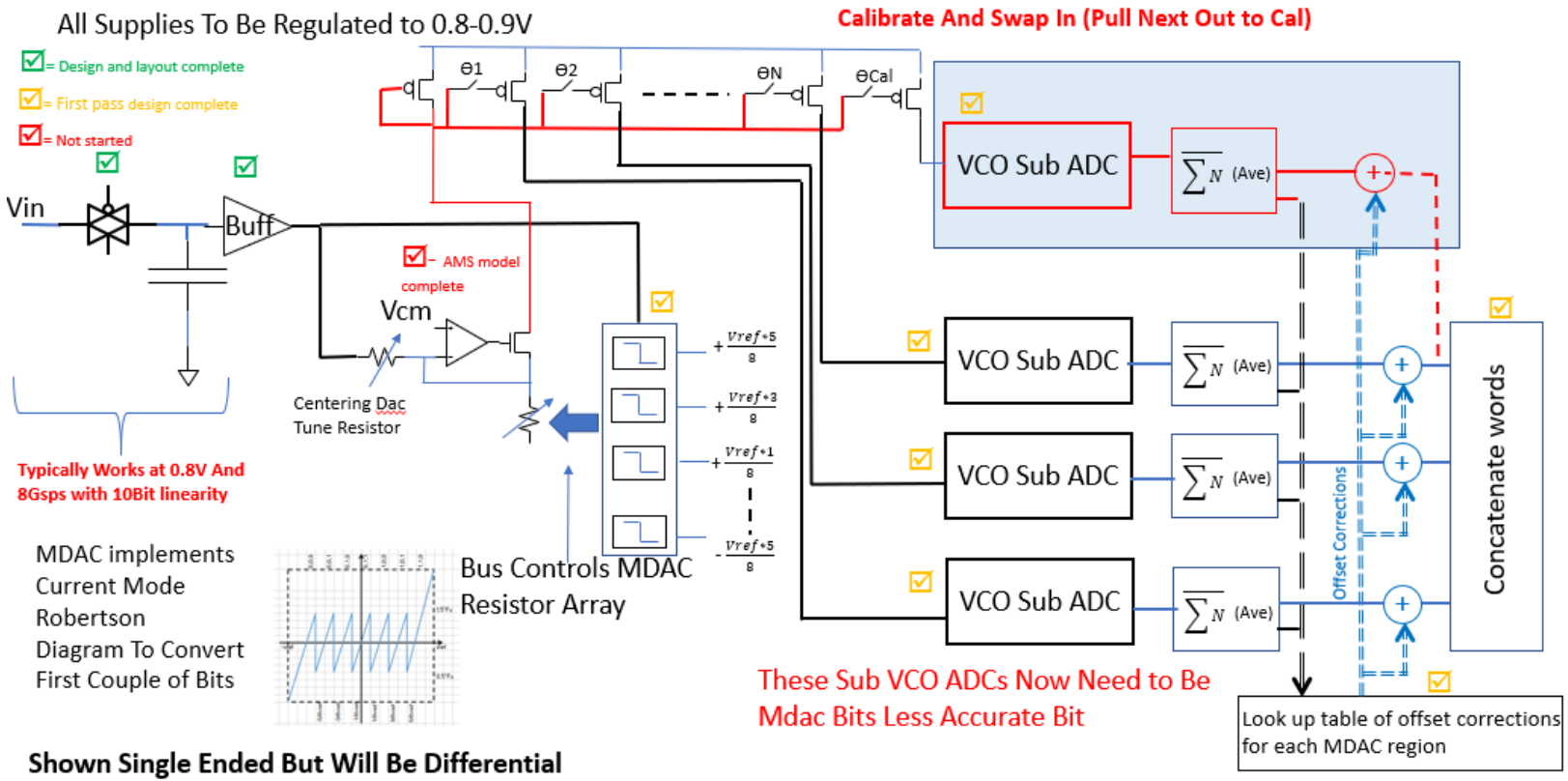


Fig. 30. Measured input frequency dependences of SNDR and SFDR.

*K. Ohhata, “A 2.3-mW, 1-GHz, 8-bit Fully Time-Based Two-Step ADC Using a High-Linearity Dynamic VTC,” IEEE JSSC, July 2019

*another possible approach…4-8Gs/s ADC in 16nm



*Braswell, Kunnen, MDAC Based Time-Interleaved Analog-to-Digital Converters and Related Methods, US patent #10,720,934

conclusions and recommendations:

- While progress is being made, there is still plenty of work to be done…
- Industry needs collaborate closely with university researchers through internal/external funding sources
- Industry needs to collaborate CLOSELY with the university researchers to ensure that the developed ADCs meet all requirements and NOT just FoMs
- Universities (and IEEE conferences) need to be willing to accept an ADC with possibly a slightly worse FoM but that actually works…
- Industry/other funding sources need to provide university researchers with regular/consistent access to sub-16nm process technologies