Reliability of scaled Metal Gate / High-K CMOS devices

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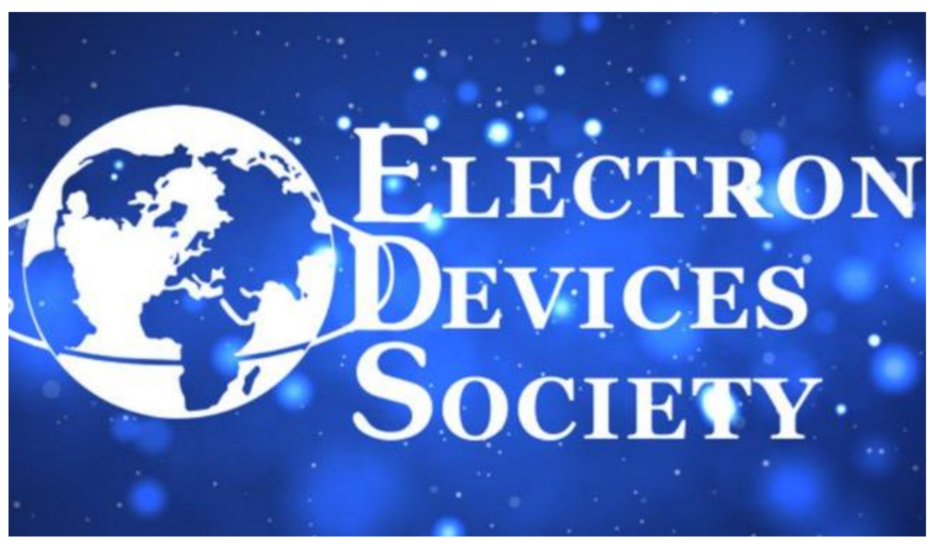

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- The opinions expressed in this lecture are my own and do not necessarily reflect the views of my employer, Intel Corp.

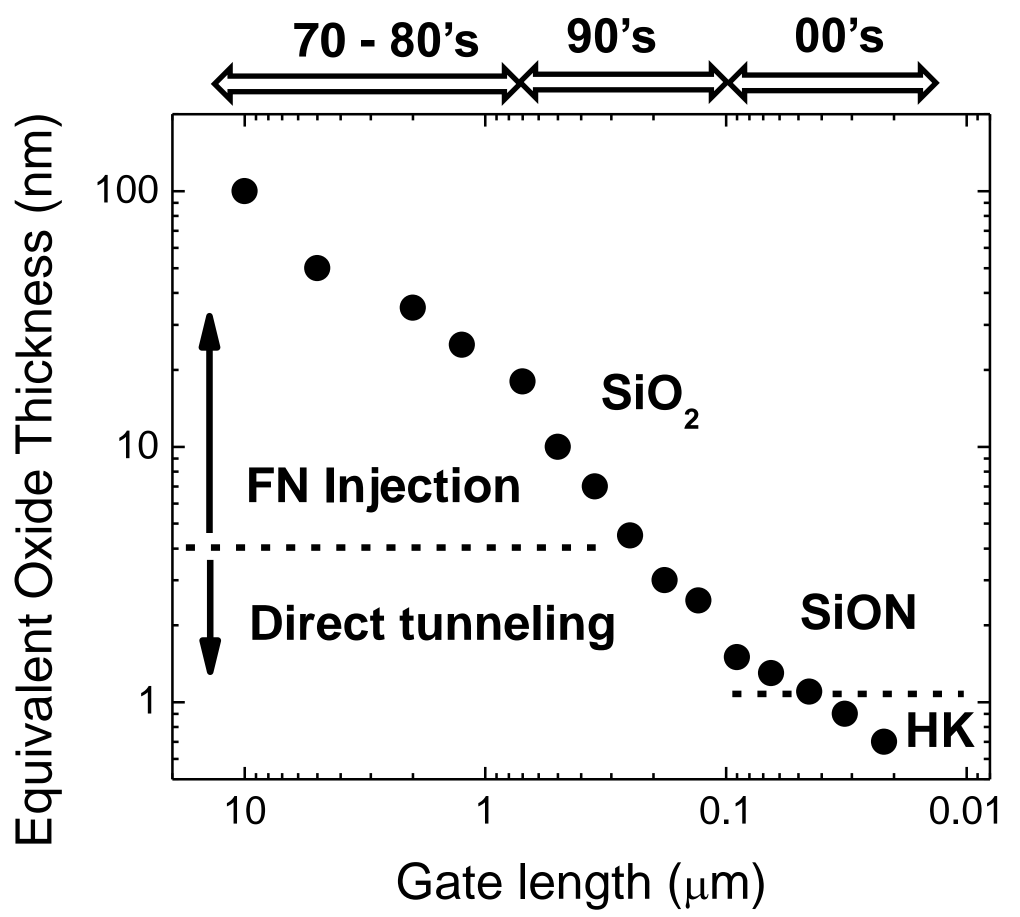
- The data presented in this lecture was collected and published during my employment with AMD & GLOBALFOUNDRIES

Brief history of semiconductor devices

- Dec 1947 invention of the point contact transistor by Shockley, Bardeen and Brattain at Bell Labs
  - Bipolar transistor went through various process improvements in the following years

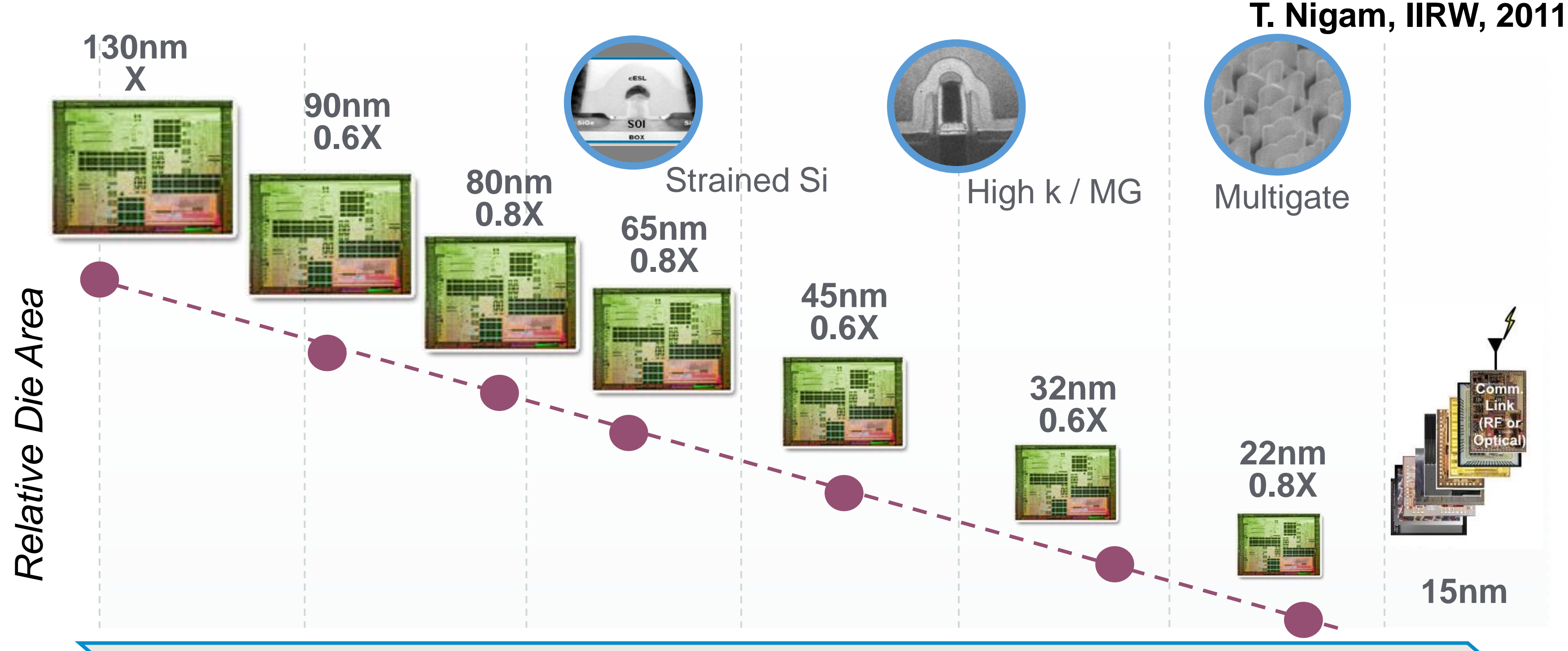
- MOSFET was proposed in 1925 by Lilienfeld and first demonstrated by Atalla and Kahng at Bell Labs in 1959
- In 1958 Kilby at TI invented the first integrated circuit which was followed shortly after by Noyce at Fairchild with a “true” monolithic IC

Motivation



- MOS Technologies successfully scaled since ~1970 following scaling laws introduced by R. Dennard
  - Feature sizes reduced from 10μm to <100nm
  - Equivalent Oxide thickness scaled to ~1nm
  - Dopant concentration increased for gate control
- Reduction in feature size and introduction of new materials presented challenges for characterization and modeling of advanced technology nodes

Technology Enablers for the last 2 decades



Lithography Enabled

- Density
- Power / Performance
- Cost

Materials Enabled

- Power / Performance
- Strained Silicon
- High K / Metal Gates
- Low-K

3D enabled

- Density
- Functionality
- Integration

Critical FEOL reliability challenges accompanying CMOS scaling

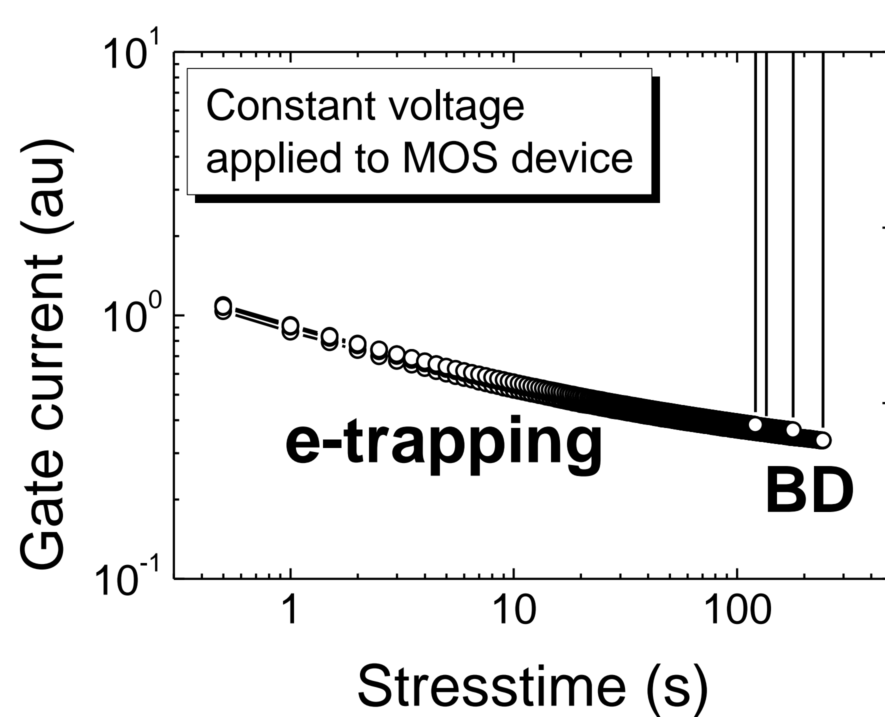
- Ionic contamination of the gate dielectric caused by alkali metals (Na, K)
  - Reducing contamination from tooling, process and handling
- Hot carrier challenges
  - Focusing on implant process and introduction of lightly doped drain (LDD) process
- Gate oxide scaling limitation
  - Reexamining the time dependent dielectric breakdown (TDDB) model leading to the introduction of the power law model
- Bias Temperature Instability
  - Minimizing impact of process (nitridation on NBTI, IL/HK thickness for PBTI in MG/HK technologies) and introduction of time resolved characterization
- Metal Gate / High-k reliability
  - Industry wide effort including research consortia's to address fundamental process and reliability challenges

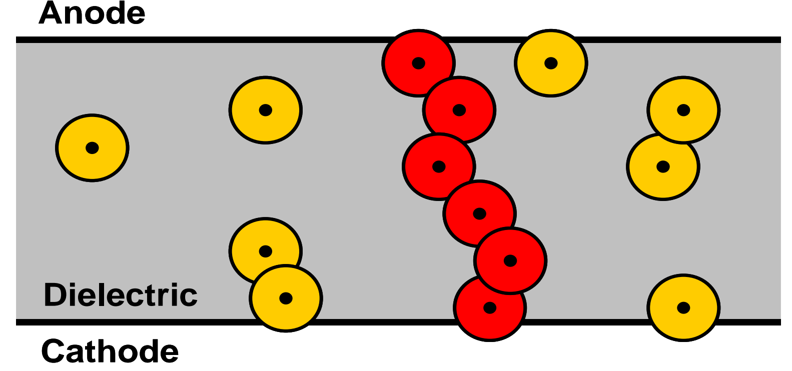
Outline

- Introduction
- Discrete device reliability
  - TDDB mechanism
  - BTI characterization
  - Summary
- Circuit reliability
  - Ring oscillator degradation
  - Summary
- Outlook

Dielectric breakdown in MOS devices

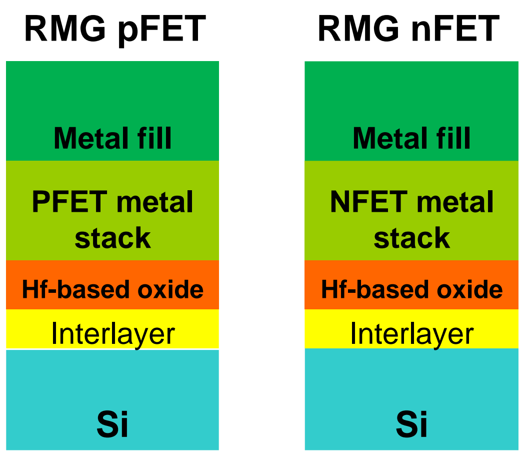
- **Definition:** Dielectric breakdown occurred when the dielectric has lost its insulating property
- Losing insulating property in a dielectric leads to a current increase when connected to a voltage source
- Breakdown is a statistical process and failure times are modeled using Weibull statistic (β, t63%)





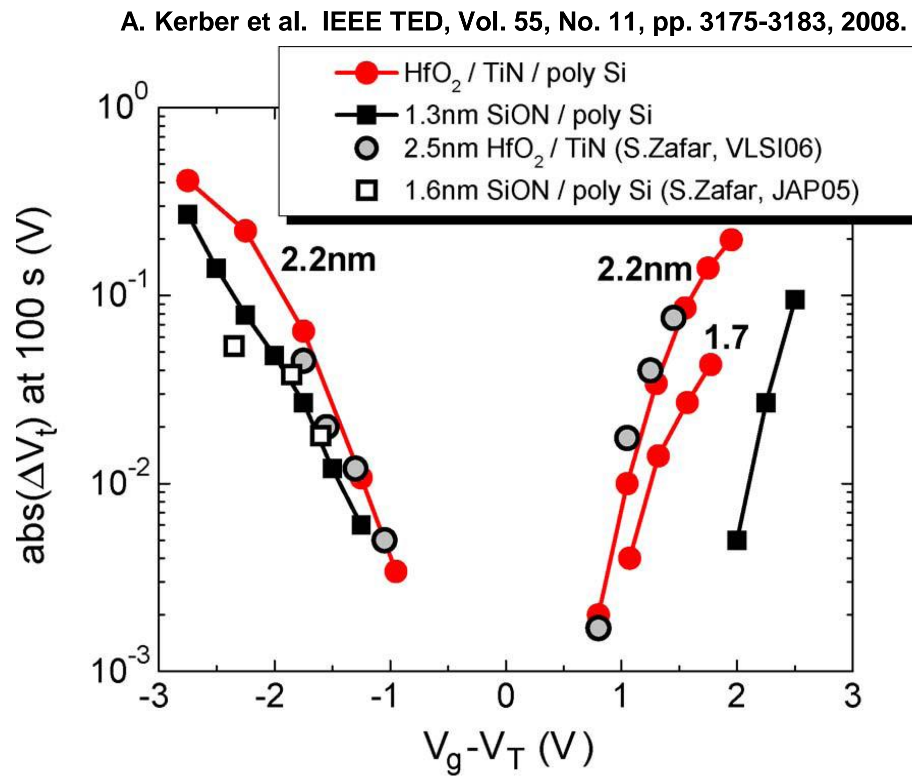
Bias Temperature Instability (BTI) CMOS devices

- The introduction of MG/HK into CMOS technologies added PBTI in nFETs as emerging device reliability mechanism in addition to NBTI in pFETs

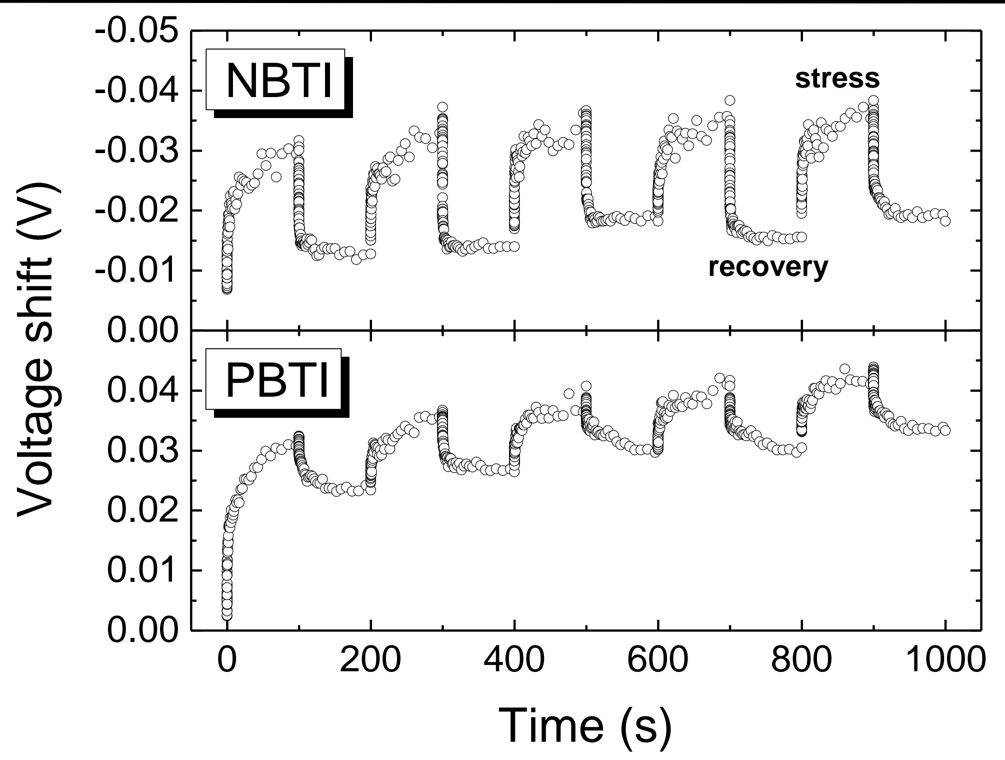


- The introduction of MG/HK did not require an adaption in BTI characterization methodology

A. Kerber et al. IEEE TED, Vol. 55, No. 11, pp. 3175-3183, 2008.



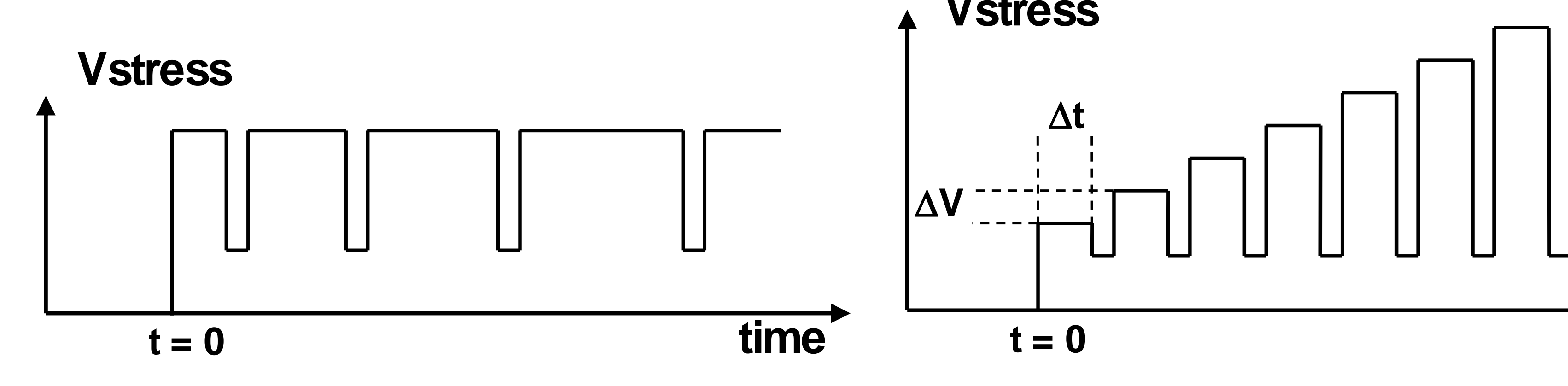
BTI recovery



G. Chen, et al. EDL, Vol. 23, No. 12, pp. 734-736, 2002.
S. Rangan, et al. IEDM, pp. 341–344, 2003.
B. Kaczer, et al., IRPS, pp. 381–387, 2005.
H. Reisinger, et al. IRPS, pp. 448–453, 2006.
A. Kerber, et al., IEEE TED Vol. 55, No. 11, pp. 3175, 2008.
K. Zhao, et al., IRPS, pp.50-54, 2010.

- BTI recovers when the stress bias is removed
- NBTI and PBTI show same qualitative features
- **What is the impact of recovery on logic CMOS circuit degradation?**

Method to assess reliability



TDDB

$$TBD_{CVS} = \frac{1}{RR}\left(\frac{1}{V_{CVS}}\right)^{n}\frac{VBD^{\,n+1}}{n+1}$$

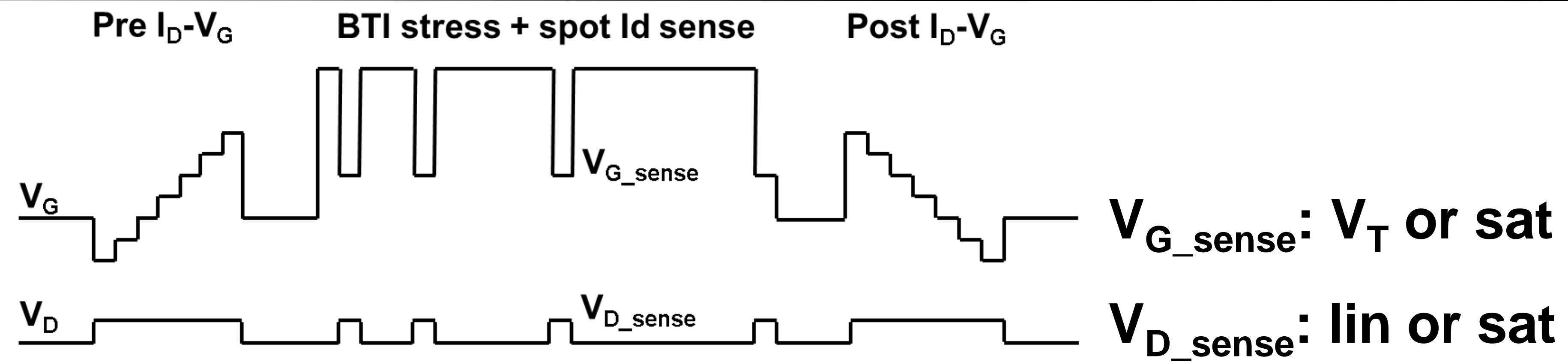
A. Kerber et al., Microelectronics Reliability, 2007.

BTI

$$\Delta V_T\left(t_{CVS}, V_{CVS}\right) = A \cdot t_{CVS}^{n} \cdot V_{CVS}^{m} \qquad \Delta V_T\left(RR_{VRS}, V_{VRS}^{\max}\right) = \frac{A}{\left(m/n+1\right)^{n}}\frac{{V_{VRS}^{\max}}^{m+n}}{RR_{VRS}^{n}}$$

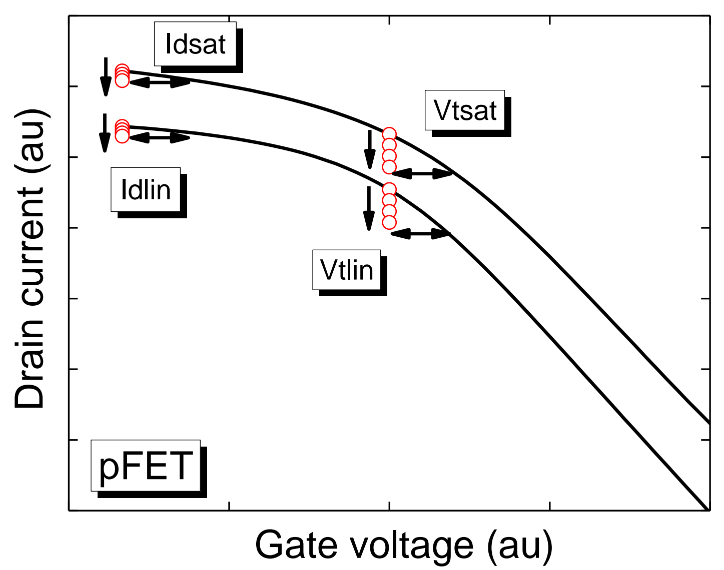
A. Kerber et al., IEEE EDL, 2009.

Fast BTI characterization



V_{G_sense}: V_T or sat

V_{D_sense}: lin or sat



Voltage shift through interpolation

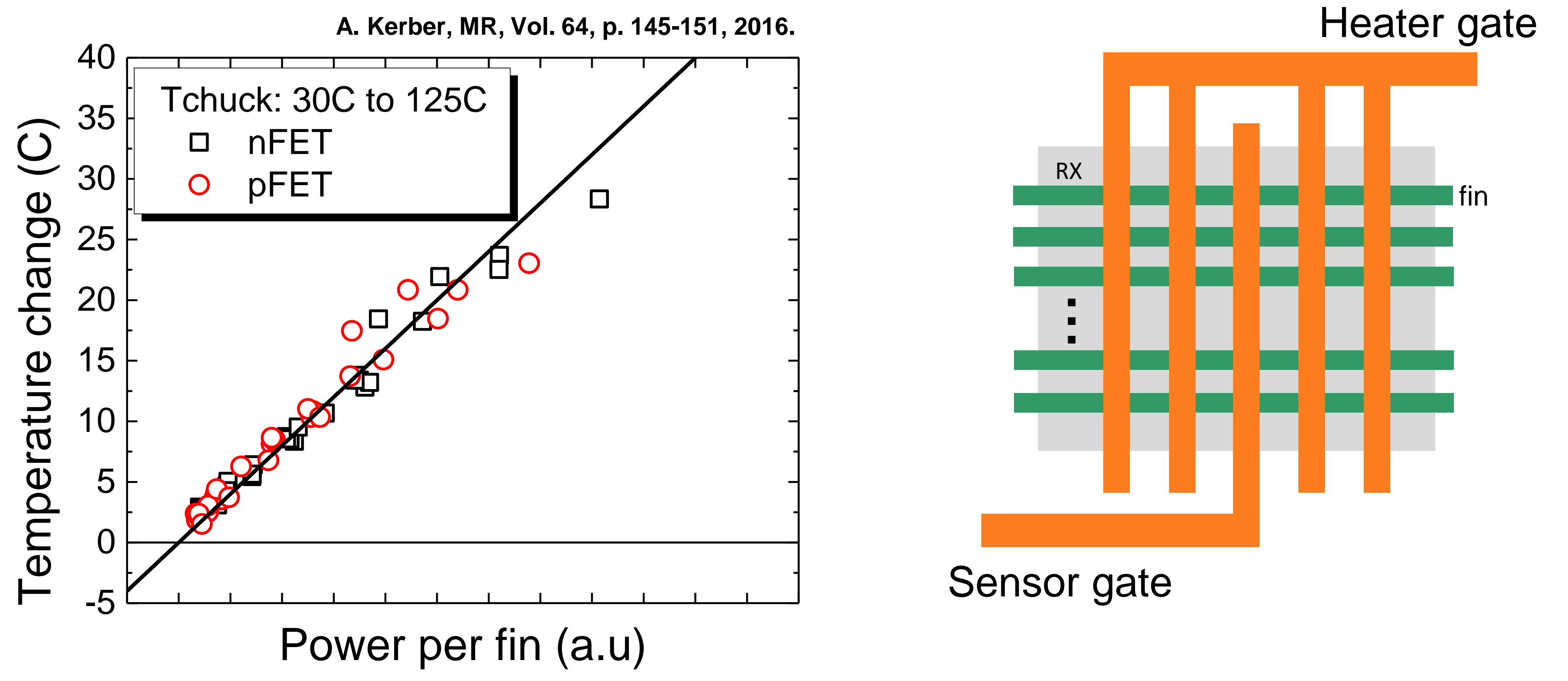
$$\Delta V = V_{G_sense} - V_G(i) + \left(I_D(i) - I_{D_sense}(t)\right) \cdot \frac{V_G(i) - V_G(i-1)}{I_D(i) - I_D(i-1)}$$

Sense current degradation

$$\Delta I_D = \frac{I_D(0) - I_D(t)}{I_D(0)}$$

Current degradation and voltage shift used as metric

Self heating characterization in bulk FinFET devices



1. Determine V_T (T) of MOSFET sensor by modulating chuck temperature
2. Measure V_T of MOSFET sensor without and with power dissipation in heater device
3. Determine ΔV_T and translate into ΔT and plot versus power per Fin in the heater

➔ **ΔT<30C covering typical HCI stress condition in 14nm bulk FinFETs**

➔ **Self-heating a growing concern for future nodes**

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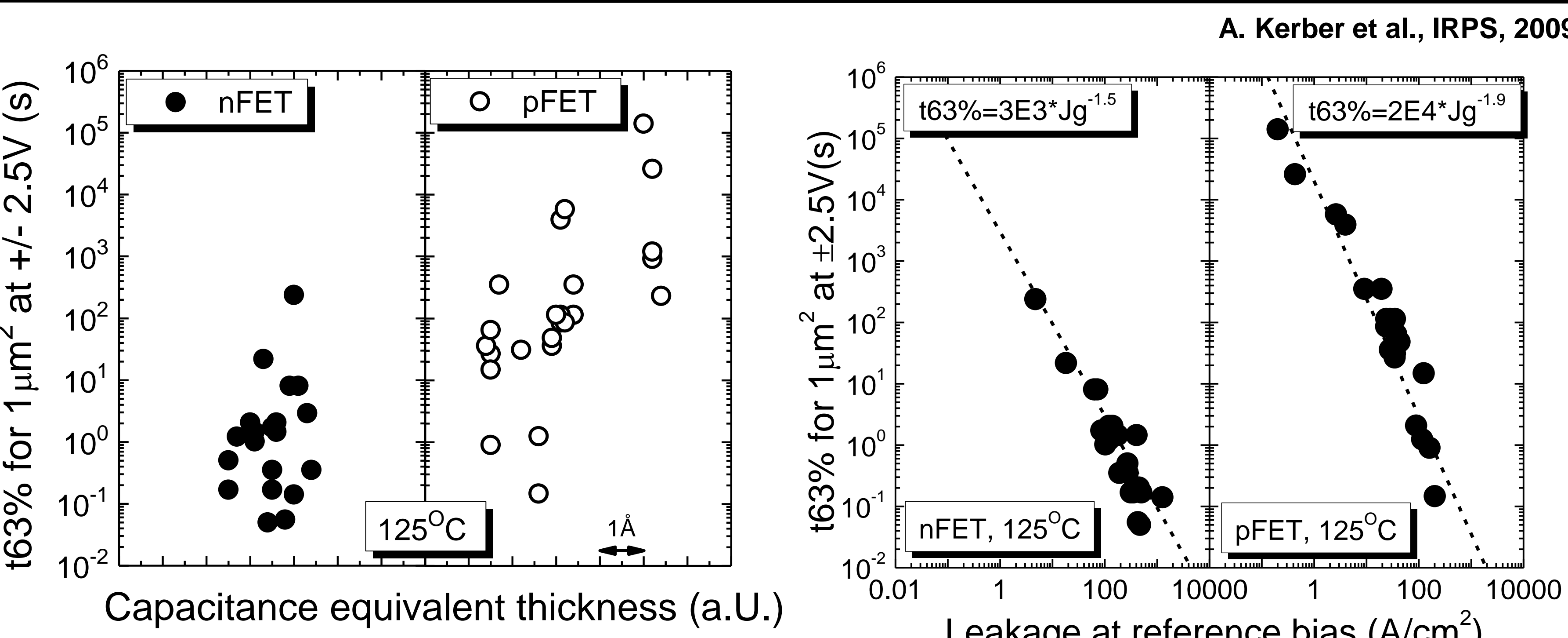
TDDB Figure of Merit

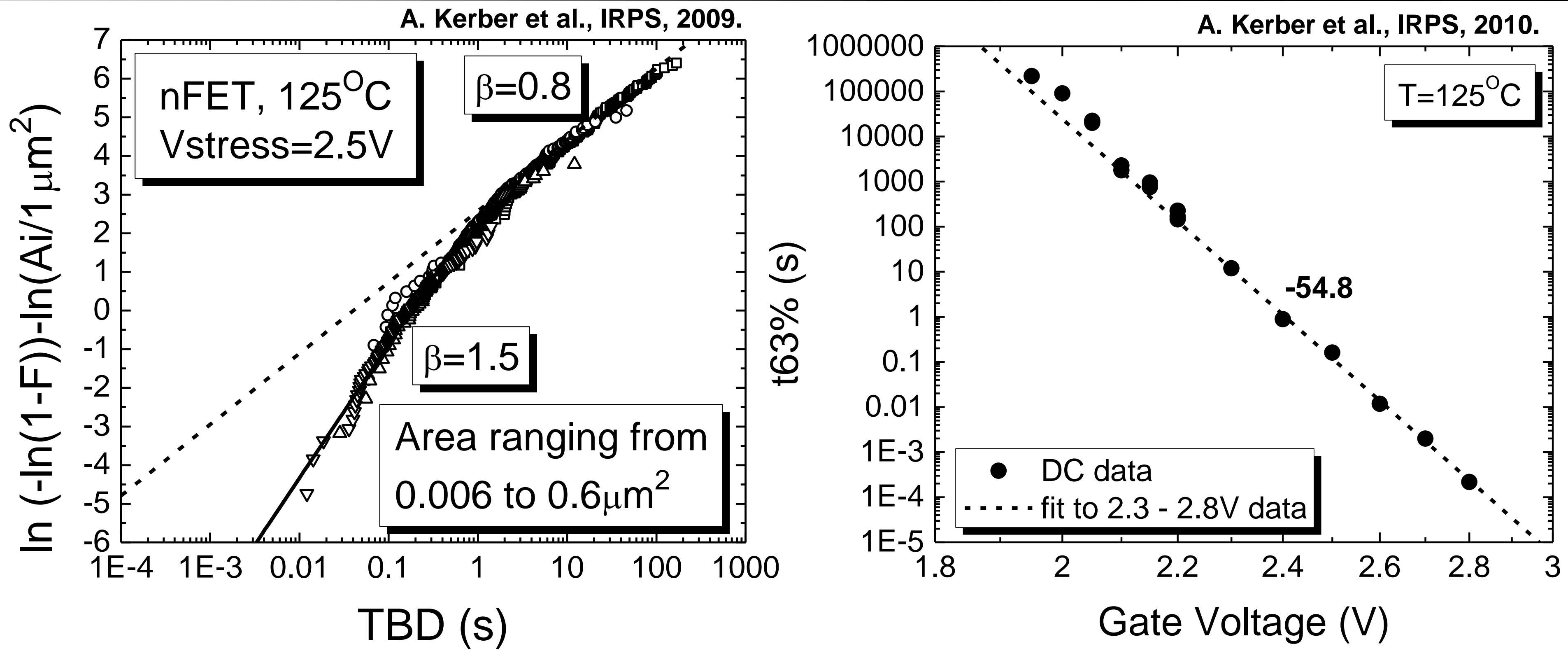
A. Kerber et al., IRPS, 2009.



- Poor correlation between failure time and CET
- Strong correlation between t63% and gate leakage current

  ➔ **t63% versus Jg used as FOM for process development**

TDDB distribution and voltage dependence

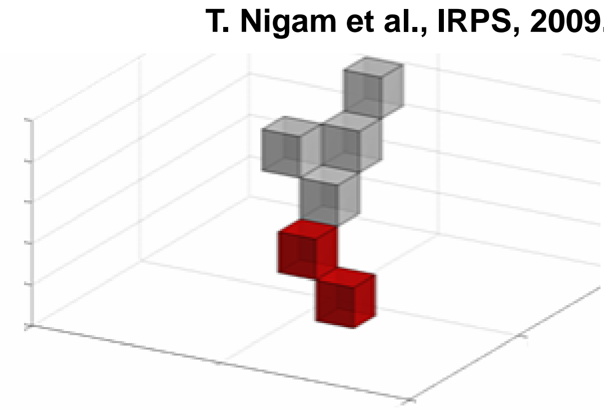


- MG/HK TDDB follows Poisson scaling / vertical area scaling
  - Increase in Weibull slope with increasing gate area
- Voltage dependence well described by power law model

Modeling TDDB failure distribution in core MG/HK devices

- Competing degradation of a dual layer gate stack
  - Failure distribution well described by applying the percolation concept with the assumption of different generation rates for interface and high-k layer

T. Nigam et al., IRPS, 2009.



- Progressive failure
  - Since failure distributions are similar to ultra-thin SiON / poly-Si stacks, it is feasible that a similar concept applies to MG HK

S. Sahhaf et al., TED, pg. 1424, 2009.

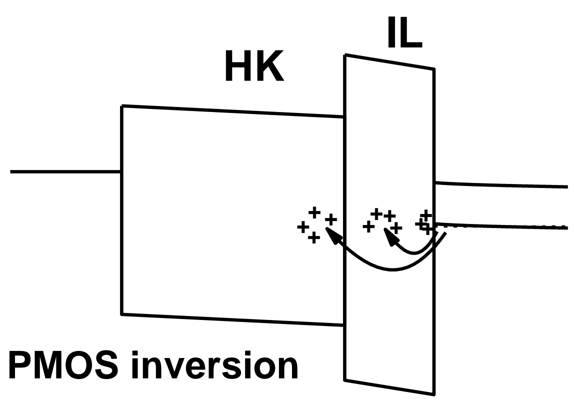
- Competing degradation of a dual layer gate stack + progressive wear out

J. Sune et al., IEDM, pg. 230, 2010.

BTI mechanism in CMOS devices

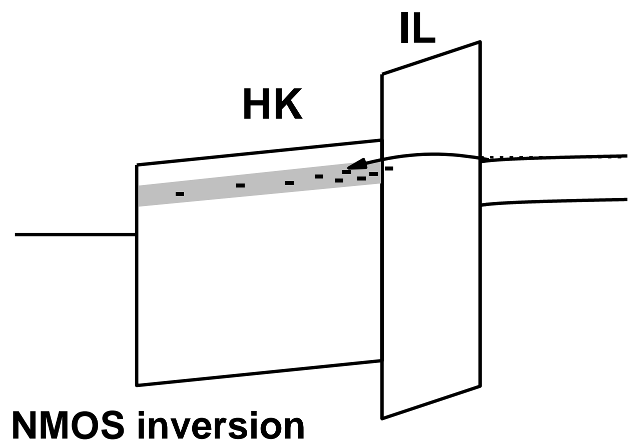
A. Kerber et al. IEEE EDL, Vol. 24, No. 2, pp. 87-89, 2003.

NBTI in pFETs



- NBTI leads to build up of positive charge
- Interface states, hole traps in the interlayer and high-k layer are contributors

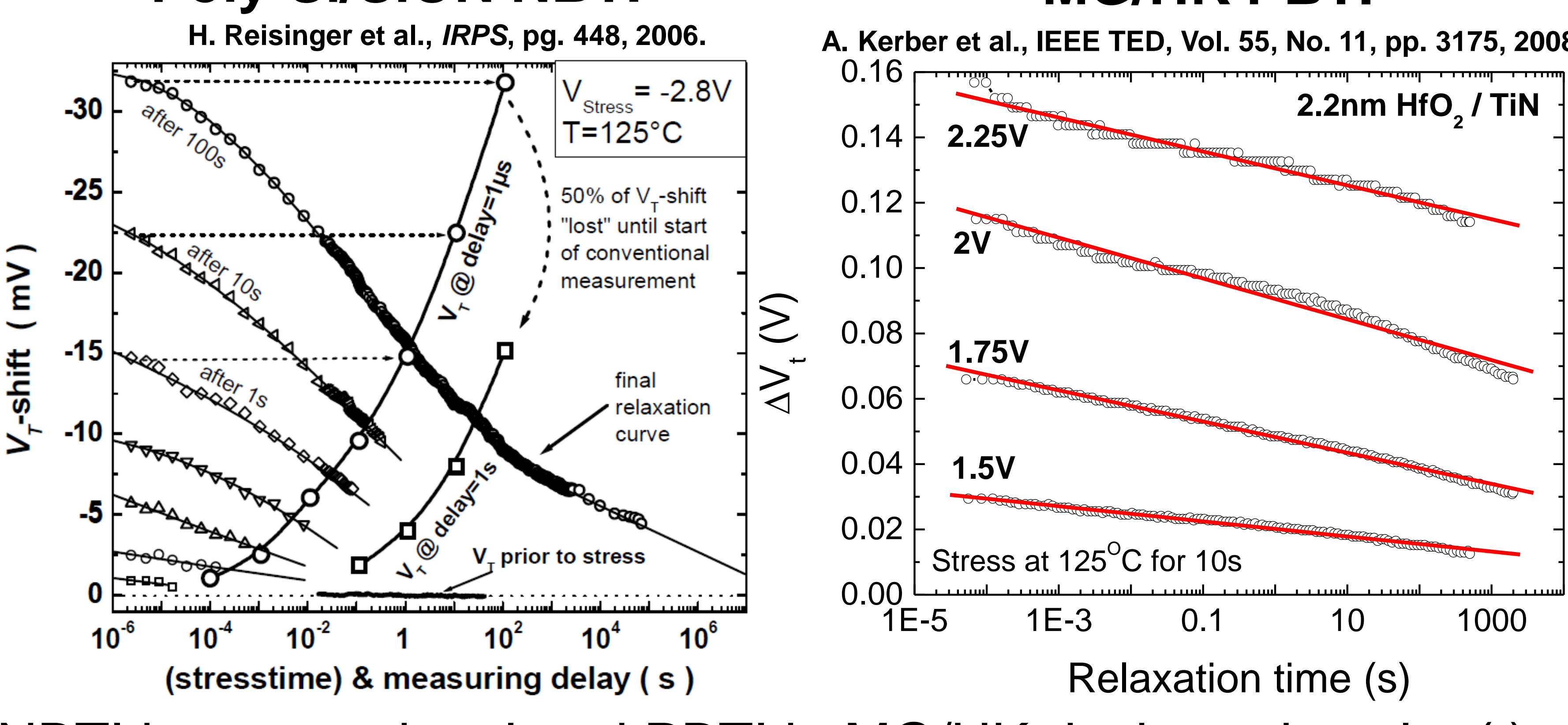
PBTI in nFETs



- PBTI leads to a build up of negative charge
- A defect band positioned in energy above the Si-conduction band edge is the primary cause and attributed to oxygen vacancies

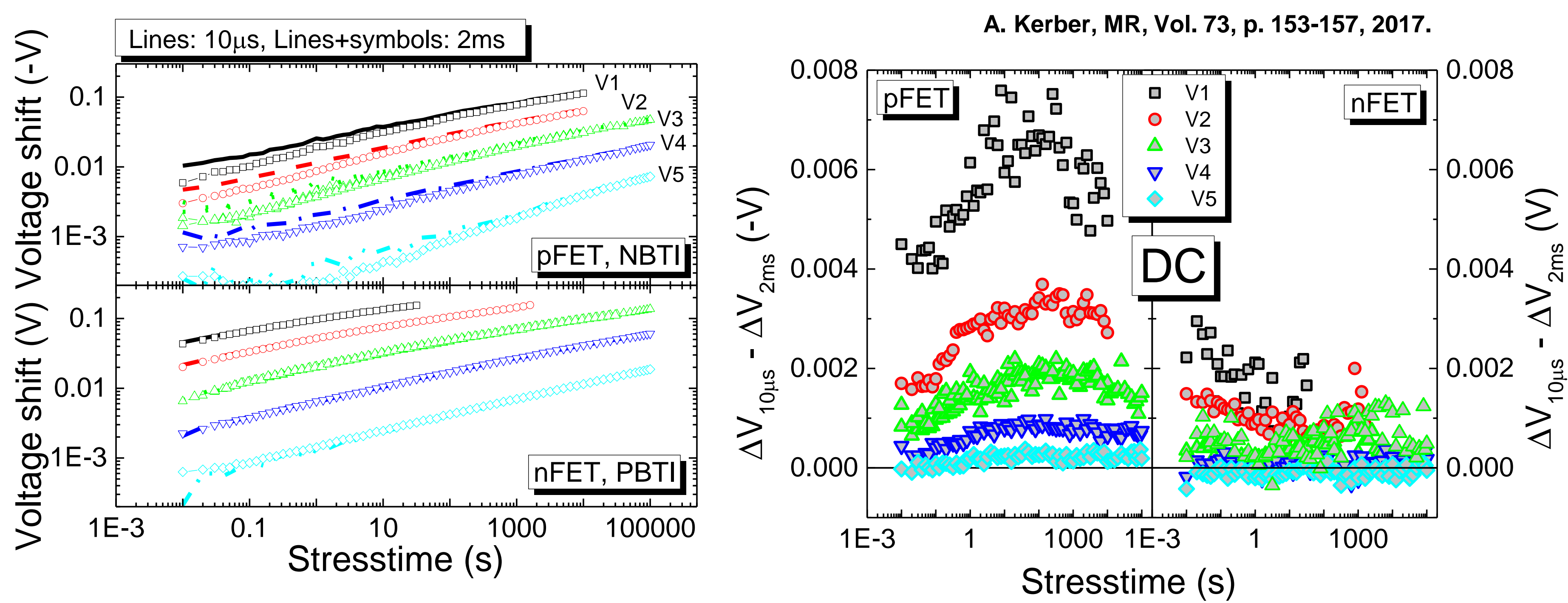
Band diagrams after R. G. Southwick III, et al., *IEEE TDMR,* vol. 11, pp. 236-243, 2011.

BTI recovery effects using stress and sense method



- NBTI in conventional and PBTI in MG/HK devices show log(t) like recovery behavior
  ➔ recovery studies need do cover many decades in time
  ➔ characterization focused to minimize sense duration

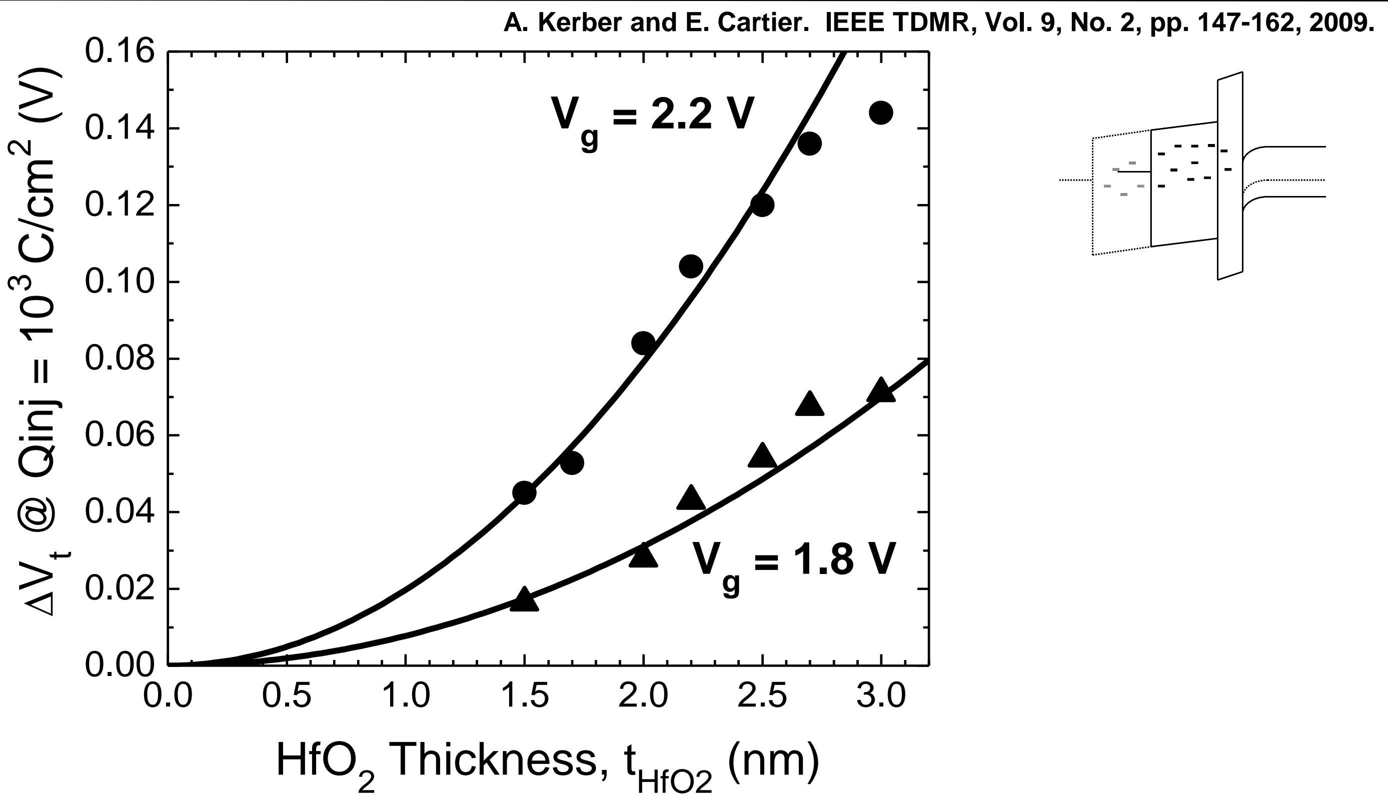
xBTI degradation in MG/HK devices



- Fast (2ms) & ultra-fast (10µs) xBTI degradation follows power law time evolution
- For NBTI 2ms & 10µs degradation merge at long stress times
- For PBTI negligible difference between 2ms & 10µs
  ➔ **fast versus ultra-fast characterization does not impact long term projection**

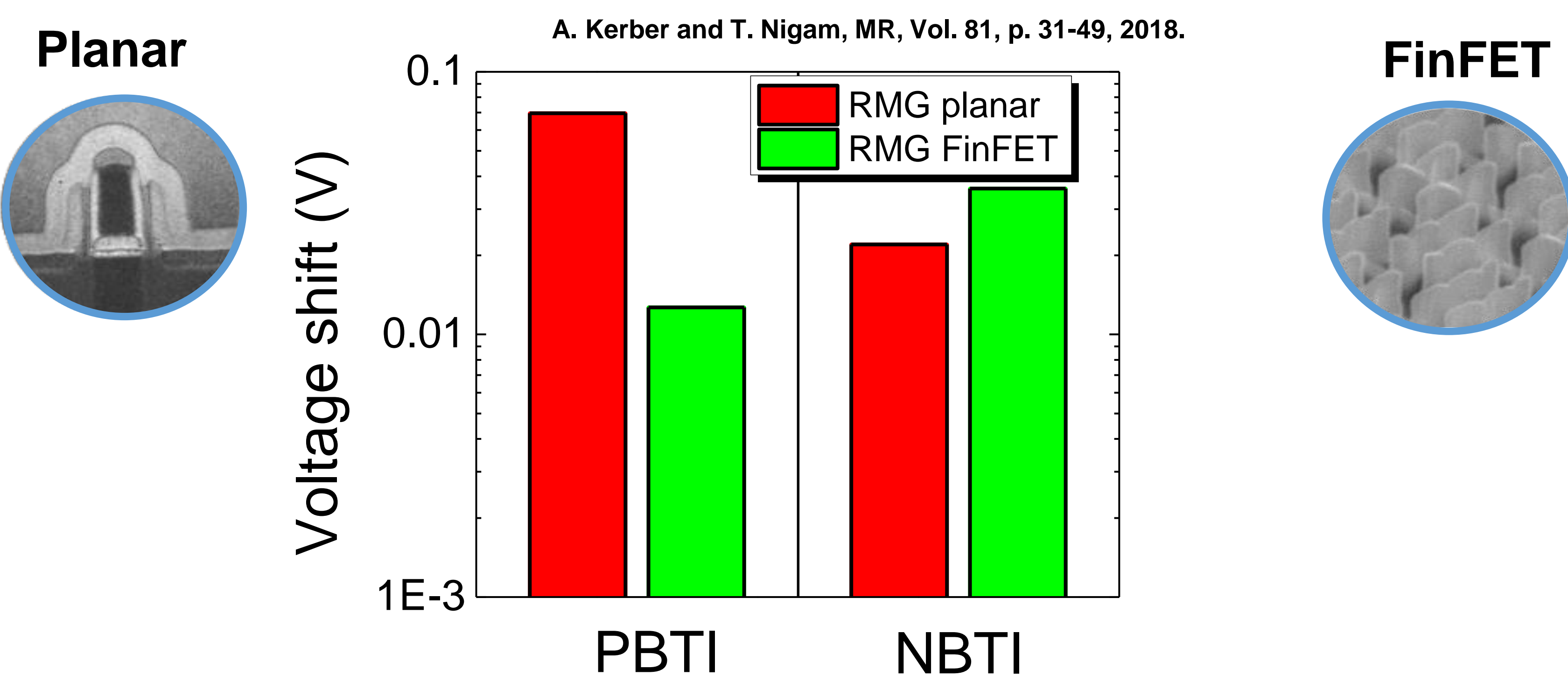
PBTI scaling in nMOS

A. Kerber and E. Cartier. IEEE TDMR, Vol. 9, No. 2, pp. 147-162, 2009.



- HfO_2 thickness dependence for PBTI consistent with bulk-charging model → $\Delta Vt \sim (t_{HfO2})^2$
- High-k thickness scaling an effective means to reduce PBTI

Planar versus FinFET xBTI comparison



- Consistent trend throughout the industry
- Substantial Reduction in nMOS PBTI ➔ FinFETs operating at lower field
- Enhanced pMOS NBTI ➔ Change in crystal orientation or Roughness induced by Fin formation

BTI and its implication on circuits

- Voltage and time evolution of xBTI is frequently modeled using power law dependences

$$\Delta V_T \; or \; \Delta Id_{sat} = A(t_{ref}, V_{ref}) \left(\frac{t}{t_{ref}}\right)^n \left(\frac{V}{V_{ref}}\right)^m$$

- In small devices BTI becomes a stochastic process

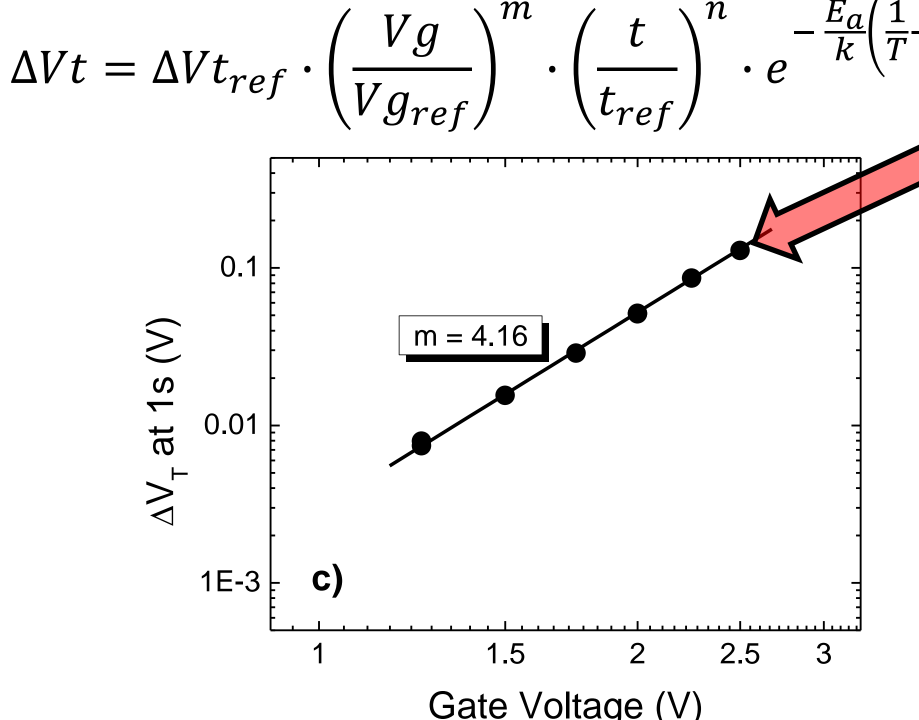
- Circuit implication:
  - For logic circuits like RO the mean degradation $(\overline{\Delta V_T} \; or \; \overline{\Delta Id_{sat}})$ remains most relevant since the circuit is comprised of several stages
  - For SRAM circuits stochastic variations $(\sigma(\Delta V_T))$ in addition to mean degradation $(\overline{\Delta V_T})$ are important

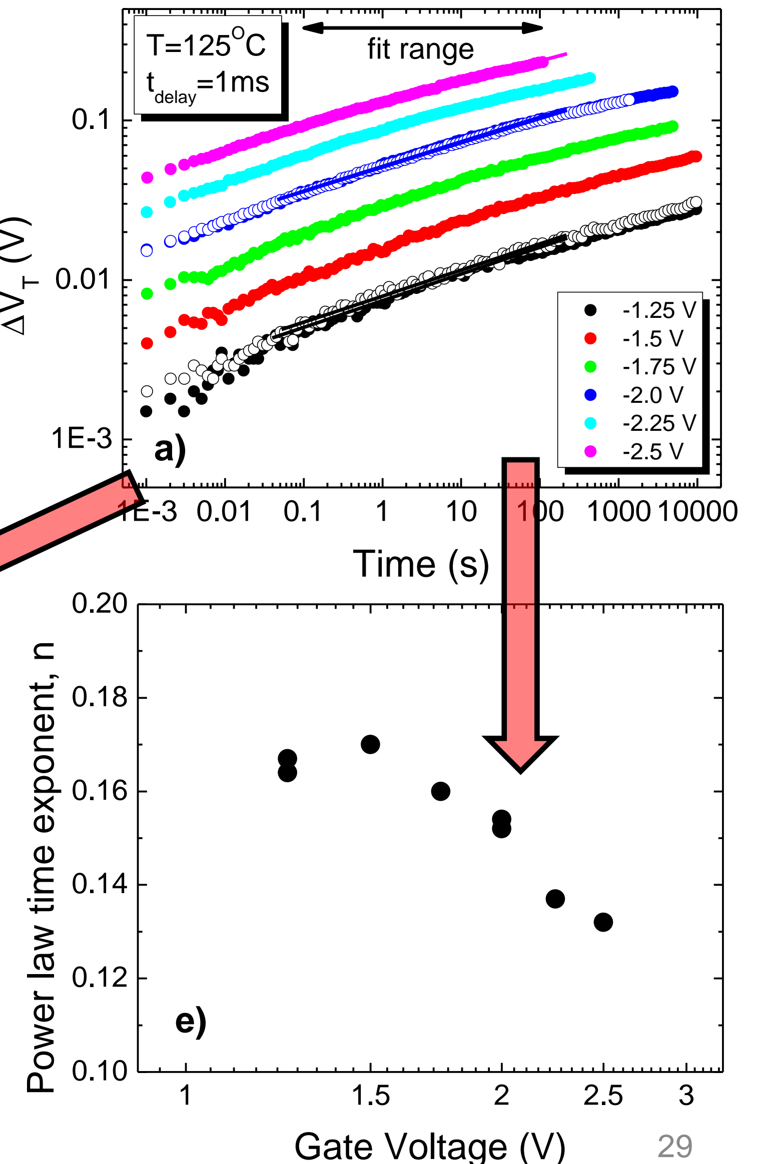
Basic BTI model for thin oxide CMOS devices

data A. Kerber, S. Krishnan, E. Cartier, IEEE EDL, VOL. 30, NO. 12, *pp. 1347–1349,* 2009.

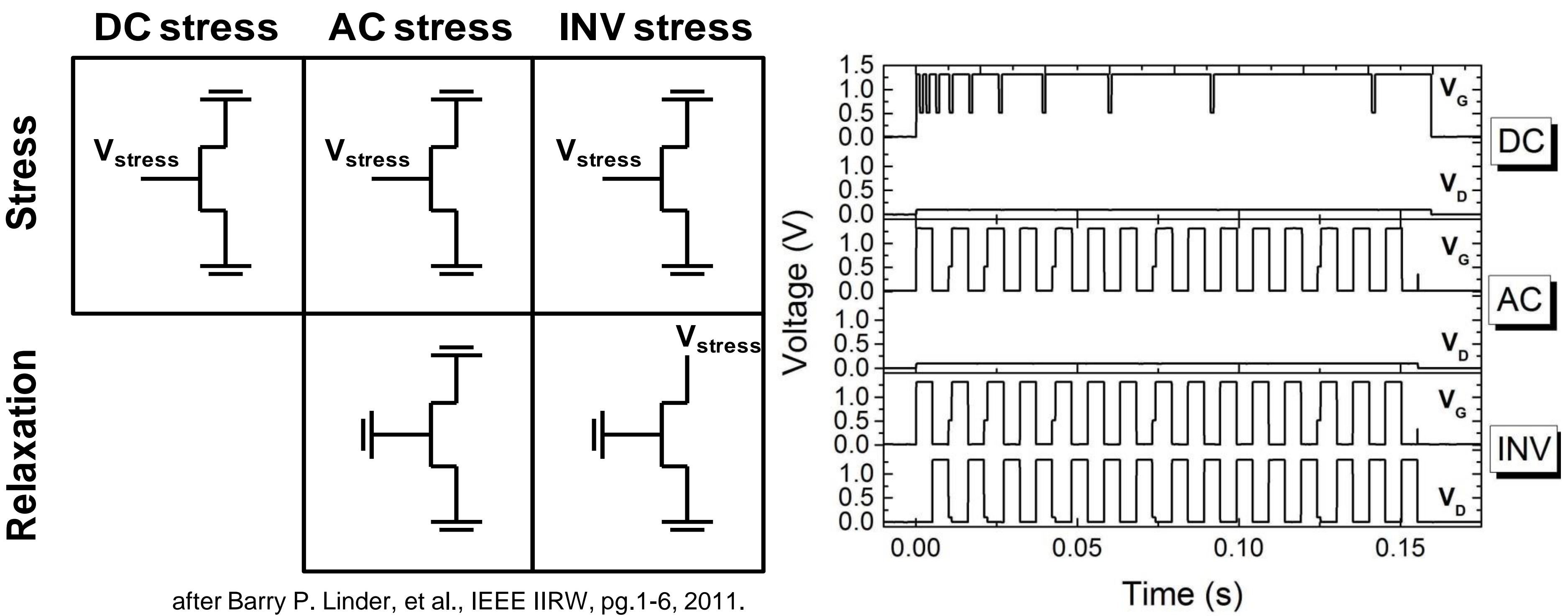
- ΔVT time traces used to extract super-linear voltage (m) and sub-linear time evolution (n)
- Typical n values: 0.15<n<0.25
- 3.5<m<6 for NBTI and 5<m<9 for PBTI
- Typical Ea values: 0.1 < Ea <0.2

$$\Delta Vt = \Delta Vt_{ref} \cdot \left(\frac{Vg}{Vg_{ref}}\right)^{m} \cdot \left(\frac{t}{t_{ref}}\right)^{n} \cdot e^{-\frac{E_a}{k}\left(\frac{1}{T}-\frac{1}{T_{ref}}\right)}$$





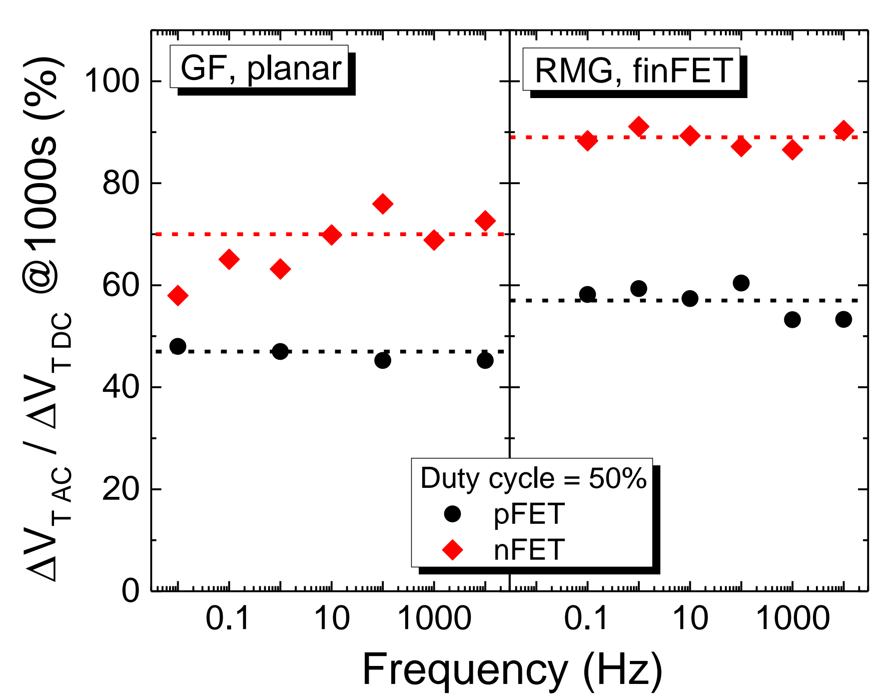
Discrete device stress modes to mimic circuit operation



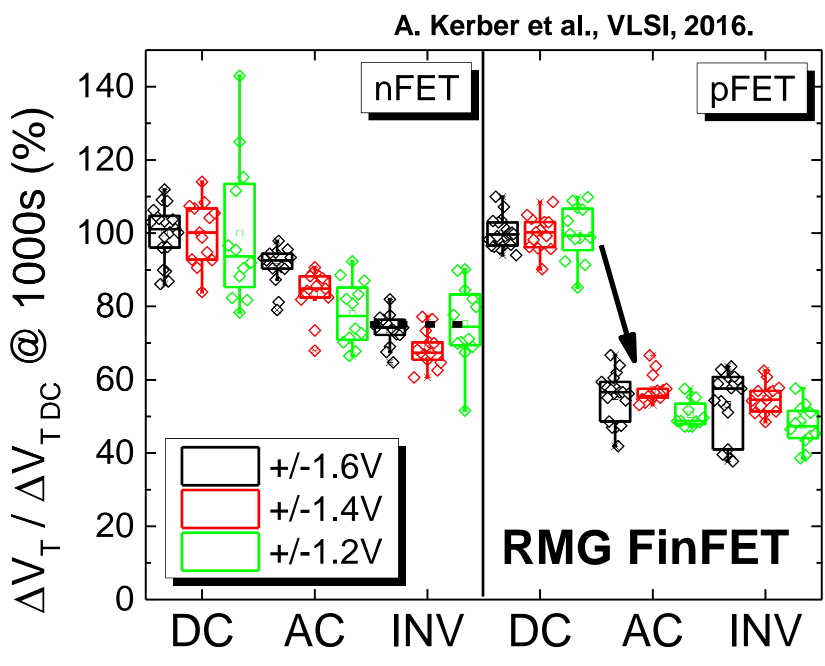
after Barry P. Linder, et al., IEEE IIRW, pg.1-6, 2011.

- AC stress alters between stress and GND
- INV stress mimics relaxation in SRAM and inverter ROs

Frequency dependence of discrete device BTI



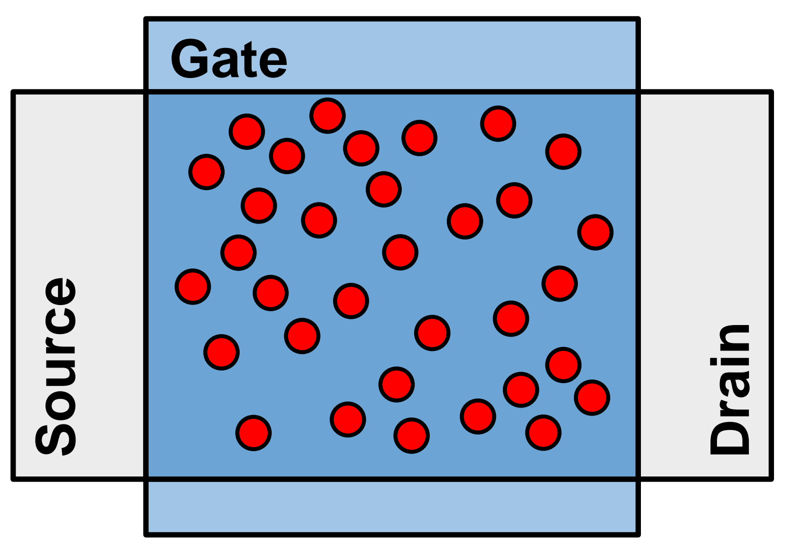
A. Kerber et al., VLSI, 2016.

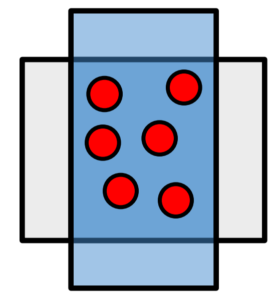


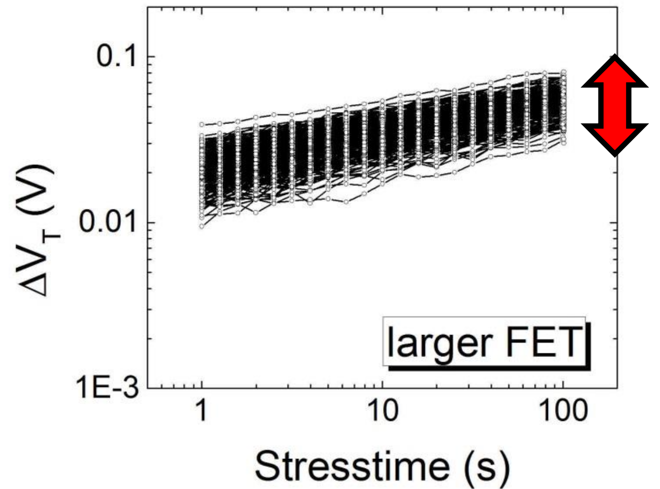
- No frequency dependence for BTI from sub-Hz to 10kHz for RMG FinFET and GF planar MG/HK devices
  - Remaining NBTI fraction: ~ 40% to ~60%
  - Remaining PBTI fraction: ~70% to ~90%
- No impact of stress mode on NBTI recovery while PBTI shows enhanced de-trapping for inverter stress

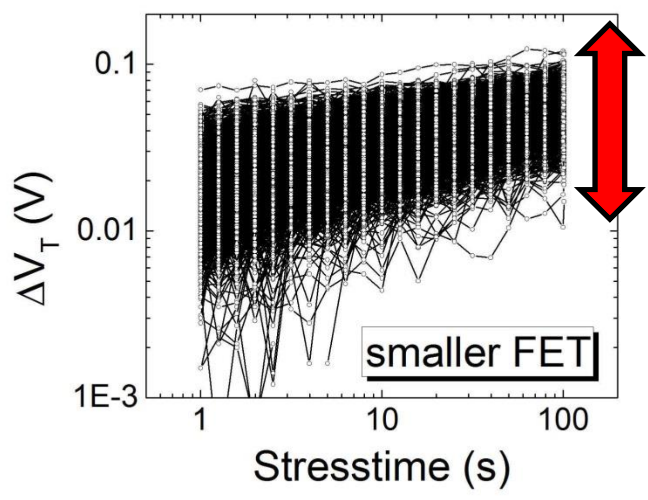
Stochastic BTI process

Oxide or interface charge

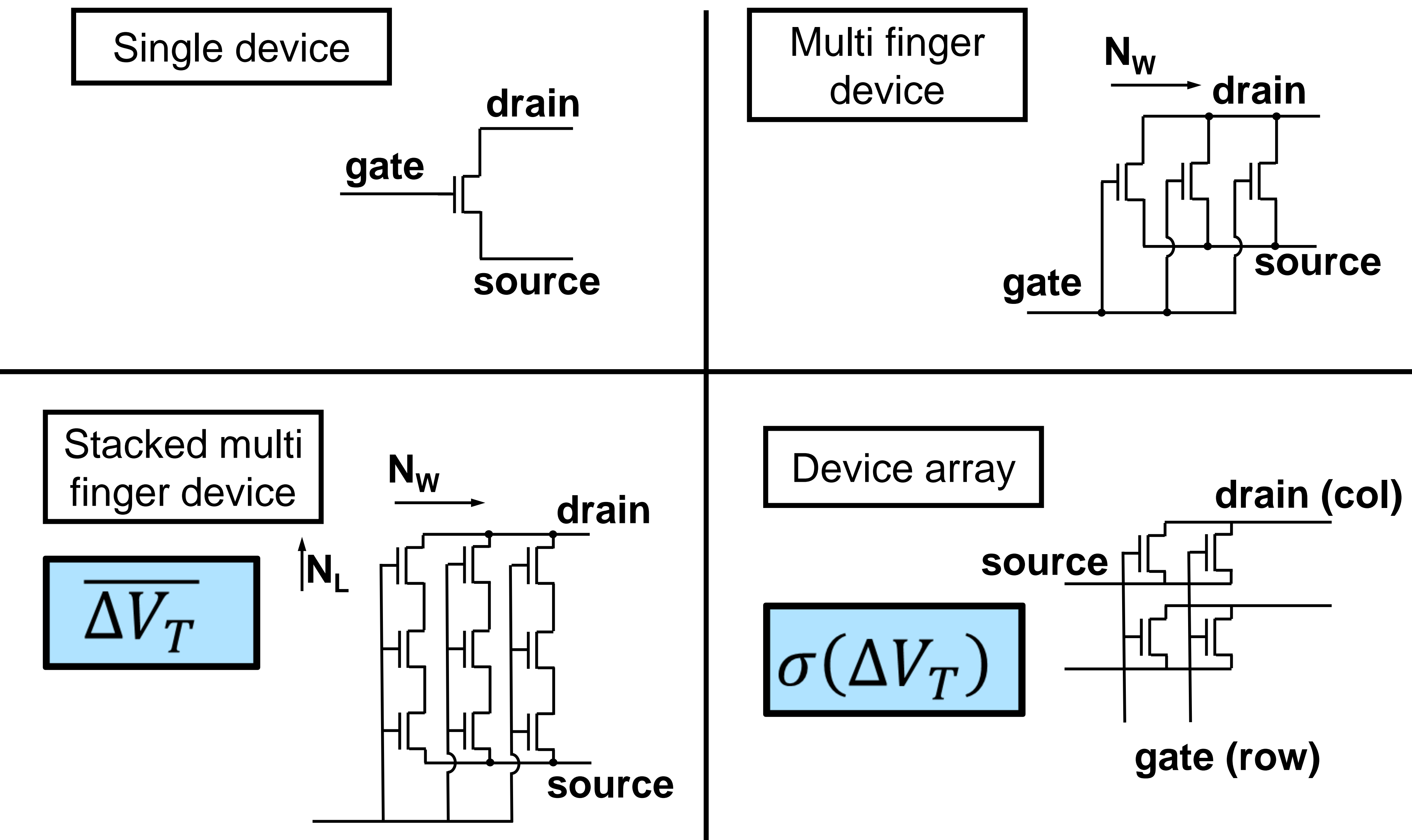








Test structure innovation to assess stochastic BTI



Modeling of stochastic BTI process

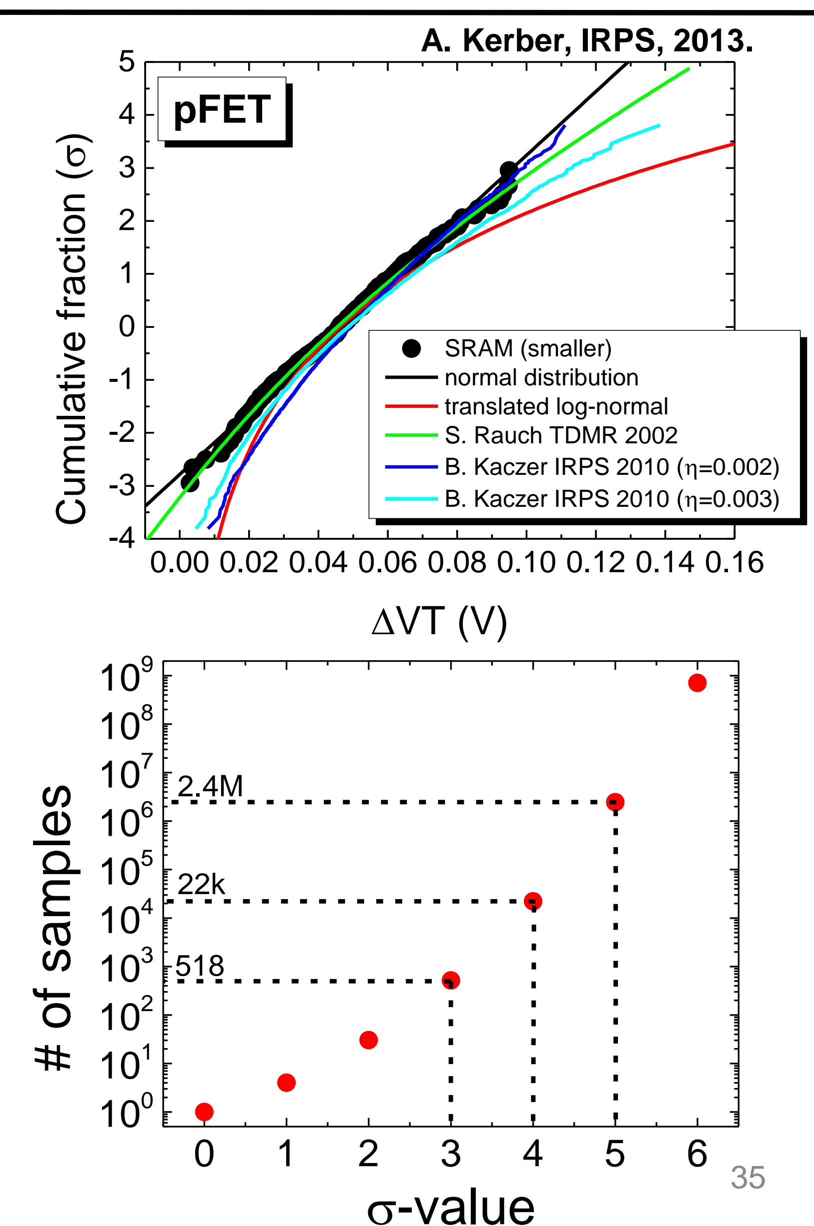
- How is BTI induced ΔV_T in small devices described?

$$\Delta Vt_{use} = \Delta Vt_{stress} \cdot AF_{volt} \cdot AF_{time} \cdot AF_{temp} \cdot AF_{percentile}$$

- Voltage, time and temperature dependence of the mean degradation is model as for large devices
- Percentile scaling is the main focus for stochastic BTI modeling
  - Popular choices are normal distribution, compound Poisson process (S. Rauch, TDMR 2002), Gamma functions (B. Kaczer, IRPS 2010), …

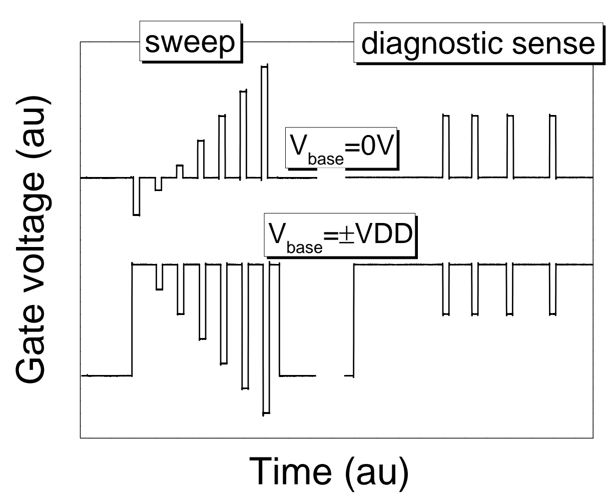
How to validate stochastic BTI models

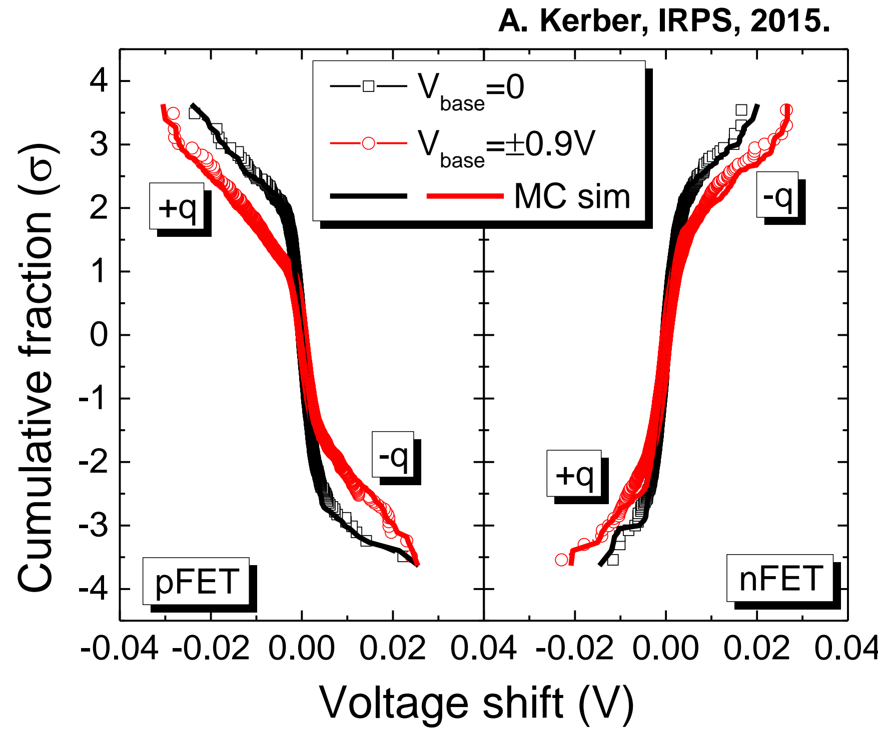
- Since most stochastic models describe the average behavior equally, large sample size is required to validate the tail
- Extending discrete device level testing beyond 3σ requires innovation
  - Shared gate devices
  - Variability test chip

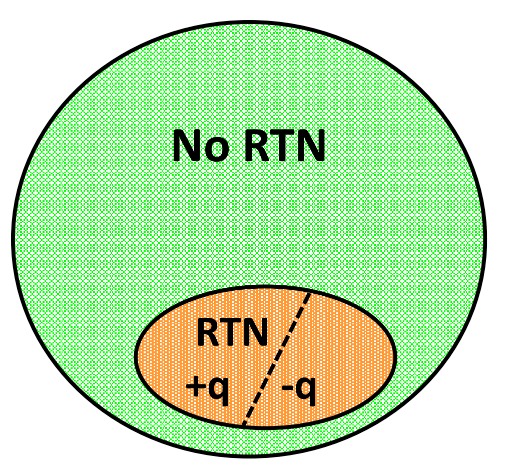


Time-zero RTN and its impact on stochastic BTI

A. Kerber, IRPS, 2015.

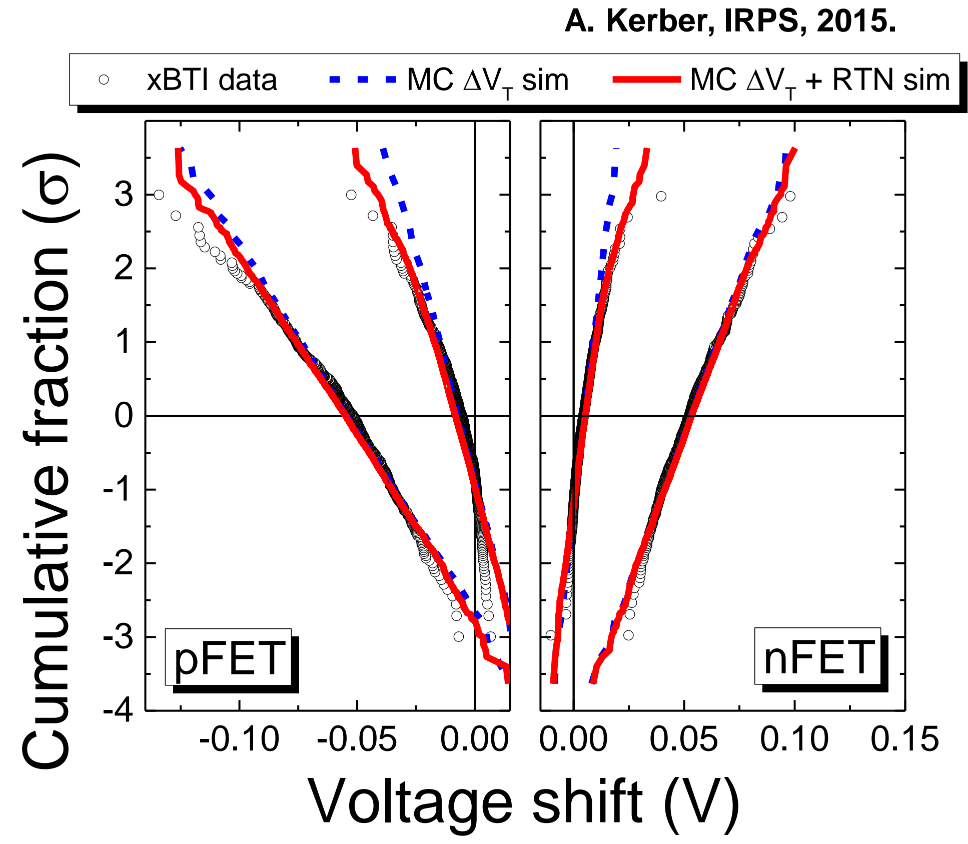






- RTN in scaled devices leads to random voltage shifts in + or – negative direction
- CDF well reproduce by MC simulations with a σ=1.5mV and σ_{RTN}=9mV with adjusted P_{RTN}, P_+ and P_-
- RTN can dominate stochastic BTI for small degradation

Impact of RTN on BTI induced ΔV

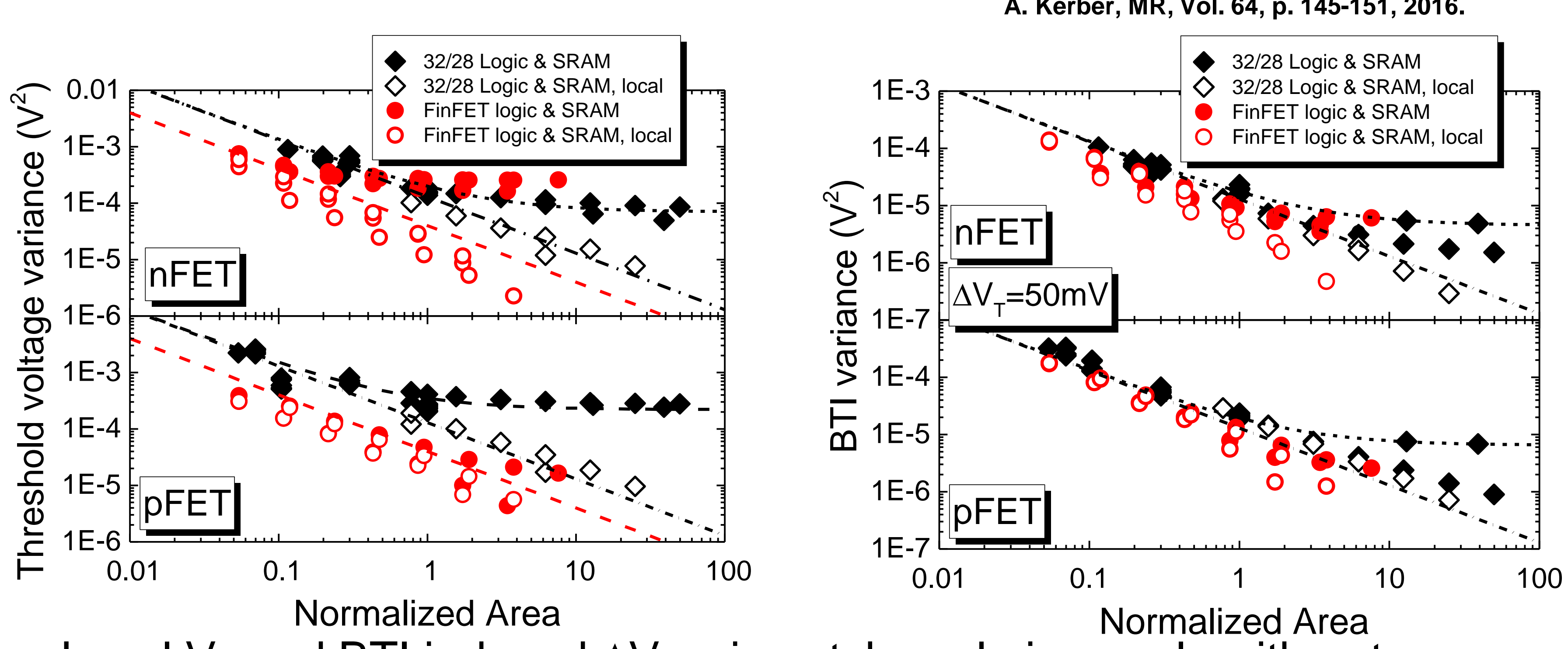


- RTN causes significant t_0 skew in ΔV distribution and remains a contributor for small BTI degradation
- At technology relevant BTI degradation RTN becomes a diminishing factor

- **RTN impact well captured by MC simulations**

Time-zero V_T and BTI induced ΔV_T variance comparison

A. Kerber, MR, Vol. 64, p. 145-151, 2016.



- Local V_T and BTI induced ΔV_T mismatch scale inversely with gate area
- Improved V_T mismatch for FinFETs due to reduced RDF compared to planar bulk and PDSOI devices
- Variance of large area devices across wafer limited by process variation for time-zero V_T and BTI induced ΔV_T

Discrete device reliability: Summary

- TDDB failure distributions in MG/HK Devices follows Poisson scaling and is successfully described by dual layer percolation model
- AC effects are critical for modeling logic circuits aging due to xBTI
- Decoupling RTN from xBTI and comprehending ΔV_T to V_T correlations important for the development of stochastic degradation models for SRAM devices
- Self-heating becoming a growing concern for scaled technology nodes

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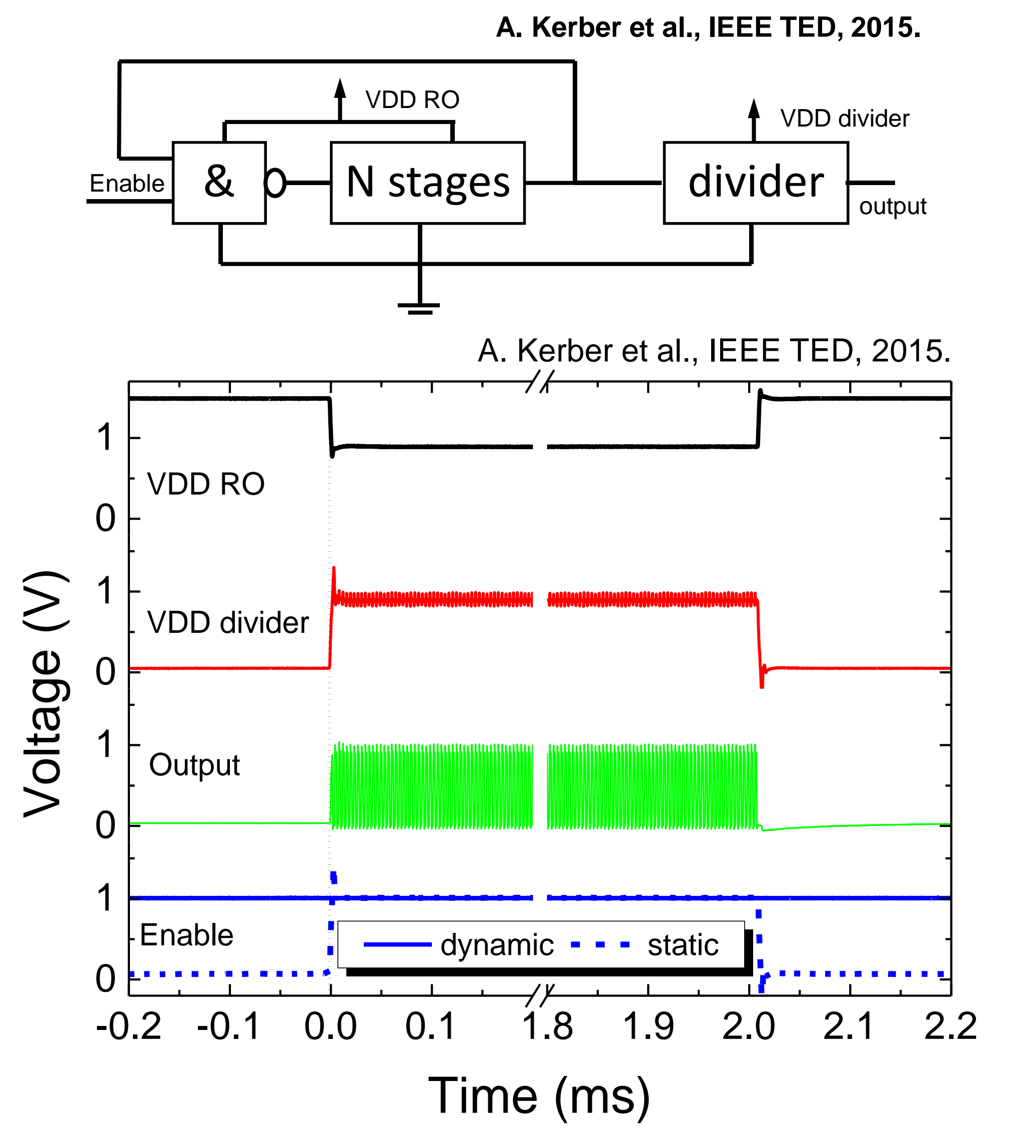
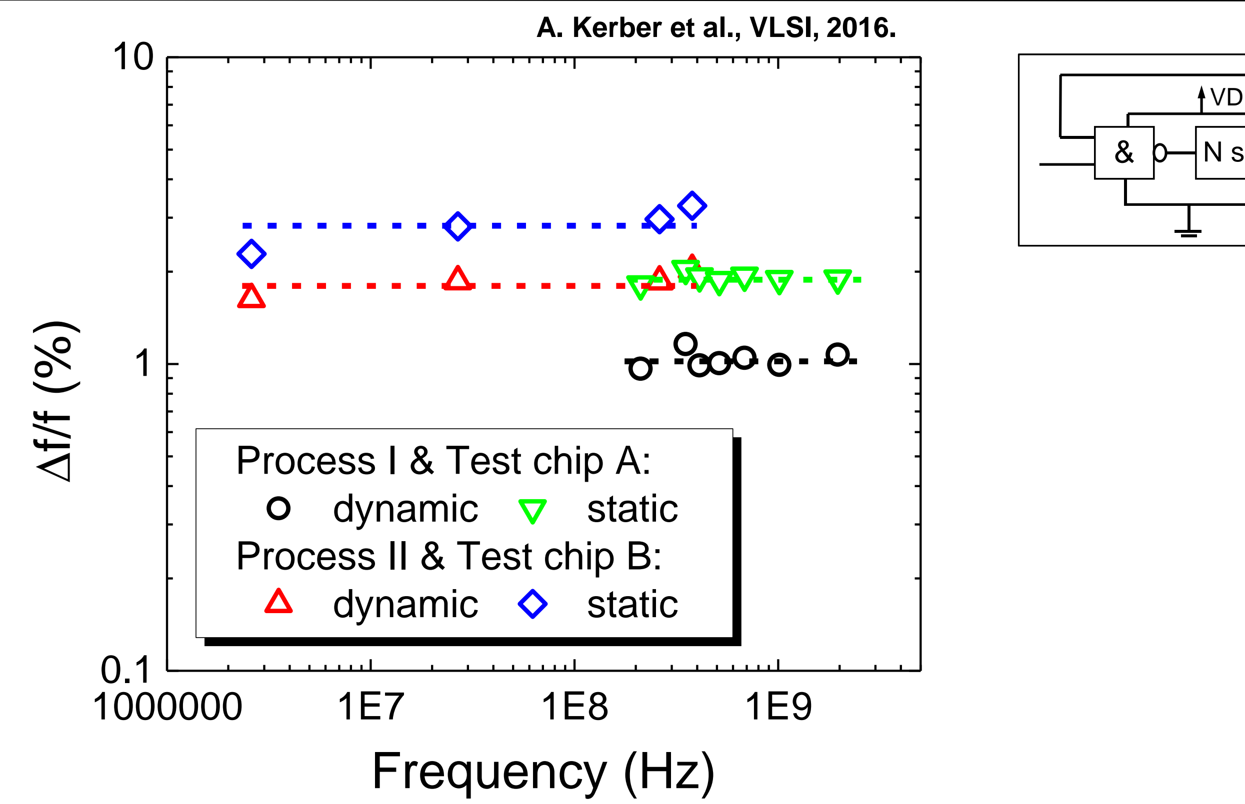
Time-resolved RO characterization



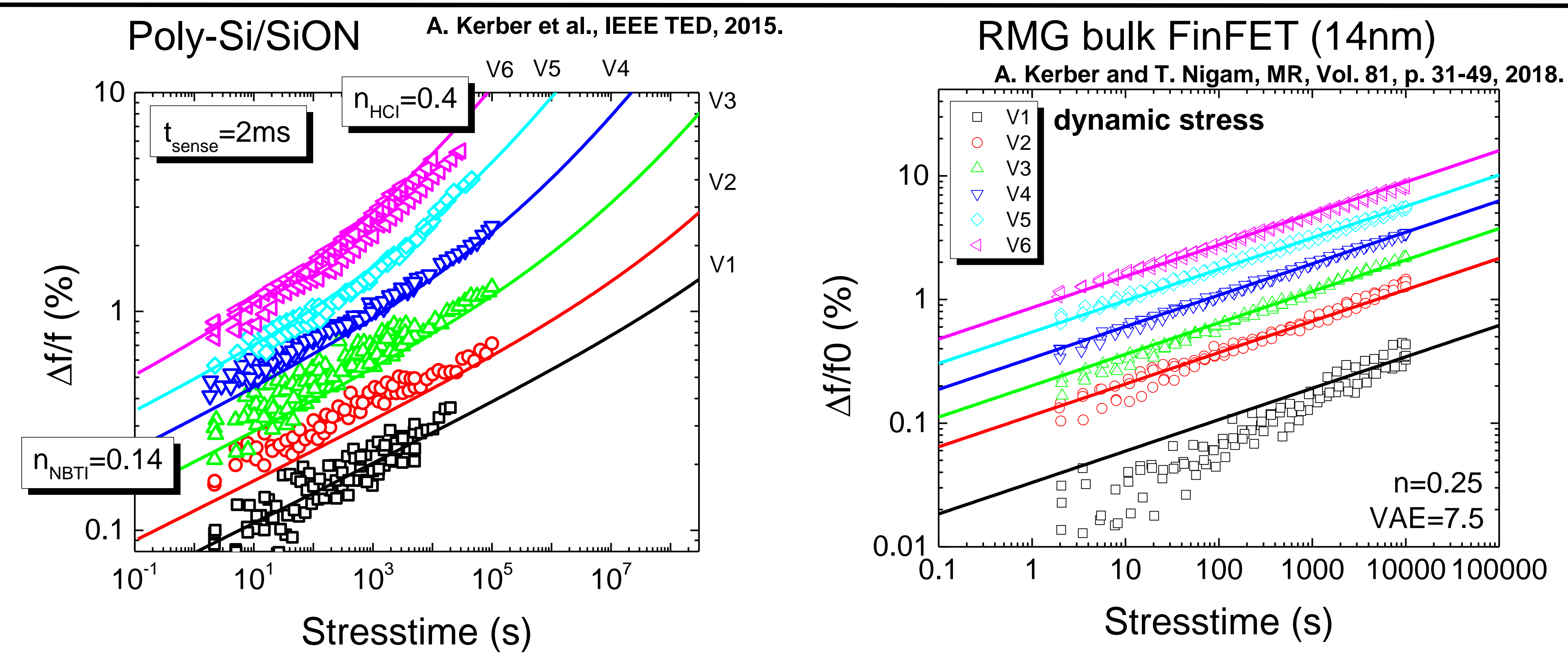
- Sub-ms sense intervals achieved via synchronized switching of power supply units (VDD RO, VDD divider, enable pin)
- RO frequency measured with digital scope using “jitter” function
- Degradation determined at nominal supply voltage
- Supply currents recorded to study dielectric breakdown

RO degradation based on CVS



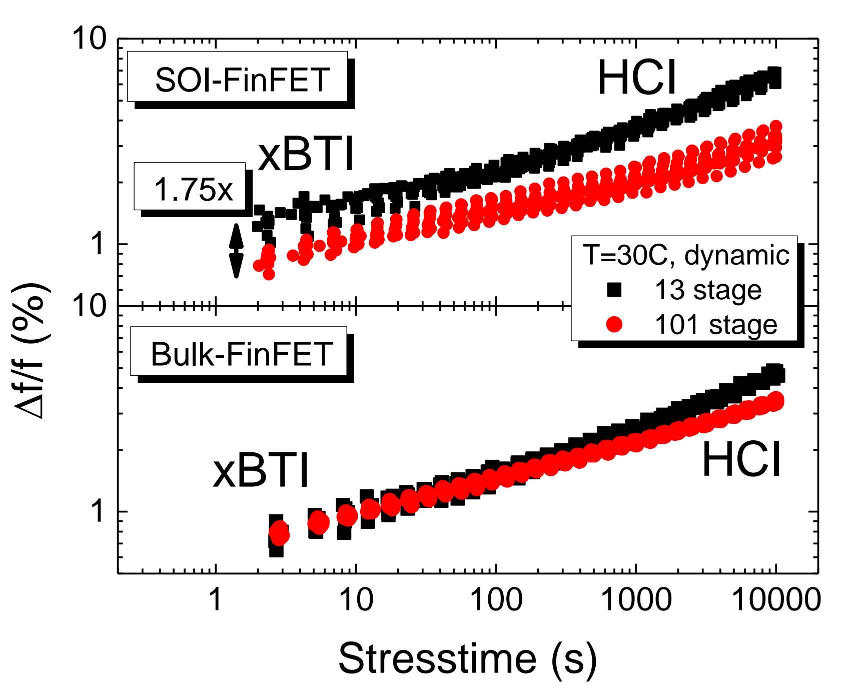
- Static (DC) stress mode leading to higher frequency degradation compared to dynamic (AC) stress
- RO degradation in dynamic mode show negligible frequency dependence from GHz to MHz

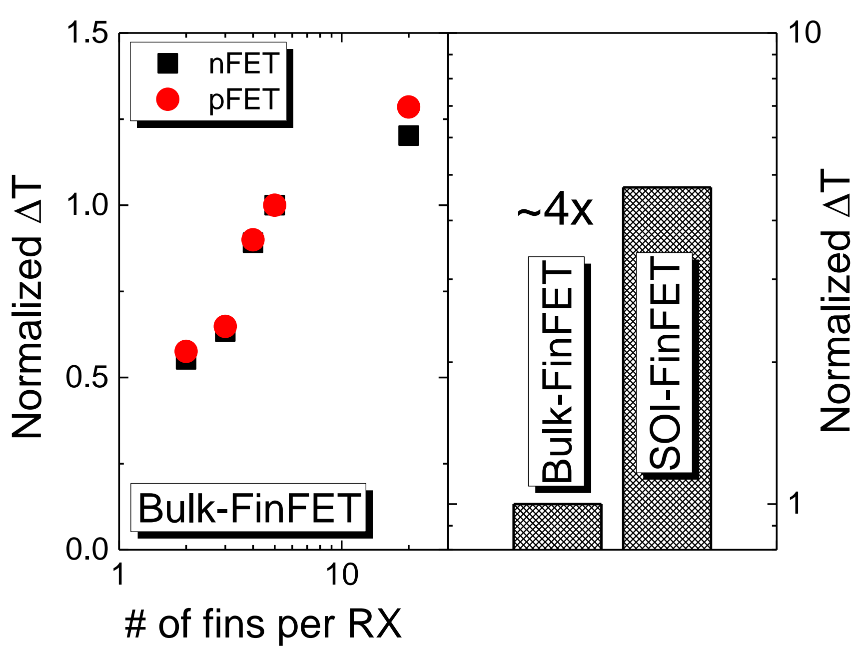
Kinetic RO degradation model



- For poly-Si/SiON, fast RO degradation reveals HCI contribution to frequency degradation causing an increase in time-slope at high stress voltage
- For RMG bulk FinFET, the model parameter for RO degradation are consistent with device level NBTI and PBTI (n~0.25, VAE=7.5)

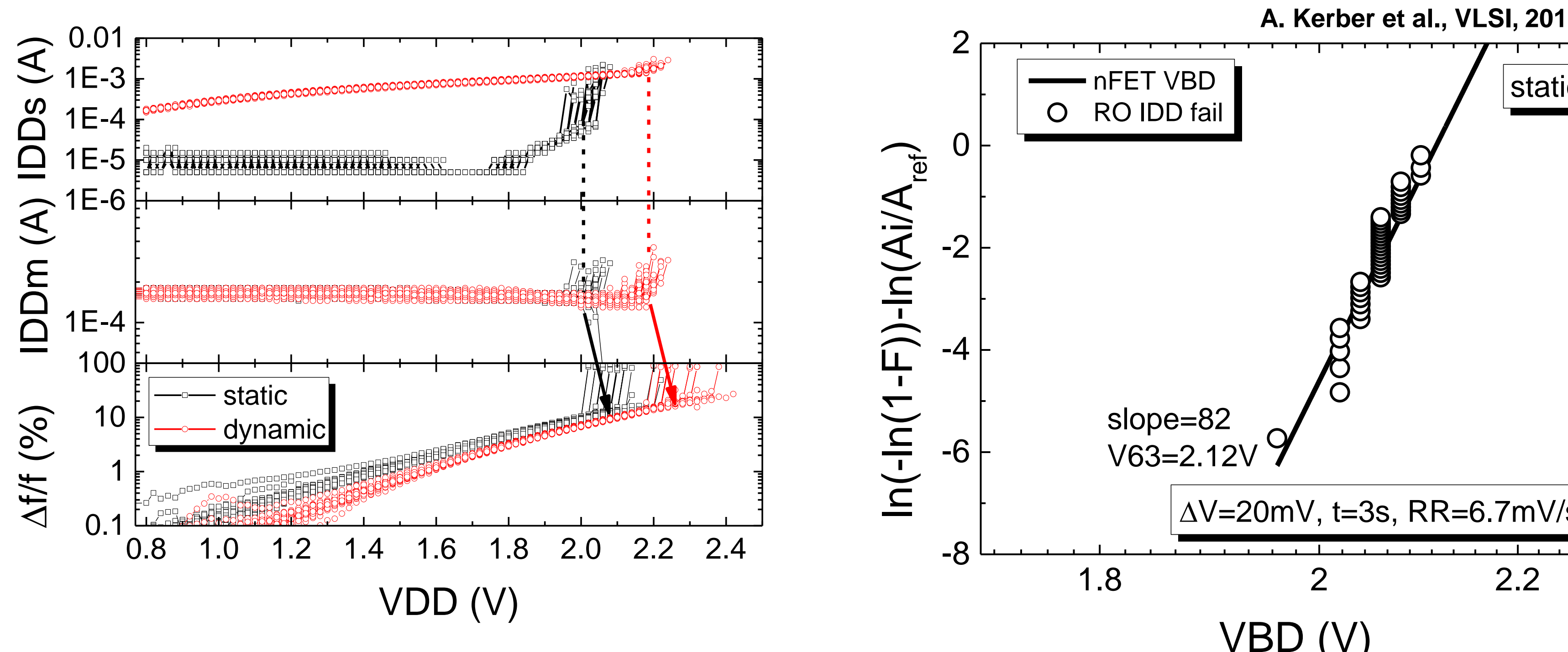
Evidence of Self-Heating in SOI FinFETs





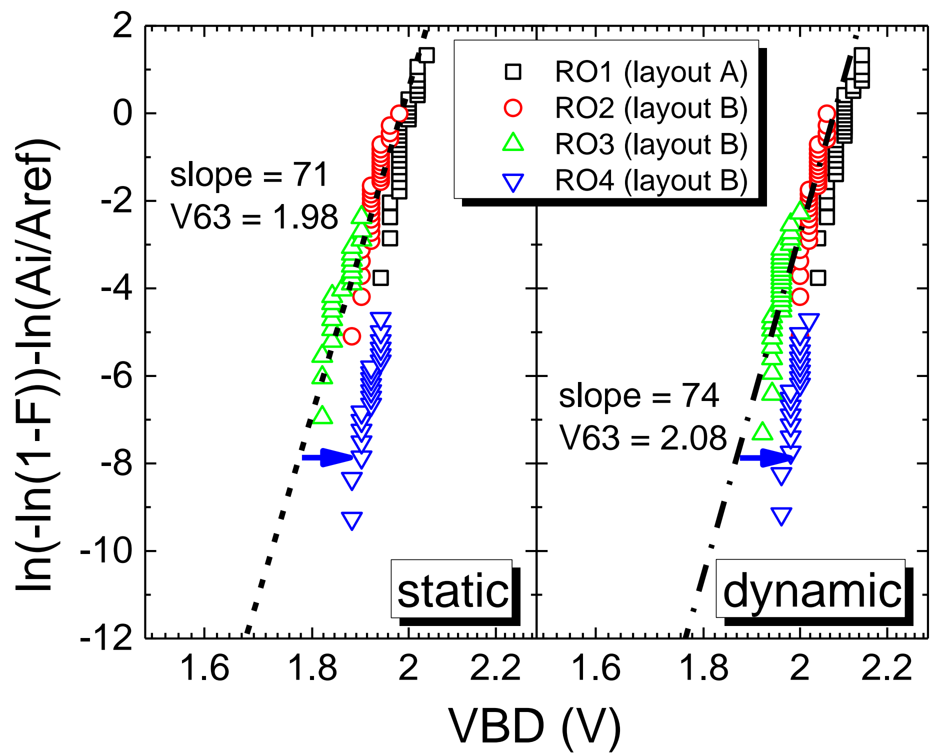
- Bulk-FinFETs at short stress time show same degradation for 13 and 101 stage RO
- SOI-FinFETs at short stress time show ~1.75x higher degradation ➔ temperature rise of ~30C at high stress condition

RO degradation and BD utilizing VRS

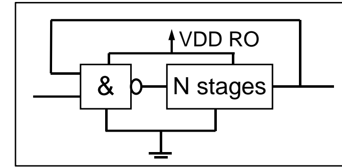


- Dielectric breakdown of ROs correlates very well with nFET TDDB based on supply current fail criteria
- Supply current increase typically occurs prior to erratic frequency changes making it a more robust breakdown monitor

RO VBD Poisson scaling



A. Kerber et al., VLSI, 2016.



- RO VBD follows Poisson scaling of dielectric breakdown
  - Dynamic stress shows ~100mV higher VBD compared to static stress
- Largest circuit area deviates to higher breakdown voltage due to IR since stress currents >10mA

Circuit reliability: Summary

- Frequency independence for BTI confirmed for frequencies ranging from 0.1Hz to 3GHz using RO circuits and discrete devices
- At short stress time and elevated junction temperature BTI dominates RO aging
- Hot Carrier contributions can be observed at longer stress times at high stress voltage and reduced junction temperature

Outlook

- Fundamentals of TDDB and BTI are not expected to alter in future MG/HK technology nodes (FinFETs, FDSOI, gate-all-around)
- With further reducing dimension stochastic variations remain in the focus
  - Time-zero and aging induced variation are in competition
  - Gate-to-contact TDDB is becoming an emerging failure mode and modeling / comprehending variation is key
- Self-heating is a growing concern in particular when moving to gate-all-around
- Device to circuit correlations are critical to establish performance and reliability trade-offs

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