Emerging Memories and Pathfinding for the Era of sub-10nm System-on-Chip

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Memory Is Big Business

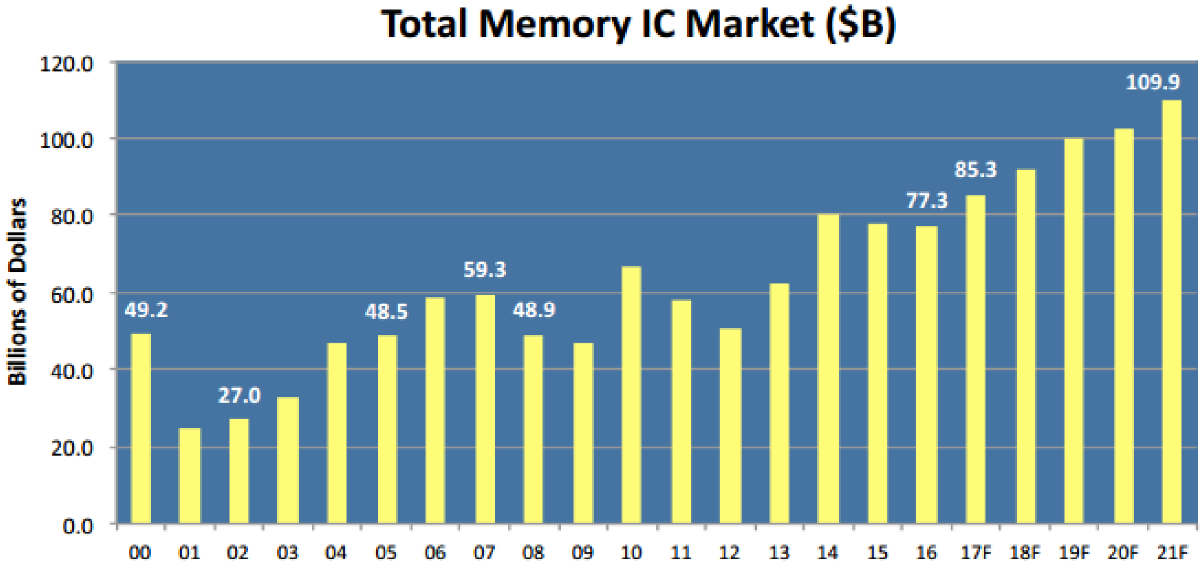
>> $100 Billions*

RESEARCH BULLETIN

IC Insights

DECEMBER 20, 2016

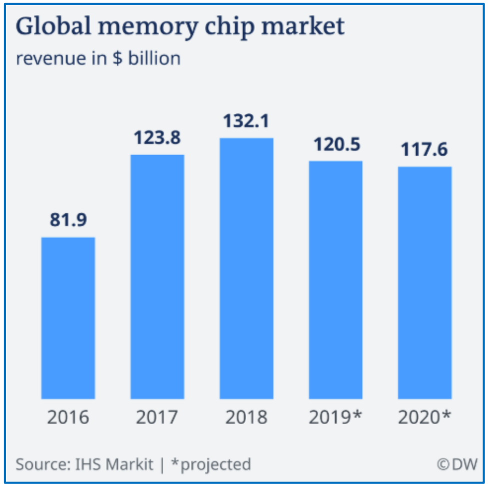
Total Memory Market Forecast to Increase 10% in 2017



http://www.icinsights.com/news/bulletins/Total-Memory-Market-Forecast-To-Increase-10-In-2017/

DW Made for minds.

Chipmakers under pressure as semiconductor 'supercycle' stalls

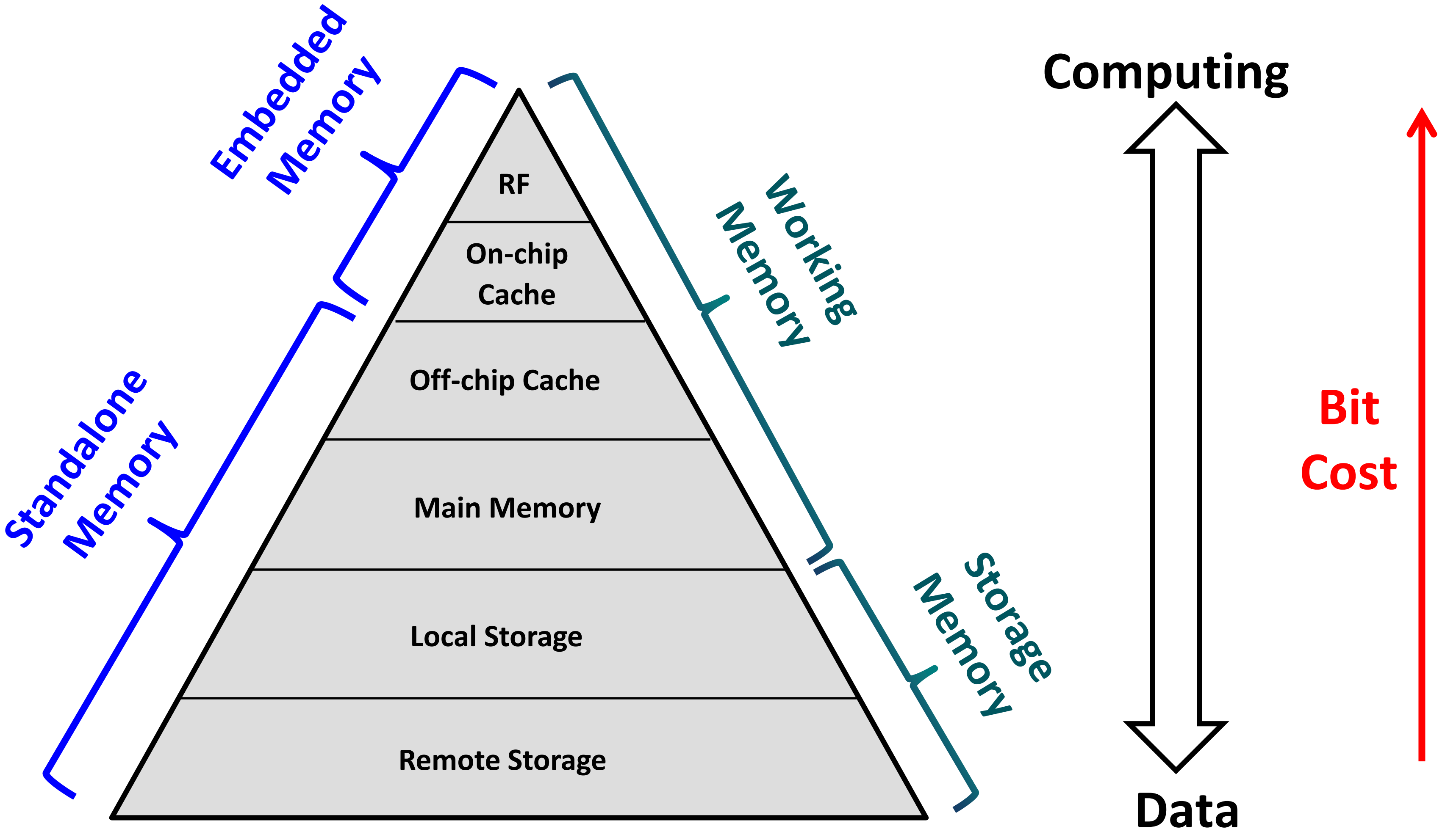


https://www.dw.com/

*** Not including embedded memories for AP, SOC, and MCU***

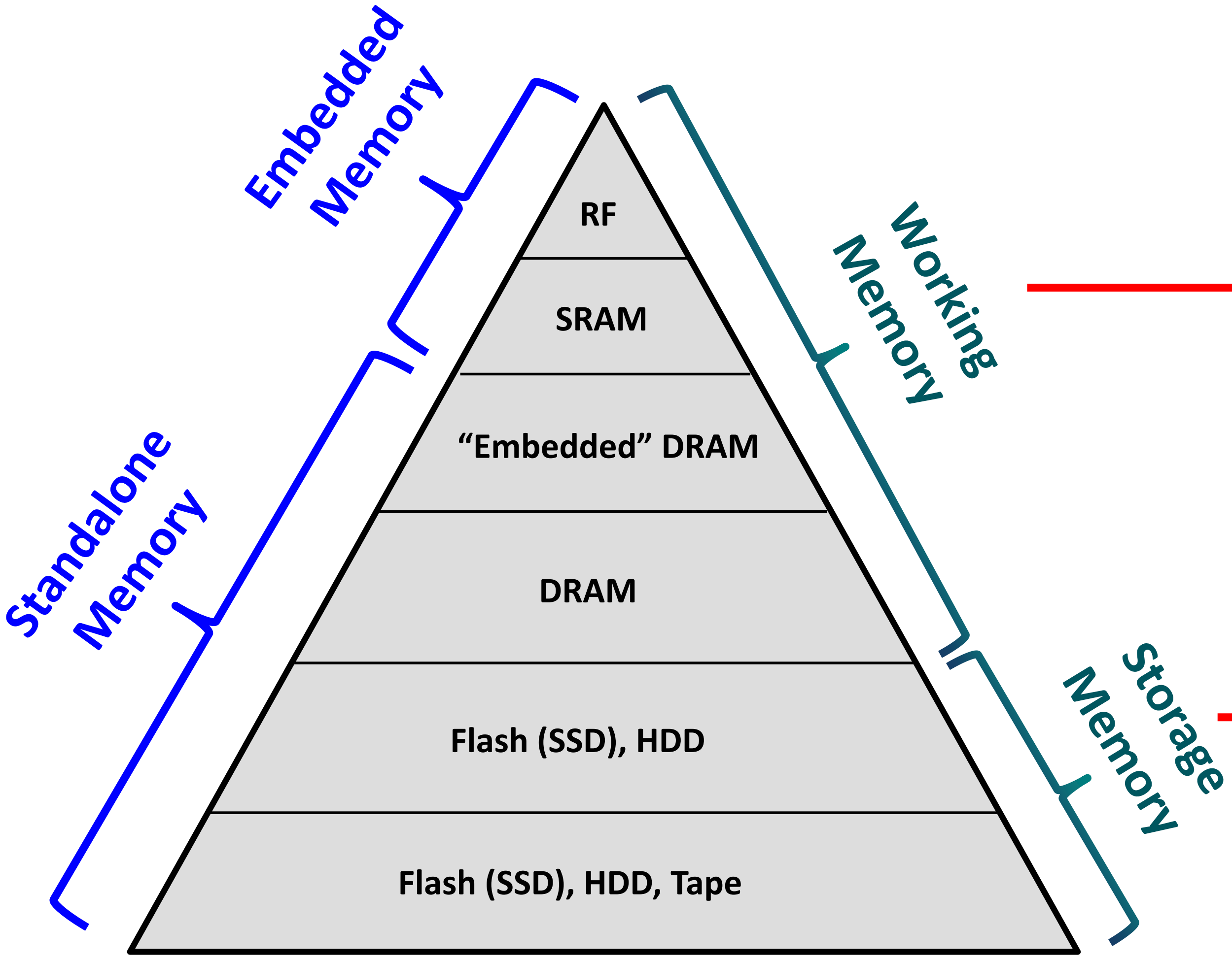
Memory Subsystem

Hierarchical memory layers



Memory Subsystem

There is no such thing like a universal memory



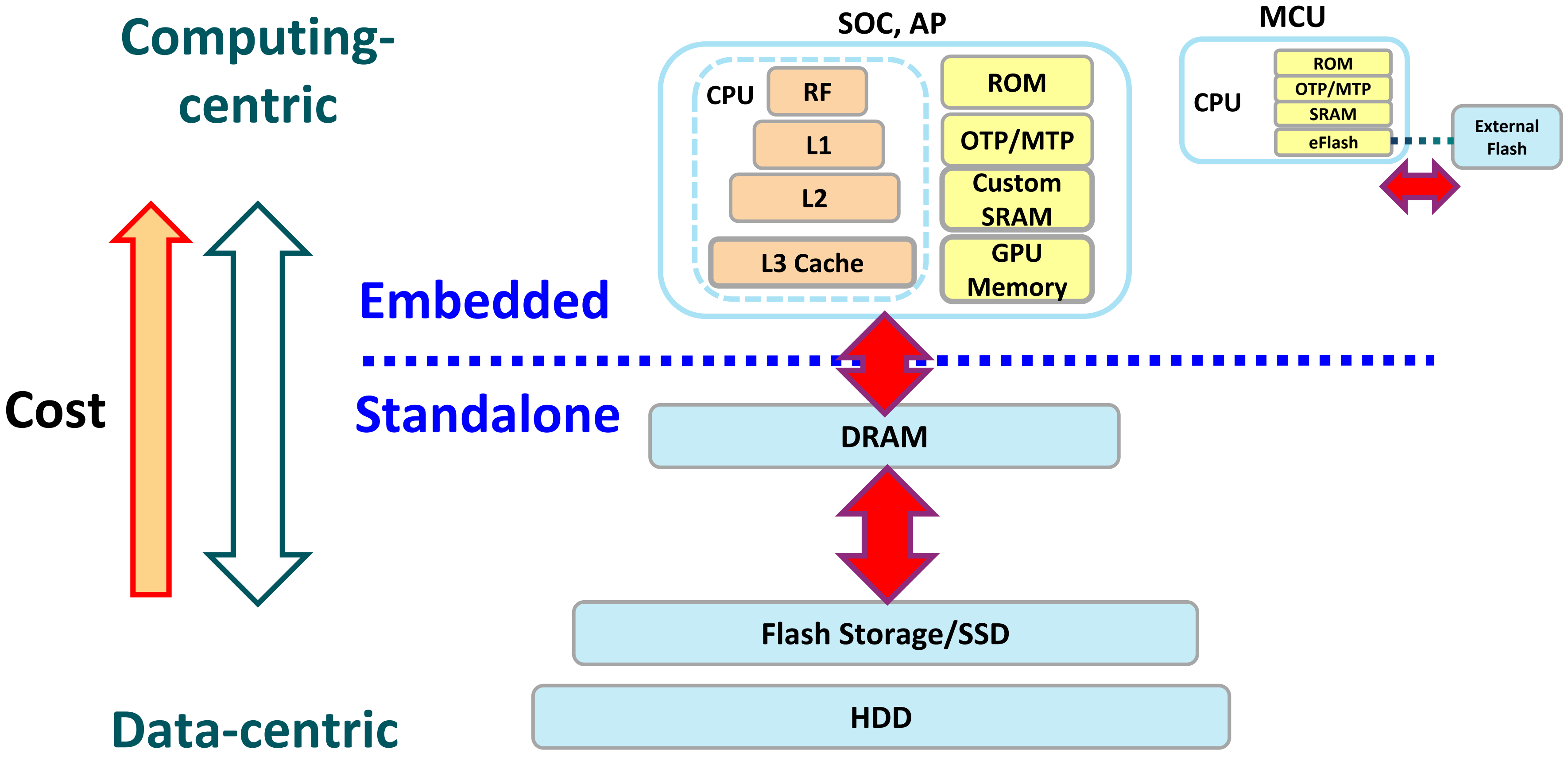
Working Memory → **Speed; Endurance**

Storage Memory → **Density; Retention**

Problem Statement 1

"Memory Wall"

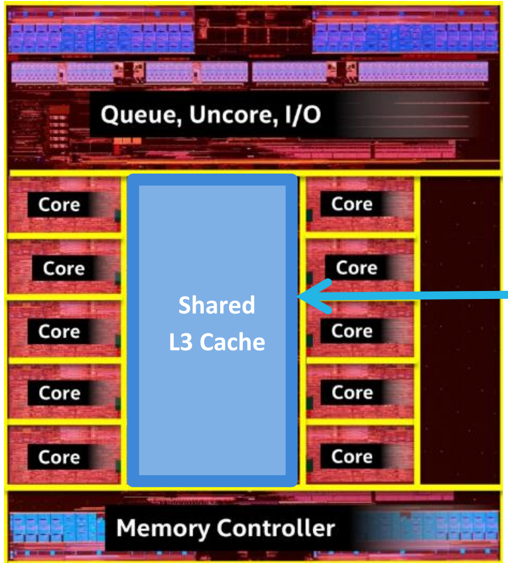
Overall system performance & power governed more by memory subsystem than by CPU subsystem



Problem Statement 2

Many-Core Processors

Increasing SRAM area & leakage power overhead



25 Mbytes of L3 cache (60 Mbytes for 24 cores)

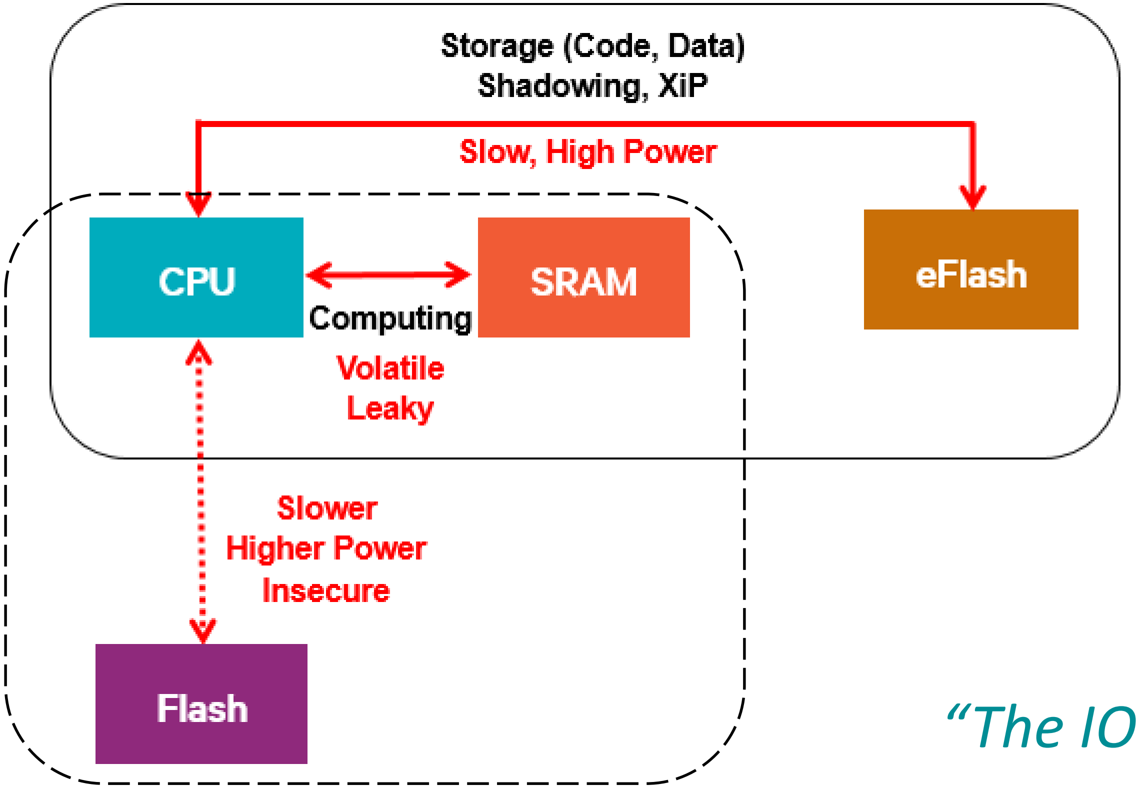
Intel Broadwell-E (14nm node)

- Datacenter applications projecting ~120 Mbytes (960 Mb) L3 cache at 10nm and beyond.
- More expensive at advanced nodes (6T-SRAM: ~550 F^2 at 7 nm *vs.* ~150 F^2 at 40 nm)
- High standby/leakage power (worse at high T)

Problem Statement 3

IOT & Embedded System

Inherent drawbacks caused by memory limitations



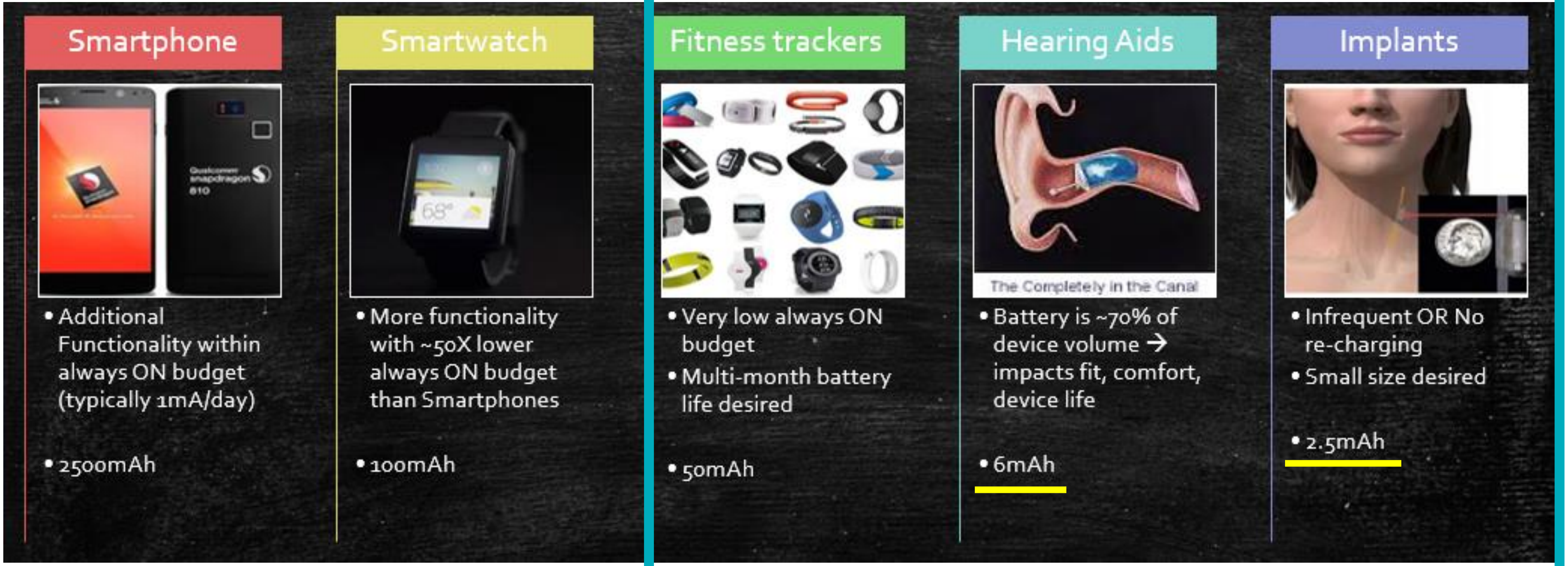
- **Energy-hungry**
- **Poor form factor**
- **High cost**
- **Security vulnerability**

“The IOT is an NVM problem.”

Greg Yeric, ARM (2015 IEDM Plenary Talk)

A New Perspective on Energy Efficiency

New Demand and Criteria for Wearable and Bioelectronic Devices

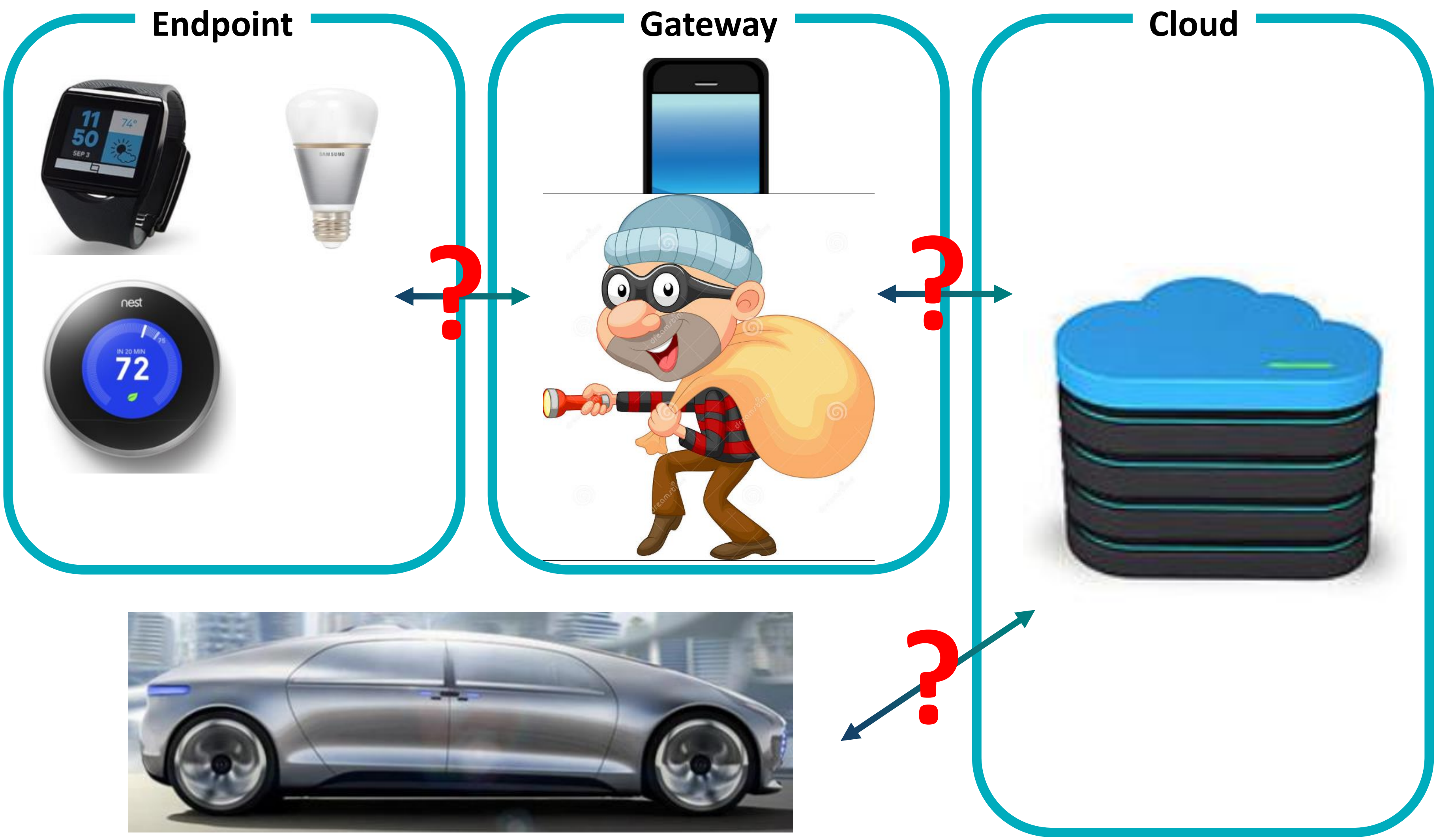


Smartphone	Smartwatch	Fitness trackers	Hearing Aids	Implants
			The Completely in the Canal	
• Additional Functionality within always ON budget (typically 1mA/day)	• More functionality with ~50X lower always ON budget than Smartphones	• Very low always ON budget • Multi-month battery life desired	• Battery is ~70% of device volume → impacts fit, comfort, device life	• Infrequent OR No re-charging • Small size desired
• 2500mAh	• 100mAh	• 50mAh	• 6mAh	• 2.5mAh

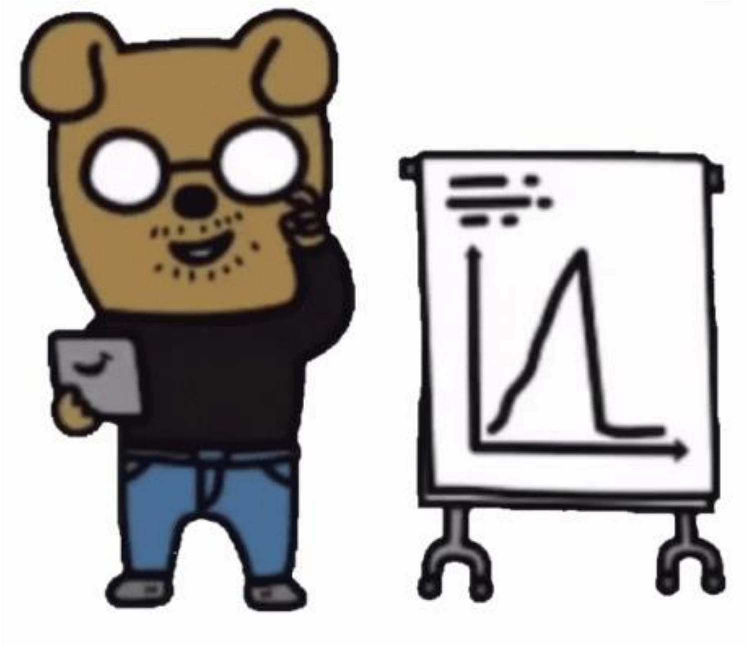
Critical Challenge: Battery Life (Energy Efficiency)

A New Perspective on Security & Privacy

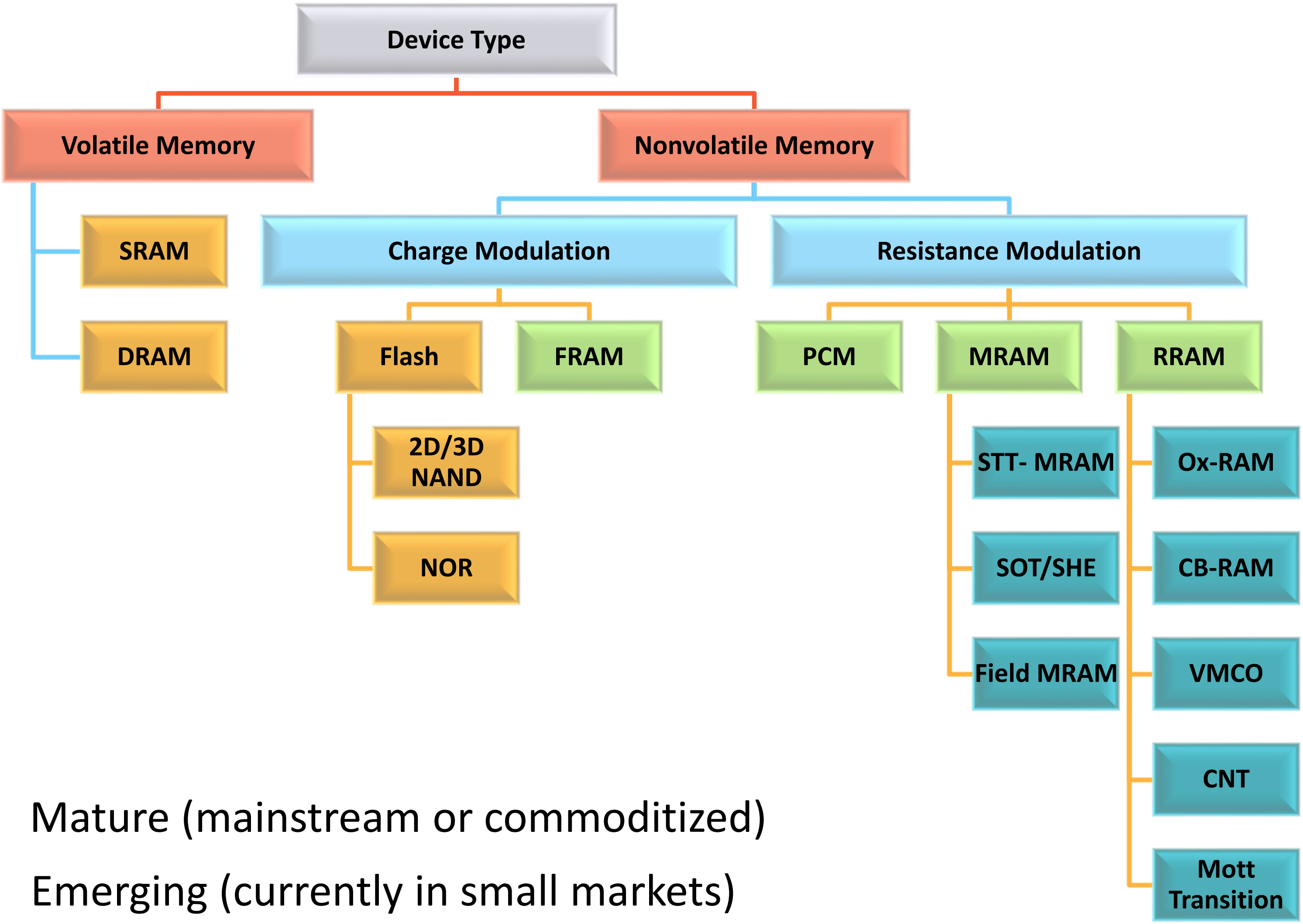
Demand for secure memory and HW primitives (e.g. PUF)



**Problems,
new requirements,
and opportunities
demand advanced
memories…**



Memory Classification



- Device Type
  - Volatile Memory
    - SRAM
    - DRAM
  - Nonvolatile Memory
    - Charge Modulation
      - Flash
        - 2D/3D NAND
        - NOR
      - FRAM
    - Resistance Modulation
      - PCM
      - MRAM
        - STT- MRAM
        - SOT/SHE
        - Field MRAM
      - RRAM
        - Ox-RAM
        - CB-RAM
        - VMCO
        - CNT
        - Mott Transition

🟧 Mature (mainstream or commoditized)

🟩 Emerging (currently in small markets)

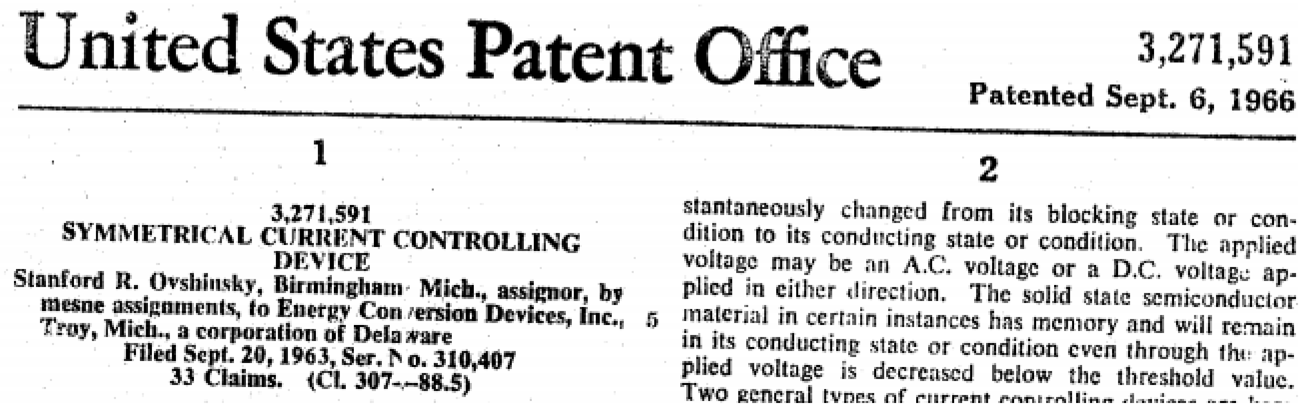
Phase Change Memory

PCM

PC-RAM

PRAM

PCM: Early History



United States Patent Office

3,271,591

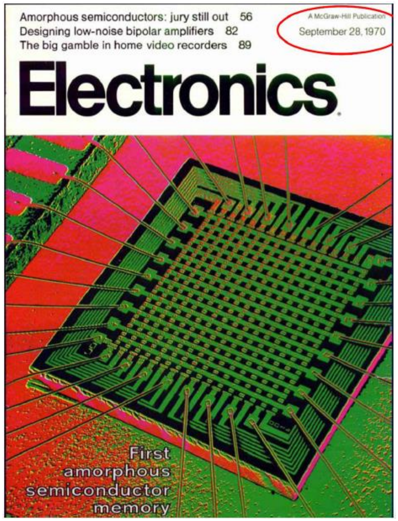
Patented Sept. 6, 1966

1

3,271,591
SYMMETRICAL CURRENT CONTROLLING DEVICE
Stanford R. Ovshinsky, Birmingham, Mich., assignor, by mesne assignments, to Energy Conversion Devices, Inc., Troy, Mich., a corporation of Delaware
Filed Sept. 20, 1963, Ser. No. 310,407
33 Claims. (Cl. 307—88.5)

2

stantaneously changed from its blocking state or condition to its conducting state or condition. The applied voltage may be an A.C. voltage or a D.C. voltage applied in either direction. The solid state semiconductor material in certain instances has memory and will remain in its conducting state or condition even through the applied voltage is decreased below the threshold value. Two general types of current controlling



Amorphous semiconductors: jury still out 56
Designing low-noise bipolar amplifiers 82
The big gamble in home video recorders 89

A McGraw-Hill Publication
September 28, 1970

Electronics

First amorphous semiconductor memory

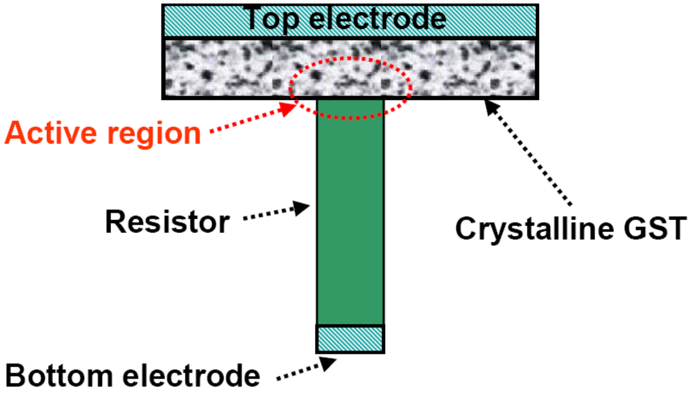
Neale, Nelson, & Moore, *Electronics*, 1970

“Nonvolatile and reprogrammable, the read-mostly memory is here”

- Density: 256 bits
- Die Size: 122-by-131-mil (10.3 mm^2)
- Read: 2.5 mA, < 5 V
- Set: 5 mA, ~25 V, 10 ms
- Reset: < 200 mA, 25 V, 5 µs

PCM: Basic Concept

Phase-change Element

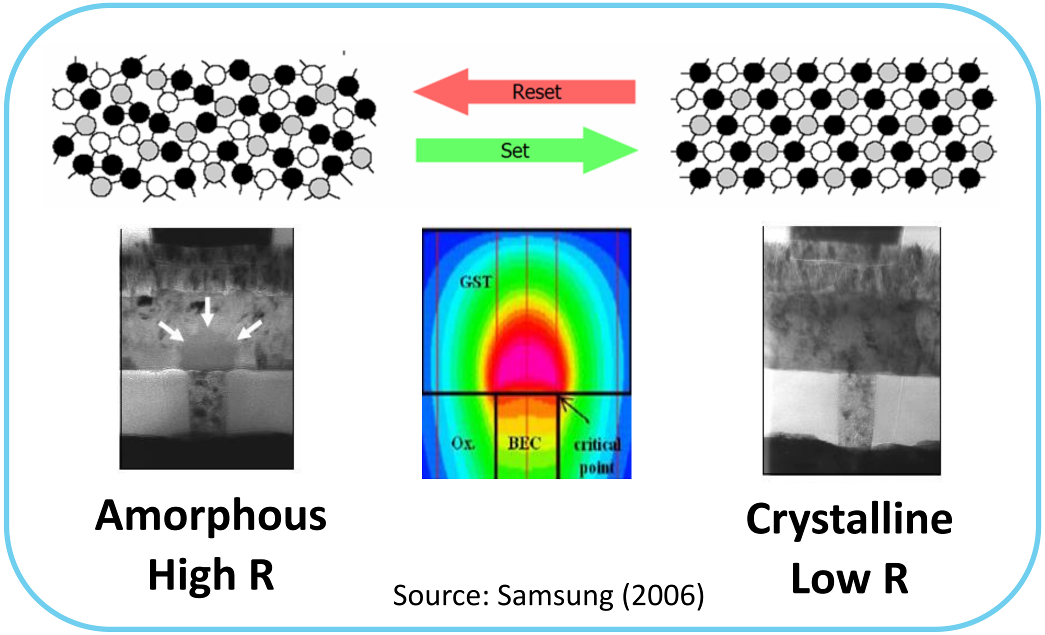


Active region

Resistor

Crystalline GST

Bottom electrode

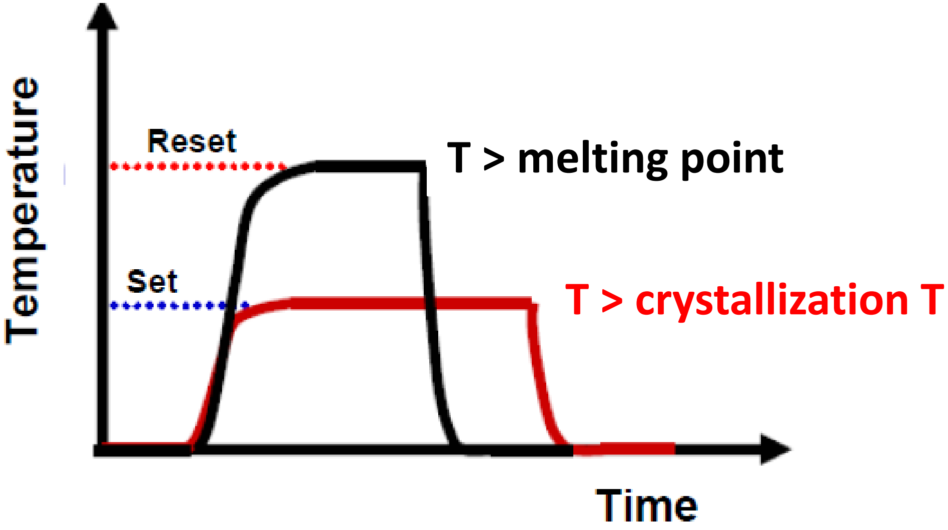


Amorphous
High R

Crystalline
Low R

Source: Samsung (2006)

- Chalcogenide alloy (e.g. Ge-Sb-Te/GST))
- Programming: Joule heating followed by natural cooling
- **Relatively simple physics!**

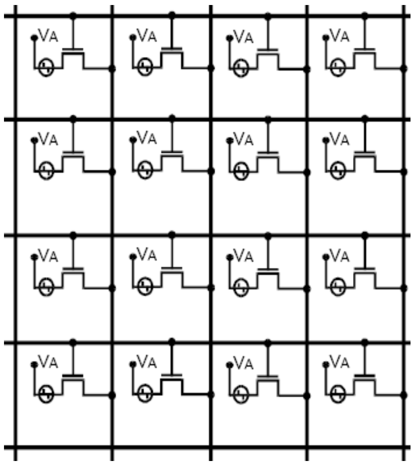


T > melting point

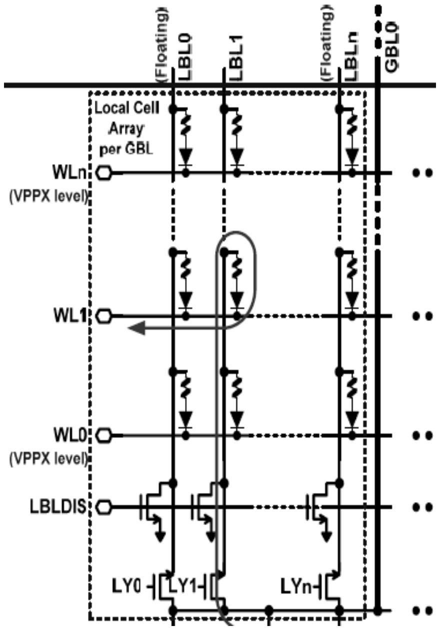
T > crystallization T

PCM: Cell and Array Architecture

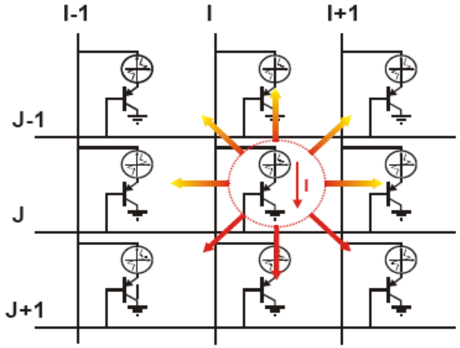
Cell = Access Device + Phase-change Element



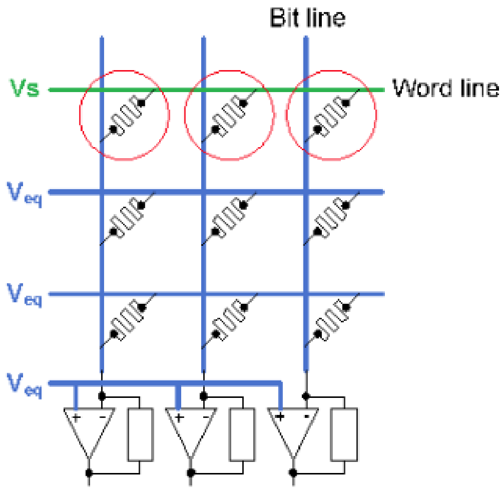
1FET-1R



1Diode-1R



1BJT-1R



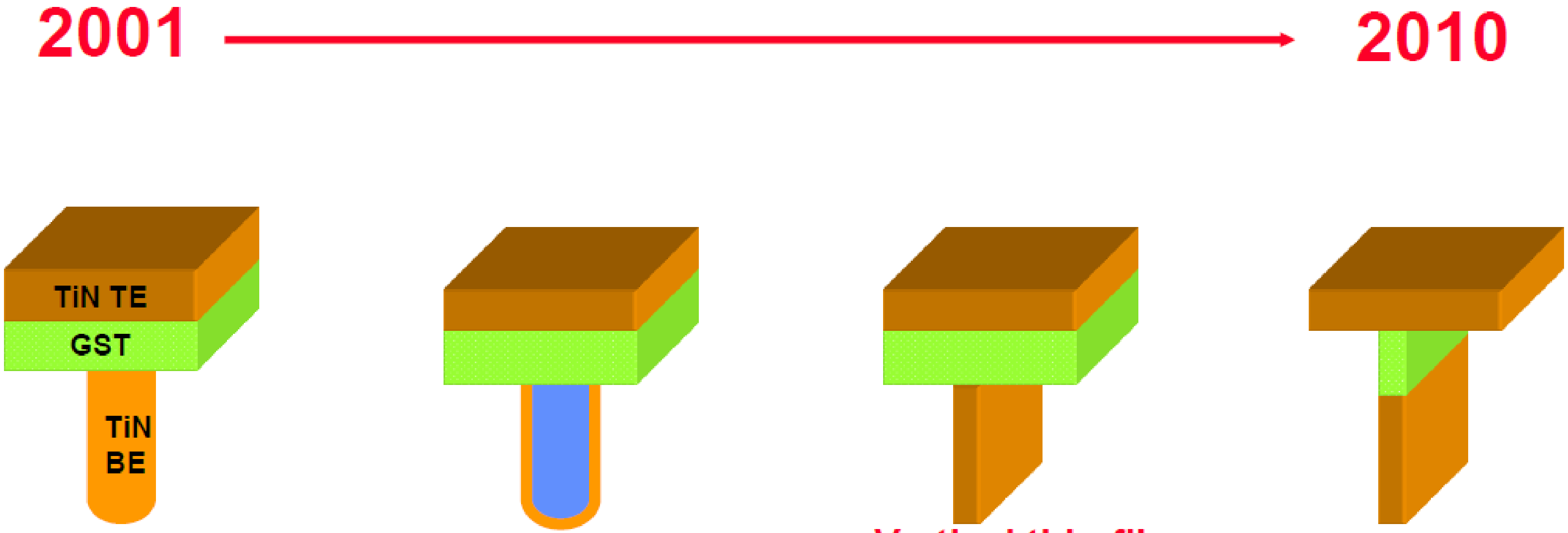
Cross-bar Array

The required characteristics of access FET, diode, or BJT are largely governed by the upper limit of the reset current (to drive localized melting) at a target cell size.

PCM: Evolution of Cell Configuration

Improve thermal isolation

Source: H.-L. Lung (ITRS ERD, 2014)



Solid bottom electrode

Ring bottom electrode

Vertical thin film bottom electrode

Thermal confined cell

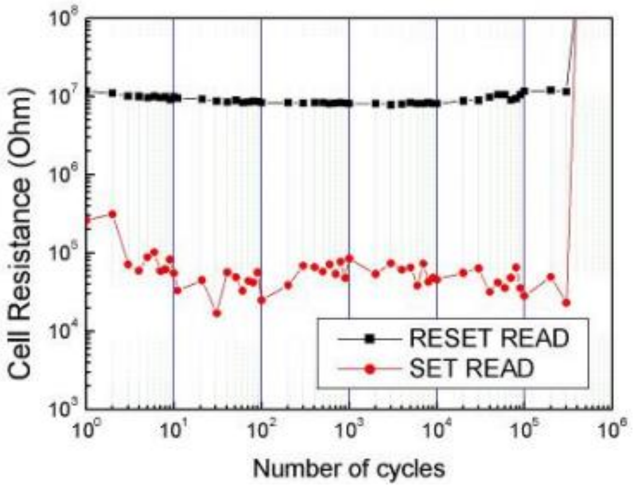
>90% of heat is wasted during reset

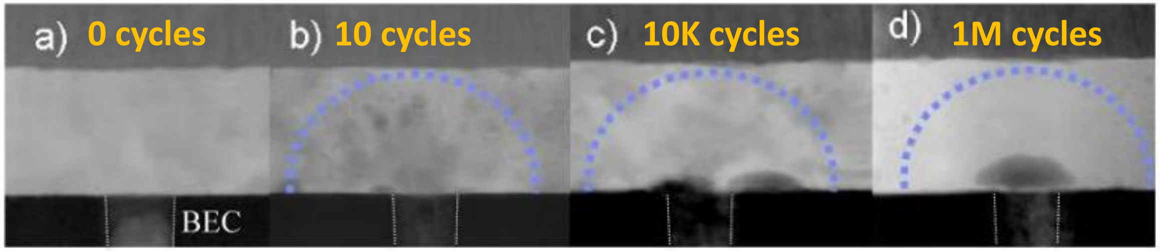
Lower reset current/power
Improved endurance & retention

PCM: Reliability

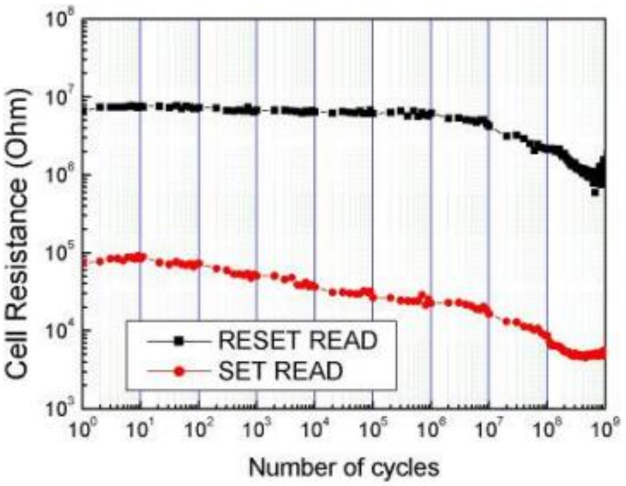
Cycling Endurance

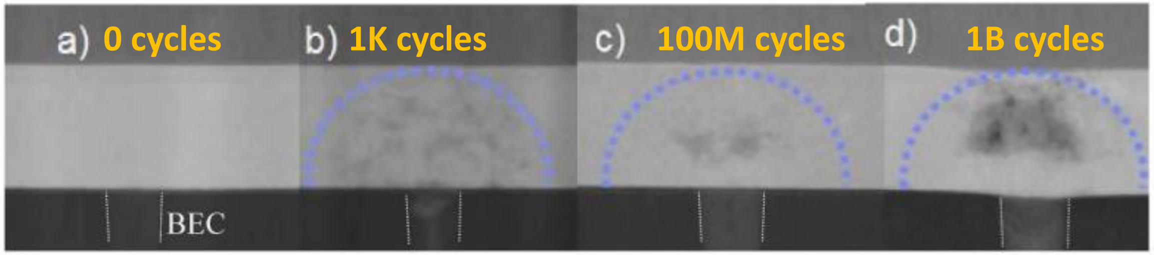
Chen et al. (Macronix-IBM, IMW, 2009)





Updoped GST

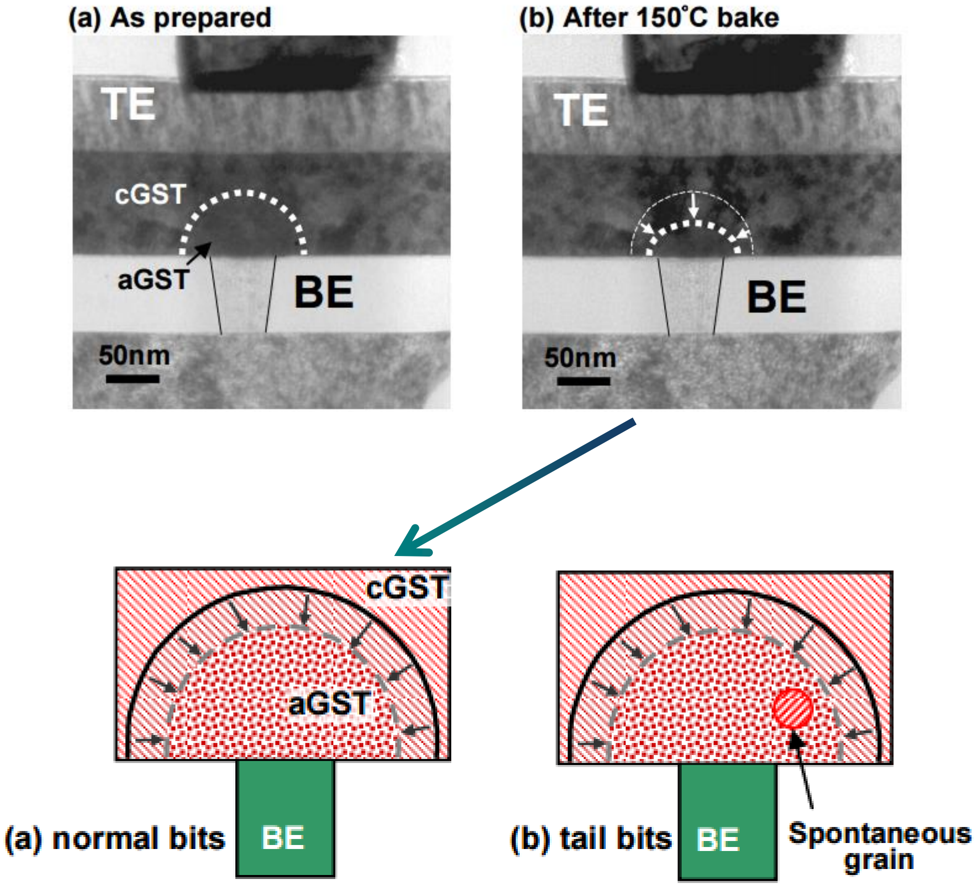


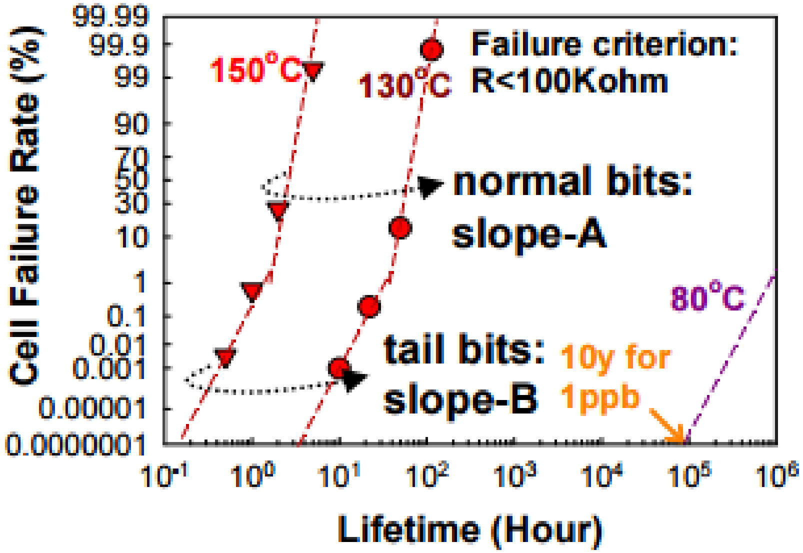


Doped GST

PCM: Reliability

Retention

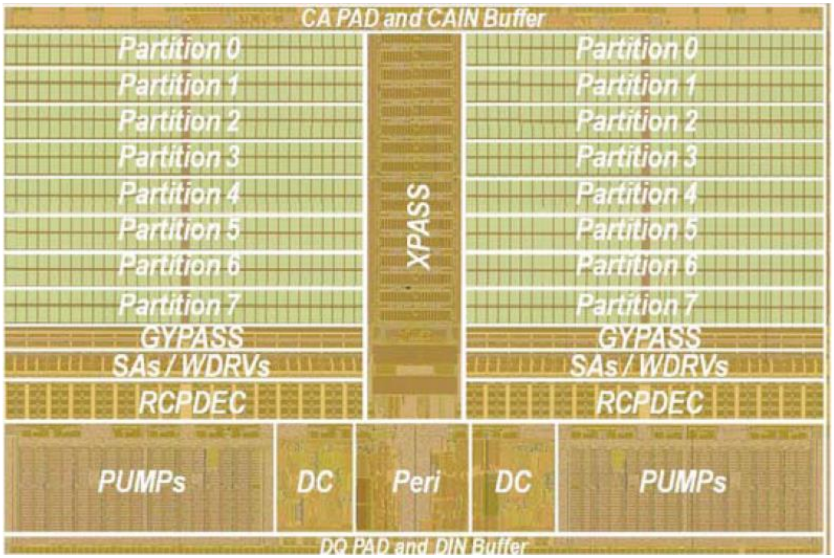


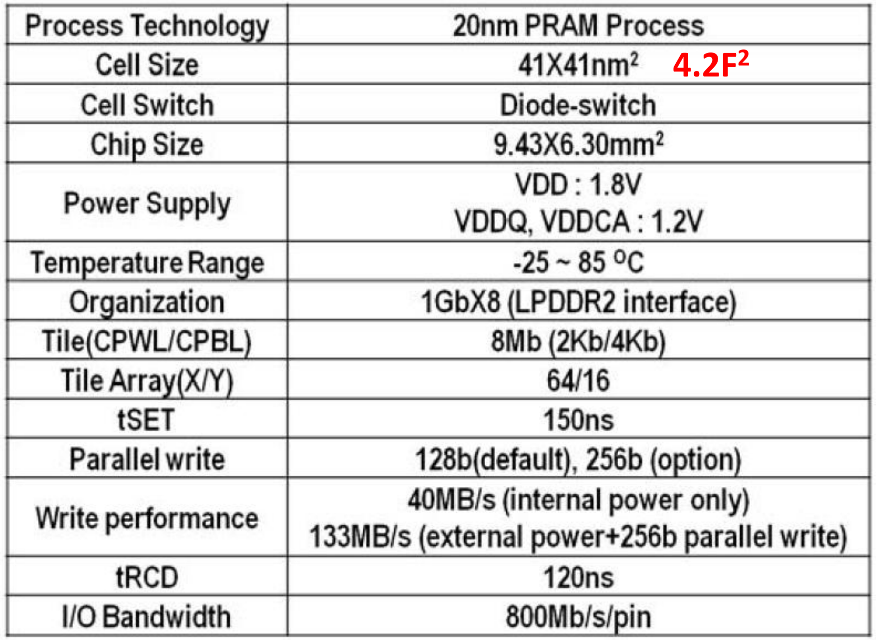


Shih et al. (Macronix-IBM, IEDM, 2008)

PCM: Prototype

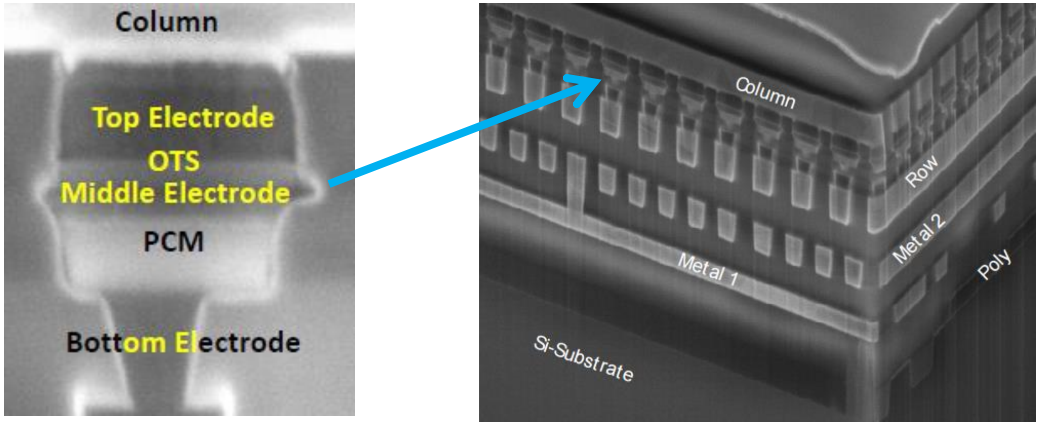
Samsung 8Gb PCM (ISSCC, 2012)





Process Technology	20nm PRAM Process
Cell Size	41X41nm^2 **4.2F^2**
Cell Switch	Diode-switch
Chip Size	9.43X6.30mm^2
Power Supply	VDD : 1.8V VDDQ, VDDCA : 1.2V
Temperature Range	-25 ~ 85 °C
Organization	1GbX8 (LPDDR2 interface)
Tile(CPWL/CPBL)	8Mb (2Kb/4Kb)
Tile Array(X/Y)	64/16
tSET	150ns
Parallel write	128b(default), 256b (option)
Write performance	40MB/s (internal power only) 133MB/s (external power+256b parallel write)
tRCD	120ns
I/O Bandwidth	800Mb/s/pin

PCM: Evolution to 3D

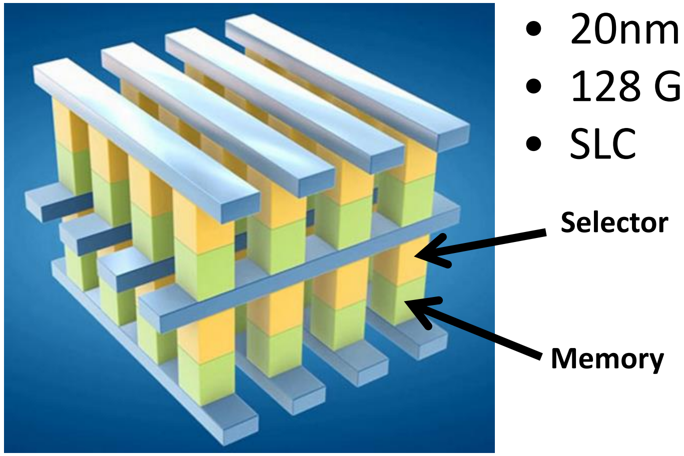


Kau et al. (Intel & Numonyx, IEDM, 2009)

- PCMS
- Phase-change memory (PCM) coupled with a **selector** (OTS)
- OTS: Ovonic Threshold Switch
- 64 Mb
- Endurance: 10^6 cycles

3D XPoint (Intel & Micron, 2016)

- 20nm node
- 128 Gb
- SLC



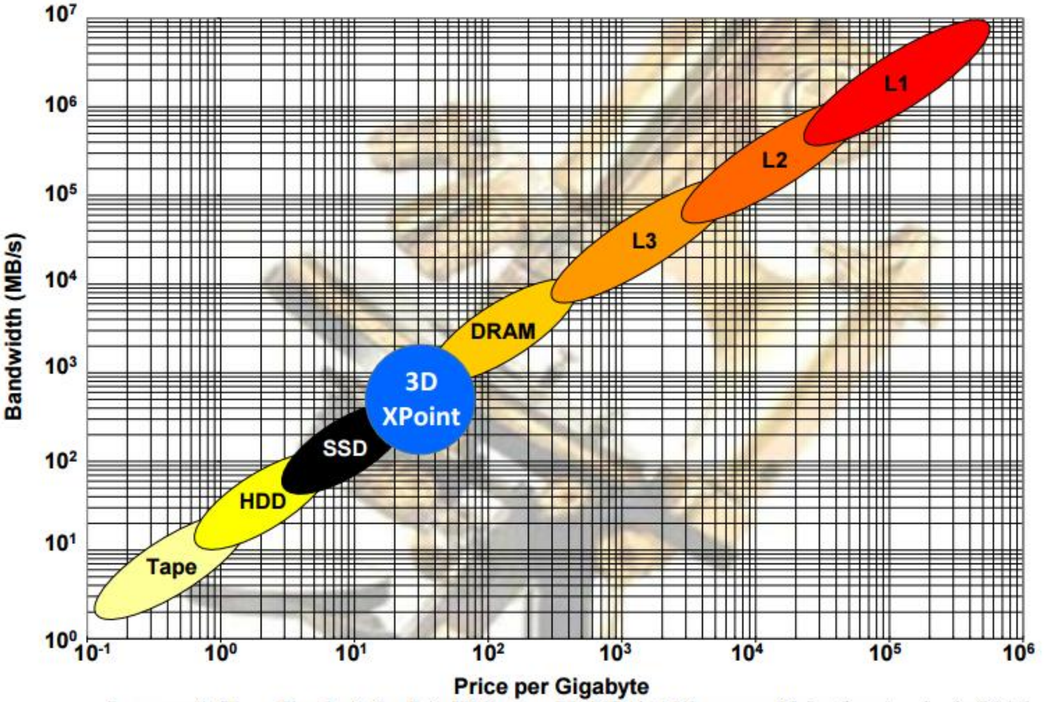
Intel Optane Memory Series (2017)

Chip Density	16 GB (128 Gb)	32 GB
Read Latency	7 μs	9 μs
Write Latency	18 μs	30 μs
Random Read	190K IOPS	240K IOPS
Random Write	35K IOPS	65K IOPS
Sequential Read	900 MB/s	1350 MB/s
Sequential Write	145 MB/s	290 MB/s
Power (Active/Idle)	3.5 W / 1 W	
Endurance (Lifetime Writes)	182.5 TB	

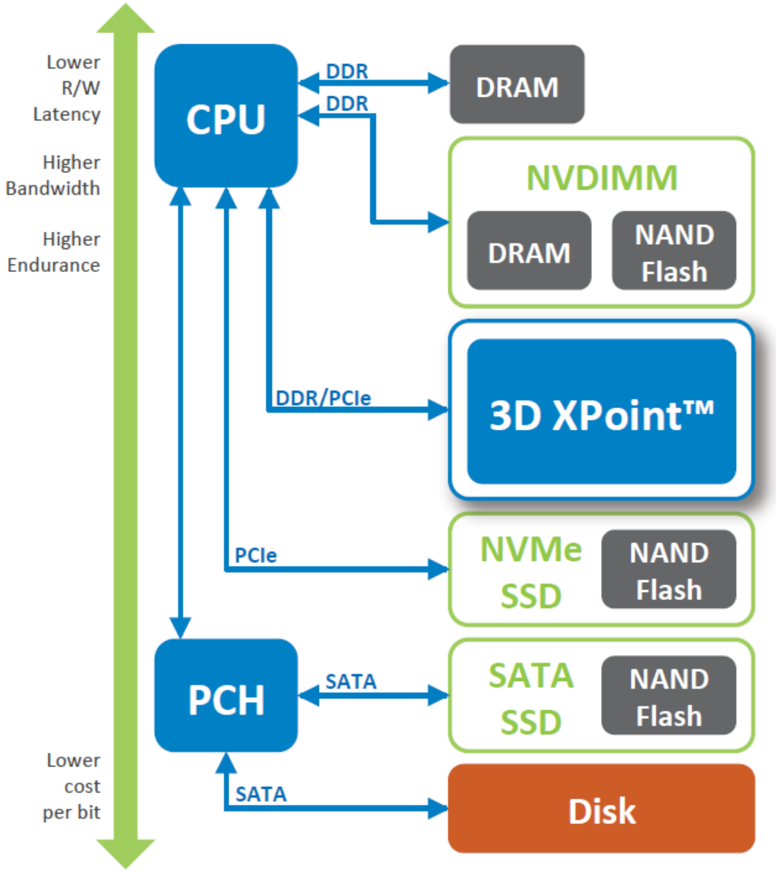
Source: Intel.com

3D XPoint as Storage Class Memory

It does not replace DRAM, or NAND storage, but it adds a new *layer* to improve the subsystem



Source: ***A Close Look at the Intel/Micron 3D XPoint Memory***, Objective Analysis 2015



Source: Intel-Micron, 2015

Magnetoresistive RAM

MRAM

Spin-transfer-torque MRAM

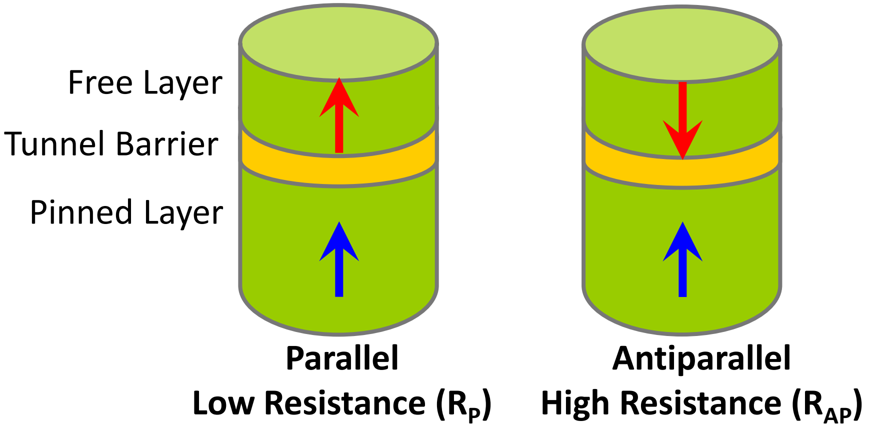
STT-MRAM

ST-MRAM

STT-RAM

A Building Block: Magnetic Tunnel Junction

Multiple flavors, but perpendicular MTJ



Free Layer

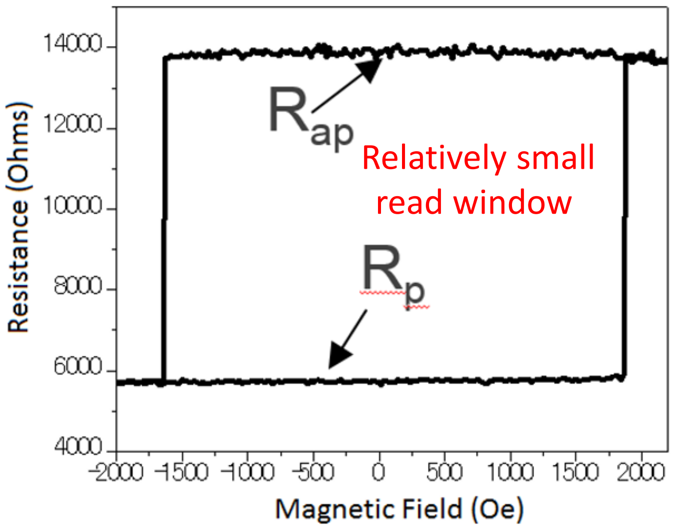
Tunnel Barrier

Pinned Layer

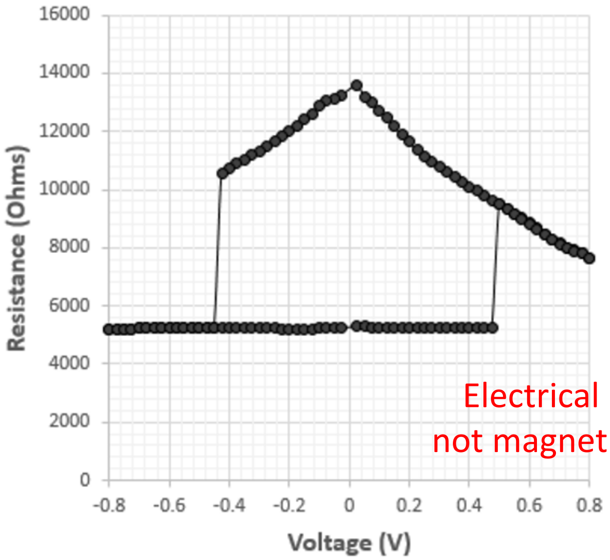
Parallel
Low Resistance (R_P)

Antiparallel
High Resistance (R_{AP})

Electrical resistance varied by relative electron spin alignment : Magnetoresistance (MR)



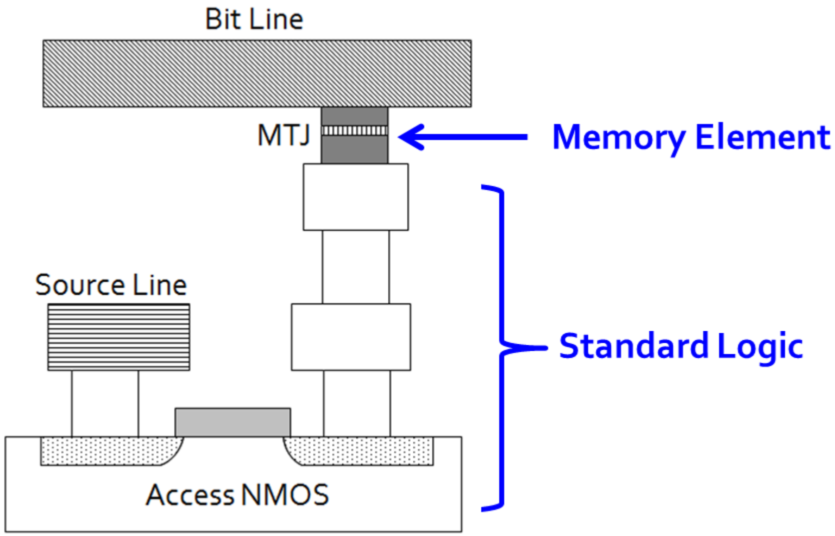
Relatively small read window



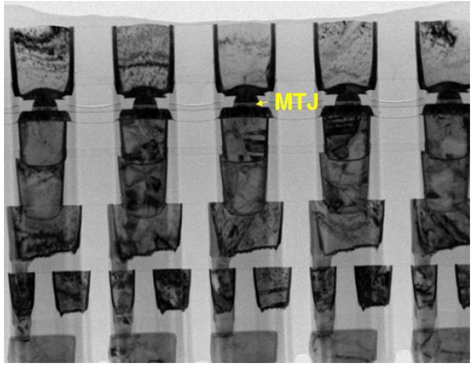
Electrical switching, not magnetic switching

MRAM Snapshot

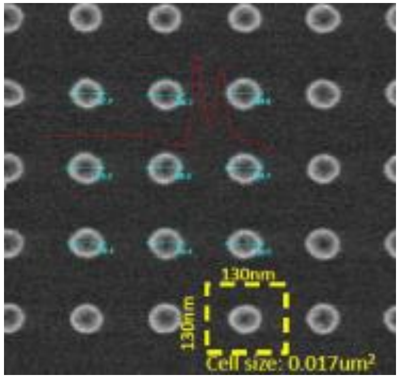
A new class of memory: Nonvolatile RAM



- Fast NVM
- High endurance
- ~3 additional masks over baseline logic
- Low voltage (no charge pump)
- Scalable



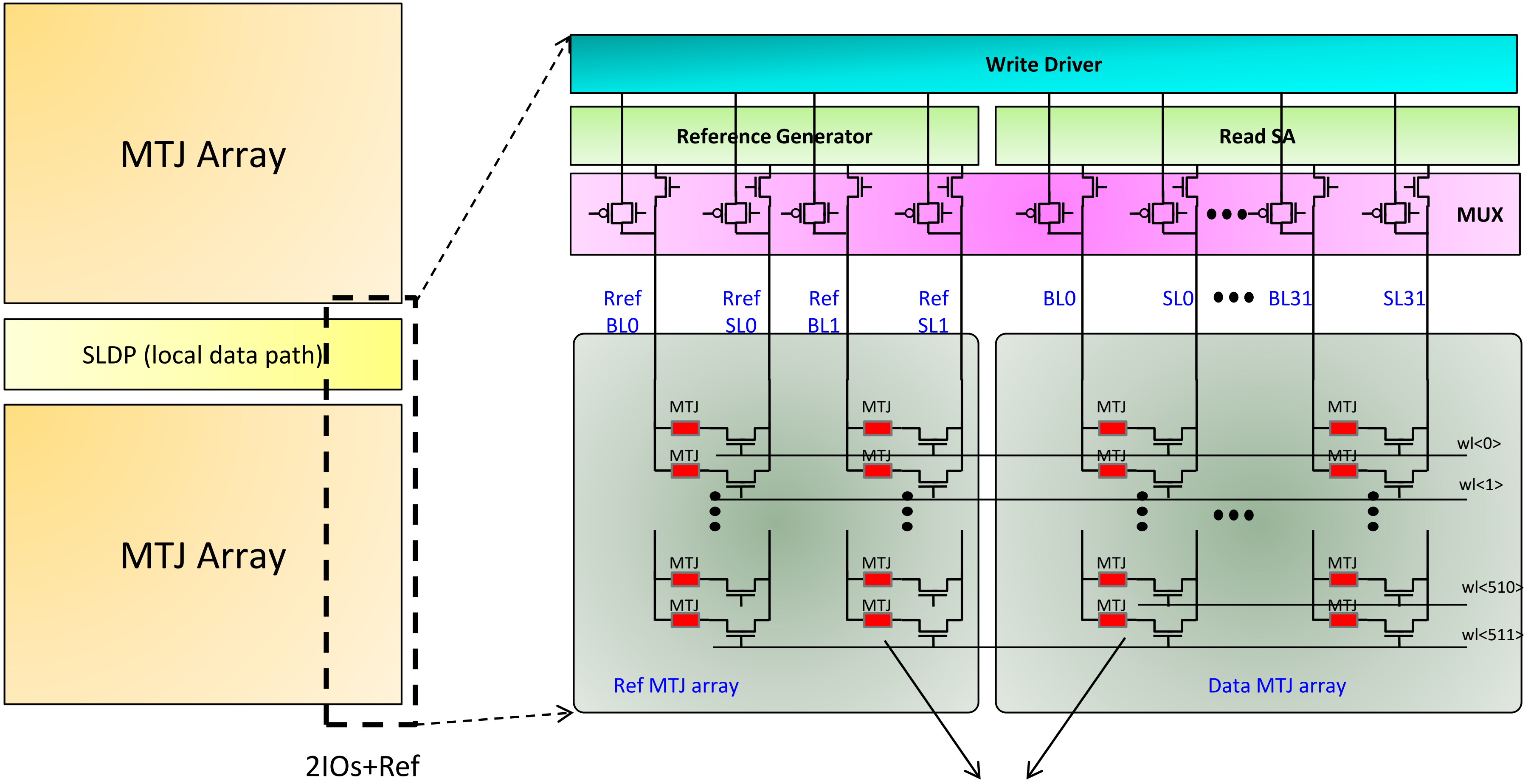
Lu et al. (Qualcomm & TDK)
IEDM, 2015



Park et al. (Qualcomm & Applied Mat.)
IEDM, 2015

Operation voltage on MTJ
Read: ~0.1 V
Write: 0.3 – 0.5 V

MRAM Array Architecture

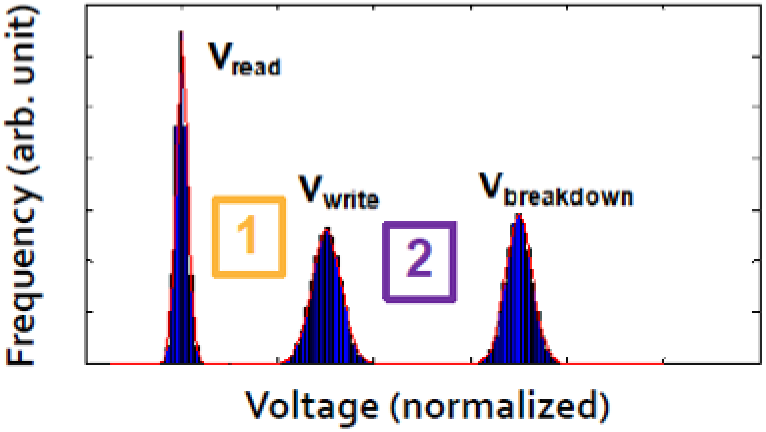


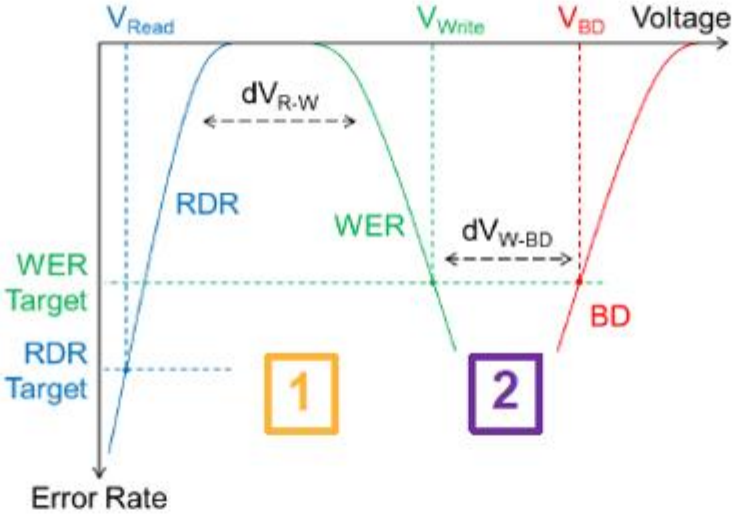
Use the same bitcell for both data and reference array

- Small read window → Design for robust read (sensing) is critical
- Balancing switching asymmetry and source generation

Challenges for MRAM Design and Reliability

Narrow design window for deeply scaled nodes





Prevent read error

- Low V_{Read} (~0.1V)
- High TMR
- Fast fall off of RDR slope

Prevent write error

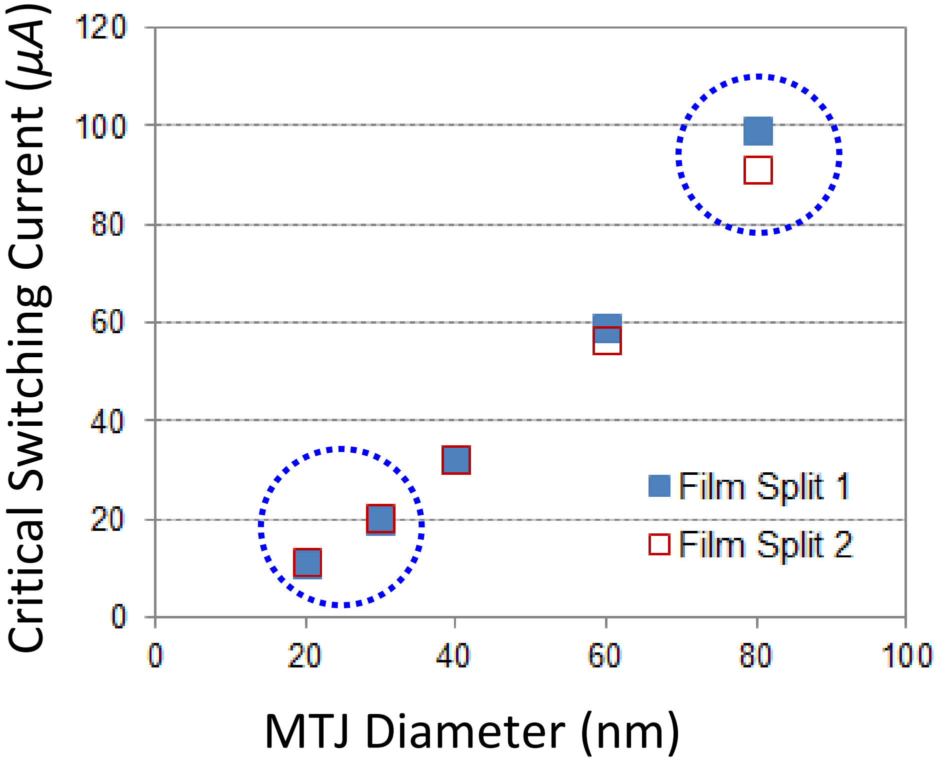
- Low V_{Write}
- Fast fall off of WER slope

Improve barrier reliability

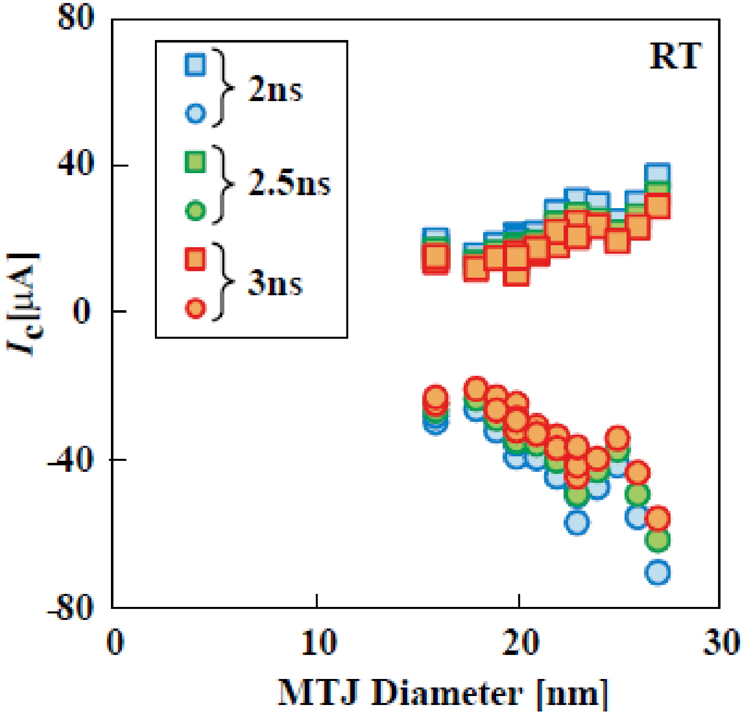
- High V_{BD}
- Contain TDDB

MRAM Device Scalability: I_c

Most important bitcell and design parameter



Kang, VLSI Symp., 2014



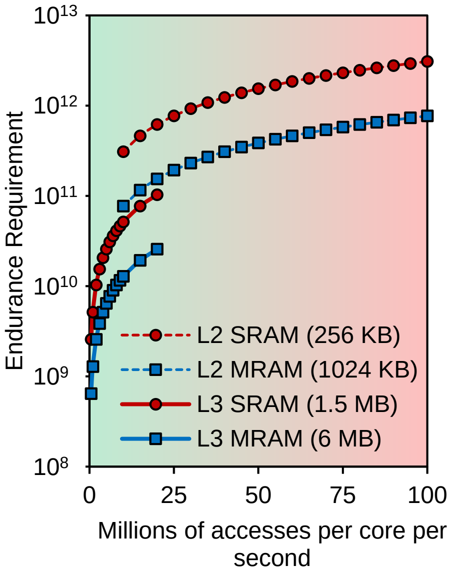
Saida et al., VLSI Symp., 2016

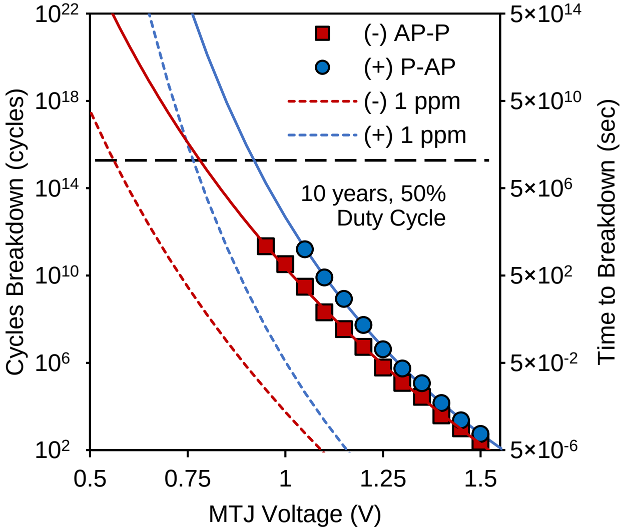
At small dimensions, dynamic current consumption becoming comparable with that of SRAM cell current

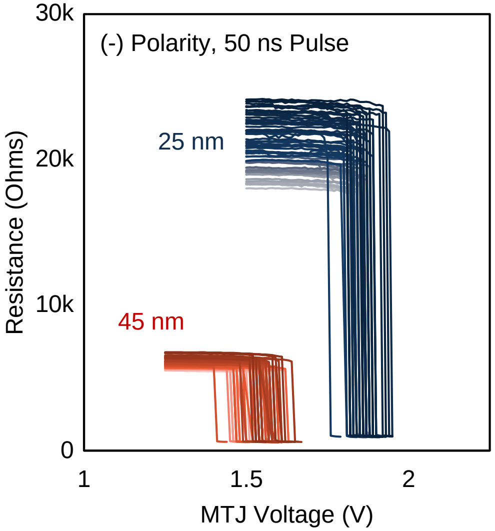
MRAM Device Scalability: Endurance

Practically unlimited endurance for cache applications

Kan et al., IEDM, 2016







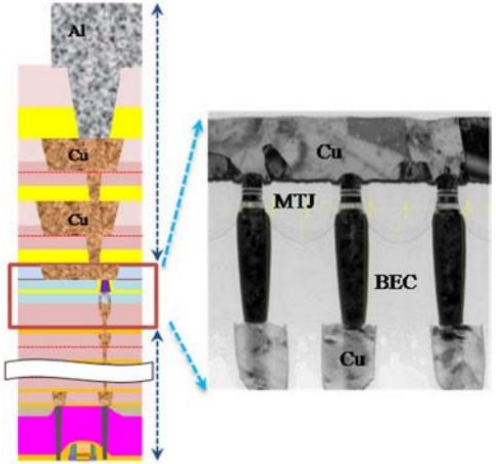
Intrinsically solid

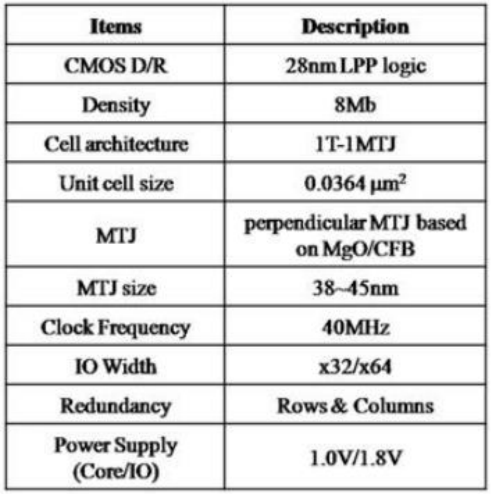
Better with MTJ scaling

In real life, subjected to design robustness & defect control

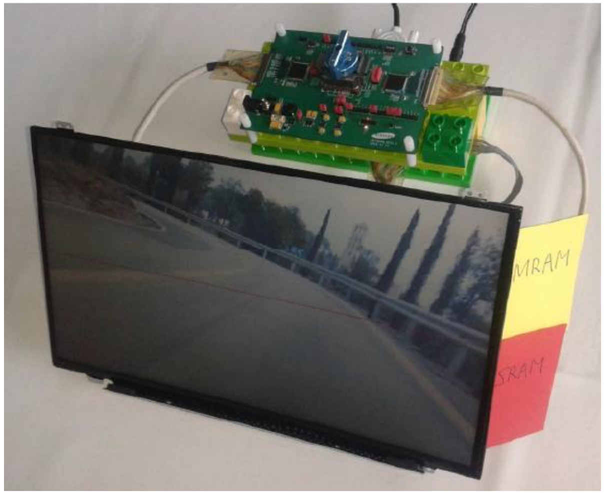
MRAM: Prototypes

Samsung (IEDM, 2016 / 7th MRAM Global Innovation Forum)

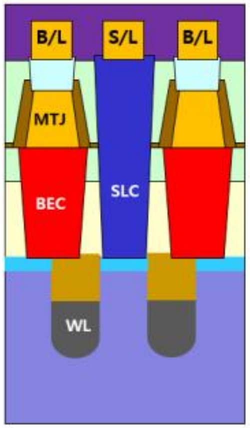


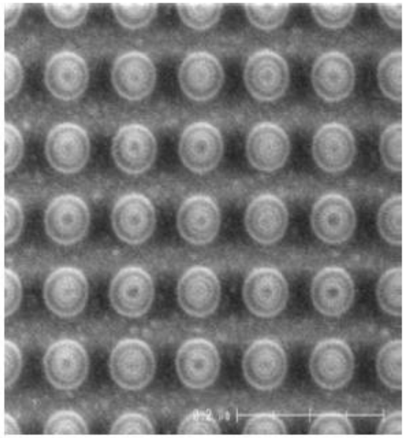


Items	Description
CMOS D/R	28nm LPP logic
Density	8Mb
Cell architecture	1T-1MTJ
Unit cell size	0.0364 μm²
MTJ	perpendicular MTJ based on MgO/CFB
MTJ size	38~45nm
Clock Frequency	40MHz
IO Width	x32/x64
Redundancy	Rows & Columns
Power Supply (Core/IO)	1.0V/1.8V



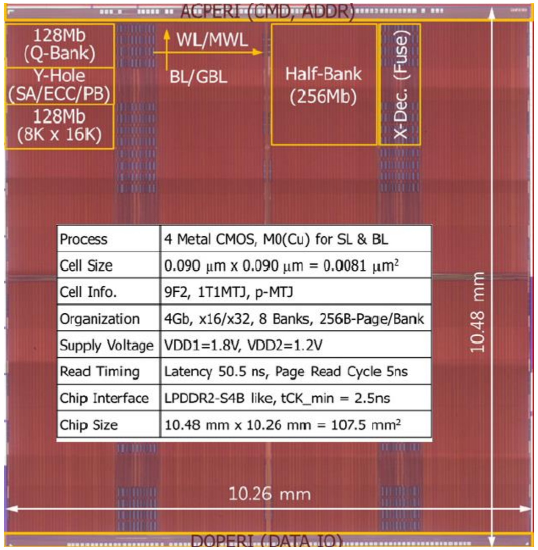
SK Hynix-Toshiba (IEDM, 2016 / ISSCC, 2017)





4Gb

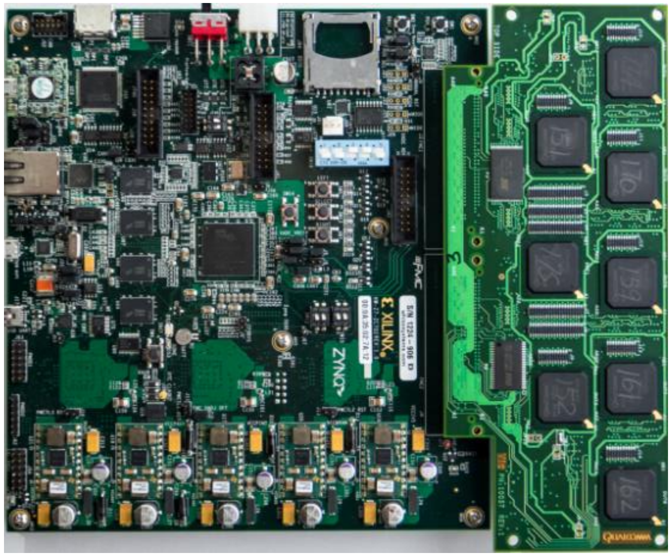
9F² (30nm)



Process	4 Metal CMOS, M0(Cu) for SL & BL
Cell Size	0.090 μm x 0.090 μm = 0.0081 μm²
Cell Info.	9F2, 1T1MTJ, p-MTJ
Organization	4Gb, x16/x32, 8 Banks, 256B-Page/Bank
Supply Voltage	VDD1=1.8V, VDD2=1.2V
Read Timing	Latency 50.5 ns, Page Read Cycle 5ns
Chip Interface	LPDDR2-S4B like, tCK_min = 2.5ns
Chip Size	10.48 mm x 10.26 mm = 107.5 mm²

MRAM: Qualcomm Demo System

MRAM integrated along with PSRAM and NOR Flash for performance and power benchmarking



Integrated into a demo tablet

~350X faster than Flash

~3X faster than PSRAM

Kang, IMW, 2016

MRAM can unify PSRAM (volatile RAM) and NOR (nonvolatile storage) with PPAC advantages

MRAM In Production


EE|Times

DESIGNLINES | MEMORY DESIGNLINE

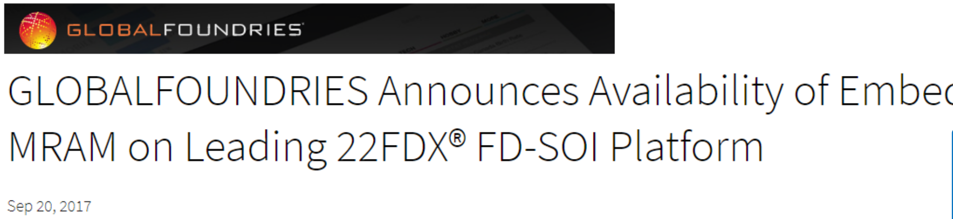
Samsung Says It's Shipping 28-nm Embedded MRAM

By Dylan McGrath, 03.07.19 4


eeNews ANALOG

EVERSPIN SHIPS 1GBIT STT-MRAM

January 14, 2019 //By Peter Clarke


GLOBALFOUNDRIES

GLOBALFOUNDRIES Announces Availability of Embedded MRAM on Leading 22FDX® FD-SOI Platform

Sep 20, 2017


eeNews ANALOG

TSMC EMBEDDED MRAM IS KEY TO GYRFALCON AI CHIP

November 22, 2018 //By Peter Clarke


TECHSPOT

Intel confirms non-volatile MRAM is being produced with high yield

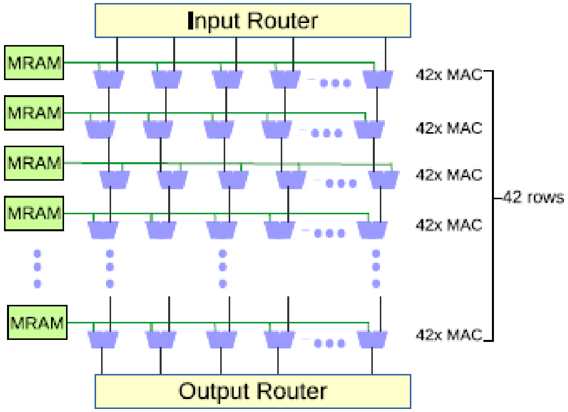
A candidate to replace DRAM, SRAM, and flash

By **Greg Synek** on February 21, 2019, 7:50 AM

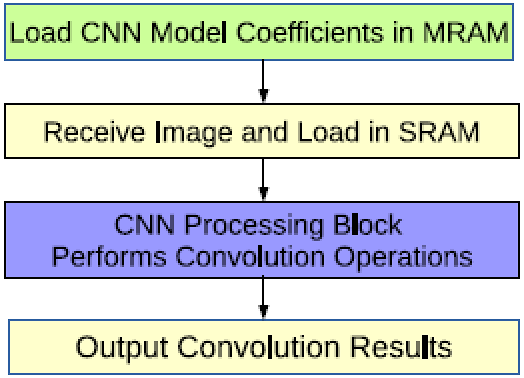
MRAM for Processing-in-Memory CNN Accelerator

A single-chip solution for Mobile and IOT applications

From Gyrfalcon Technologies (2018)



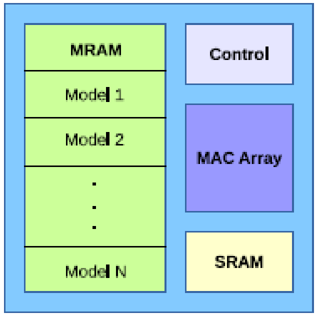
CNN Matrix Processing Engine (MPE)


Load CNN Model Coefficients in MRAM

Receive Image and Load in SRAM

CNN Processing Block
Performs Convolution Operations

Output Convolution Results



CNN block with memory array

Power(mW)			
Conditions		MRAM	SRAM
Room Tempreature	Dynamic	38.3	39.2
Room Tempreature	Standby	5.5	34.3
High Tempreature	Dynamic	35.4	43.1
High Tempreature	Standby	7.2	136

- 22nm eMRAM (40 MB)
- 9.9 TOPS/W

Resistive RAM

RRAM

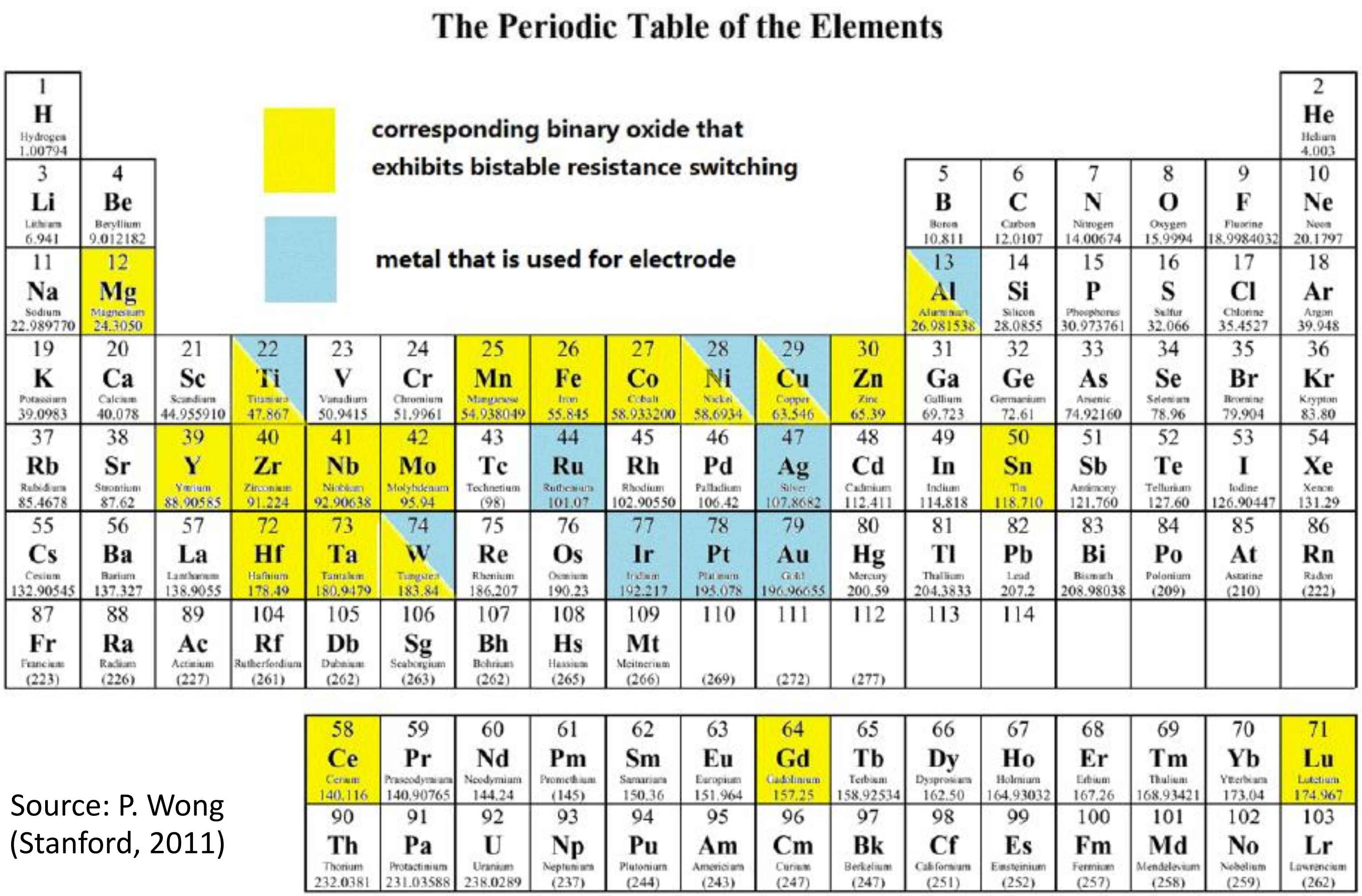
ReRAM

Conductive Bridge RAM

CB-RAM

RRAM: Materials

Two-terminal resistive switching elements (excluding PCM and MRAM). Found in numerous combinations of materials.



The Periodic Table of the Elements

🟨 corresponding binary oxide that exhibits bistable resistance switching

🟦 metal that is used for electrode

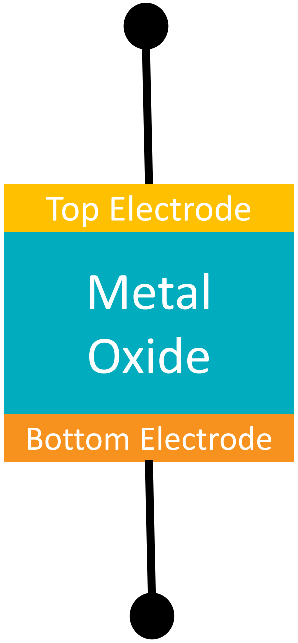
1 H Hydrogen 1.00794																	2 He Helium 4.003
3 Li Lithium 6.941	4 Be Beryllium 9.012182											5 B Boron 10.811	6 C Carbon 12.0107	7 N Nitrogen 14.00674	8 O Oxygen 15.9994	9 F Fluorine 18.9984032	10 Ne Neon 20.1797
11 Na Sodium 22.989770	🟨 12 Mg Magnesium 24.3050											🟨🟦 13 Al Aluminum 26.981538	14 Si Silicon 28.0855	15 P Phosphorus 30.973761	16 S Sulfur 32.066	17 Cl Chlorine 35.4527	18 Ar Argon 39.948
19 K Potassium 39.0983	20 Ca Calcium 40.078	21 Sc Scandium 44.955910	🟨🟦 22 Ti Titanium 47.867	23 V Vanadium 50.9415	24 Cr Chromium 51.9961	🟨 25 Mn Manganese 54.938049	🟨 26 Fe Iron 55.845	🟨 27 Co Cobalt 58.933200	🟨🟦 28 Ni Nickel 58.6934	🟨🟦 29 Cu Copper 63.546	🟨 30 Zn Zinc 65.39	31 Ga Gallium 69.723	32 Ge Germanium 72.61	33 As Arsenic 74.92160	34 Se Selenium 78.96	35 Br Bromine 79.904	36 Kr Krypton 83.80
37 Rb Rubidium 85.4678	38 Sr Strontium 87.62	🟨 39 Y Yttrium 88.90585	🟨 40 Zr Zirconium 91.224	🟨 41 Nb Niobium 92.90638	🟨 42 Mo Molybdenum 95.94	43 Tc Technetium (98)	🟦 44 Ru Ruthenium 101.07	45 Rh Rhodium 102.90550	46 Pd Palladium 106.42	🟦 47 Ag Silver 107.8682	48 Cd Cadmium 112.411	49 In Indium 114.818	🟨 50 Sn Tin 118.710	51 Sb Antimony 121.760	52 Te Tellurium 127.60	53 I Iodine 126.90447	54 Xe Xenon 131.29
55 Cs Cesium 132.90545	56 Ba Barium 137.327	57 La Lanthanum 138.9055	🟨 72 Hf Hafnium 178.49	🟨 73 Ta Tantalum 180.9479	🟨🟦 74 W Tungsten 183.84	75 Re Rhenium 186.207	76 Os Osmium 190.23	🟦 77 Ir Iridium 192.217	🟦 78 Pt Platinum 195.078	🟦 79 Au Gold 196.96655	80 Hg Mercury 200.59	81 Tl Thallium 204.3833	82 Pb Lead 207.2	83 Bi Bismuth 208.98038	84 Po Polonium (209)	85 At Astatine (210)	86 Rn Radon (222)
87 Fr Francium (223)	88 Ra Radium (226)	89 Ac Actinium (227)	104 Rf Rutherfordium (261)	105 Db Dubnium (262)	106 Sg Seaborgium (263)	107 Bh Bohrium (262)	108 Hs Hassium (265)	109 Mt Meitnerium (266)	110 (269)	111 (272)	112 (277)	113	114				

				🟨 58 Ce Cerium 140.116	59 Pr Praseodymium 140.90765	60 Nd Neodymium 144.24	61 Pm Promethium (145)	62 Sm Samarium 150.36	63 Eu Europium 151.964	🟨 64 Gd Gadolinium 157.25	65 Tb Terbium 158.92534	66 Dy Dysprosium 162.50	67 Ho Holmium 164.93032	68 Er Erbium 167.26	69 Tm Thulium 168.93421	70 Yb Ytterbium 173.04	🟨 71 Lu Lutetium 174.967
				90 Th Thorium 232.0381	91 Pa Protactinium 231.03588	92 U Uranium 238.0289	93 Np Neptunium (237)	94 Pu Plutonium (244)	95 Am Americium (243)	96 Cm Curium (247)	97 Bk Berkelium (247)	98 Cf Californium (251)	99 Es Einsteinium (252)	100 Fm Fermium (257)	101 Md Mendelevium (258)	102 No Nobelium (259)	103 Lr Lawrencium (262)

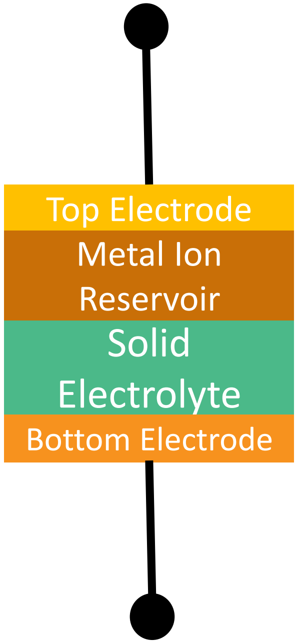
Source: P. Wong (Stanford, 2011)

RRAM: Common Classification

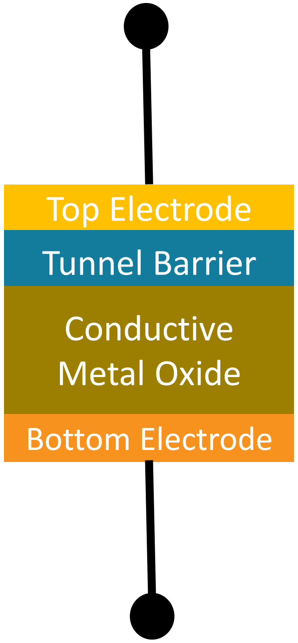
Different materials & switching characteristics



Oxide RRAM (Ox-RAM)
Transition Metal Oxide RRAM



Conductive Bridge RRAM (CB-RAM)
Programmable Metallization Cell (PMC)

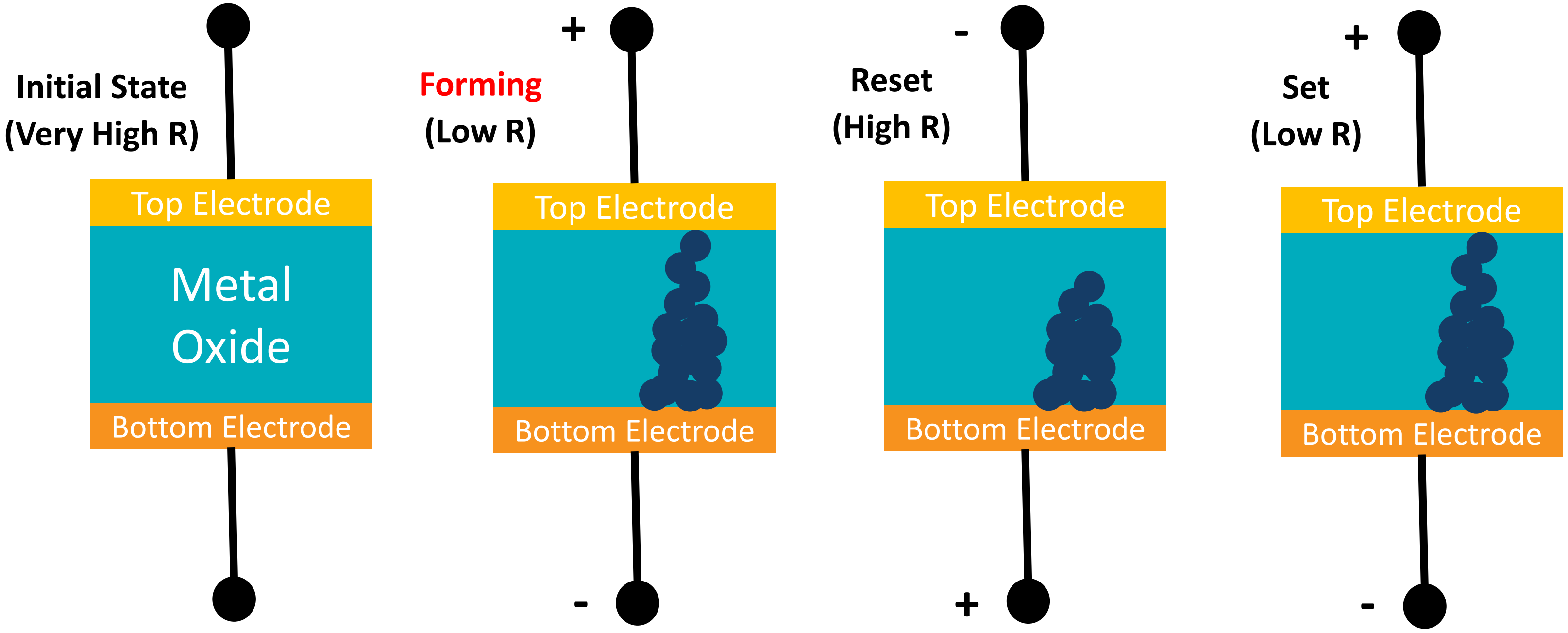


Conductive Metal Oxide RRAM
Vacancy Modulated Conductive Oxide RRAM (VMCO RRAM)

Filamentary Switching (1D)

Interfacial Switching (2D)
Uniform Switching
(No forming)

RRAM: Switching



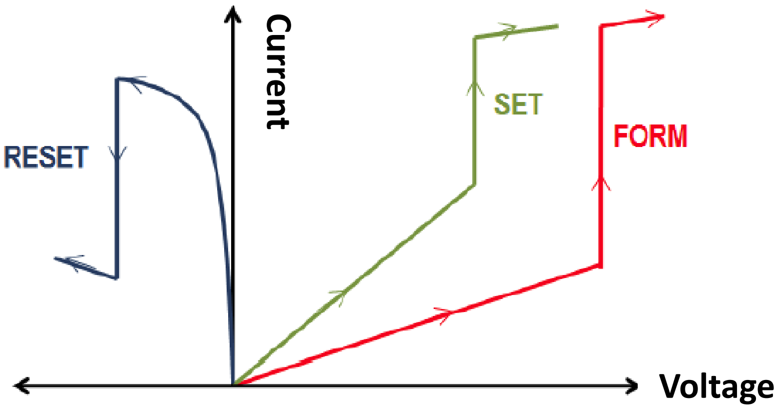
Initial State
(Very High R)

Top Electrode
Metal Oxide
Bottom Electrode

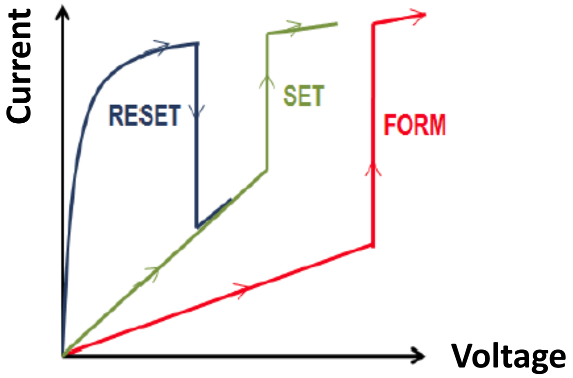
+ **Forming**
(Low R)
Top Electrode
Bottom Electrode
-

- **Reset**
(High R)
Top Electrode
Bottom Electrode
+

+ **Set**
(Low R)
Top Electrode
Bottom Electrode
-

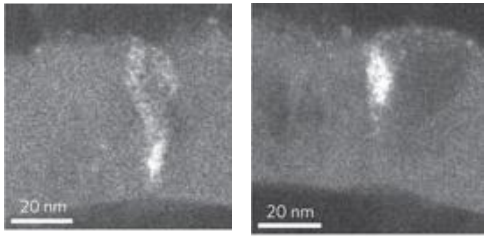


Bipolar Switching



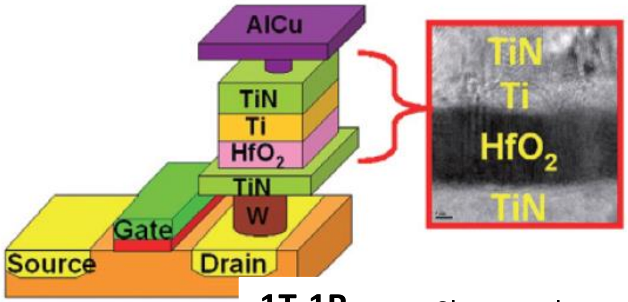
Unipolar Switching

Observation of a filament



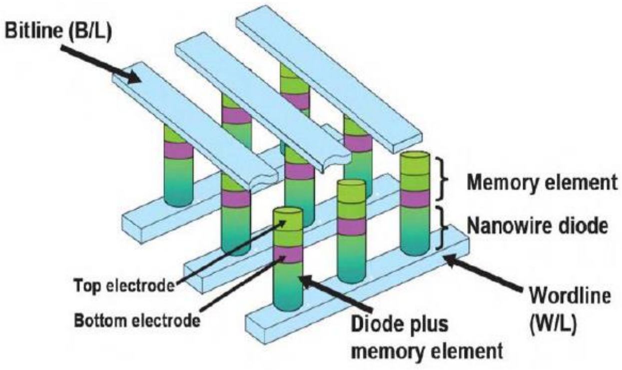
Kwon et al.
Nature Nanotechnology (2010)

RRAM: Cell and Array Architecture



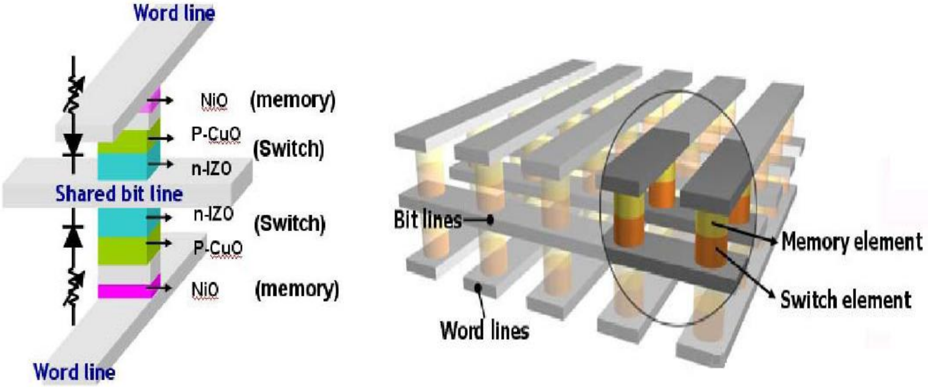
1T-1R

Sheu at al.
(VLSI Symp., 2008)



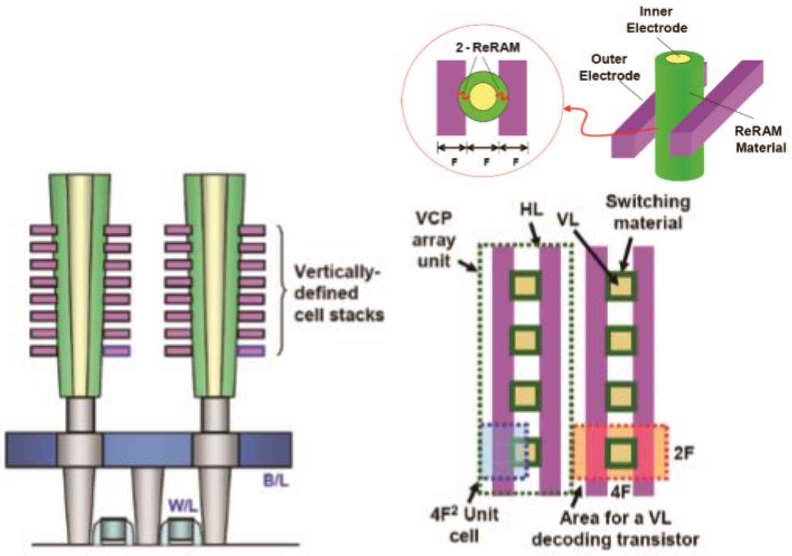
P. Wong (Stanford)

1D-1R
(Diode selector for unipolar RRAM)



1D-1R/1S-1R
(Stacked Cross Point Array)

Lee et al. (IEDM, 2007)

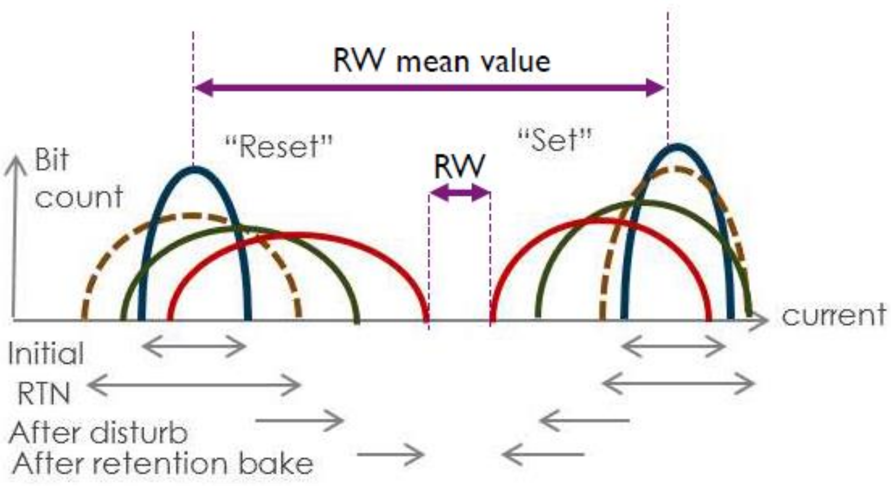


Yoon et al. (VLSI Symp., 2009)

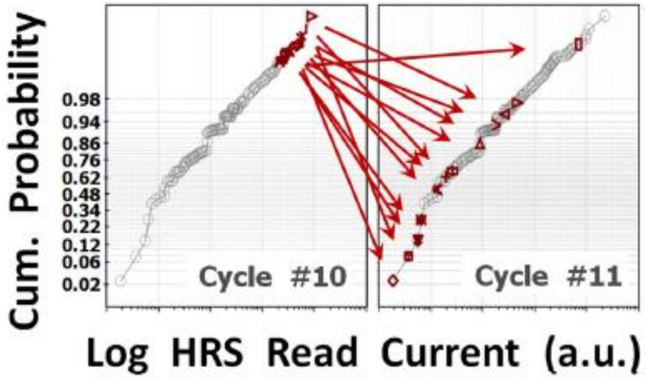
3D Vertical Cross Point RRAM

RRAM: Variability

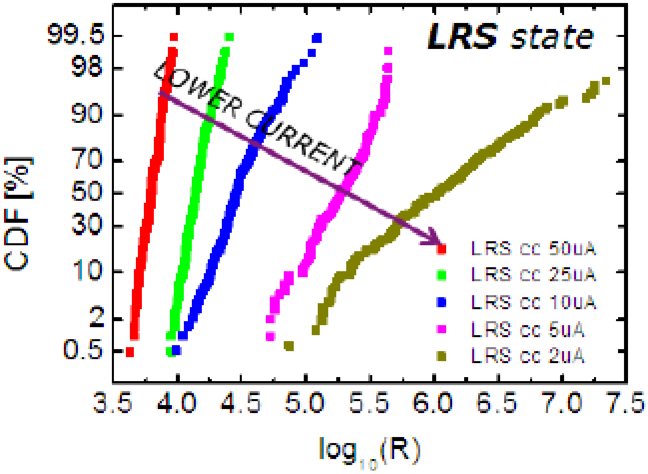
Temporal and spatial variability



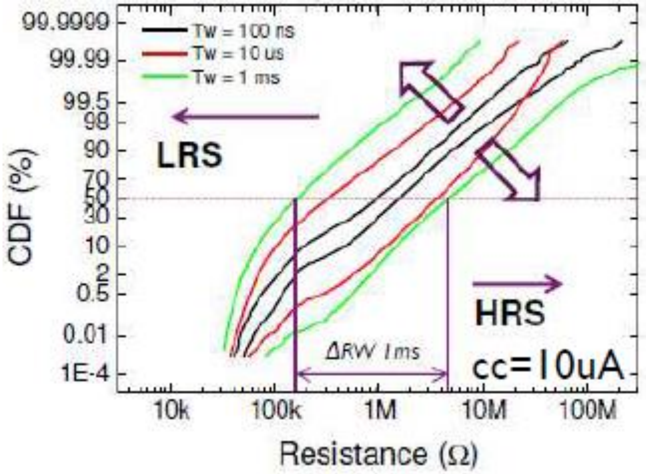
Jurczak (ITRS ERD, 2014)



Sills et al. (VLSI Symp., 2014)



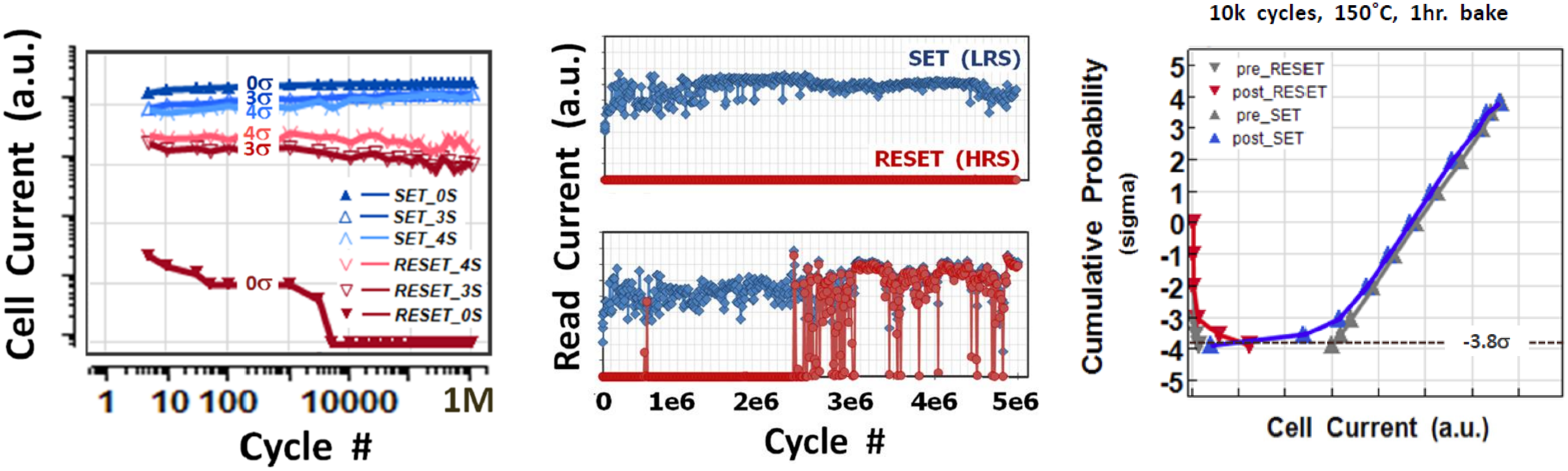
Resistance Variation vs. Switching Current



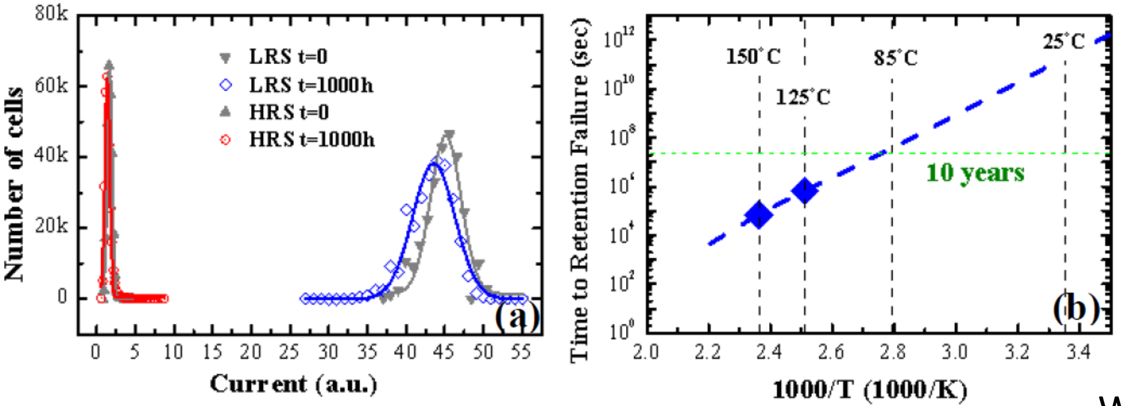
Write Speed vs. Read Margin

RRAM: Reliability

Endurance & Retention



Sills et al. (VLSI Symp., 2014)

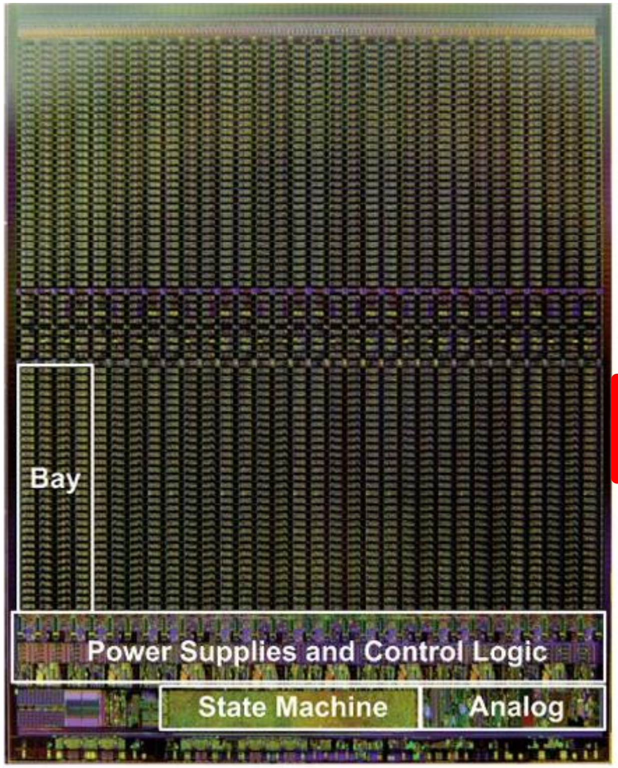


Wei et al. (IEDM, 2011)

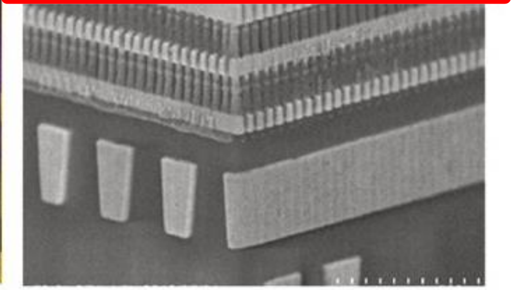
256 Kbit array baked at 150ºC for 1000 hours

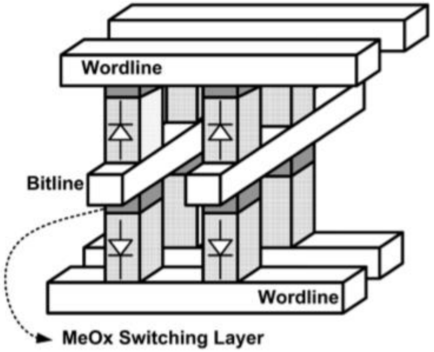
RRAM: Prototypes

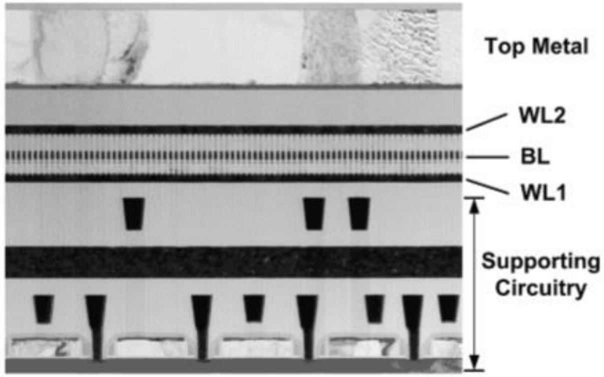
SanDisk-Toshiba RRAM (ISSCC, 2013)



Density	32Gb
Cell Size	24nm x 24nm
Die Size	130.7mm^2
Interface	NAND-Compatible
Page Size	2KB
Read Latency	40us
Write Latency	230us





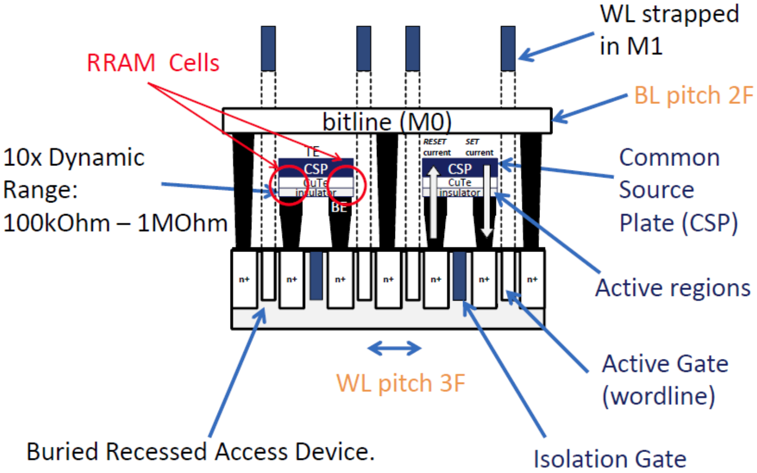


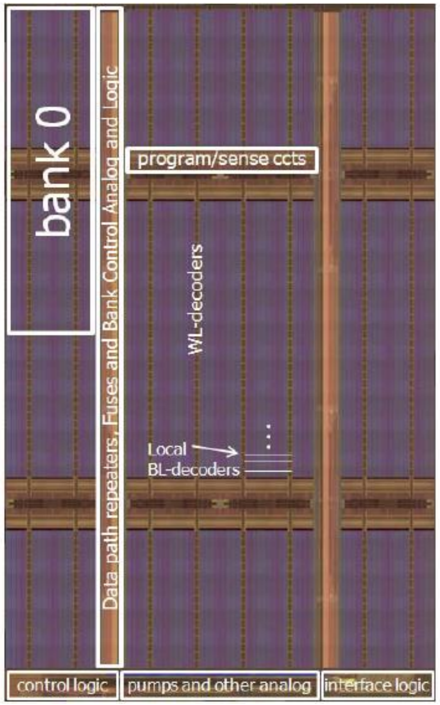
T.-Y. Liu et al. (JSSCC, 2014)

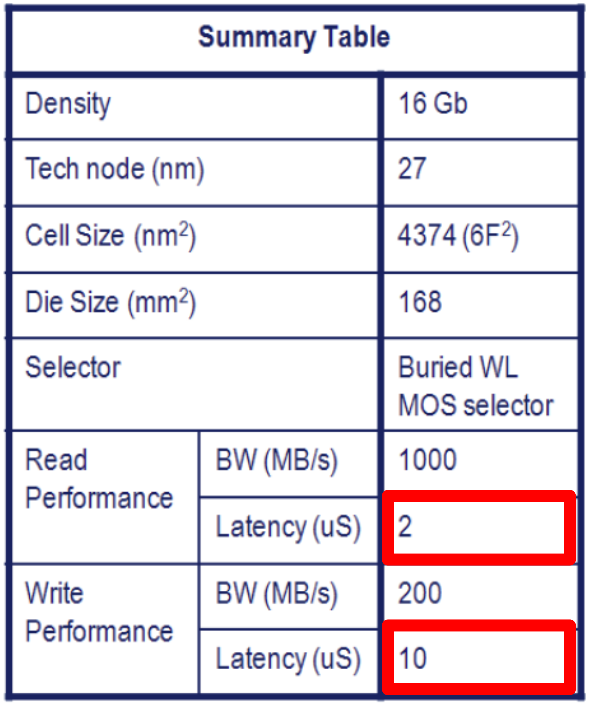
- By far, largest density RRAM test chip
- Relatively slow performance (NAND Flash alternative)

RRAM: Prototype

Micron-Sony CB-RAM (ISSCC, 2014)







Summary Table		
Density		16 Gb
Tech node (nm)		27
Cell Size (nm^2)		4374 (6F^2)
Die Size (mm^2)		168
Selector		Buried WL MOS selector
Read Performance	BW (MB/s)	1000
	Latency (uS)	2
Write Performance	BW (MB/s)	200
	Latency (uS)	10

- Target application: storage class memory
- Endurance target: >10^6 cycles
- Raw BER
  - Endurance <$3X10^{-5}$ at 10^6 cycles
  - Retention: <$2X10^{-4}$ at 10 years, 70^{o}C, 10^4 cycles
  - Read disturb: <$2X10^{-5}$ at 10^6 reads

Acceptable for SCM?

Memristor

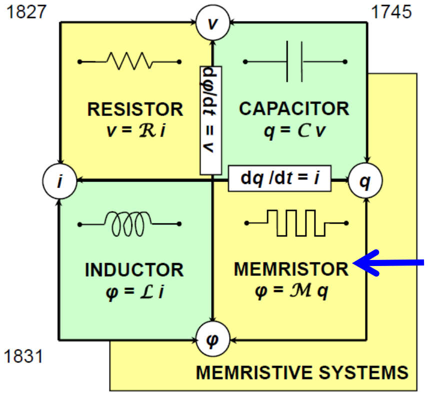
nature Vol 453|1 May 2008|doi:10.1038/nature06932

LETTERS

The missing memristor found

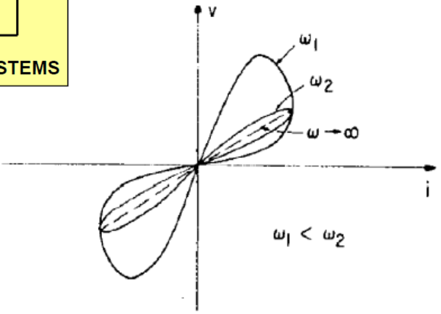
Dmitri B. Strukov[1], Gregory S. Snider[1], Duncan R. Stewart[1] & R. Stanley Williams[1]

Nature v.453, p.80 (2008)

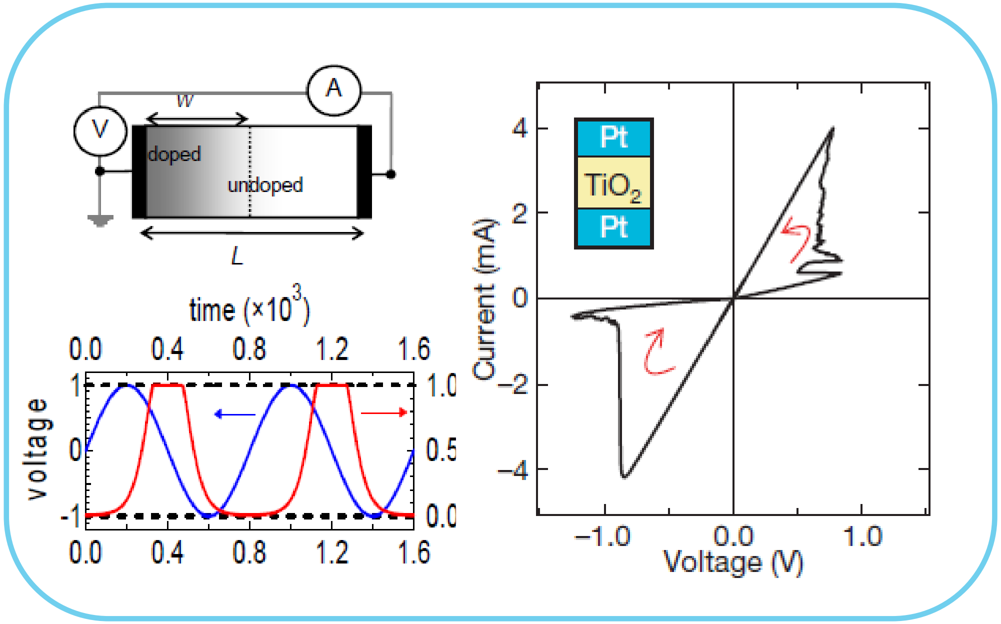


$$v = M(w, v)i$$

$$\frac{dw}{dt} = f(w, i)$$



L.O. Chua, IEEE Trans. Circuit Theory 18, p.507 (1971)



RRAM (and also MRAM and PCM) may show memristic behaviors (analog memory characteristics)

Ferroelectric Memory

FRAM

FeRAM

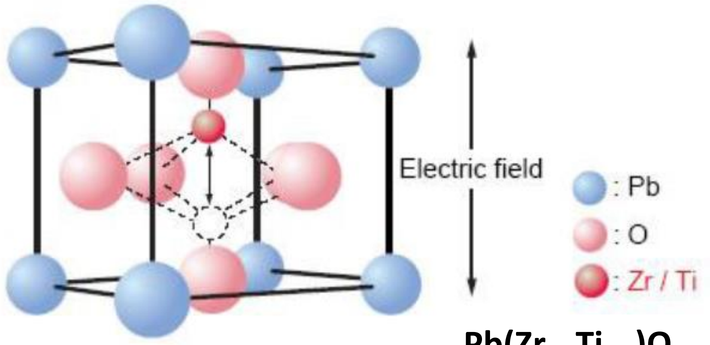
Ferroelectric FET

FeFET

Conventional FRAM

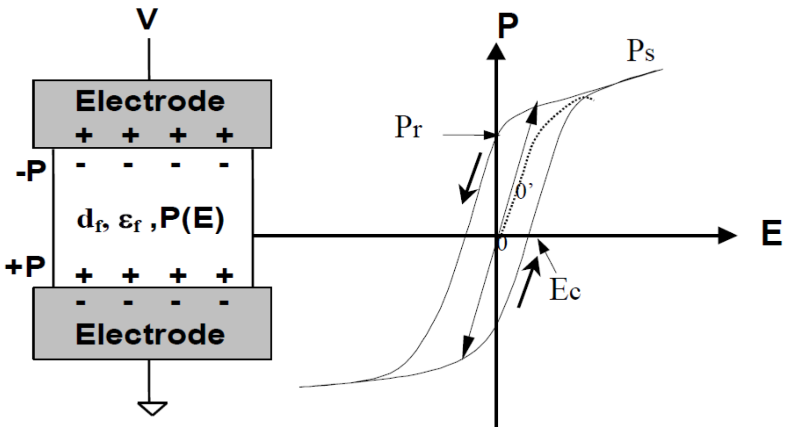
Perovskite crystals (PZT, SBT)

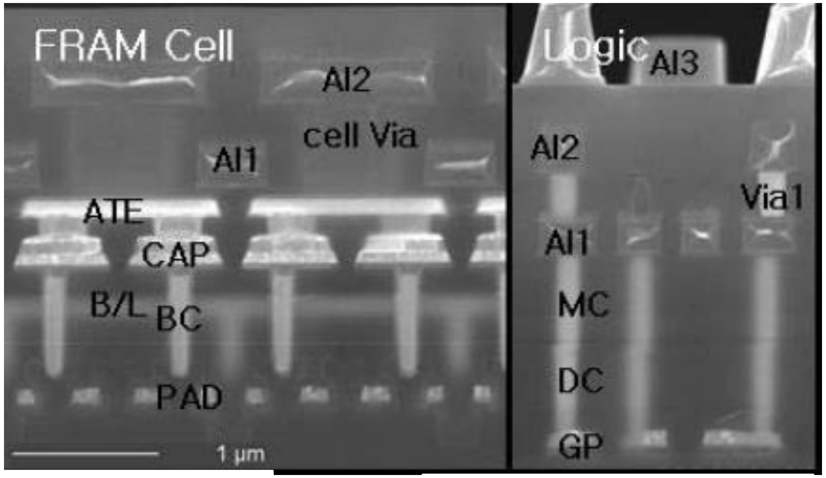
Internal electric dipole reversibly switchable by electric field



$Pb(Zr_x, Ti_{1-x})O_3$

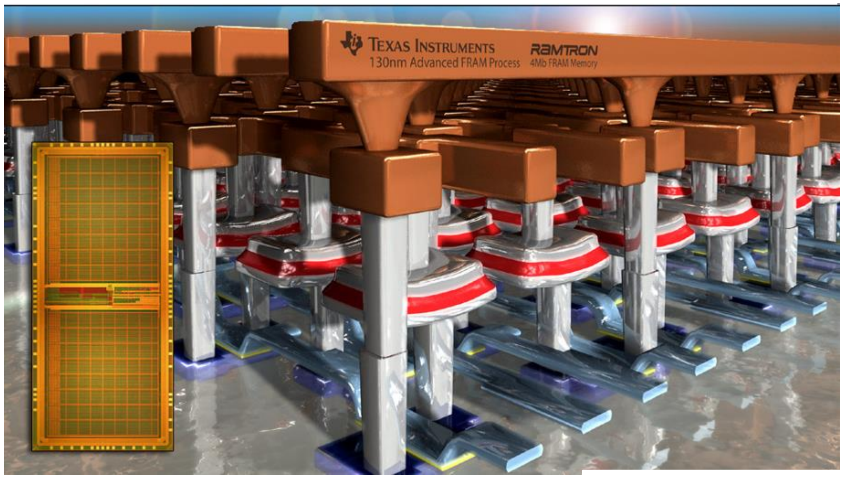
PZT: lead zirconate titanate
SBT: strontium bismuth tantalate





1T-1C (C=FeCAP)

Kim et al. (IEDM, 2005)

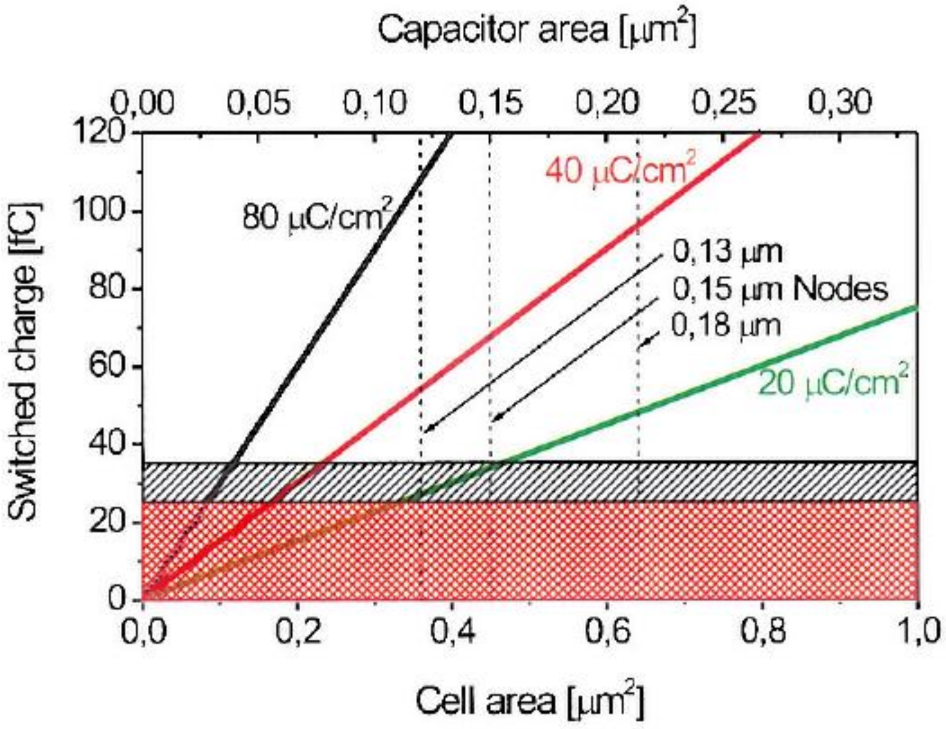


Ramtron (2012)

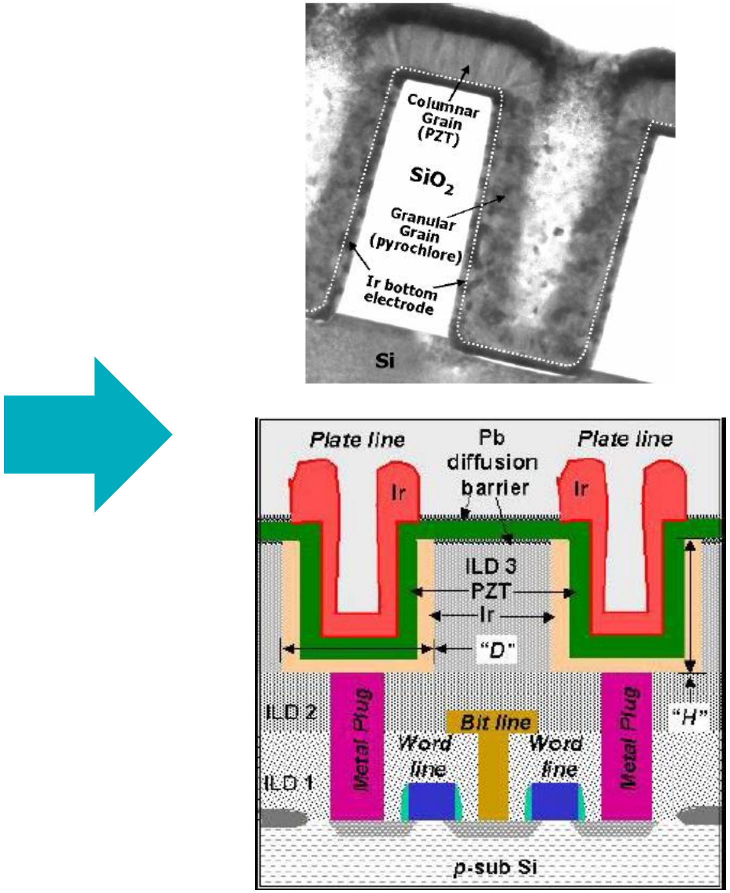
Conventional FRAM

In production, but not scaling beyond 130nm

Fundamental scaling limit requires 3D FeCAP (very challenging)



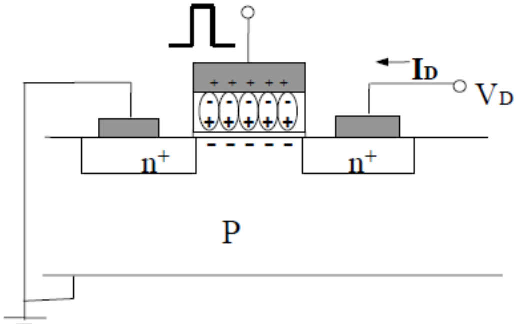
U. Bottger and S.R. Summerfelt, Ferroelectric RAM, from Nanoelectronics and Information Technology (ed. by R. Waser)



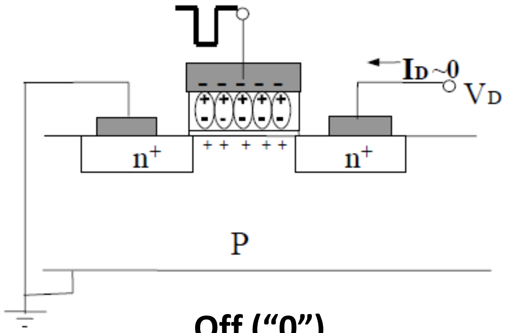
Koo et al. (IEDM, 2006)

FeFET

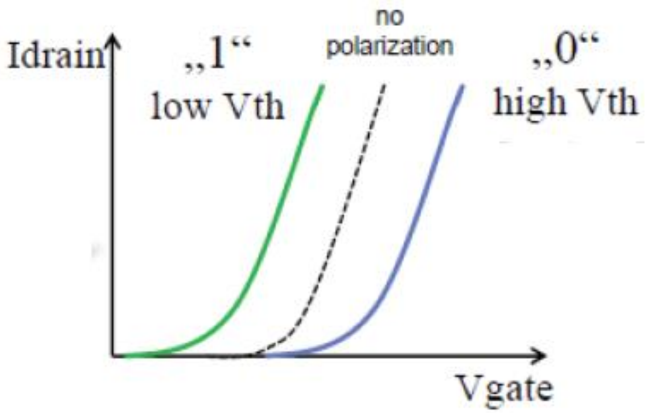
Polarization of ferroelectric layer over the Si channel modulates the threshold voltage (V_{th}) → 1T FRAM

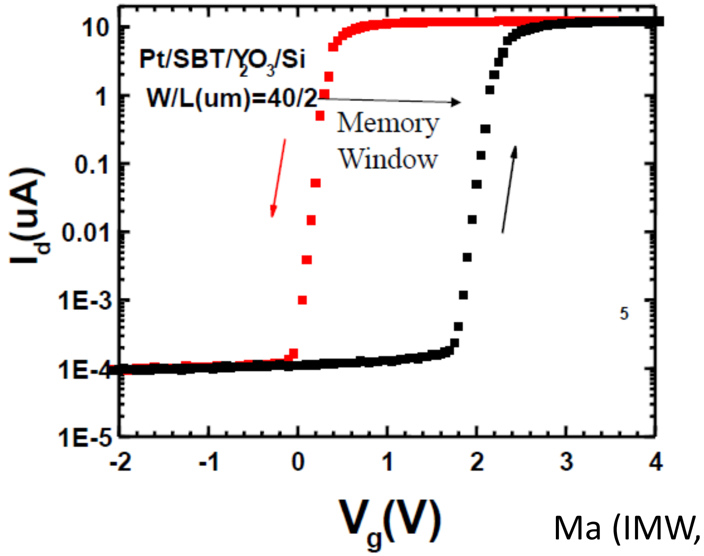


On (“1”)



Off (“0”)





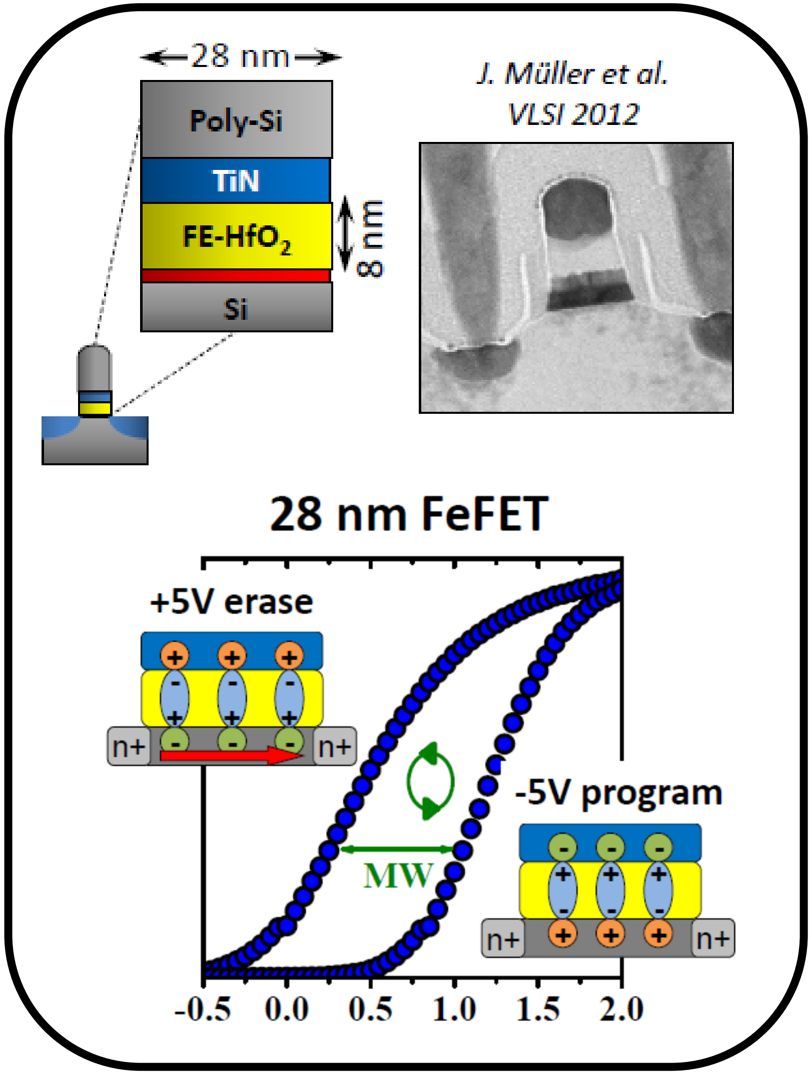
Ma (IMW, 2014)

Challenges

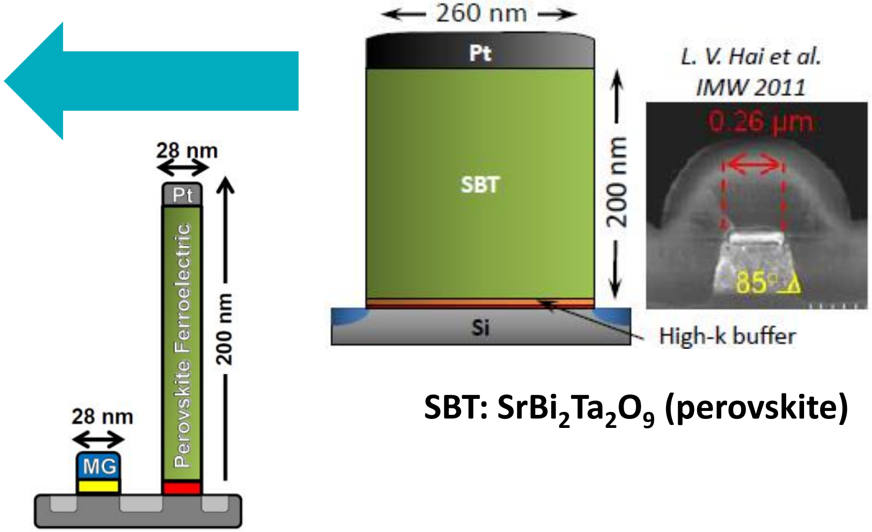
- Required perovskite configuration difficult to integrate
- Data retention (→ FeDRAM?)
    - ○ Depolarization field
    - ○ Leakage

FeFET: Renewed Hope for Scaling

Orthorhombic phase of HfO_2



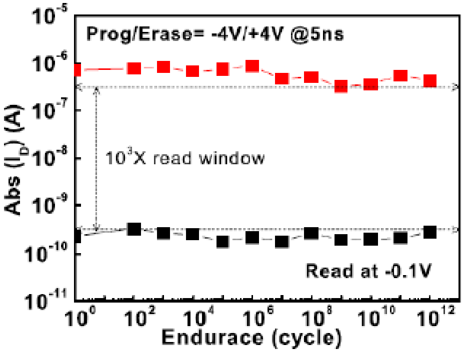
J. Müller et al.
VLSI 2012



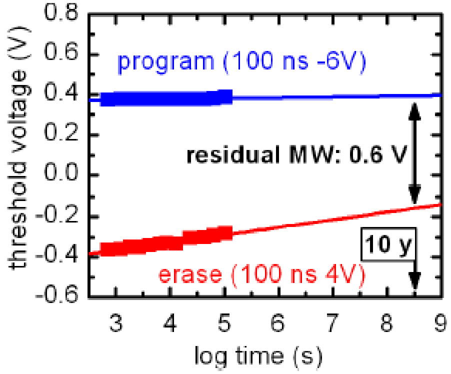
L. V. Hai et al.
IMW 2011

SBT: $SrBi_2Ta_2O_9$ (perovskite)

Cheng & Chin (EDL, 2014)



Muller et al. (VLSI Symp. 2012)



High endurance
at limited retention (<10^3 sec)

Good retention
at limited endurance (<10^5)

Hype?
Promise?
Reality?
Opportunities?

PCM…
MRAM…
RRAM…
FRAM…

Emerging Memory Reality Check

There is no universal memory

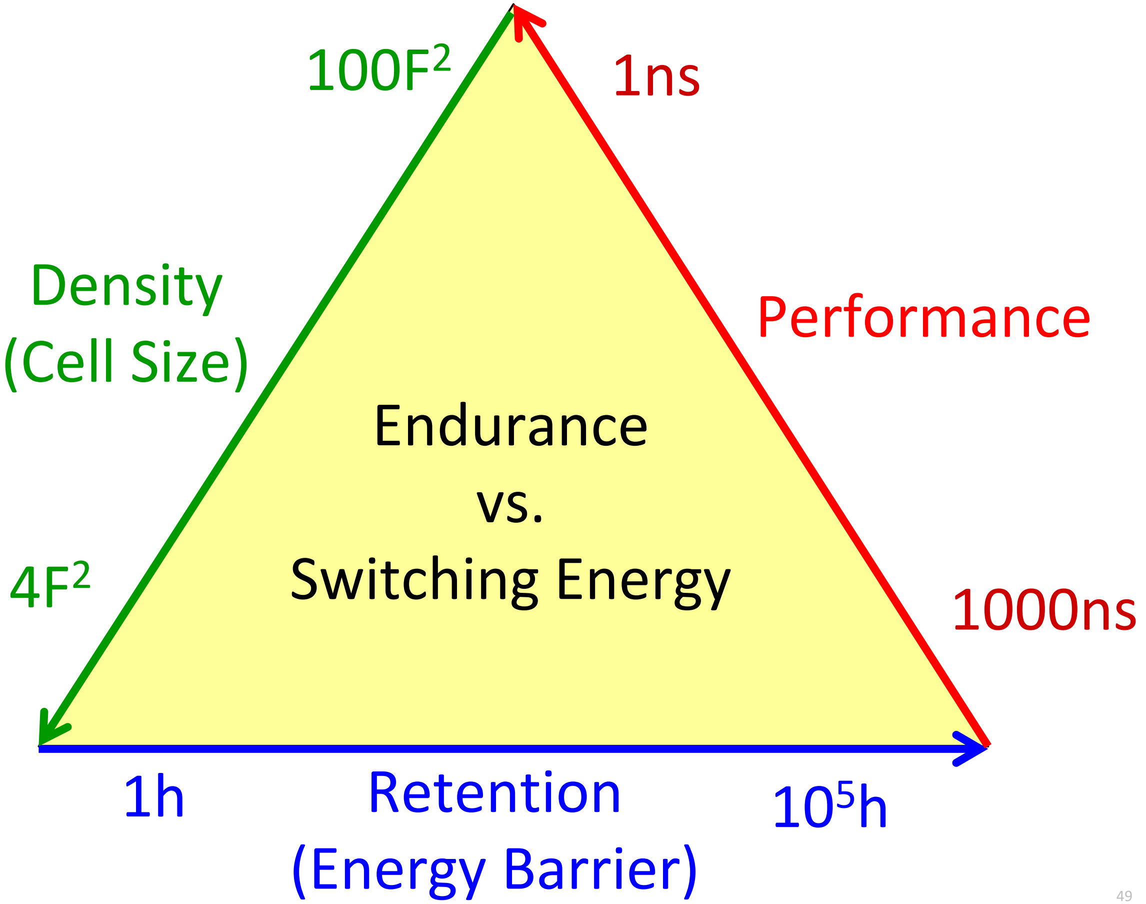
Opportunities in tunability (system differentiation, user experiences)

Ideally

1ns
$4F^2$
$>10^5$h
10^{15} cycles

Universal Memory

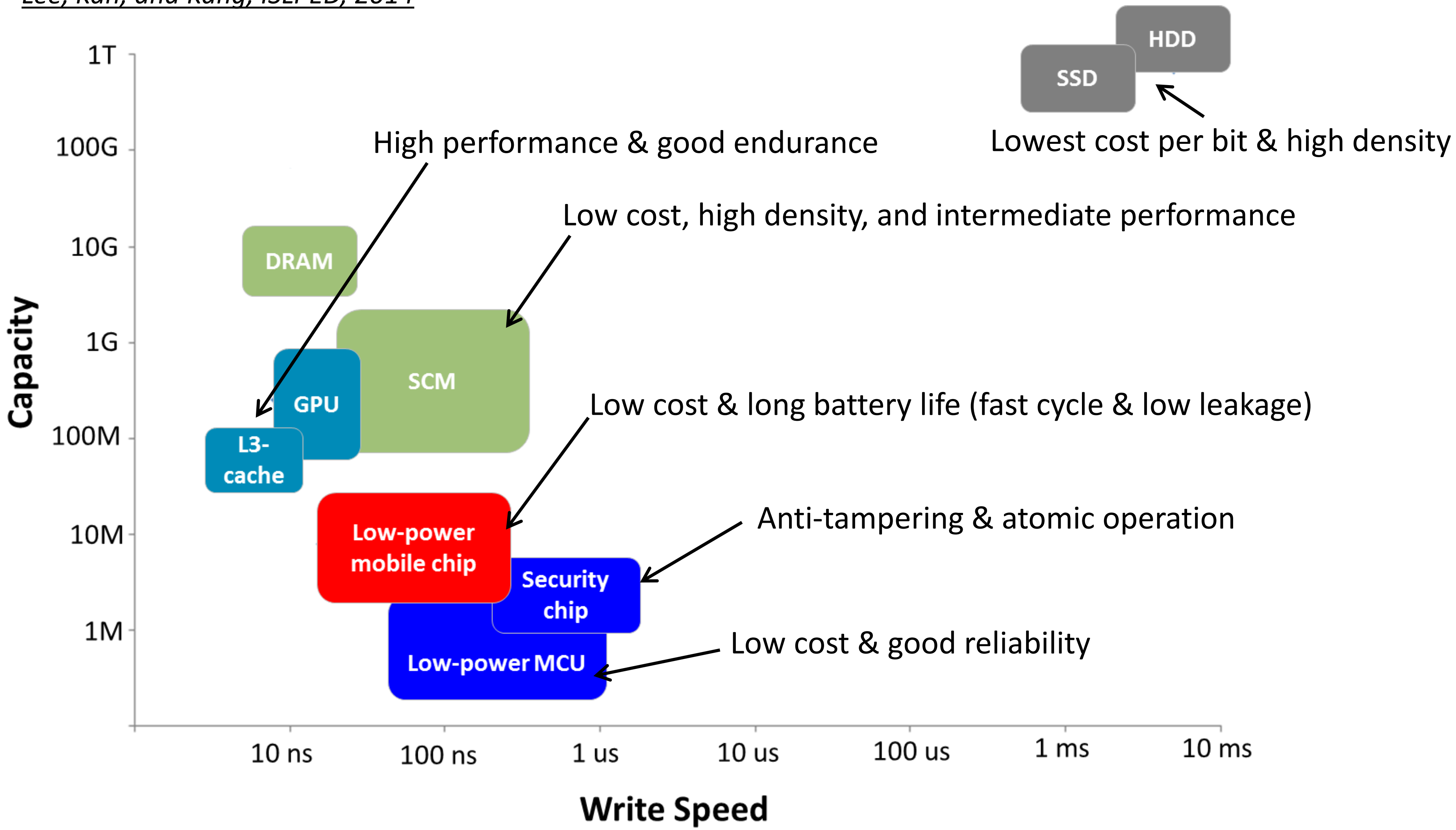
In Reality



Positioning Emerging Memory

Need to understand the application space

Lee, Kan, and Kang, ISLPED, 2014



Lowest cost per bit & high density

High performance & good endurance

Low cost, high density, and intermediate performance

Low cost & long battery life (fast cycle & low leakage)

Anti-tampering & atomic operation

Low cost & good reliability

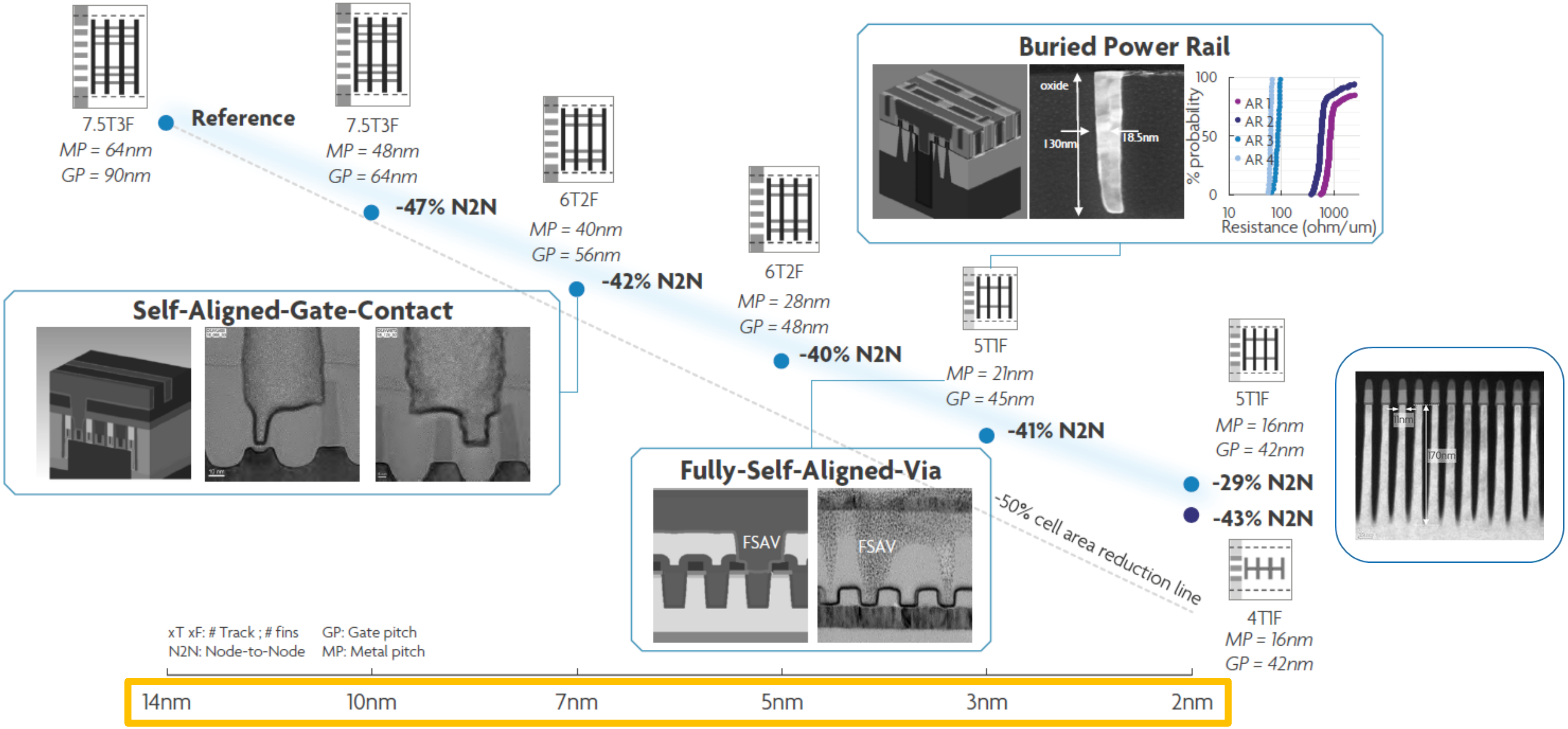
Emerging Memory Pathfinding for Sub-10nm CMOS

MRAM as an example because of its NV-RAM attributes and recent advances at major IC manufacturers

CMOS Logic Scaling

Intrinsic FinFET scaling is limited

Logic scaling is about standard cell architecture innovation



7.5T3F
MP = 64nm
GP = 90nm

Reference

-47% N2N

7.5T3F
MP = 48nm
GP = 64nm

6T2F
MP = 40nm
GP = 56nm

-42% N2N

6T2F
MP = 28nm
GP = 48nm

-40% N2N

5T1F
MP = 21nm
GP = 45nm

-41% N2N

5T1F
MP = 16nm
GP = 42nm

-29% N2N

-43% N2N

4T1F
MP = 16nm
GP = 42nm

-50% cell area reduction line

Buried Power Rail

Self-Aligned-Gate-Contact

Fully-Self-Aligned-Via

xT xF: # Track ; # fins
N2N: Node-to-Node

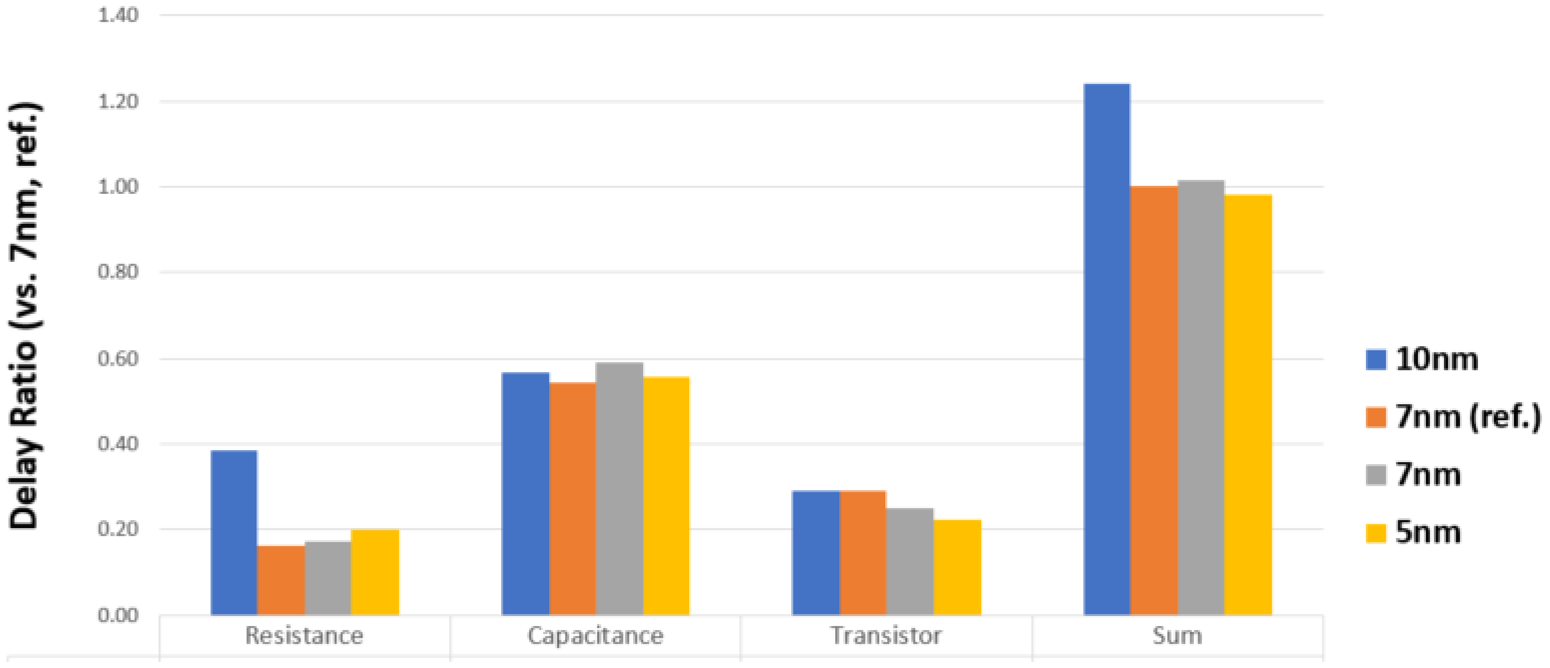
GP: Gate pitch
MP: Metal pitch

14nm 10nm 7nm 5nm 3nm 2nm

Source: A. Steegen, 2018 ITF Belgium

Parasitic R & C Impact

MOL and BEOL parasitic R & C causing more delays than intrinsic transistor delay



Negatively impacting essentially all types of resistance-based memory designs (MRAM, RRAM, PCM)

SRAM Scaling

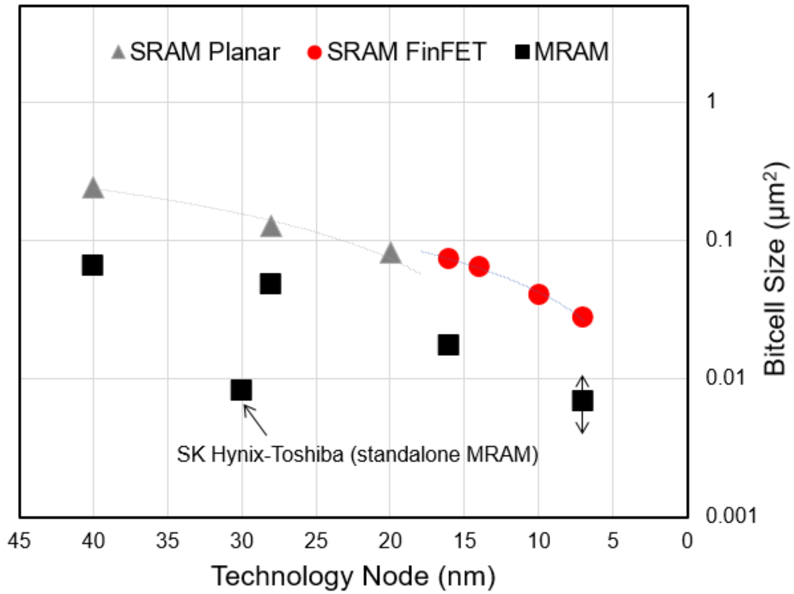
Relatively more expensive at advanced nodes

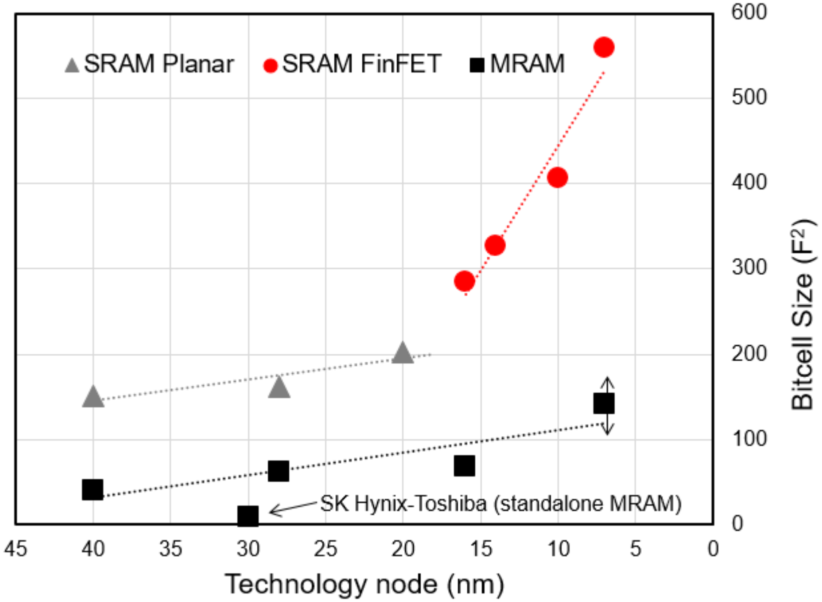
FinFET SRAM near the end of scaling

High-density 6T SRAM: ~550F^2 at 7nm

Expect ~1000F^2 at 5nm

F: node number



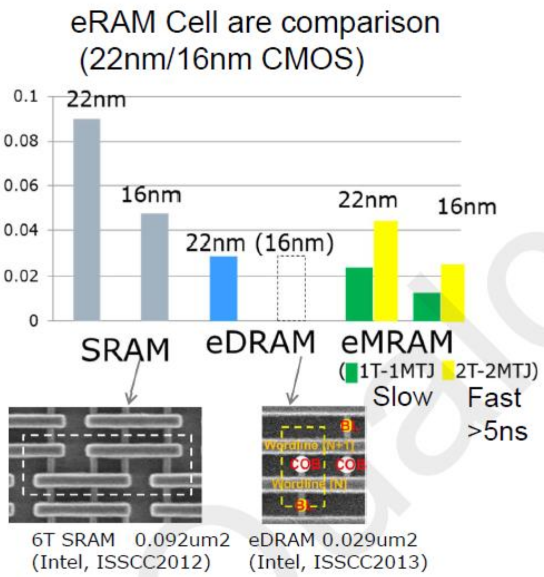


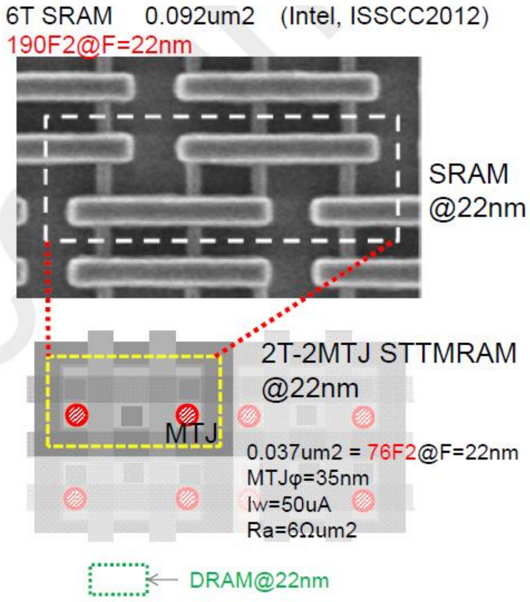
Kang & Park, IEDM 2017

MRAM Pathfinding as an SRAM Alternative

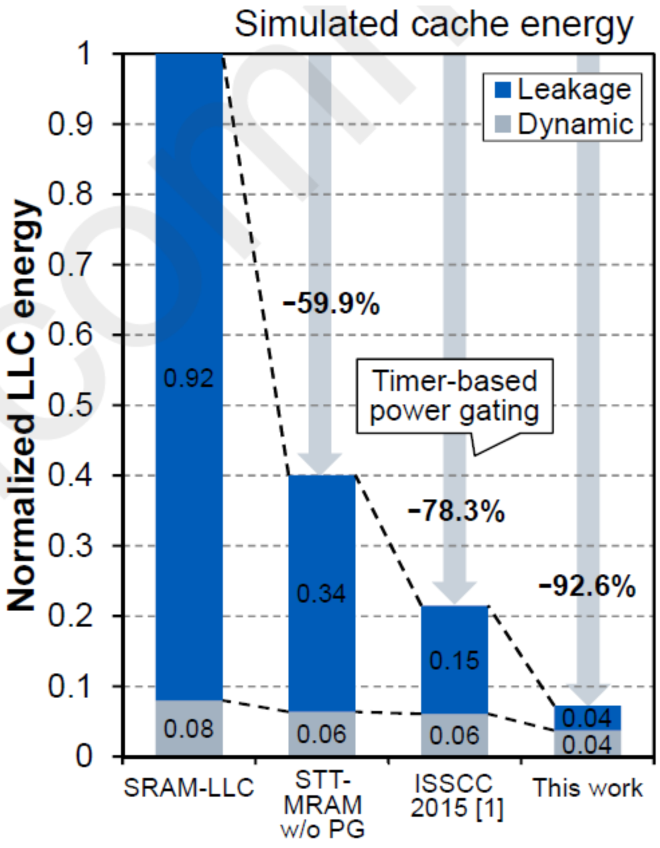
Reduce last-level-cache area and energy consumption

A 22nm case study by Toshiba





Expected area reduction of SRAM with MRAM
x 50% or less with 2T-2MTJ (Fast), x 25% or less with 1T-1MTJ (Slow)



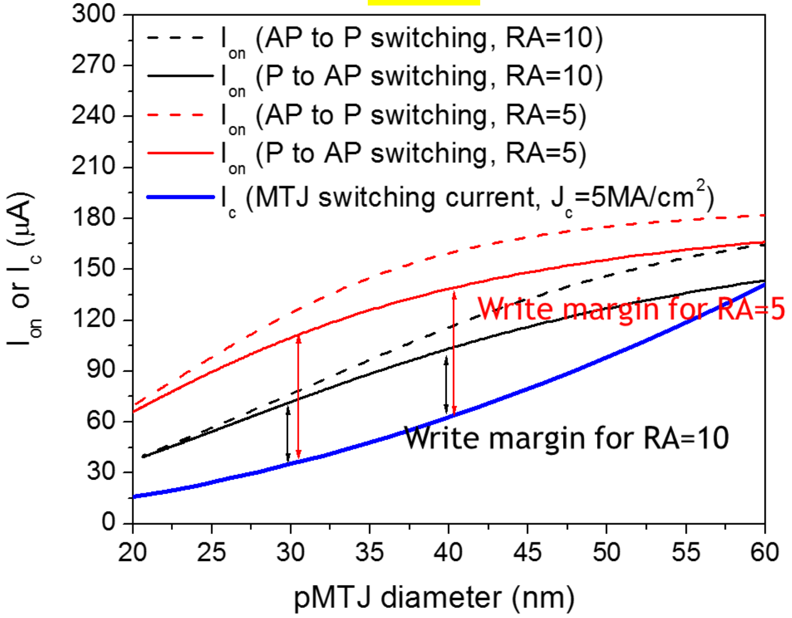
Toshiba , ISSCC 2016

Cell Design Challenge: Supply Current

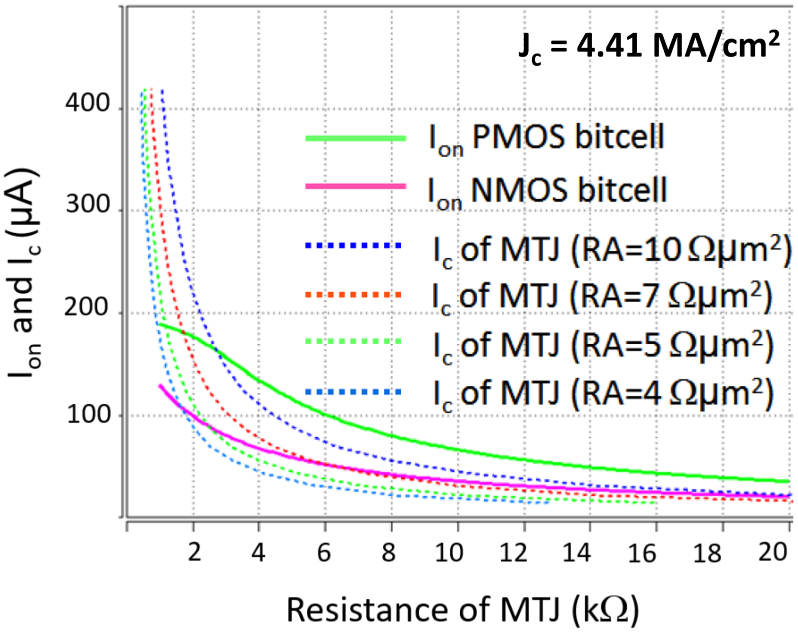
CMOS supply current much smaller at advanced nodes

→ Requiring low switching current and low MTJ resistance

28nm



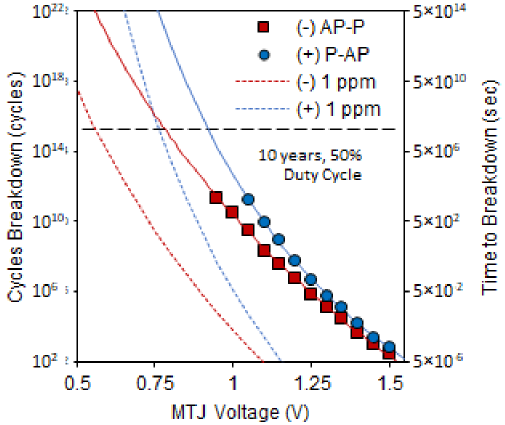
7nm



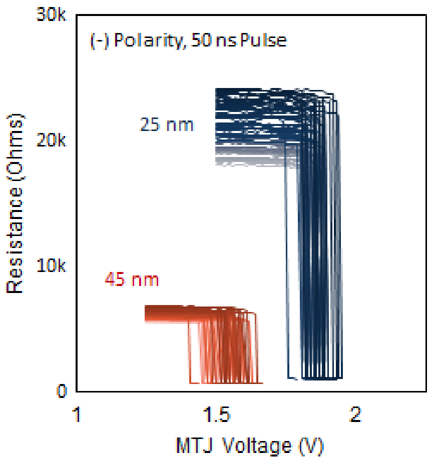
Park et al., VLSI Symp. 2018

Reliability Challenge: Endurance

Intrinsic endurance practically unlimited
However, endurance sensitive to switching voltage & MgO TDDB



Need TDDB test



Smaller MTJ → Higher V_{bd}

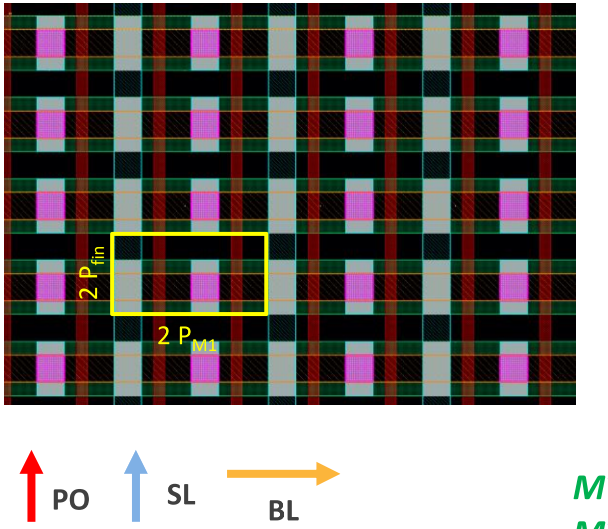
Example Use Case	Memory Size (Mbyte)	Assumptions	10 Year Endurance Requirement
L2 Cache	1	10^8 access/sec, 40 % write traffic	7.7×10^{11}
L3 Cache	6	10^7 access/sec, 40 % write traffic	1.3×10^{10}
Unified eNVM	32	1.6 GB/sec, 64-bit IO, constant write traffic	1.6×10^{10}
IOT Unified	1	400 MB/sec, 64-bit IO, 1 % duty cycle	1.3×10^{9}
Repeated Address Attack	N/A	50 ns attack period, 100 % duty cycle	6.3×10^{15}

Common memory applications < 10^{12}

Kan et al., IEDM 2016 & TED 2017

Cell Architecture Pathfinding for 7nm

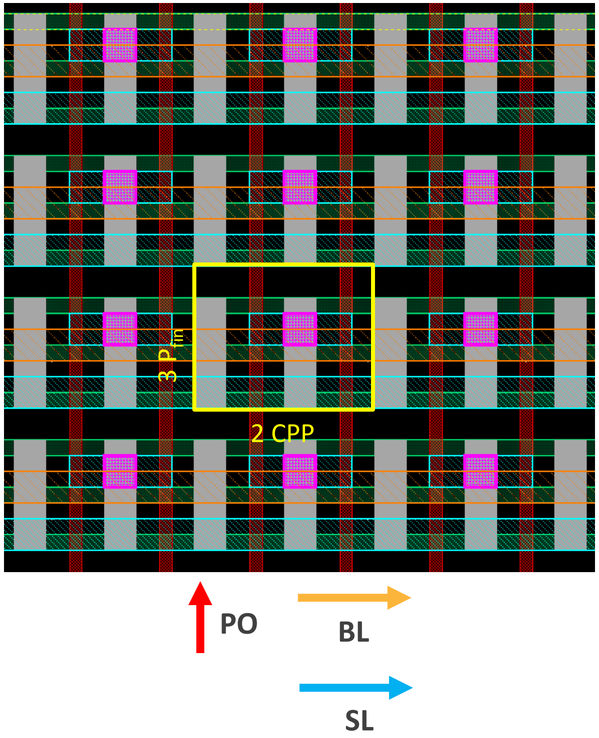
1T-1MTJ



Bitcell (X,Y): (2P_{M1}, 2P_{fin})
Area (2-fin cell): ~140 F^2
MRAM:SRAM → ~0.25X (for area)

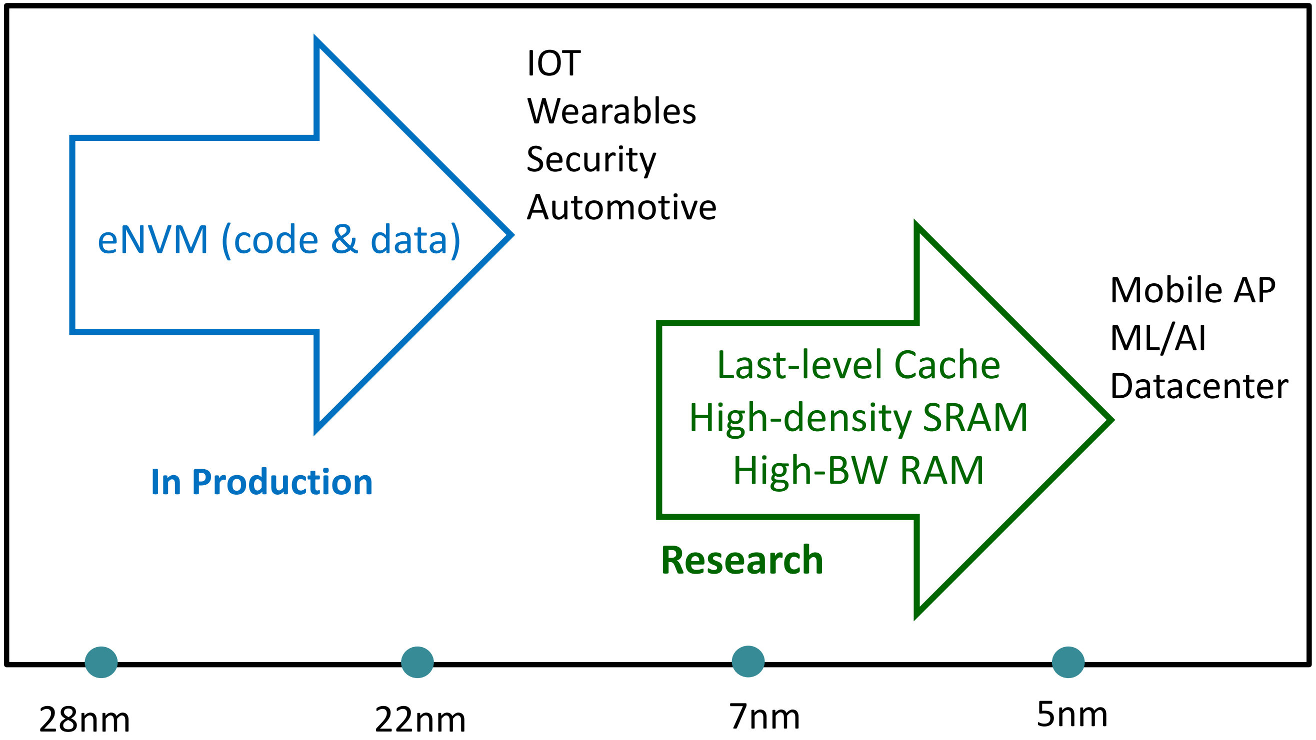
MTJ pitch → 85-90 nm
MTJ CD → 30-35 nm

2T-1MTJ



Bitcell (X,Y): (2CPP, 3P_{fin})
Area (6-fin cell): ~210 F^2
MRAM:SRAM → ~0.35X (for performance)

Prospect

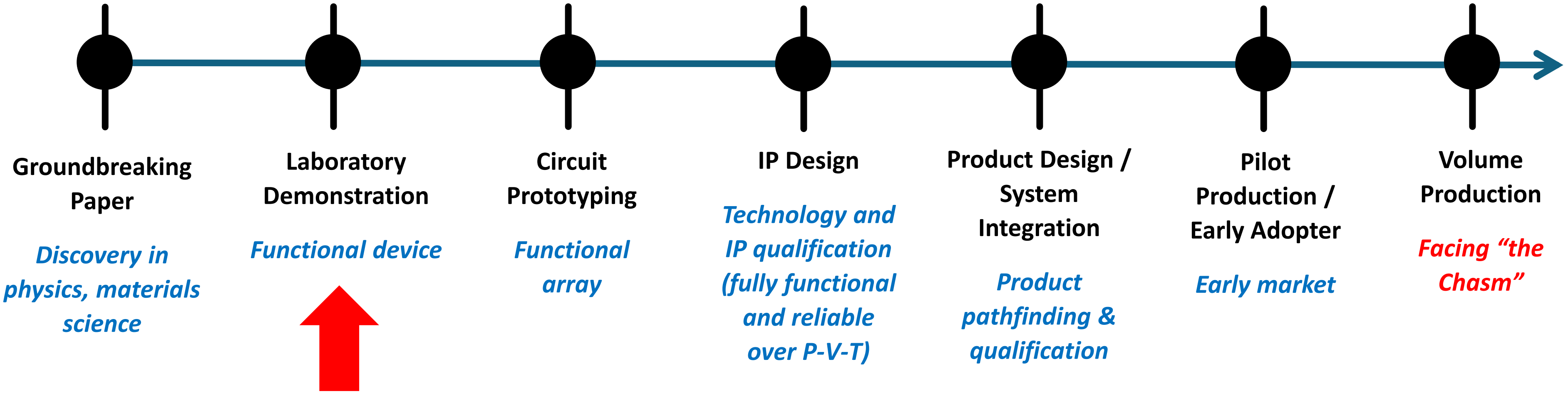


Kang, 2014 VLSI Symp. & 2019 CIES Tech Forum

From Research to Commercialization

Semiconductor devices typically require >~10 years of R&D (e.g. FinFET)

Can you stay in the game?



Groundbreaking Paper

Discovery in physics, materials science

Laboratory Demonstration

Functional device

Circuit Prototyping

Functional array

IP Design

Technology and IP qualification (fully functional and reliable over P-V-T)

Product Design / System Integration

Product pathfinding & qualification

Pilot Production / Early Adopter

Early market

Volume Production

Facing “the Chasm”

Any fundamental showstopper?

Thank You.

For questions and feedbacks,
contact kang@qti.qualcomm.com