Hybrid PLL Architectures and Implementations

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September 26, 2019

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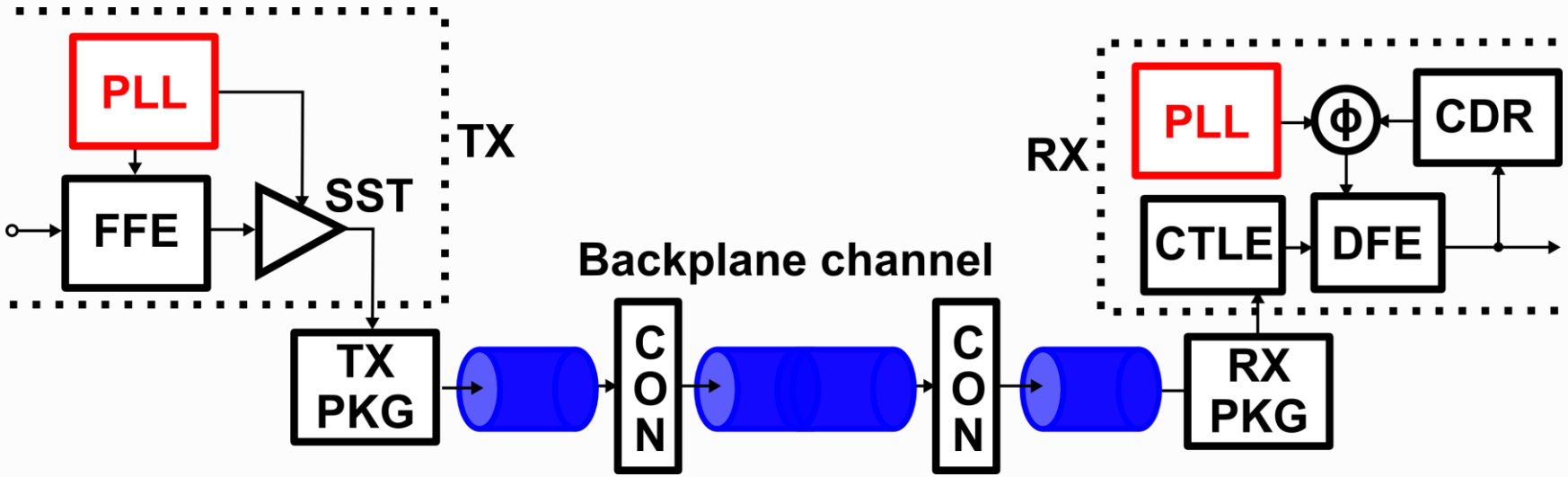
Outline

- Introduction and motivation: hybrid architectures
- Initial implementation: proof-of-concept
- Flexible synthesizer: frac-N w/ noise cancellation
- Flexible synthesizer: coarse band elimination
- Flexible synthesizer: flicker noise suppression exploration
- Summary/conclusion

Motivation: Application challenges

Context/relevant applications:

- High speed serial links
- Clock synthesis for mm-wave wireless



Opportunities for hybrid analog/digital PLLs:

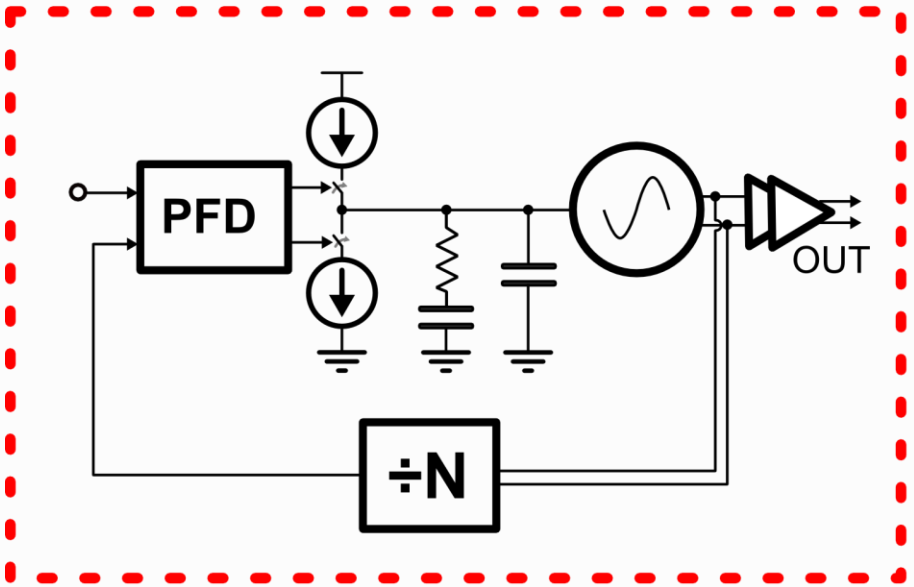
- Reduce dependence on special technology elements
- Reduce PLL area
- Introduce new functionality and improve testability

Challenges:

- *must continue to meet stringent phase noise, tuning range, and robustness requirements set by application*

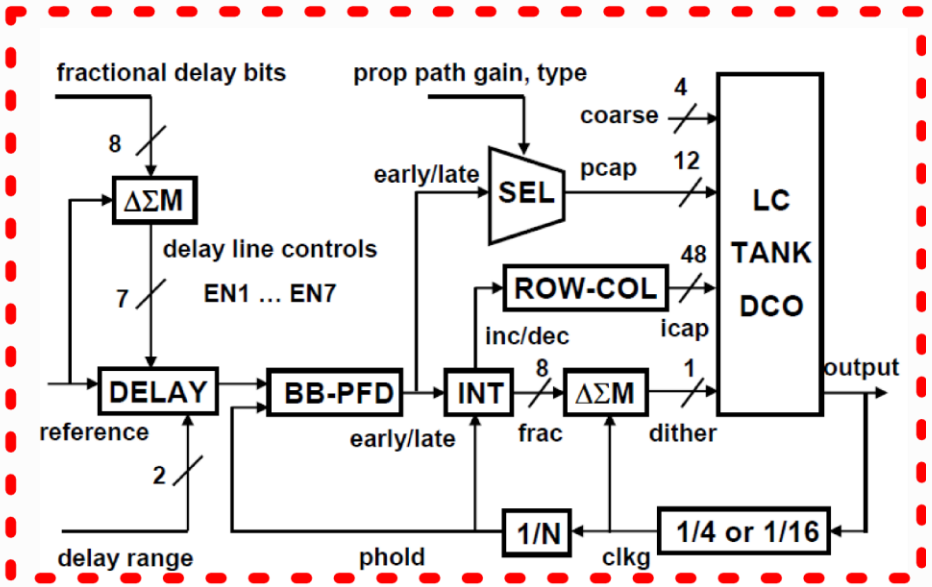
Architecture tradeoff: Analog versus digital

Conventional analog PLL



- Requires large, low leakage capacitor (unfriendly to digital process)
- Requires wide dynamic range charge pumps

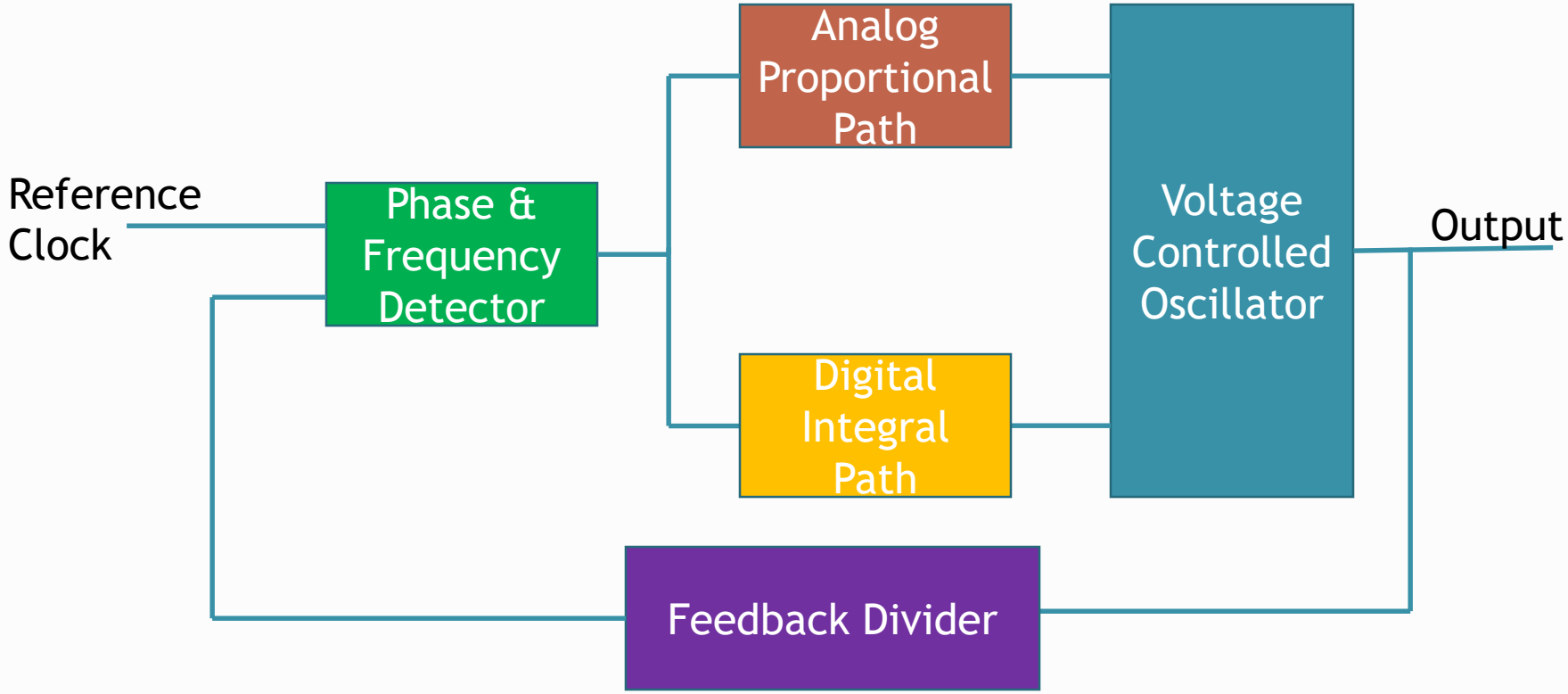
Prior art digital PLL [1]



A. Rylyakov et al., ISSCC 2009.

- Nonlinearity of digital components leads to spurs in the output spectrum
- PLL can slew in response to small phase errors
- Transfer function of all digital PLL is noise-dependent

Hybrid PLL: Core Concept

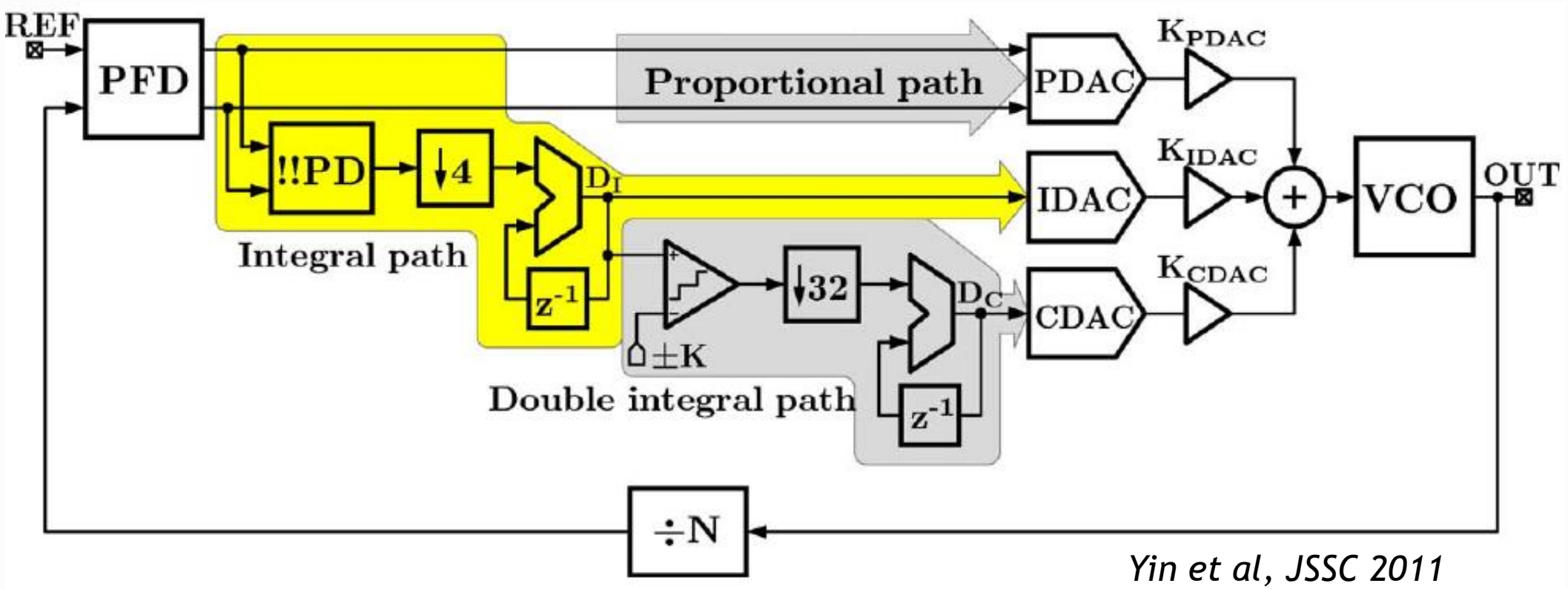


- Proportional path: pulse width modulated signal as in analog PLL
- Integral path: create control word using DSP as in digital PLL

Opportunity to achieve best-of-both worlds properties

- **Linear proportional path with simplified charge pump versus analog PLL**
- **Compact digital integral path with extensive digital domain sensing and actuation enablement**

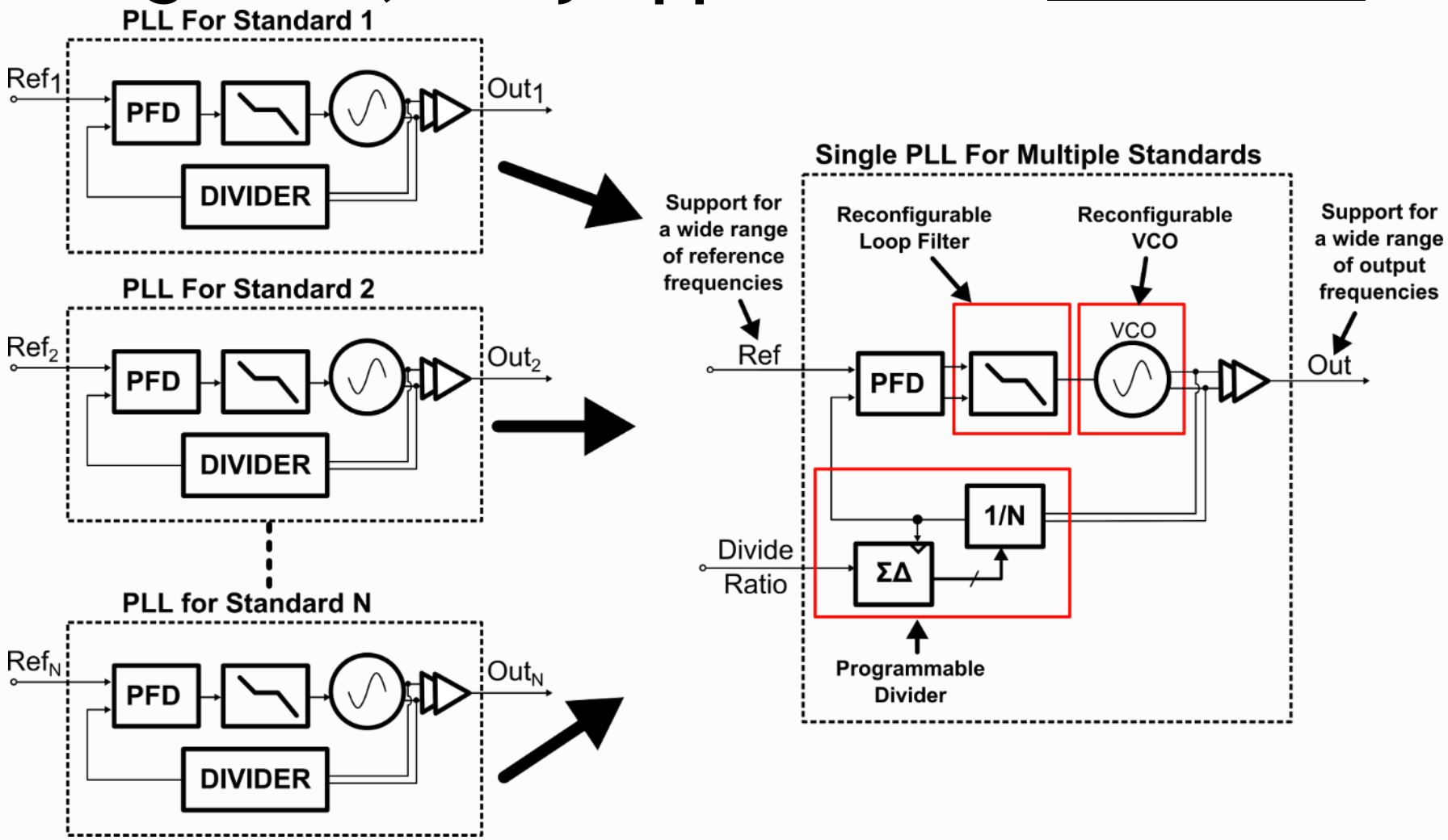
Example Hybrid PLL Architecture



Yin et al, JSSC 2011

- Proportional path drives a scaled pulsewidth modulated signal into VCO control node
- Integral path drives a digital control word to the IDAC/CDAC path
- Oscillator is current-controlled ring

Hybrid PLL Opportunity:
Single PLL, Many Applications- *2 - 26GHz*



Vision: Replace multiple custom synthesizers with a single, flexible, dynamically reconfigurable PLL for wireless and wireline high performance applications

Preview: Flexible Synthesizer Features Achieved Using Hybrid PLL Approach

Characteristic	Objectives	Implementation Approach
Tuning range 2-26GHz	Continuous tuning range to maximum frequency	Wide-range dual linearized transconductance VCO complex
Loop transfer function control	High programmability over wide range through digital control	Leverage highly digital architecture of dual-path HPLL
Supported reference rate	Flexible without sacrificing performance	Fractional-N synthesis
Fractional-N quantization noise	Active noise cancellation scheme that does not limit bandwidth	Proportional & integral path highly digital cancellation architecture
Area	Less than 1 mm^2 total	Single PLL with wide-range dual VCO complex
Fast frequency hopping	Fast settling time based on digital memory	Leverage digital memory/parameter replay
Spurious content	Minimize to enable broader use model	Reduced by utilization of digital/predictive techniques
Extended range in main loop	Eliminate need for coarse bands in supporting wide tuning range	Enhance and extend digital integral path approach to include full VCO range

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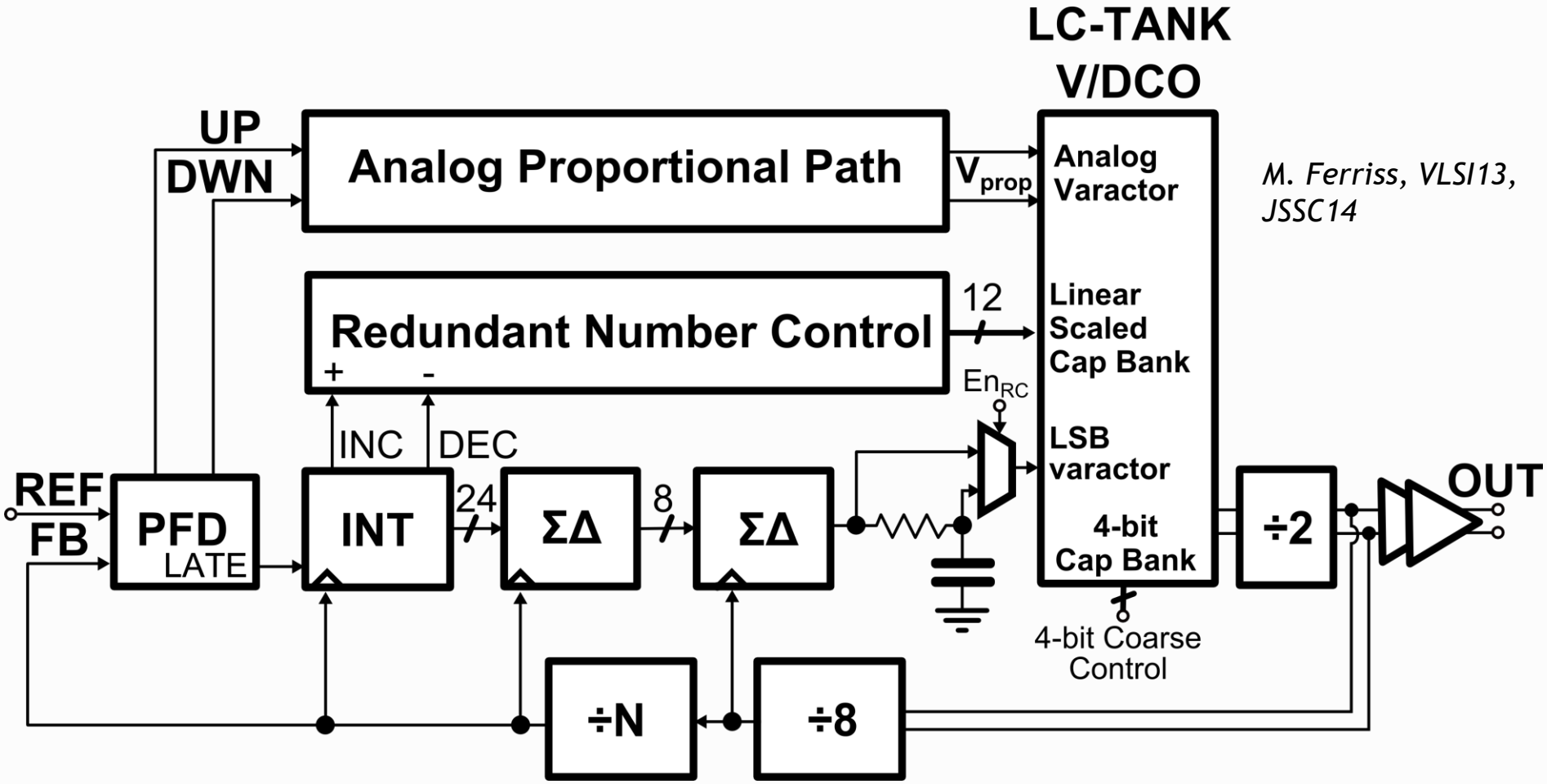
High Performance Hybrid PLL

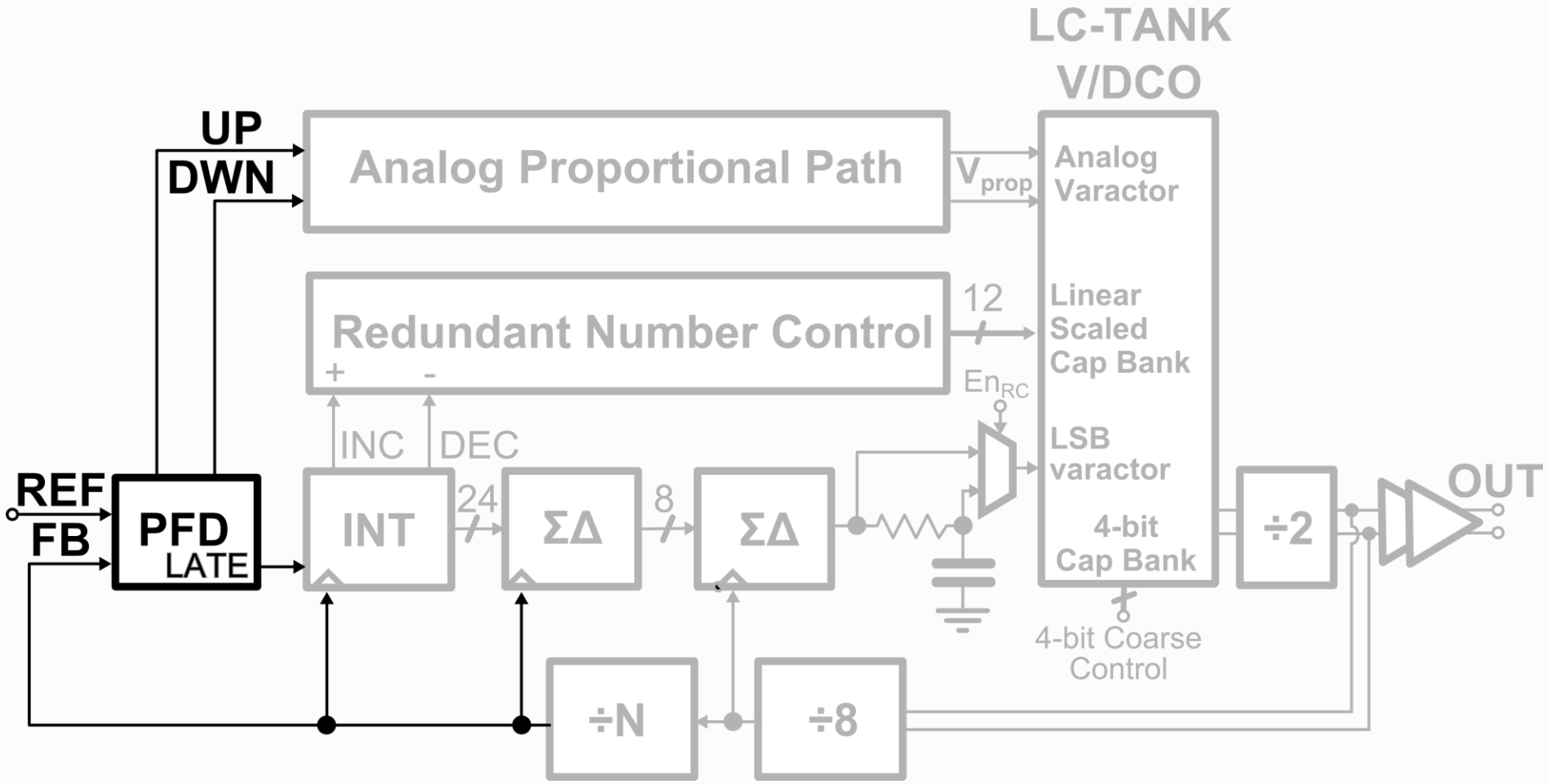
- Objective: demonstrate hybrid PLL in high performance (LC-VCO-based) context while maintaining tuning range of analog implementation
- Approach
  - Proportional path varactor driven by simplified PWM path
  - Integral path controls fixed and $\Sigma\Delta$ modulated switched capacitance in D/VCO (implicit DAC)
  - Coarse band architecture to enable wide tuning range without sacrificing phase noise performance
- Key challenges
  - Integral path design
  - D/VCO integration

Hybrid PLL with Redundant Numbering Integral Path: Architecture Overview



- PLL utilizes a mixture of analog (proportional path) and digital (integral path) techniques
- Analog component simplified → easy to implement in low voltage CMOS

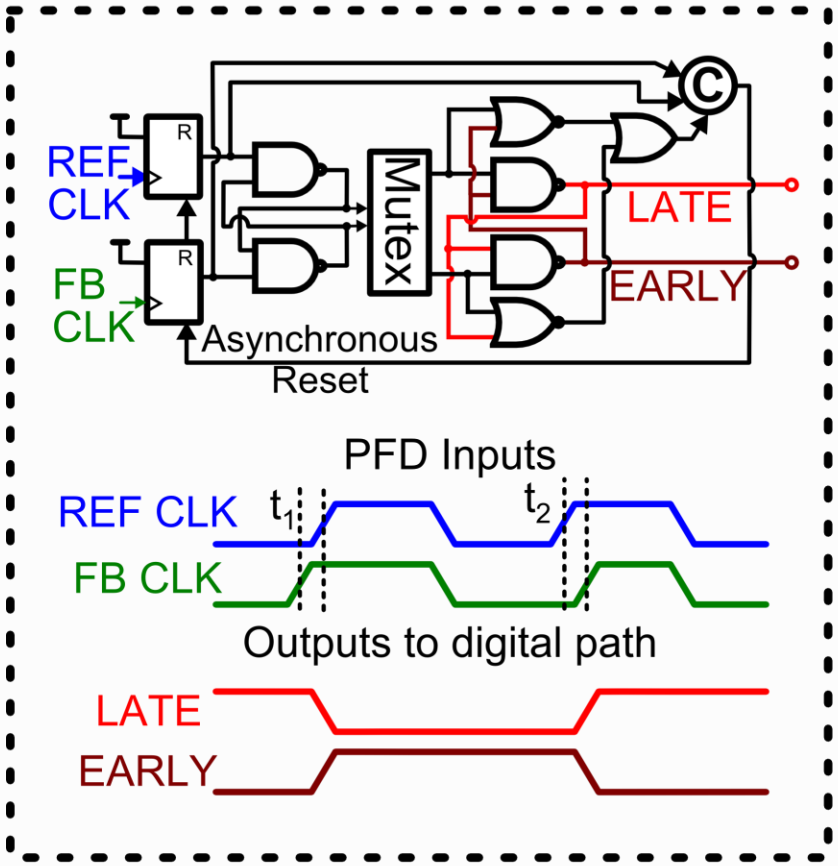
HPLL Phase and frequency detector (PFD)



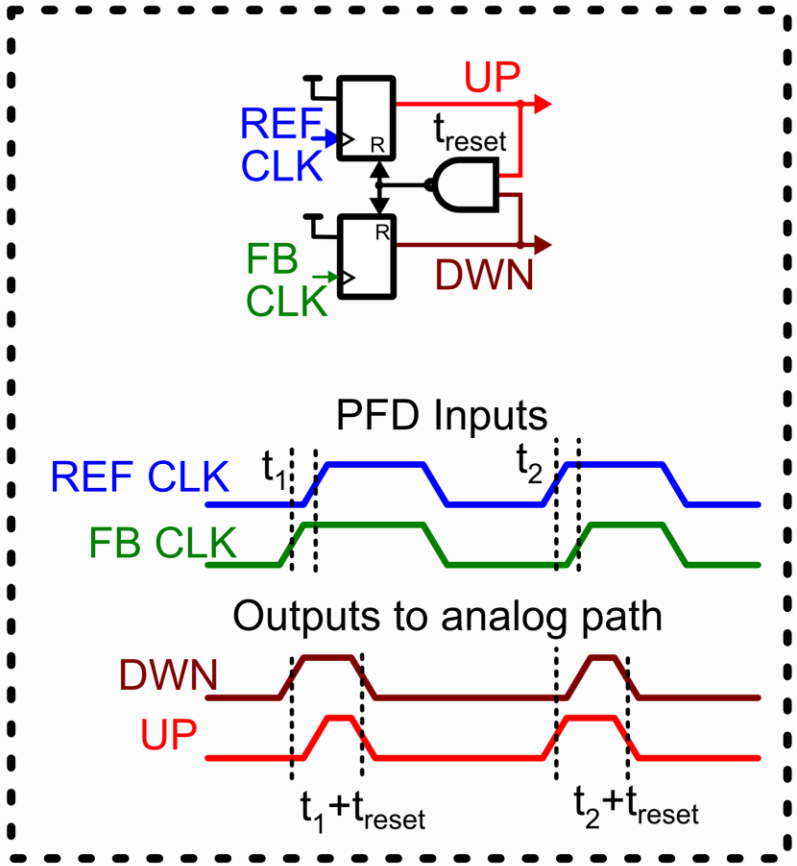
- Requires phase detector with analog (linear) and digital (bang-bang) outputs
- **Do we need two phase detectors?**

Example phase detectors for digital and analog PLLs

Prior art BB-PFD [2] for digital PLL



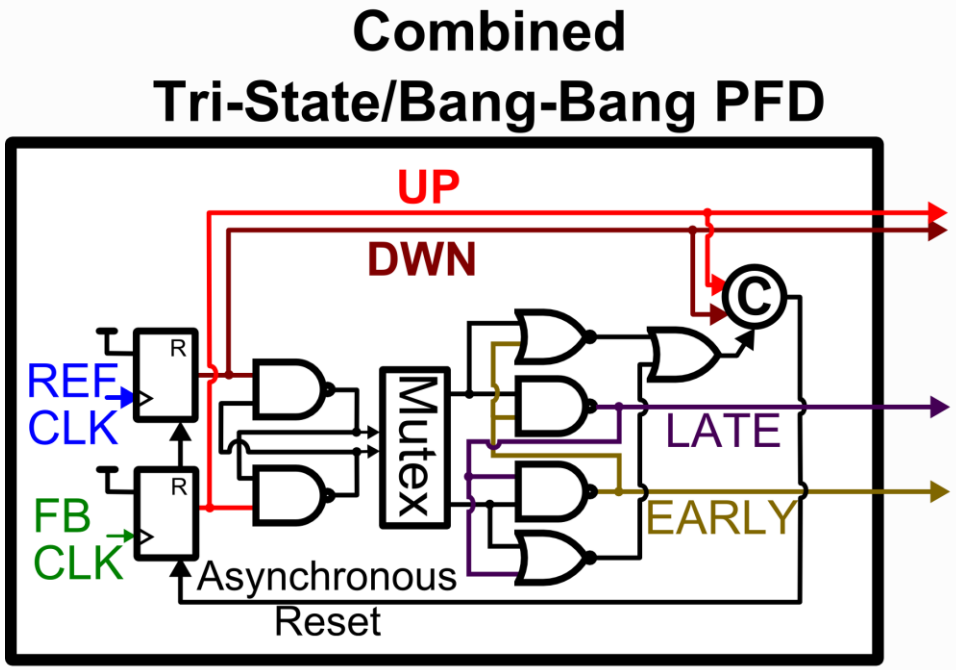
Conventional tri-state PFD for charge pump based PLL

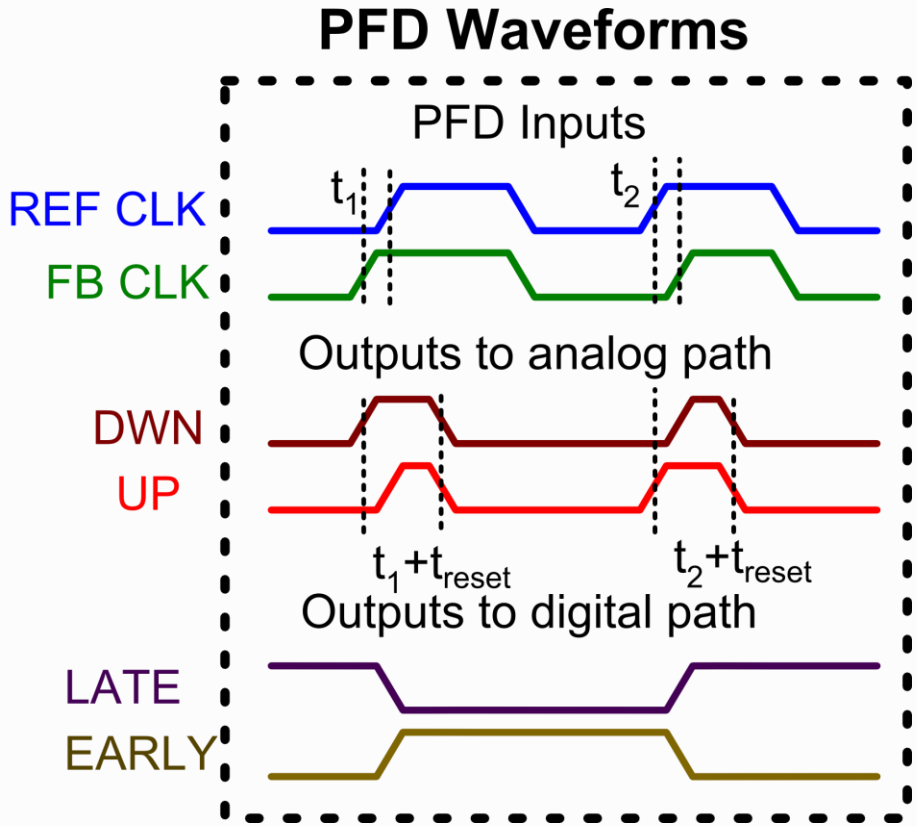


Ⓒ -Muller C element. If all inputs have the same logic value, then the output matches inputs.

Mutex -Mutex for metastability rejection.

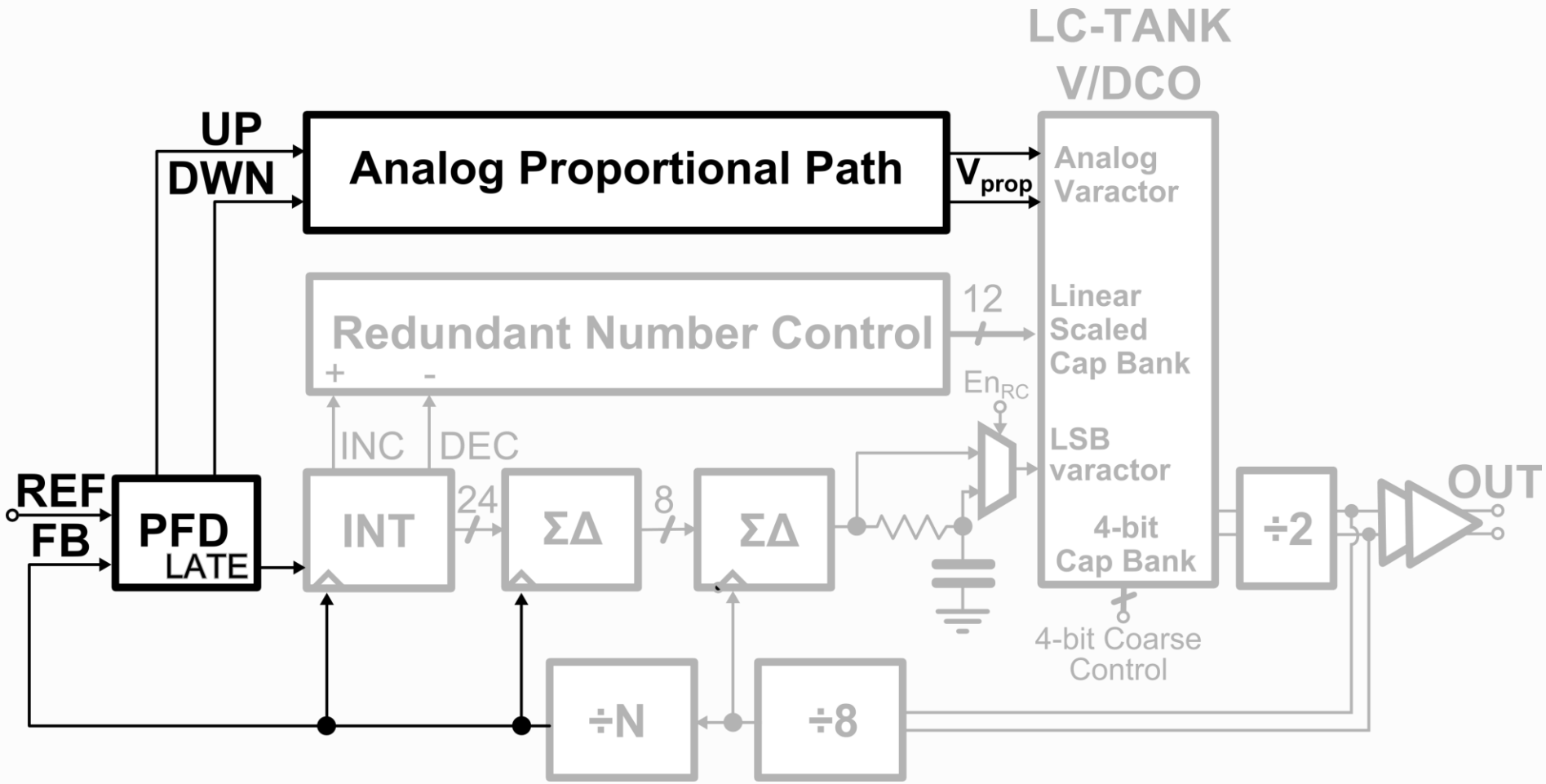
Hybrid PLL Approach: Single PFD with two sets of outputs



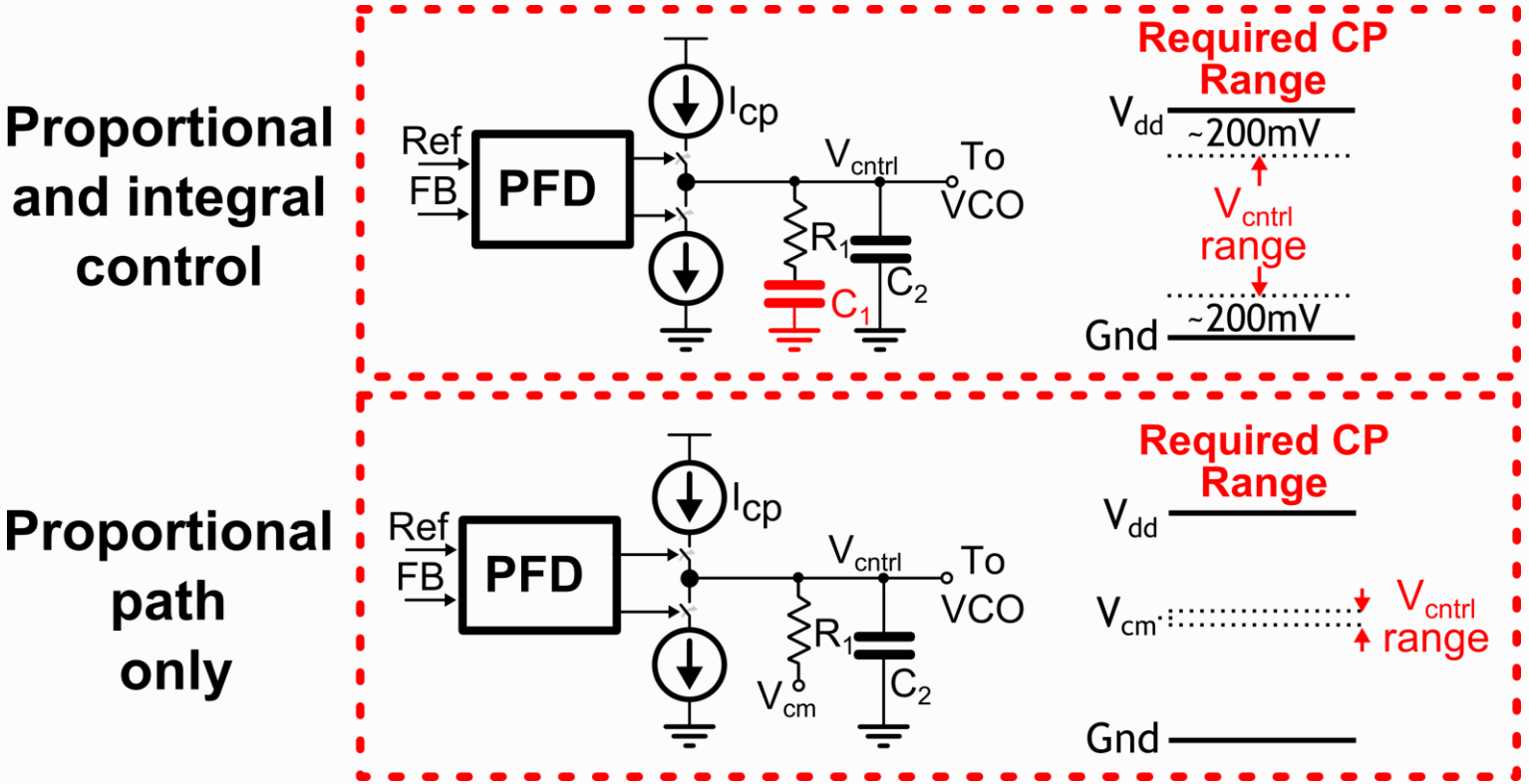


- Offset of input latches is common to both paths
- Digital discriminator takes time to resolve – similar to delay path in tri-state PFD

Analog proportional path

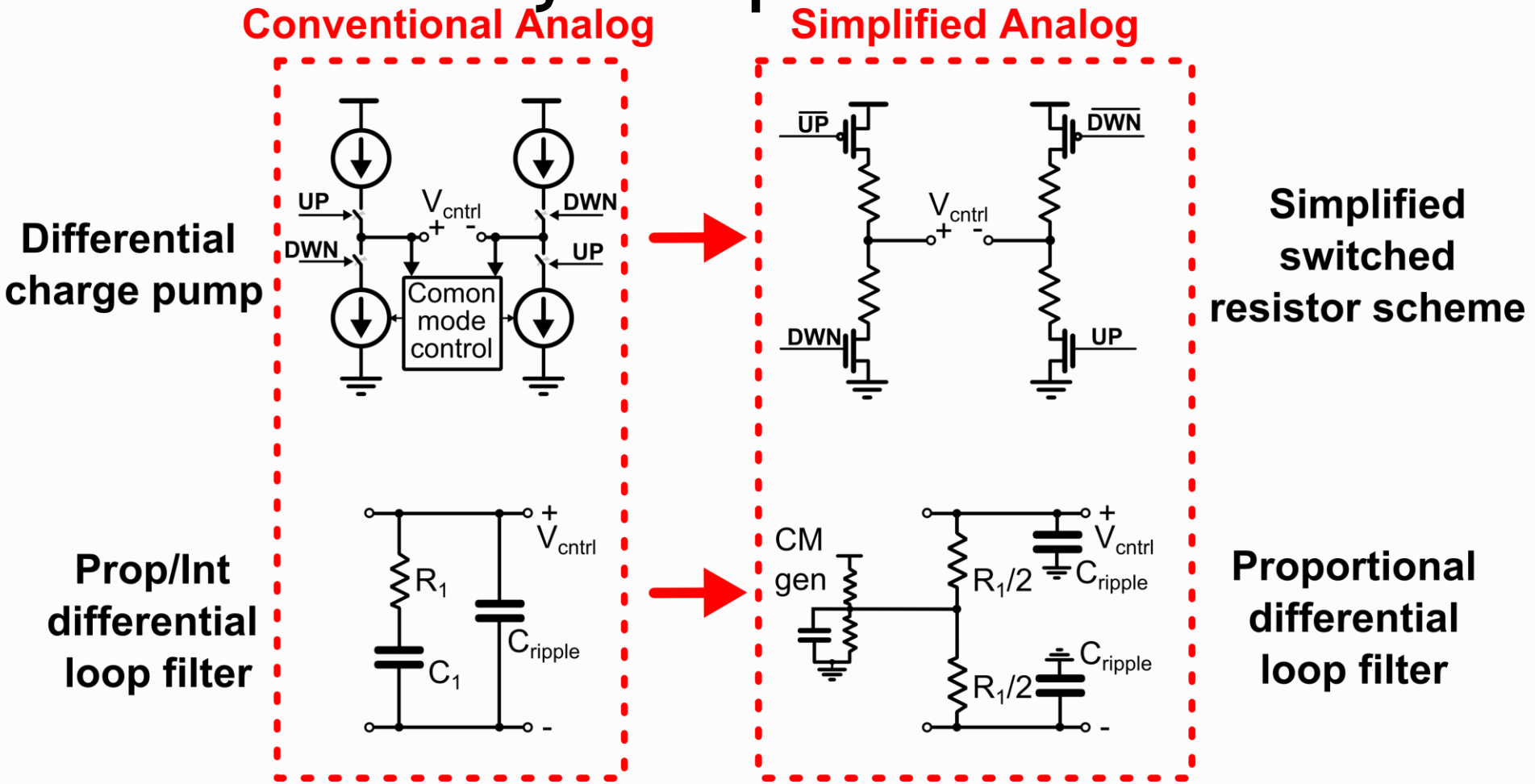


Dual path architecture enables proportional path simplification



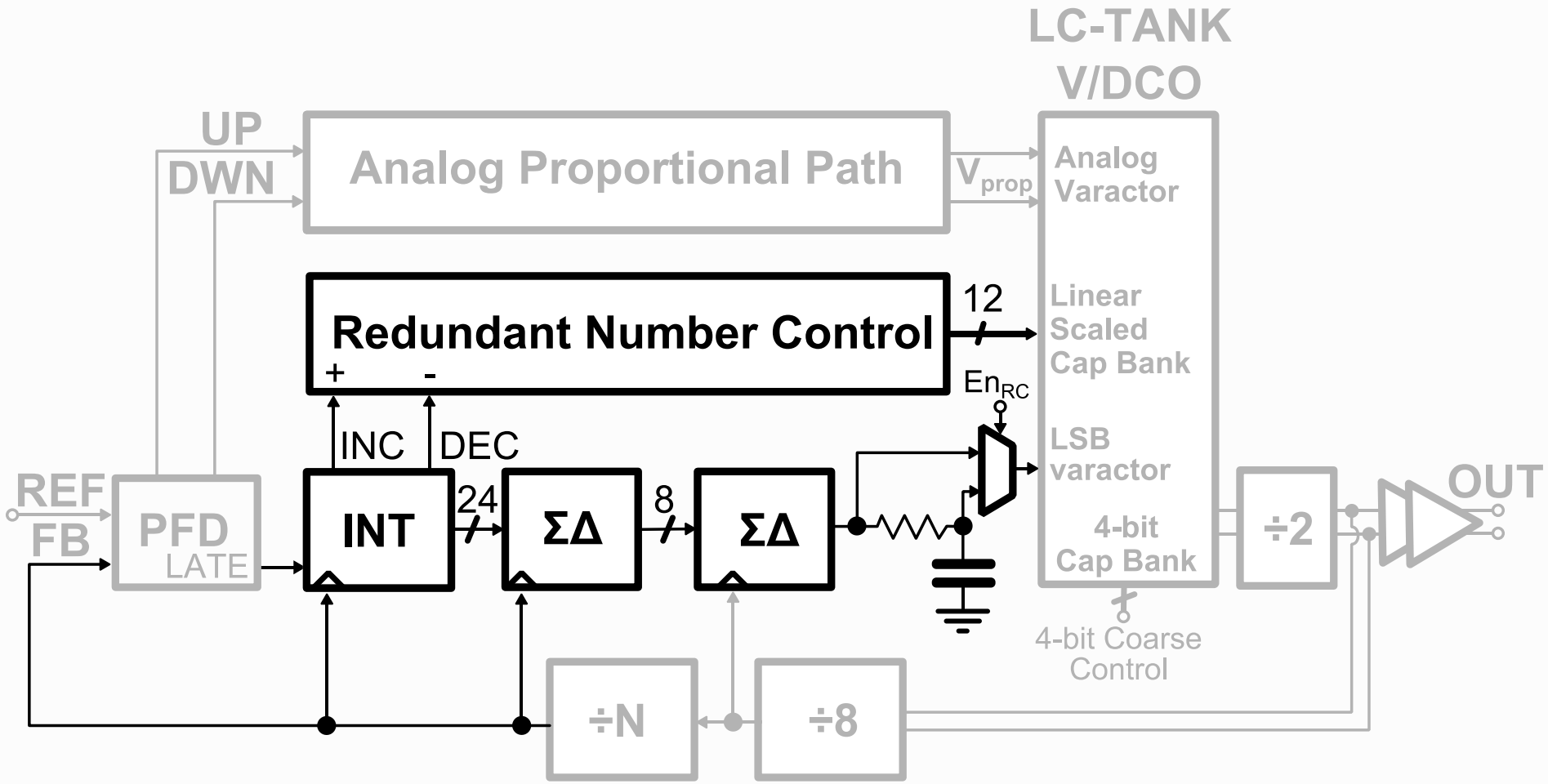
- **Proportional/Integral control path** operates over large voltage range → requires charge pump to operate across wide voltage range
- **Proportional path** stays close to common-mode (once PLL is locked) → relaxes charge pump performance requirements

Proportional path simplifications enabled by dual path architecture

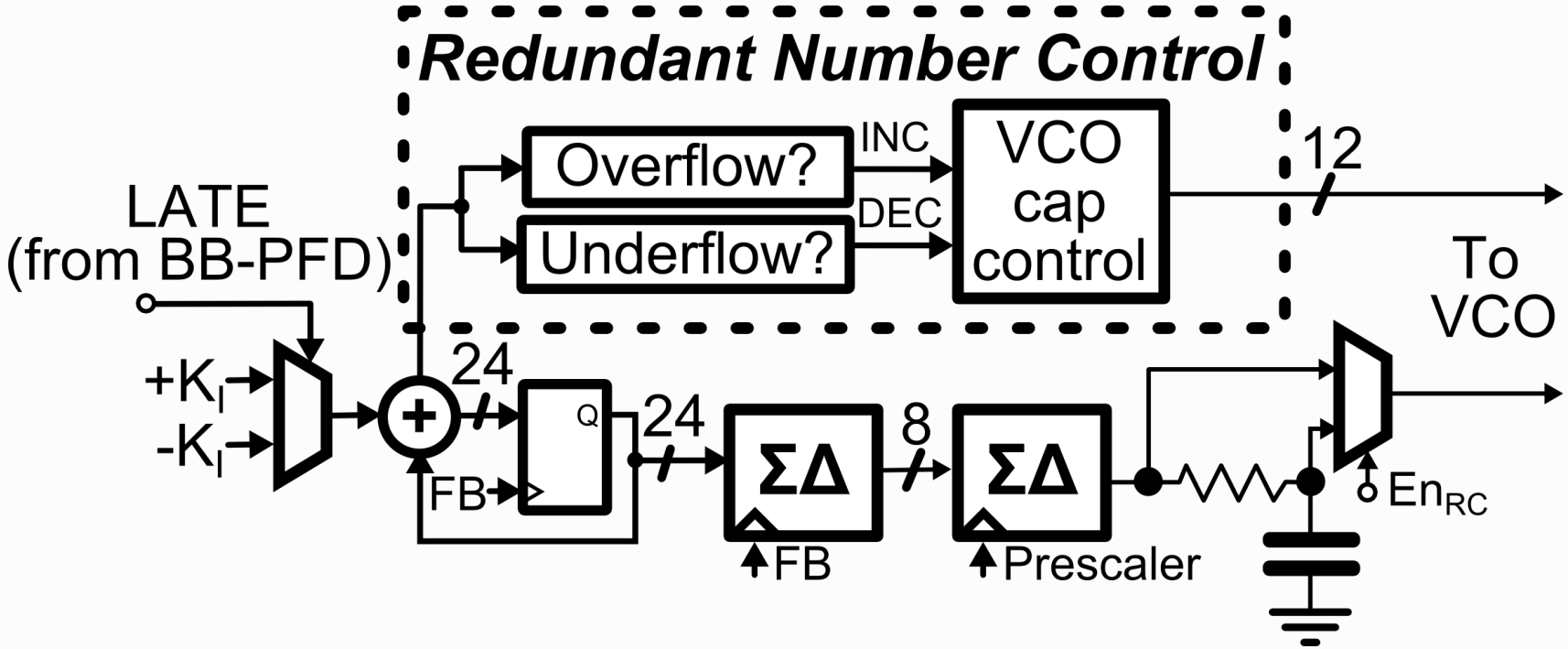


- Switched resistor scheme has lower flicker noise than conventional CP
- Common mode control greatly simplified

PLL integral path control

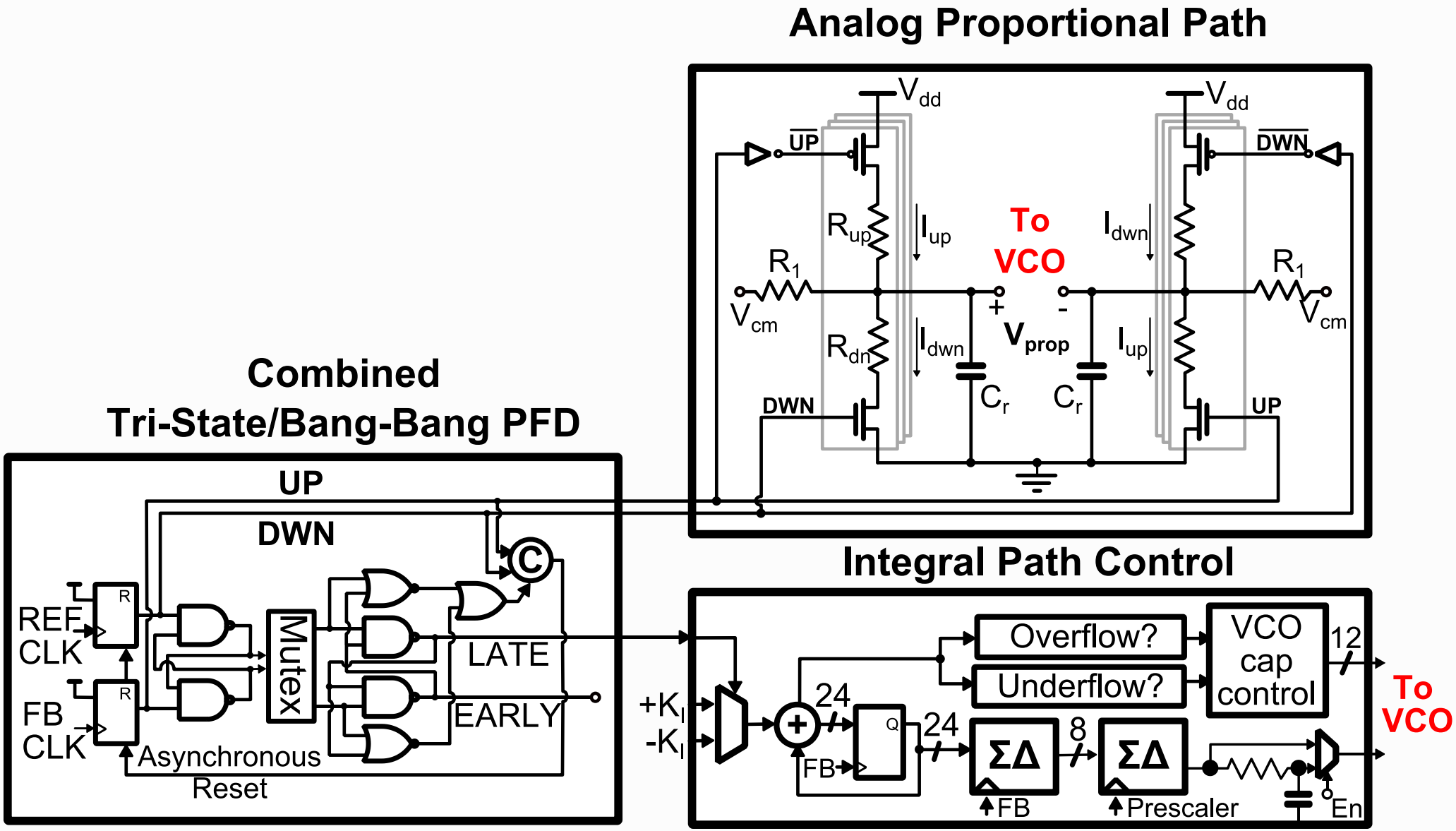


Integral path overview

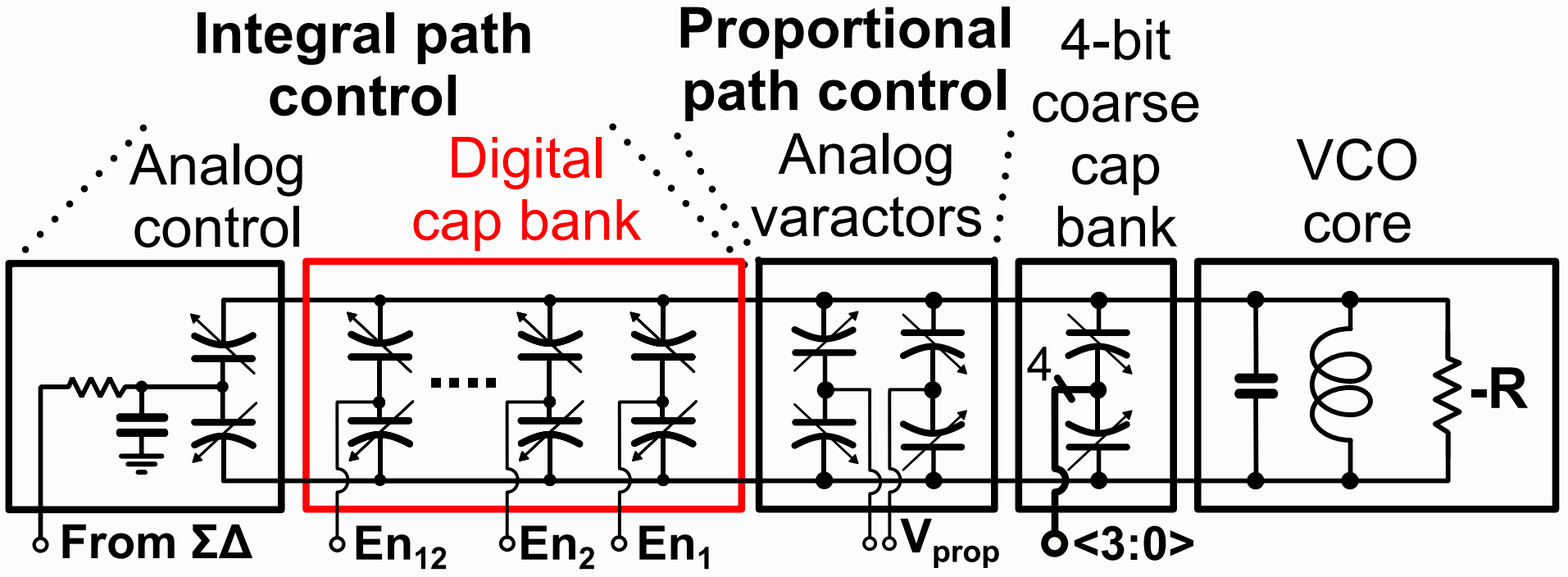


- Digital accumulator step size, K_I, programmable using serial interface
- VCO frequency control split into two paths
  - A 12-bit digitally switched capacitor bank
  - A ΣΔ-controlled analog varactor

Composite hybrid PLL control path

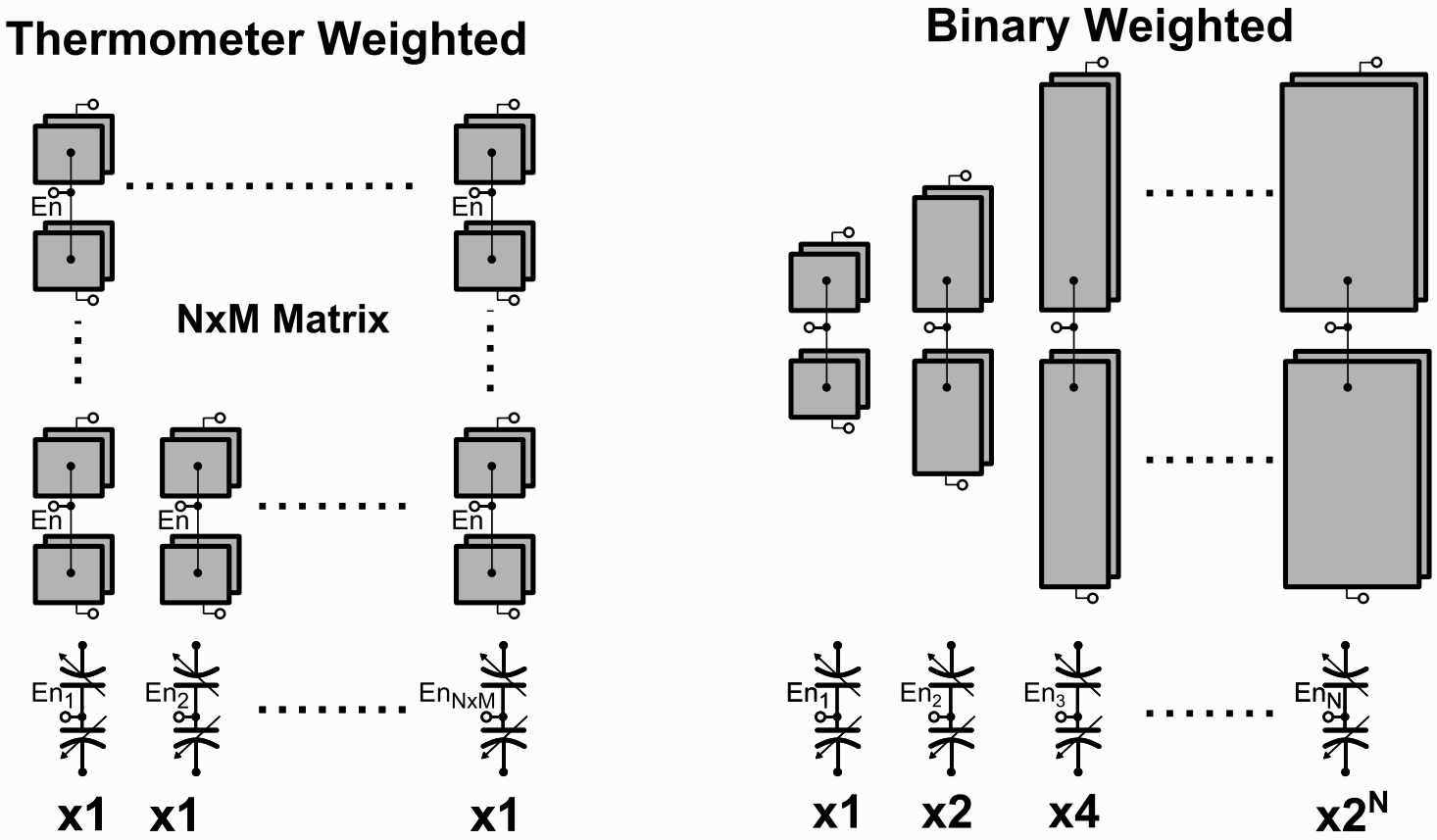


VCO conceptual diagram



- Control of VCO comprised of a mixture of digitally switched capacitors and varactors
- Implementation strategy for integral path digital cap bank: ***redundant numbering***

The VCO capacitor bank: options

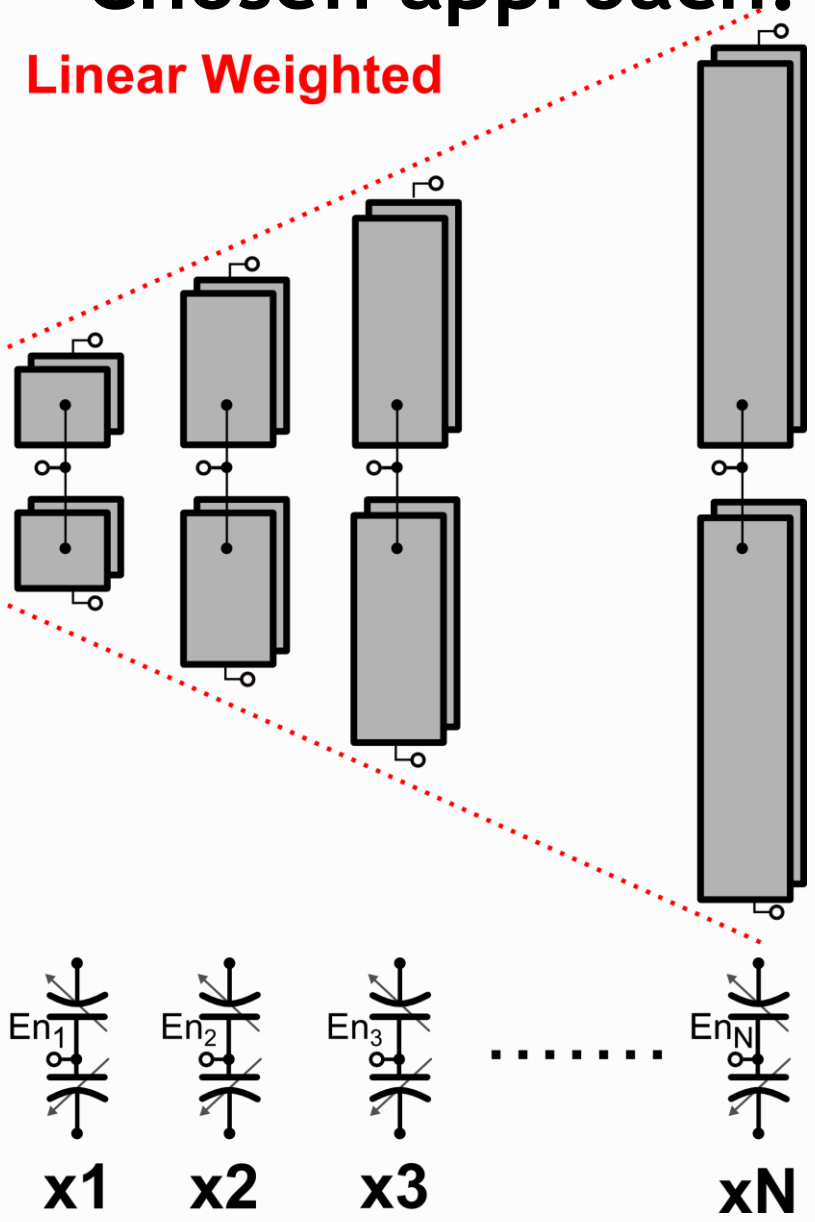


- Very large number of control lines
- Complex interconnect inductance, difficult to extract and simulate

- Stringent matching requirements
- Major code transition problem
  - 01111 → 10000

Is there a better way?

Chosen approach: redundant numbering



- Fewer control lines than thermometer weighted
- Matching requirements easier than binary
- Many capacitor configurations can result in the same total capacitance: ***scheme is redundant***
- Major code transitions can be avoided by utilizing redundancy

Integral path digital control options

Coding Scheme	Redundant numbering	Thermo-meter	Binary
Steps	78	78	64-128
Control wires	12	78	6-7
Matching requirements	moderate	trivial	extreme
Simultaneous switching events per inc/dec	2	1	Up to 7 1000000→0111111

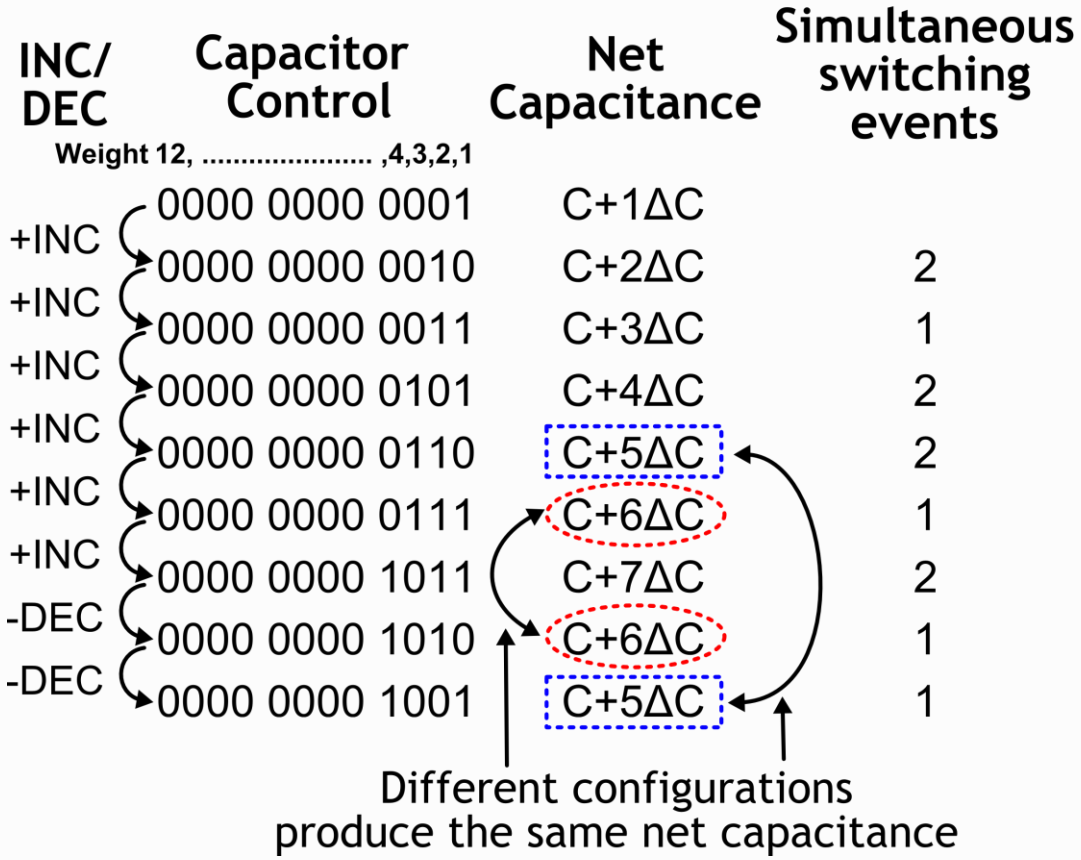
Redundant numbering based capacitor bank

→ Fewer switching events than binary

→ Fewer control lines than thermometer

Switching sequence example

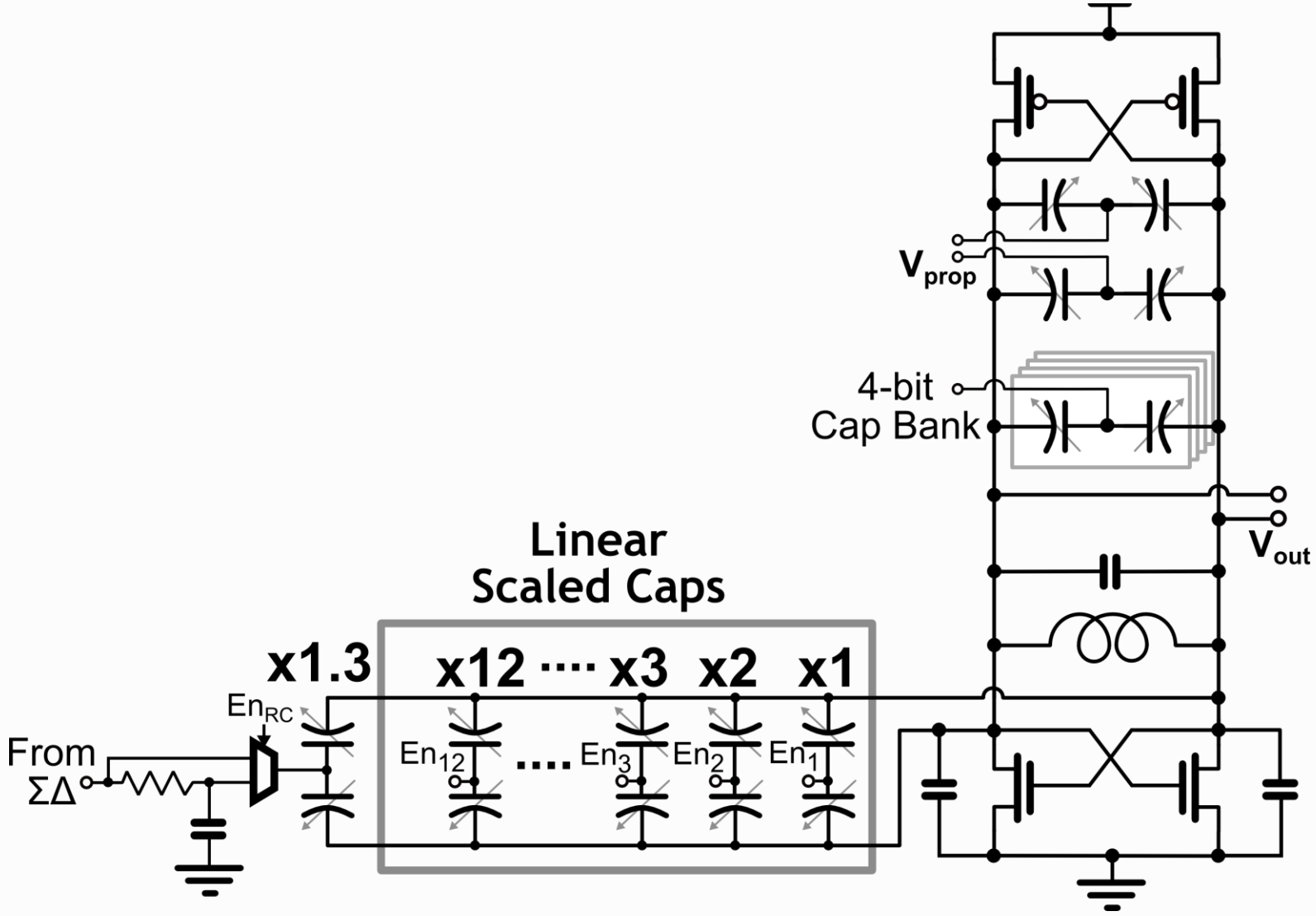
Example Control Sequence



We can increment or decrement with at most 2 capacitor changes → mitigates major code transition problem

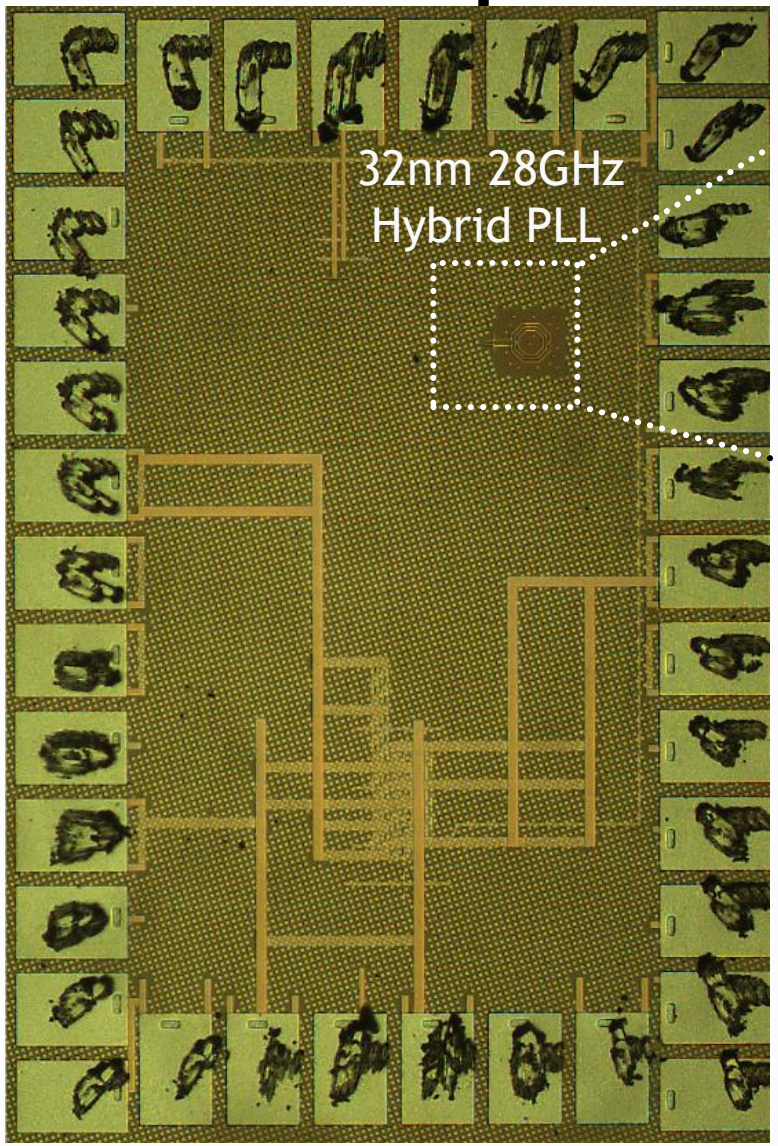
. . . But transition problem remains—better solutions described later in talk

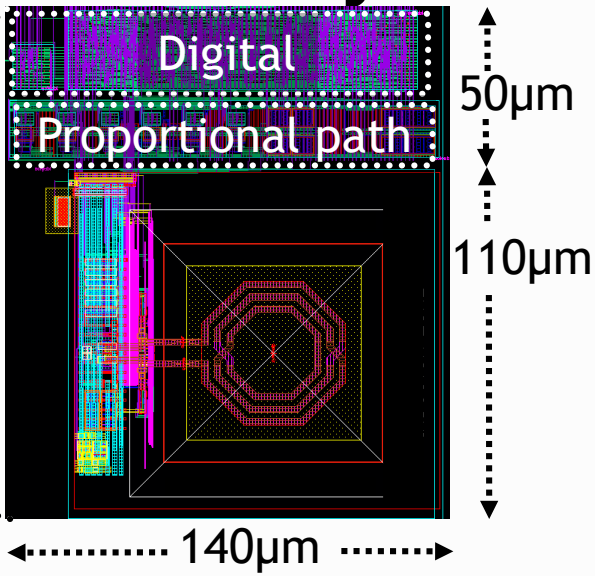
VCO schematic view



ΣΔ path varactor oversized to prevent gaps in tuning range

Die microphotograph, physical design, and performance summary

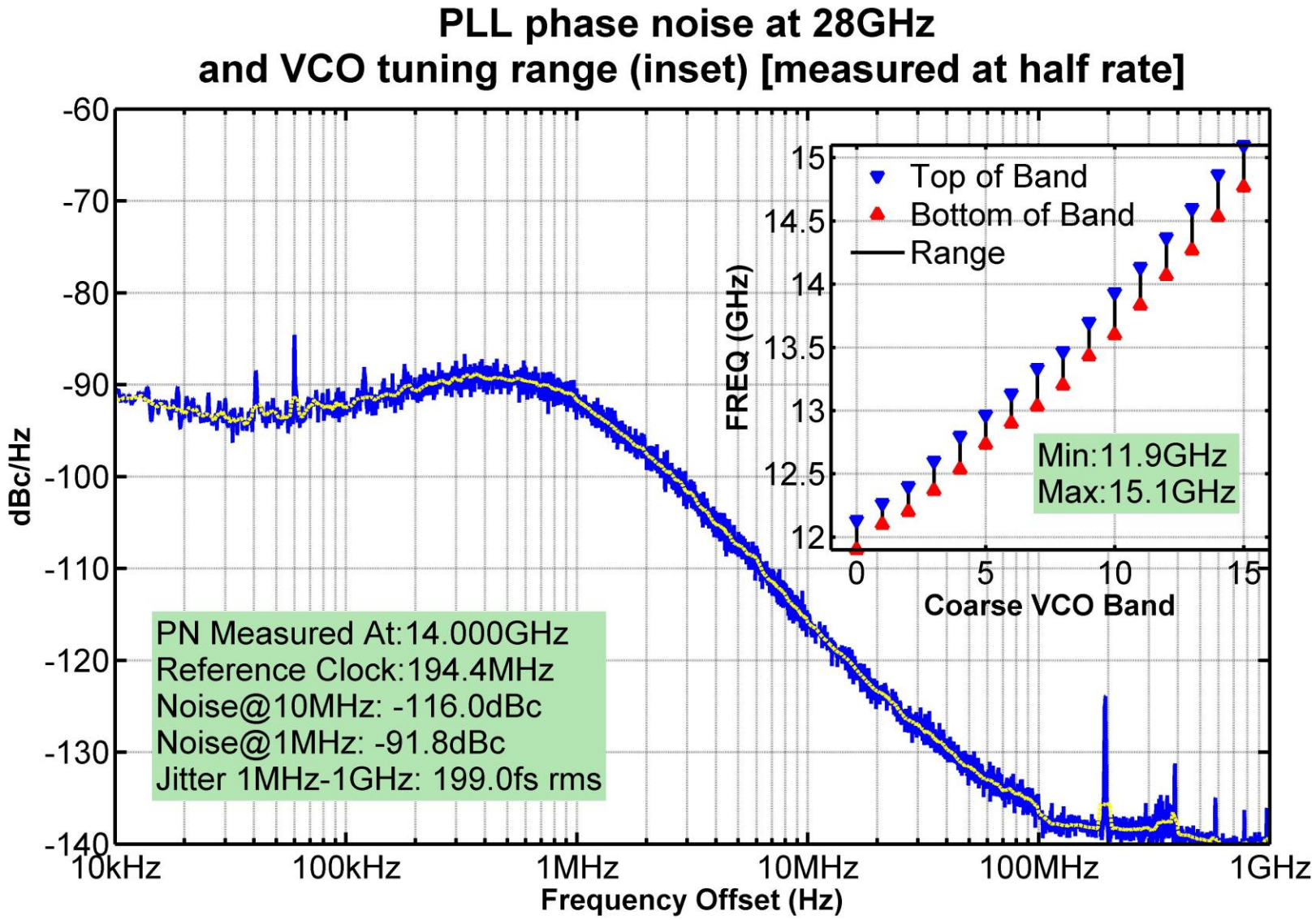




Performance Summary

Area (32nm CMOS)	0.0225mm^2
Power	31mW from 1V
Frequency range	23.8-30.2GHz
Phase noise @10MHz	-110dBc/Hz
Phase noise @1MHz	-86dBc/Hz*

*Varies with bandwidth

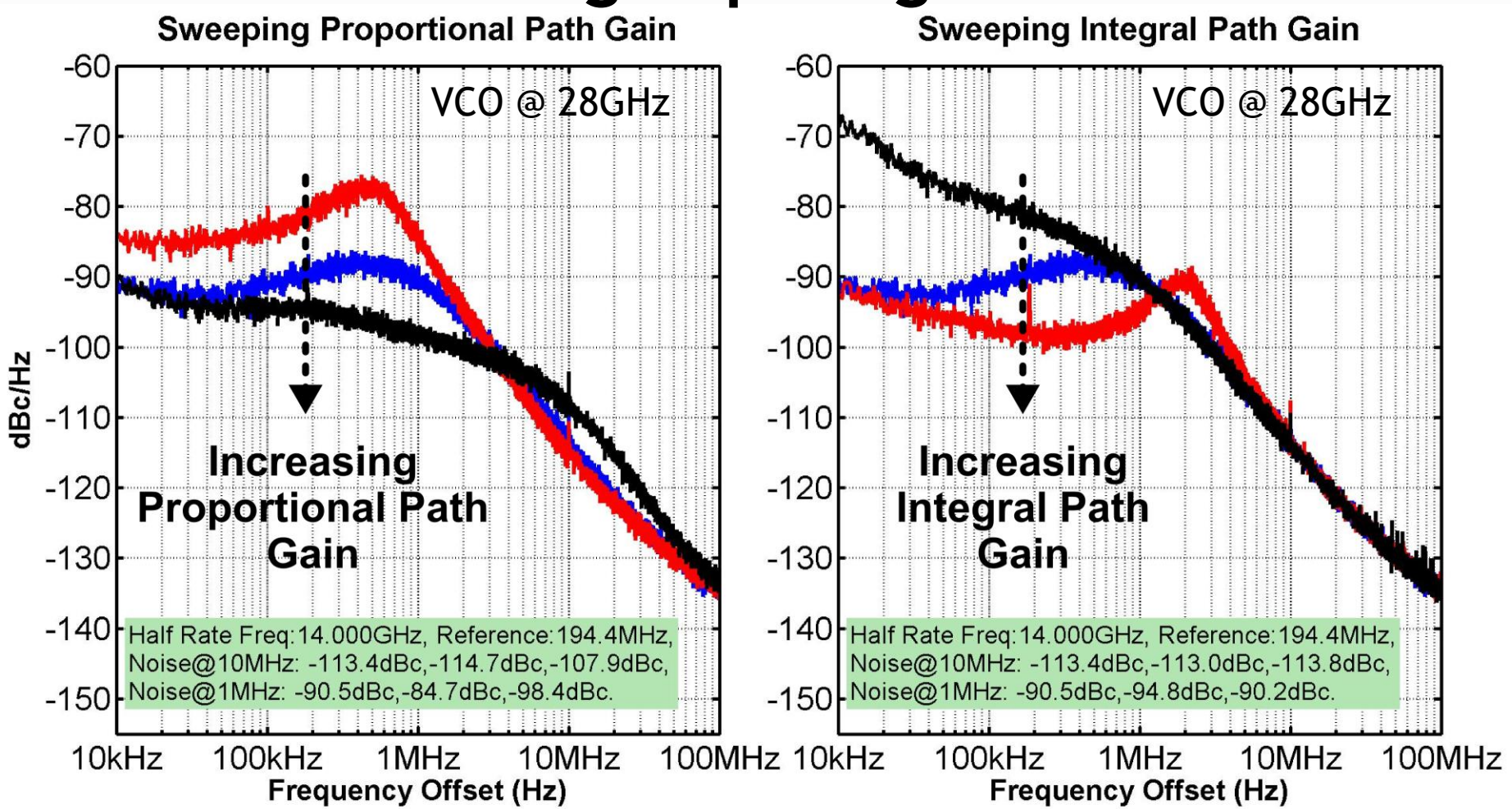


For equivalent full rate phase noise, add 6dB

[-110dBc/Hz @10MHz from 28GHz]

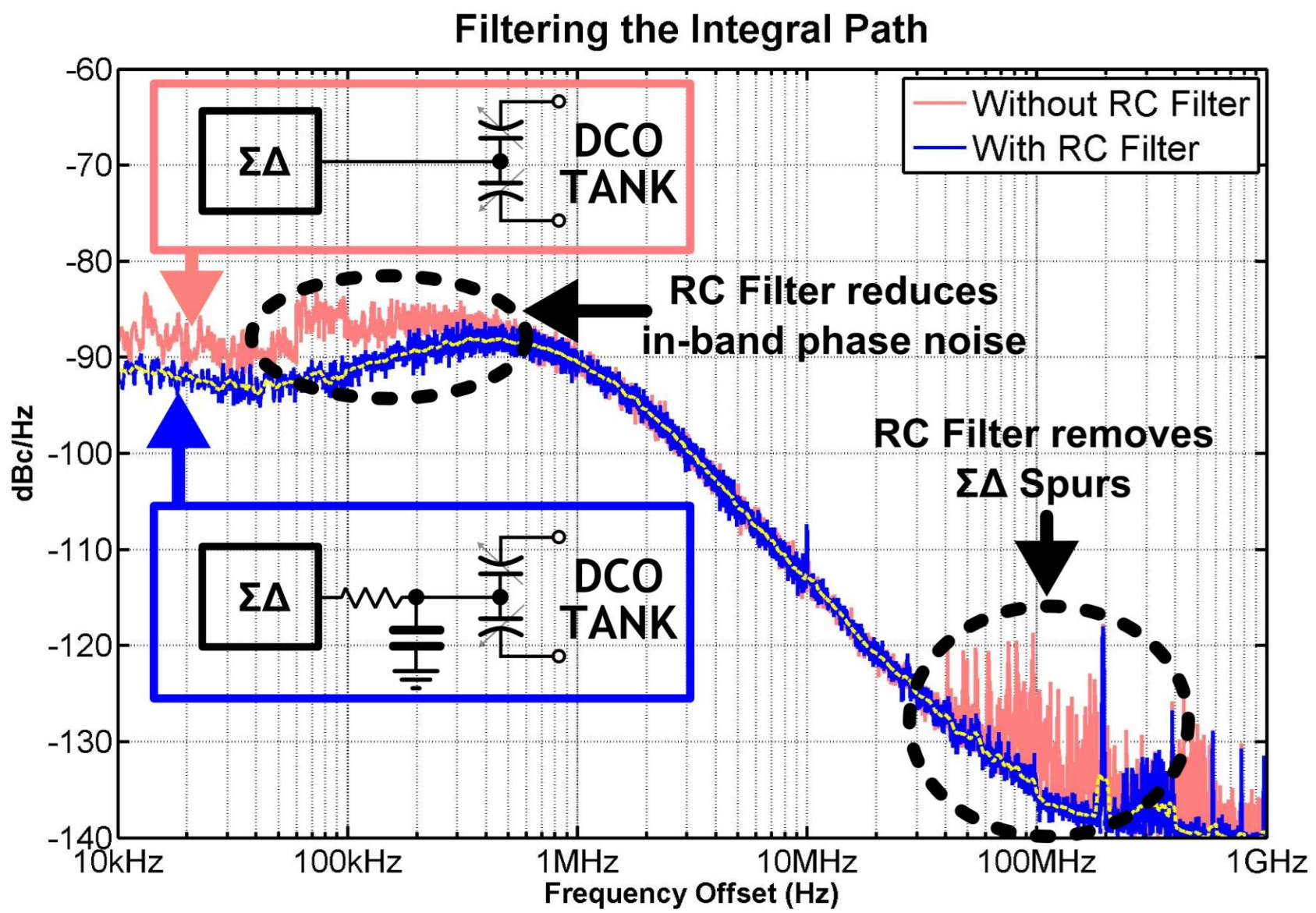
M. Ferriss et al, VLSI13, JSSC14

Demonstration of independent control of proportional and integral path gains



Hybrid PLL responds to changes in proportional/integral path gains in a similar fashion as a dual path analog PLL

Measured effects of RC filter on ΣΔ output



Conclusion: Initial High Performance Hybrid PLL Implementation

Key results

- A 28GHz, low noise hybrid PLL drawing 31mW from 1V demonstrated in 32nm CMOS
- Compact, digital friendly implementation comparable to that of digital PLL achieved
- Linear phase response and spurious spectral content similar to that of all analog PLL achieved

Challenges

- Integral path redundant numbering implementation still problematic
- Does not really exploit opportunities presented by hybrid architecture

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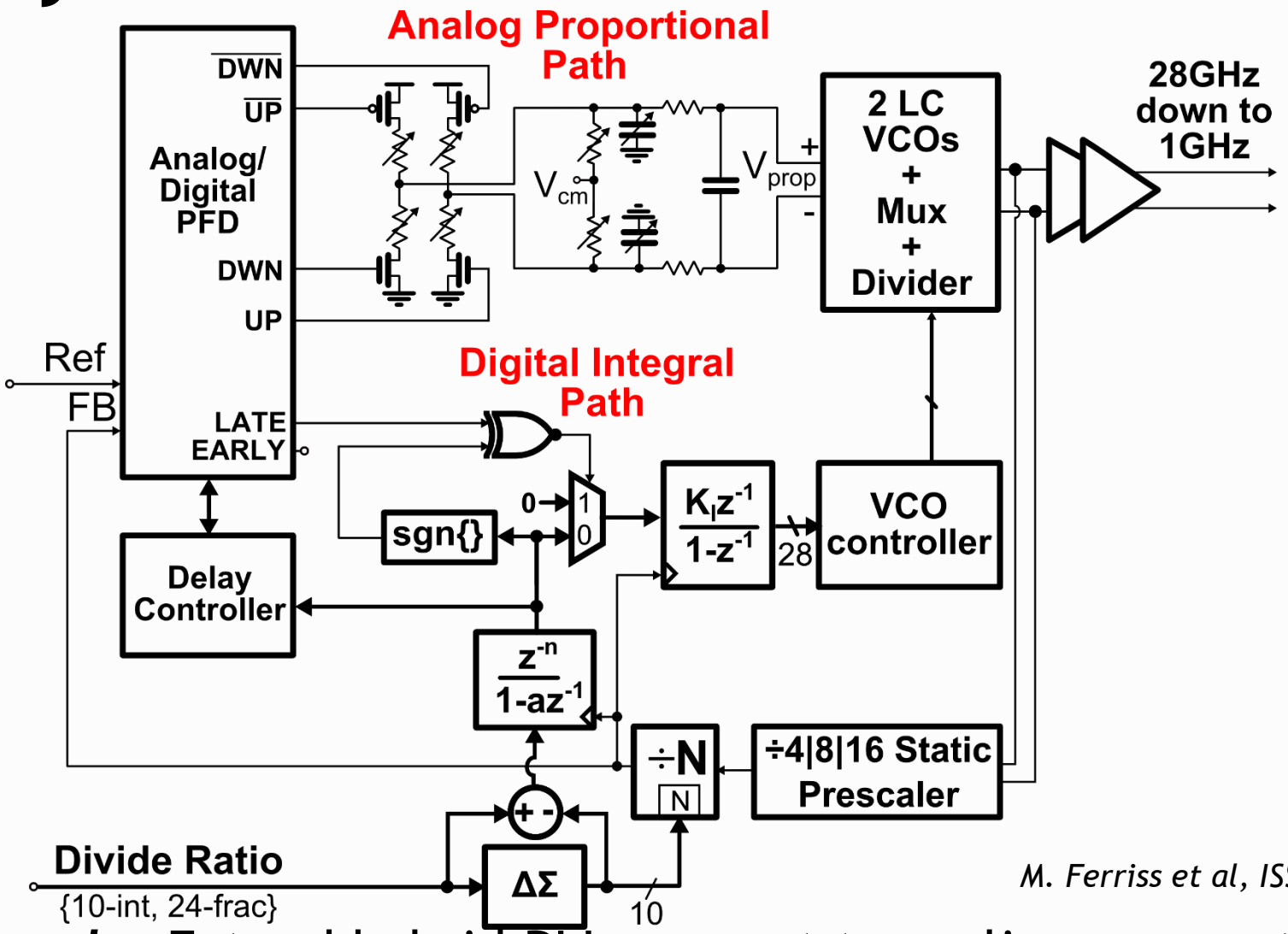
Fractional-N Hybrid PLL

- Objective: demonstrate frac-N synthesizer with integrated noise cancellation compatible with hybrid PLL architecture, and demonstrate new features enabled by the architecture
- Approach
  - Introduce proportional path digital-to-time conversion infrastructure
  - Introduce integral path scale/ignore infrastructure
  - Explore use of replay to support fast hopping
- Key challenges
  - Introduction of new elements
  - Support background calibration of digital-to-time converter

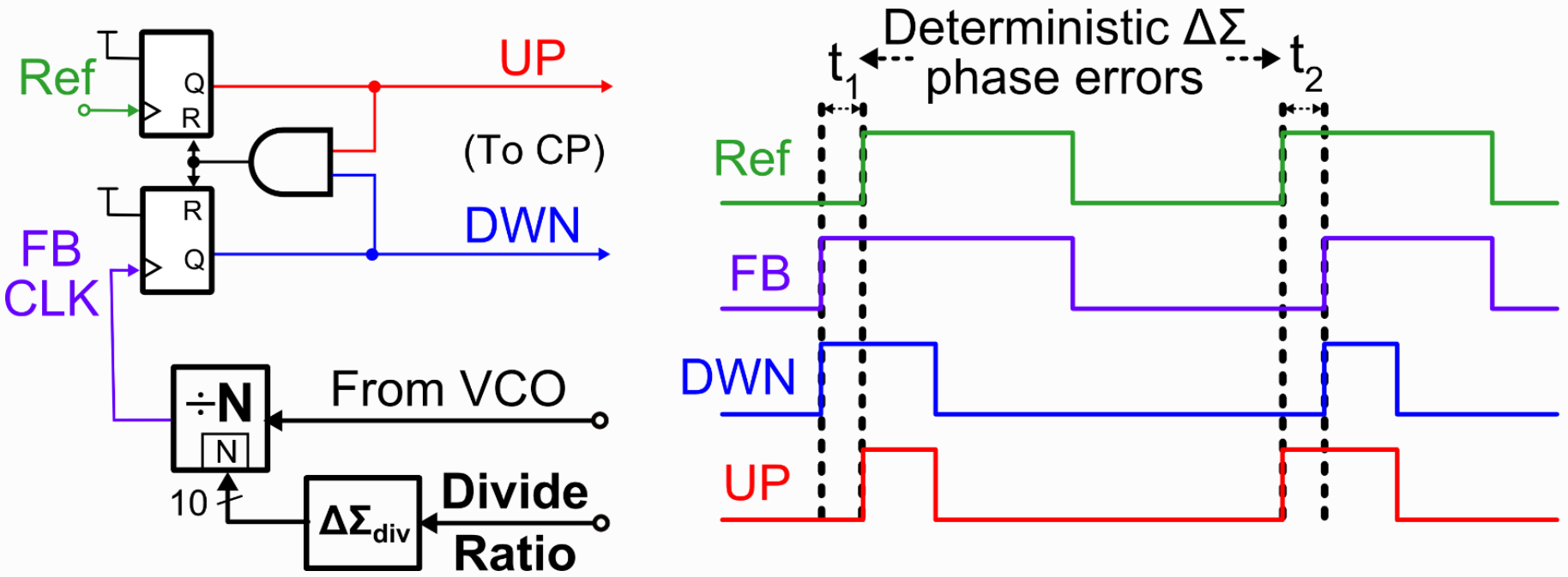
Hybrid PLL Architecture: Frac-N



M. Ferriss et al, ISSCC15

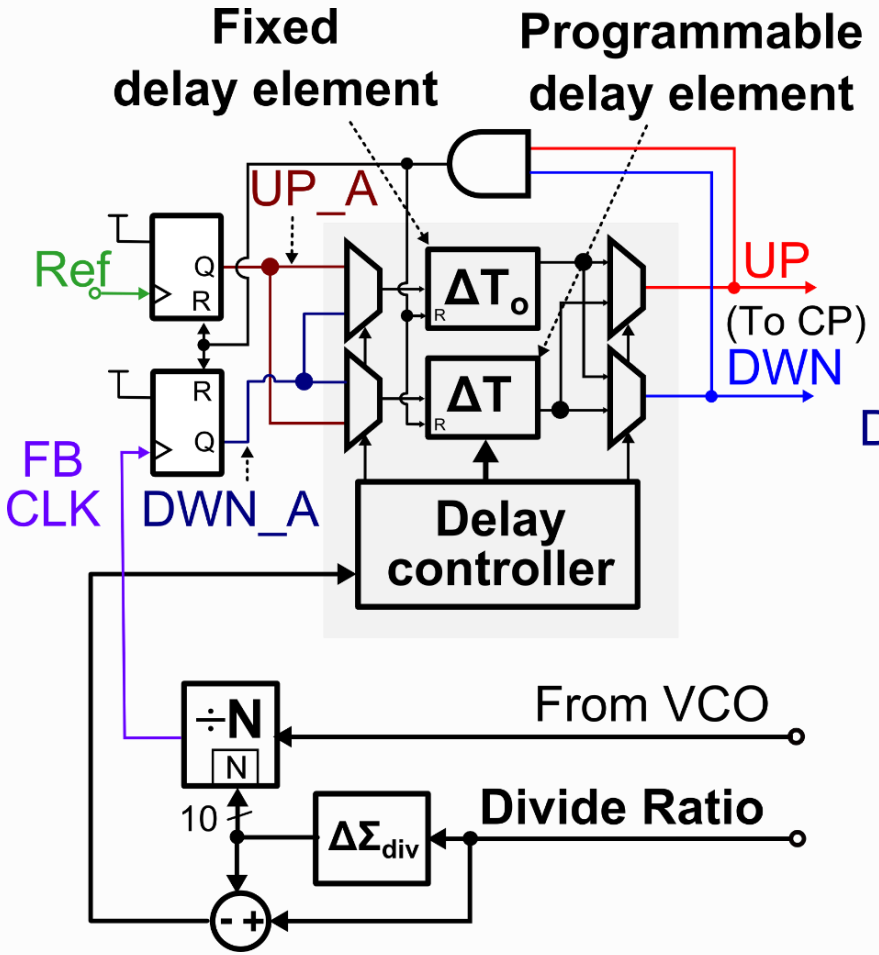
Technical Approach: Extend hybrid PLL concept to realize compact, flexible fractional-N synthesizer

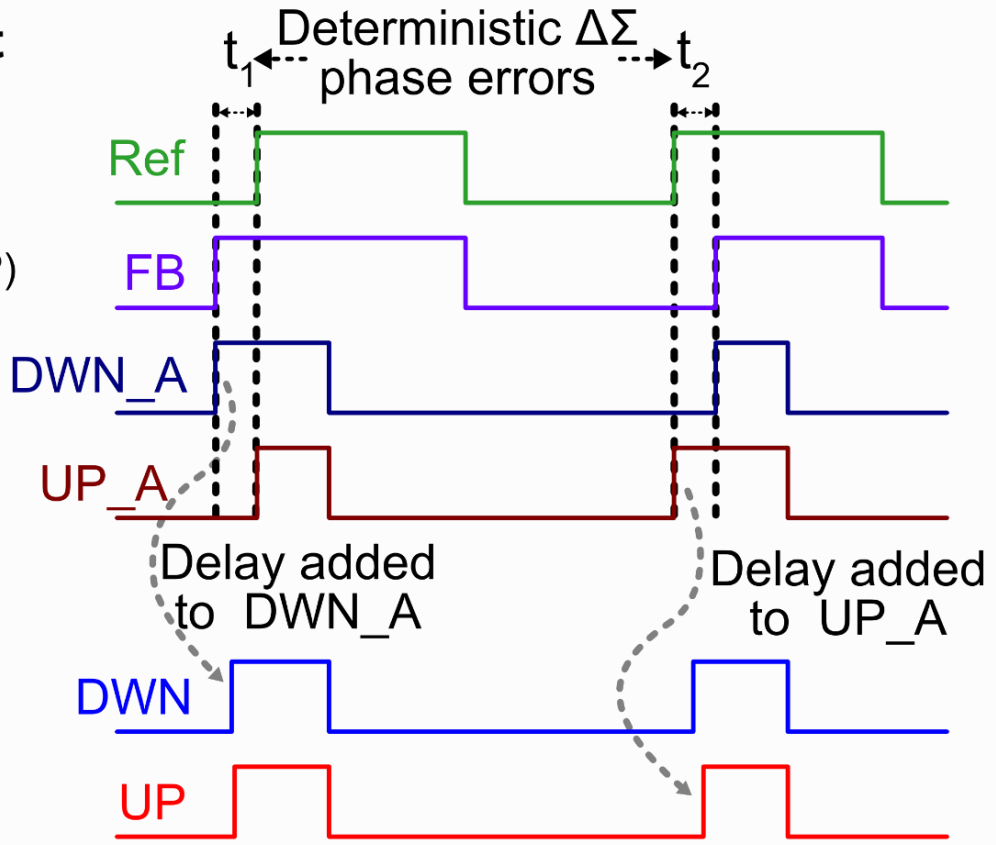
Classic ΔΣ Problem



- Divider's ΔΣ dithers PLL's feedback (FB) clock
- ΔΣ noise contributes to PLL's phase noise

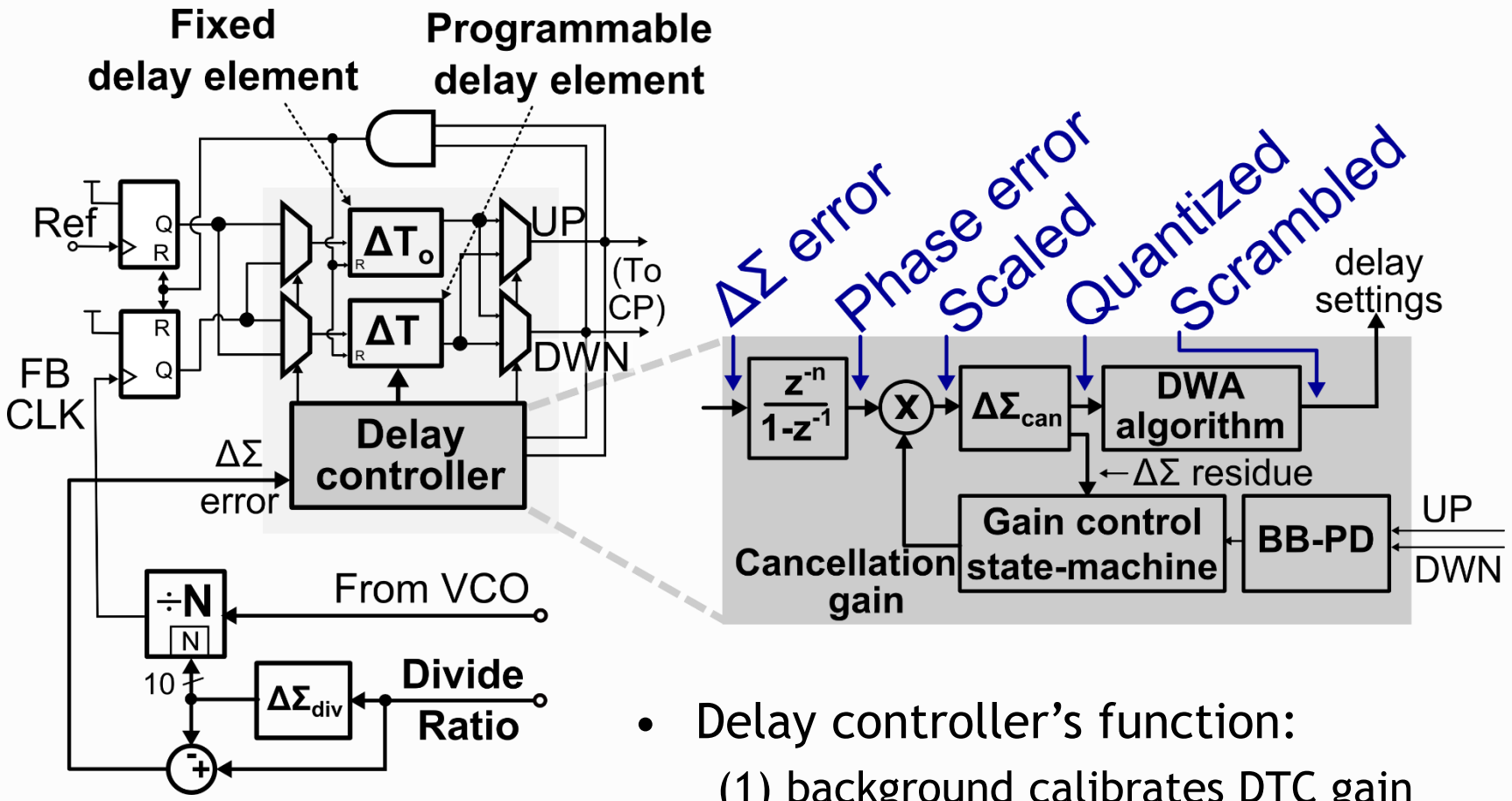
Time-based Cancellation Concept





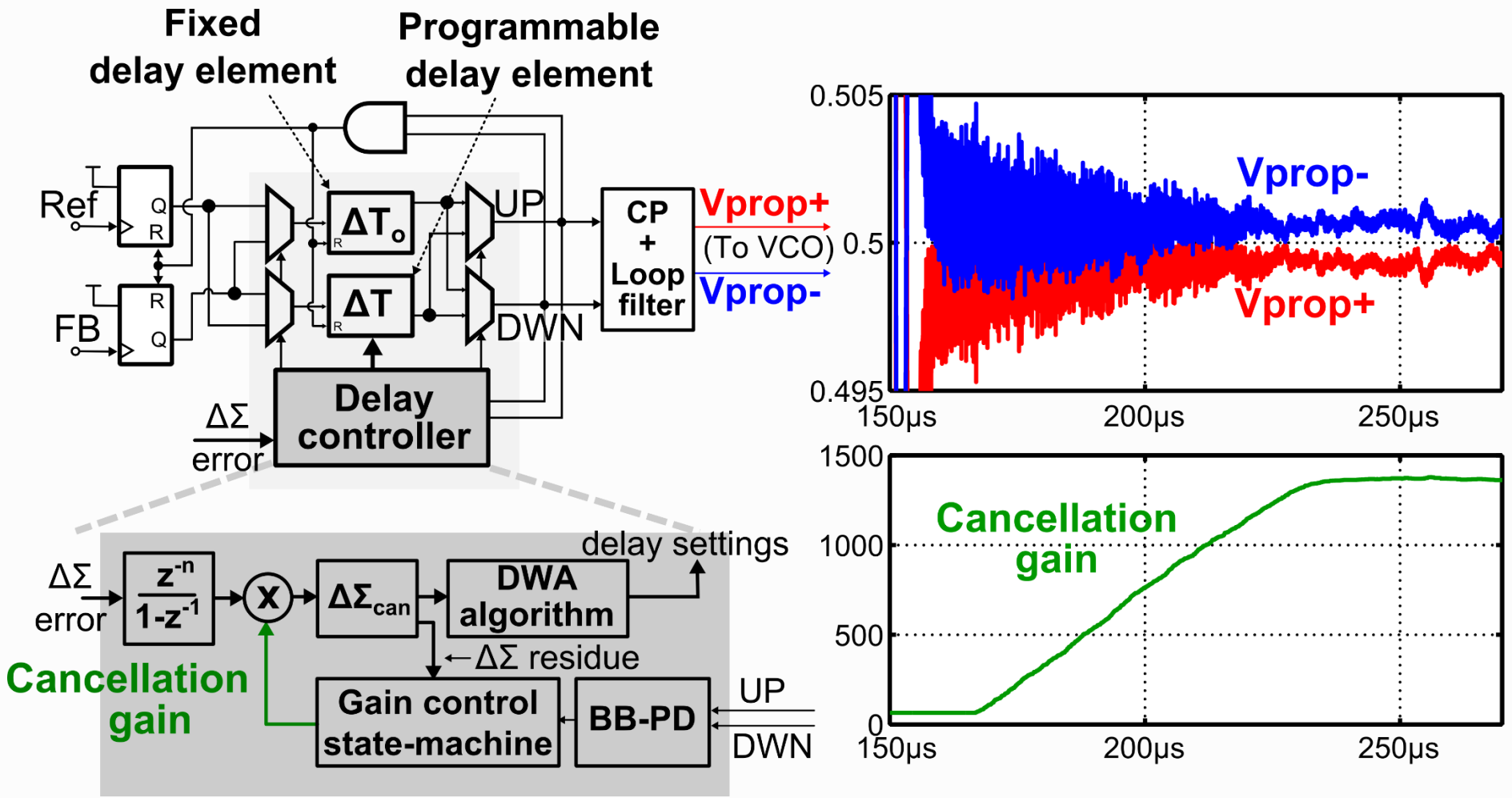
- Digital-to-time based delay scheme used *on analog path*
  - Utilizes loop filter's low pass response to remove delay path quantization noise → do not need fine quantization step.

Delay Controller Architecture

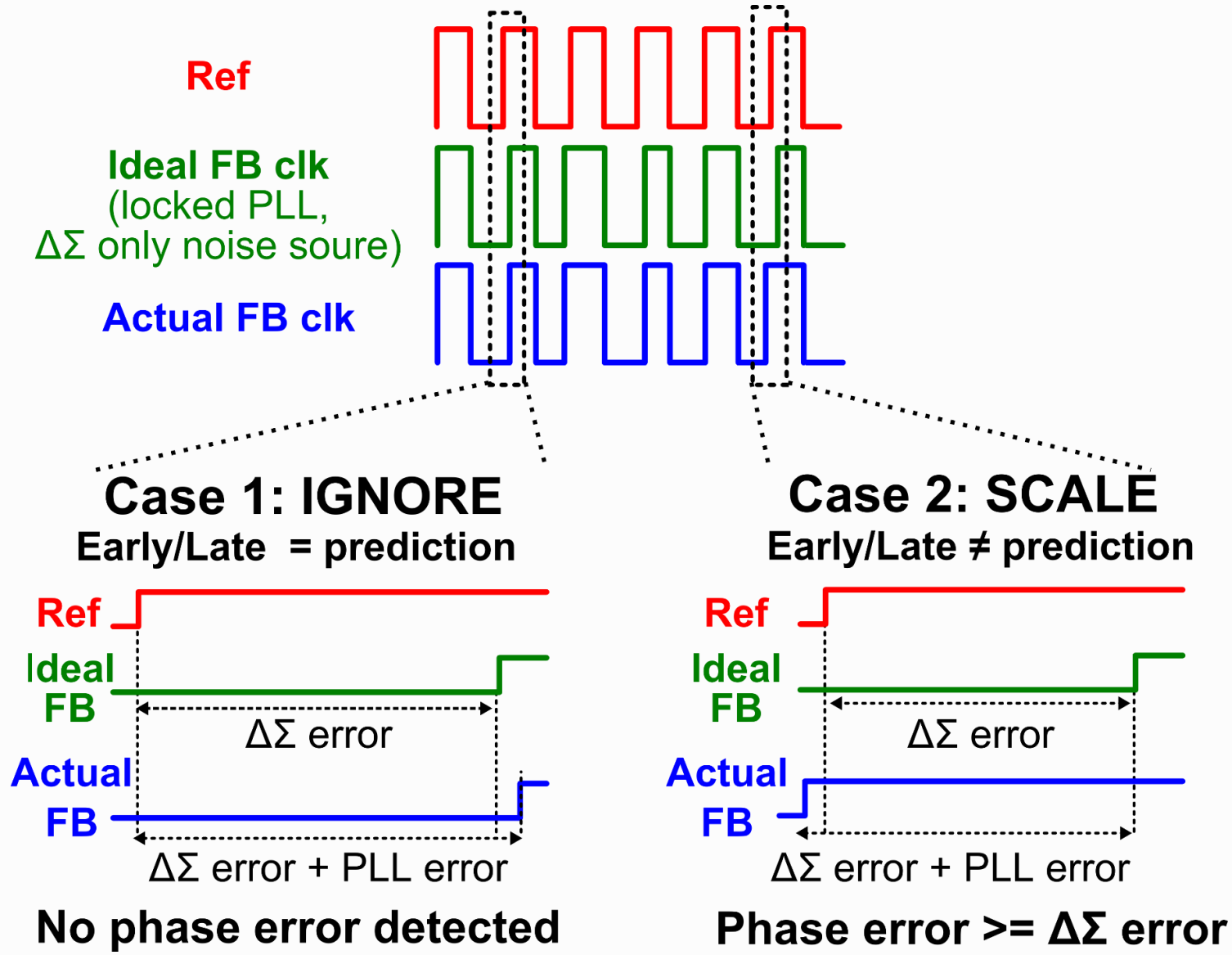


- Delay controller's function:
  - (1) background calibrates DTC gain
  - (2) shapes ΔT quantization error
  - (3) scrambles mismatch error

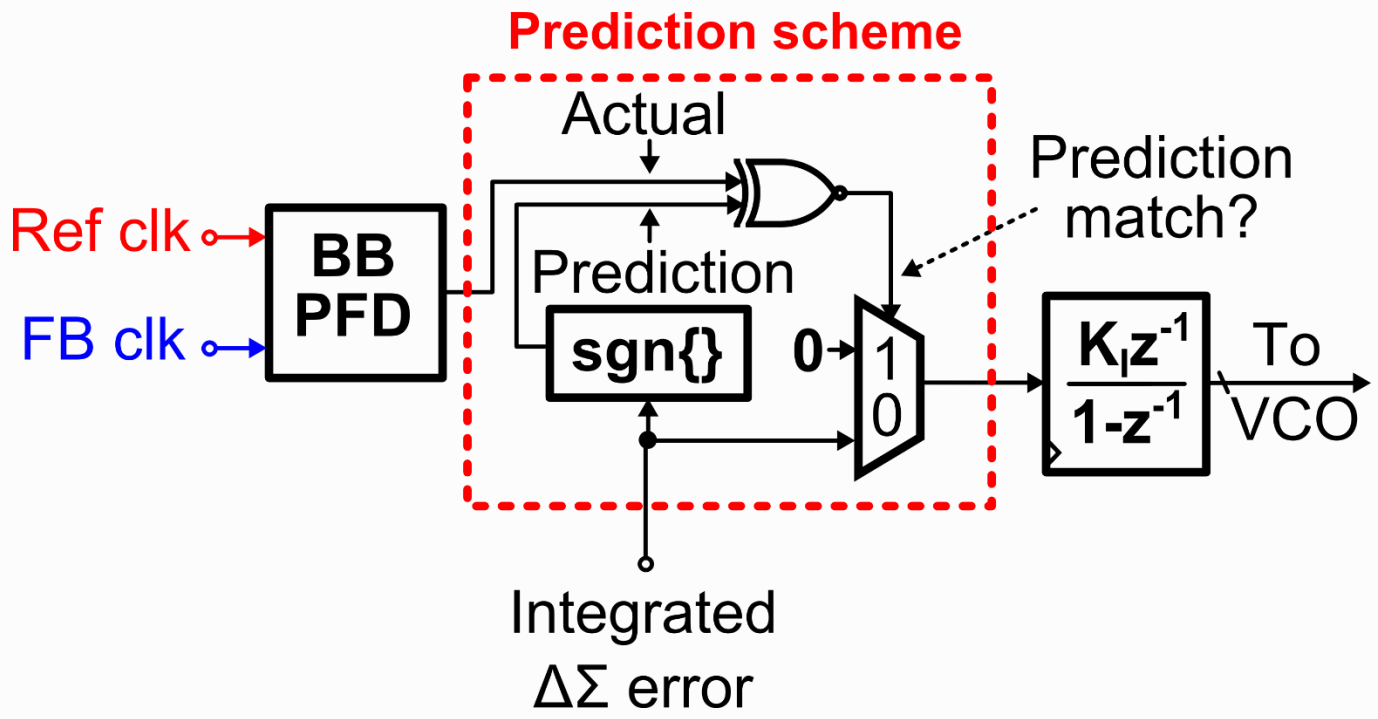
Delay Controller Operation Simulation



Integral Path Prediction Concept

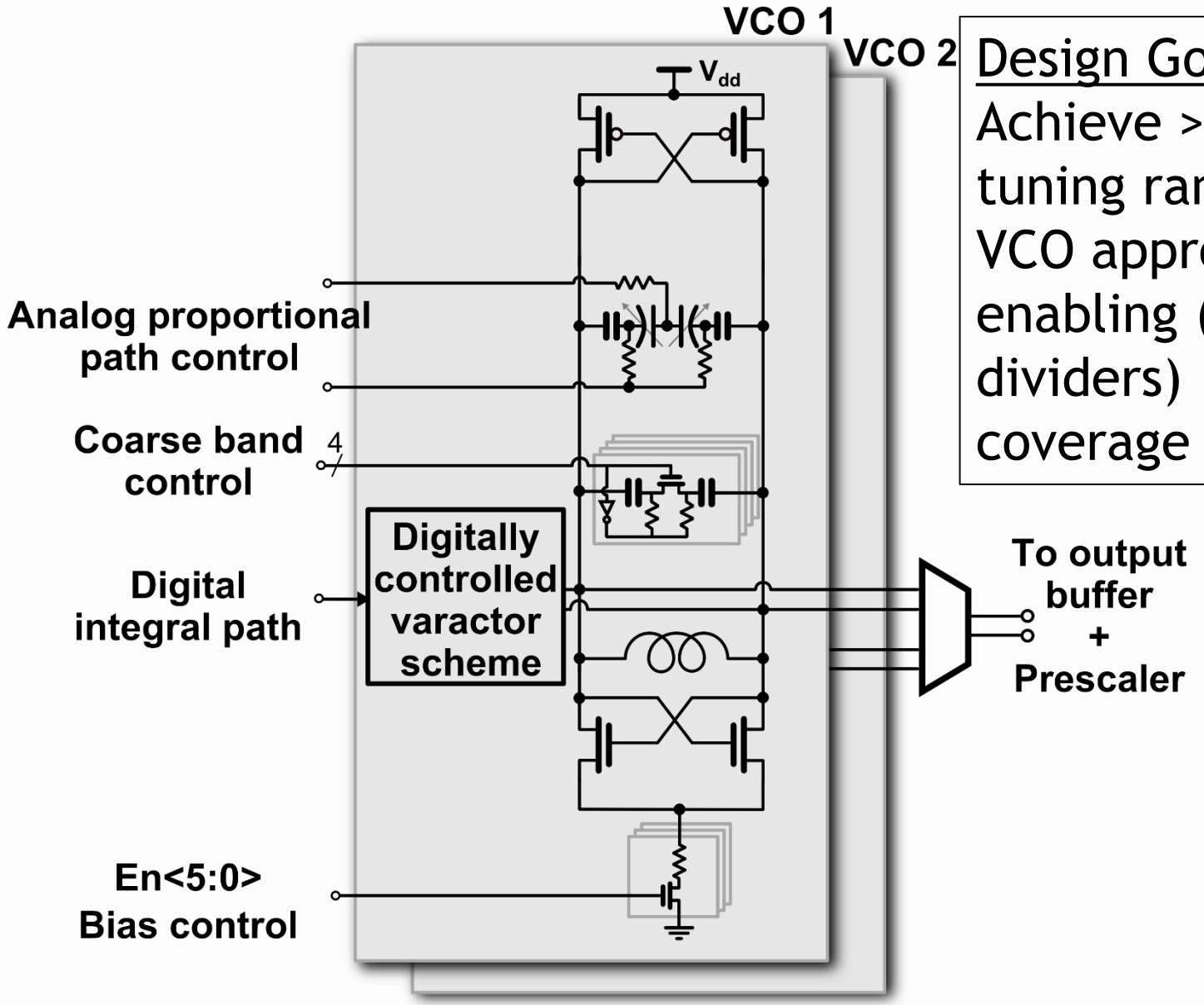


Integral Path Prediction Circuit



- Integral path operates from single BB phase detector
  - Works in parallel with the analog proportional path
- Ignores BB results that match prediction

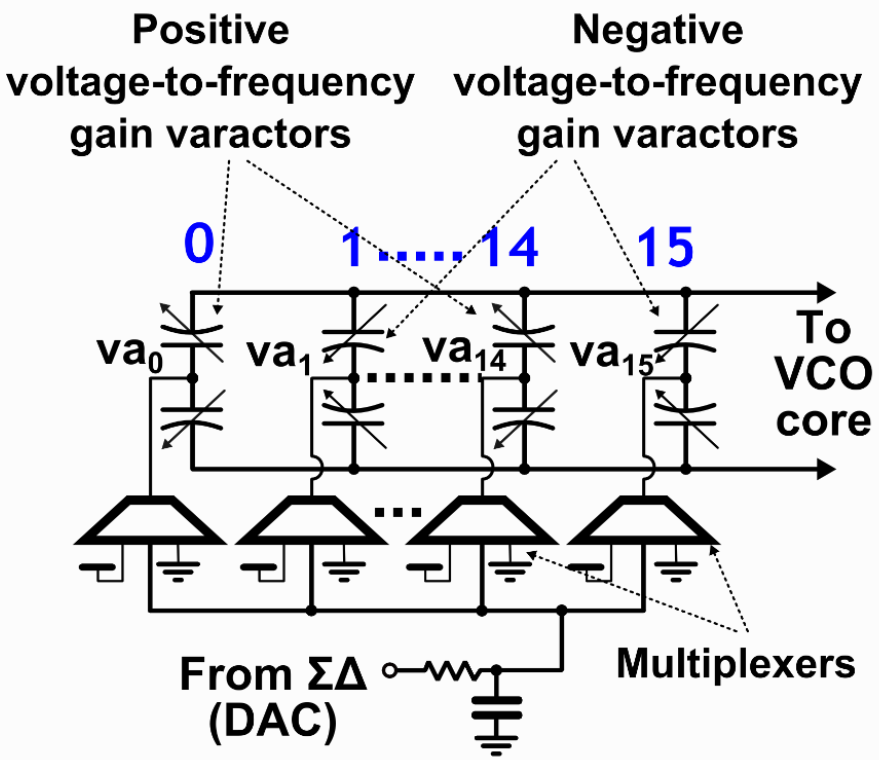
Dual D/VCO Scheme

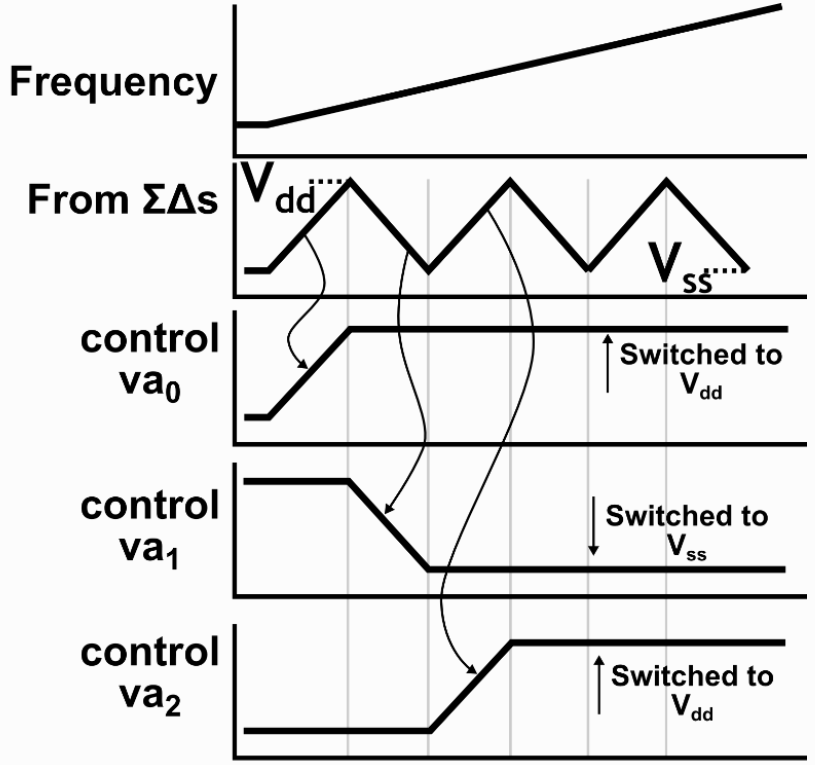


Design Goal:
Achieve > 1 octave of tuning range using dual VCO approach, enabling (with output dividers) 2-26GHz coverage

Improving the Integral Path: Introduction to Varactor Folding

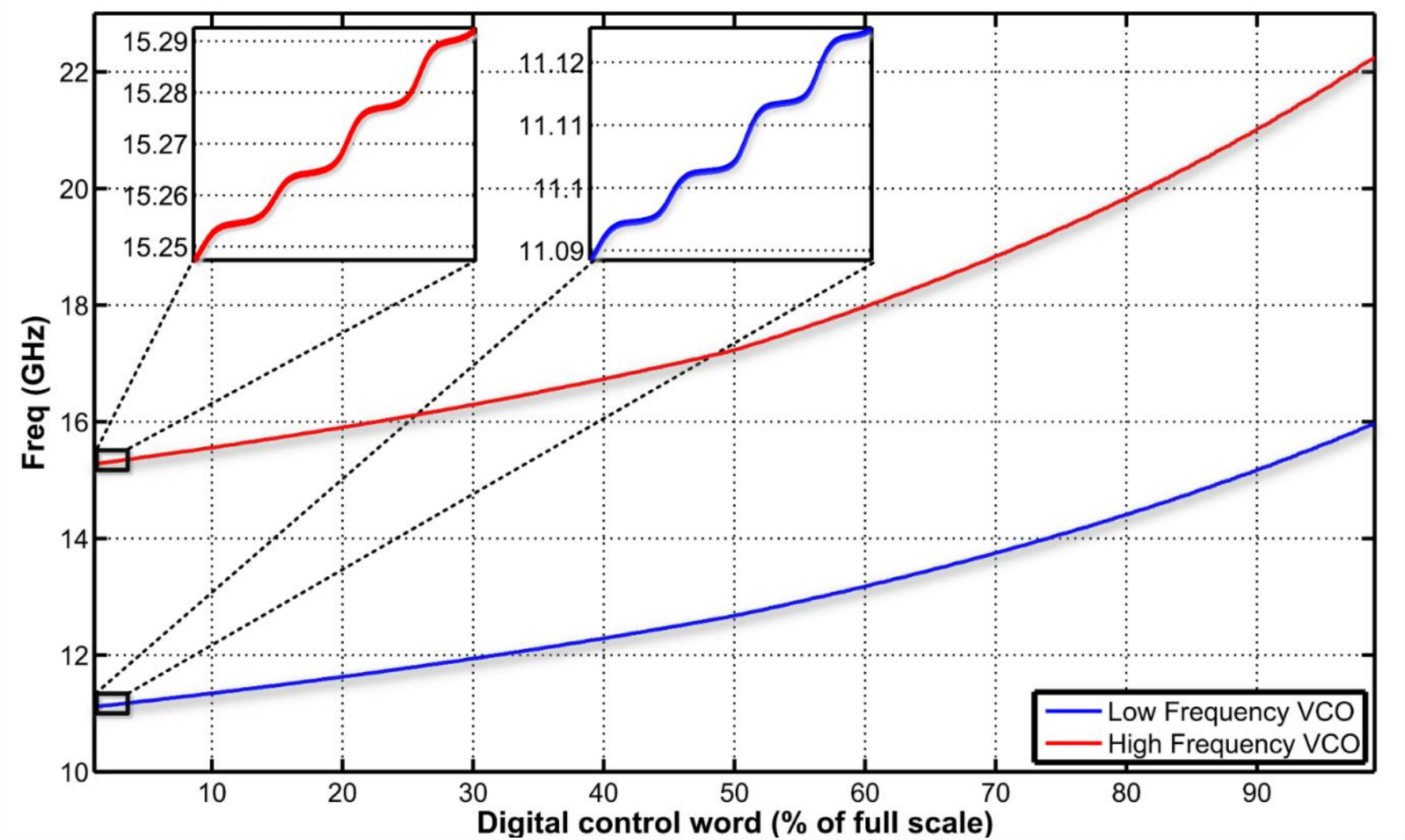
Objective: address disturbance that occurs in previous implementation's redundant numbering control scheme during digital switching



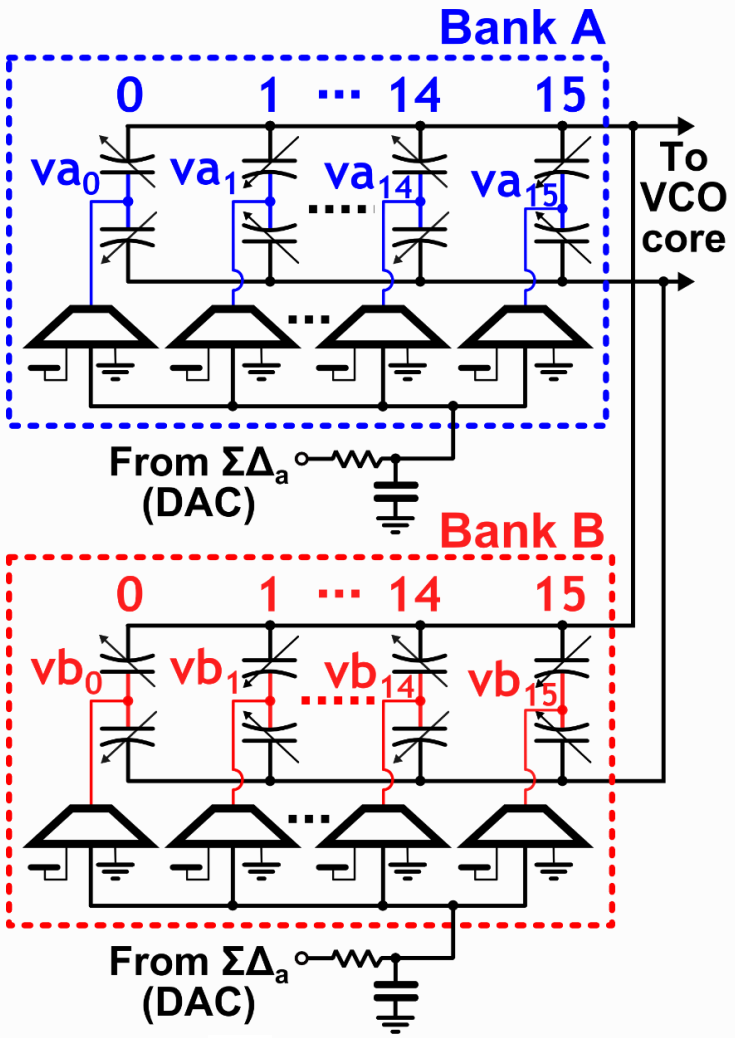


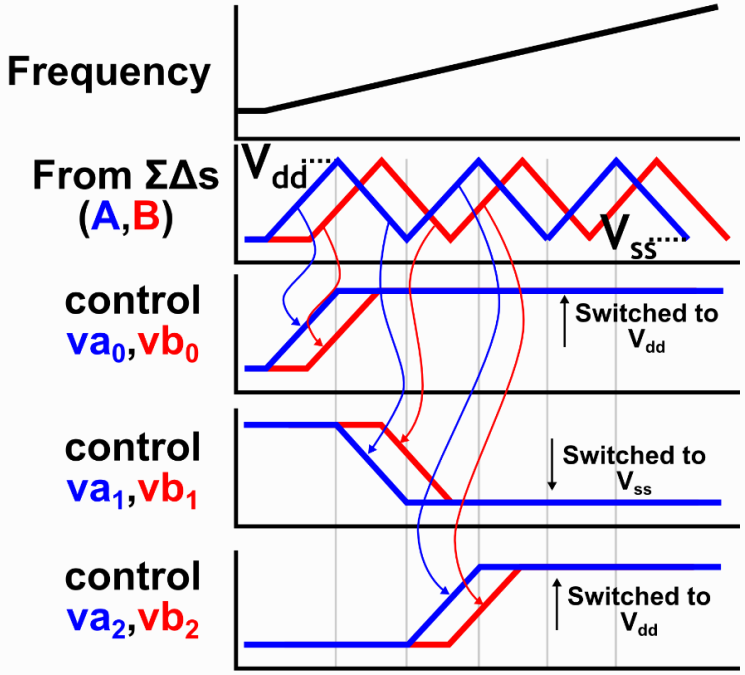
Similar concept used in P. Wang, et al., JSSC 2009

VCO Linearization Challenge



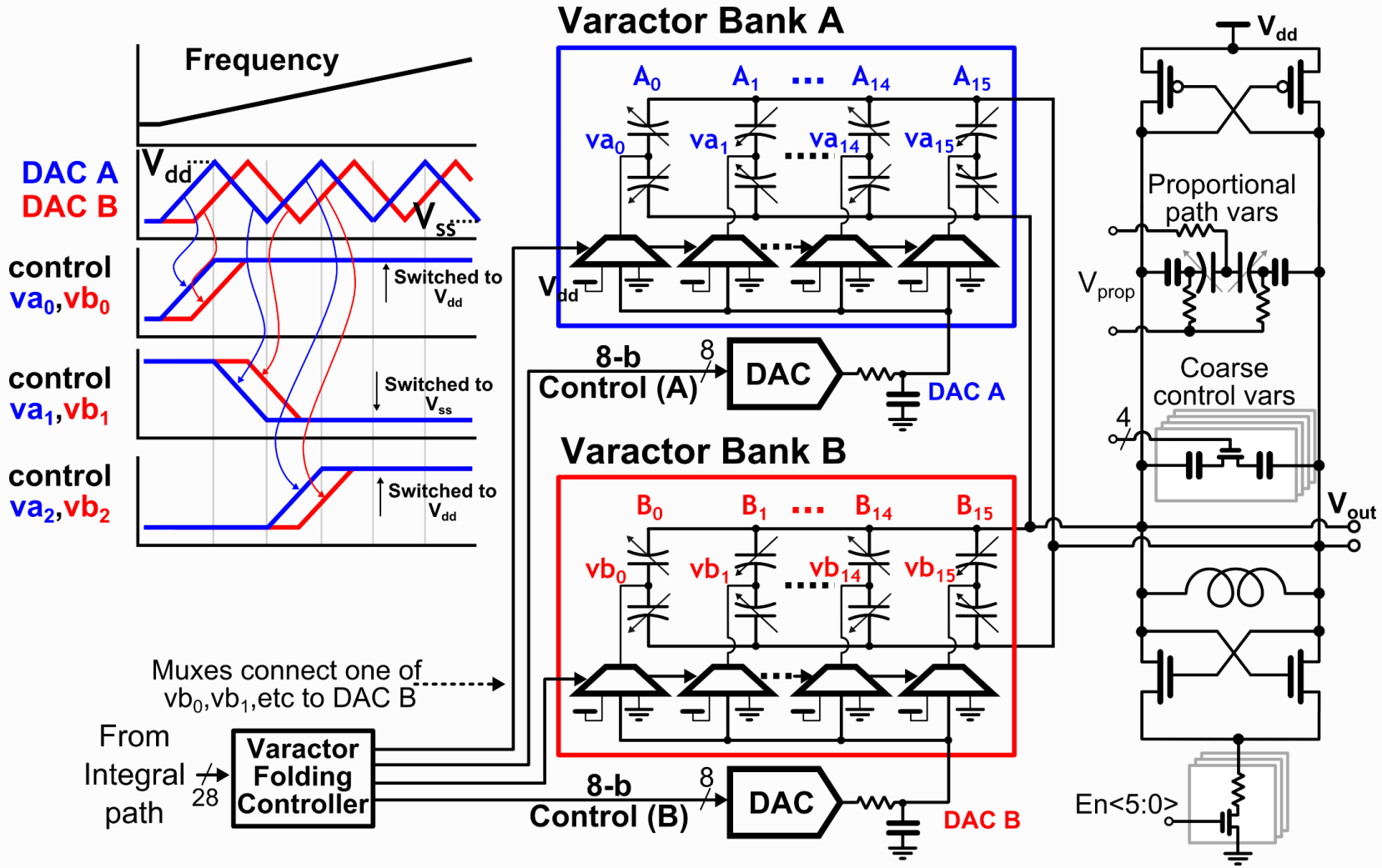
Linearization in the Varactor Folding Design





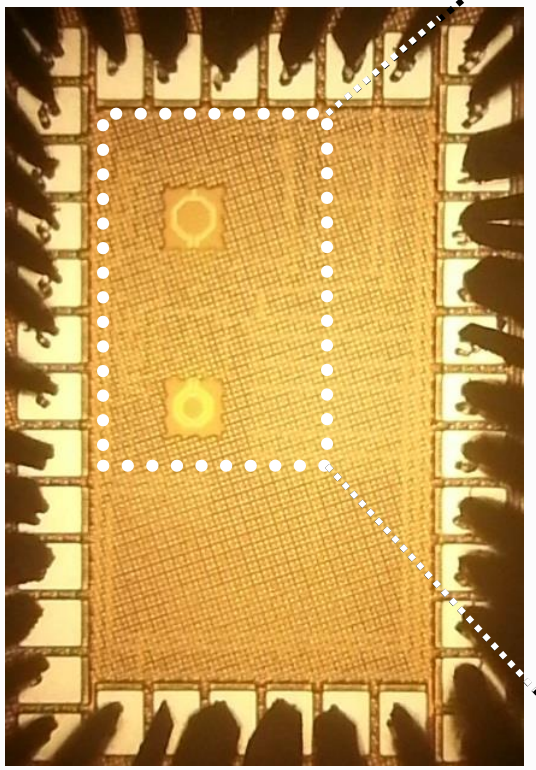
Concept: Introduce two parallel paths with offset control vectors that are combined in the D/VCO; the resulting transfer characteristic is a combination of the offset banks yielding linearization

Varactor Folding and Linearization in the Full PLL Context



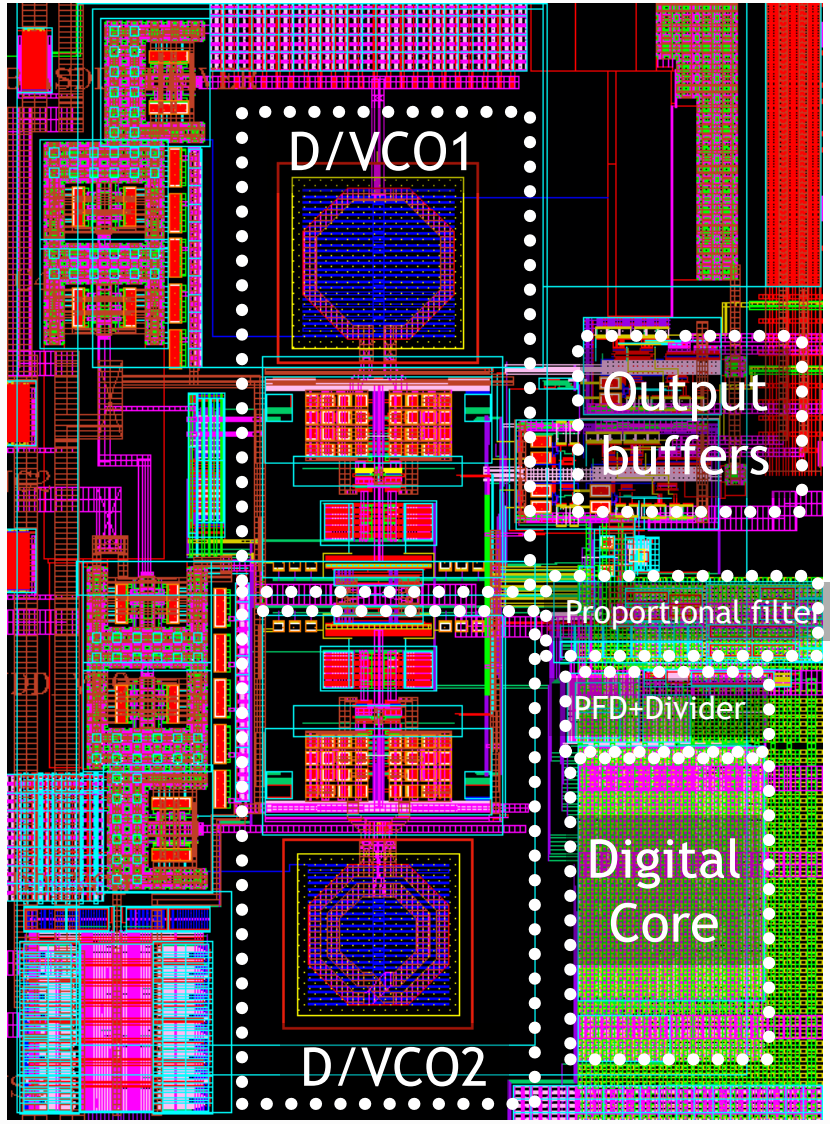
Die Photo with Layout

32nm SOI CMOS Prototype



1300μm

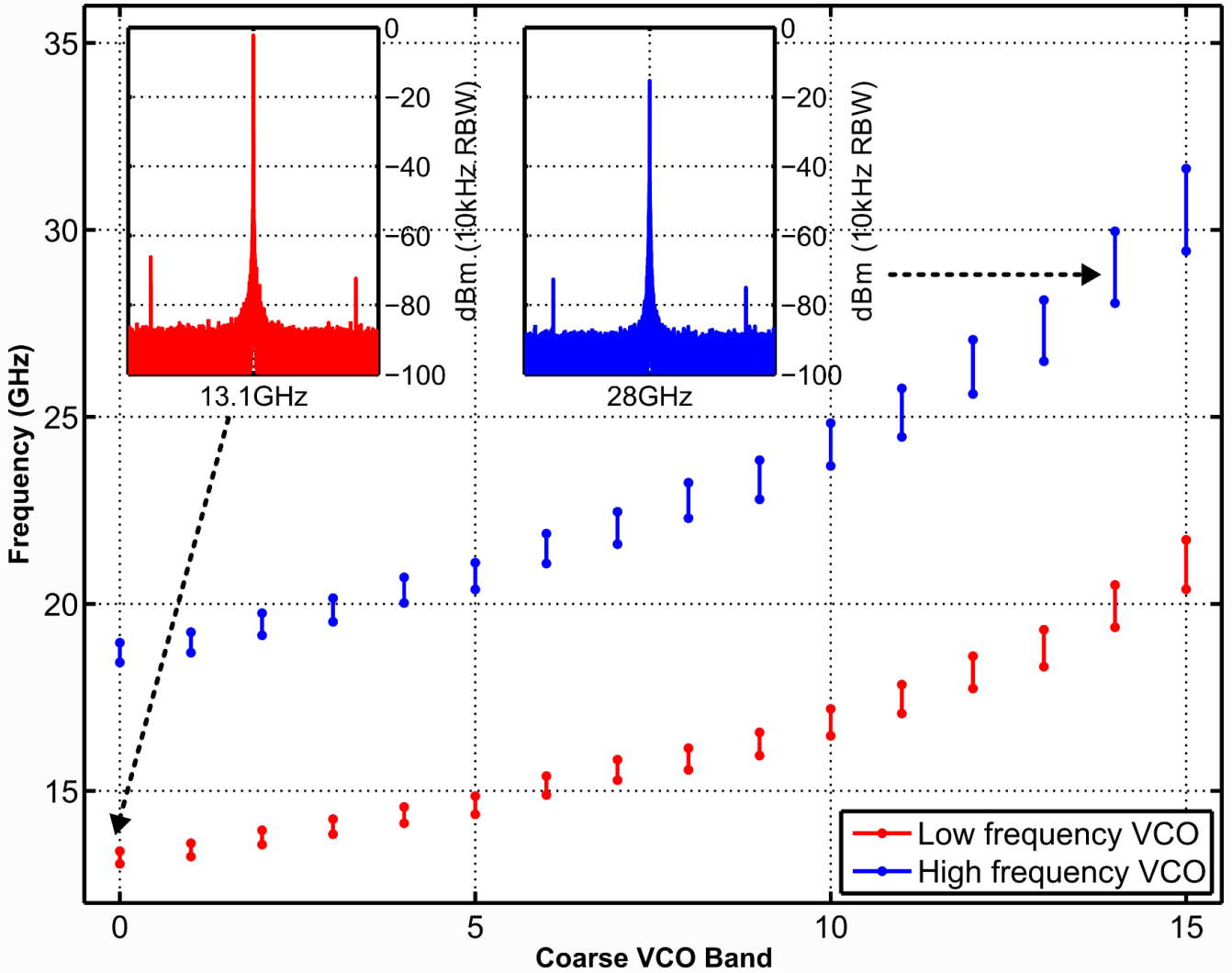
860μm



600μm

400μm

Dual D/VCO Tuning Characteristic

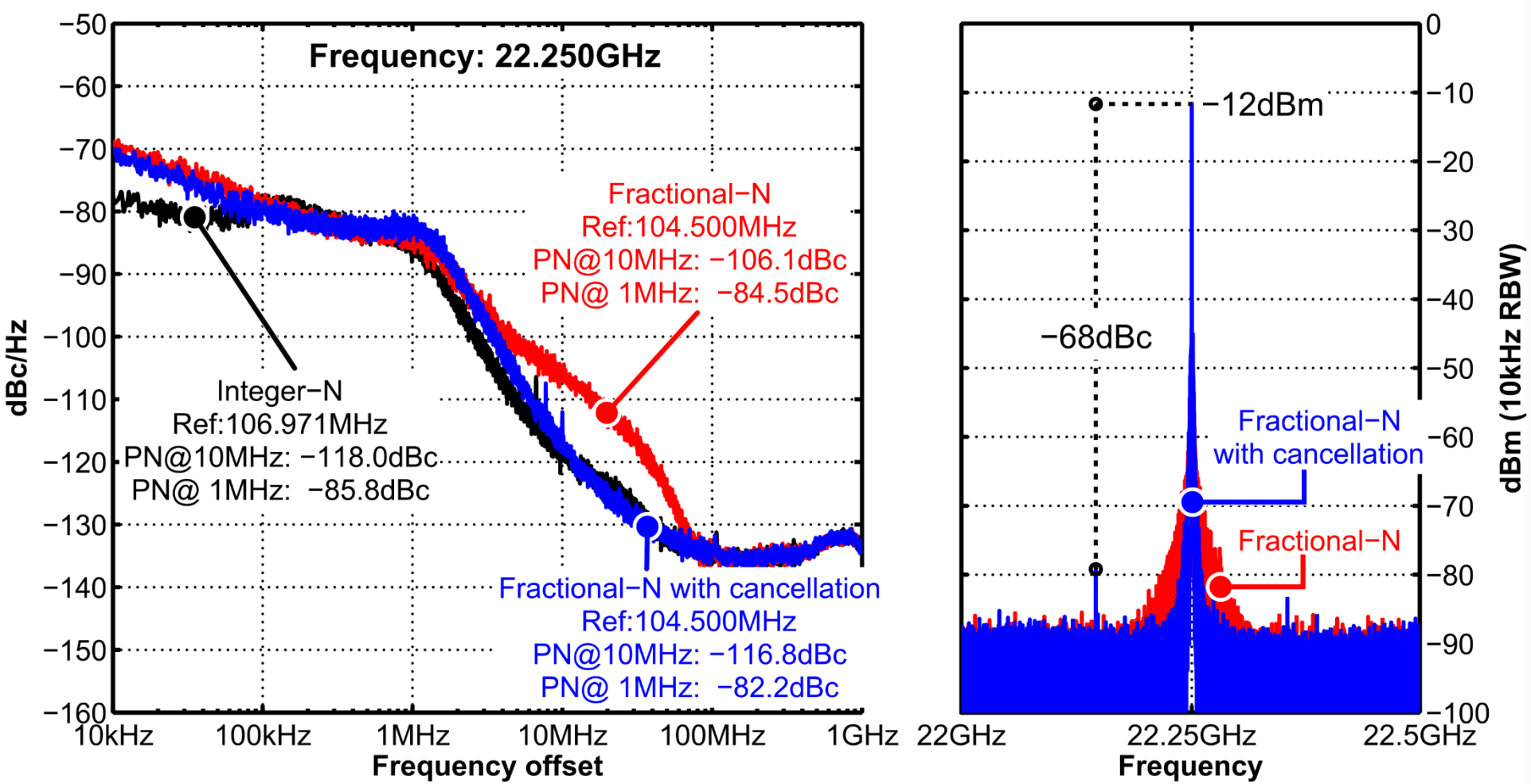


PLL's frequency range is 13.1GHz to 28GHz

M. Ferriss et al, ISSCC15

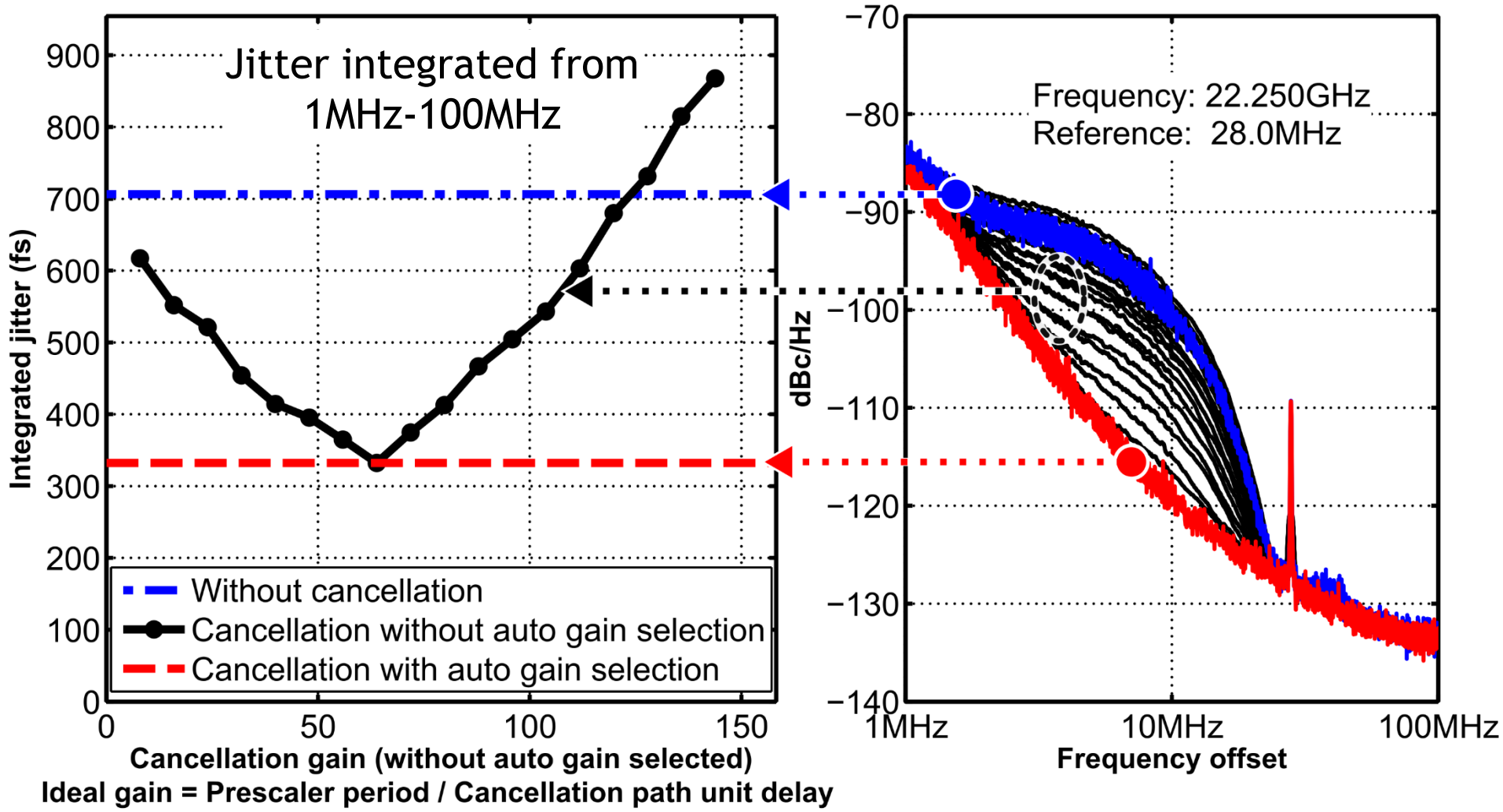
(D/VCO max frequency is 31GHz)

Measured Phase Noise and Output Spectrum



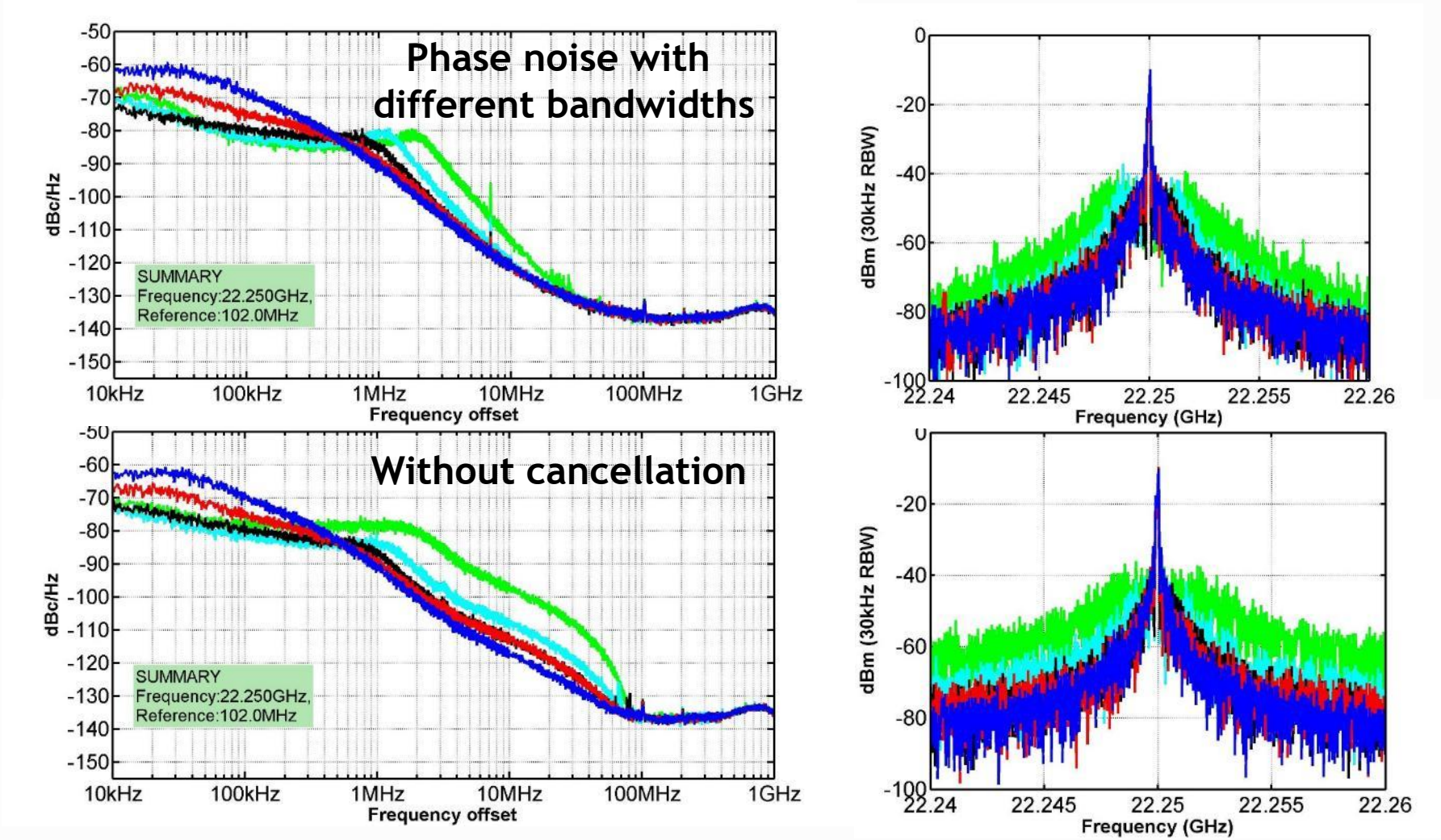
M. Ferriss et al, ISSCC15

Demonstration of DTC Background Cal



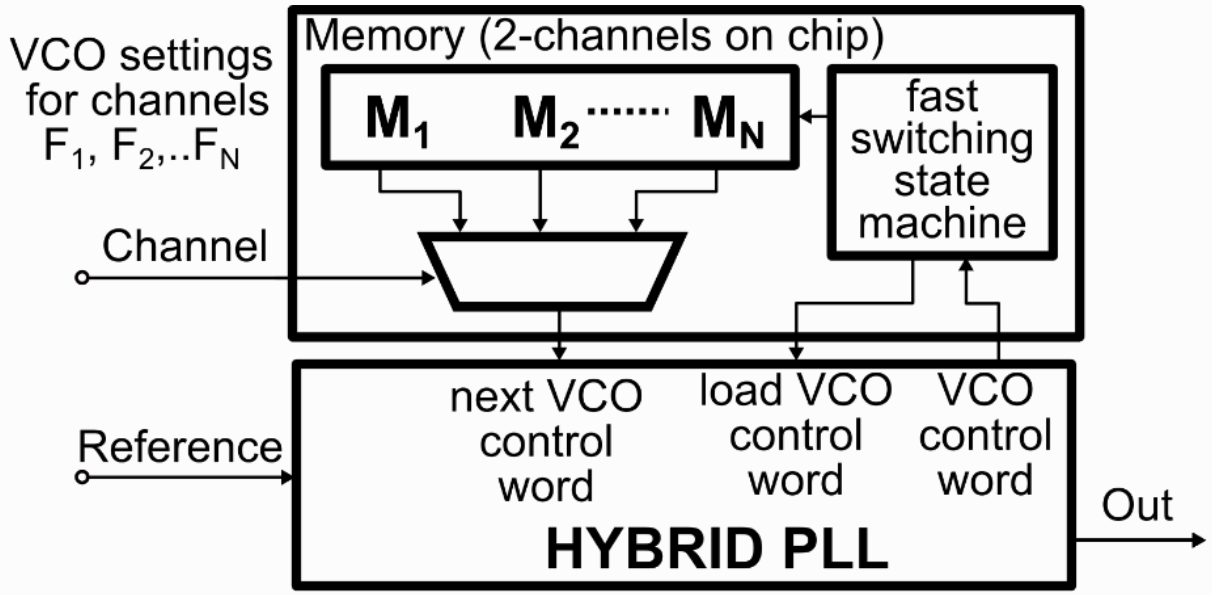
Background calibration engine finds the optimum setting

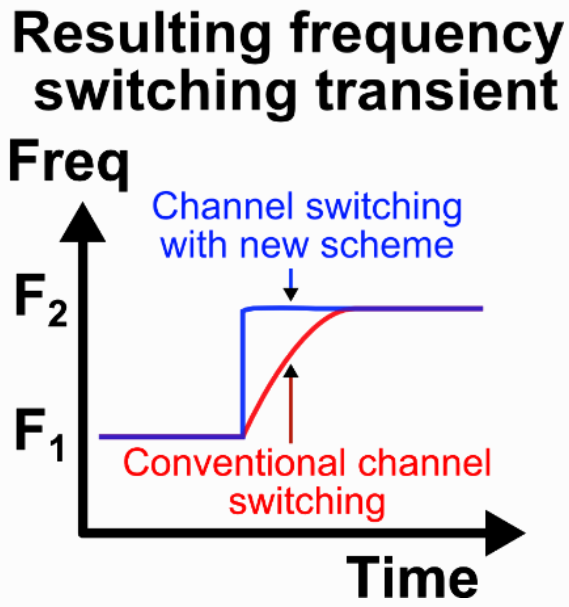
Trading off High Offset (>1MHz) Noise with Low Offset Noise: PLL Enables Flexible Bandwidth Control



Noise cancellation scheme demonstrated independent of bandwidth (*BW range does not affect dynamic range requirements on cancellation path*)

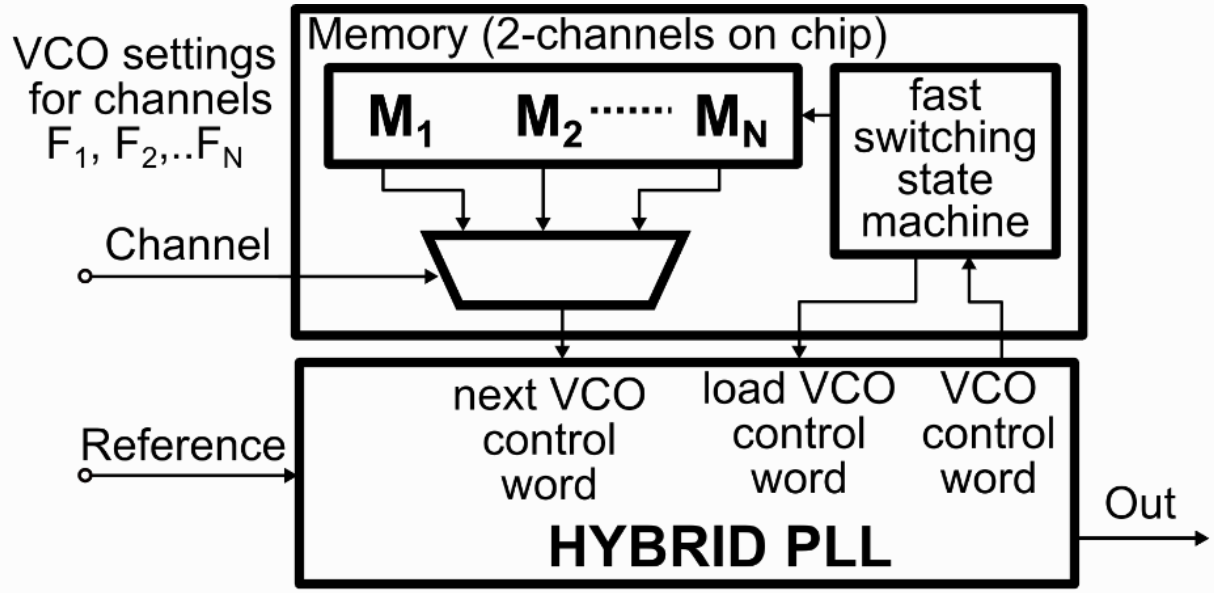
Fast Hopping with Hybrid PLL: Infrastructure

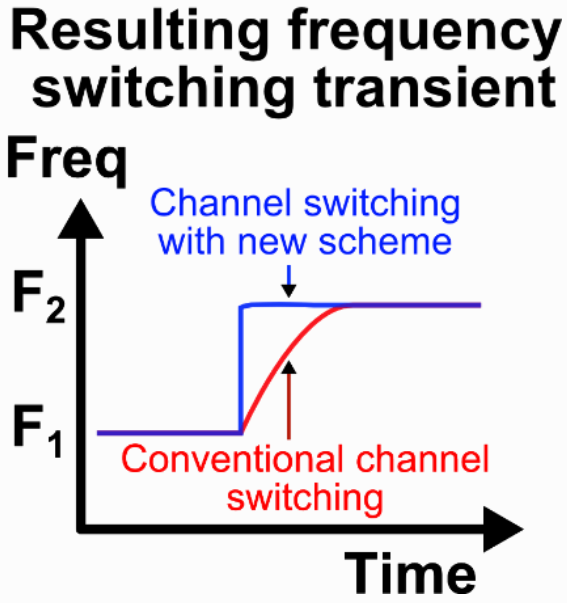




- Memory space to hold digital state information associated with a second frequency
- Fast switching state machine to support transition between active and stored frequency state words
- Within state machine, configurable delays to enable enhanced management of frequency transition

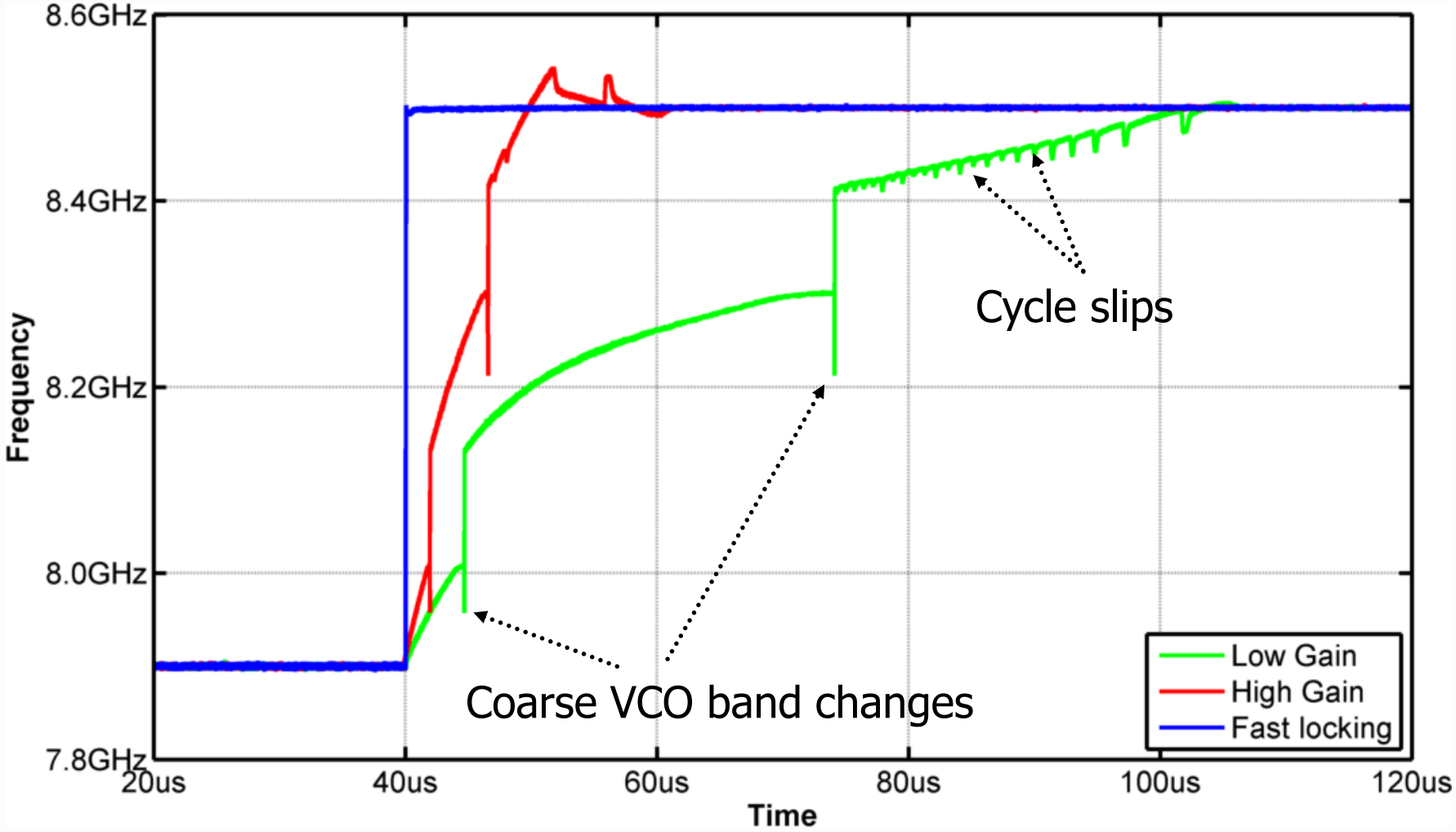
Fast Hopping with Hybrid PLL: Use Model





- Two frequency case (simplest, illustrated on next chart):
  - Initialization: Lock to f1, store PLL state, then lock to f2
  - Hopping: on each transition, load stored state for new frequency and store current state for future use
- General case
  - Initialization: Lock to f1, . . . , fn, store PLL states in external memory using serial interface
  - Hopping: (1) load future target state from serial interface prior to hop request; (2) execute hop as in 2-frequency case; (3) store updated state information for last frequency used in external memory using serial interface

Transient Locking



Measured response to step in division ratio (1) with different integral path gain settings (green, red), and (2) *with direct loading of digital control word as in control scheme described in previous charts* (blue)

Conclusion: Frac-N, Fast-Hopping Hybrid PLL Implementation

Key results

- A 13.1-28 GHz, frac-N, low noise hybrid PLL drawing 31mW from 1V demonstrated in 32nm CMOS
- Design features analog proportional path, and (mostly) digital $\Delta\Sigma$ cancellation and integral paths
- Supports reference frequencies from 15-400MHz and includes infrastructure for fast hopping

Challenges and opportunities

- Further improve integral path
- Can we do something about banded nature of design?

Outline

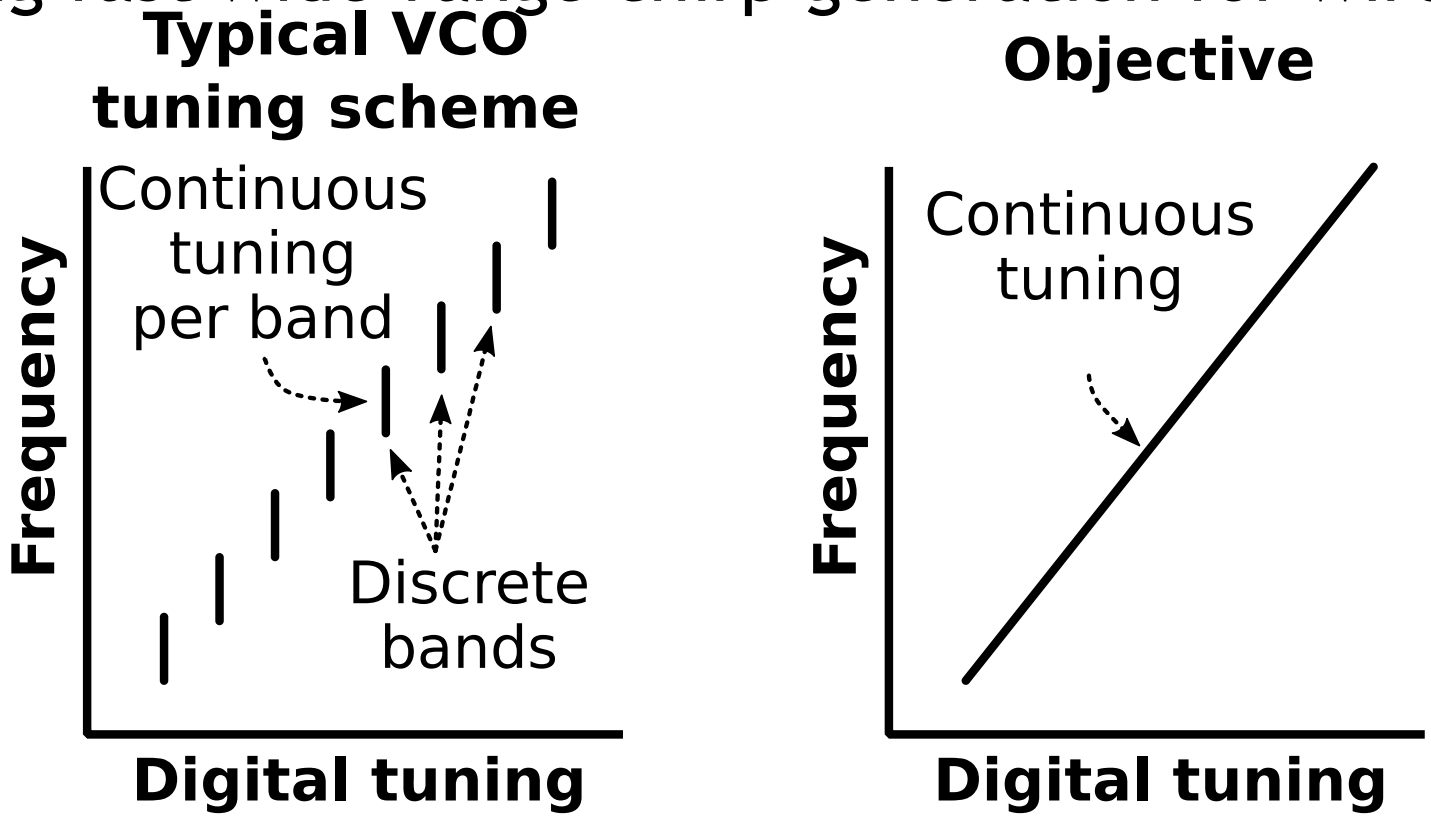
- Introduction and motivation: hybrid architectures
- Initial implementation: proof-of-concept
- Flexible synthesizer: frac-N w/ noise cancellation
- **Flexible synthesizer: coarse band elimination**
- Flexible synthesizer: flicker noise suppression exploration
- Summary/conclusion

Fractional-N Hybrid PLL with Coarse Band Elimination

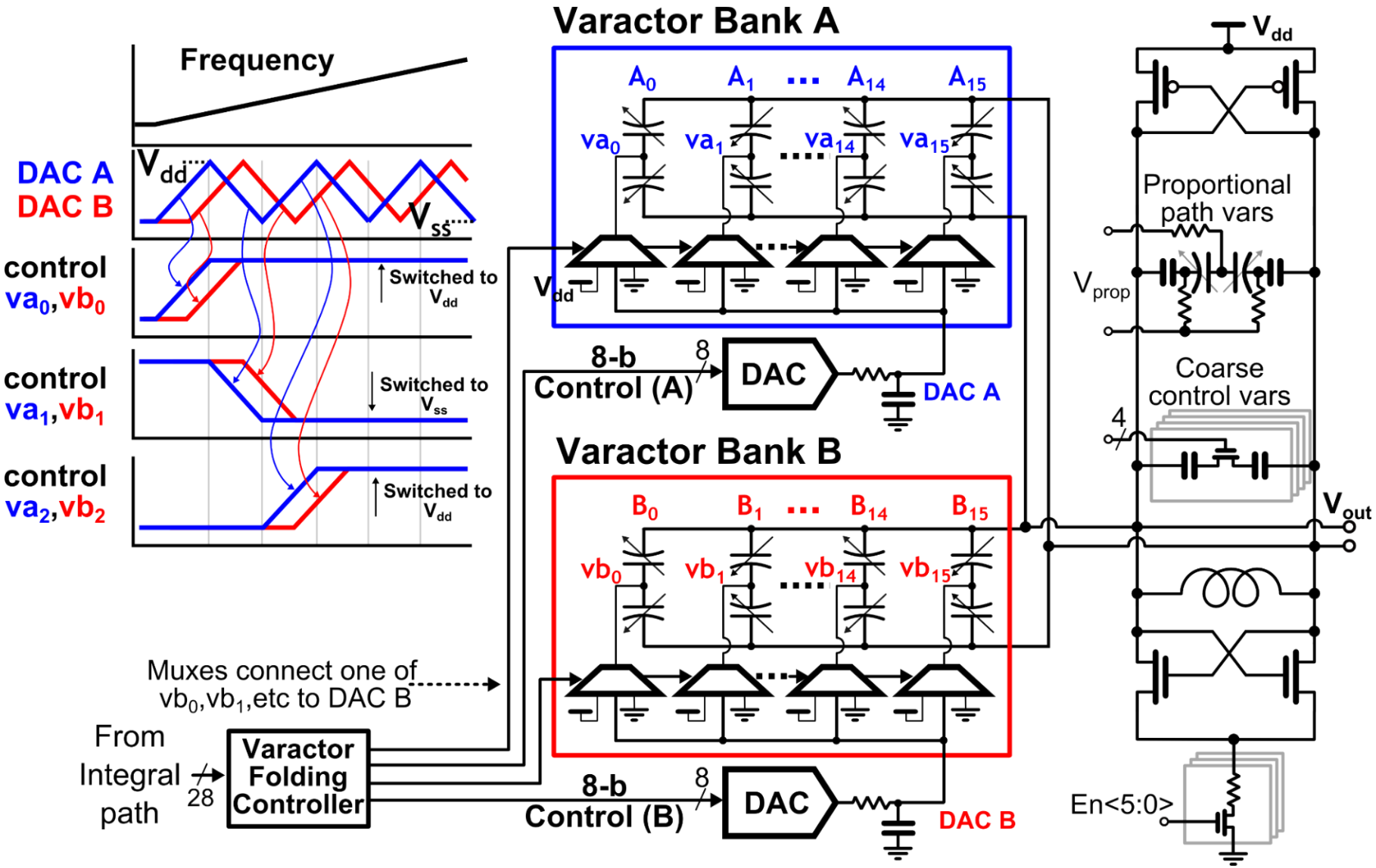
- Objective: retain benefits and capabilities of hybrid frac-N design, and remove need for VCO frequency banding without sacrificing noise performance
- Approach
  - Extend varactor folding concept to include coarse band capacitance
  - Enhance integral path design to improve performance
- Key challenges
  - Switched capacitor element choice
  - Introduction of enhanced control scheme

Motivation

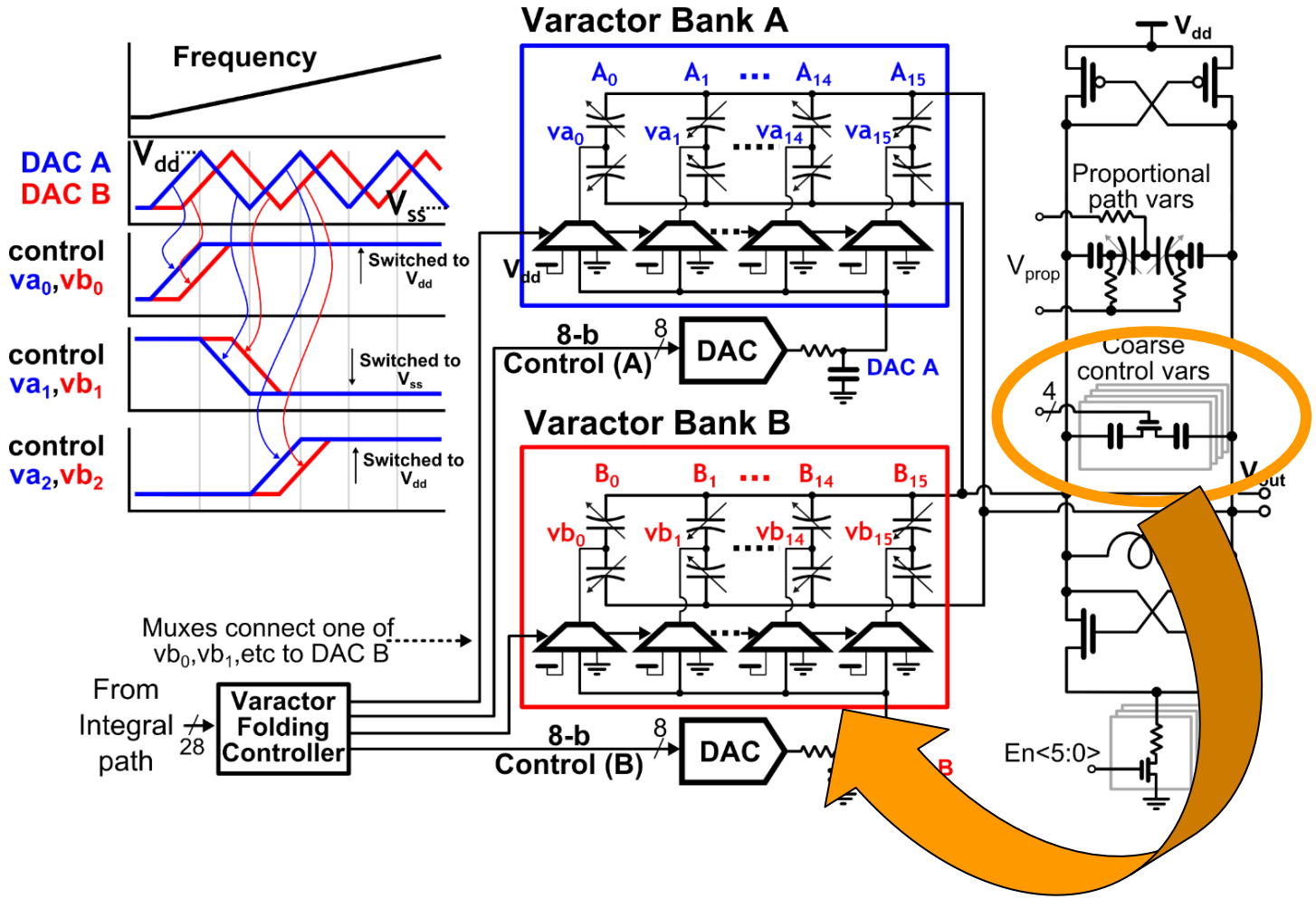
- Objective: Remove coarse bands of CMOS oscillators
- Impact: extends PLL lock range to entire VCO tuning range, allowing, for example, improvement in lock maintenance in wireline applications and enabling fast wide-range chirp generation for wireless/radar



Varactor Folding in the Full PLL Context: Reminder



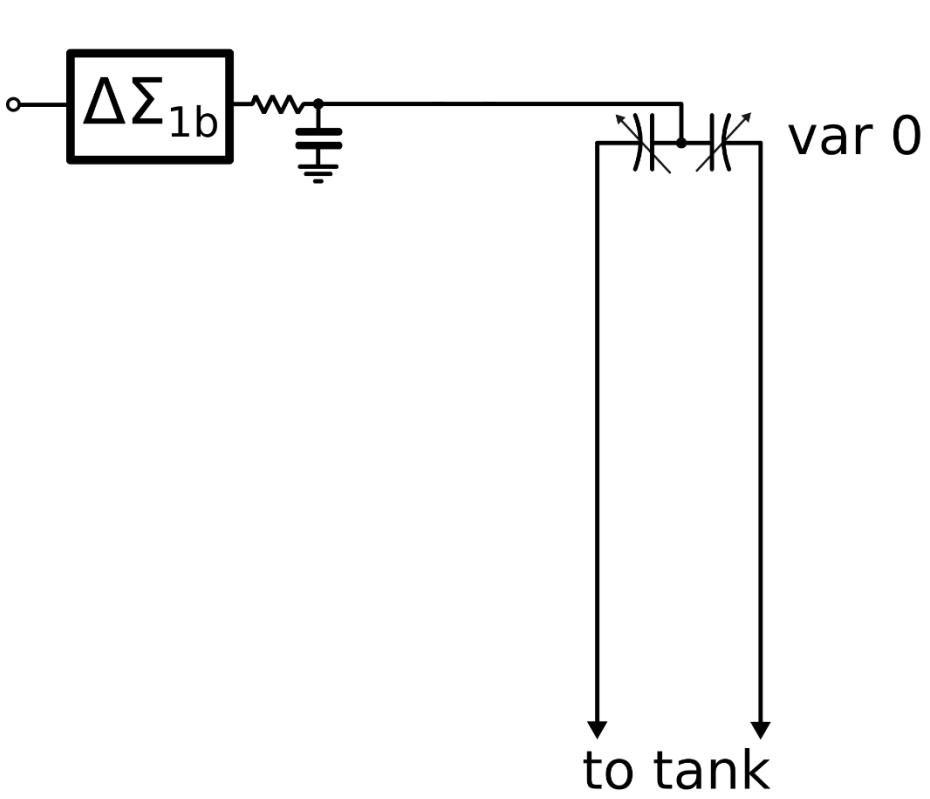
Coarse Band Elimination in VCO Design Context

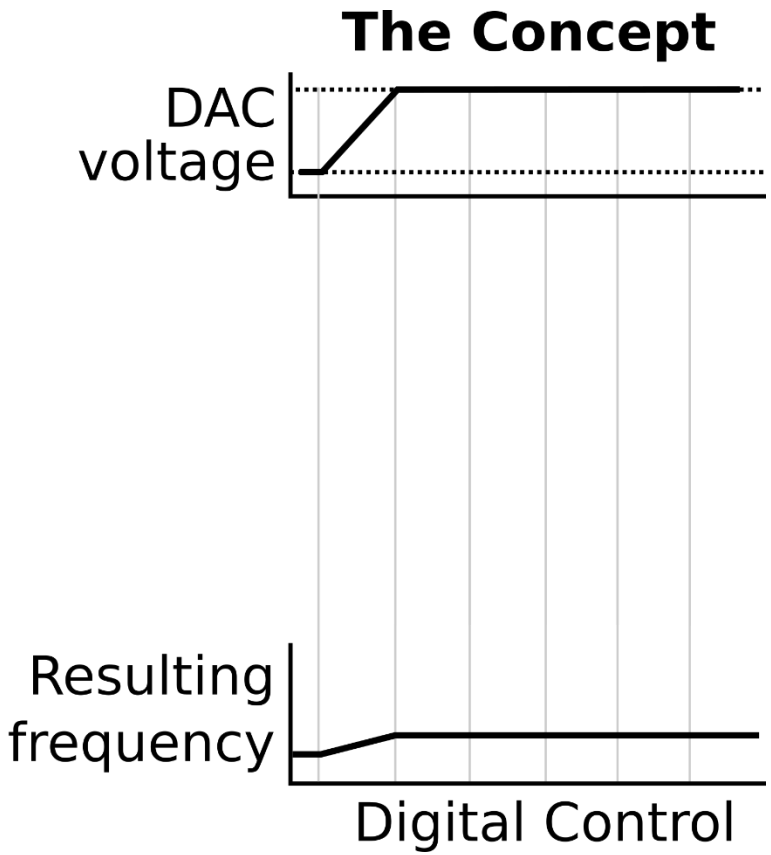


Key goal: move all coarse varactor capacitance into integral path varactor folding infrastructure

M. Ferriss et al, ISSCC16

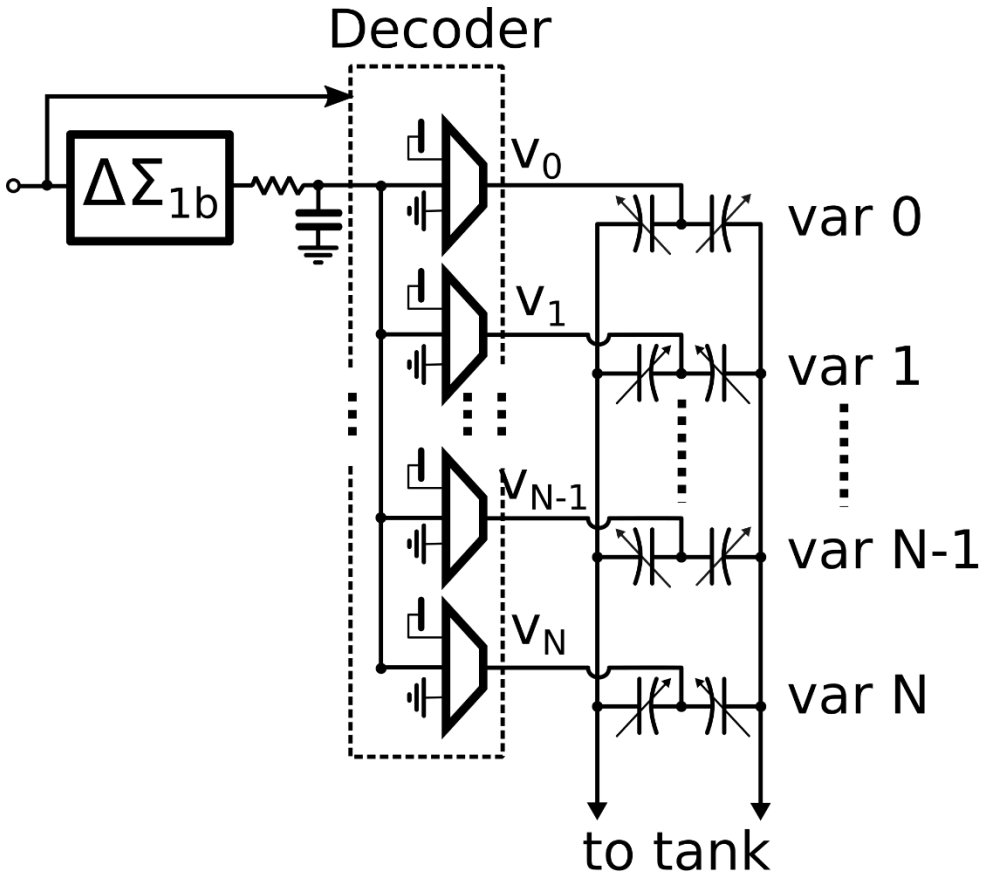
Digital control of a varactor

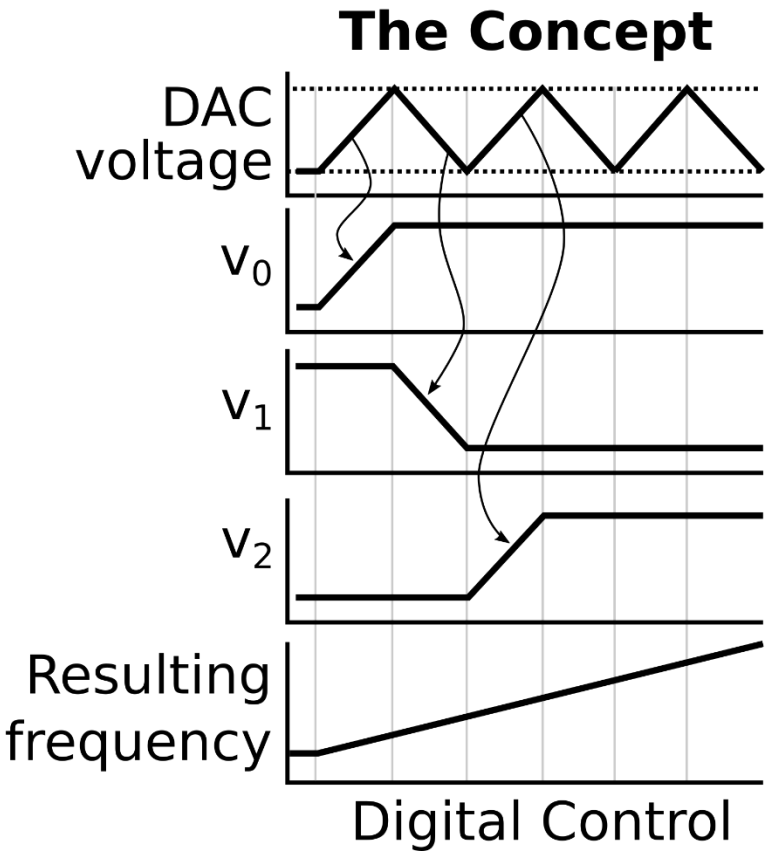




Trade off between ΣΔ noise and gain/tuning range

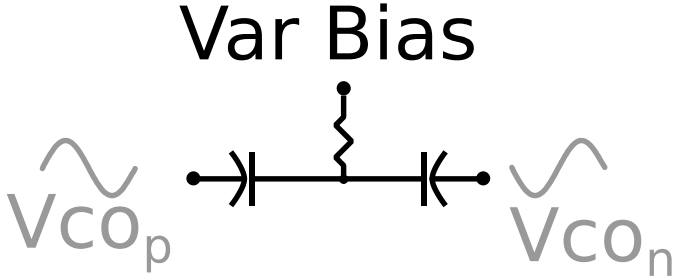
Extending the range: varactor folding (review)



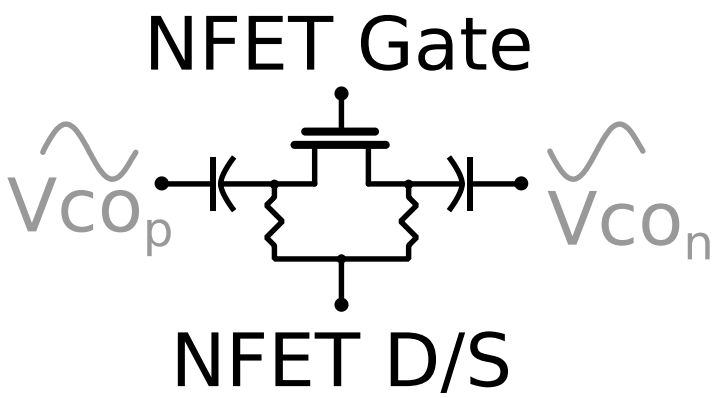


Comparing typical tuning mechanisms

Continuous tuning:
UGN varactor

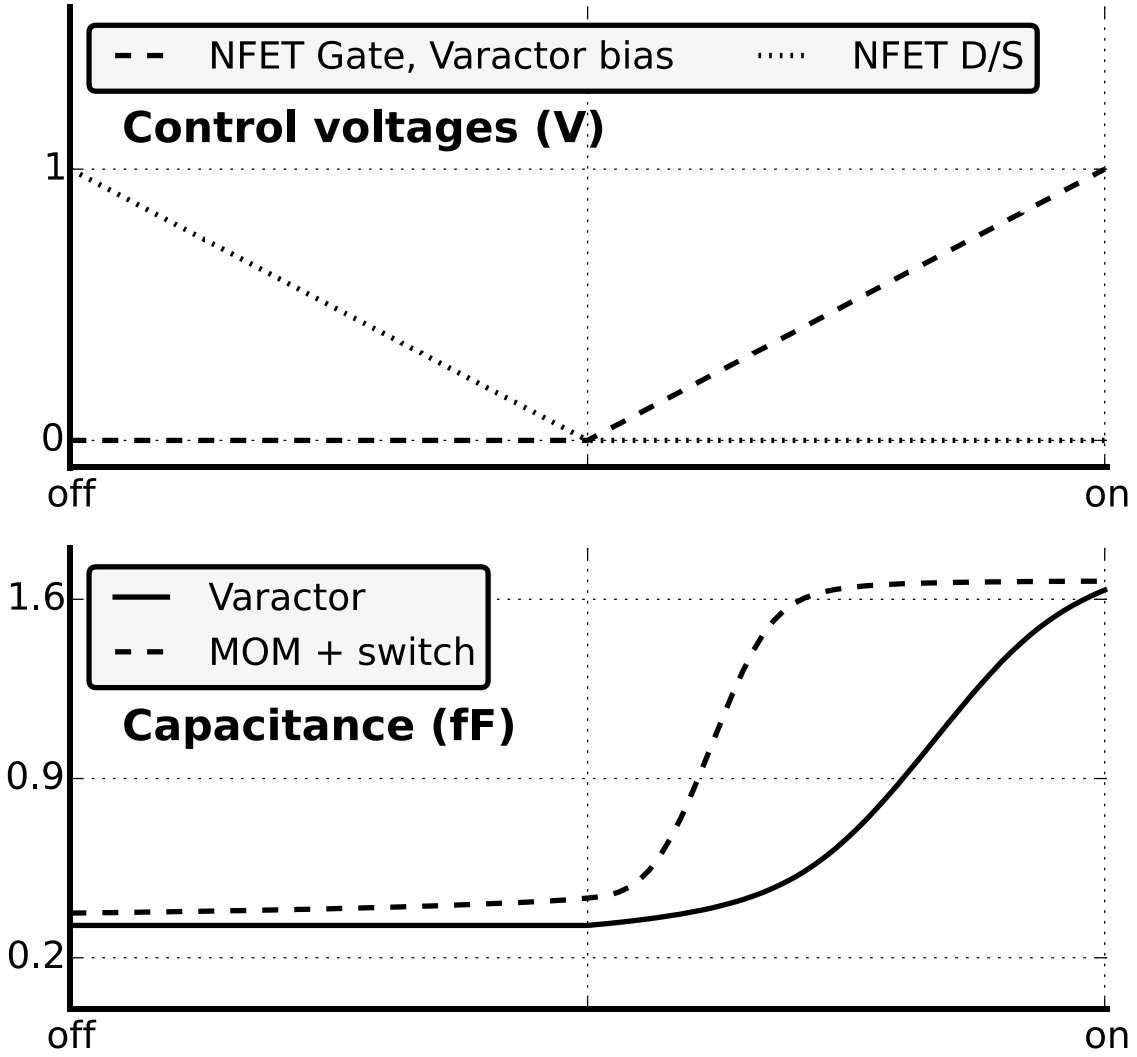


Discrete tuning:
MOM + Switch



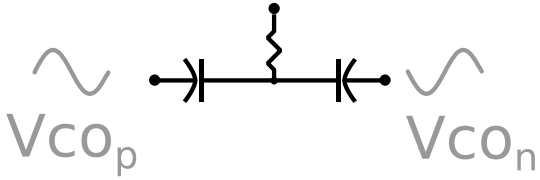
Can we use MOM+switch for continuous tuning?

Varactors vs MOM+switch (Cap)



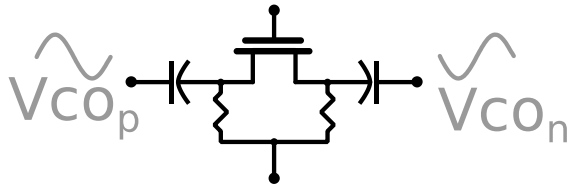
UGN varactor

Var Bias



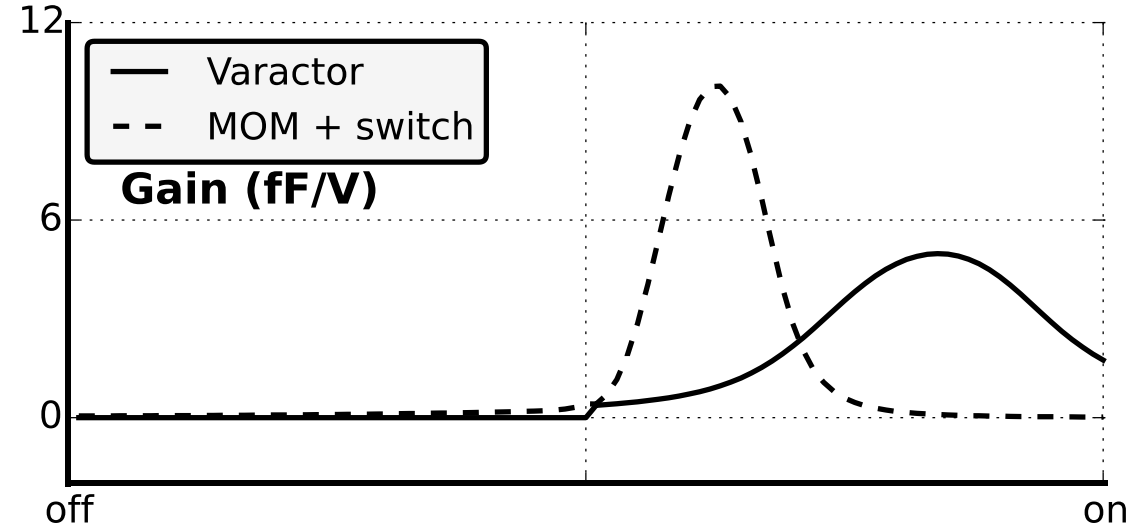
MOM + Switch

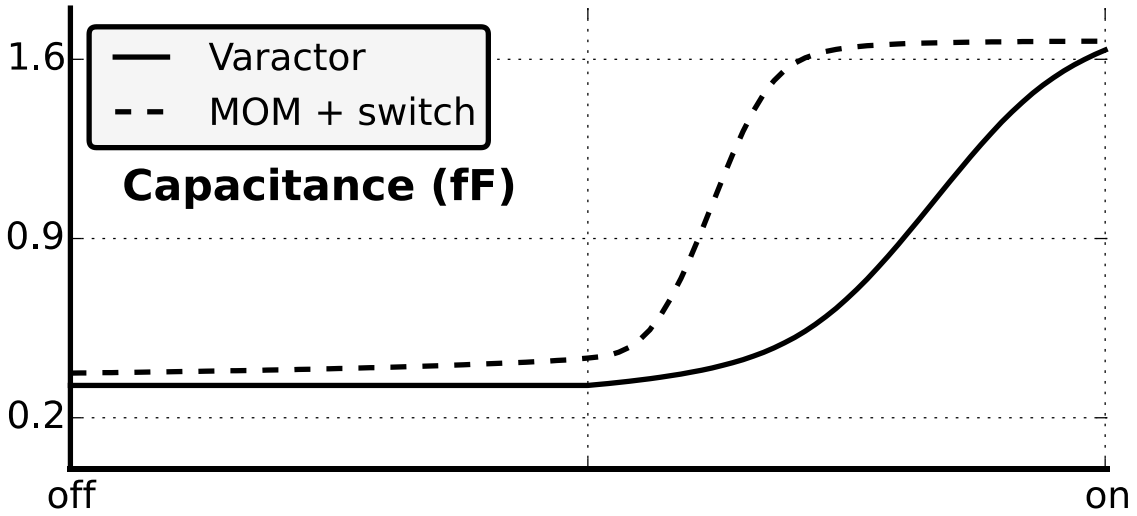
NFET Gate



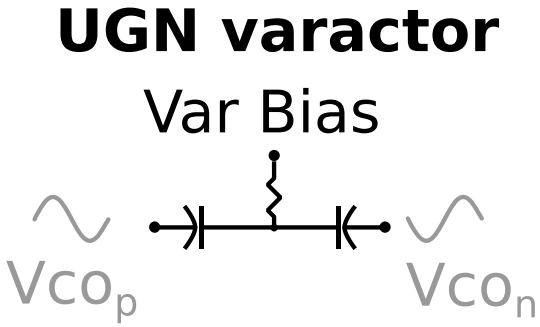
NFET D/S

Varactors vs MOM+switch (Gain)

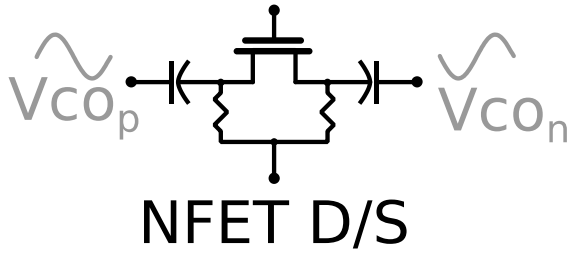




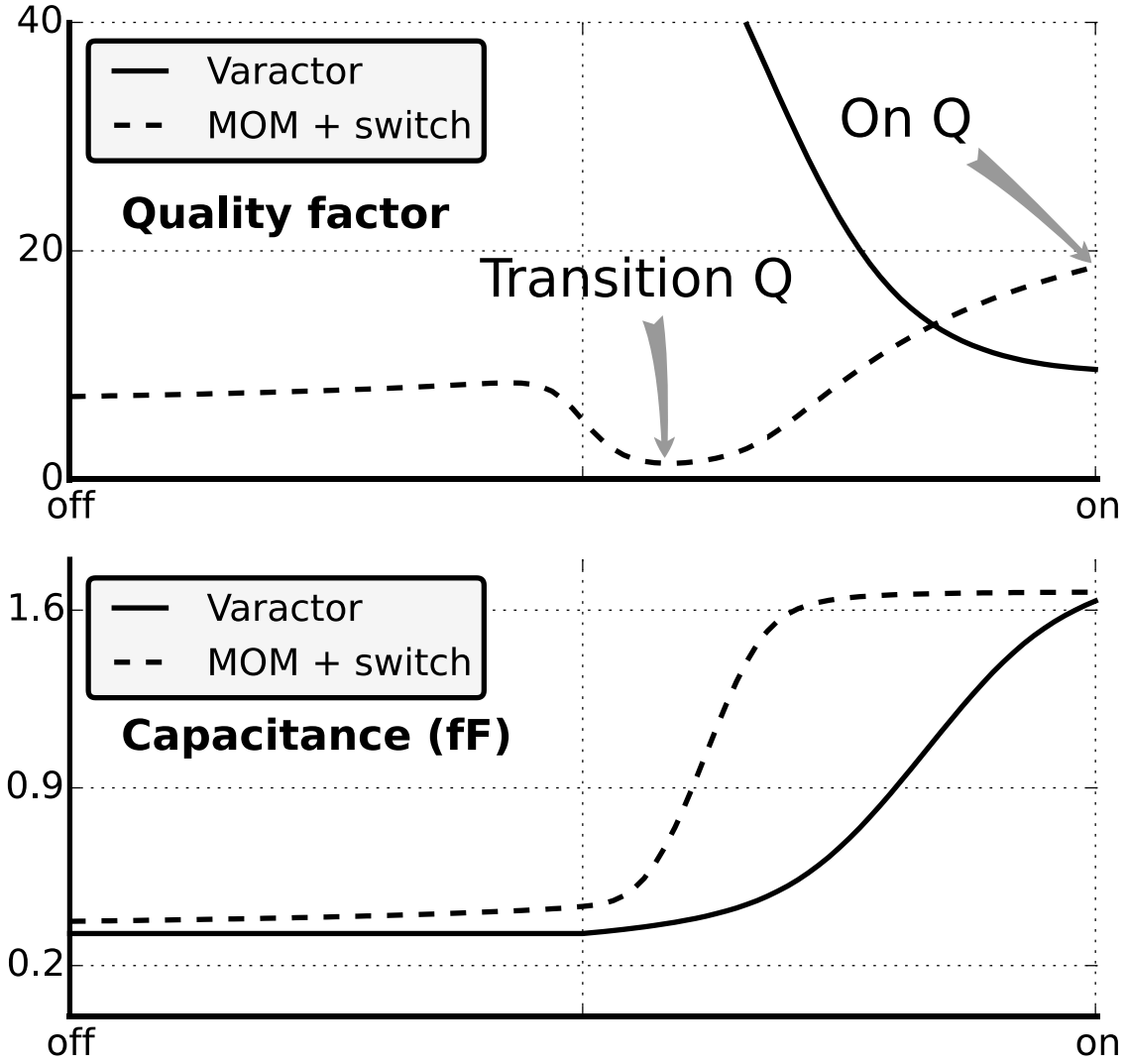
UGN varactor



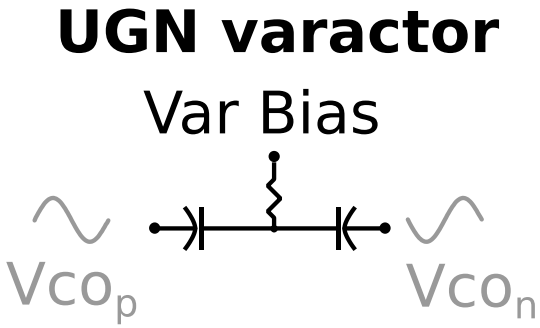
MOM + Switch



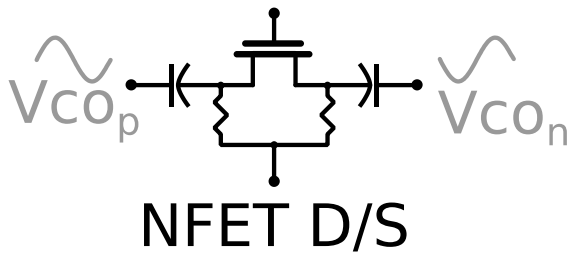
Varactors vs MOM+switch (Q)



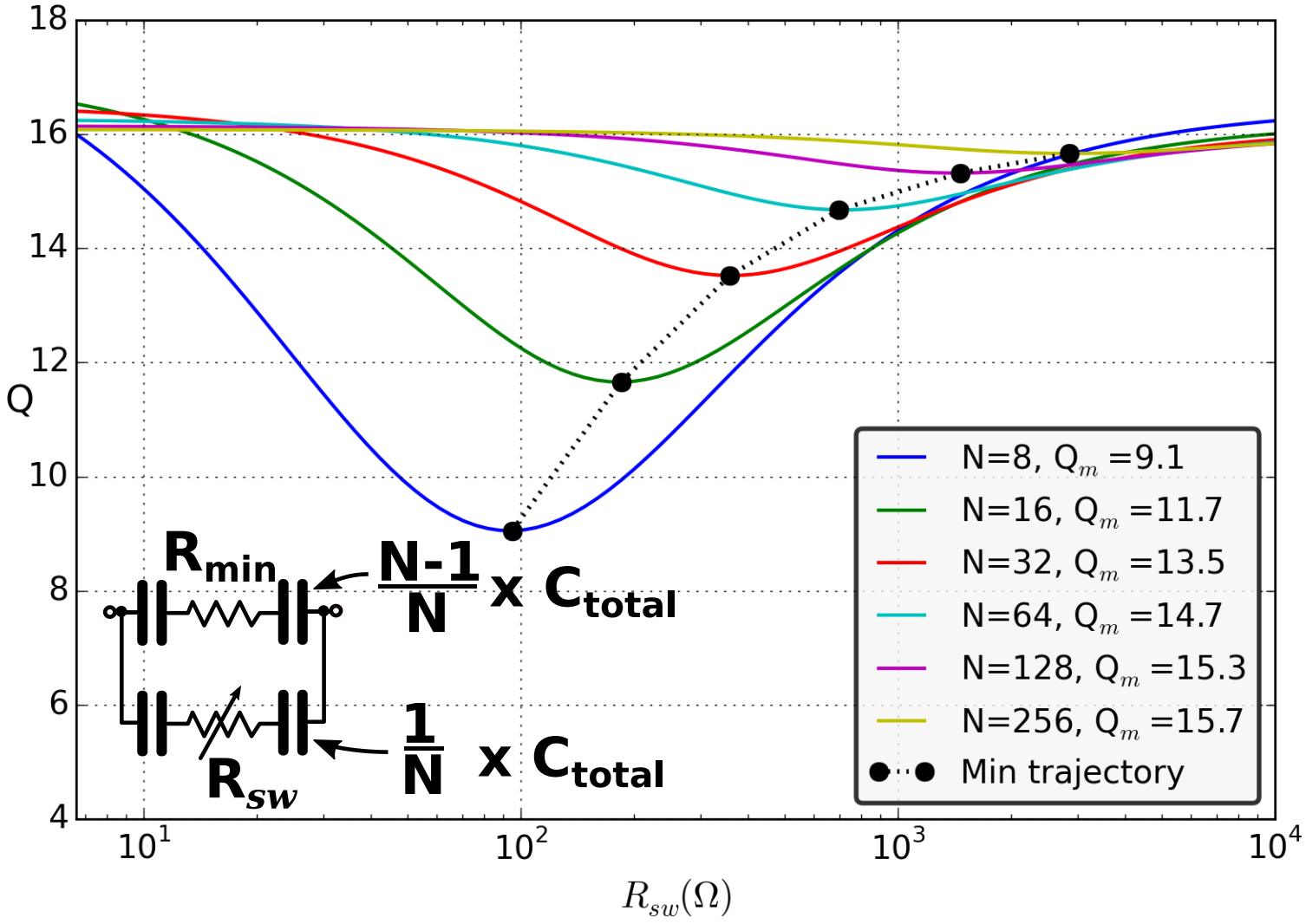
UGN varactor



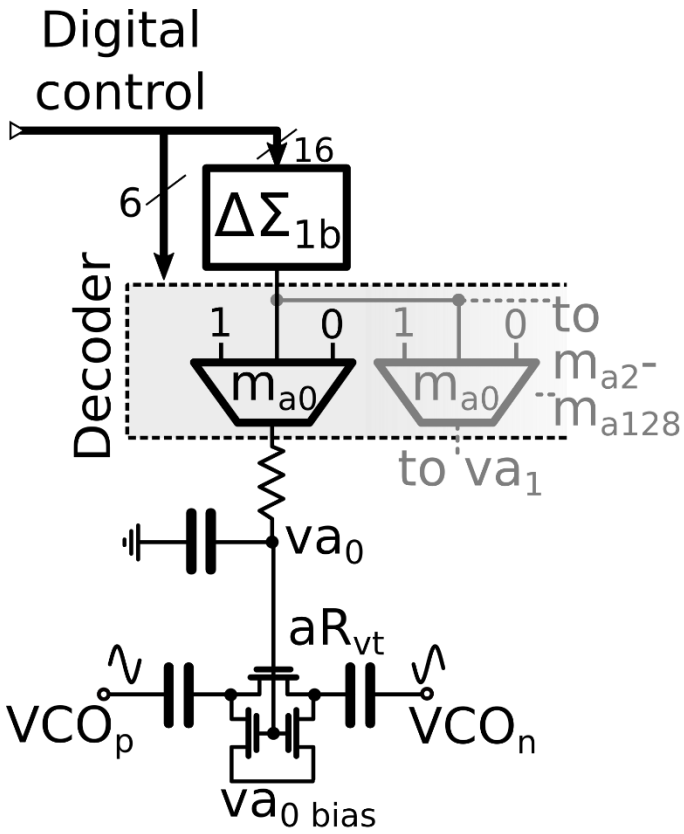
MOM + Switch

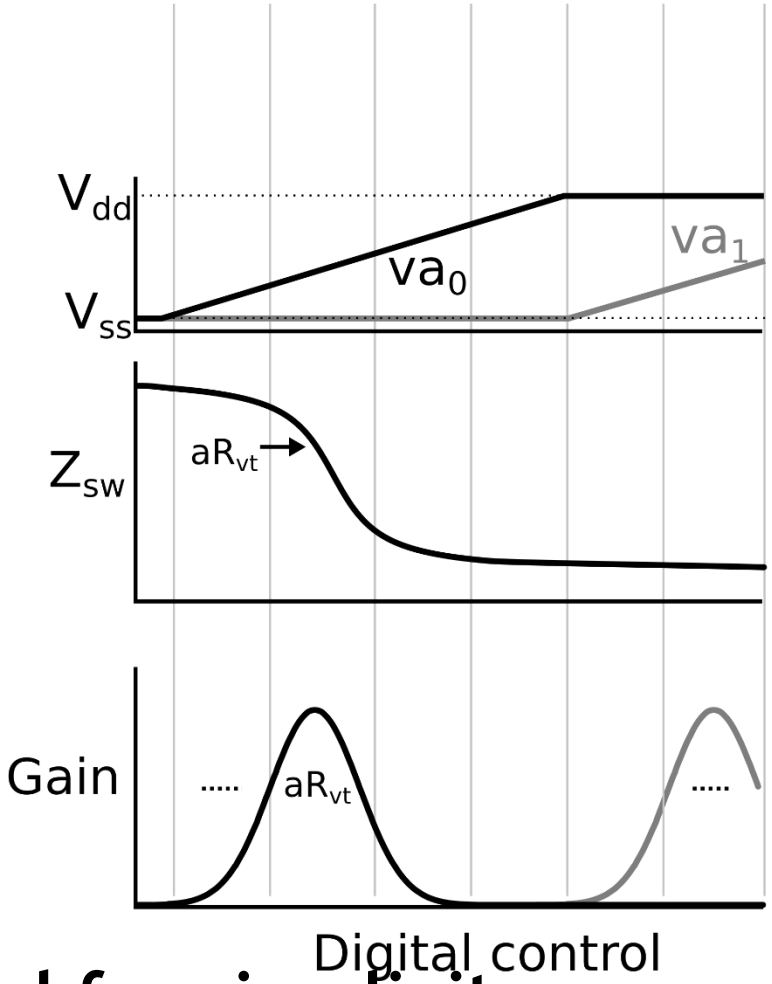


Q degradation



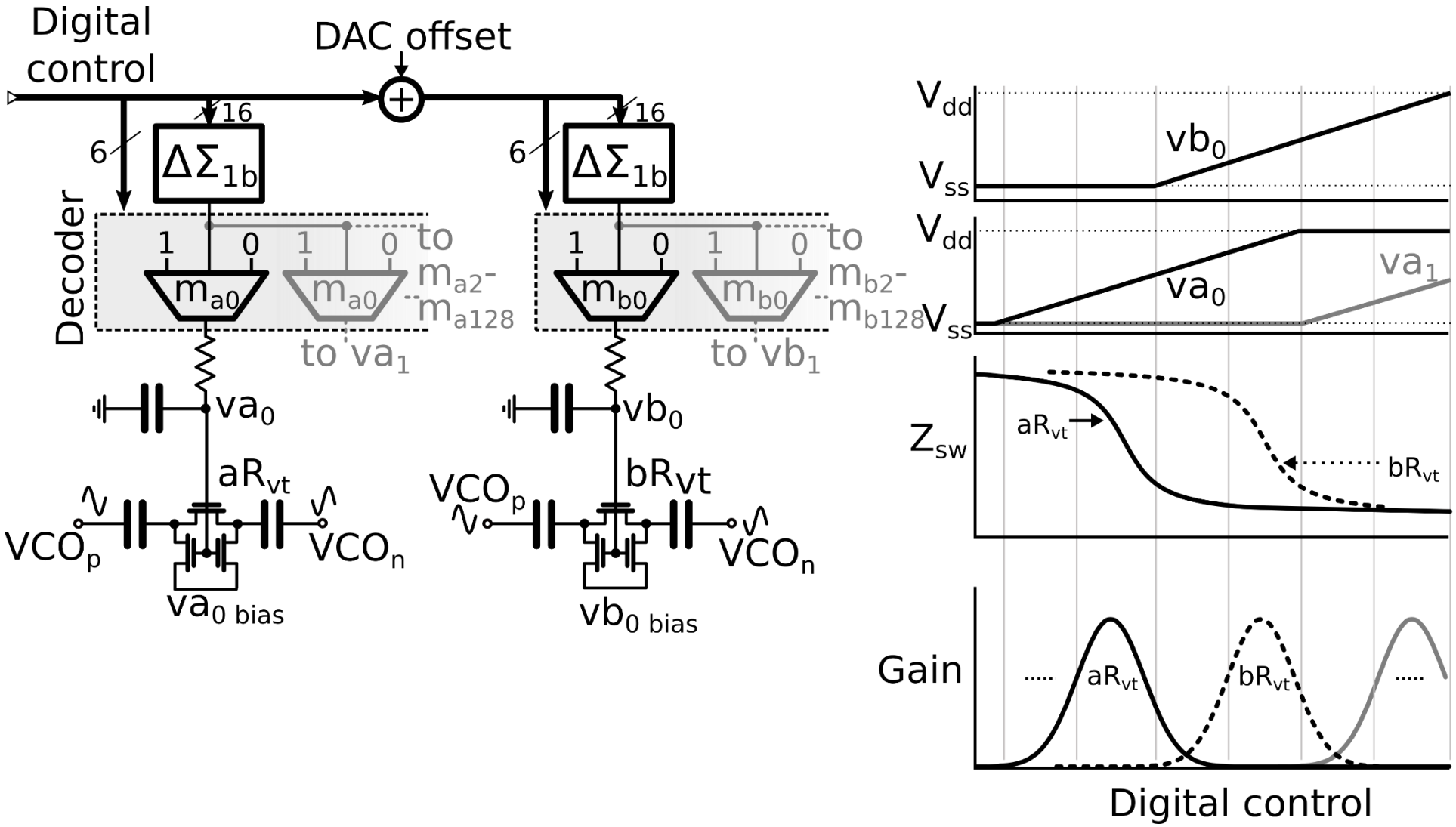
One band





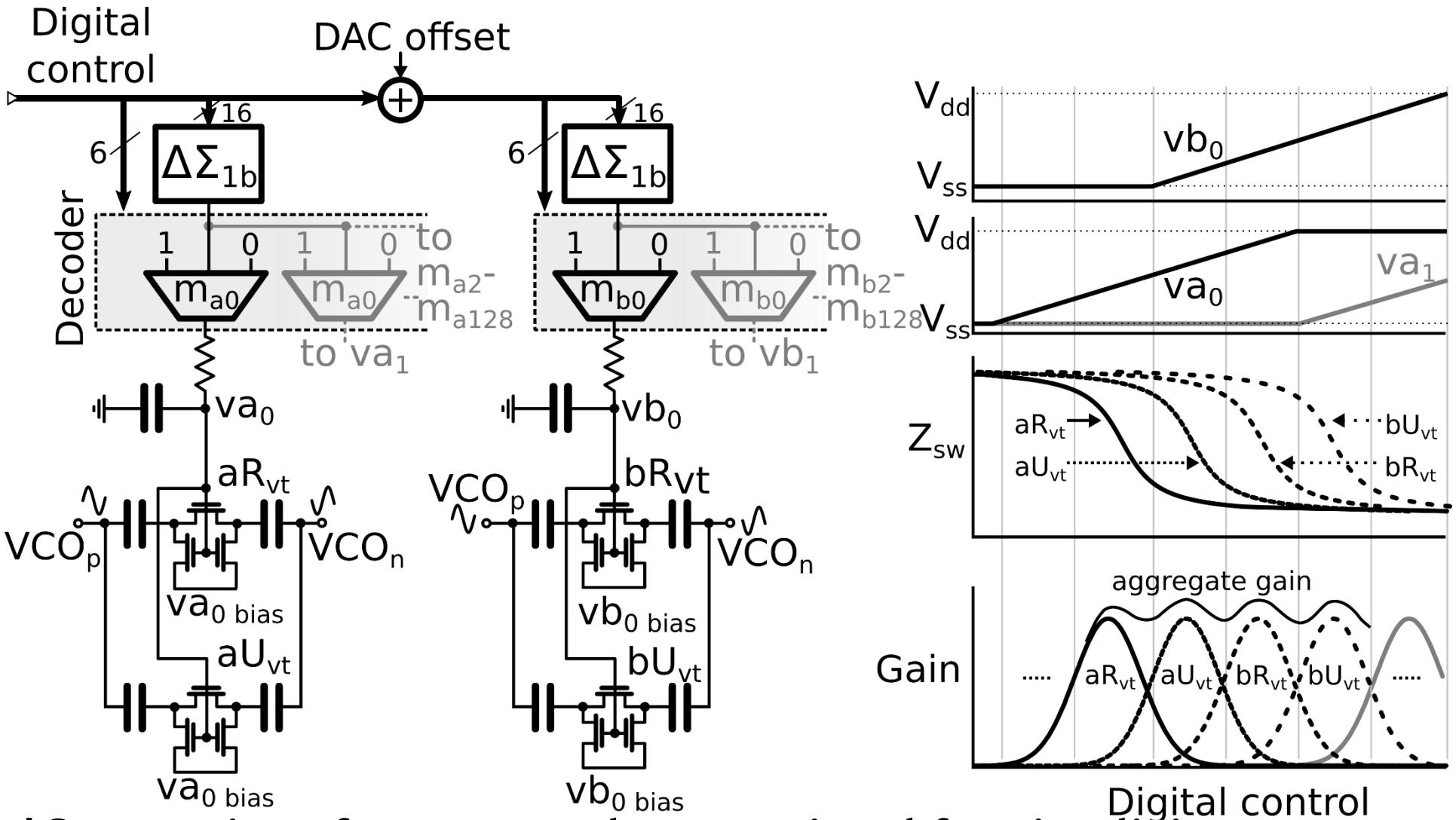
***Connections for $va_{0\ bias}$ omitted for simplicity**

Two bands with offset



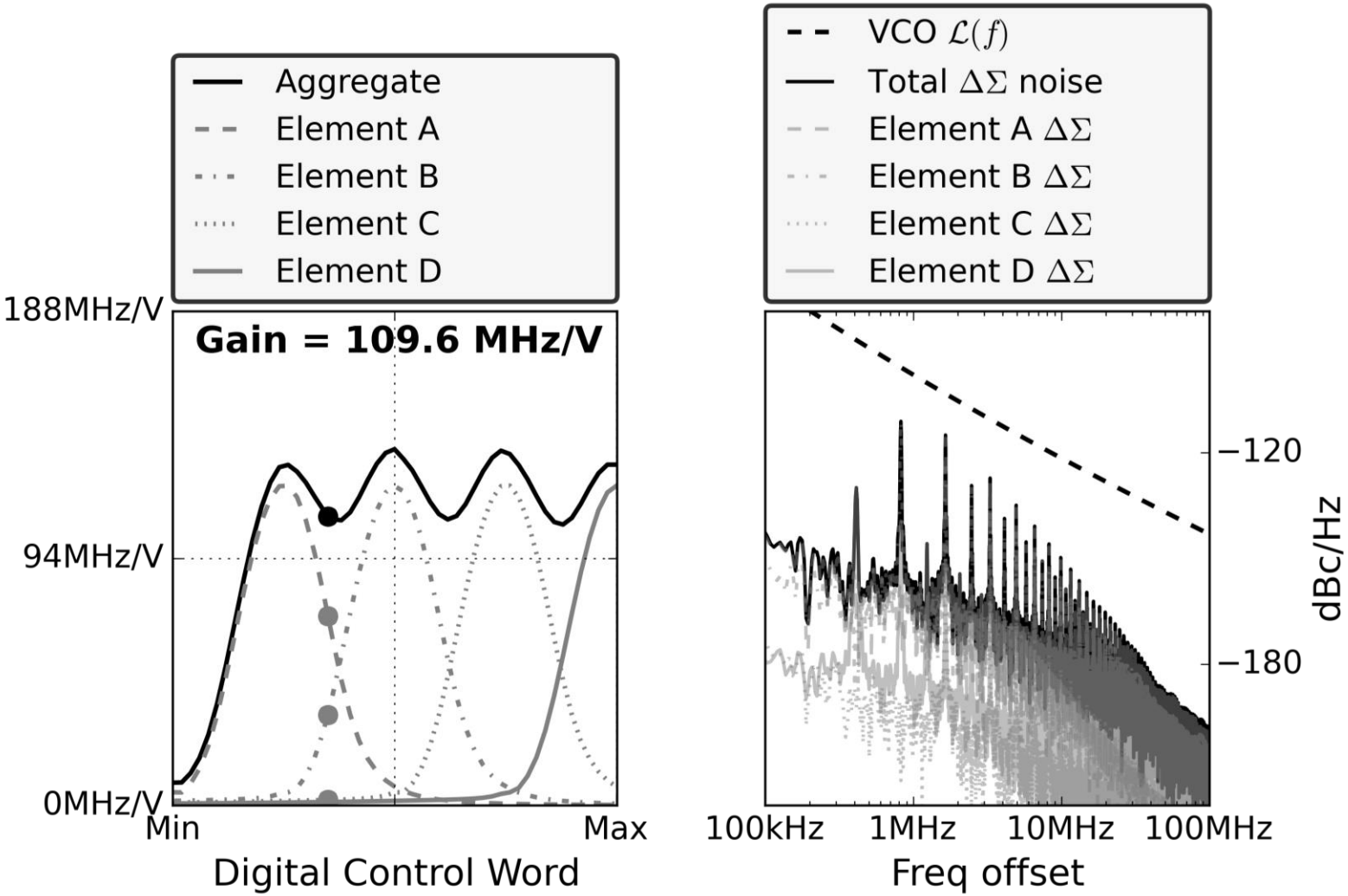
*Connections for $va_{0\ bias}$, $vb_{0\ bias}$ omitted for simplicity

Two bands and two thresholds

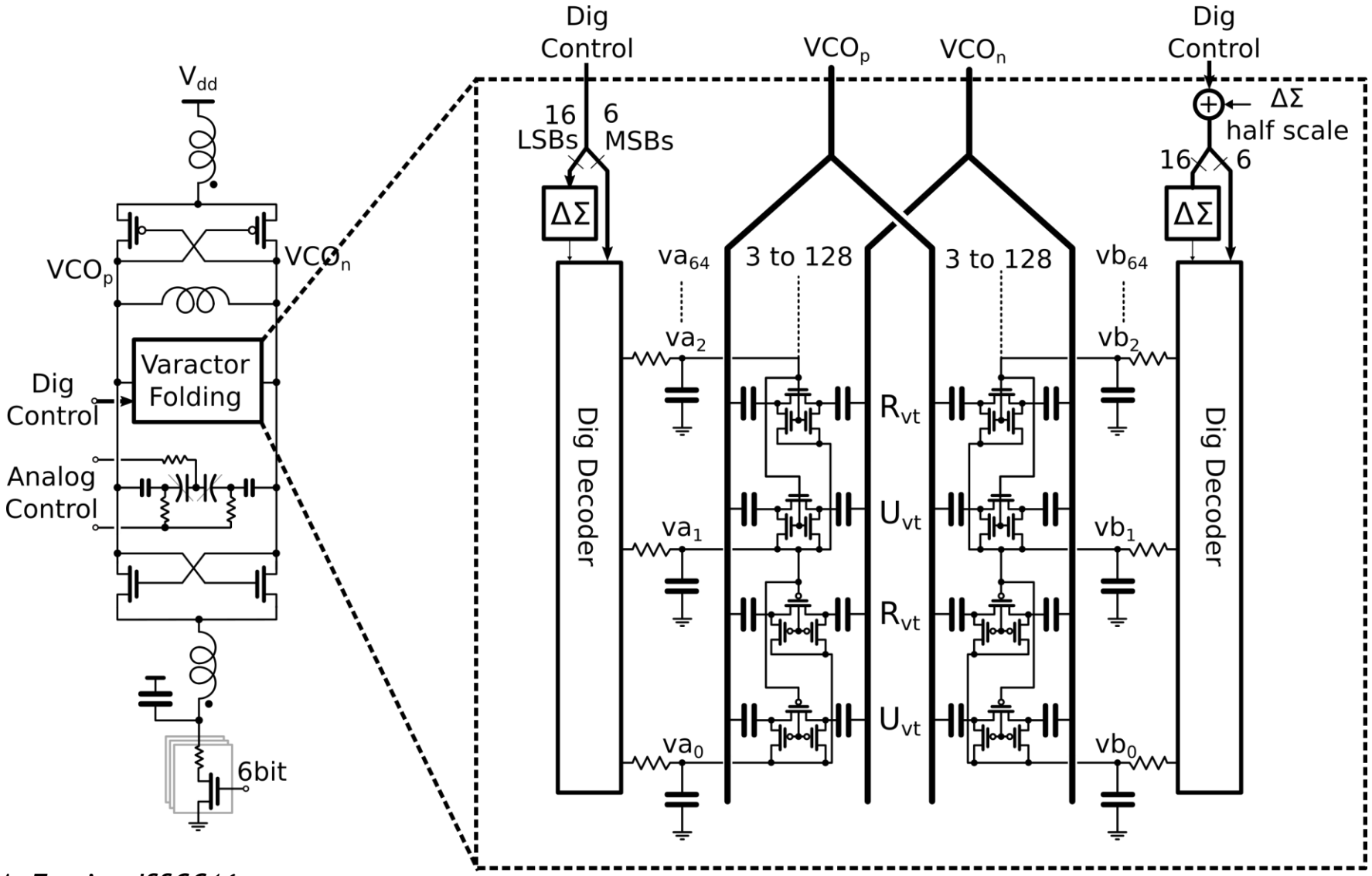


***Connections for $va_{0\ bias}$, $vb_{0\ bias}$ omitted for simplicity**

Varactor gain versus frequency

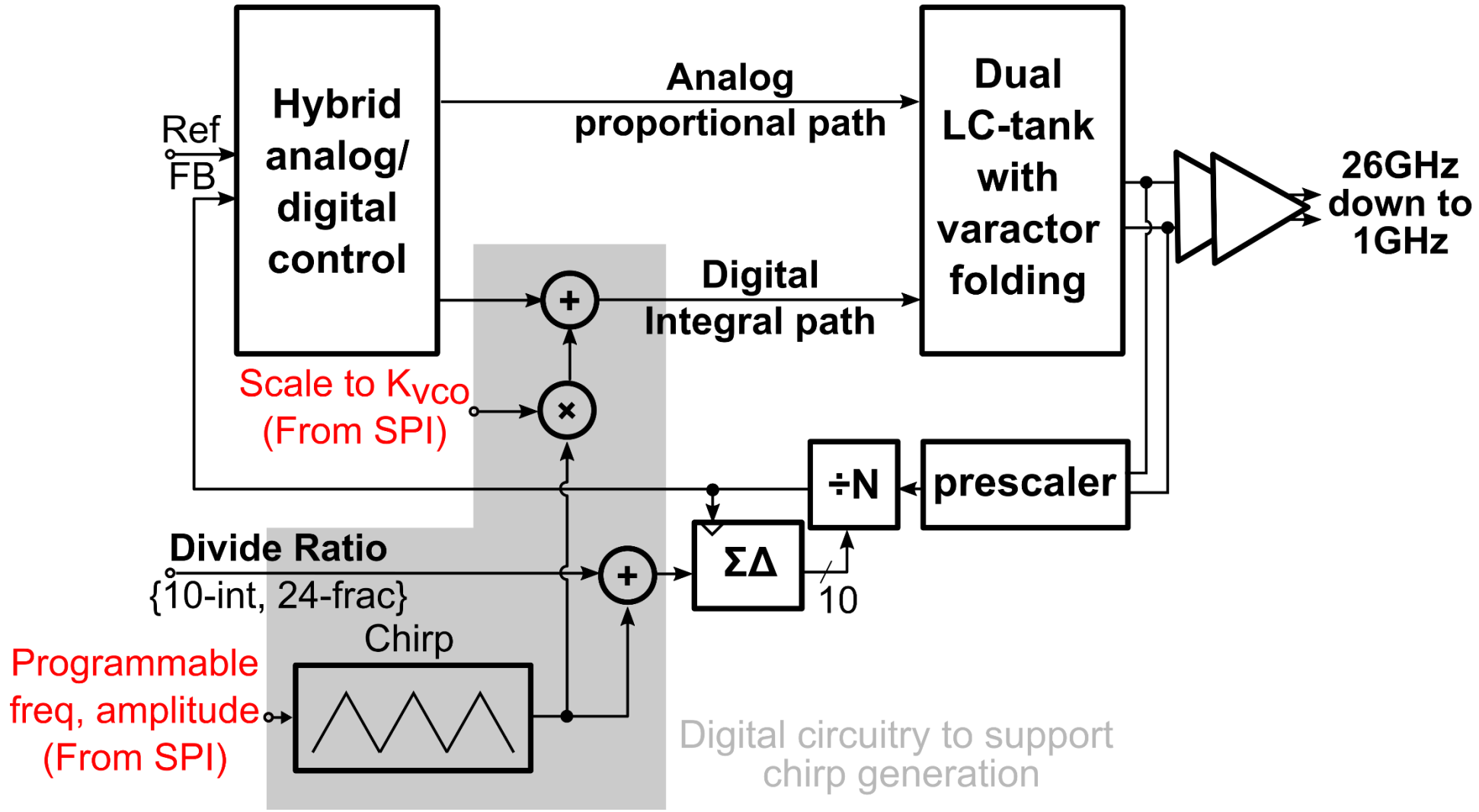


VCO: Coarse Band Elimination



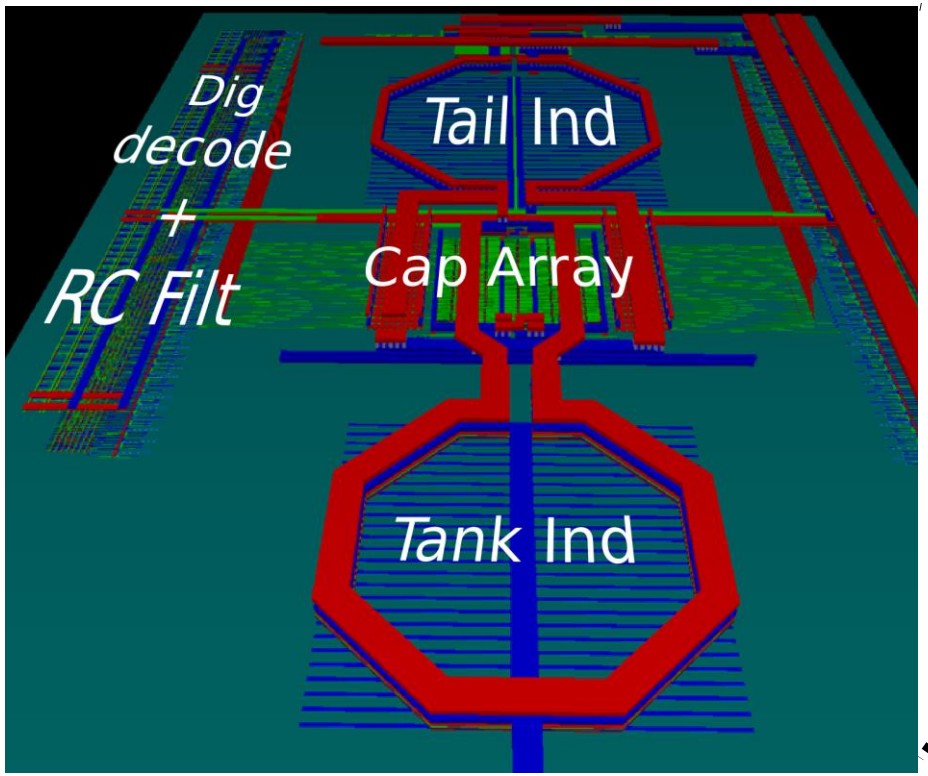
M. Ferriss, ISSCC16

PLL architecture

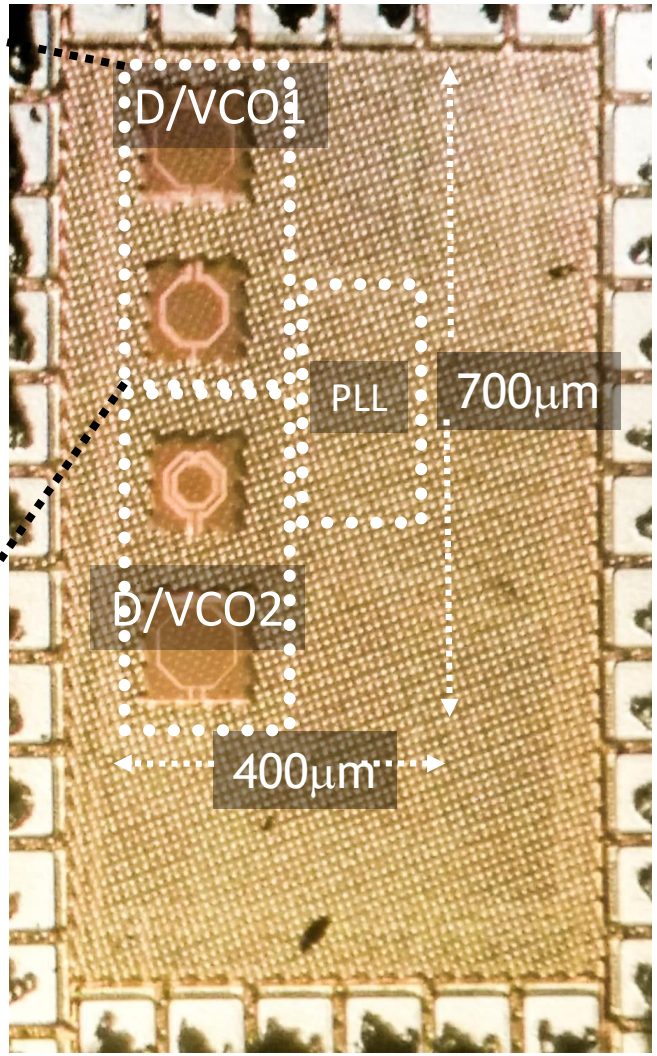


M. Ferriss et al, ISSCC16

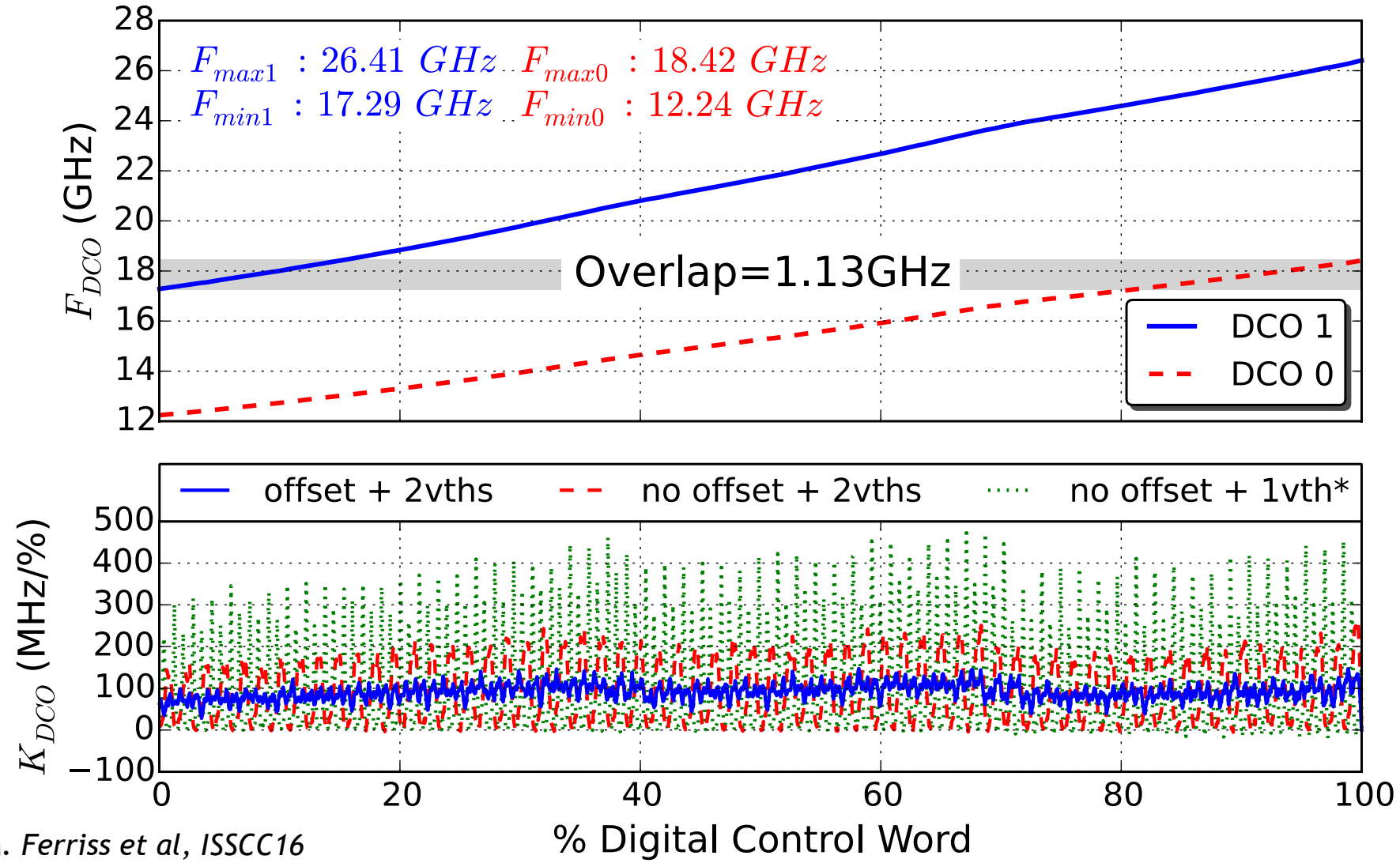
32nm SOI CMOS prototype



Visualization with GDS3D

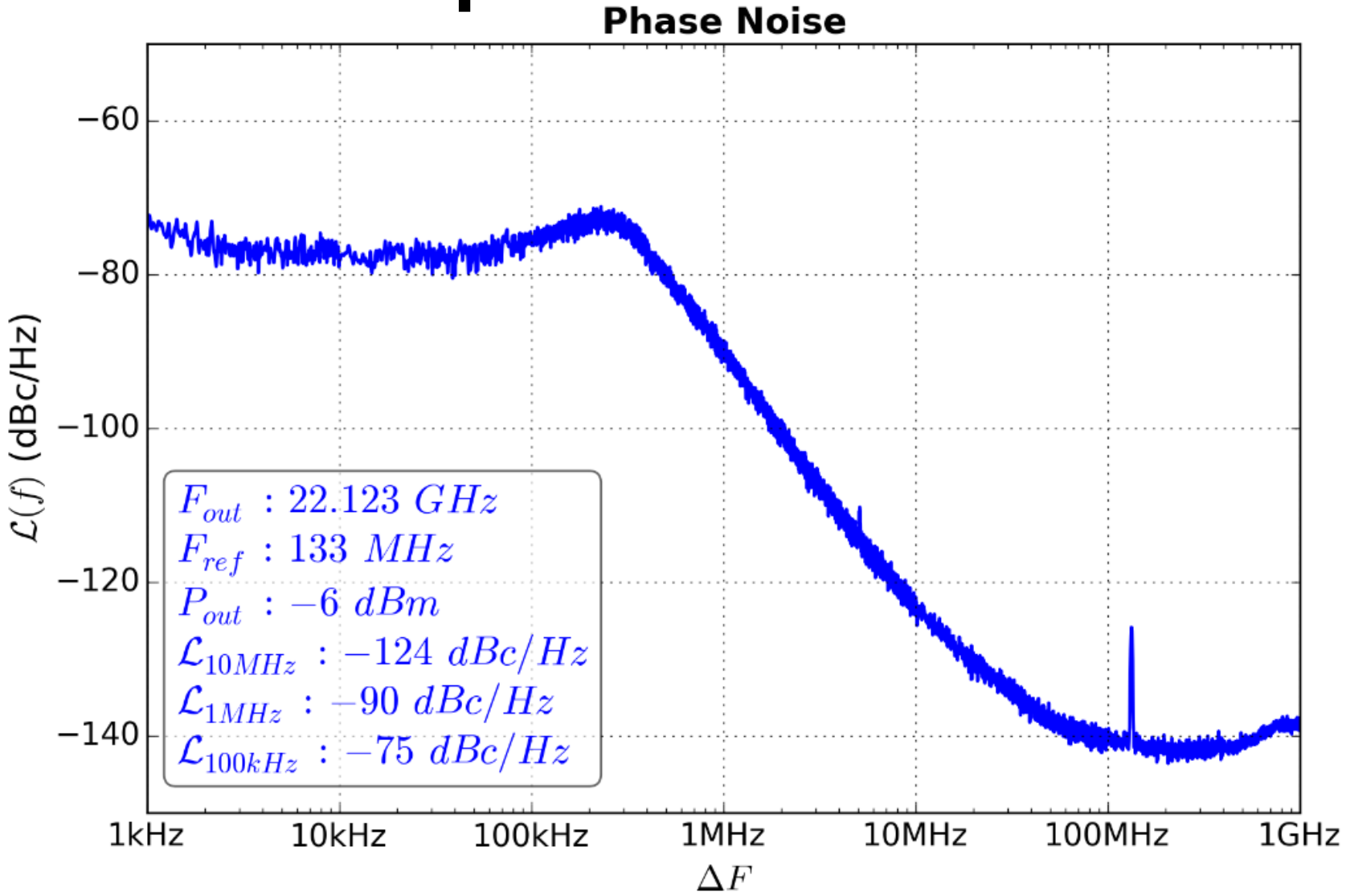


Measured tuning range and gain



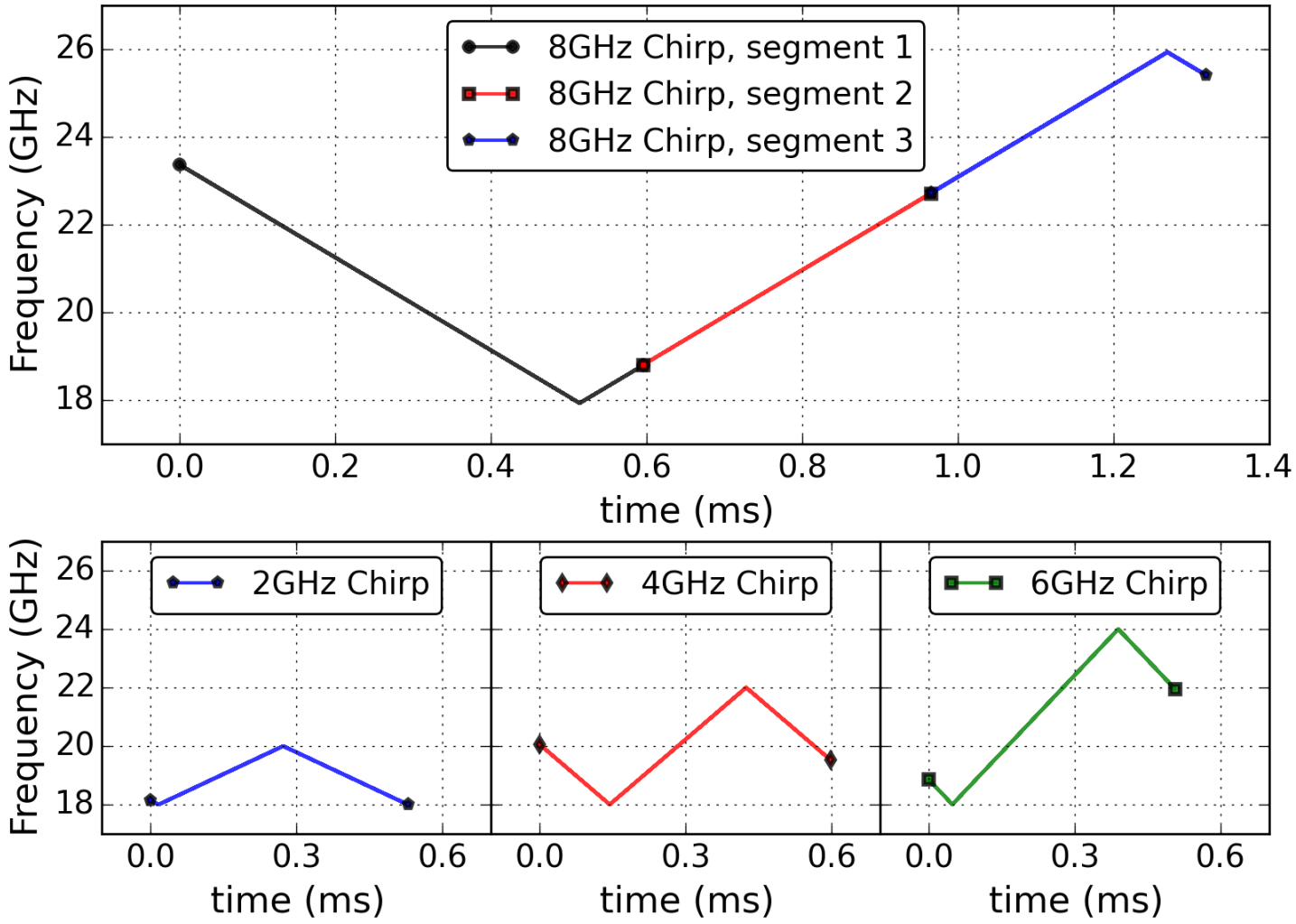
M. Ferriss et al, ISSCC16

Measured phase noise at 22GHz



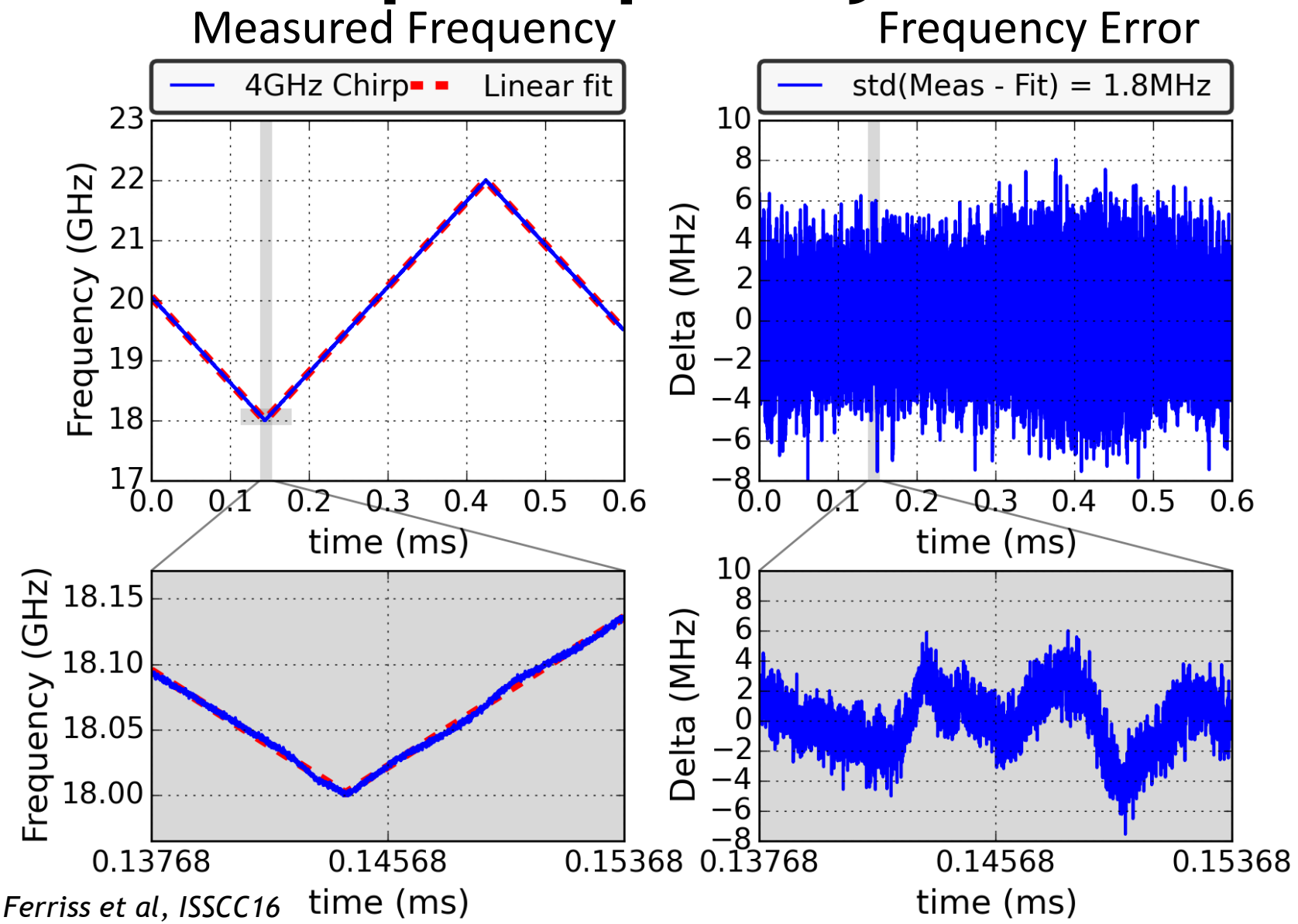
VCO's FOM = 181dBc/Hz, FOMT = 188dBc/Hz @10MHz offset

Measured transient frequency



An 80GHz oscilloscope directly samples PLLs output.
The 8GHz chirp was measured in segments due to scope memory limitations.

Chirp frequency errors



M. Ferriss et al, ISSCC16

Conclusion: Frac-N Hybrid PLL with Coarse Band Elimination

Key results

- Can support wide-range designs within integral path loop
- Linearization enhancement demonstrated
- Features of previous versions maintained

Outline

- Introduction and motivation: hybrid architectures
- Initial implementation: proof-of-concept
- Flexible synthesizer: frac-N w/ noise cancellation
- Flexible synthesizer: coarse band elimination
- **Flexible synthesizer: initial thoughts on flicker noise suppression**
- Summary/conclusion

Hybrid PLL and upconversion noise suppression

Recent Advances in CMOS oscillator flicker noise suppression

Strategy: Add phase shift to VCO loop [Pepe, et al., JSSC 2013]

- ✓ Simple implementation.
- × Magnitude of phase shift depends on absolute component values.

Strategy: Add tank resonance modes at second / third harmonics. [Shahmohammadi, et al., JSSC 2016]

- ✓ Dramatic improvement in phase noise.
- × Depends on component matching / difficult to precisely model impedances at very high harmonic frequencies

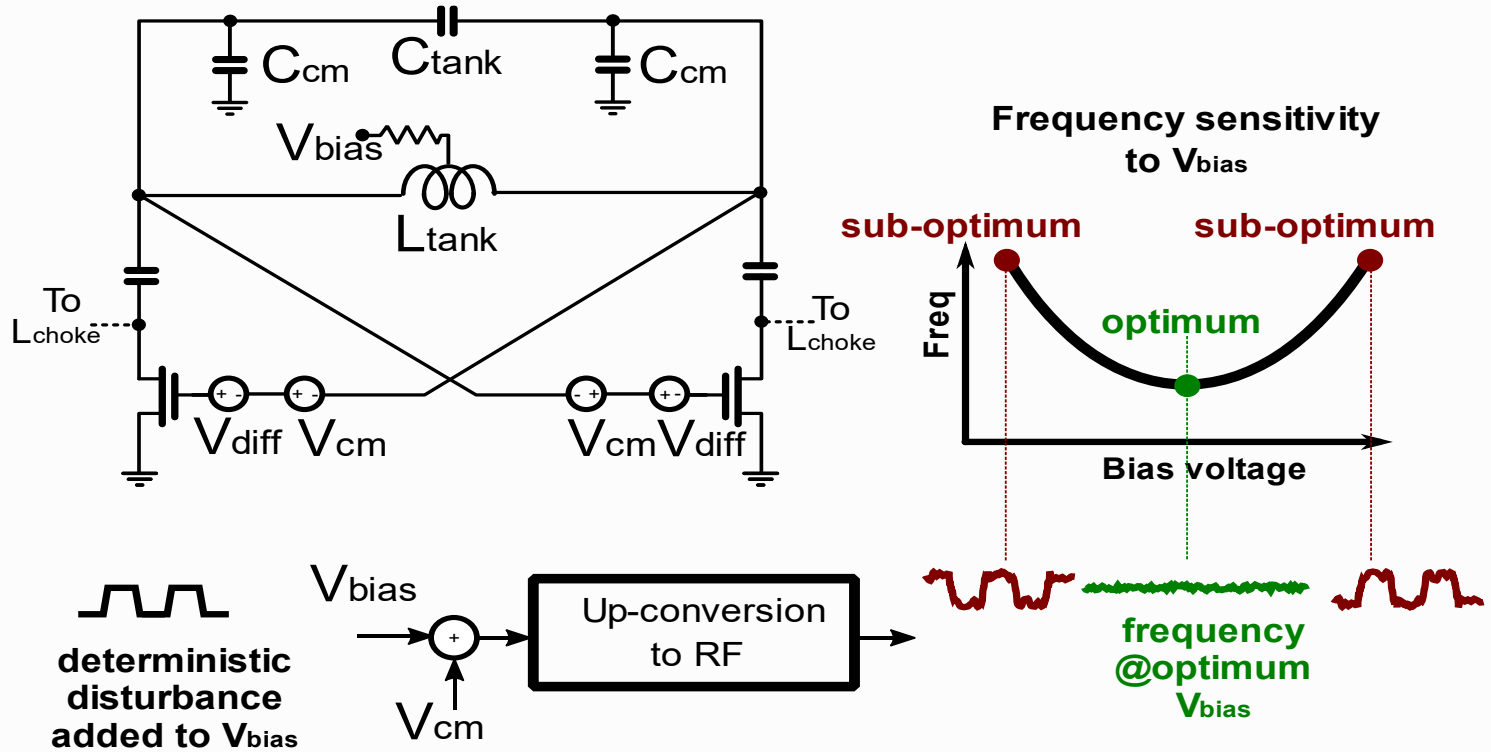
Opportunity: suppression of up-conversion mechanisms in a closed loop

An optimizing scheme is proposed that:

- Suppresses VCO upconverted noise
- Does not rely on absolute values of components
- Does not require accurate control of higher order resonance modes

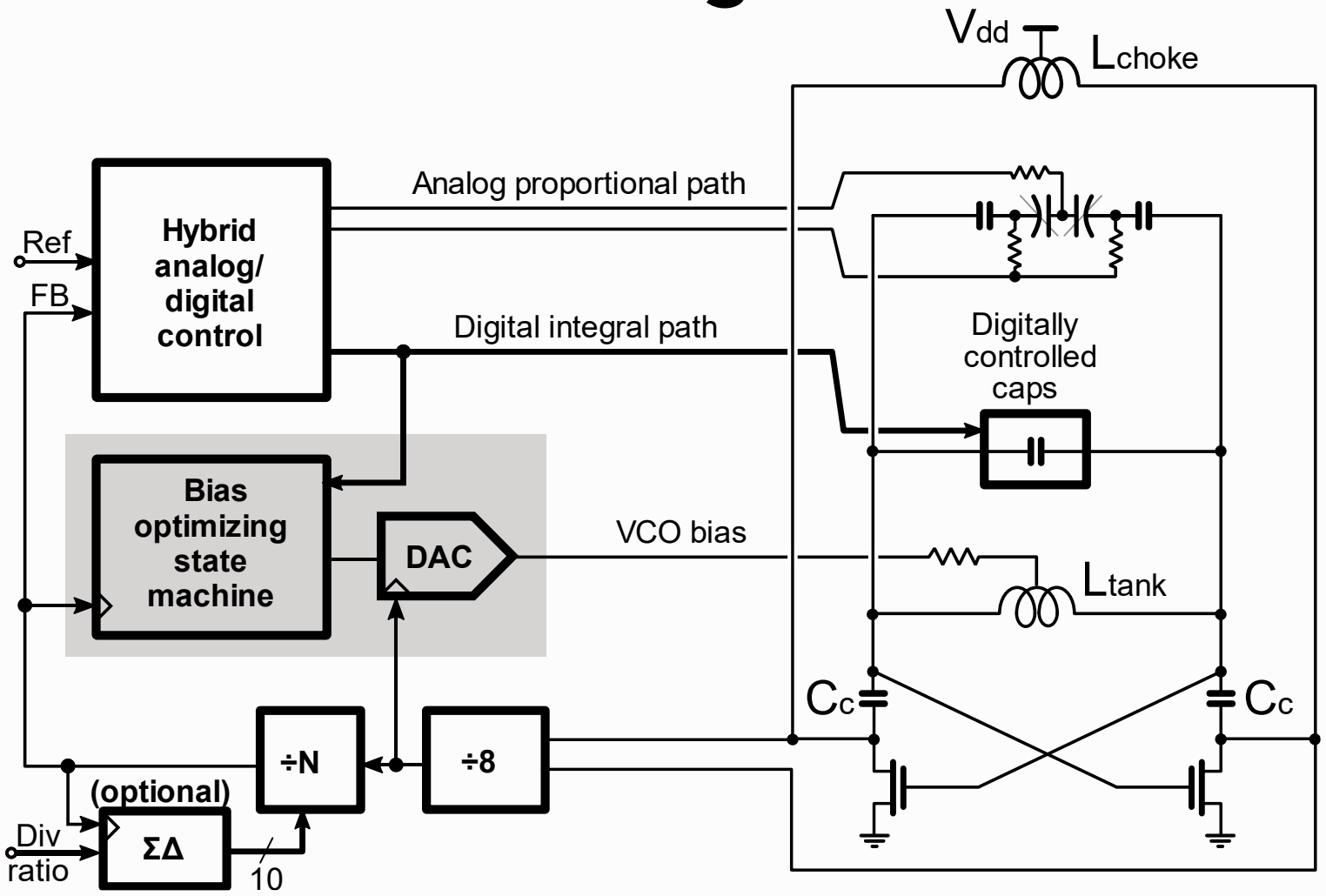
M. Ferriss et al, RFIC 2018

Noise and bias up-conversion gain

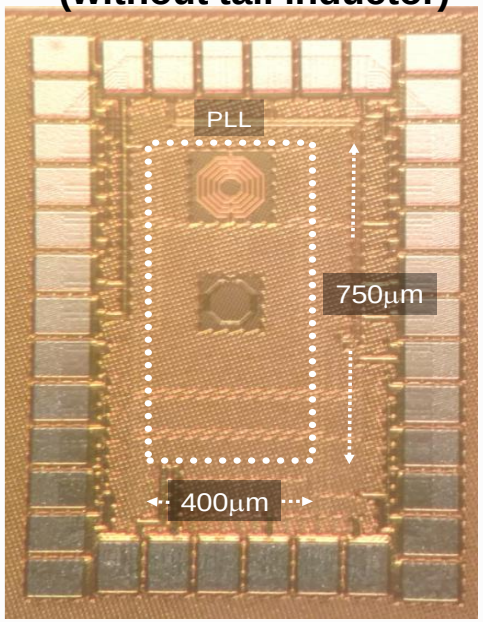


Same up-conversion mechanism for V_{cm} and V_{bias}
Minimizing bias-to-frequency gain minimizes noise up conversion

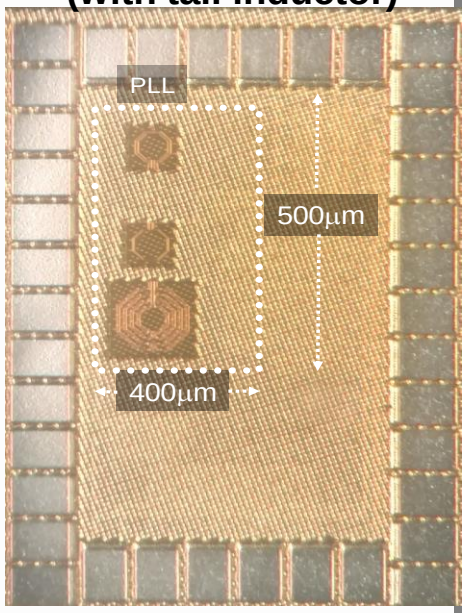
Design and Architecture



45nm
(without tail inductor)



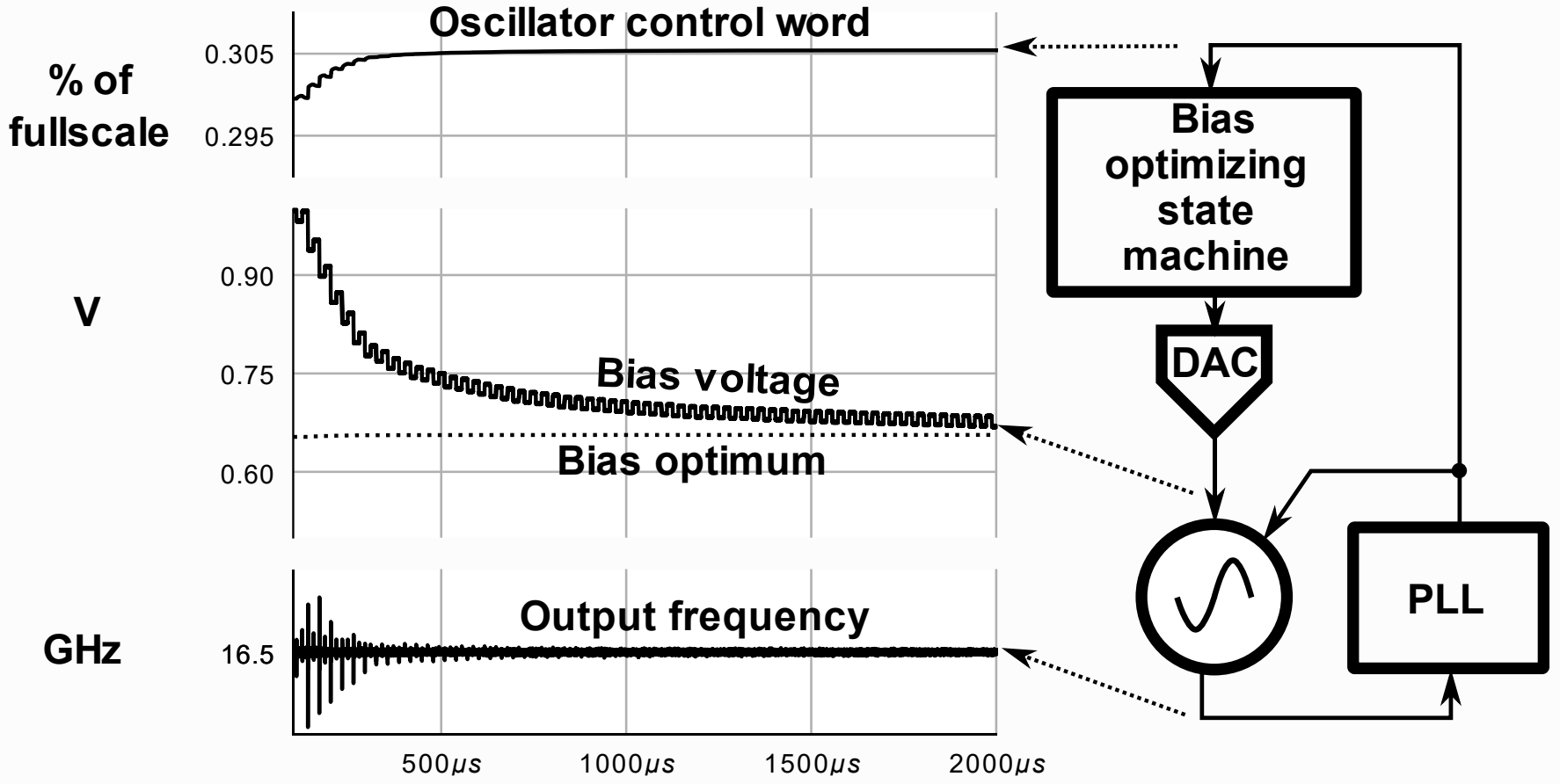
32nm
(with tail inductor)



Hybrid PLL's bias optimizing state machine

- Monitors digital control word for frequency
- Actuates on bias point of transconducting transistors in VCO

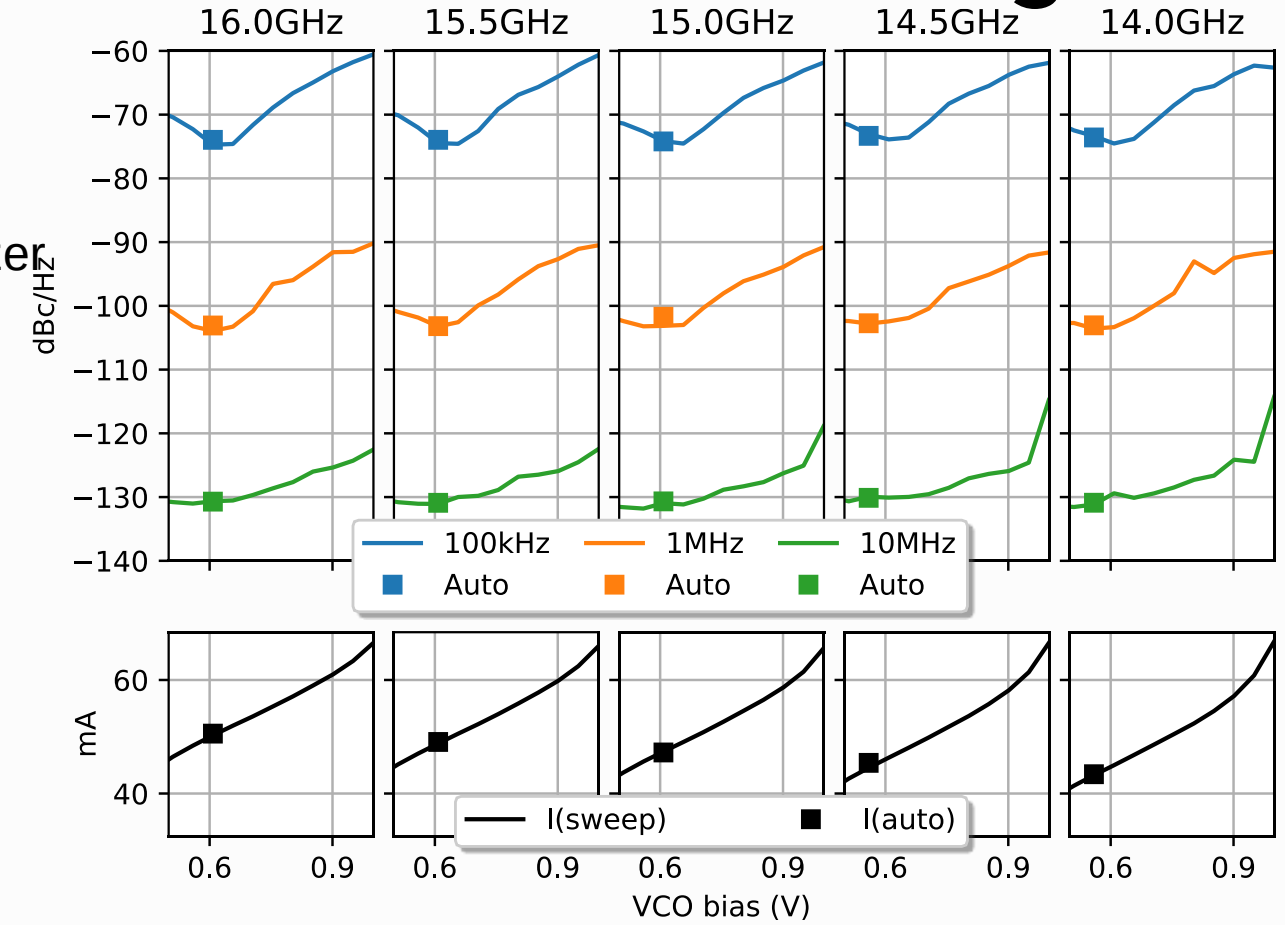
Behavioral sim shows the optimizer converging

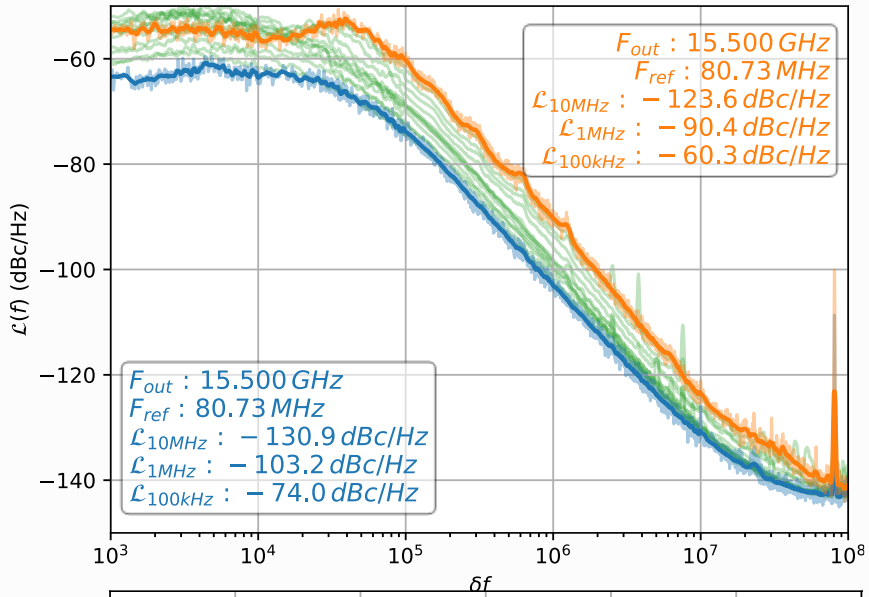


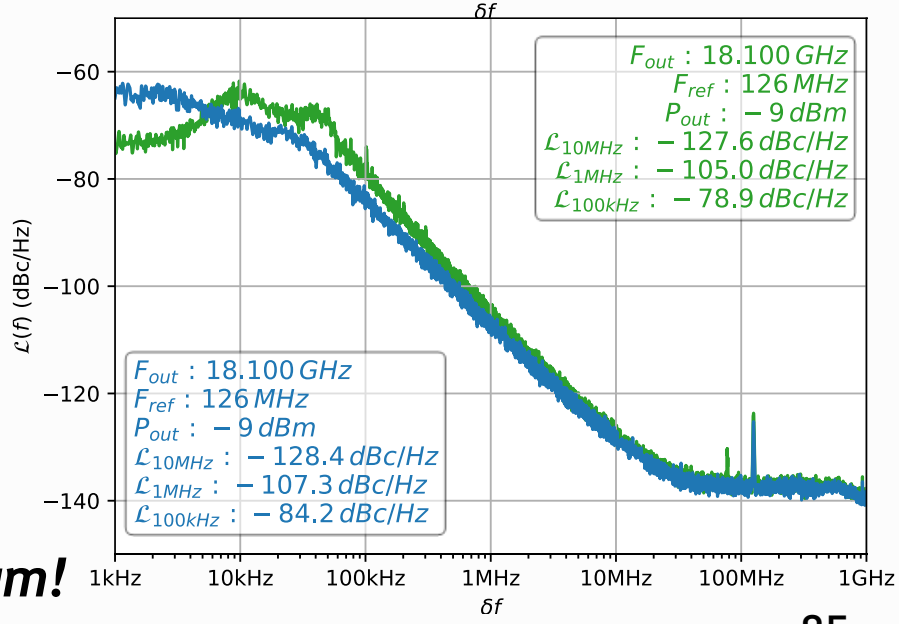
Disturbance is added to bias voltage and detected on oscillator control word
As bias approaches optimum, frequency disturbance disappears

Phase noise versus bias voltage

Squares (▪) → with optimizer
Solid lines → without optimizer







Result:
True closed loop system; no external calibration.
Prototypes in two different technologies: 45nm and 32nm

The VCO topology enables phase noise optimization, and
the optimization state-machine finds that phase noise minimum!

Outline

- Introduction and motivation: hybrid architectures
- Initial implementation: proof-of-concept
- Flexible synthesizer: frac-N w/ noise cancellation
- Flexible synthesizer: coarse band elimination
- Flexible synthesizer: flicker noise suppression exploration
- **Summary/conclusion**

Summary: Flexible Synthesizer Features Achieved Using Hybrid PLL Approach

Characteristic	Objectives	Implementation Approach
Tuning range 2-26GHz	Continuous tuning range to maximum frequency	Wide-range dual linearized transconductance VCO complex
Loop transfer function control	High programmability over wide range through digital control	Leverage highly digital architecture of dual-path HPLL
Supported reference rate	Flexible without sacrificing performance	Fractional-N synthesis
Fractional-N quantization noise	Active noise cancellation scheme that does not limit bandwidth	Proportional & integral path highly digital cancellation architecture
Area	Less than 1 mm^2 total	Single PLL with wide-range dual VCO complex
Fast frequency hopping	Fast settling time based on digital memory	Leverage digital memory/parameter replay
Spurious content	Minimize to enable broader use model	Reduced by utilization of digital/predictive techniques
Extended range in main loop	Eliminate need for coarse bands in supporting wide tuning range	Enhance and extend digital integral path approach to include full VCO range
Flicker noise suppression	Reduce low offset noise in CMOS PLLs	Closed-loop algorithm acting on noise proxy; ***more research required!***

Acknowledgements

- This work has been partially funded by DARPA under AFRL contract # FA8650-09-C-7924. The views, opinions, and/or findings contained in this presentation are those of the author/presenter and should not be interpreted as representing the official views or policies, either expressed or implied, of the Defense Advanced Research Projects Agency or the Department of Defense.
- Technical contributors and management support
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  - Bodhisatwa Sadhu
  - Alexander Rylyakov
  - Jose Tierno
  - Herschel Ainspan
  - Alberto Valdes Garcia
  - Daniel Friedman
  - Mehmet Soyuer

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