“Ultra-Thin Embedded Capacitance Laminates and how they improve the PDN and can Impact EMC”
Agenda

1. Typical/ Traditional PDN
2. The PDN using embedded capacitance
3. Some Causes of Resonance and EMC in PCB’s
4. Ultra-Thin Laminates for Embedded Capacitance and the reducing impact on EMC
5. Some practical results/ case studies
6. What’s Next
TYPICAL/ TRADITIONAL POWER DISTRIBUTION NETWORK
TYPICAL/ TRADITIONAL POWER DISTRIBUTION NETWORK

- Capacitor interconnects;
- Individual capacitor values and packaging forms;
- Number of capacitors needed;
- Capacitor placement;
- PCB stack-up;
- Power/ground plane pair geometry;
- Segmentation and isolation

Courtesy of Dr. Jun Fan
Device Switching And Noise Current

PDN Design Objectives

1. Ensure charge supply for logic transitions
   - Enough capacitance to store charge
   - Enough charge readily available for short transitions

2. Minimize noise voltage distribution on the $V_{cc}$/GND plane pair
   - Low power bus impedance over frequency
   - Noise decoupling
   - Noise isolation

Courtesy of Dr. Jun Fan
Component density is reaching its limit

High capacitance and capacitance uniformity is the key to embed
Trends in PCB Development

Ultra-thin Laminate Approach to Embedded Capacitance Technology-

BENEFITS

• Reduction and/or elimination of surface CAPACITORS and resistors increases reliability of the device

• ELECTROMAGNETIC INTERFERENCE (EMI) from the PCB is reduced or eliminated using some ultra thin film based laminates

• IMPEDANCE is greatly reduced!!!

• RoHS compliant

• Provides more efficient/ excellent POWER DELIVERY (charge comes directly underneath the device, 1 mil up)

• SIMPLIFY CIRCUIT ROUTING and eliminates 2 vias, traces, and pads for every capacitor eliminated.

• Allows for a smaller PWB DESIGN- FORM FACTOR if needed.
## Background / Motivation

### Trends in PCB Development

**Cost saving**
- Remove thousands of SMT capacitors
- Reduce assembly cost and time
- Improve quality associate with assembly defects
- Reduce board size

**Cost Increase**
- Additional cost of BC material

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(a) Original board design  
(b) Board design with BC

---

*When enhanced performance is required*
Background / Motivation

Trends in PCB Development

Ultra thin Laminate Approach to Embedded Capacitance Technology-
BENEFITS (continued)

• **BETTER ELECTRICAL PERFORMANCE** and **HIGHER RELIABILITY** demonstrate the benefit of this ultra thin film based embedded capacitance approach

• **ASSEMBLY COST** is reduced by minimizing passives used

• Eliminates or minimizes issues with **POOR SURFACE MOUNT CONNECTIONS** or poor joints since the shared capacitor layer is embedded

• This technology is **NOT NEW** and has been used for many years although there is now more need for it due to densities of the newest designs

• PCB and assembly will be **LIGHTER**
Planar Capacitor and Discrete Capacitor
Embedded Capacitance Technology

Range for Planar Capacitors
Background of demand for PCB with Embedded Capacitor

“Thin” power ground plane is the key parameter to improve electrical performance at high frequency!

Voltage Regulator

Embedded capacitance layer

Power

Ground

L ∝ Loop area ∝ Power ground thickness

⊿V = I*R + L*di/dt

Voltage is decreasing

Allowable ∆V is ±5% of Voltage

Will increase as Power increase

Will increase as clock speed increase

ITRS 2010

ITRS, Swaminathan et al.

⊿V < 50mV

⊿V < 250mV

⊿V < 500mV
**Target Impedance Concept**

**Target Impedance Trend through Year**

<table>
<thead>
<tr>
<th>Year</th>
<th>Design Rule (nm)</th>
<th>Power (W)</th>
<th>Vdd (V)</th>
<th>Current (A)</th>
<th>Target Impedance (mΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2004</td>
<td>90</td>
<td>84</td>
<td>1.2</td>
<td>70</td>
<td>1.7</td>
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<tr>
<td>2007</td>
<td>65</td>
<td>103.6</td>
<td>0.9</td>
<td>115.11</td>
<td>0.7</td>
</tr>
<tr>
<td>2010</td>
<td>45</td>
<td>119</td>
<td>0.6</td>
<td>198.33</td>
<td>0.3</td>
</tr>
</tbody>
</table>

ITRS, Swaminathan et al.

\[ Z_{\text{target}} = \frac{(V_{dd} \times 0.05)}{(I \times 50\%)} \]

**Target Impedance Trend**

*When enhanced performance is required*
**Plane Impedance Characteristic**

- **Capacitance Domain**
  - $1/\omega C = -20 \text{ dB/dec}$
  - Bulk Capacitor
  - Decoupling Capacitor

- **Inductance Domain**
  - $\omega L = 20 \text{ dB/dec}$
  - Plane Capacitor
  - On-Chip Capacitor

---

**Speed of charge delivery**

- Decreasing interconnect inductance
- Amount of charge available for delivery

---

**FaradFlex**

**OAK-MITSUI TECHNOLOGIES**
Solution

High speed computing boards
Servers, Routers, Super computers

- CPU processor speed $\uparrow$
- Operation voltage $\downarrow$
- Power consumption $\uparrow$

- Power distribution improvement

- Planar embedded capacitor

Module boards
Cell phones, PDA, Note book

- Multiple band $\uparrow$
- More functions $\uparrow$
- Cost $\downarrow$

- Miniaturization / HDI

- Discrete embedded capacitor

WHEN ENHANCED PERFORMANCE IS REQUIRED
Power/Ground Plane Pair

- thin is always better

Ultra-Thin substrate for use as power distribution layer

Construction of ultra-thin substrate

Copper Foil

Dielectric layer 8 to 24 um

Copper Foil
TYPICAL PCB DESIGN AND STACK UP
10 LAYER PCB STACK-UP
With 2 Power-Ground layers at L2/L3 and L8/L9
(using 24 micron laminate in the Power-Ground allows for buried capacitance)
PCB Example

24 Layer Board

Sun Microsystems PCB
High Volume Server

12 µm
IMPROVED IMPEDENCE/INDUCTANCE
PCB Electrical Performance

MEASURE $S_{21}$ BY DIRECT STIMULUS INJECTION INTO THE COPPER PLANES

4 LAYER TEST BOARD CROSS SECTION VIEW

- Layer 1: VNA Port 1
- Layer 2: Filler Prepreg
- Layer 3: Dielectric Layer
- Layer 4: Under Test
- Layer 5: Filler Prepreg

VIA HEIGHTS REMAIN CONSTANT FOR ALL DLUT THICKNESS

0.050
PCB Electrical Performance

Discrete capacitors of 0.1μF have a resonance frequency of about 15 MHz
Discrete capacitors of 0.01μF have a resonance frequency of about 40 MHz.

Panel Size= 50 in²
80% Retained Cu

<table>
<thead>
<tr>
<th>Product</th>
<th>nF</th>
</tr>
</thead>
<tbody>
<tr>
<td>ZBC2000</td>
<td>16</td>
</tr>
<tr>
<td>ZBC1000</td>
<td>32</td>
</tr>
<tr>
<td>BC24</td>
<td>40</td>
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<tr>
<td>BC16</td>
<td>64</td>
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<tr>
<td>BC12</td>
<td>76</td>
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<td>124</td>
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<tr>
<td>BC12T M</td>
<td>180</td>
</tr>
<tr>
<td>BC16T</td>
<td>440</td>
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</table>
PCB Electrical Performance  (Up to 1 GHz)

Panel Size= 50 in²
80% Retained Cu

<table>
<thead>
<tr>
<th>Product</th>
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<tbody>
<tr>
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<td>BC12TM</td>
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<td>BC16T</td>
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</table>
PCB Electrical Performance (Up to 3 GHz)

Panel Size = 50 in²
80% Retained Cu

<table>
<thead>
<tr>
<th>Product</th>
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<tbody>
<tr>
<td>ZBC2000</td>
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<td>BC12TM</td>
<td>180</td>
</tr>
<tr>
<td>BC16T</td>
<td>440</td>
</tr>
</tbody>
</table>

Product Specifications
- ZBC-2000
- ZBC-1000
- FaradFlex BC24
- FaradFlex BC16
- FaradFlex BC12TM
- FaradFlex BC8
- FaradFlex BC16T

Panel Size = 50 in²
80% Retained Cu

Self Impedance (Ohms)

Frequency (Hz)
RELIABILITY
## Reliability Tests

<table>
<thead>
<tr>
<th>Description</th>
<th>Result</th>
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</thead>
<tbody>
<tr>
<td>6x Through Hole Solder Shock</td>
<td>PASS</td>
</tr>
<tr>
<td>6x Blind Via Solder Shock</td>
<td>PASS</td>
</tr>
<tr>
<td>Dielectric Thickness per Cross Section within +/-10%</td>
<td>PASS</td>
</tr>
<tr>
<td>T-288 (&gt;20min)</td>
<td>PASS</td>
</tr>
<tr>
<td>IST Testing (500 cycles)</td>
<td>PASS</td>
</tr>
<tr>
<td>Core Level Hi-Pot Testing 100Cores (100V/sec; 500Vmax)</td>
<td>PASS</td>
</tr>
<tr>
<td>Finished Circuit Level Hi-Pot 50 circuits (100V/sec; 500Vmax)</td>
<td>PASS</td>
</tr>
</tbody>
</table>

*Courtesy of Sanmina-SCI*
PCB FABRICATION/ PROCESSING
Processing guideline

**Pre-clean**
- Standard process

**Dry Film lamination**
- Standard process

**Expose Image**
- Standard process

**Pattern etching**
- Thin core compatible line recommended
  Ex) Thin core Schmid etching line
- Use leader board if not confident
- Careful Handling required

**Black oxidizing or alternative oxides**
- Thin core compatible line recommended
- Use leader board if not confident
- Horizontal line preferred
- Careful Handling required

---

Important
Comparison of Inner layer Processes

8 μm to 24 μm Film based laminate and partially filled
1. Pre-Clean
2. Dry Film lamination
3. Expose Image
4. Pattern etching (Both sides)
5. Black Oxide or Alternative

16 μm (Highly Filled with High Dk Particles)
1. Pre-Clean
2. Dry Film lamination
3. Expose Image (Pattern/Blanket)
4. Pattern etching (One side)
5. Black Oxide or Alternative
6. Laminate Prepreg/Cu to Imaged Side
7. Pre-Clean
8. Dry Film Laminate
9. Expose Image (Both Sides)
10. Pattern Etching (Both Sides)
11. Black Oxide or Alternative

Second Imaging Step

When enhanced performance is required
POWER DISTRIBUTIONS NETWORK SIMULATIONS
RESONANCE/ NOISE/ EMI
Why Buried Capacitance Designs Using Buried Capacitance Can Reduce EMI

1. Can minimize loop area  \( E_r = 1.316 \times 10^{-14} \times I \times f^2 \times S / r \)
2. Can minimize power bus noise
3. Can minimize resonance
4. Can minimize propagation to the edge (Related to Transfer Impedance (S21))

[Diagram]

E : Electric Field Strength
I : Normal Mode Current
f : Frequency
S : Loop Area
r : Distance
Transfer Impedance Simulation (Z₂₁) with PIStream

Transfer Impedance Analysis  2 mil FR4 VERSUS 1 mil Laminate

FR-4 (0.6 mm Core)  24 micron polymer film type laminate

If the transfer impedance is too high...
1. Increase power bus noise
2. Digital circuit noise would affect RF or Analog circuit.
3. Increase EMI (related to S₂₁)
Resonance Distribution

35- 0.1μF caps for power supply

0.4mm (16 mil P/G)

24 μm P/G
Dk 4.4
No additional caps

Can not place caps!

35- 0.1μF caps for power supply
+44-0.1 μF caps for resonances

26dB
Resonance Distribution - Lower Noise Threshold

-26 dB

400 μm (16 mil P/G)
79 caps

24 μm P/G
Dk 4.4
35 caps

12 μm P/G
Dk 10
35 caps
Test Board - Simulation #2

Standard core (400umFR-4) with no caps  Standard core (400umFR-4) with caps
Test Board- Simulation #2

- P/G Plane 16 micron Dk 30
- P/G Plane 1 mil
- P/G Plane ½ mil
- P/G Plane 16 micron Dk 30

FaradFlex
When Enhanced Perform
CASE STUDY 1
PCB Construction of Reference Board

<table>
<thead>
<tr>
<th>No.</th>
<th>Layer</th>
<th>Thickness [mm]</th>
<th>Notes</th>
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<tbody>
<tr>
<td>1</td>
<td>Signal</td>
<td>0.057</td>
<td>Include Plating</td>
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<tr>
<td></td>
<td>resist</td>
<td></td>
<td></td>
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<tr>
<td>2</td>
<td>Gnd(Plane)</td>
<td>0.032</td>
<td></td>
</tr>
<tr>
<td></td>
<td>prepreg</td>
<td>0.11</td>
<td></td>
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<tr>
<td>3</td>
<td>Signal</td>
<td>0.032</td>
<td></td>
</tr>
<tr>
<td></td>
<td>prepreg</td>
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<tr>
<td>4</td>
<td>Gnd(Plane)</td>
<td>0.032</td>
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<tr>
<td></td>
<td>prepreg</td>
<td>0.14</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Vdd(Plane)</td>
<td>0.032</td>
<td></td>
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<tr>
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<td>6</td>
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<tr>
<td></td>
<td>prepreg</td>
<td>0.14</td>
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<tr>
<td>7</td>
<td>Gnd(Plane)</td>
<td>0.032</td>
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<tr>
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<tr>
<td>8</td>
<td>Signal</td>
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<td>9</td>
<td>Signal</td>
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<td>Vdd(Plane)</td>
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<td>12</td>
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<td>0.032</td>
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<td>14</td>
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<td>0.057</td>
<td>Include Plating</td>
</tr>
<tr>
<td></td>
<td>resist</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Total: 2.36 ±0.2 mm

(by courtesy of NEC System Technology, Inc. & NEC Information Technology, Inc.)
A Conception Diagram of The Distant Place Magnetic Field Measurement

- Antenna direction is Horizontal (Horizontal Polarized Wave Measurement)
- Antenna direction is Vertical (Vertical Polarized Wave Measurement)

- PCB Horizontal
- PCB Vertical

Turn Table
Antenna
Preamp
Spectrum Analyzer
Controller
Control Terminal PC

(Source: Noise Laboratory)
Comparison between reference board with Caps and BC without Caps

1 mil Laminate

1/2 mil Laminate
CASE STUDY 2
3.3V

L1 – Signal ½ Oz
L2 – 3.3V Power 1 Oz
L3 – Signal 1 Oz
L4 – GND 1 Oz
L5 – Signal 1 Oz
L6 – 48V, 12V_A, 1.5V Power 1 Oz
L7 – GND 1 Oz
L8 – Signal 1 Oz
L9 – 1.5V, 1.8V, VCC, 12V_B Power 1 Oz
L10 – Signal 1 Oz
L11 – GND 1 Oz
L12 – Signal ½ Oz

1.5V

L1 – Signal ½ Oz
L2 – Power 1 Oz
L3 – GND 1 Oz
L4 – Signal 1 Oz
L5 – GND 1 Oz
L6 – Signal 1 Oz
L7 – Power 1 Oz
L8 – GND 1 Oz
L9 – Signal 1 Oz
L10 – GND 1 Oz
L11 – Signal 1 Oz
L12 – Power 1 Oz
L13 – GND 1 Oz
L14 – Signal ½ Oz

781 0.1μF decoupling capacitors

Current Stackup
Total Copper:
Power – 3oz
GND – 3 oz

Embedded Material

Emb Capacitance Stackup
Total Copper:
Power – 3oz
GND – 5 oz

WHEN ENHANCED PERFORMANCE IS REQUIRED
### Capacitance Measurements
(courtesy of Univ. of Missouri at Rolla)

<table>
<thead>
<tr>
<th>Plane Pair</th>
<th>FR-4 (nF)</th>
<th>24 μm (nF)</th>
<th>12 μm (nF)</th>
<th>12 μm DK10 (nF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.5V/GND</td>
<td>76.1 (75.8)</td>
<td>179.5 (179.0)</td>
<td>286.7 (266)</td>
<td>487 (478)</td>
</tr>
<tr>
<td>3.3V/GND</td>
<td>21.2 (21.2)</td>
<td>323.8 (321.3)</td>
<td>551 (541)</td>
<td>1148 (1082)</td>
</tr>
</tbody>
</table>

**From LCR Meter**

**Extracted from VNA**

Note: 1.5V plane is split resulting in smaller capacitor area

Replaces 78.1 μF of capacitance on standard board (781 capacitors of 0.1 μF)
Board Impedance Measurements (S21, Z11)

Measurement Equipment: Agilent 8753D (Vector Network Analyzer)
Probe Point: Decoupling Capacitor Pad

Graphs showing impedance measurements for different conditions.
Time Domain Power Bus Noise Measurement

Measurement Equipment: Agilent Infiniium 54855A (Digital Sampling Oscilloscope)
Probe Point: Decoupling Capacitor Pad

1.5V/GND (FR-4) 50 μm  
1.5V/GND 24 μm  
1.5V/GND 12 μm  
1.5V/GND 12 μm Dk 10

3.3V/GND (FR-4) 50 μm  
3.3V/GND 24 μm  
3.3V/GND 12 μm  
3.3V/GND 12 μm Dk 10
Frequency Domain Power Bus Noise Measurement

Measurement Equipment: Agilent E7404A (Spectrum Analyzer)
Probe Point: Decoupling Capacitor Pad

Tested to 1 GHz
CASE STUDY 3
The Embedded Passives Journey

IPC/APEX – April 2, 2008
Authors:
Bill Devenish – Harris Corp., Mechanical Advanced Development (MAD)
Andrew Palczewski – Harris Corp., PCB Technologist
<table>
<thead>
<tr>
<th>COST SAVINGS</th>
<th>$37.88</th>
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<tbody>
<tr>
<td><strong>- Part Cost</strong></td>
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<tr>
<td>CAPACITORS</td>
<td>$1.19</td>
</tr>
<tr>
<td>RESISTORS</td>
<td>$9.77</td>
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<tr>
<td><strong>- Cost of Quality</strong></td>
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</tr>
<tr>
<td>Component Body</td>
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<tr>
<td>CAPACITORS</td>
<td>$4.04</td>
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<td>0603</td>
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<td>0201</td>
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<td>0402</td>
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<tr>
<td><strong>- Assembly Cost</strong></td>
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<tr>
<td>Total Parts</td>
<td>591</td>
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</table>

Used with the permission of Harris Corporation.
## Analysis Results:

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<thead>
<tr>
<th></th>
<th>Conventional</th>
<th>Embedded</th>
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<tbody>
<tr>
<td>Board Width (inches)</td>
<td>2.5</td>
<td>2.42</td>
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<tr>
<td>Board Length (inches)</td>
<td>4.0</td>
<td>3.87</td>
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<tr>
<td>Number Up</td>
<td>30</td>
<td>32</td>
</tr>
<tr>
<td>Number of Layers</td>
<td>12</td>
<td>10</td>
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<tr>
<td>Panelization Efficiency</td>
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<td>0.63</td>
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<td>Component Cost Difference</td>
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<tr>
<td>Board Price Difference</td>
<td>-4.32</td>
<td>-26.0</td>
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<tr>
<td>System Total Cost Difference</td>
<td>-28.9</td>
<td>-28.9</td>
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</table>

Positive values (red) indicate increases in cost when passives are embedded.
Negative values (green) indicate decreases in cost when passives are embedded.
Other Benefits
## Capacitor Material vs. FR4

<table>
<thead>
<tr>
<th>Properties</th>
<th>NiP/Capacitor Core</th>
<th>NiP Core FR-4 (control)</th>
<th>Remarks and Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sheet Resistivities (ohm/square)</td>
<td>25</td>
<td>25</td>
<td>Nominal</td>
</tr>
<tr>
<td>Material Tolerance</td>
<td>+/-5%</td>
<td>+/-5%</td>
<td></td>
</tr>
<tr>
<td>Load Life Cycling Test</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Resistor Size: 0.500&quot; X 0.050&quot;</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Loaded: (Δ R%) 150mW</td>
<td>&lt;0.9 after 3200 hrs.)</td>
<td>&lt;5</td>
<td>MIL-STD-202-108I</td>
</tr>
<tr>
<td>Unloaded: (Δ R%)</td>
<td>&lt;0.74 after 3200 hrs.)</td>
<td></td>
<td>Ambient Temp: 70°C</td>
</tr>
<tr>
<td>Off Cycle: 1.5 hrs</td>
<td></td>
<td></td>
<td>On Cycle: 1.5 hrs</td>
</tr>
<tr>
<td>Length Of Test: 10000 hrs</td>
<td></td>
<td></td>
<td>Off Cycle: 1.5 hrs</td>
</tr>
<tr>
<td>Current Noise Index in dB</td>
<td>&lt;=23</td>
<td>&lt;=15</td>
<td>MIL-STD-202-308</td>
</tr>
<tr>
<td>Humidity Test (Δ R%)</td>
<td>0.5</td>
<td>0.5</td>
<td>Voltage Applied: 5.6 Volts</td>
</tr>
<tr>
<td>Characteristic (RTC) PPM/°C</td>
<td>-6.0</td>
<td>50</td>
<td>MIL-STD-202-304</td>
</tr>
<tr>
<td>Hot Cycle: 25°, 50°, 75°, 125°C</td>
<td></td>
<td></td>
<td>Hot Cycle Temp: 125 °C</td>
</tr>
<tr>
<td>Cold Cycle: 25°, 0°, -25°, -55°C</td>
<td></td>
<td></td>
<td>Cold Cycle Temp: -65 °C</td>
</tr>
<tr>
<td>Thermal Shock (Δ R%)</td>
<td>0.2</td>
<td>-0.5</td>
<td>MIL-STD-202-107B</td>
</tr>
<tr>
<td>No of Cycles: 25</td>
<td></td>
<td></td>
<td>Hot Cycle Temp: 125 °C</td>
</tr>
<tr>
<td>Cold Cycle Temp: -65 °C</td>
<td></td>
<td></td>
<td>Cold Cycle Temp: -65 °C</td>
</tr>
<tr>
<td>Solder Float (Δ R%)</td>
<td></td>
<td></td>
<td>MIL-STD-202-210D</td>
</tr>
<tr>
<td>After 1 Cycle</td>
<td>-0.4</td>
<td>0.5</td>
<td>Temp: 260°C</td>
</tr>
<tr>
<td>After 5 cycles</td>
<td>-0.6</td>
<td></td>
<td>Immersion: 20 Second</td>
</tr>
<tr>
<td>Power Density (mW/mil²) derated at 50%</td>
<td>0.45</td>
<td>0.15</td>
<td>Step-up Power Test</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Resistor size 0.020&quot; x 0.030&quot;</td>
</tr>
</tbody>
</table>

3X better power density through resistor due to better heat conductivity of the buried capacitor laminate

Synergistic Effect!
Buried Capacitance™ Core

Some ultra thin laminates have 3 to 5 times better heat transfer

Thinner dielectric provides better heat transfer
Conclusion

• Embedded Capacitor and can Improve System Price/Performance by
  – Reducing Discrete Caps
  – Reducing PWB size
  – Increasing Functionality
  – Improving power distribution
  – Improving Signal integrity

• Thinner Power Distribution Planes are required for improved Impedance Performance at high frequency

• New Substrates have demonstrated excellent electrical performance and physical properties.

• They are compatible with PCB processing; a truly “drop in” material.

• Materials are commercially available from many Fabricators

• Substrates Filled with Ferroelectric Particles have better performance, but result in higher cost PCBs

• GREEN and Lead Free Solution
Thank You