Lee Hill

SILENT, LLC

Lee Hill is Founding Partner of SILENT, an independent electromagnetic compatibility (EMC) and RF design firm established in 1992 that specializes in EMC and RF design, troubleshooting, and training services. Lee received the Master of Science Degree in Electrical Engineering & Electromagnetics with highest honors from the University of Missouri-Rolla, (now Missouri University of Science and Technology). He is a returning instructor for the IEEE EMC Society's annual Global University program and he has over twenty-five years of experience in the EMC design and retrofit of complex electronic systems. Lee has been teaching short courses on EMC design and troubleshooting for twenty years.

Prof.James Drewniak

Missouri University of Science and Technology

James L. Drewniak (S'85-M'90-SM'01-F'07) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Illinois, Urbana-Champaign, in 1985, 1987, and 1991, respectively. In 1991, he joined the Department of Electrical Engineering, Missouri University of Science and Technology, Rolla, where he is currently a Faculty Member in the EMC Laboratory. His research and teaching interests include electromagnetic compatibility in power electronic based systems, electronics, and antenna design.

19620 Hale Ave
Morgan Hill, CA 95037

IEEE

SCV EMC 2013 Mini-Symposium October 17

featuring:

Lee Hill

and

Prof. James Drewniak

IEEE EMC SOCIETY

Santa Clara Valley

Biltmore Hotel
2151 Laurelwood Road
Santa Clara, CA 95054

Web: www.scvemc.org

Registration, Exhibits and Continental Breakfast: 7:00 AM

Morning Session: 8:30 AM – 12:00 PM

Presenter: Lee Hill, SILENT

Module 1:

Top Ten Features of Ferrites for EMI Reduction

High frequency ferrites seem simple but are actually widely misunderstood. In new electronic designs the best ferrite for a specific application is often not chosen, resulting in unnecessary cost or ineffective noise filtering. This interactive session will review the key attributes of ferrites intended for use on printed circuit boards and cable assemblies, and how to choose the right one for your design. Lee will present data sheets and actual applications for the control of emissions and immunity, and demonstrate the performance of different ferrite devices using digital noise sources and a spectrum analyzer/test receiver.

Break and Exhibits 10:00 AM – 10:30 AM

Module 2:

Bad PCB Applications Notes on EMC, and What They Did or Can Do to Your Design

When the EMI design notes you receive from the component vendor are faulty, a noise problem will almost always be created in your product design. In fact, SILENT often discovers that bad EMI design guidelines are the root cause of many noise problems that we find while working with clients on design reviews and hardware troubleshooting assignments. In this presentation, Lee will review real-life examples of defects in schematics and PCB layouts that created noise problems in physical hardware.

Lunch and Exhibits 12:00 PM – 1:30 PM

Afternoon Session: 1:30 PM – 5:00 PM

Presenter: Prof. James Drewniak, Missouri University of Science and Technology

Power Distribution Network Design in Multi-layer PCBs

Part 1 - Physics and Concepts

Fundamental concepts and physics that characterize and describe the design, performance, and limits, as well as the inductance physics and calculations that dominate the PDN performance will be presented. The outcome will be the reduction of a real production board with in excess of 20 layers used as an example, to a straight-forward physics-based equivalent circuit model where the model elements are directly related to the geometry. Then the design performance through the frequency domain PDN impedance and its accompanying time-domain voltage ripple can be related directly to the circuit elements in the model. Through this paradigm of relating the geometry features to the model topology and elements, and relating the time-domain and frequency-domain responses to the elements, both steps in a 1-to-1 fashion, a PDN design approach and trade-offs becomes clear.

Break and Exhibits 3:00 PM – 3:30 PM

Part 2 - Design Methodology

Target impedance and its time-domain manifestation in voltage ripple on the PDN will be reviewed and specified for the production board example of Part 1. Then, specifying the PWR net and its adjacent GND return layer, as well as decoupling capacitor number, value(s), and location will be detailed. Trade-offs and limitations will be discussed and quantified.

Reception and Exhibits: 5:00 PM - 6:00 PM

NOTE: The registration fee includes one copy of the technical program, continental breakfast, lunch, refreshment breaks, and the reception at the conclusion of the event. The organizing committee reserves the right to substitute speakers, restrict size, or to cancel the event and exhibition. In the event the organizing committee cancels this event, registration fees will be fully refunded. Individuals canceling their registration prior to October 3, 2013 will receive a full refund. No refunds will be made to individuals who cancel their registration after October 3, 2013. Substitutions are allowed. Attendance is limited. Registration will be confirmed on a first come, first served basis.

Registration Form

Registration Rates:

❒	IEEE Member	$250
❒	Non-Member	$275
❒	Student/Un-Employed*	$100

IEEE Membership Number:_____

$250 for group registration rate (5 or more)

*Full time students only with valid student ID presented on site

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