IEEE SCV-EMC
2019 Mini-Symposium
October 3, 2019

Brought to you by:

Santa Clara Valley Chapter

WELCOME!

Thank you for attending this special one-day Mini-Symposium and exhibition brought to you by the Santa Clara Valley chapter of the IEEE Electromagnetic Compatibility Society.

We hope you enjoy our special guest speakers: Dr. James Drewniak, Doug Smith, Mark Montrose, Sandeep Chandra, Alpesh Bhode and Phillippe Sochoux.

Dr. Drweniak's presentation will focus on 1) concepts and physics; 2) pre-layout method and calculations; and, 3) measurement method. In the past year, we have developed a physics-based approach that makes understanding PI straight-forward, and a means for doing calculations for pre-layout design. Doug S. will have a hands-on demo on how to find the source of the ESD; Mark M. will focus on examining Maxwell's equations in a visual manner; Sandeep C. will bring us to Findings on Radiated Susceptibility ABT (Audio Breakthrough), Alpesh B. and Philippe S. will teach us about New Set of EMC Challenges in Telecommunication Equipment.

The goal of this regional event is to bring technical education to IEEE members, who do not have the opportunity to attend the annual international symposium on EMC or did not have a chance to attend the pertinent sessions during the symposium.

Quite often, travel costs and time away from the office prohibit engineers from attending these large, week long, conferences. Our hope is that you will learn practical information that you can bring back to your work place. This is also an excellent opportunity to ask ono-on-one questions directly to the speakers. There will be vendor exhibits throughout the day, so please visit the vendor booths to find out what solutions they have to offer. The exhibitors will often provide trainings on site or on their campus. Special **THANK YOU's** to those who made this event a big success, including all the vendors, companies, individuals, all volunteers and officers.

There will be vendor exhibits throughout the day so please visit vendor booths to find out what EMC solutions they have to offer. The exhibitors will often provide trainings on site or on their campus.

Special **THANK YOU's** to those who made this event a big success, including all the vendors, companies, individuals, all volunteers and officers.

Please, plan on staying for the reception with our guest speakers, and discussing specific items with Jim D., Doug S., Mark M., Sandeep C., Alpesh B. and Philippe S. after each of the technical presentations. There will be appetizers, wine and beer served during Reception hours and several raffles throughout the day . Enjoy the Mini-Symposium and Exhibition!

Please visit us at http://ewh.ieee.org/r6/scv/emc/index.html (or scvemc.org)

Monthly meetings on the 2nd Tuesday except June/July and August.
Free admission. Locations change, check website for more details.

Schedule of Events

- **Registration, Breakfast & Exhibits: 7:30 AM**
- **Morning Session: 8:30 AM - 12:00 PM**
- **Breaks & Exhibits in the Exhibit Hall + RAFFLE*: 10:00 AM-10:30 AM**
- **Lunch & Exhibits: 12:00 PM - 1:30 PM**
- **Afternoon Session: 1:30 PM - 5:00 PM**
- **Breaks & Exhibits in the Exhibit Hall + RAFFLE*: 3:00 PM-3:30 PM**

• Reception & Exhibits in the Exhibit Hall + RAFFLE*: 5:00 PM - 6:00 PM

*RAFFLE: Each attendee is entered in the raffle. To earn additional tickets, fill out the Bingo Card, answer the questions and have the Vendors sign it. For each 3 vendors, you earn an extra ticket to be redeemed from any of the staff members. The more answers you get, the more winning chances you get.

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		Chuck	Bishop					

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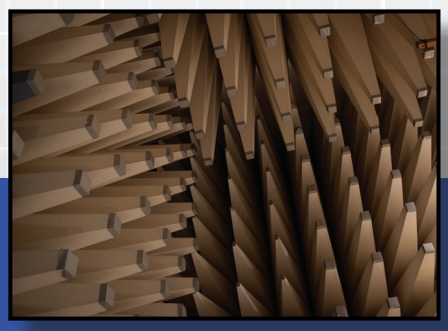

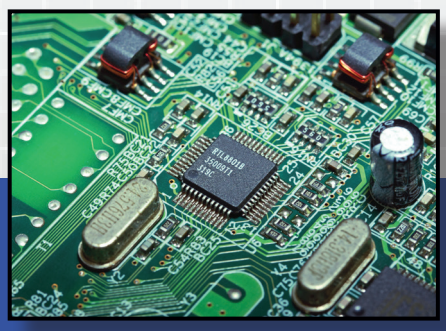

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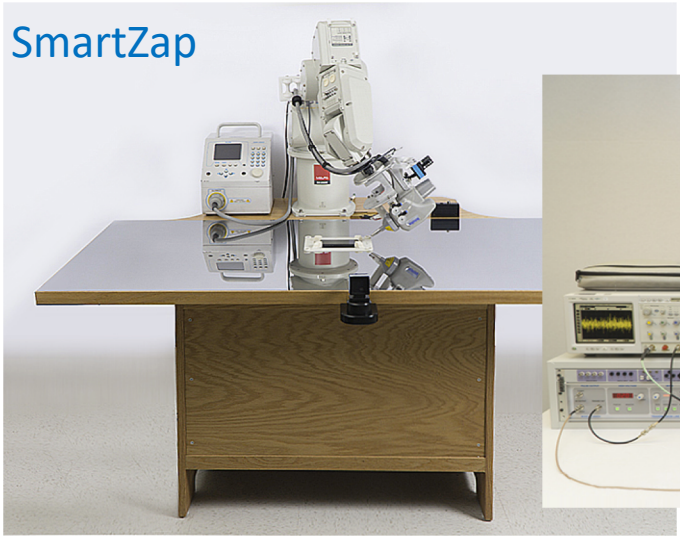

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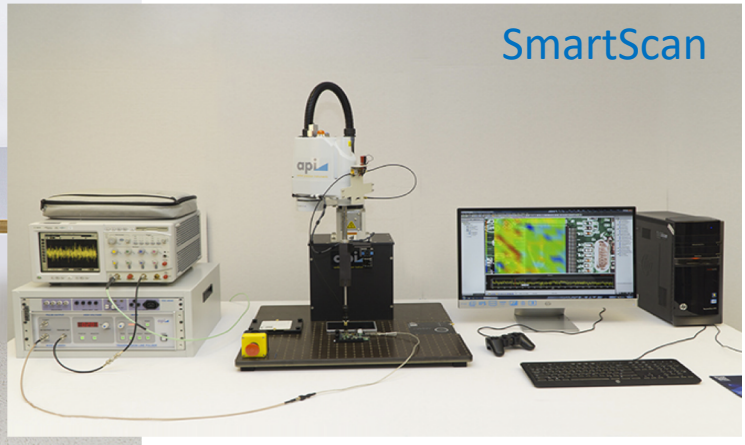

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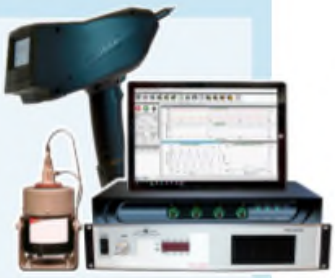

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Power Integrity for High-Speed Design on Multi-Layer PCBs

Concepts and Physics

James L. Drewniak

Clear Signal Solutions and

Missouri S&T EMC Laboratory

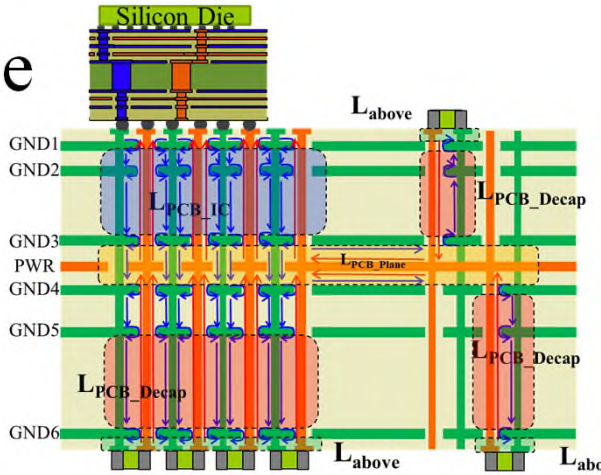
james.drewniak@clearsig.com

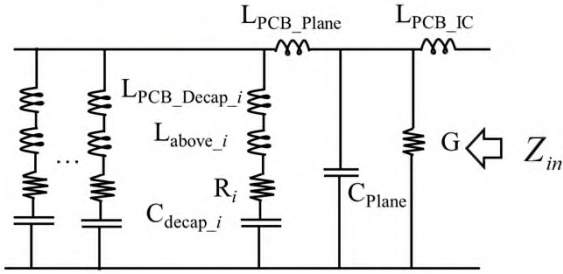
Contributors

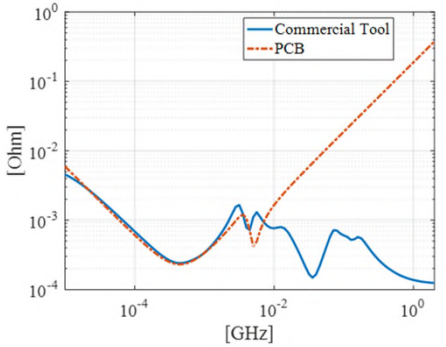
- IBM – B. Archambeault, S. Connor, M. Cocchini, W. Becker, M. Cracraft, A. Ruehli
- Cisco – B. Achkir, S. Scearce, Q. Gaumer, M. Sapazhnikov
- Missouri S&T – B. Zhao, S. Bai, S. Liang, X. Zhu, K. Shringapure, S. Pan, J. Xu, J. Fan

PI Module Overview Part 1 – Concepts and Physics

- The PDN problem
- Noise on the PDN and an FPGA example
- PDN design considerations
- A couple of preliminary concepts
- Current and inductance physics
- A reduced order circuit model from a first principles formulation
- Characteristic Z_{PDN} and relationship to physics
- Understanding PDN physics and design through examples
- Identifying limiting physics in design
- Adding decoupling capacitors

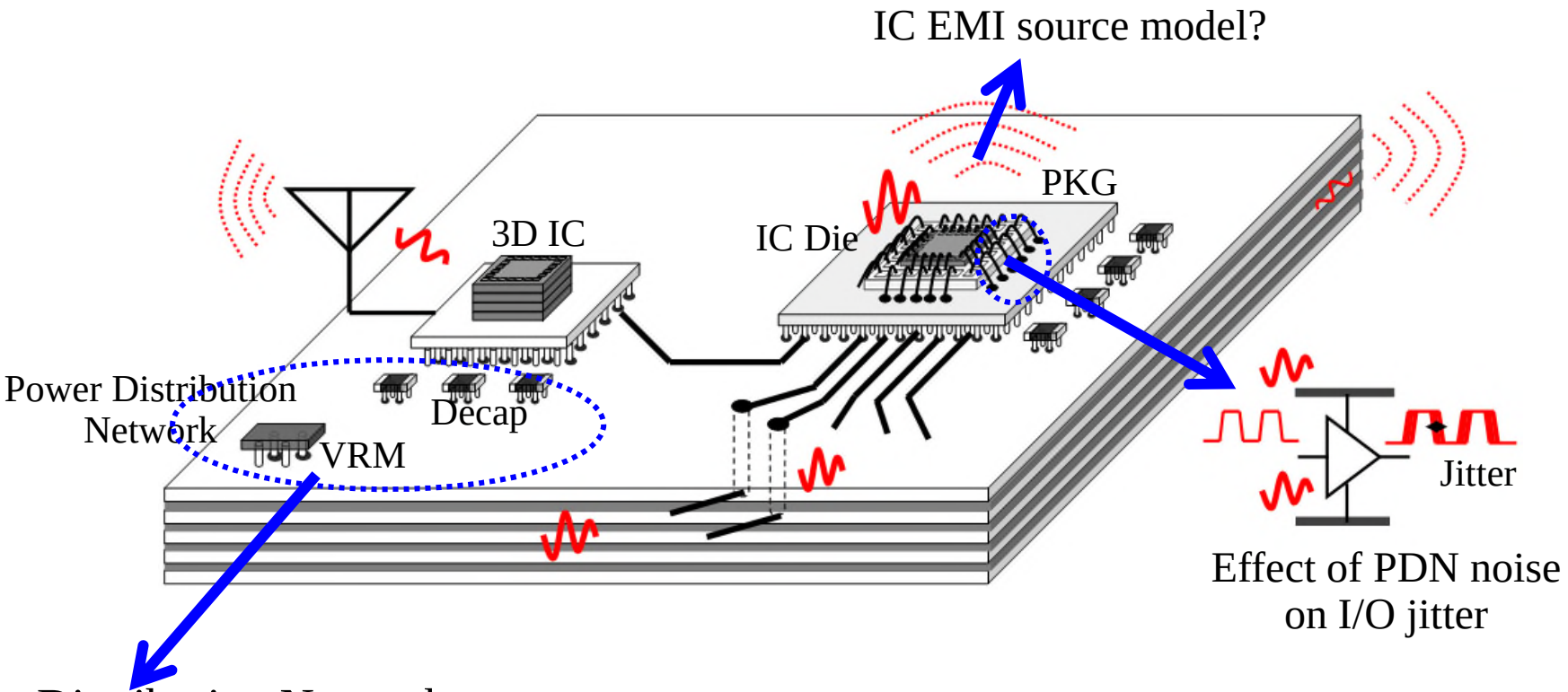






PDN Problem

High-speed, integrated, and mixed electronic system



Power Distribution Network

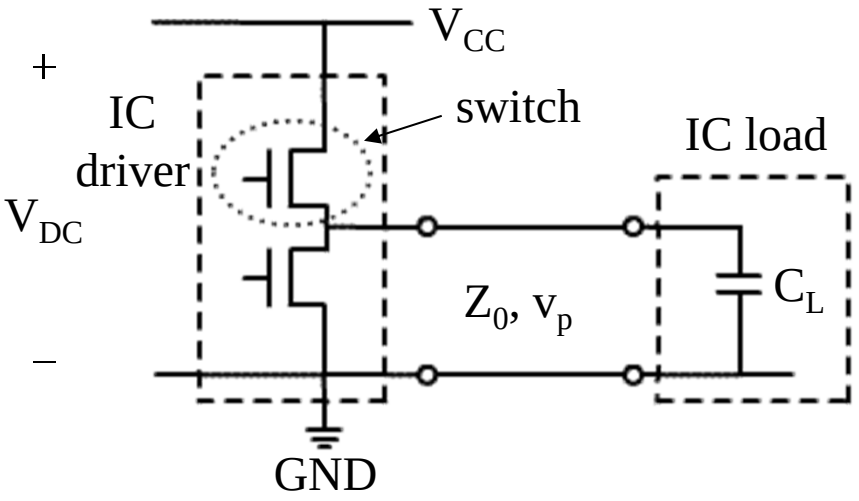
- VRM
- Decoupling capacitors
- Power net area fills

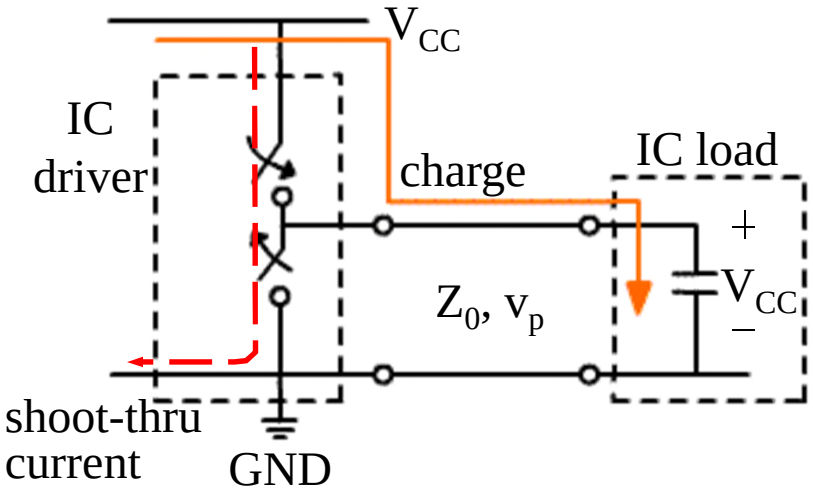
Logic Transitions and Current Draw

Shoot-thru current (and everything else we can't account for)

Load charging current

Load discharge current





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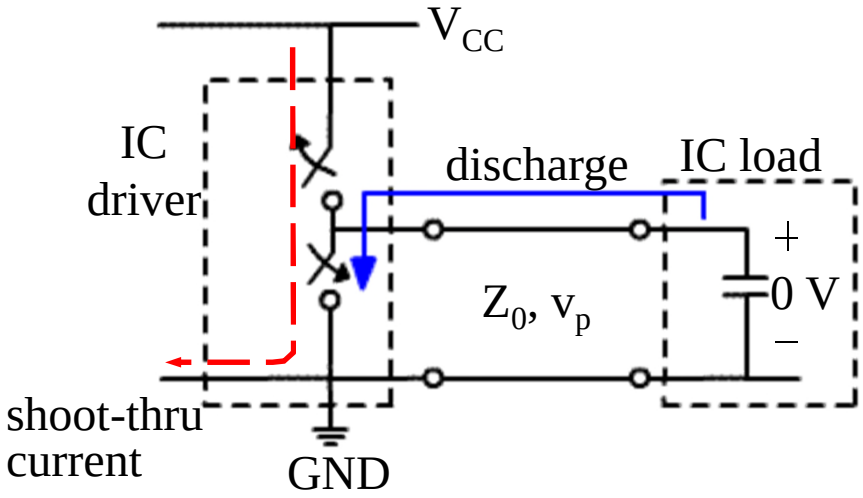
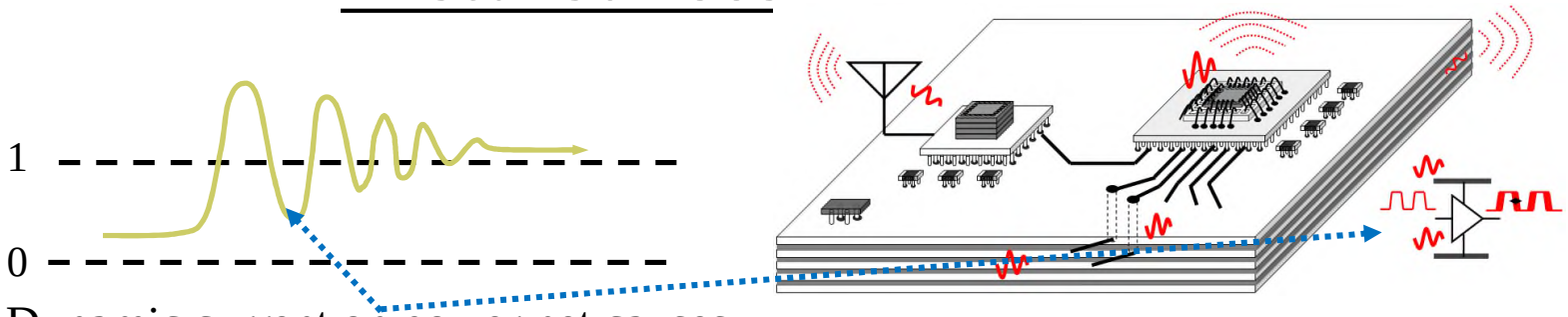


HI to LO

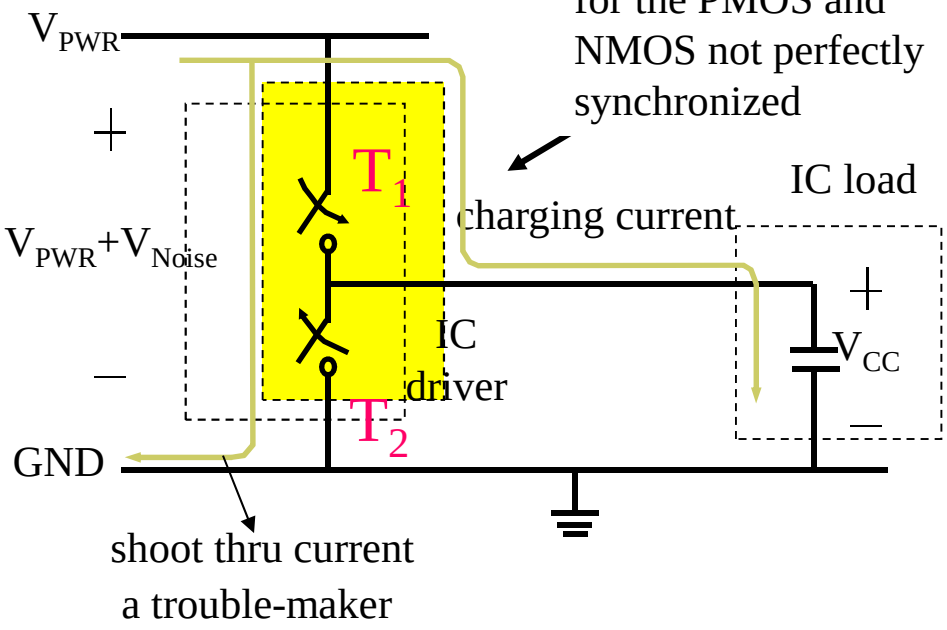
This charge to support IC switching must be provided by the PDN – package, PCB

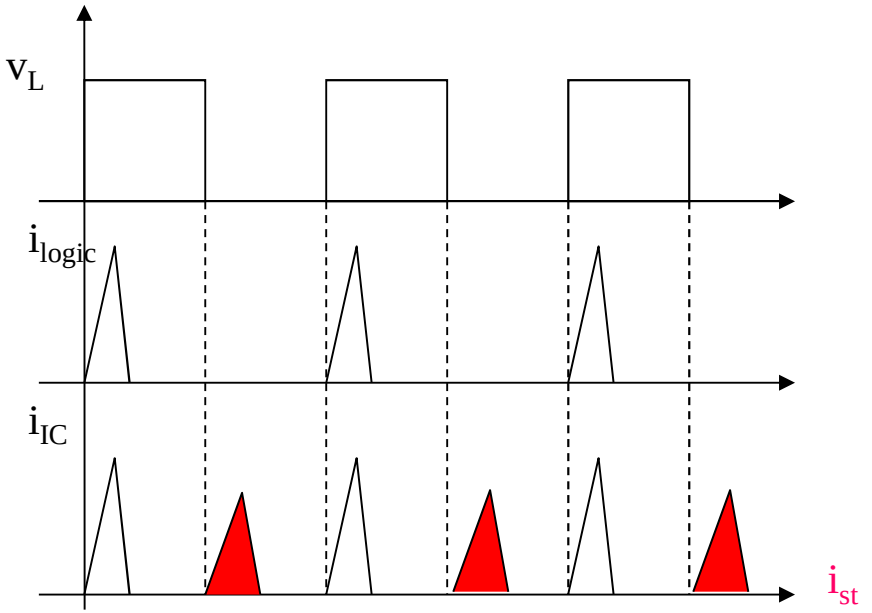
Voltage Switching/Dynamic Current Draw Disturbances



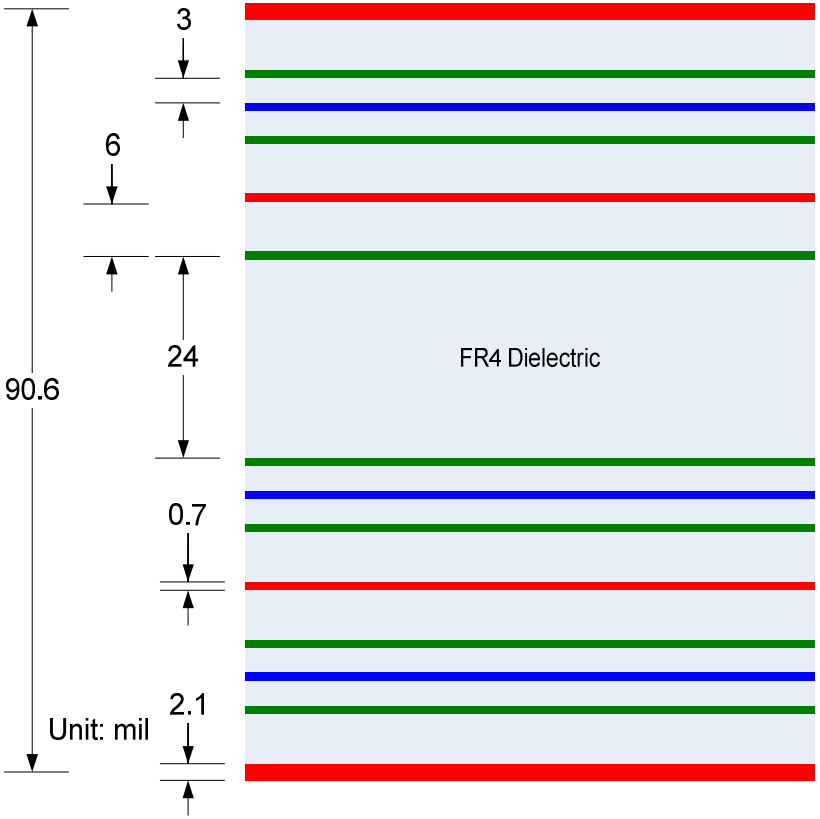
Dynamic current on power net causes disturbance and can lead to faulty switching, a source of jitter, and trouble in general

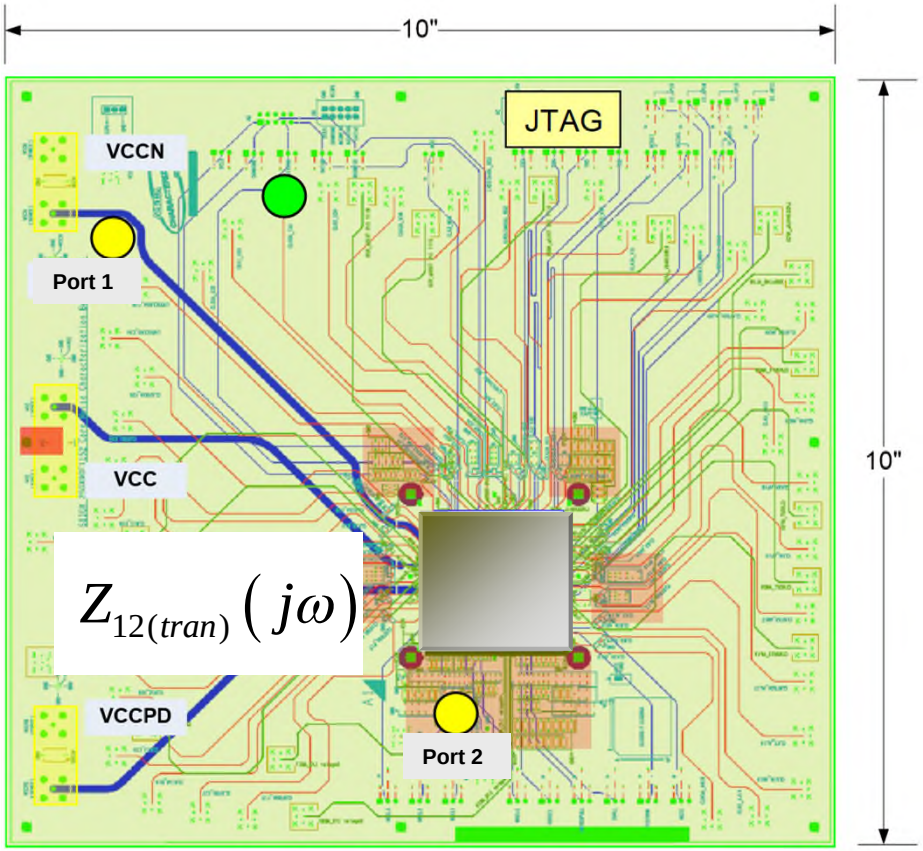
T_1 and T_2 are not simultaneous





PCB for FPGA Core PDN Noise Example

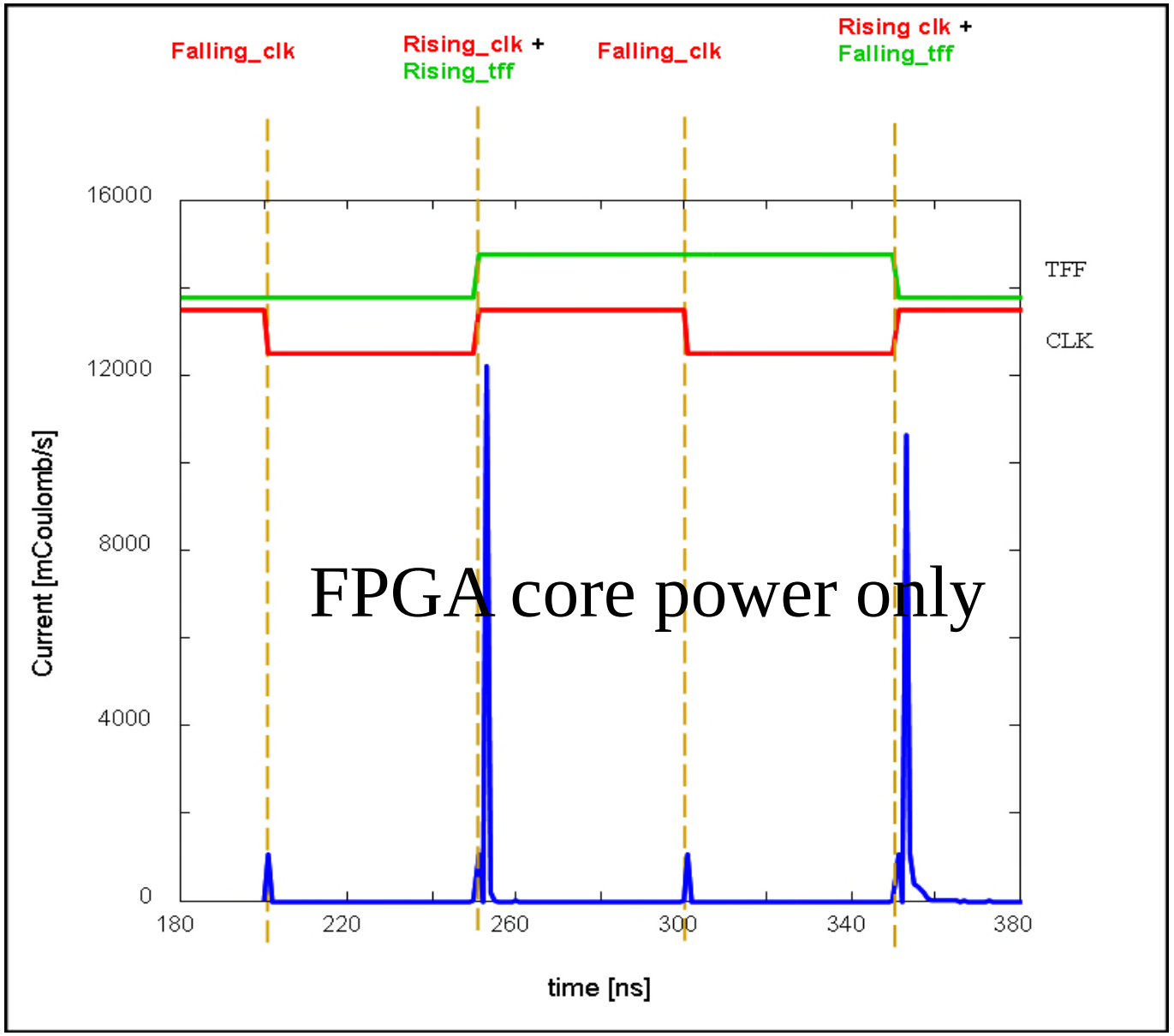




- Power planes: VCC, VCCN, VCCPD
- FR4 dielectric
- Signal layers
- Ground planes

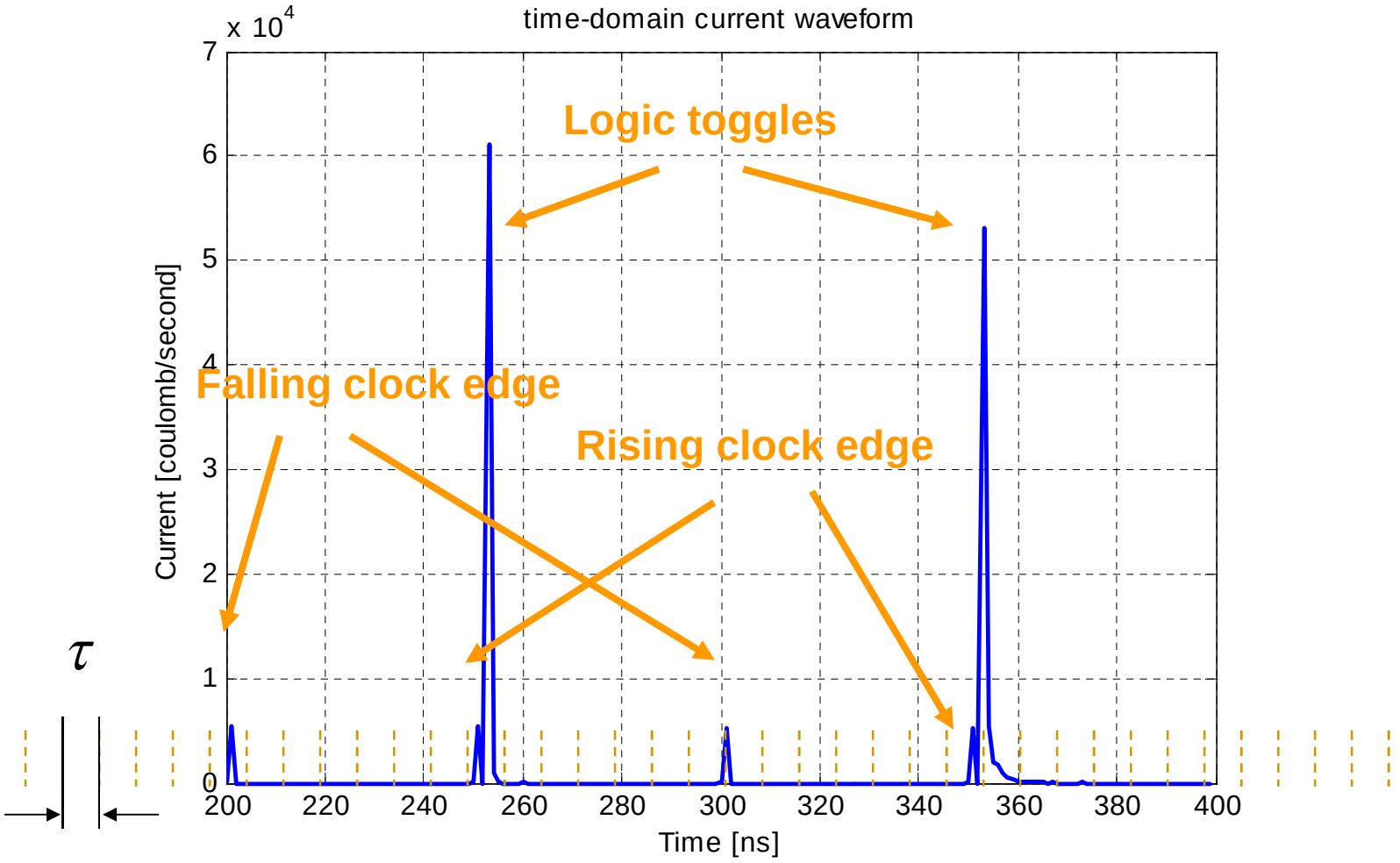
- SMT capacitor pads for 0805, 0603, 0403
- Power Supply BNC connectors (sensing line)
- Bulk Capacitor
- VCC SMA connector
- FPGA dedicated clock input SMA U33
- Port 2 is beneath the FPGA package coax probe

Current Draw and the Logic Waveform



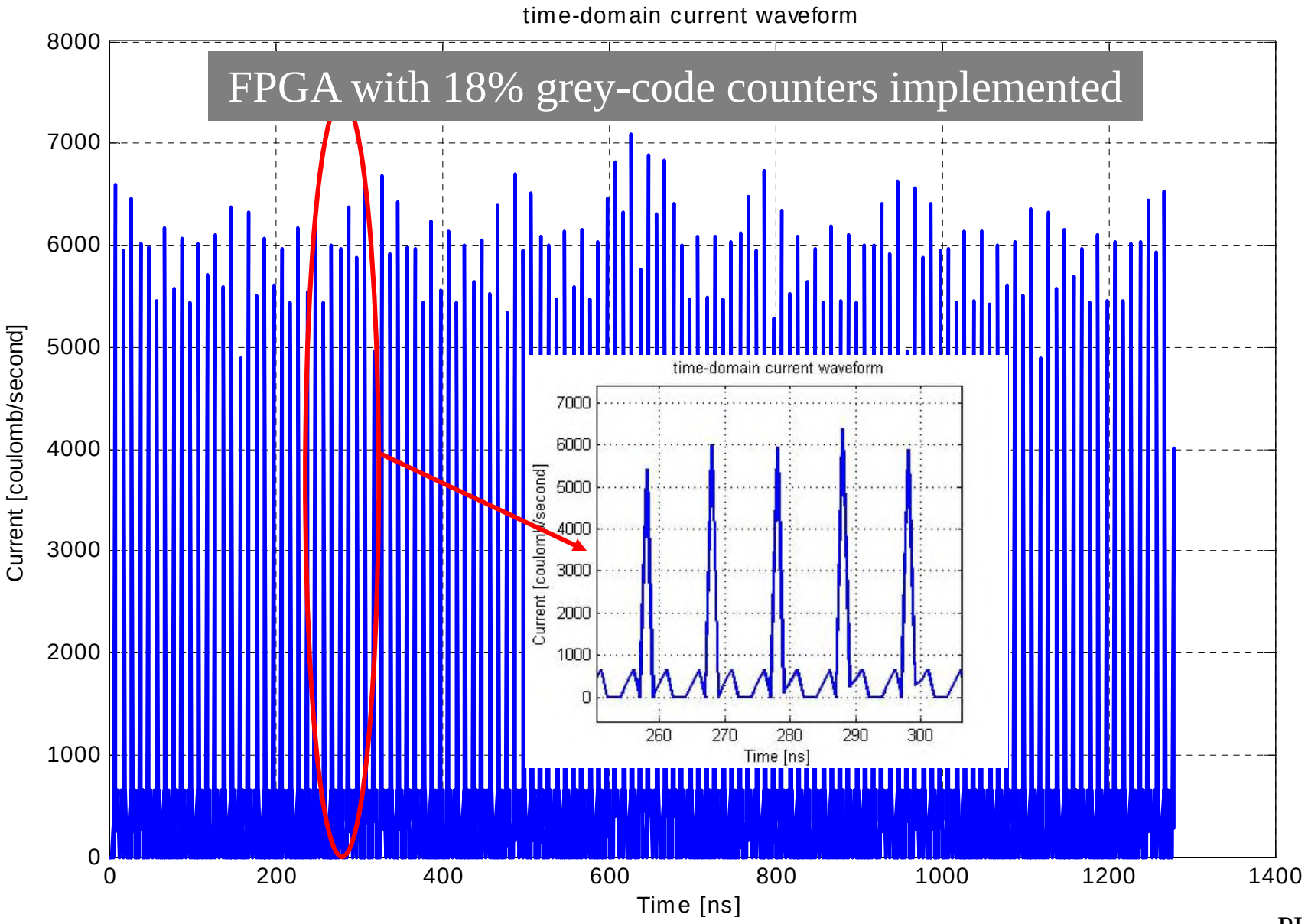
Dynamic Current Profile (calculated)

FPGA Core power only

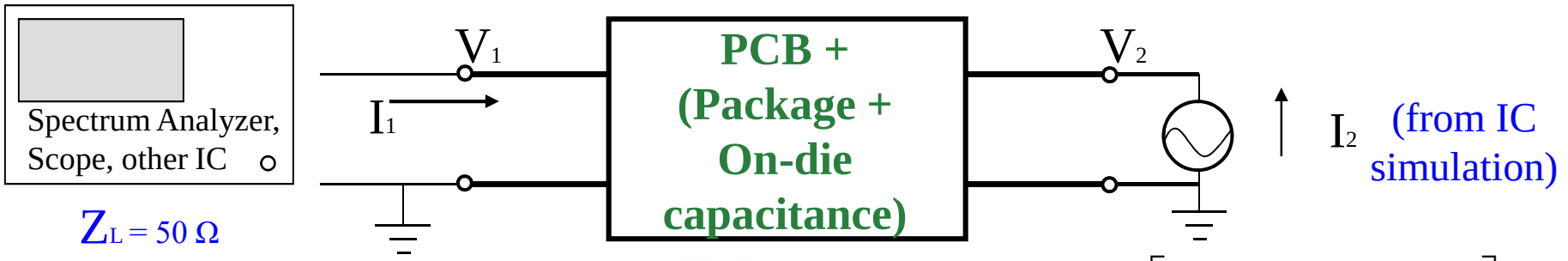


Reconstructed time domain current for a large number of toggle flip-flops

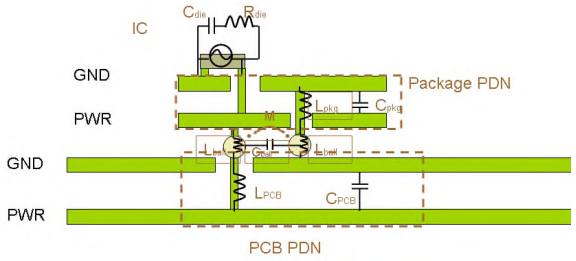
Transient Current Waveform - Simulated



Voltage Disturbance Calculations with Z-Parameters



$$V_1 = -I_1 \times Z_L$$



$$V_2 = \left[Z_{22} - \frac{Z_{21}Z_{12}}{Z_L} \frac{1}{1+\frac{Z_{11}}{Z_L}} \right] I_2$$

PDN impedance IC sees for usual case

For measurement
$Z_L = 50\Omega$
otherwise
$Z_L \rightarrow$ *open circuit*
or impedance into another IC

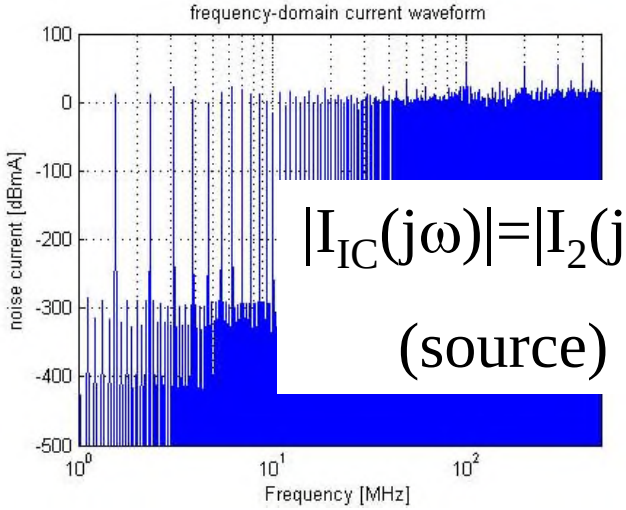
$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \times \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$$

$$V_1 = \frac{Z_{21} I_2}{\left(1+\frac{Z_{11}}{Z_L}\right)}$$

Then the PDN noise voltage is

I_2 is from IC simulation. Z_{21} and Z_{11} are both from impedance simulation (also are calculated from S-parameters from modeling or measurement).

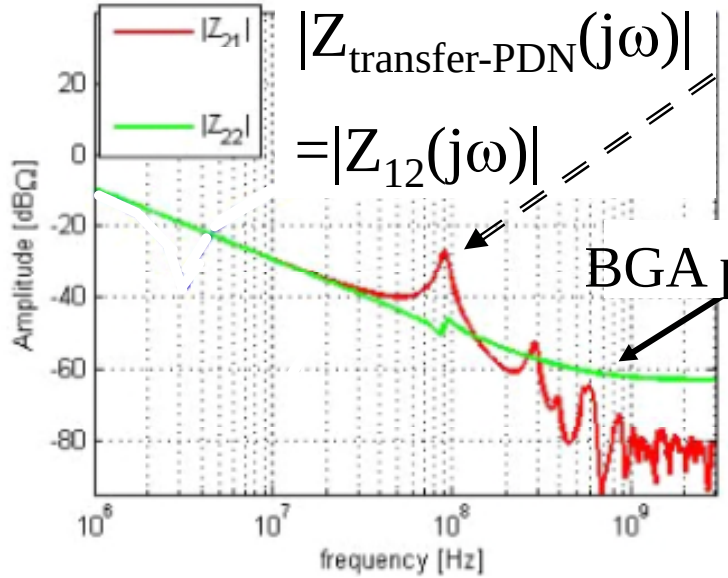
PDN Noise Voltage Spectrum Prediction



$|I_{IC}(j\omega)|=|I_2(j\omega)|$

(source)

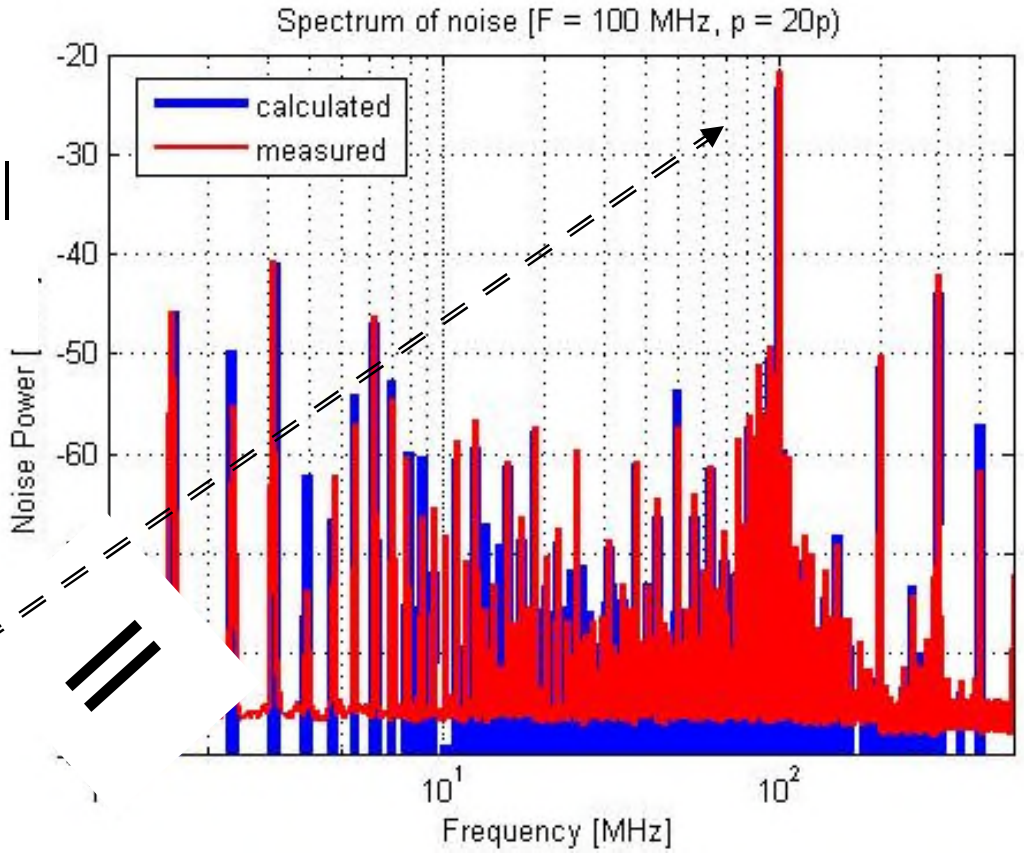
x



$|Z_{transfer\text{-}PDN}(j\omega)|$

$=|Z_{12}(j\omega)|$

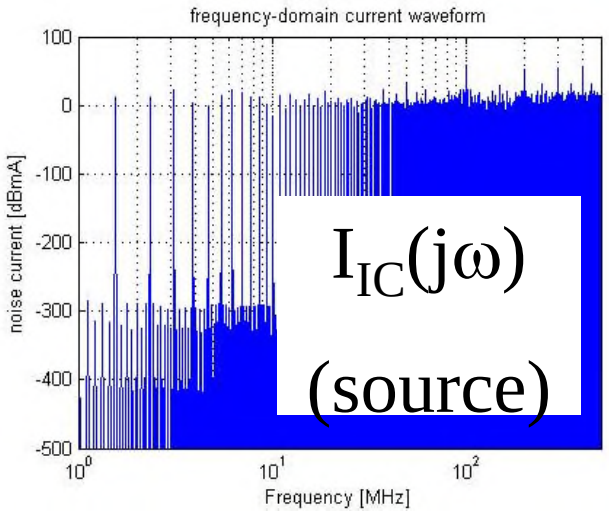
BGA package & IC



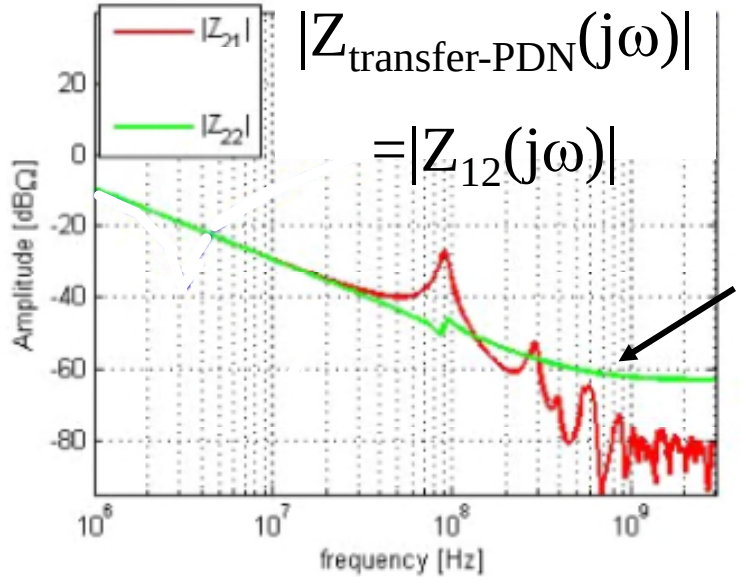
$|V_{PDNnoise}(j\omega)|=|V_1(j\omega)|$

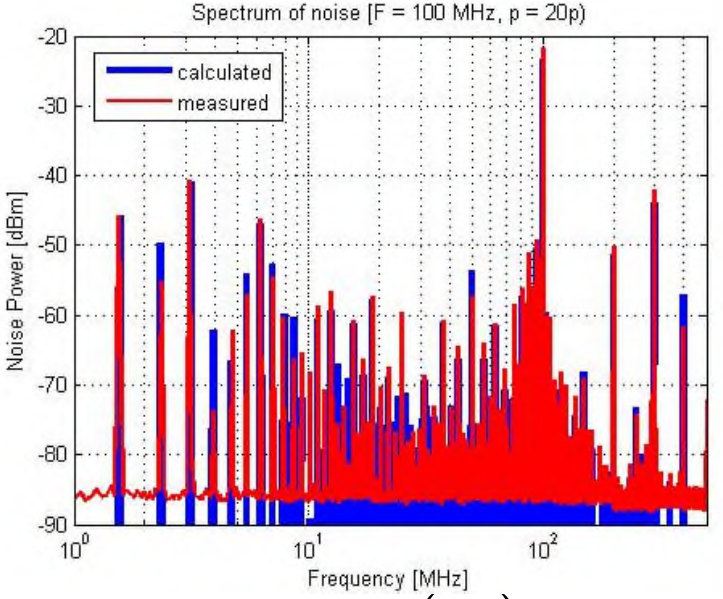
Un-freindly things happen at resonances – lumped or distributed

PDN Noise Voltage from Impedance



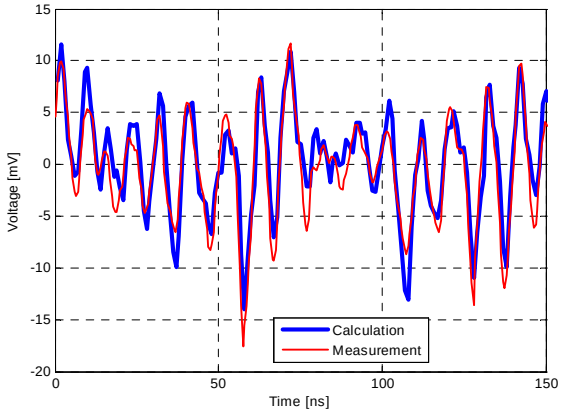
x





$$V_{PDN}(\omega) = Z_{PDN}(\omega) \times I_{IC}(\omega)$$

$$v_{PDN}(t) = F^{-1}\{V_{PDN}(j\omega)\}$$

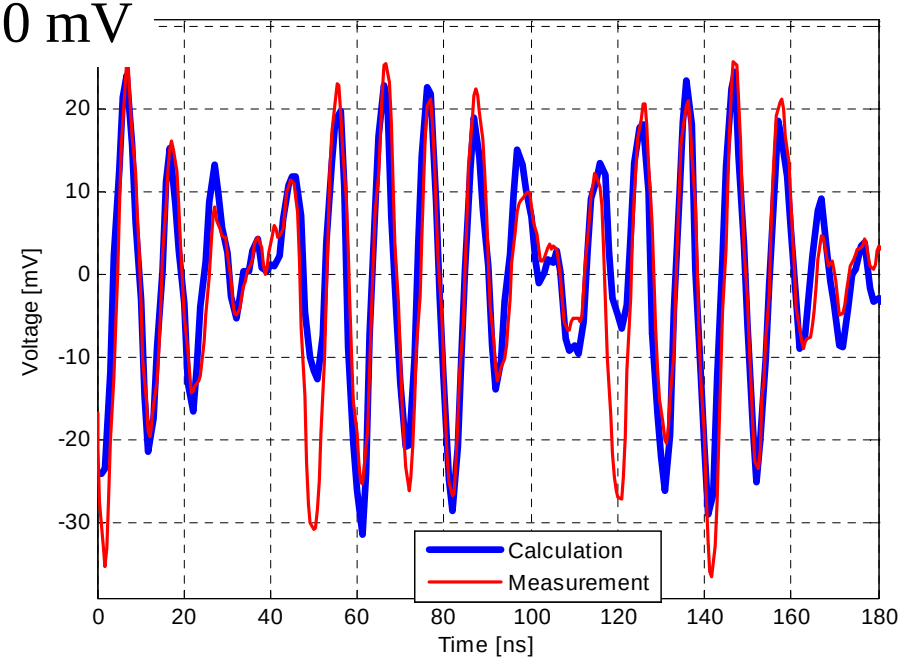


Transient PDN Noise Voltage

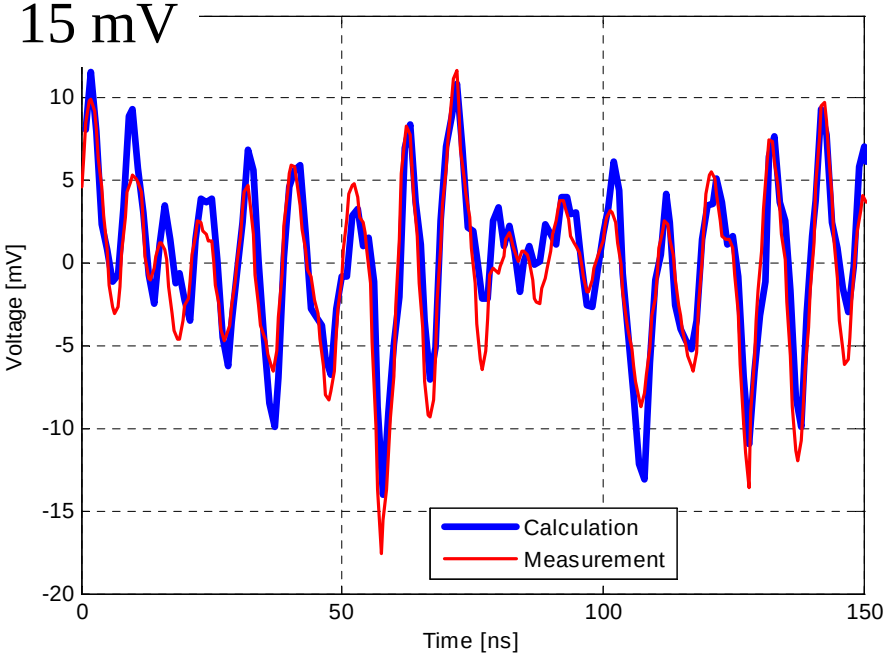
Inverse Fourier Transform to get $v_{PDN}(t)$

$$v_{PDN}(t) = F^{-1}\left\{V_{PDN}(j\omega)\right\}$$

30 mV



15 mV



NO De-Caps

WITH 16 De-Caps

The estimated and measured noise voltage were compared, with a 100 MHz clock input, multi-frequency FPGA configuration, on the bare board and decoupled board.

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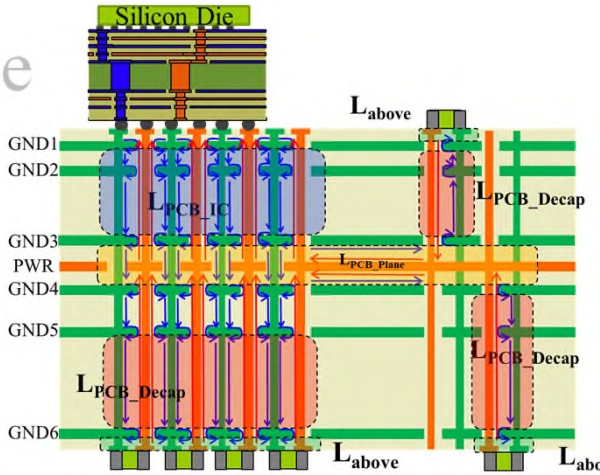
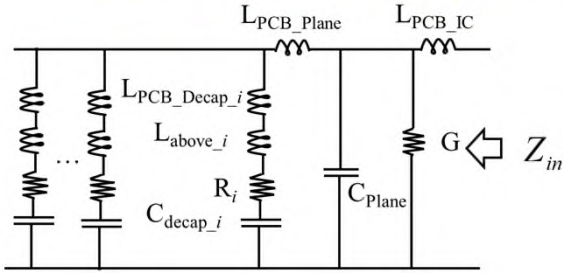
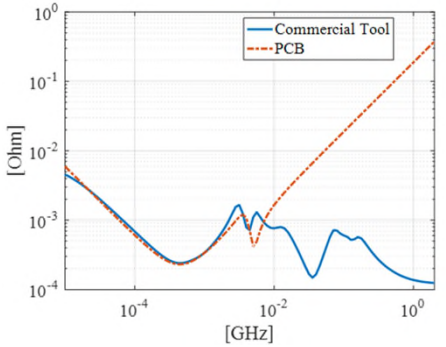
- PDN design considerations
- A couple of preliminary concepts
- Current and inductance physics
- A reduced order circuit model from a first principles formulation
- Characteristic Z_{PDN} and relationship to physics
- Understanding PDN physics and design through examples
- Identifying limiting physics in design
- Adding decoupling capacitors





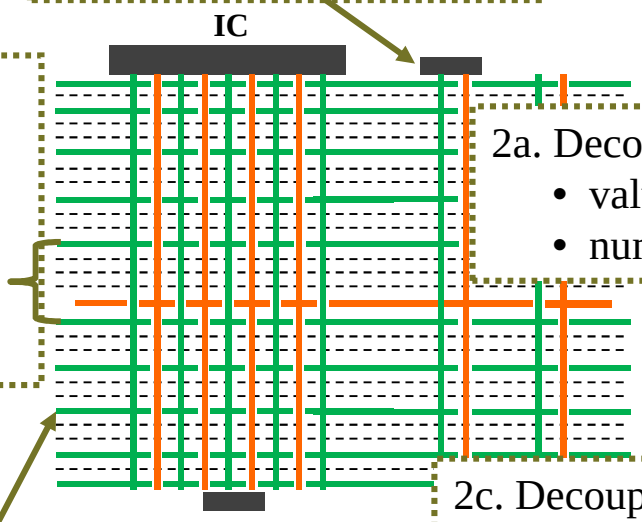


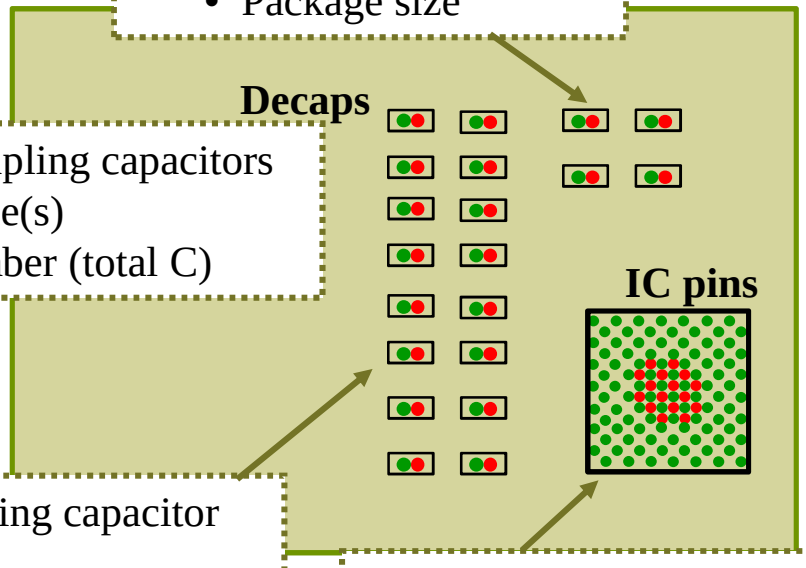
PCB PDN Design Considerations

2a. Decoupling capacitors
- top
- bottom,
- beneath IC?

2b. Decoupling capacitor connection -
- PWR/GND via geometry
- Package size

1. Power net area fill
- location in stack
- spacing to power return plane
- total area fill
- special materials





2a. Decoupling capacitors
- value(s)
- number (total C)

Effect of other ground/reference planes?

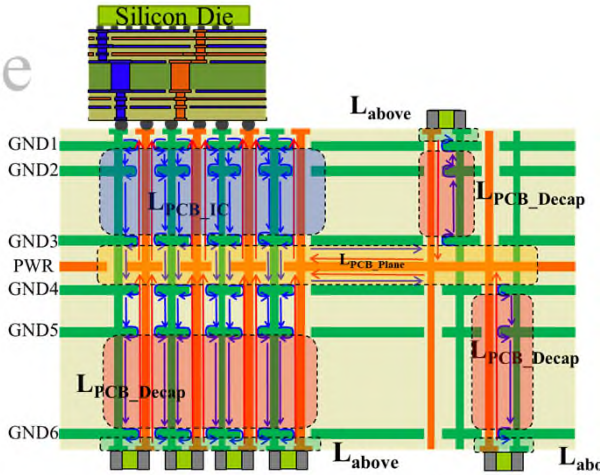
2c. Decoupling capacitor layout
- How close to IC?
- Shape – ring IC, on one side?
- doublet

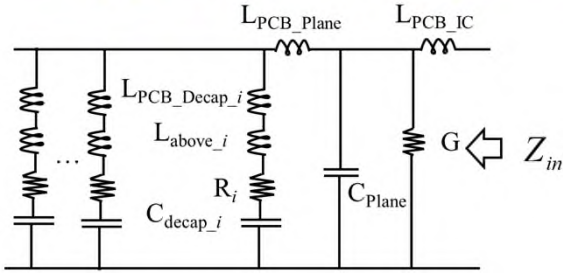
3. IC PWR/GND
- Number pins
- pin pattern
- Pitch
- on-package decaps

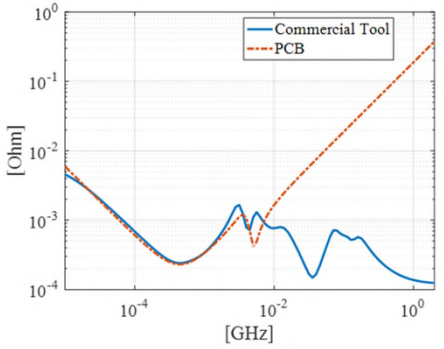
PWR
GND

PI Module Overview Part 1 – Concepts and Physics

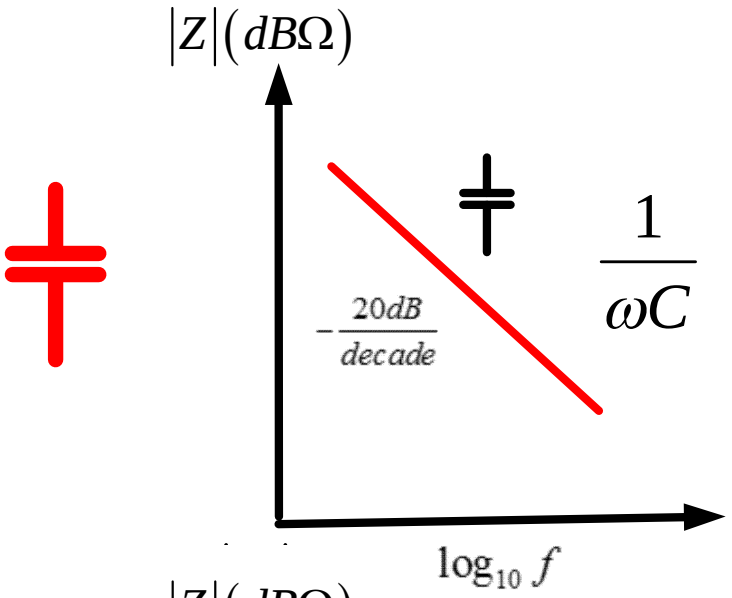
- The PDN problem
- Noise on the PDN and an FPGA example
- PDN design considerations
- A couple of preliminary concepts
  - Responses for RLC circuits
  - High-frequency current path

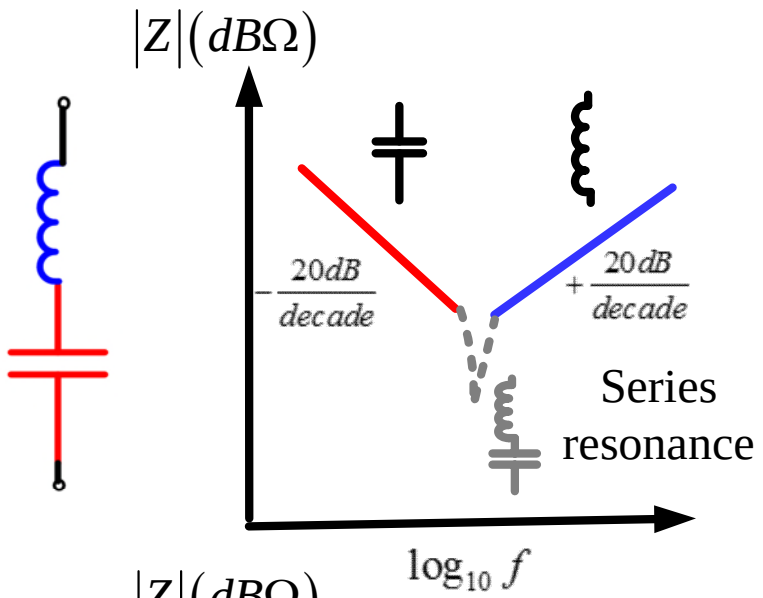


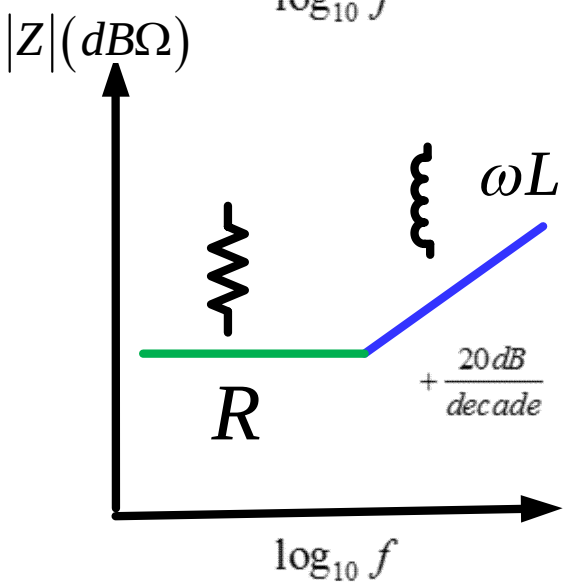


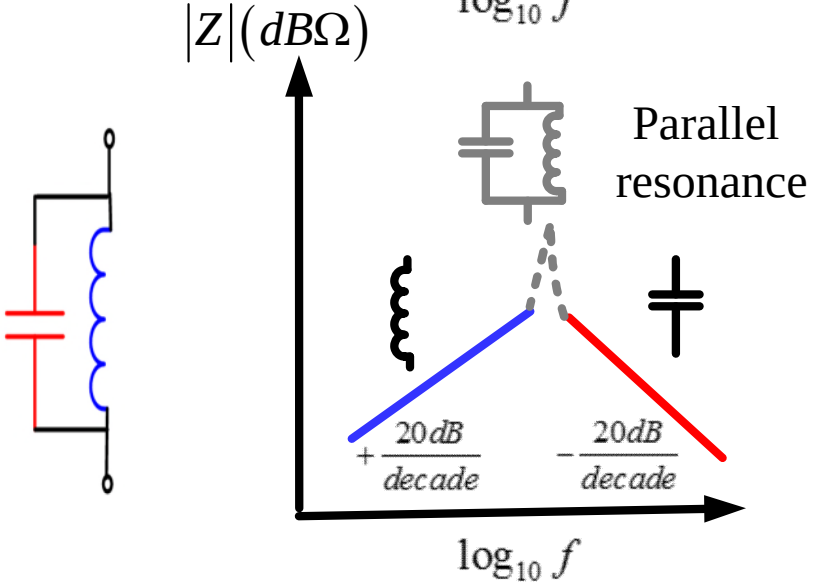


Reminder – Circuit Model Behavior with Frequency





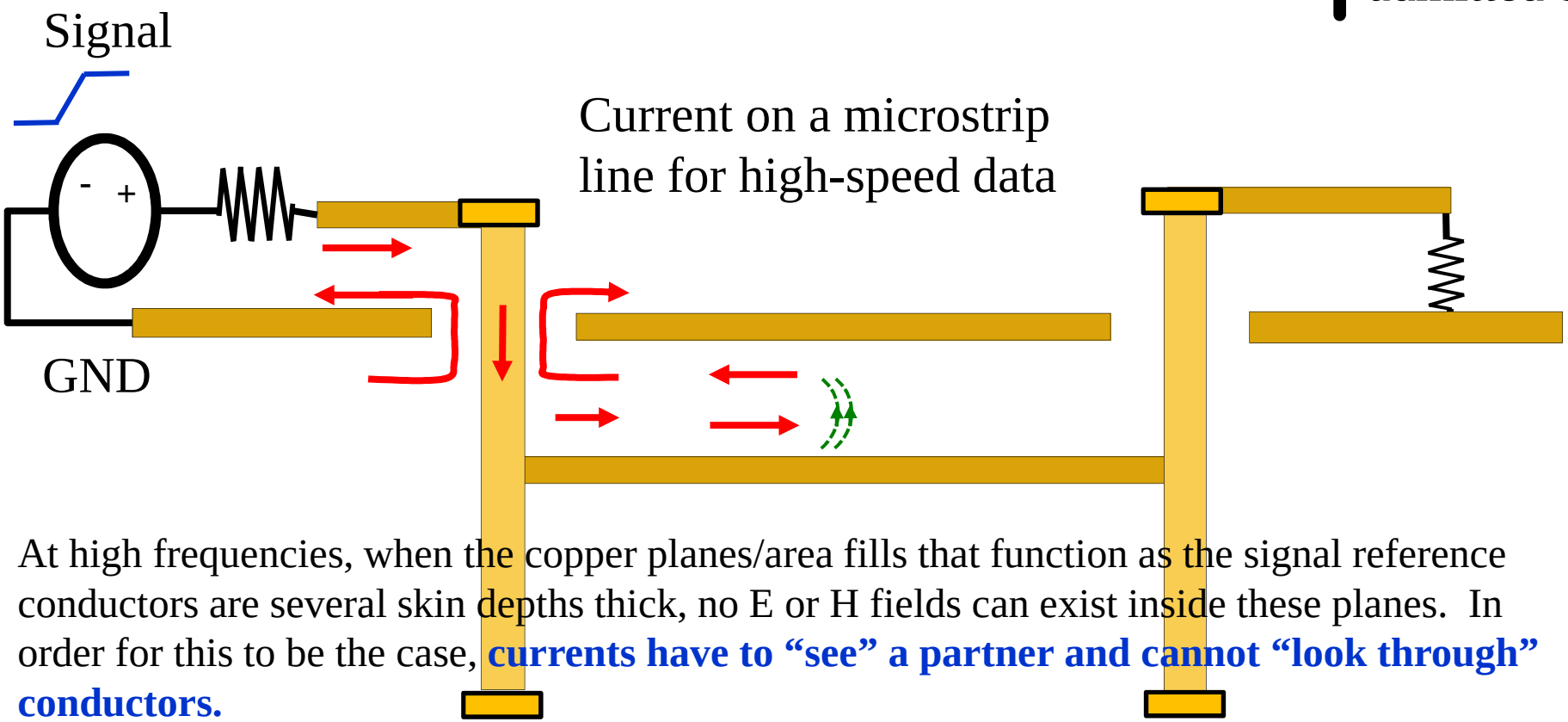




Reminder: Current Behavior

Conduction current – carried by electrons $\vec{J}_{cond} = \sigma \vec{E}$ → impeded by

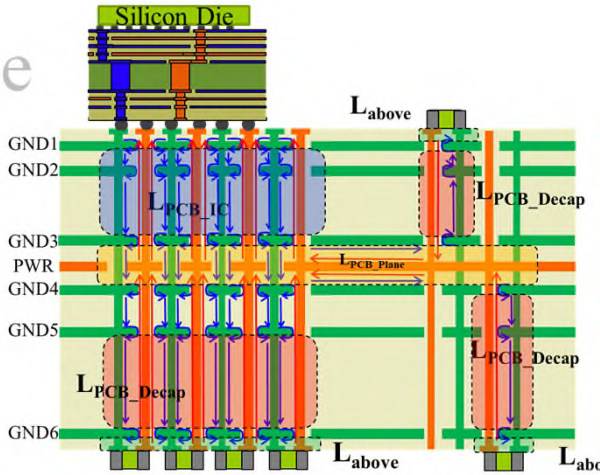
Displacement current – carried by $\vec{J}_{displ} = \varepsilon \frac{d\vec{E}}{dt}$ → admitted by

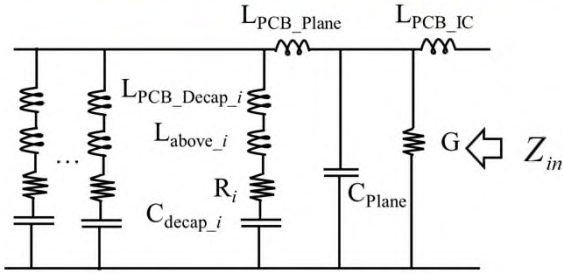


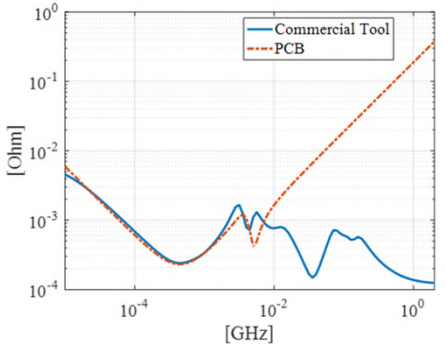
At high frequencies, when the copper planes/area fills that function as the signal reference conductors are several skin depths thick, no E or H fields can exist inside these planes. In order for this to be the case, **currents have to "see" a partner and cannot "look through" conductors.**

PI Module Overview Part 1 – Concepts and Physics

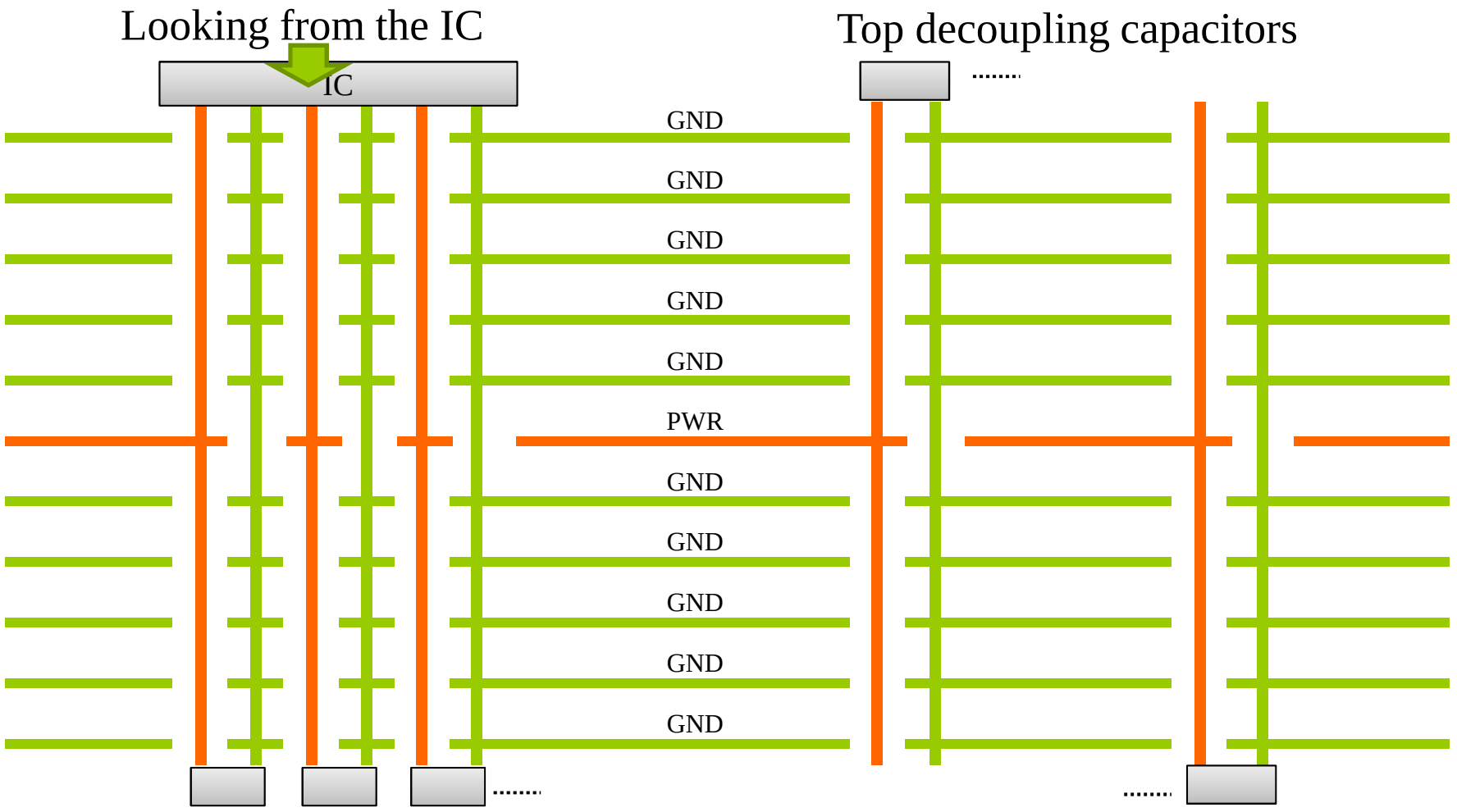
- The PDN problem
- Noise on the PDN and an FPGA example
- PDN design considerations
- A couple of preliminary concepts
- Current and inductance physics
  - Conduction current path through layers (vertical) on PCB PDN and associated inductance
  - Decomposing the inductance into pieces
  - Current path across the power net area fill and the ground power return current







The Objective and Guiding Physics:
Conduction Current Path results in Inductance



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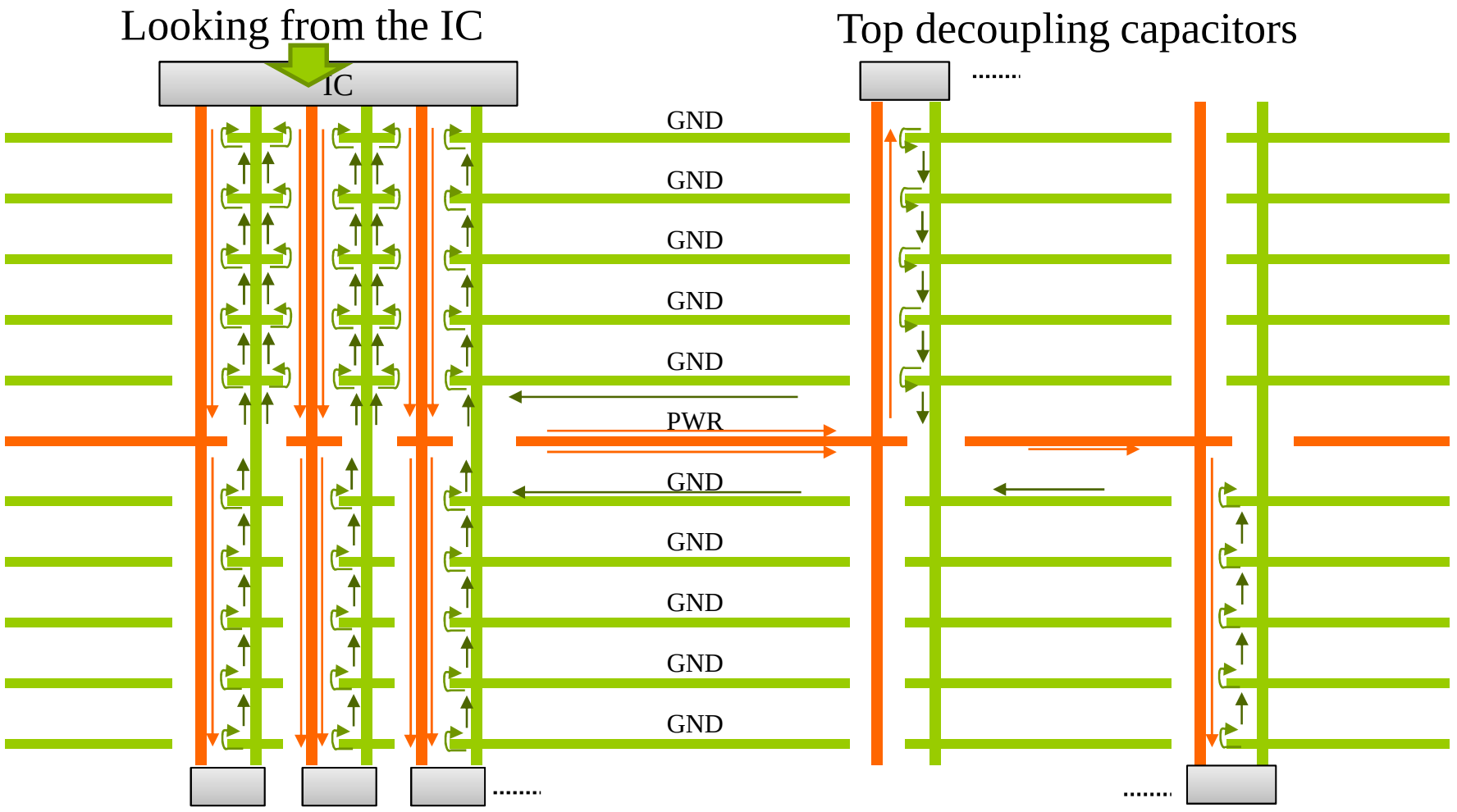

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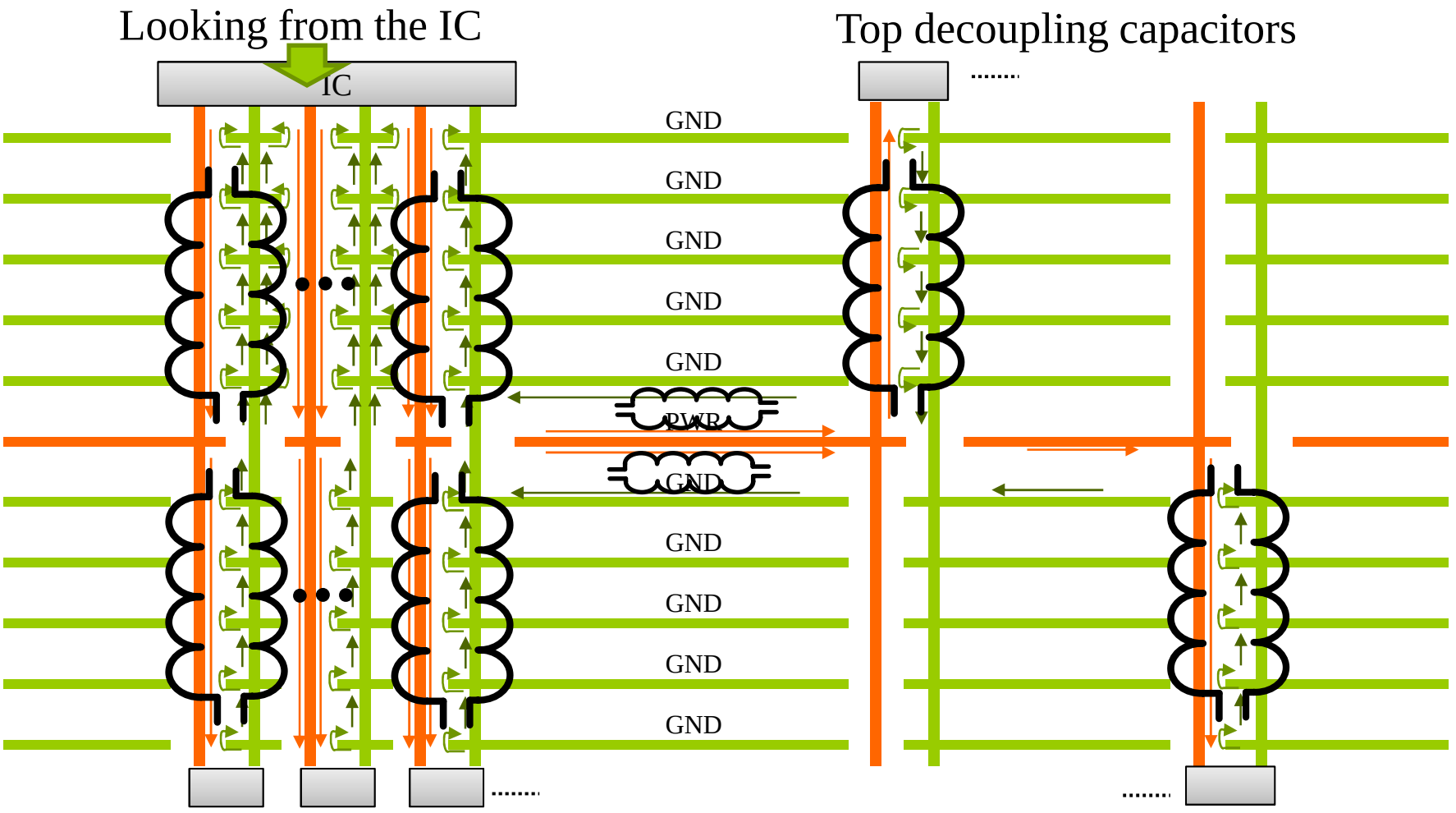
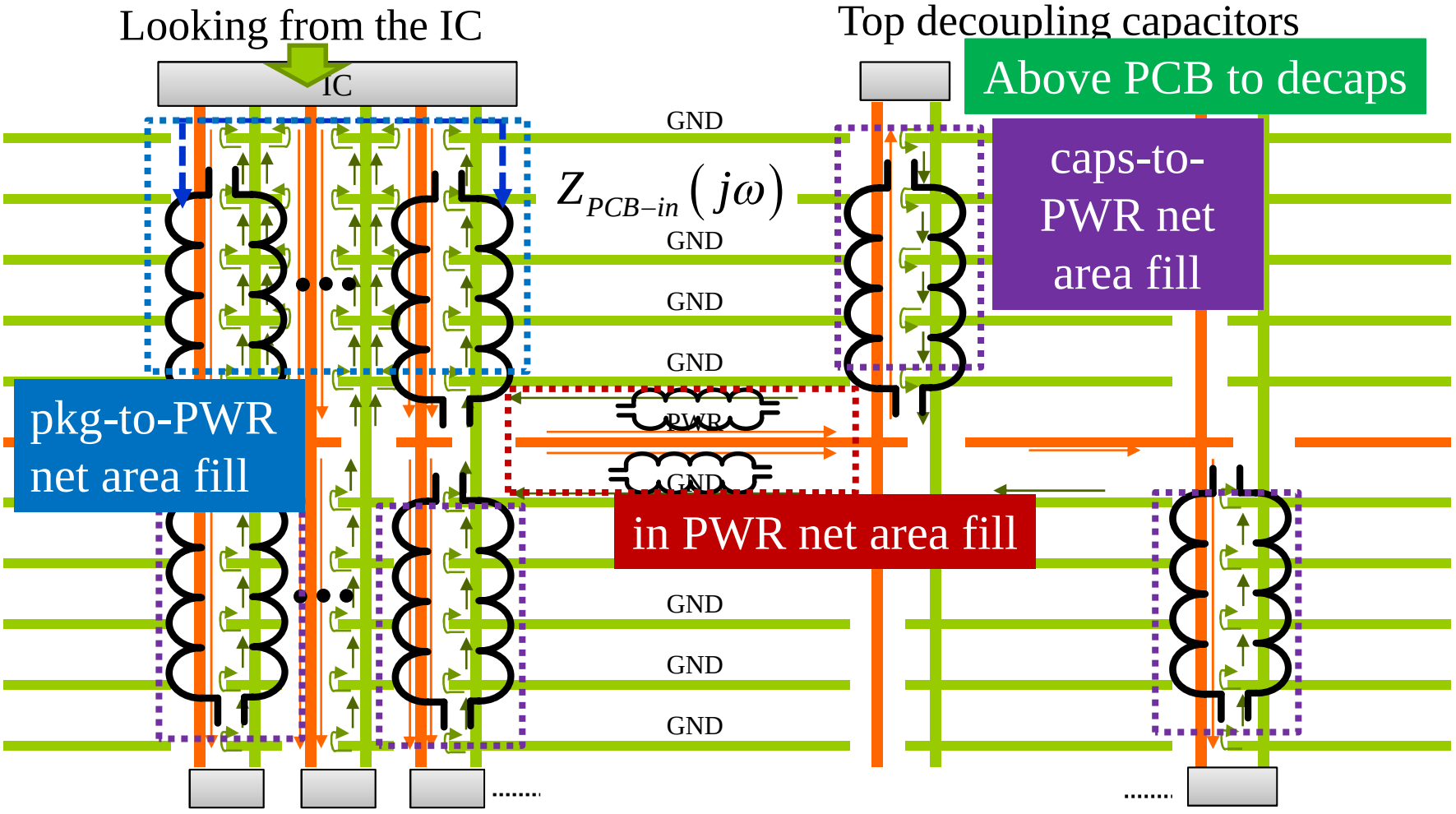
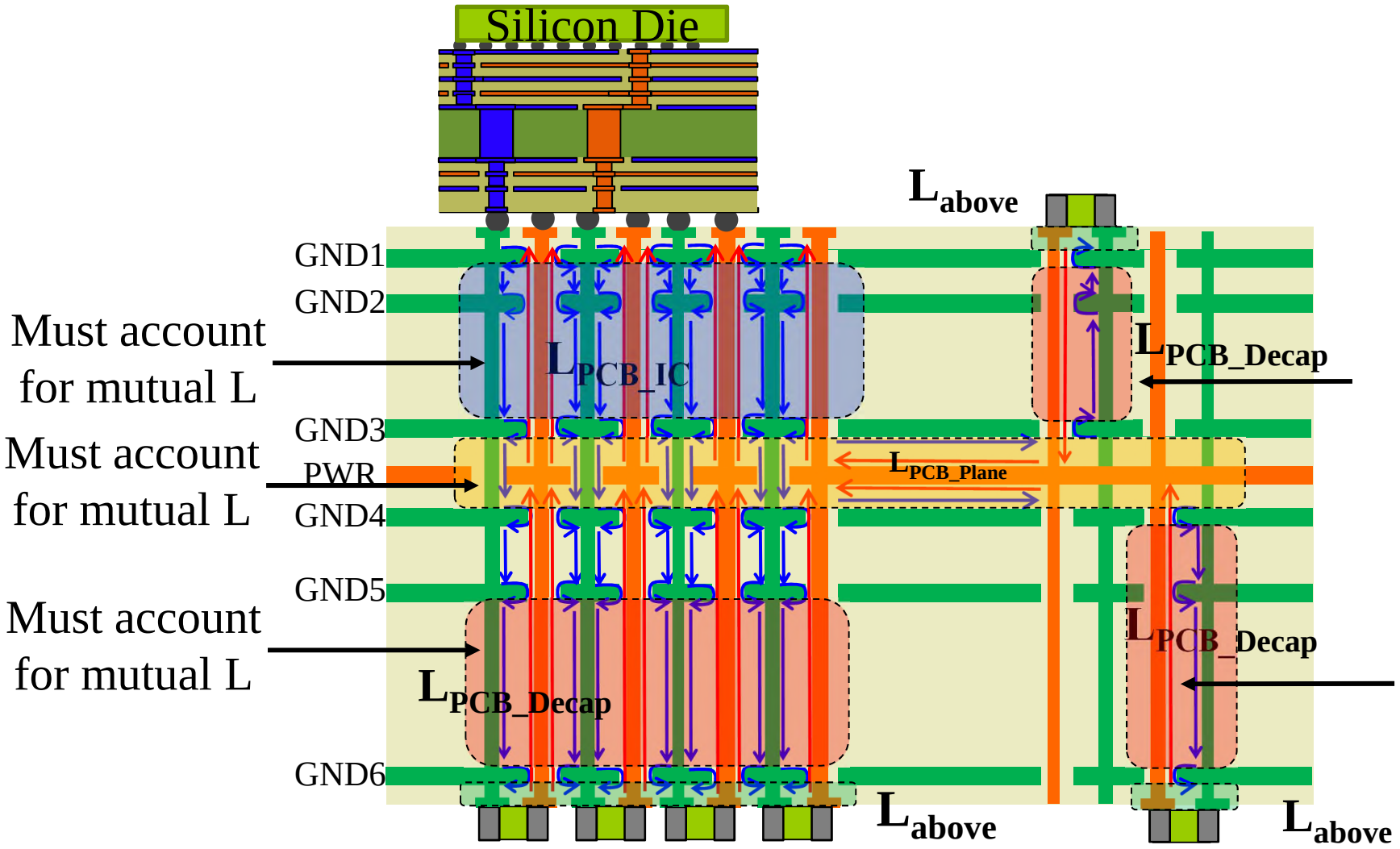


Key Point – Current Path and Inductance

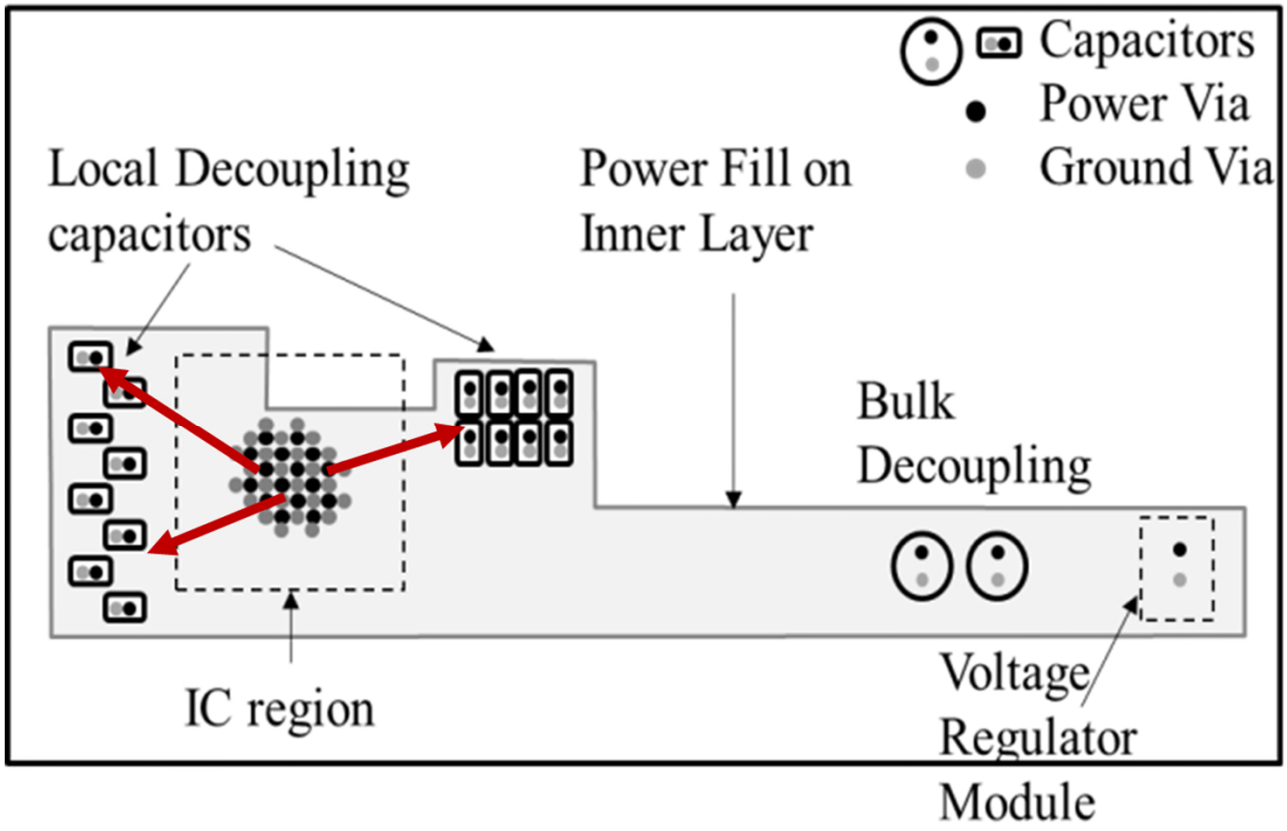
Four contributions (current path pieces) to the Z_{PDN} inductance



Geometry and Inductance Decomposition



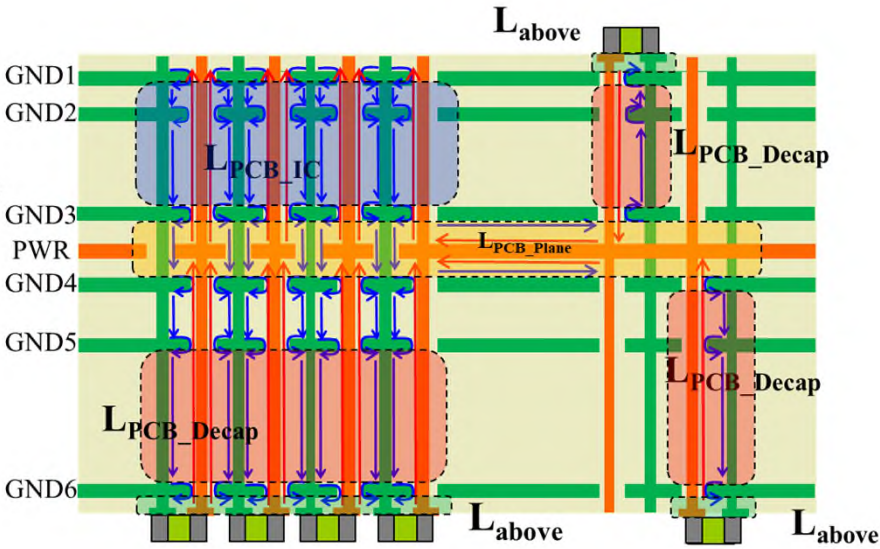
Current Path, and Inductance

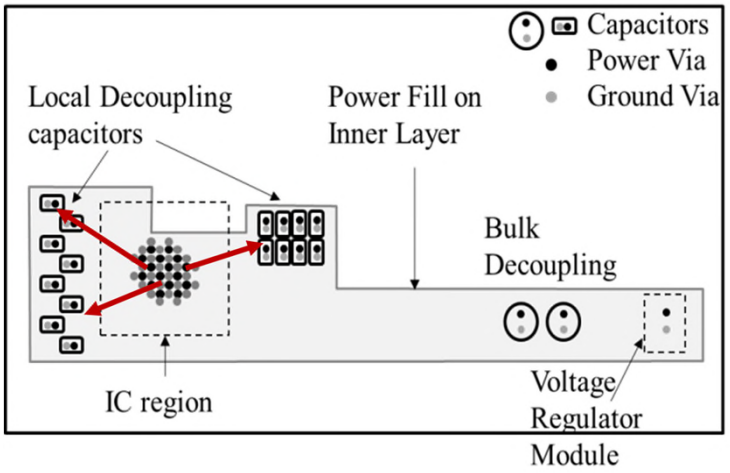


Current path from IC to decaps *in the power net area fill layer* is better to be in line (and not cross cutouts, around corners, etc.). L_{PCB_plane} is increased otherwise.

Key Points

- Production printed circuit boards that use area fills for the power net will have from 4 to over 40 layers. The IC package may have tens to hundreds of vias, and there may be tens to hundreds of decoupling capacitors. The ***complexity is high***, but the ***current path physics*** **are very** ***straight-forward***, though there will be many parallel paths.
- The inductance associated with a current path can be decomposed into four pieces along the path.
- Direct, "line-of-sight" current paths between the IC and the decaps will have less $L_{PCB\ Plane}$ inductance than current paths that cross cutouts, slots, go around corners, etc.





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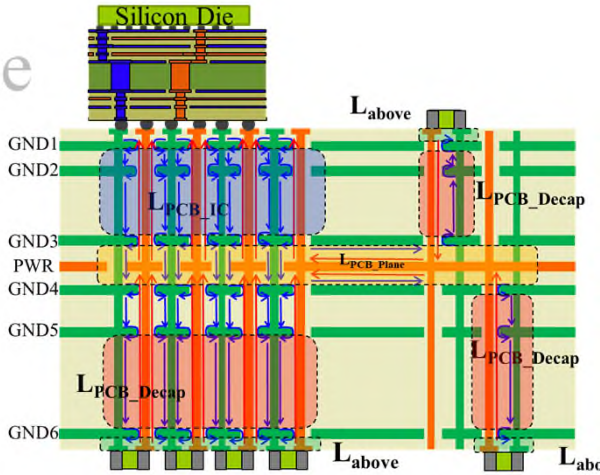
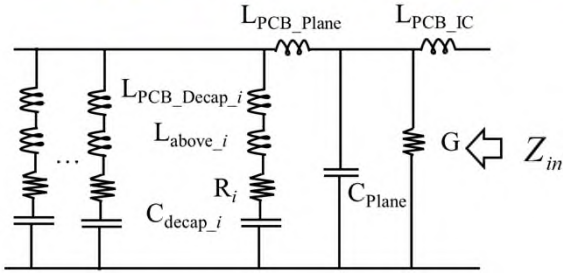
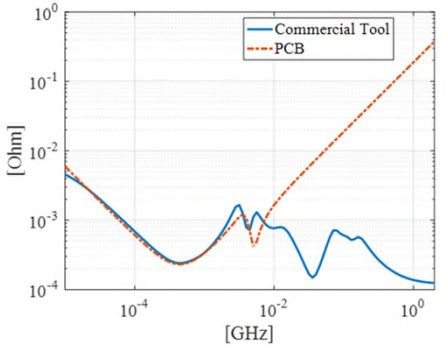
  - Impedance from a Maxwell's equation formulation
  - A many element physics-based model to a reduced order impedance equivalent circuit with inductance related to geometry decomposition

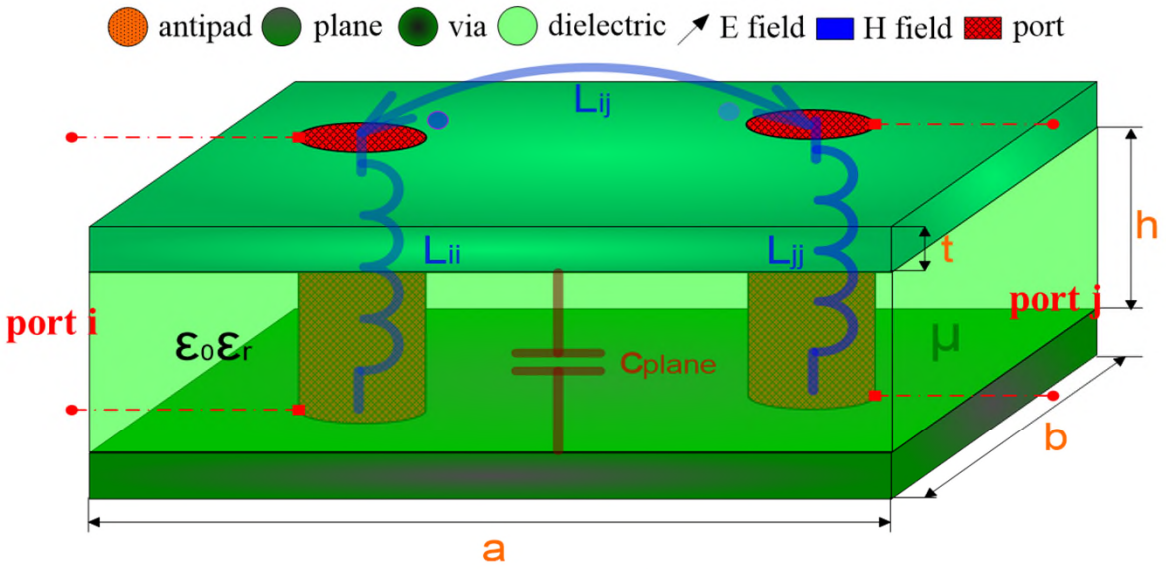






Calculating Inductance from Current Path Physics

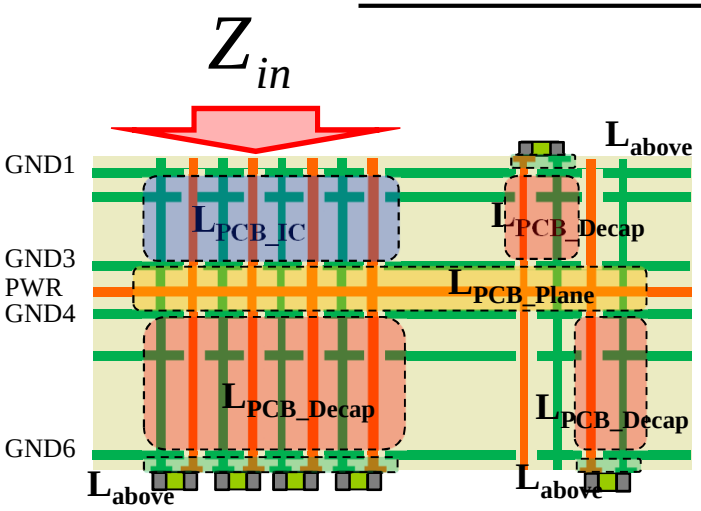
- All current segments in all layers are modeled (often many thousands or tens of thousands) and self inductances for every segment and mutual between segments are extracted using the (first principles) cavity model.
- Self and mutual inductances are included.



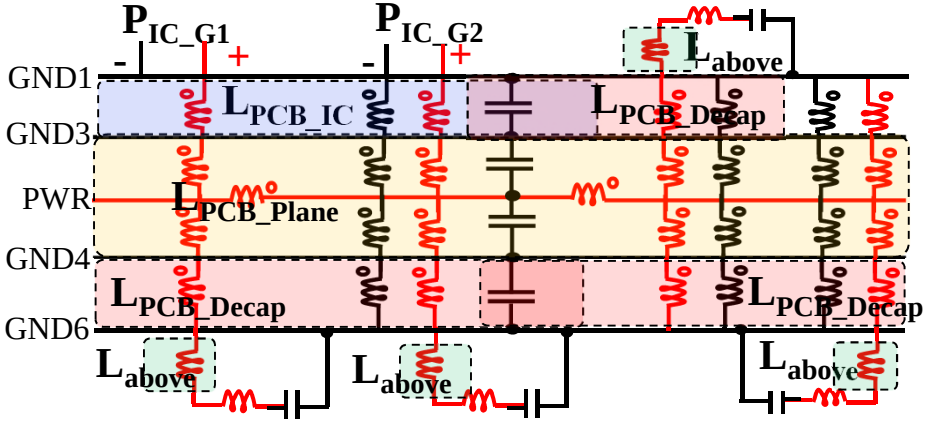
$$C_{plane} = \frac{\varepsilon_r \varepsilon_0 ab}{h}$$

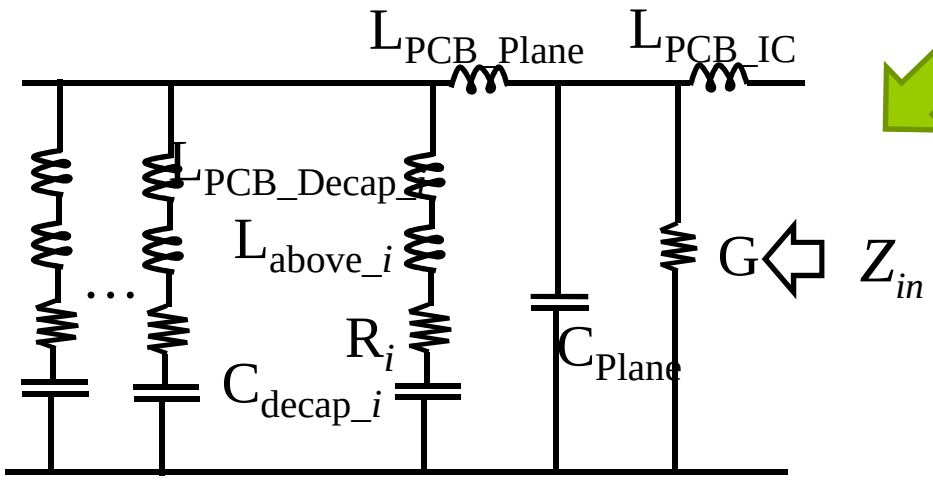
$$Z_{ij}(\omega) = \frac{1}{j\omega C_{plane}} + j\omega\mu h \left[\sum_{m=0}^{M} \sum_{n=0}^{N} \frac{\varepsilon_n^2 \varepsilon_m^2}{\left(k_{nm}^2 - k^2\right) ab} f\left(x_i, x_j, y_i, y_j\right) p\left(L_{xi}, L_{xj}, L_{yi}, L_{yj}\right) + L_{ij}^{HM} \right]_{m=n\neq 0}$$

Circuit Model for PCB PDN



physics-based circuit model

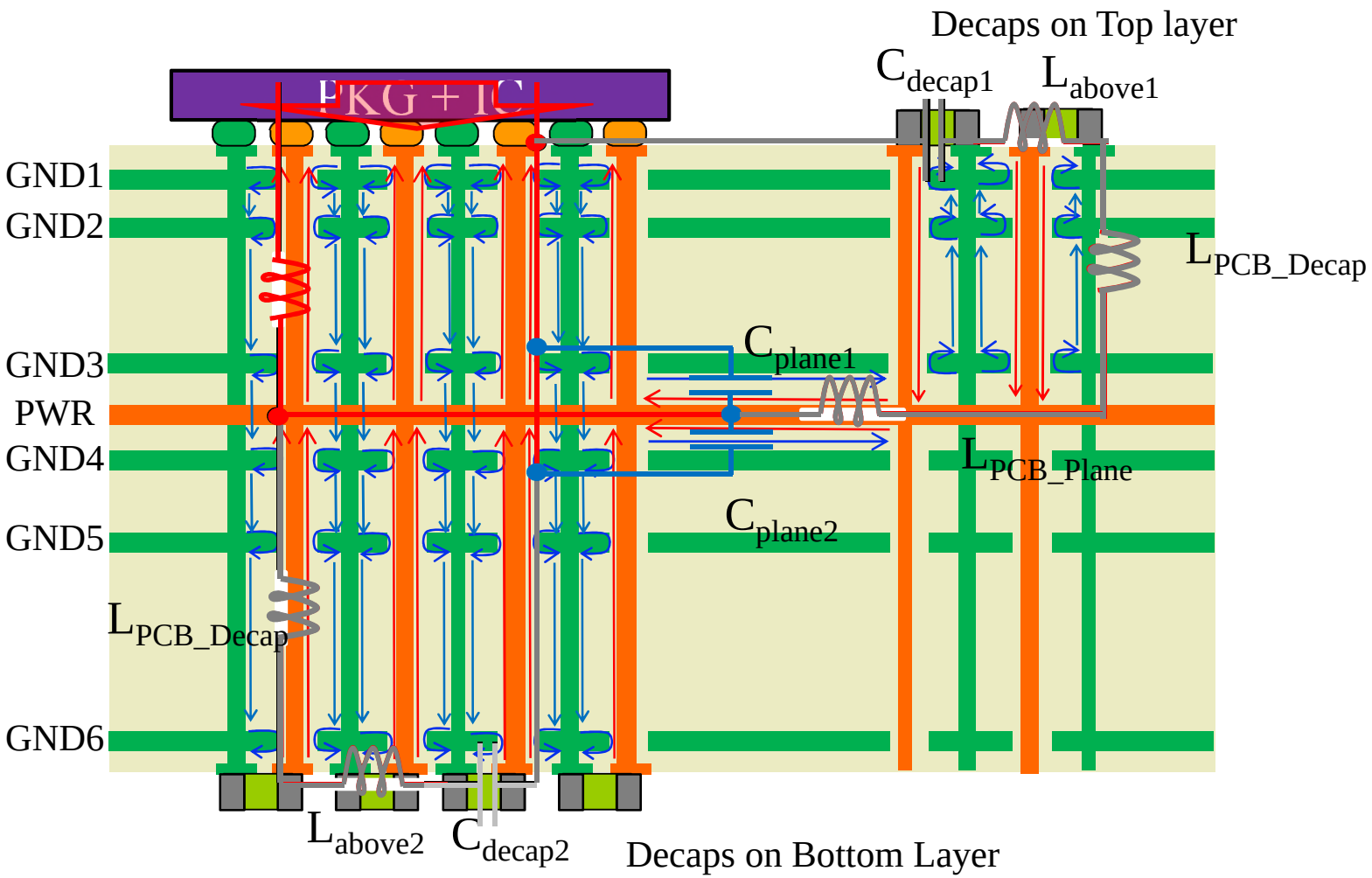




All current segments in all layers are modeled (often many thousands or tens of thousands) and self inductances for every segment and mutual between segments are extracted using the (first principles) cavity model and a SPICE model is assembled.

Circuit reduction is used to get an impedance equivalent circuit model that coincides with the large-scale current path from IC package to decaps. Inductances are related to the current path on the geometry.

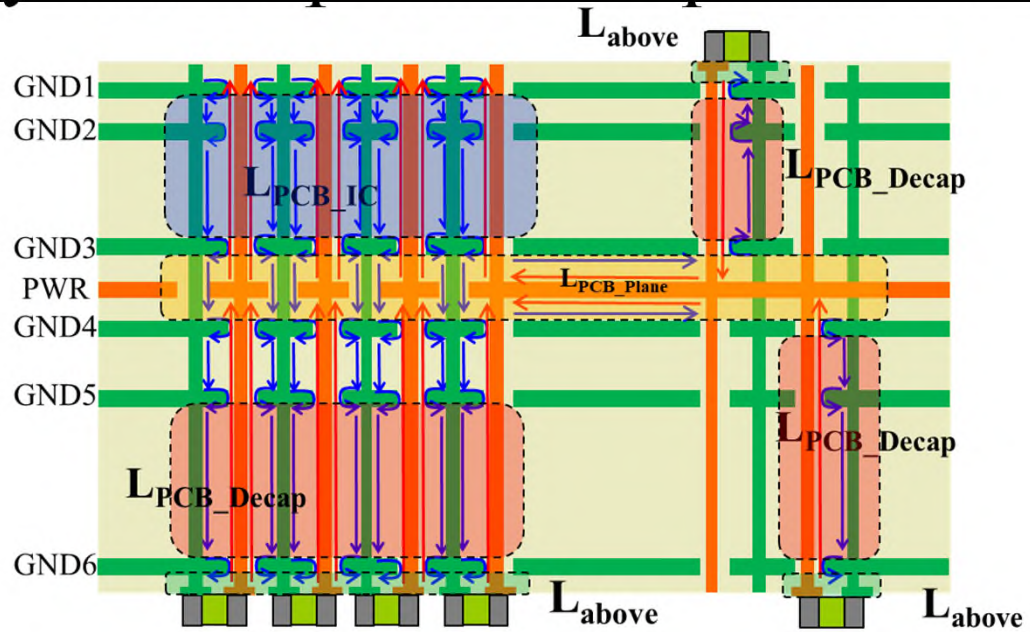
Impedance Equivalent Circuit

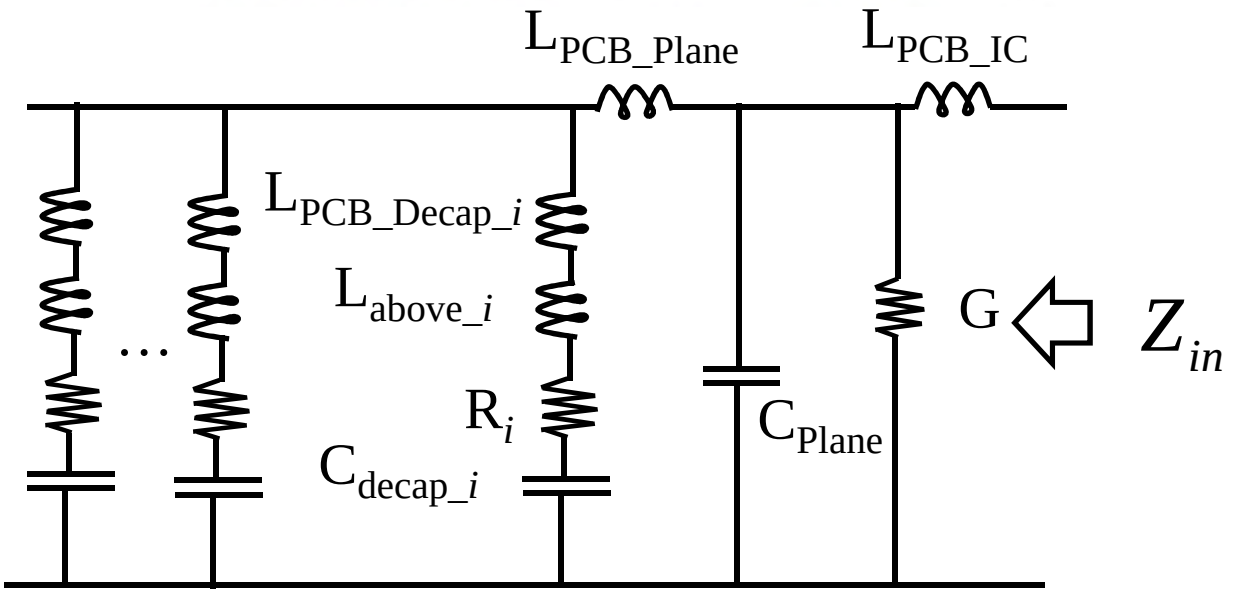


$$L_{PCB\_EQ} = L_{PCB\_Decap} + L_{PCB\_IC} + L_{PCB\_Plane} + L_{above}$$

← Includes mutual inductances

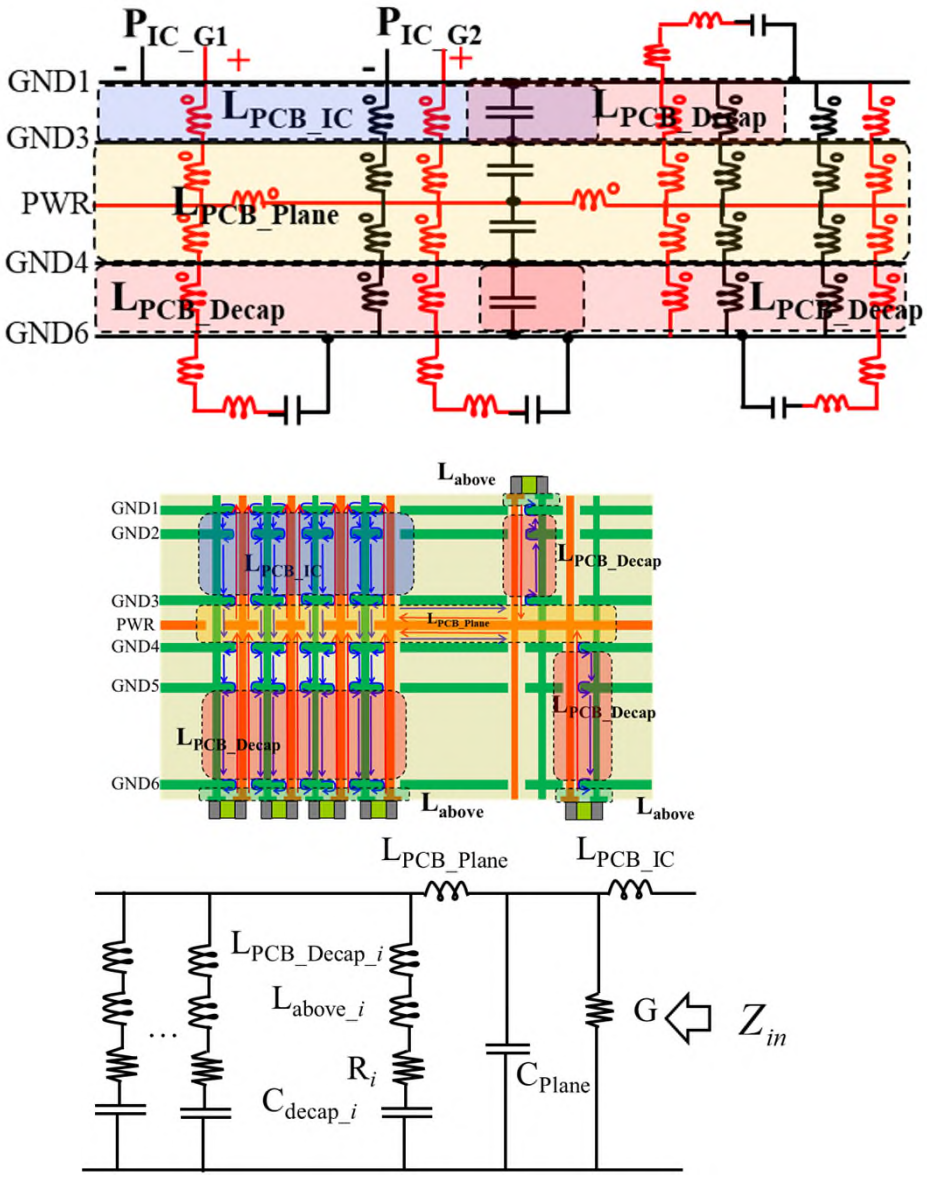
Geometry and Impedance Equivalent Circuit





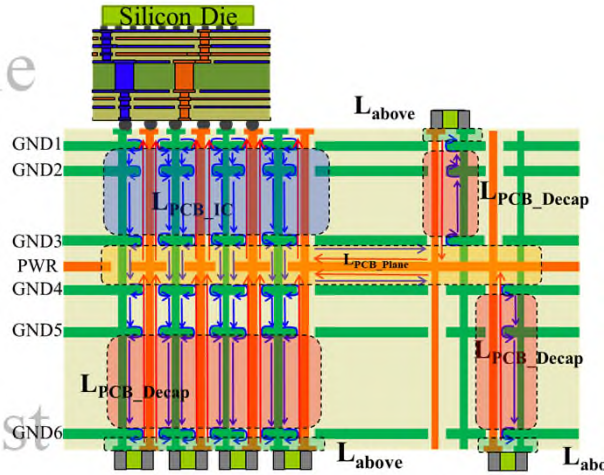
Key Points

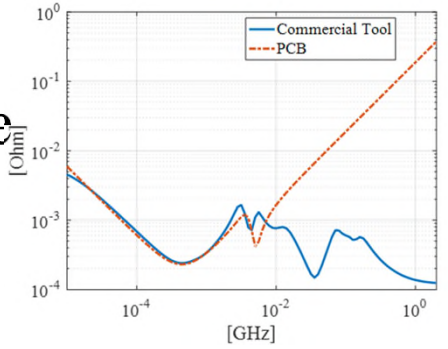
- All current segments in all layers are modeled (often many thousands or tens of thousands) and self inductances for every segment and mutual inductance between segments are extracted using the (first principles) cavity model and a SPICE model is assembled.
- Circuit reduction can be done to produce an impedance equivalent circuit model in which the model values can be calculated. The impedance equivalent circuit model can be directly related to the geometry and current paths



PI Module Overview Part 1 – Concepts and Physics

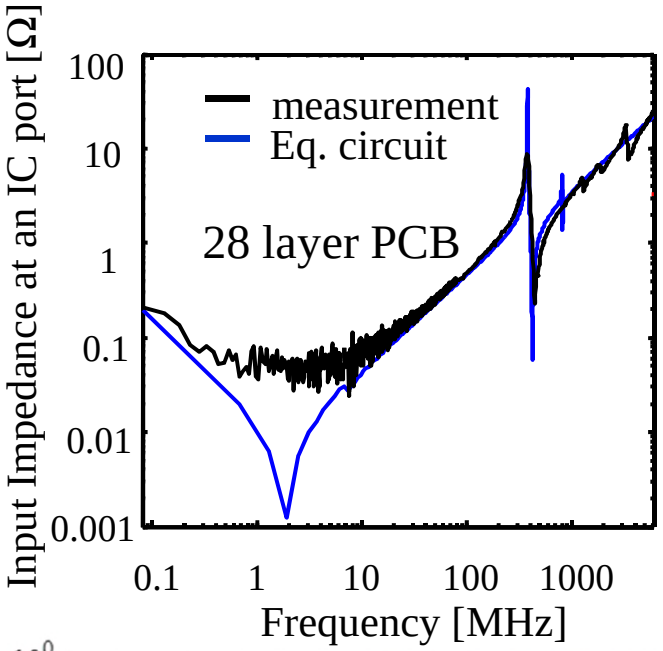
- The PDN problem
- Noise on the PDN and an FPGA example
- PDN design considerations
- A couple of preliminary concepts
- Current and inductance physics
- A reduced order circuit model from a first principles formulation
- Characteristic Z_{PDN} and relationship to physics
  - Characteristic Z_{PDN} response resulting from current-path physics and associated inductance
  - Relating the Z_{PDN} response to geometry and the impedance equivalent circuit model
  - Z_{PDN} frequency response related to physics

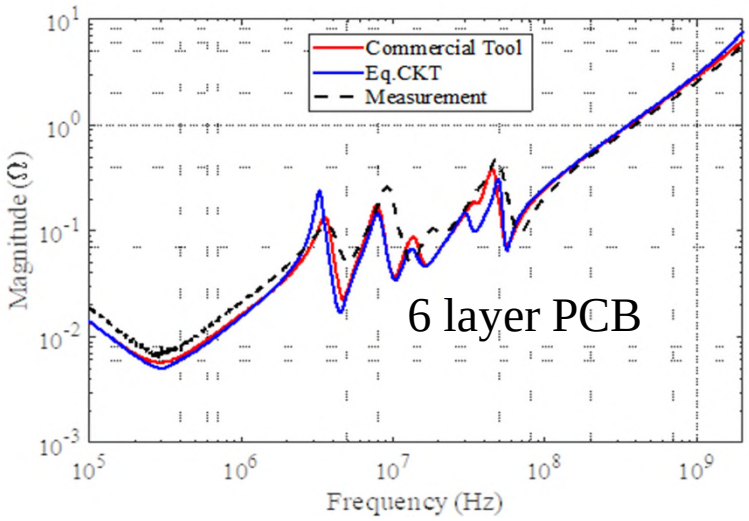


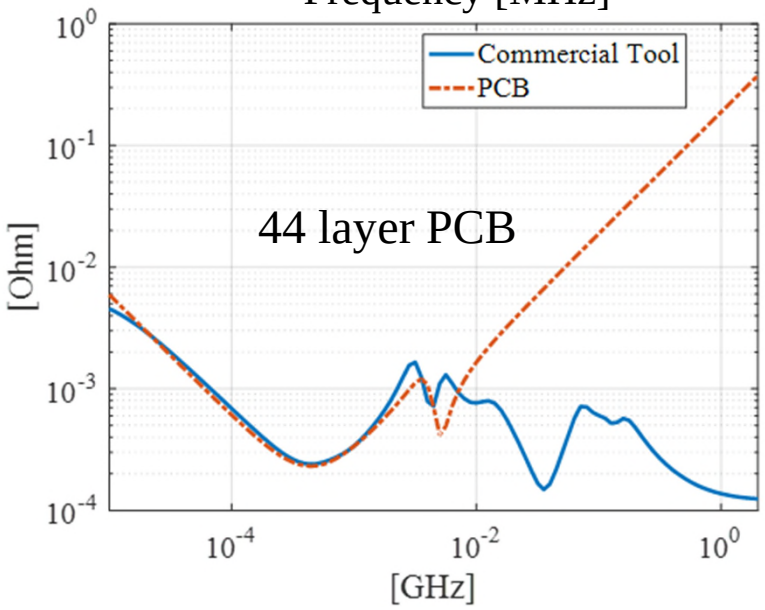


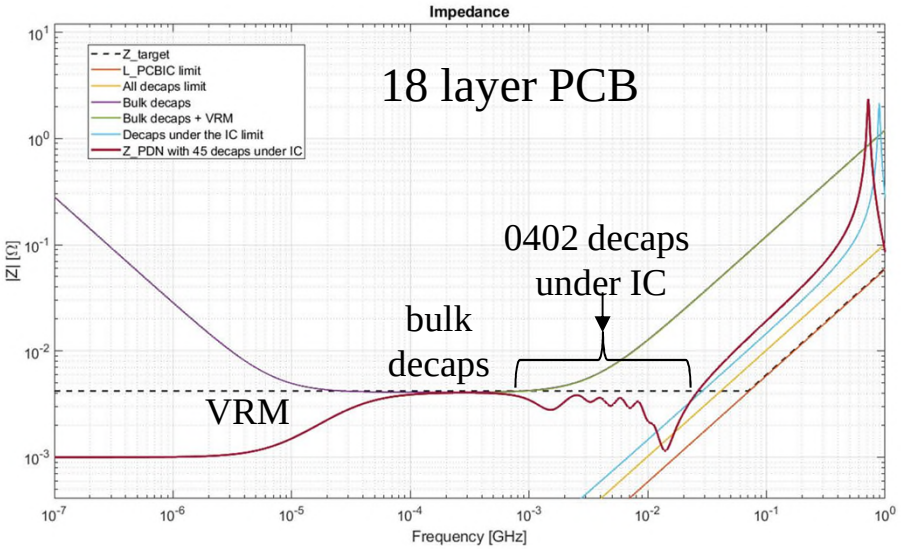
Resulting Z_{PDN} Response

Each of these production real PCBs use only a single layer for the power net area fill (with adjacent layers for power return ground).



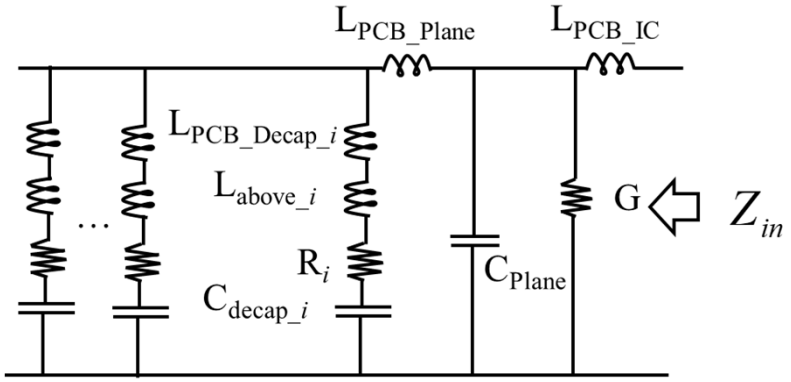


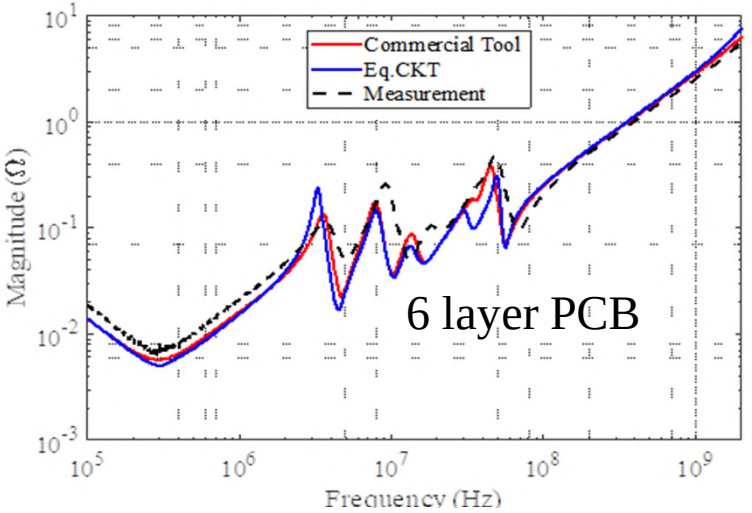


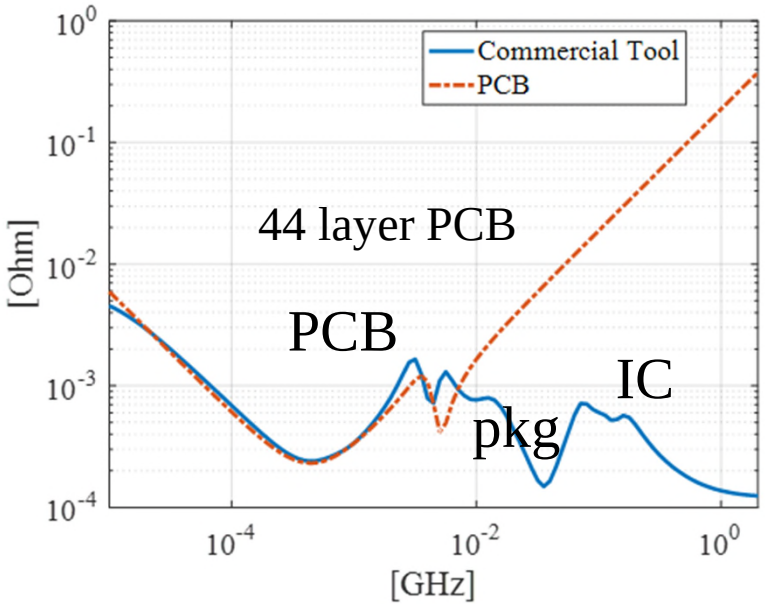


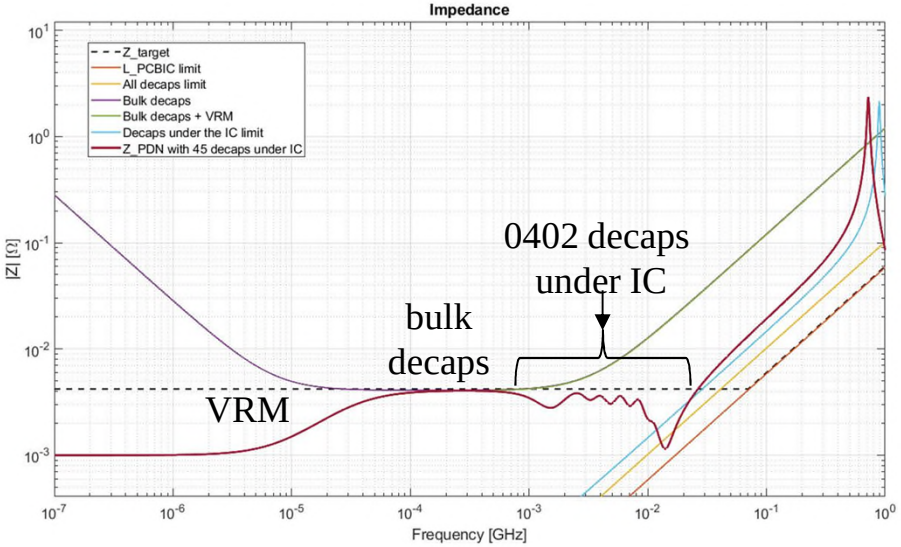
Resulting Z_{PDN} Response

Z_{PDN} response is very consistent because of the current path and its associated inductance as seen from the impedance equivalent circuit model

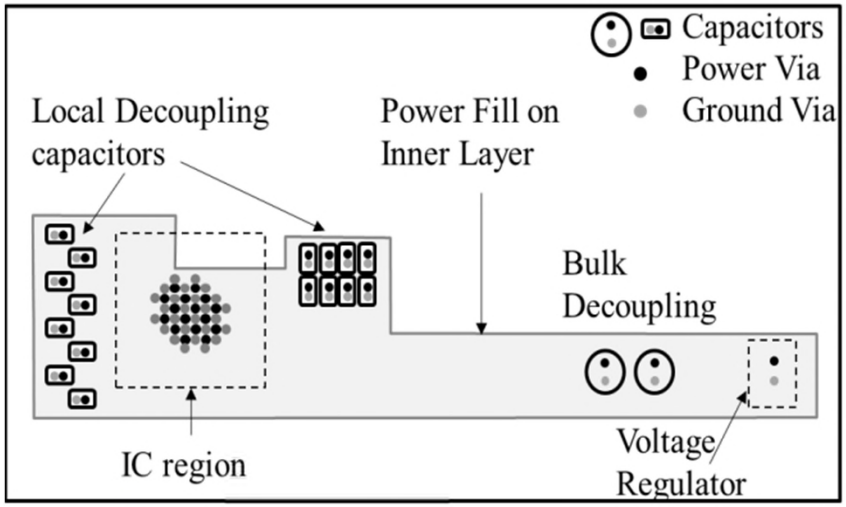


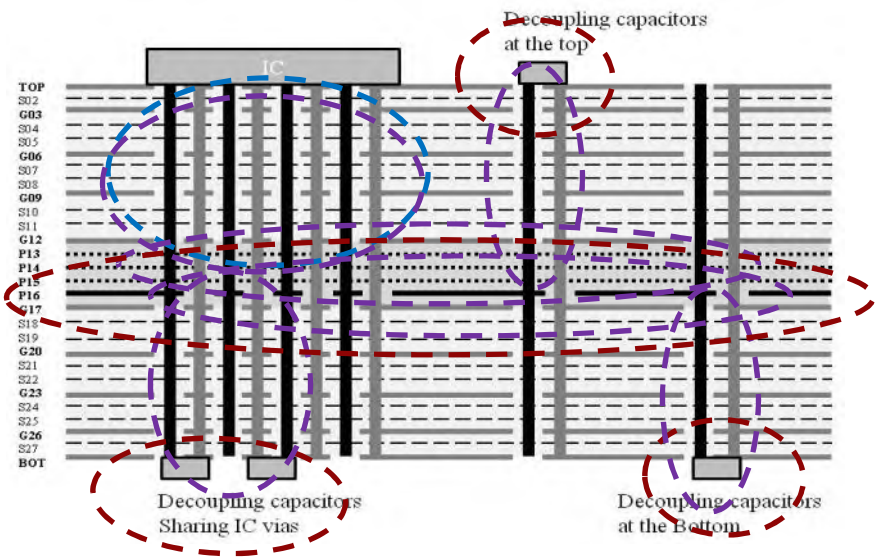


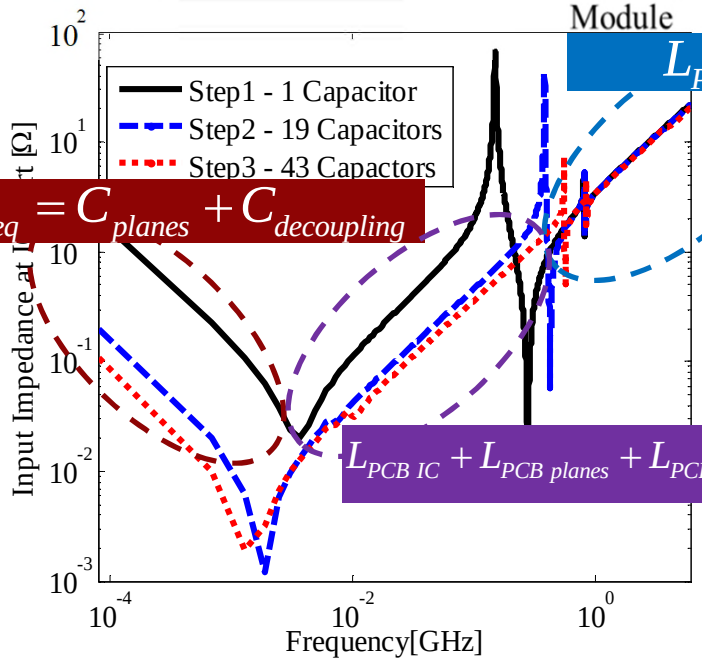




Geometry, Current Path, Model, and Z_{PDN}



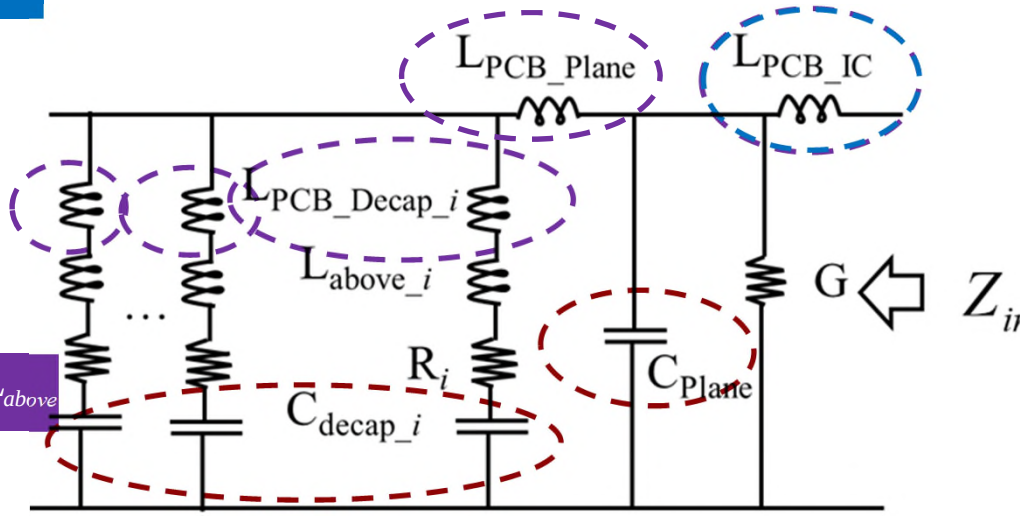




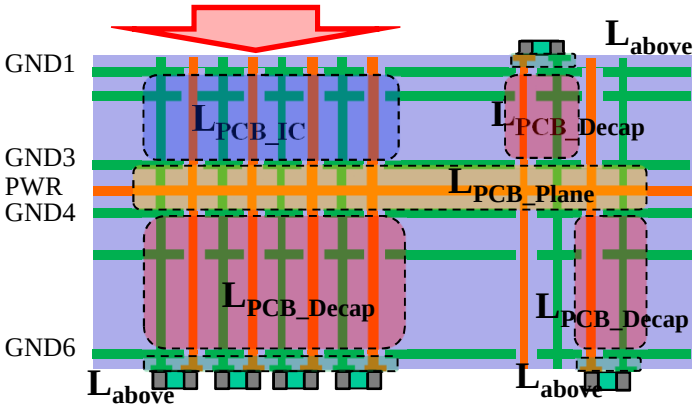
$L_{PCB\ IC}$

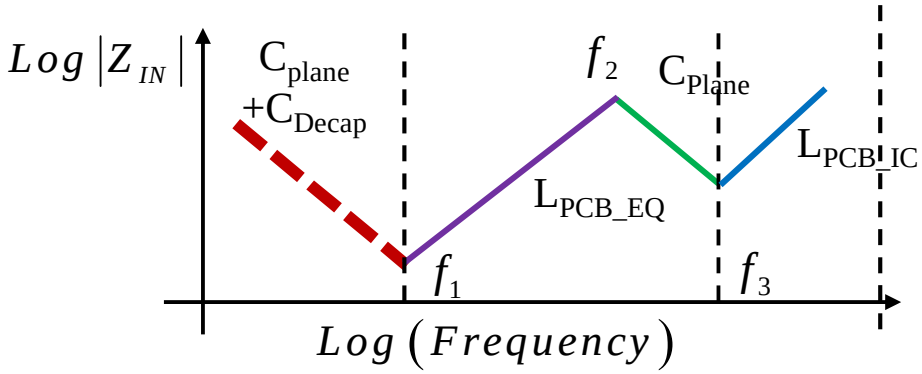
$C_{eq} = C_{planes} + C_{decoupling}$

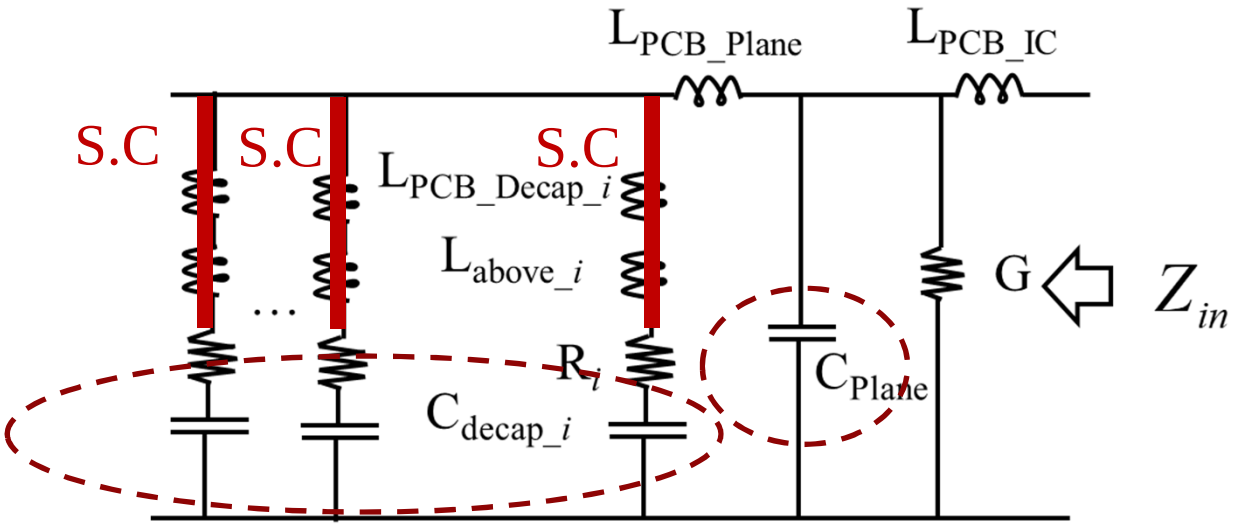
$L_{PCB\ IC} + L_{PCB\ planes} + L_{PCB\ Decaps} + L_{above}$



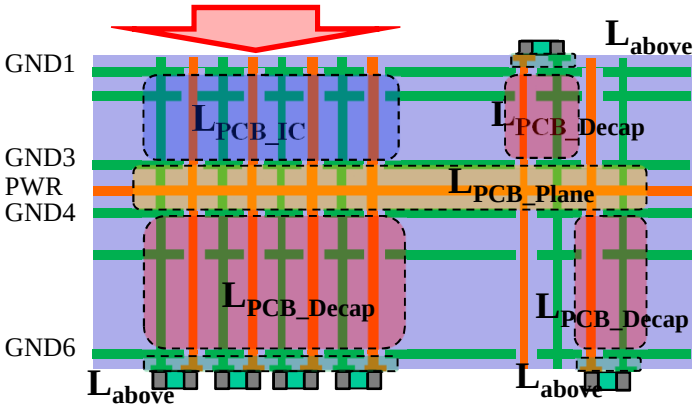
Frequency Response for PCB PDN - C

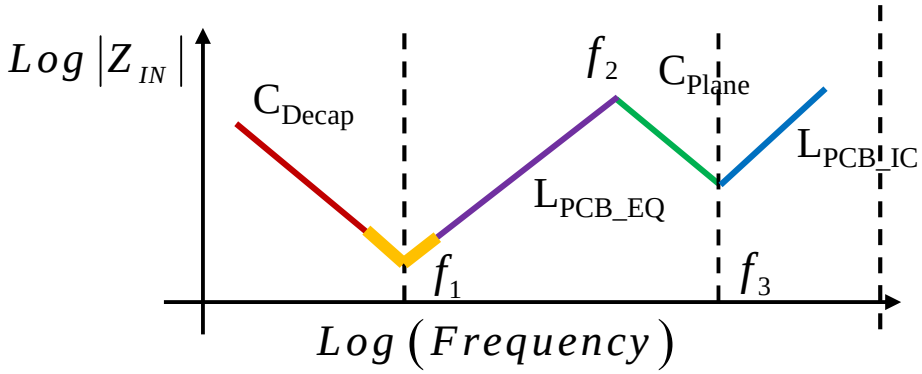


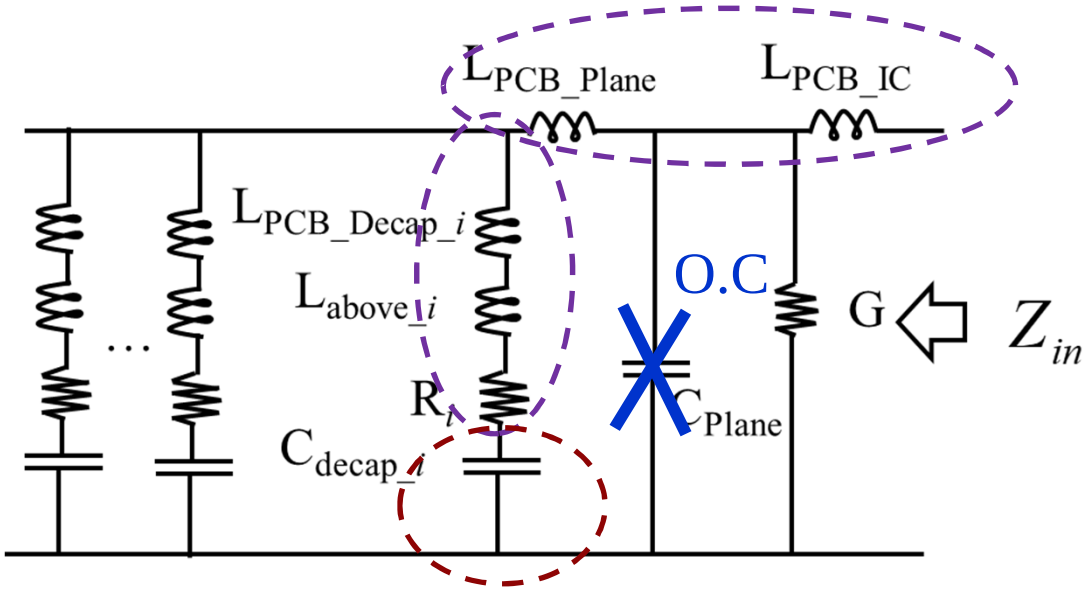




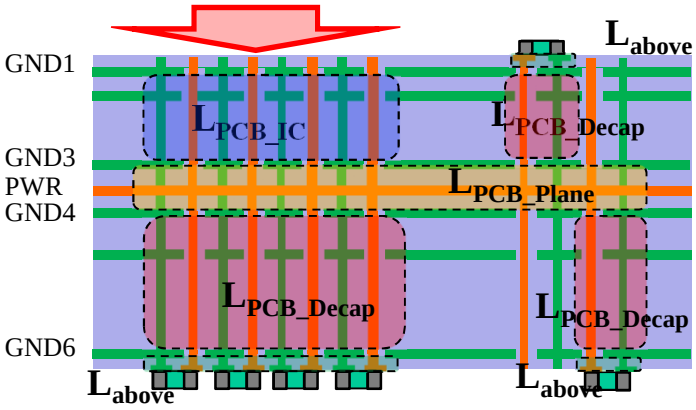
Frequency Response for PCB PDN – f_1

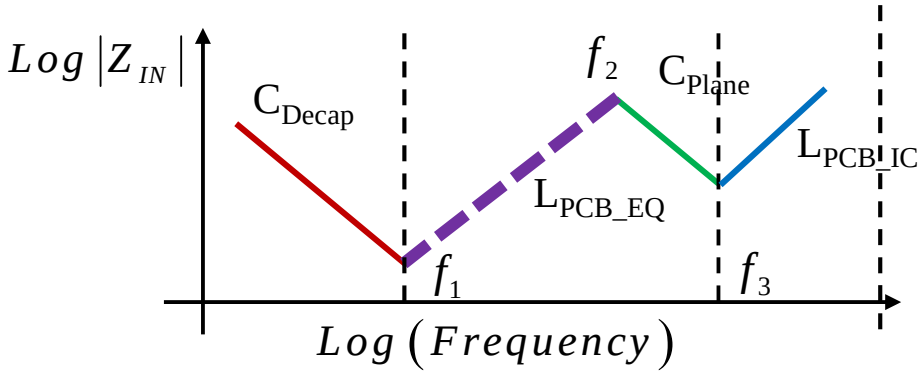


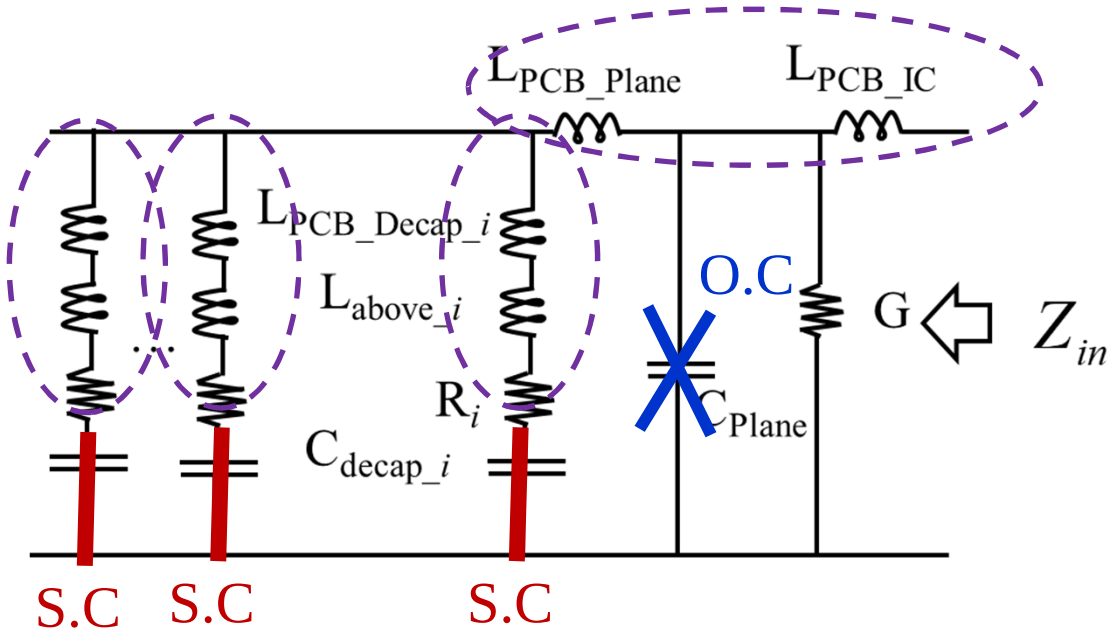




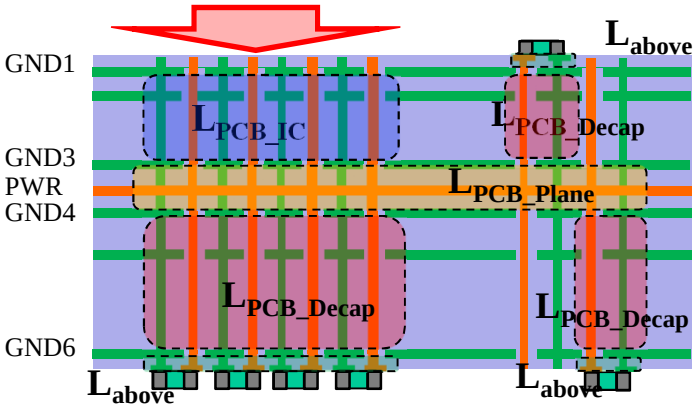
Frequency Response for PCB PDN – $L_{PCB\ EQ}$

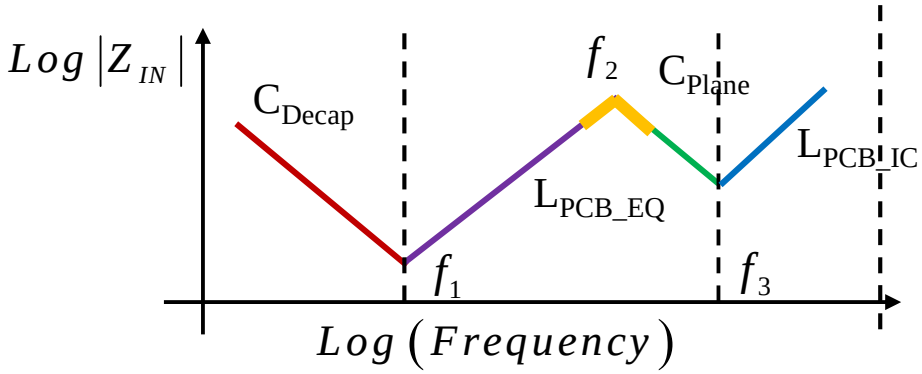


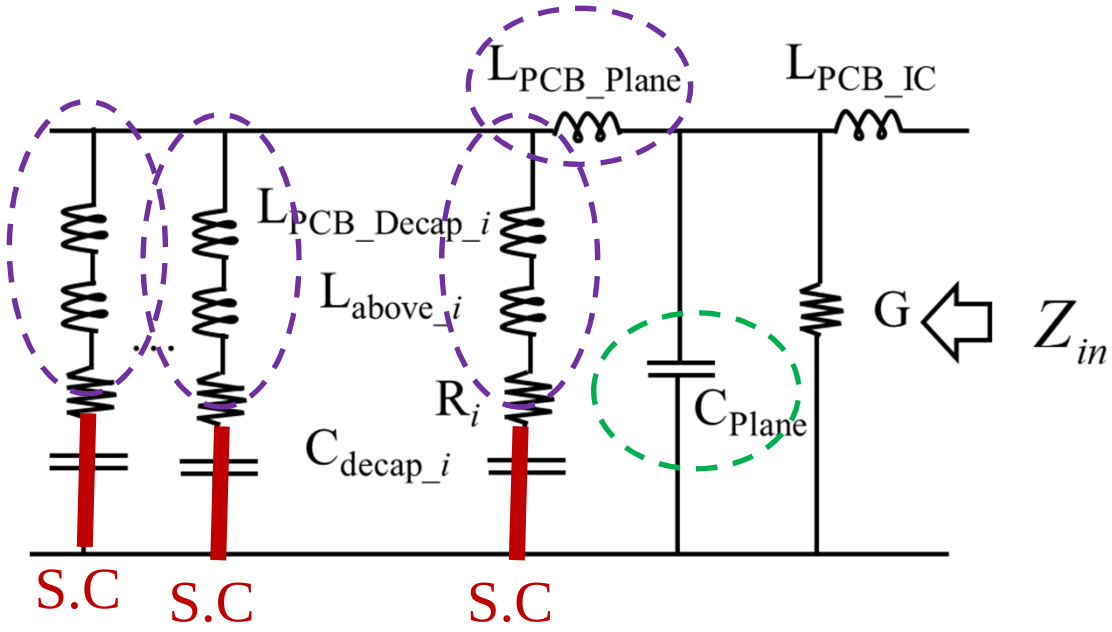




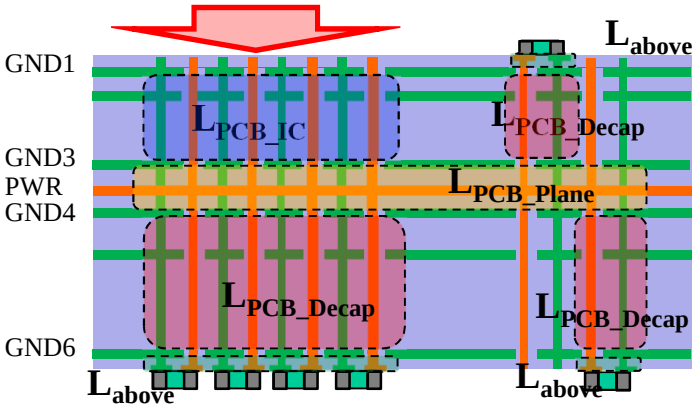
Frequency Response for PCB PDN – f_2

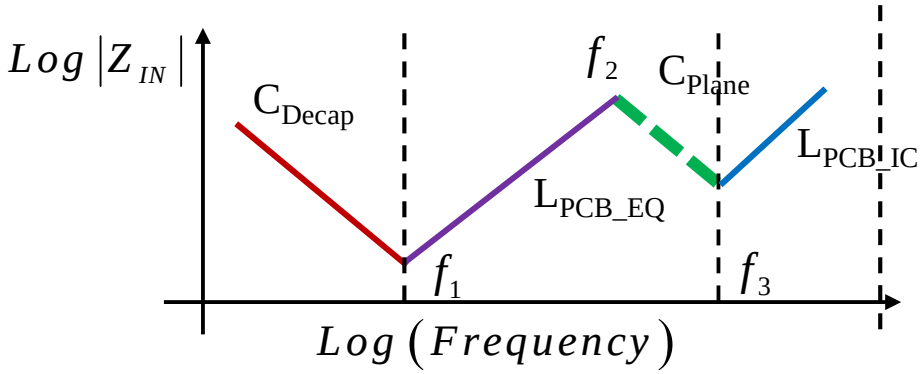


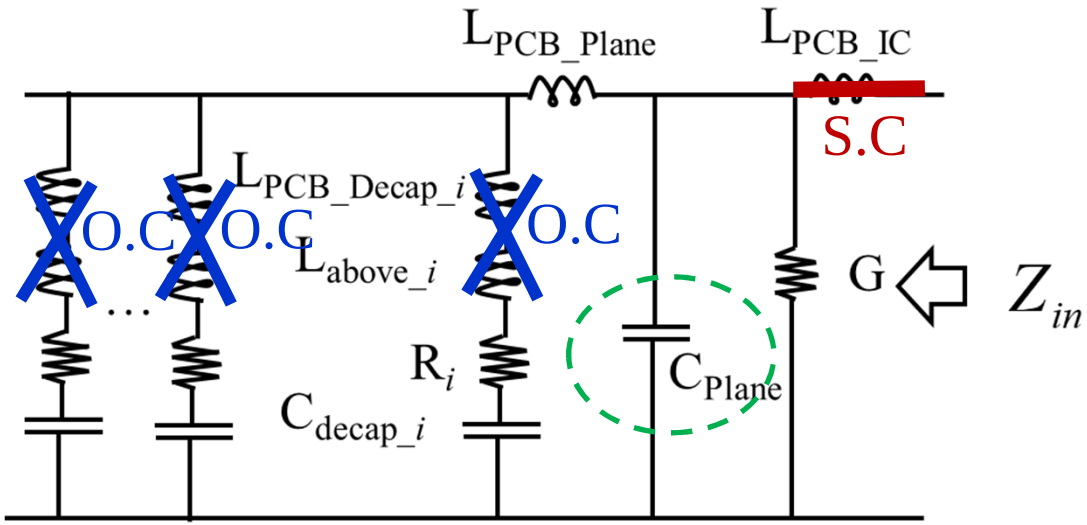




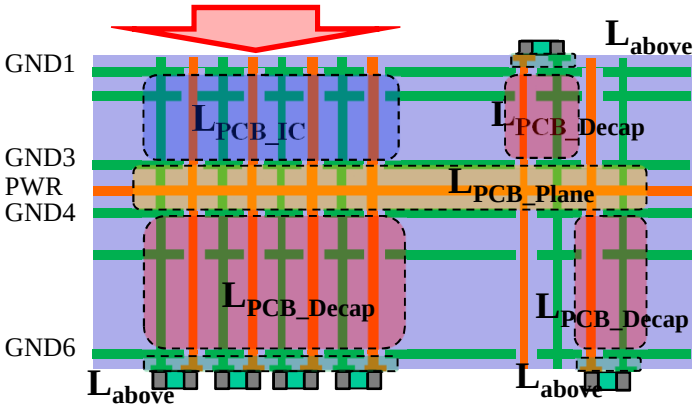
Frequency Response for PCB PDN –C_{Plane}

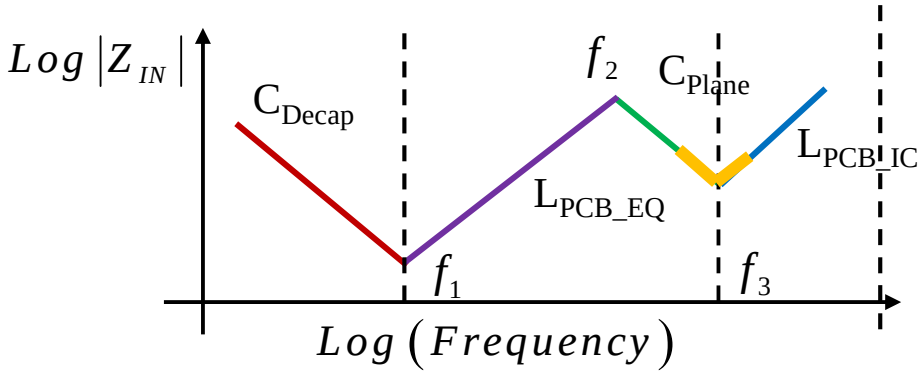


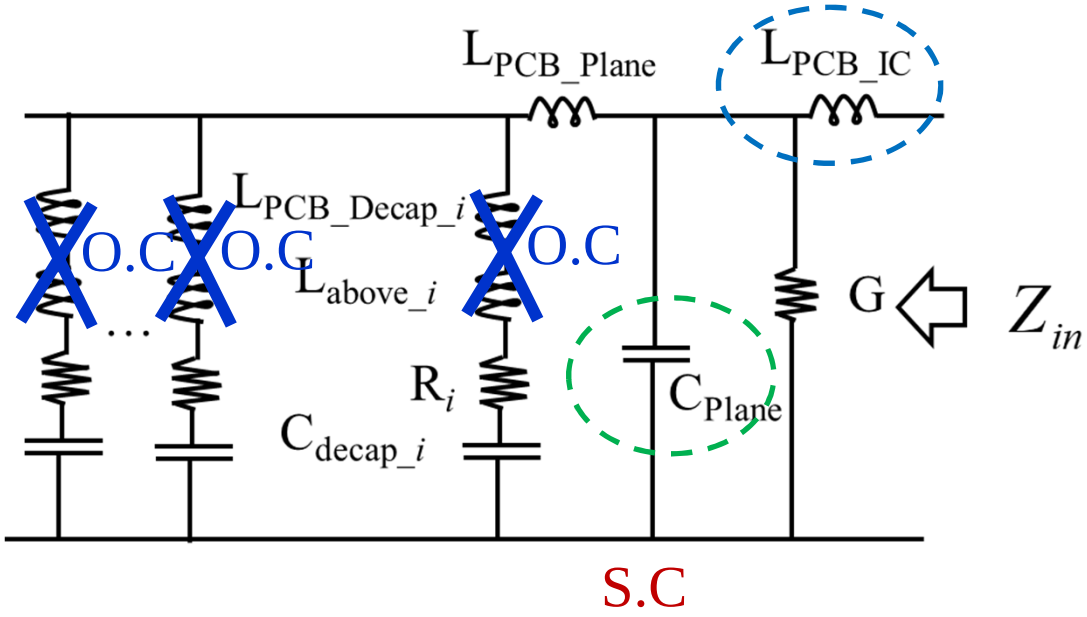




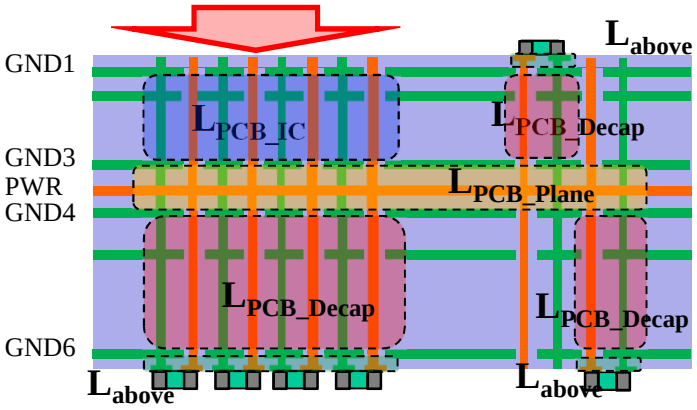
Frequency Response for PCB PDN – f_3

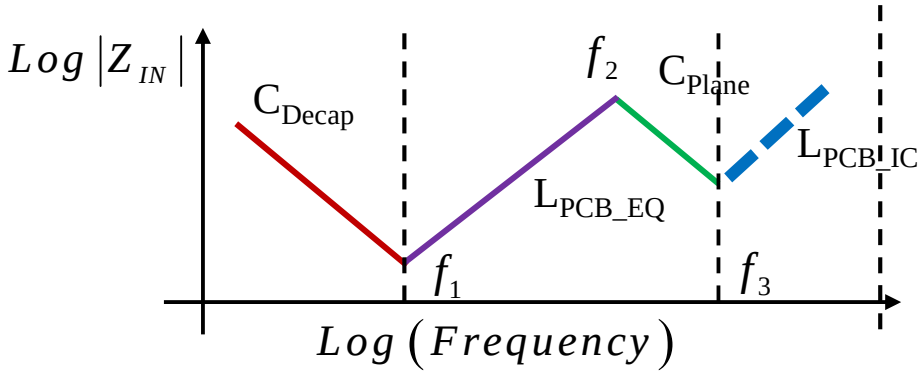


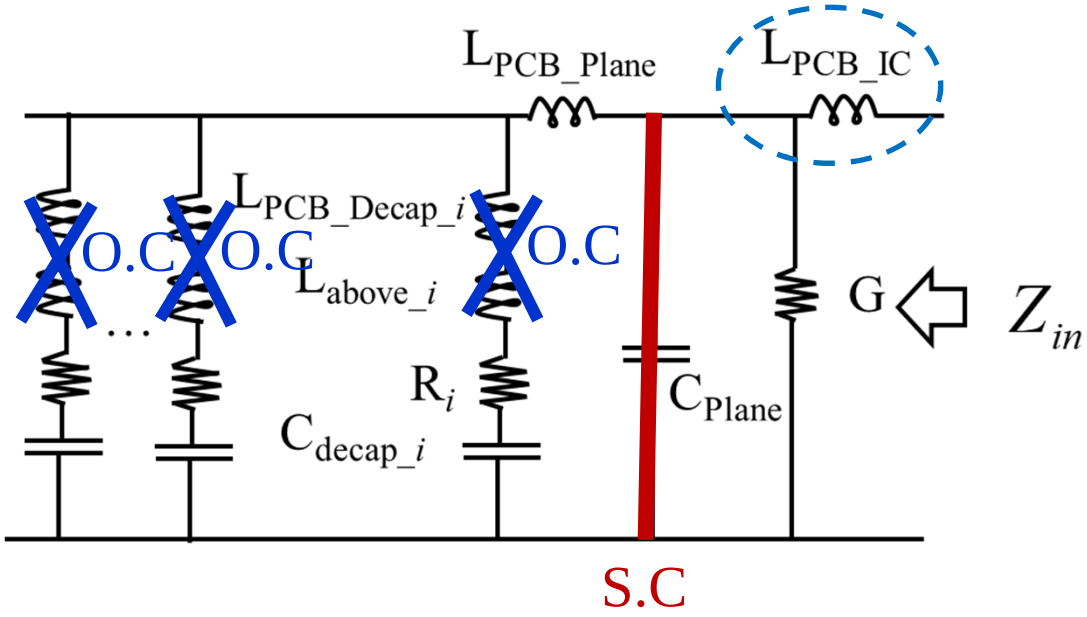




Frequency Response for PCB PDN –$L_{PCB\ IC}$

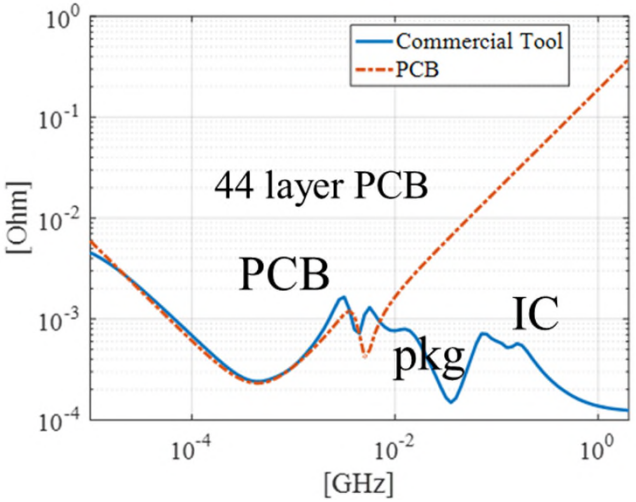


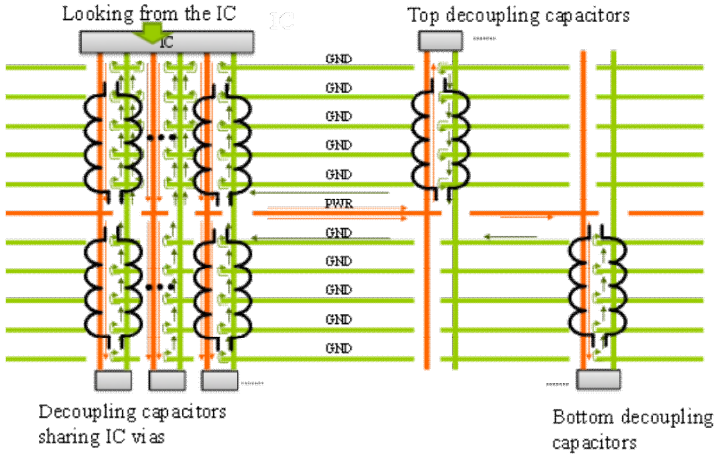




Key Points

- The shape of the Z_{PDN} curve is very characteristic but relatively simple, even though the geometry of the PDN on a multi-layer PCB is complicated
- The current-path physics governing the impedance are dominated by inductance and lumped element resonances above approximately 1 MHz
- The inductance is dominated by the current path – geometry "length/area" (series inductance), and the number of parallel paths (parallel inductance) and this will drive the design approach ("small loops and many loops")





- Where power layers are located in stackup
- Package ball pitch
- Decoupling capacitor interconnect

- Number of PWR/GND vias in package
- Number of decoupling capacitors

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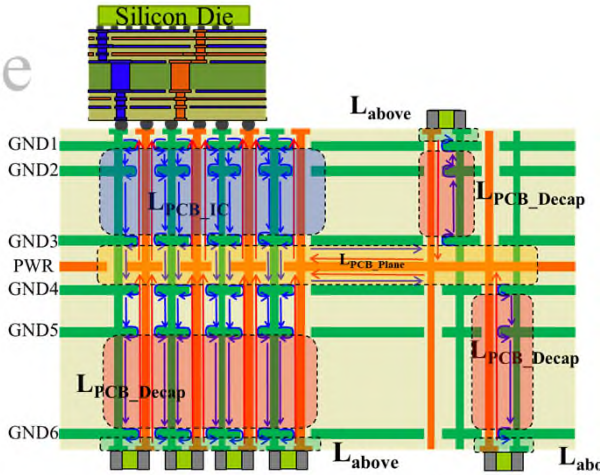
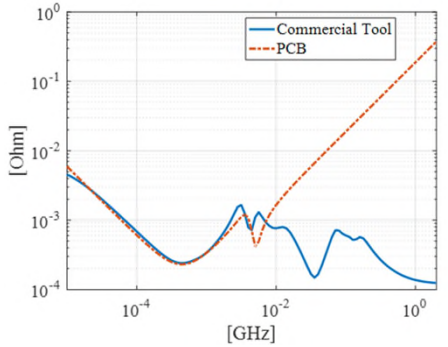
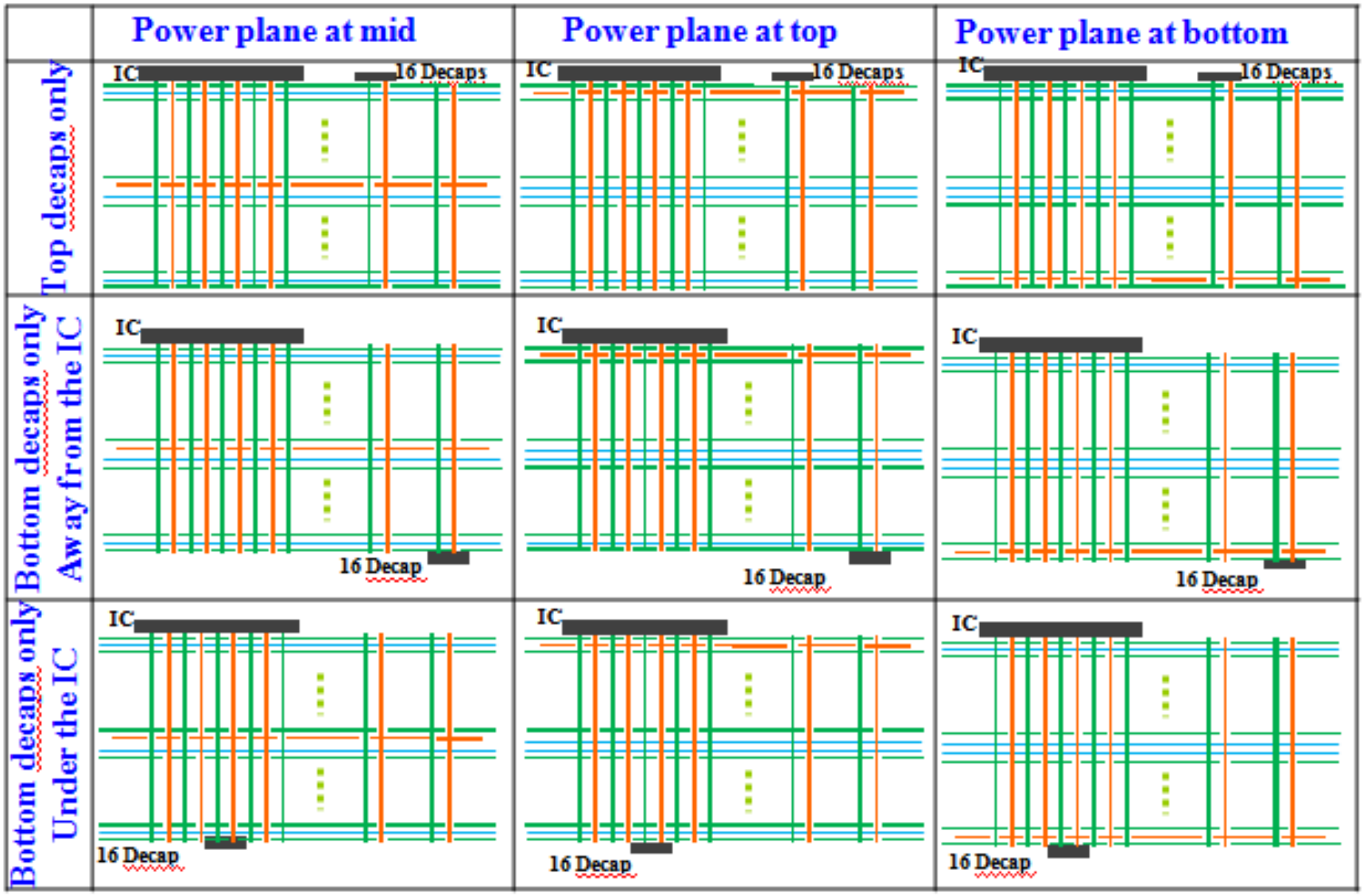
- A reduced order circuit model from a first principles formulation
- Characteristic Z_{PDN} and relationship to physics
- Understanding PDN physics and design through examples
- Identifying limiting physics in design
- Adding decoupling capacitors

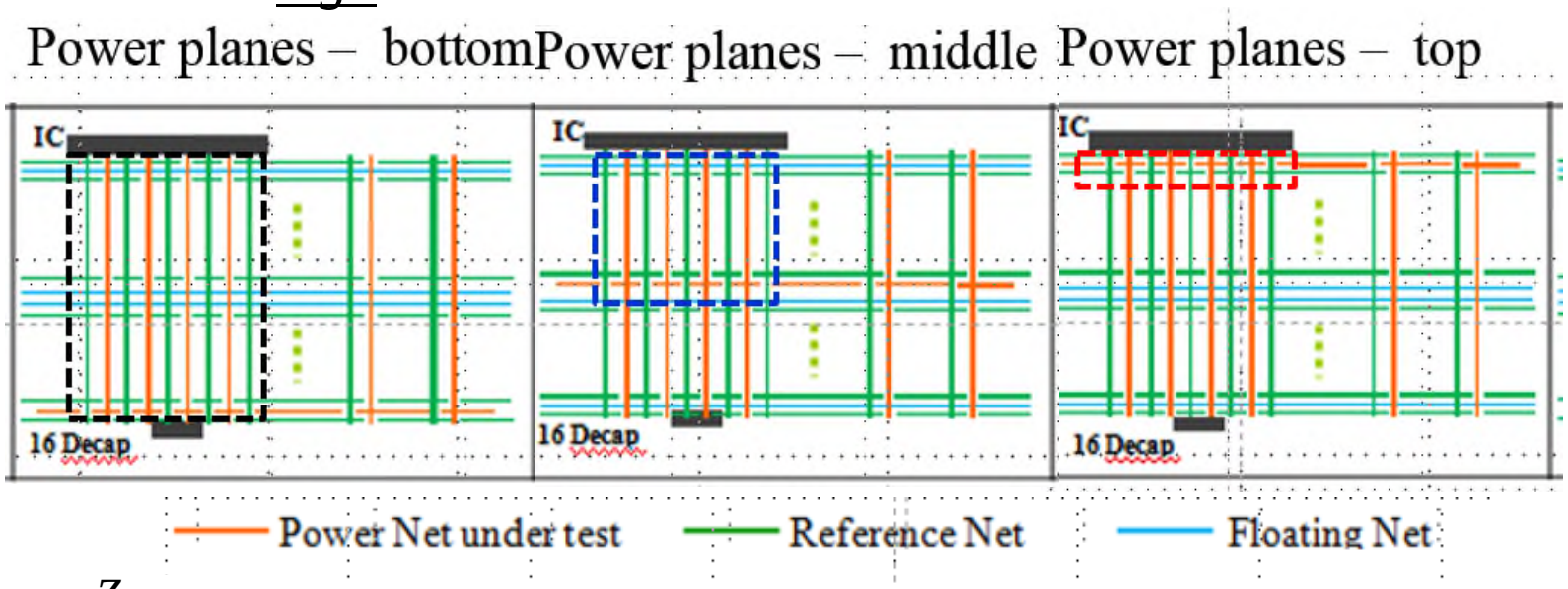


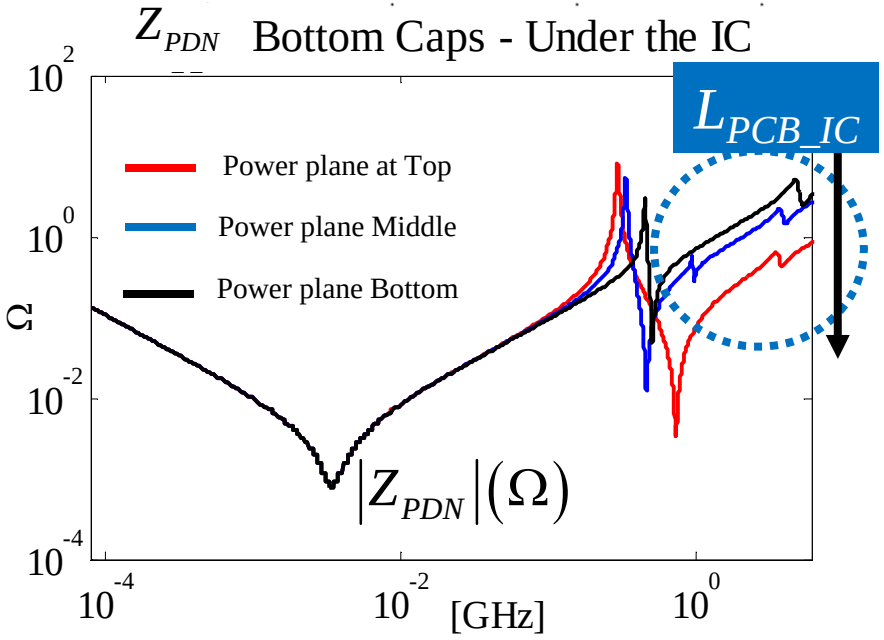


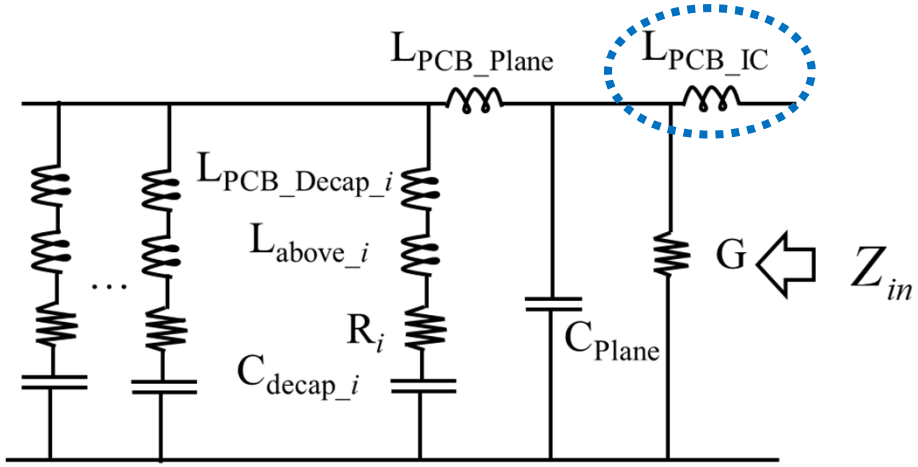
Power Plane and Capacitor Location Matrix



L_{high} – Power Plane Location in Layer Stack







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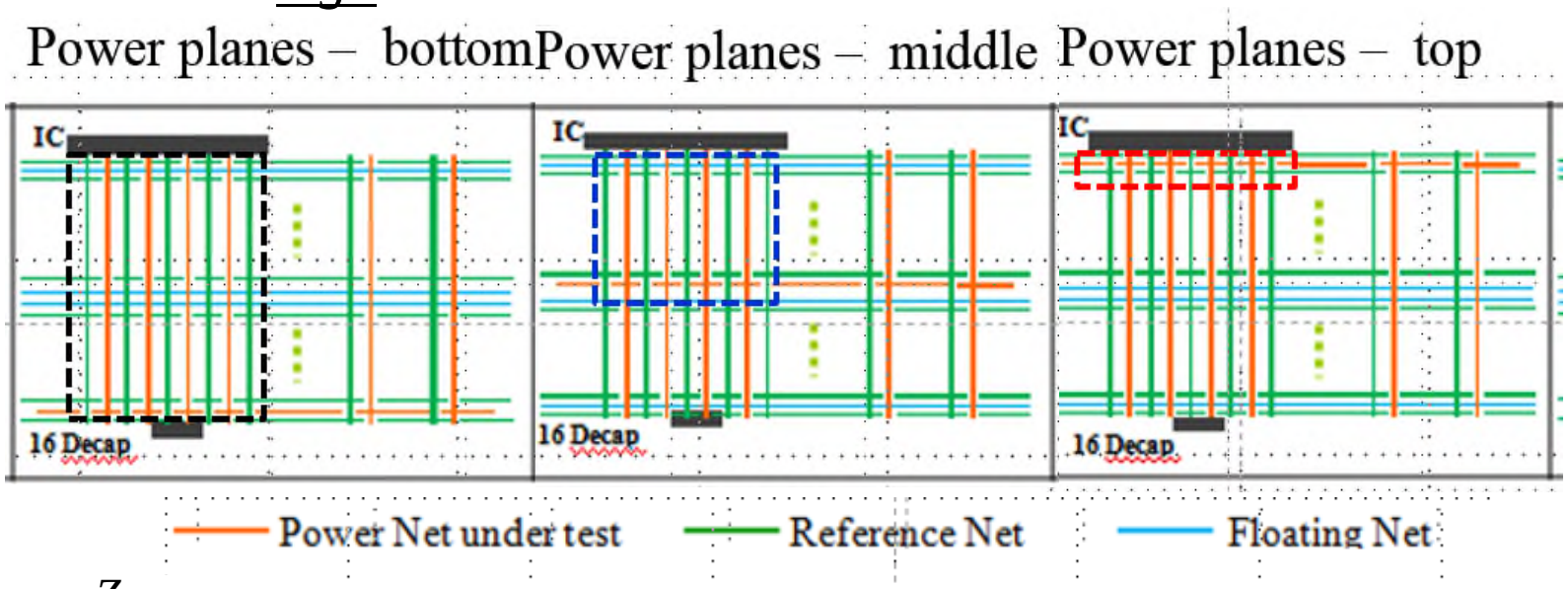
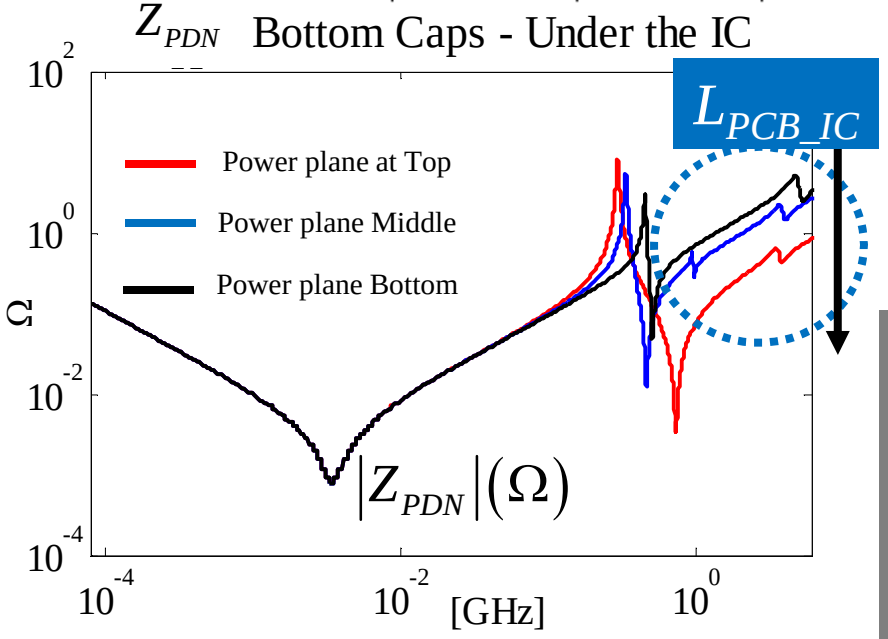
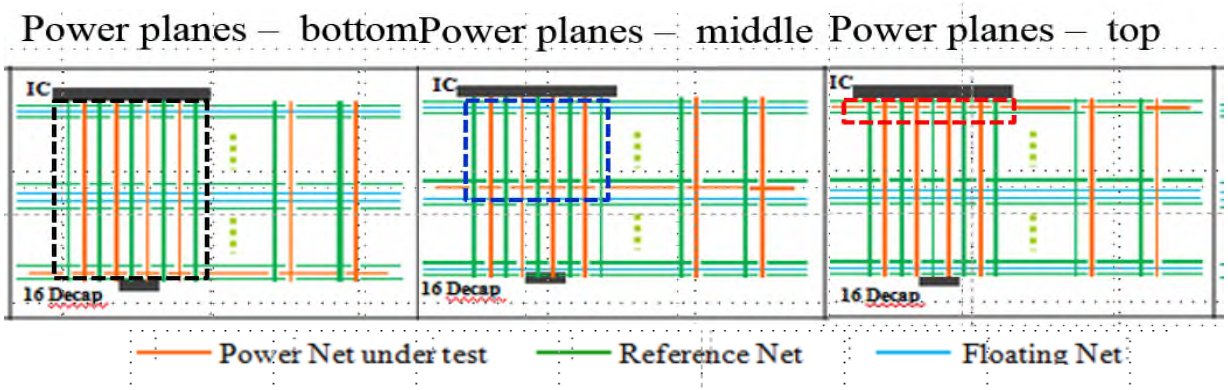


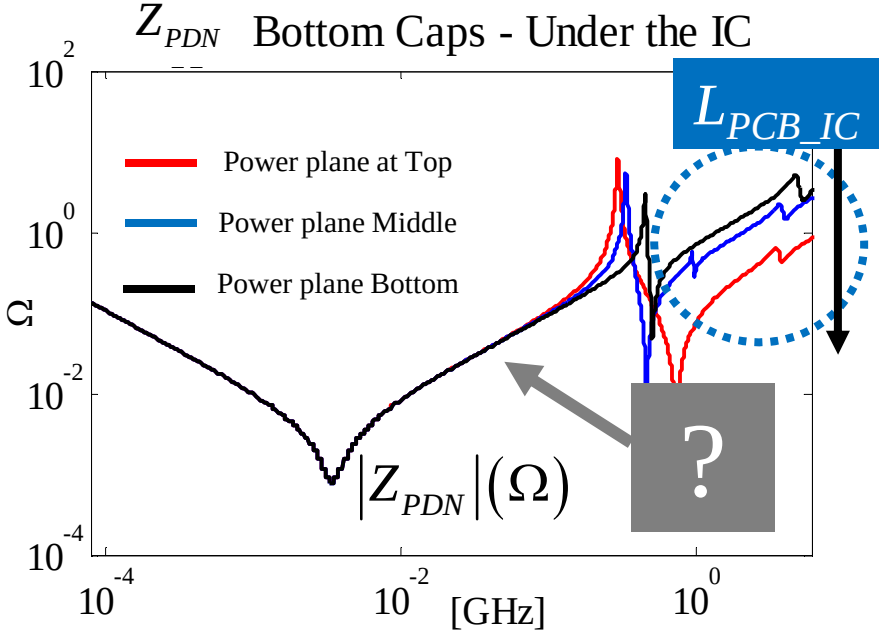


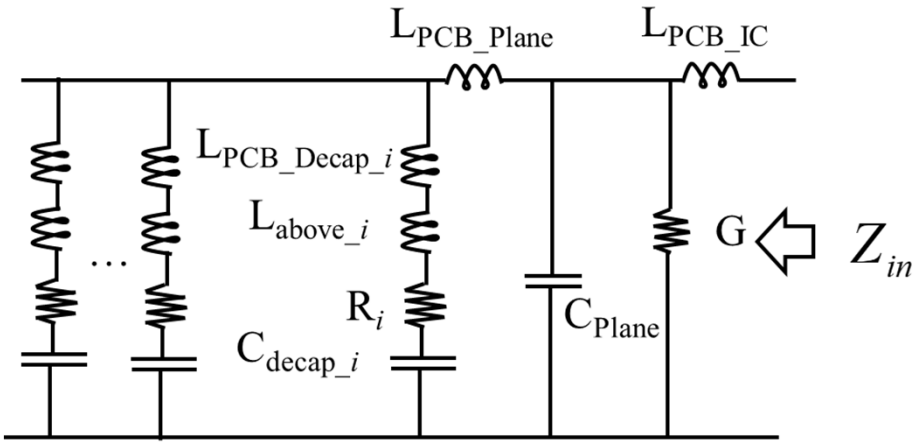
Decreasing current path and inductance from package balls to PDN power layer net

Power layer closest to the IC minimizes IC to power plane inductance. (Recall that $j\omega L_{PCB\_IC}$ is the impedance limit above a few MHz.)

L_{high} – Power Plane Location in Layer Stack



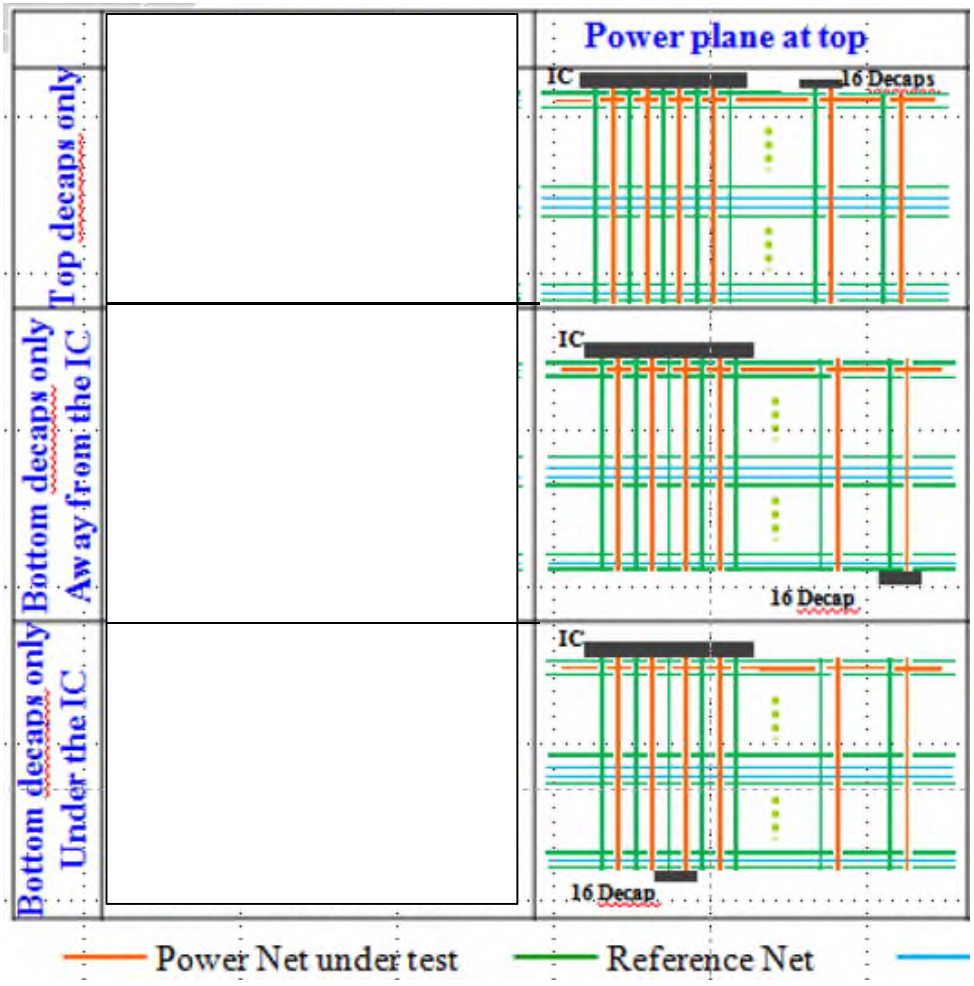


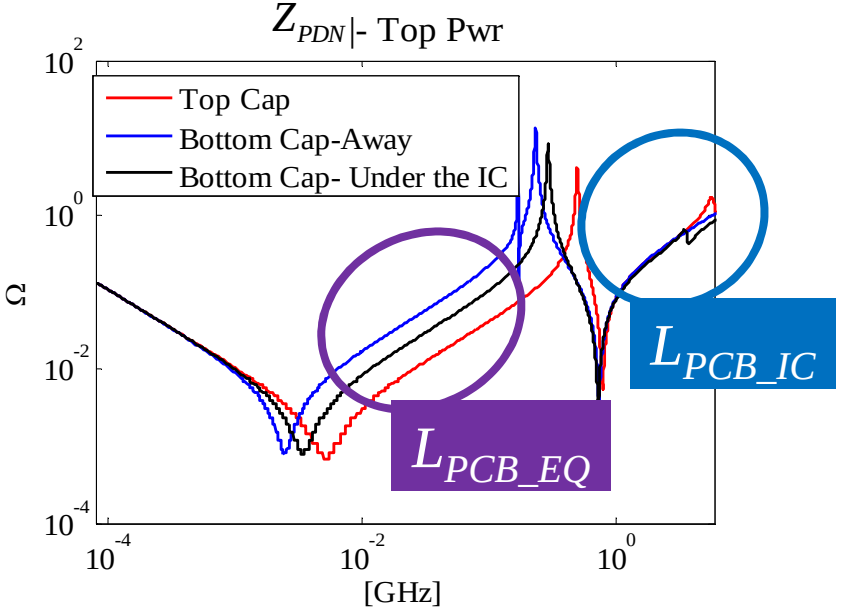


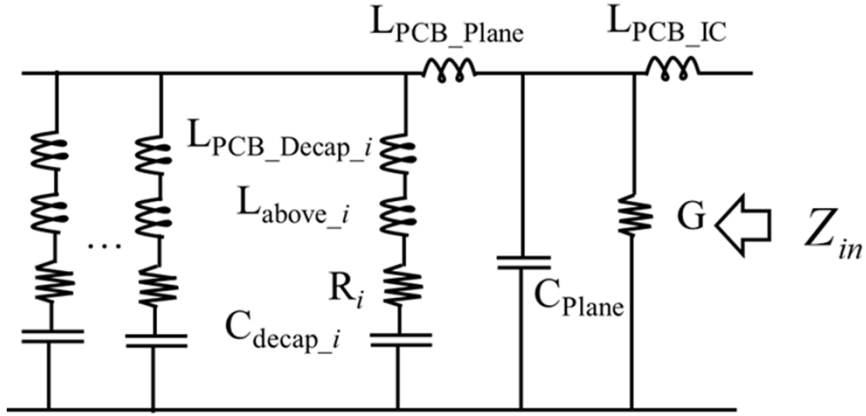
Q: How many power pins are there here?

Q: Why is the mid frequency range impedance not changing

Capacitor Location – Top, Bottom, at IC

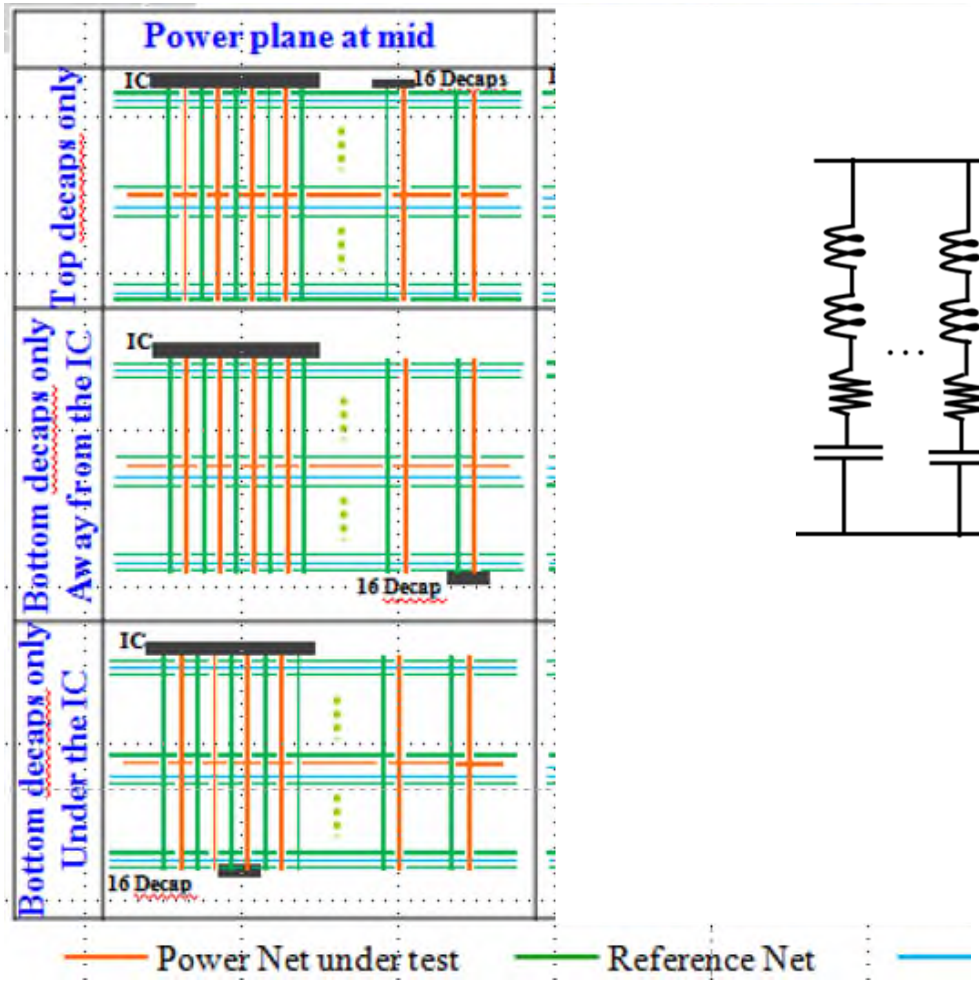


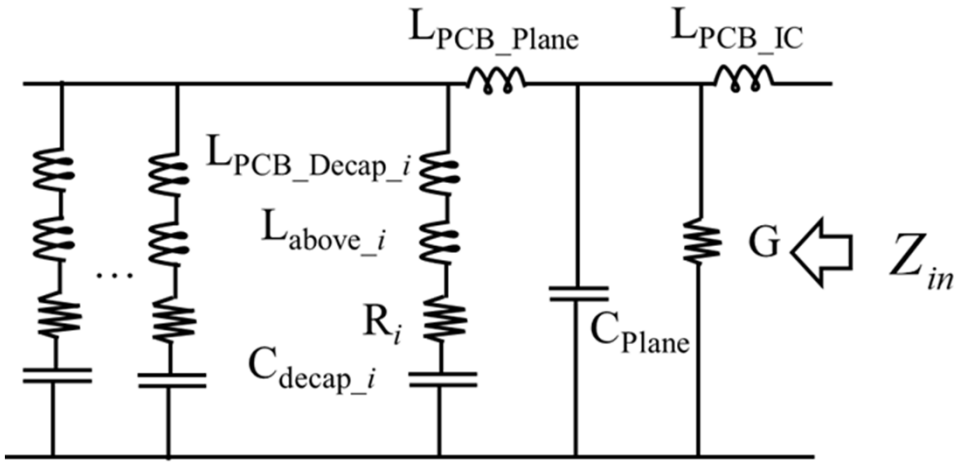


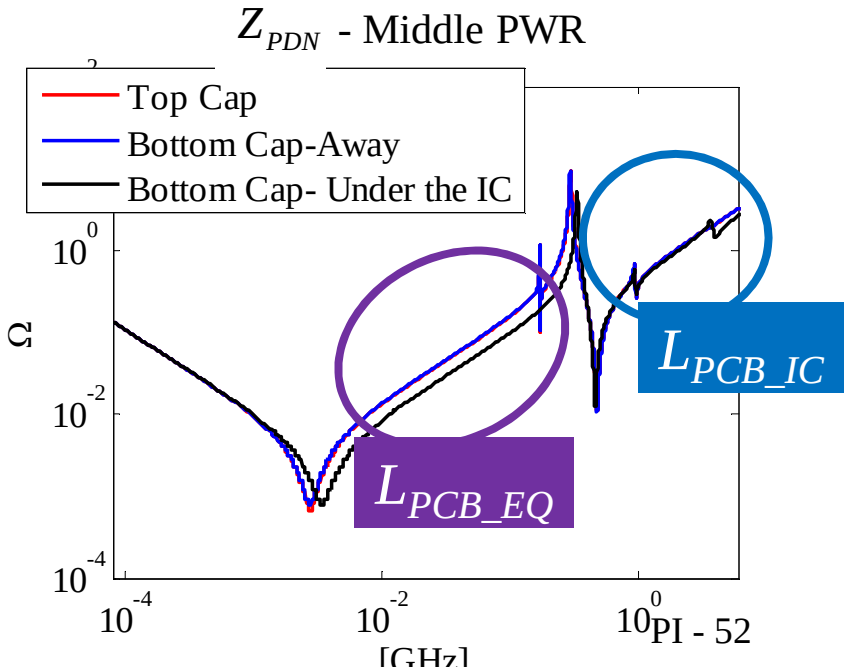


Capacitors placed on the side closest to the power plane reduces the inductance from the capacitor to power plane and L_{EQ}. The current path length/area is smallest.

Capacitor Location – Top, Bottom, at IC



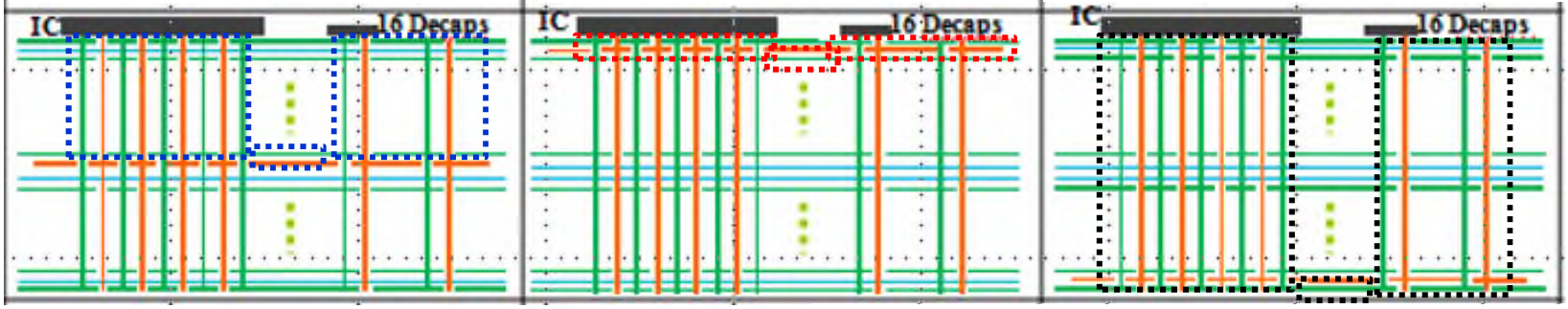


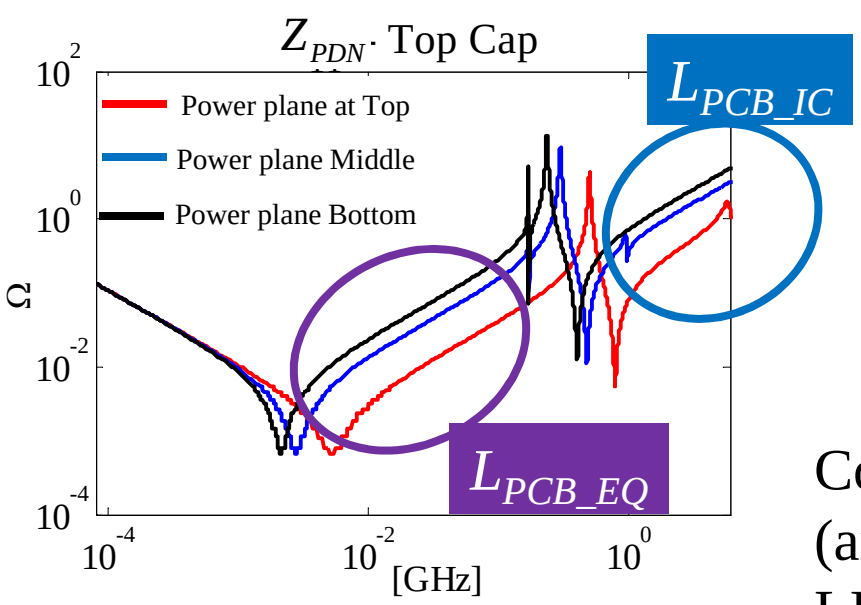


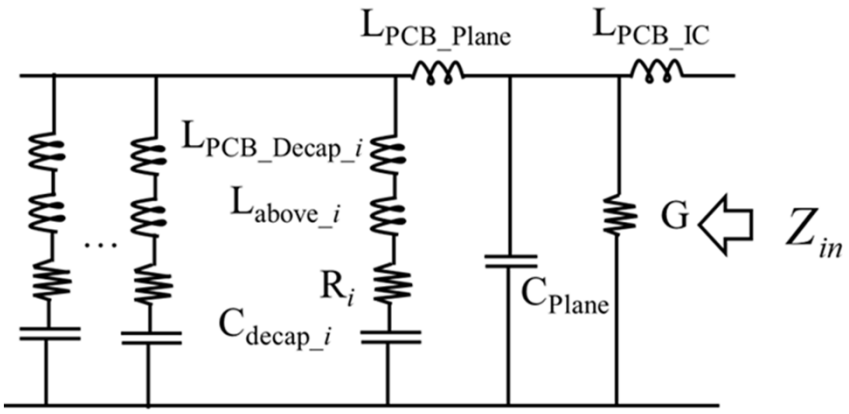
Q: Why are there only two curves in the mid-frequency range and what do they correspond to? Explain the differences.

L_{EQ} – Power Plane Location and Decaps

Power planes – mid | Power planes – top | Power planes – bottom







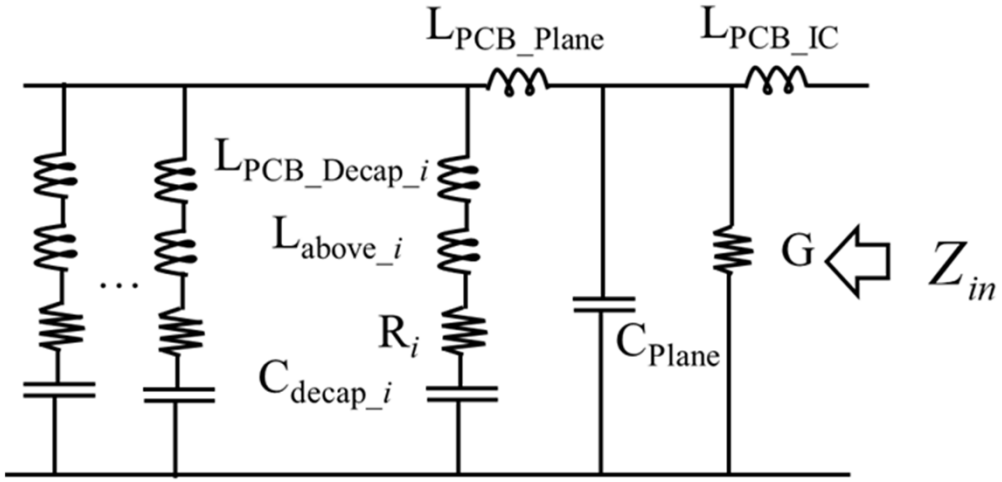
Q: What limits the PDN impedance in each case above?

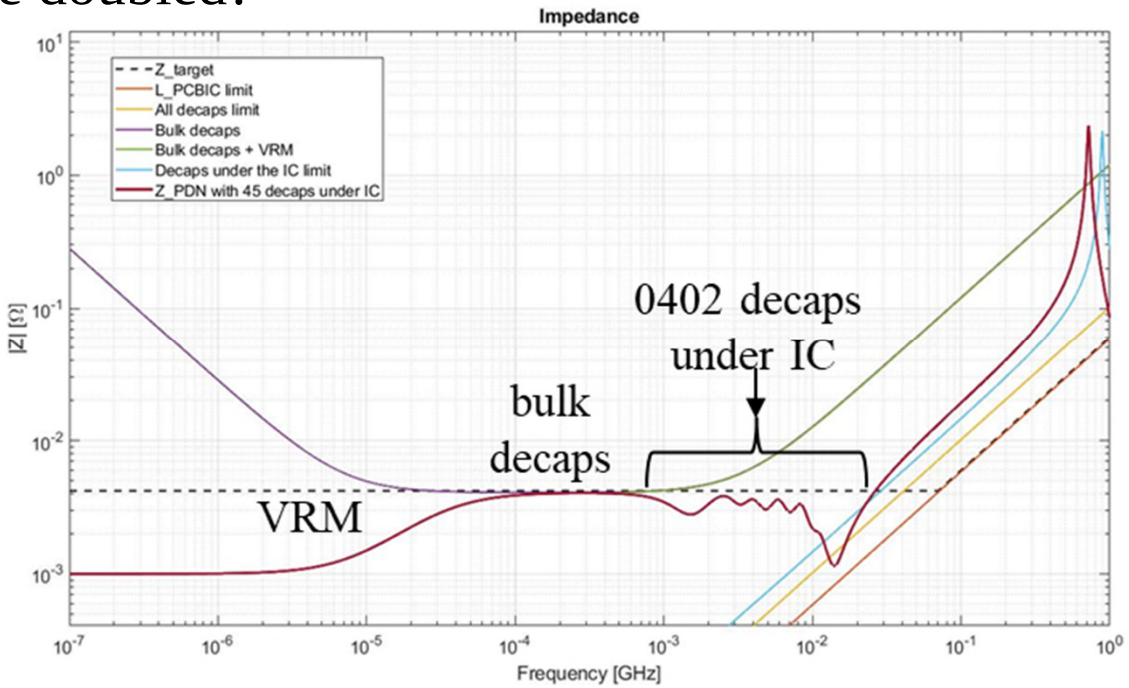
Consider the IC to have >100 PWR pins (and associated GND return) such that LPCB IC is very small. And that many decaps can be added.

Example

- 18 layer PCB
- Layer 2 is the power layer
- 45 power pins, 109 surrounding GND
- 45 decaps under the IC

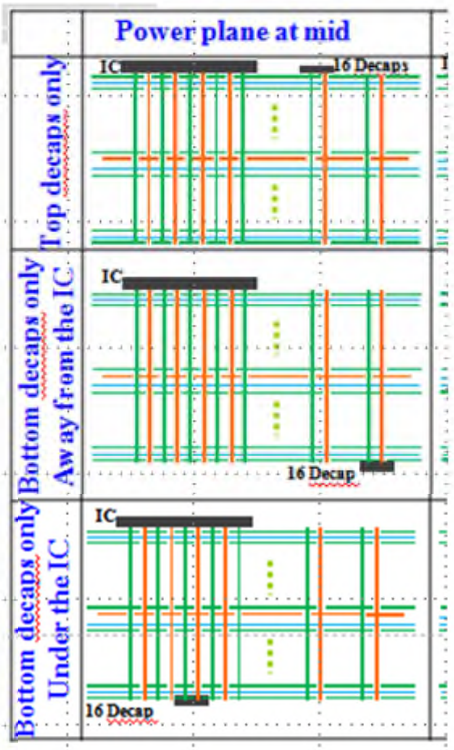
Q: What happens if the number of IC pins are doubled?

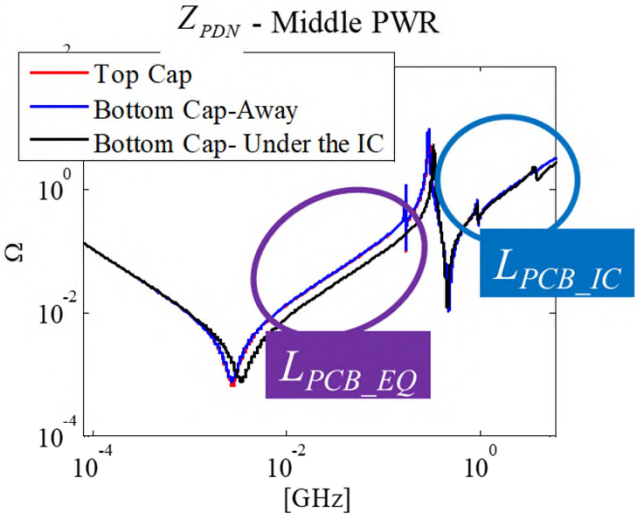


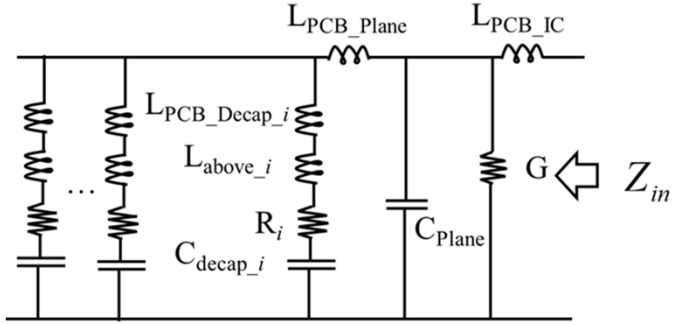


Key Points

- The Z_{PDN} response can be related to the geometry, current path and associated inductance.
- The dominant component in the impedance equivalent circuit can be identified and used to explain the behavior of the PDN response, and to guide the PDN design.







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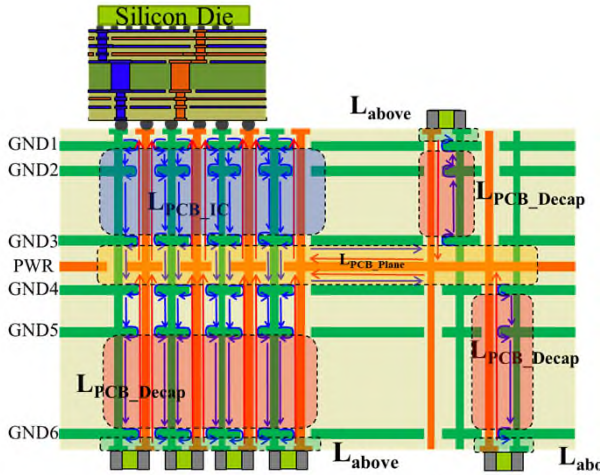
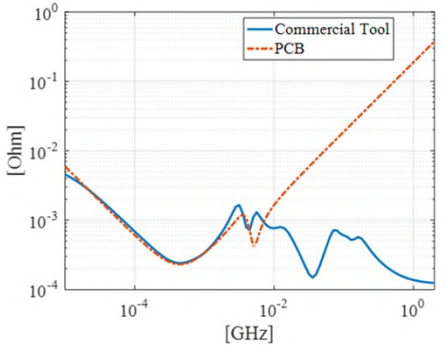
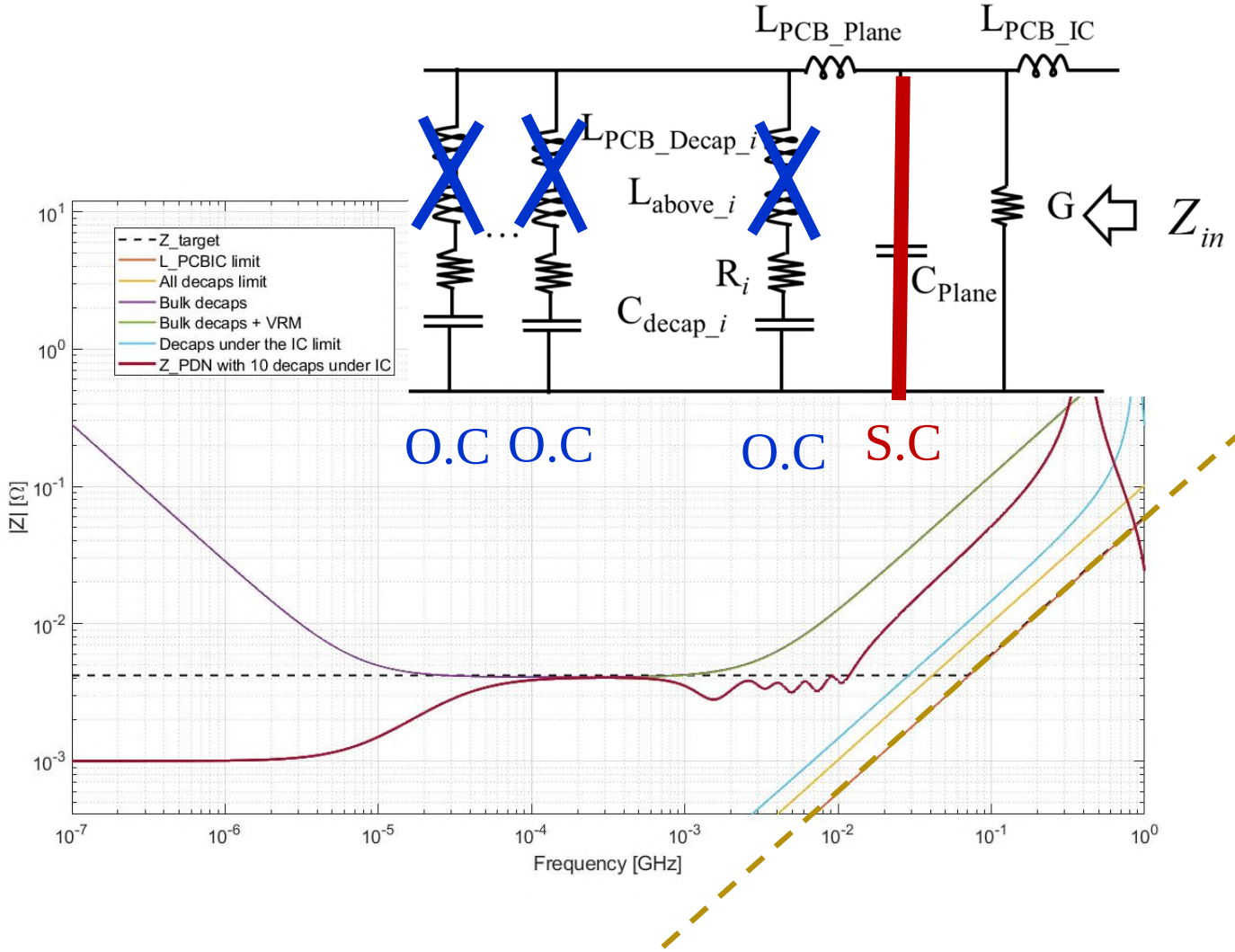
  - $L_{PCB\ IC}$
  - Decaps under the IC
  - All decaps



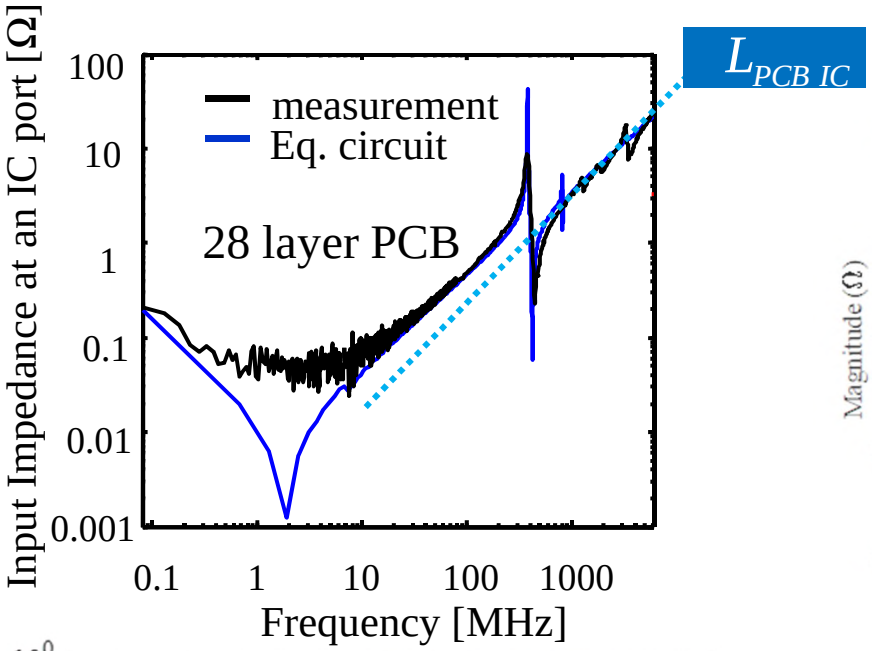


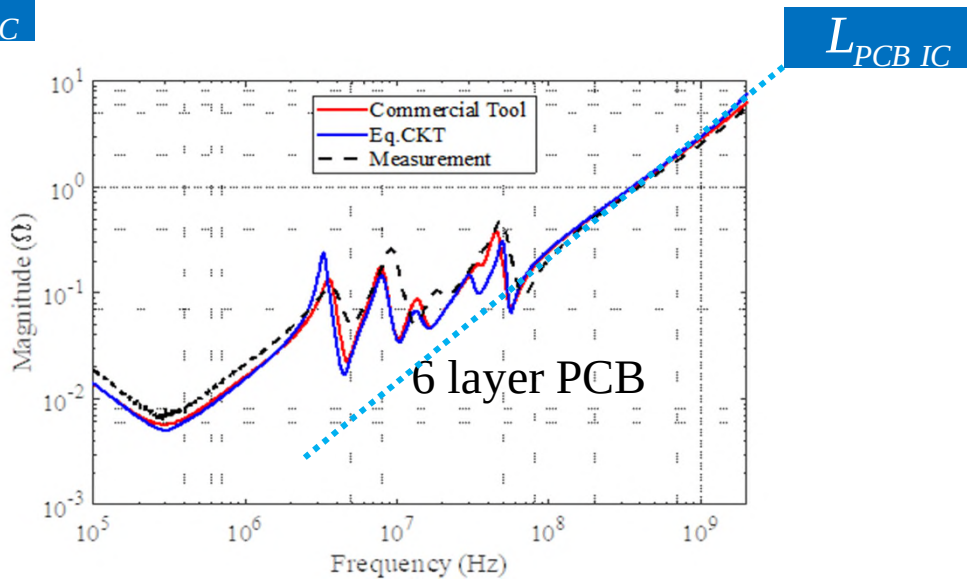
$L_{PCB\ IC}$ Physical Limit

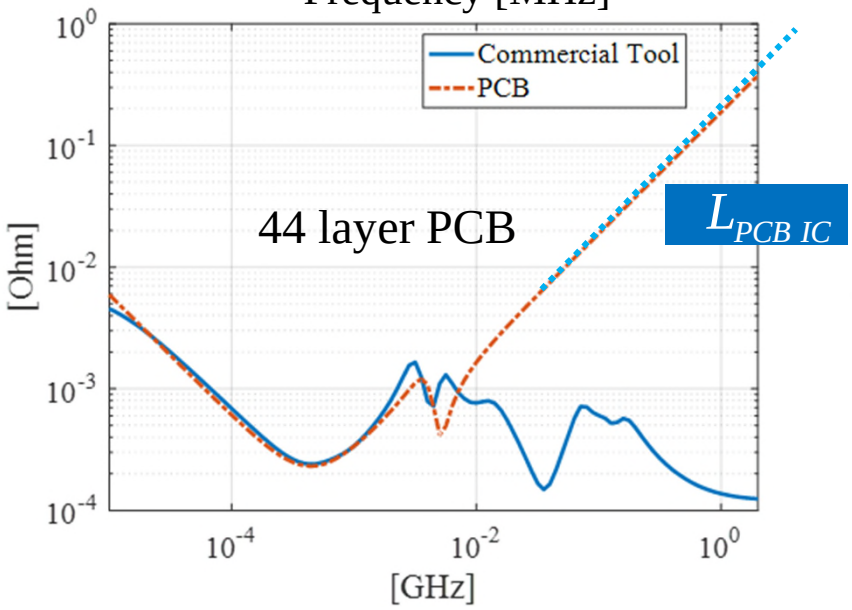
$L_{PCB\ IC}$ is the physical limit at high frequencies when the current returns through the interplane capacitance of the power net area fill and return

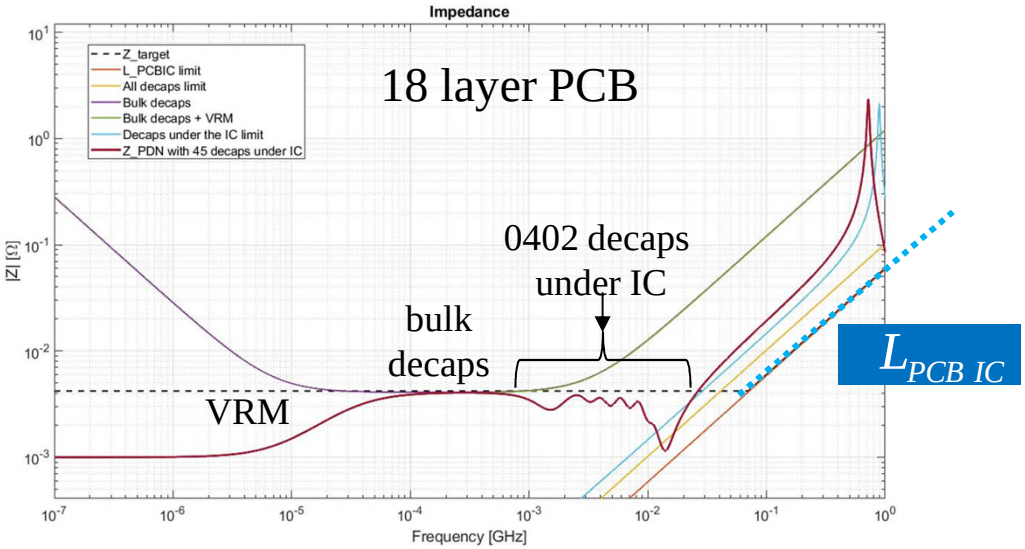


Real Board $L_{PCB\ IC}$ Examples









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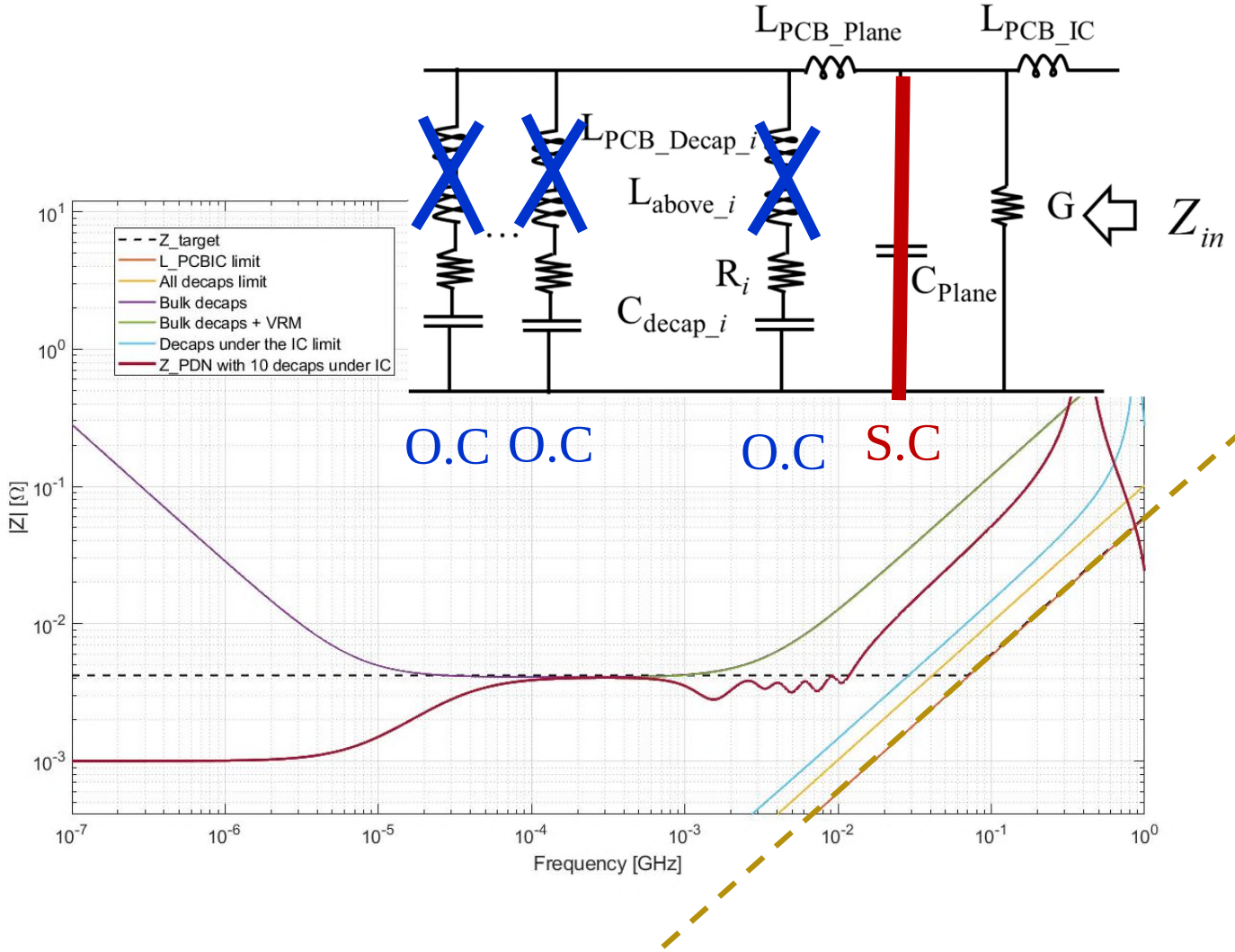
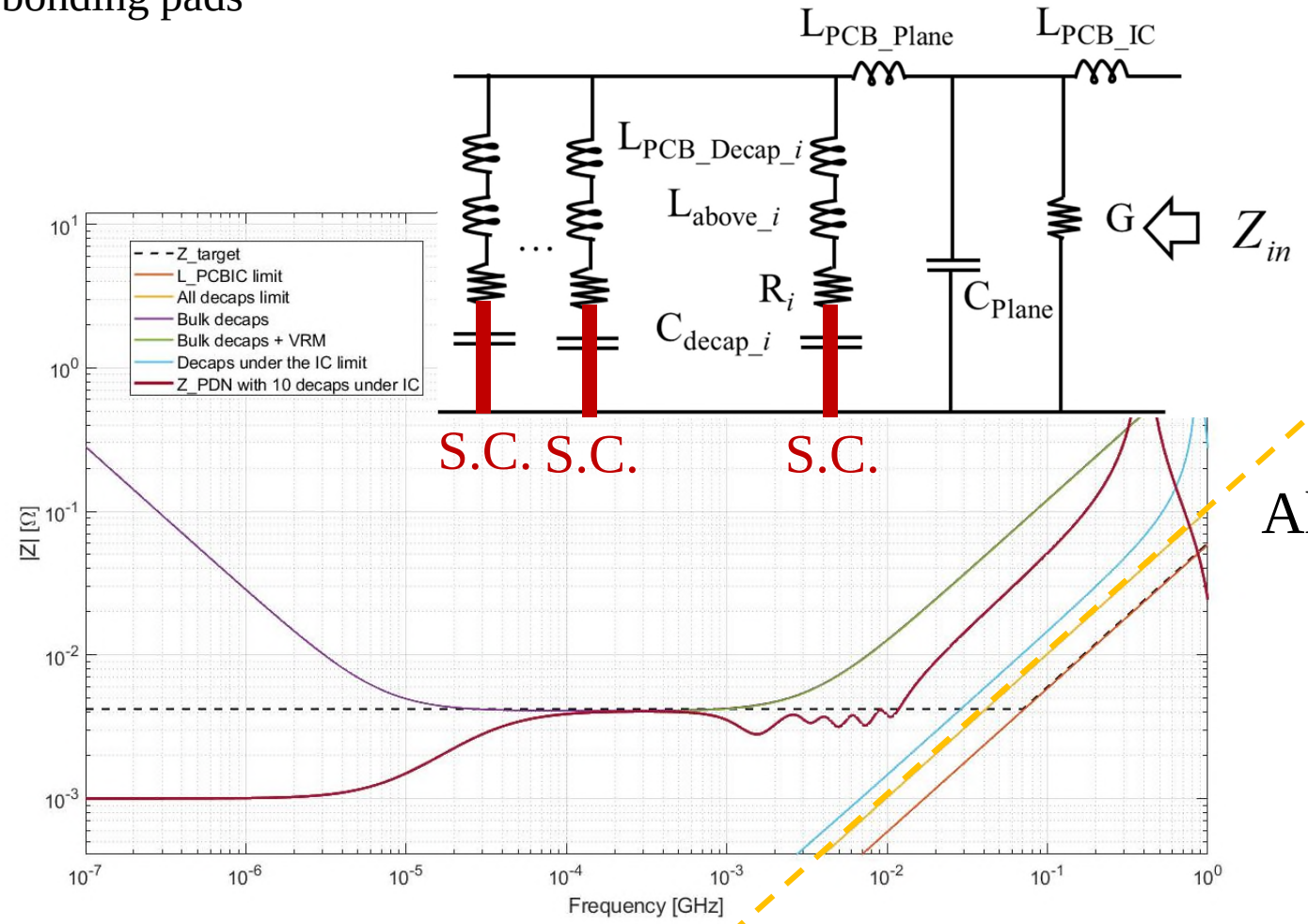


All Decaps Physical Limit

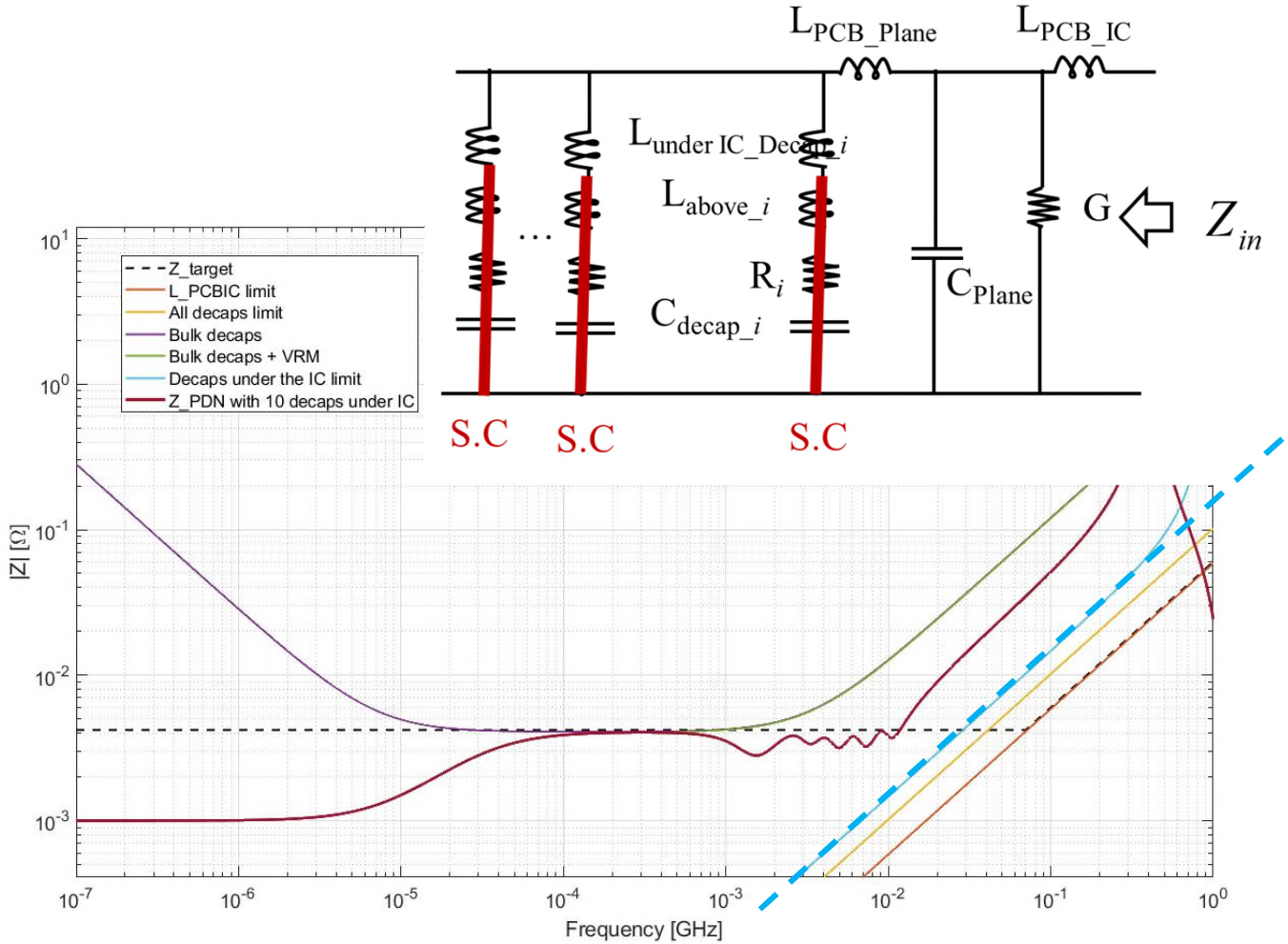
The All Decaps physical limit is when shorts are placed across all decap locations under the IC, and a ring of many capacitor locations on the top and bottom of the PCB are shorted at the bonding pads



All decaps limit

Decaps Under the IC Physical Limit

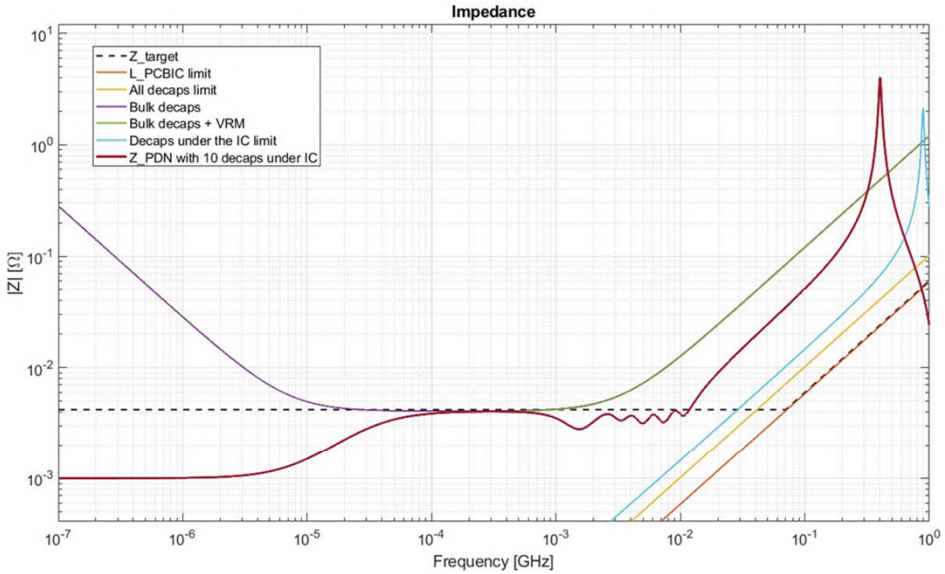
There is a physical limit when all the power pins under the IC are shorted on the bottom layer that corresponds to placing all possible decaps under the IC

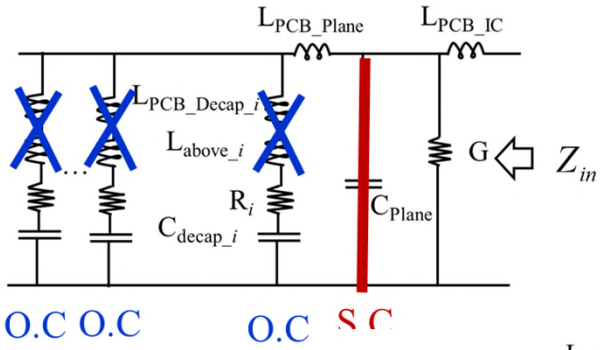


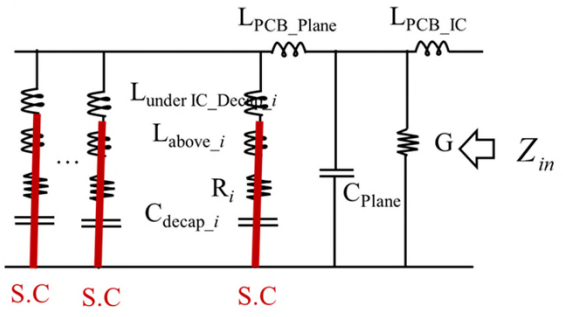
Decaps under the IC limit

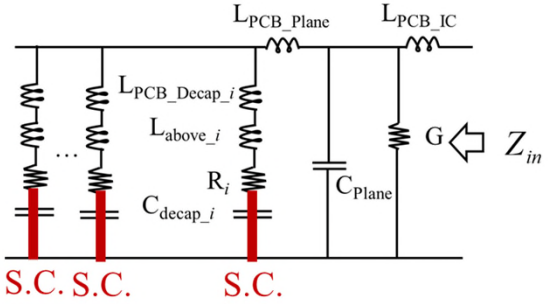
Key Points

- Physical limits can be established for the upper bound of placing decoupling capacitors at various locations
  - $L_{PCB\ IC}$
  - Decaps under the IC
  - All decaps
- If the target impedance cannot be met due to a particular limitation, the nature of the limitation and the impedance equivalent circuit can guide the design direction.









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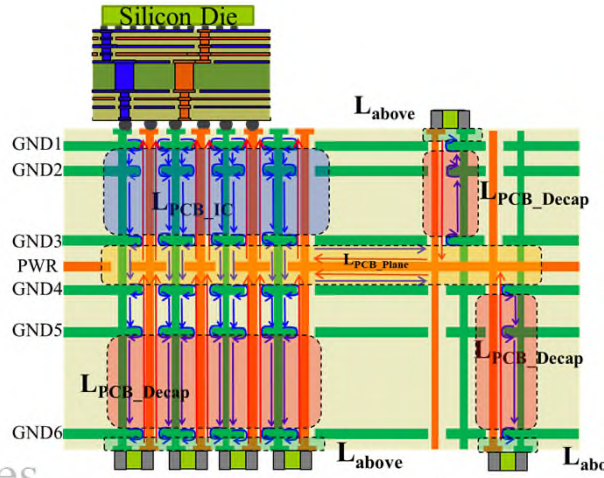
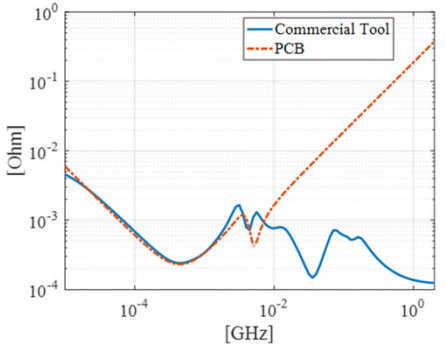
- Identifying limiting physics in design
- Adding decoupling capacitors
  - ***Values of decaps to use***
  - Where to place around the IC
  - Connecting the decap to the PCB
  - Convergence of $L_{PCB\ Decap}$ for large number of decaps



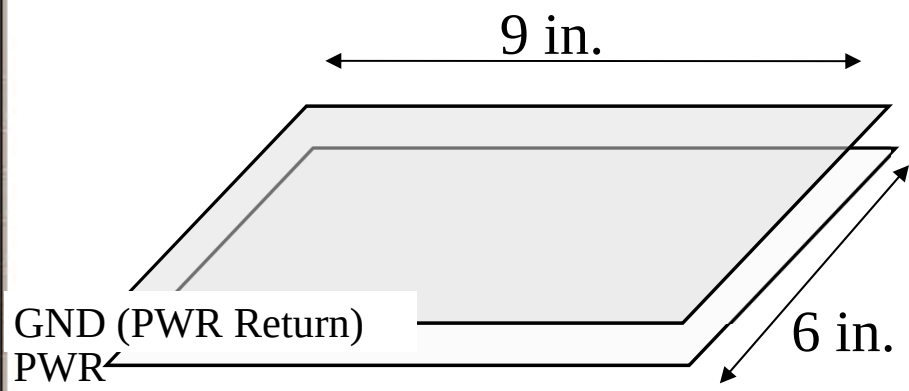


Two Approaches for SMT Decoupling

- Use an array of capacitor values:
  - This may be the best known approach in the signal integrity design community
  - Rationale: to maintain a flat impedance profile below a target impedance over a wide frequency range
  - Typically a logarithmically spaced (10, 22, 47, 100, 220, 470nF, etc.) array of several values per decade.
- Use a large capacitor value in the package size
  - This is less well-known, but an approach in the EMI design community
  - Rationale: to keep impedance as low as possible, less emphasis on a target impedance and a flat profile

Decoupling Strategy – Geometry

Capacitor Description					# of Caps		
Value (nF)	ESR (mΩ)	ESL (nH)	Inter-connect (nH)	Type	A	B	B1
3.30E+06	60	15	2	E-lytic	1	1	1
100000	11	1.4	2	1812	4	16	16
47000	12	1.4	2	1812	4		
22000	14	1.4	2	1812	4		
10000	16	1.4	2	1812	4		
4700	16	0.5	1.6	0603	4	24	
2200	19	0.5	1.6	0603	4		
1000	23	0.5	1.6	0603	4		
470	29	0.5	1.6	0603	4		
220	23	0.5	1.6	0603	4		
100	30	0.5	1.6	0603	4		
47	40	0.4	1.35	0402	4	20	44
22	55	0.4	1.35	0402	4		
10	75	0.4	1.35	0402	4		
4.7	104	0.4	1.35	0402	4		
2.2	211	0.4	1.35	0402	4		
Total # of Decoupling Capacitors =					61	61	61
Total Capacitance (milliF) =					4.05	5.01	4.90



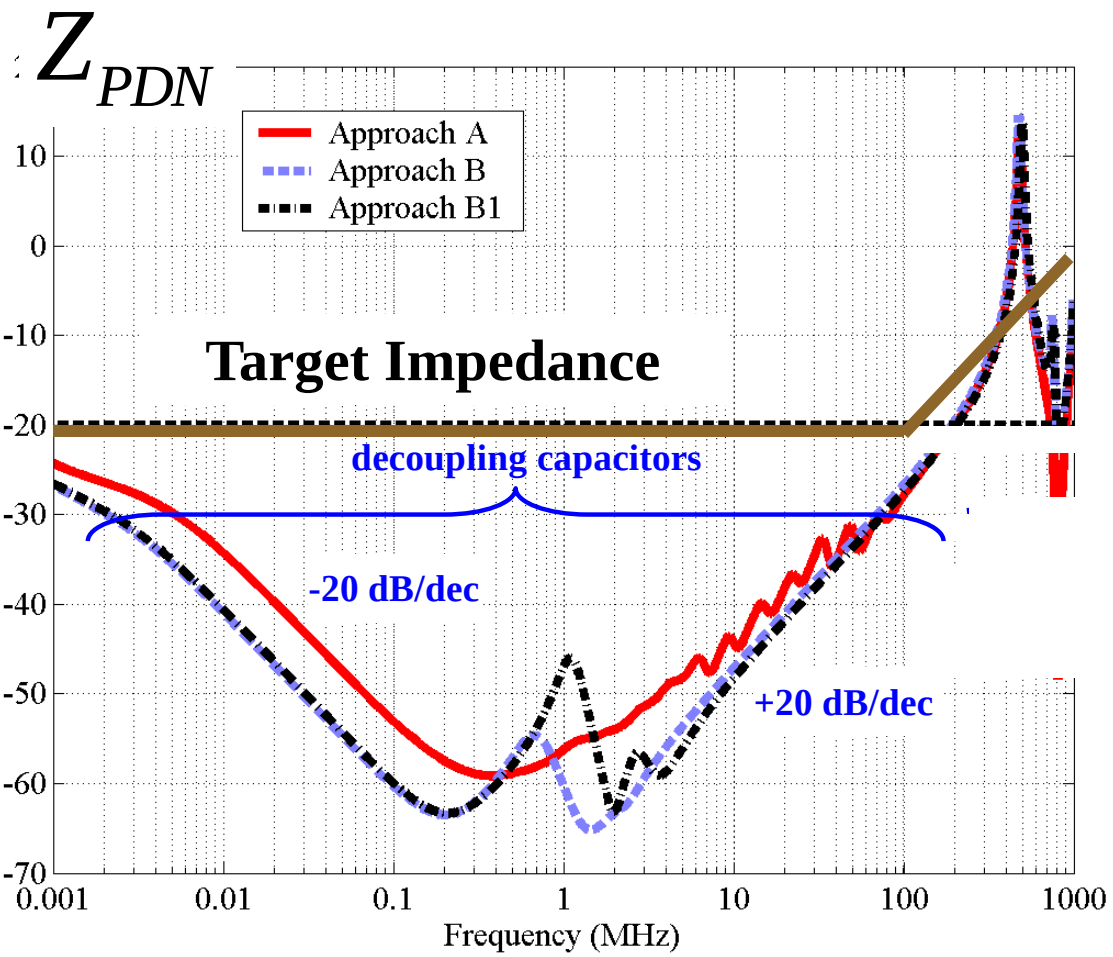
t=10 mils.

$\tan \delta = 0.02$

$\varepsilon_r = 4.5$

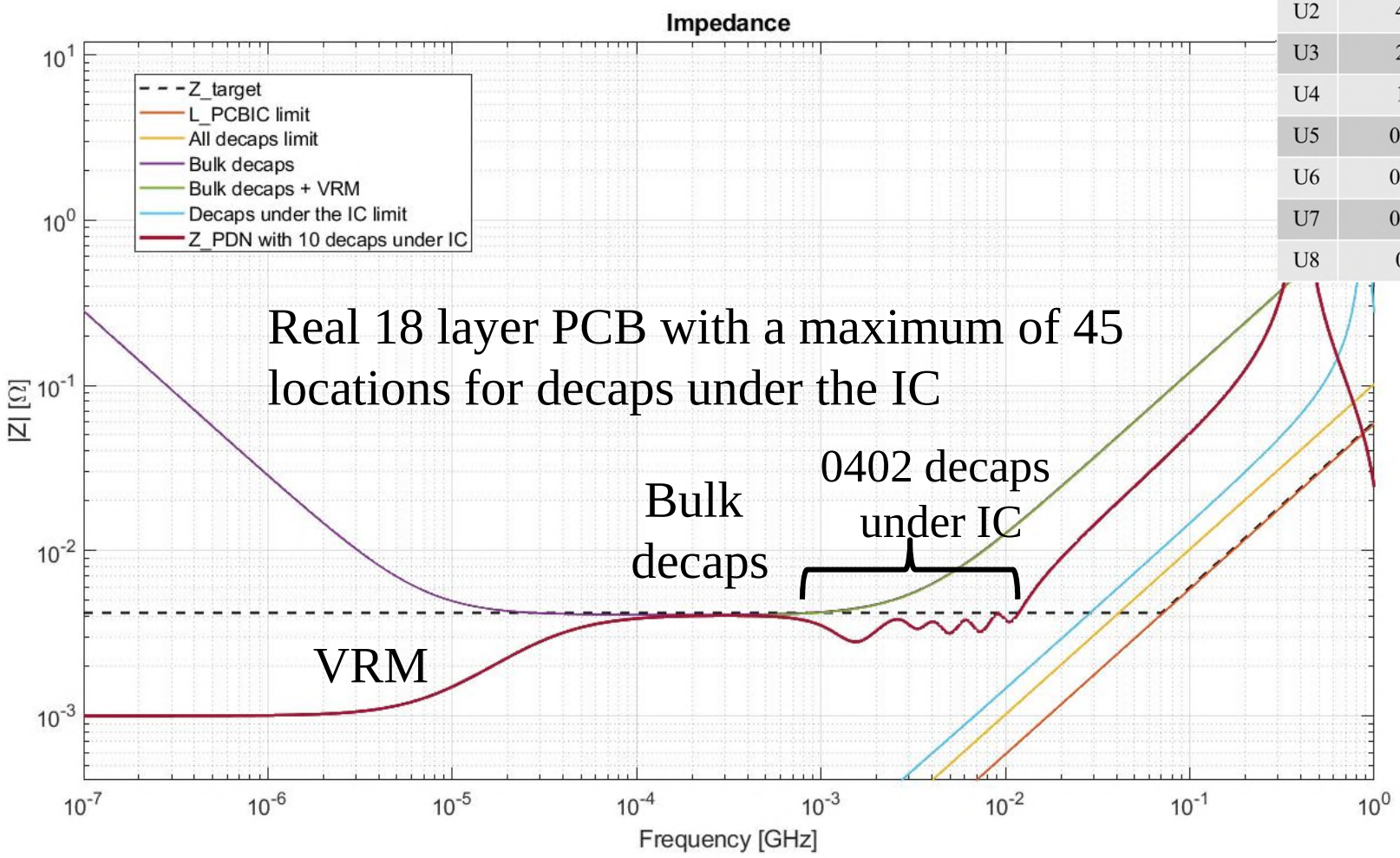
Approaches for SMT Decoupling Values

- Approach A : values of decoupling capacitors logarithmically spaced, i.e. 3 values per decade: 10, 22, 47, 100, etc.
- Approach B : largest values of decoupling available in two package sizes, i.e., 0603 and 0402
- Approach B1 : largest values of decoupling available in one package size, i.e., 0402.

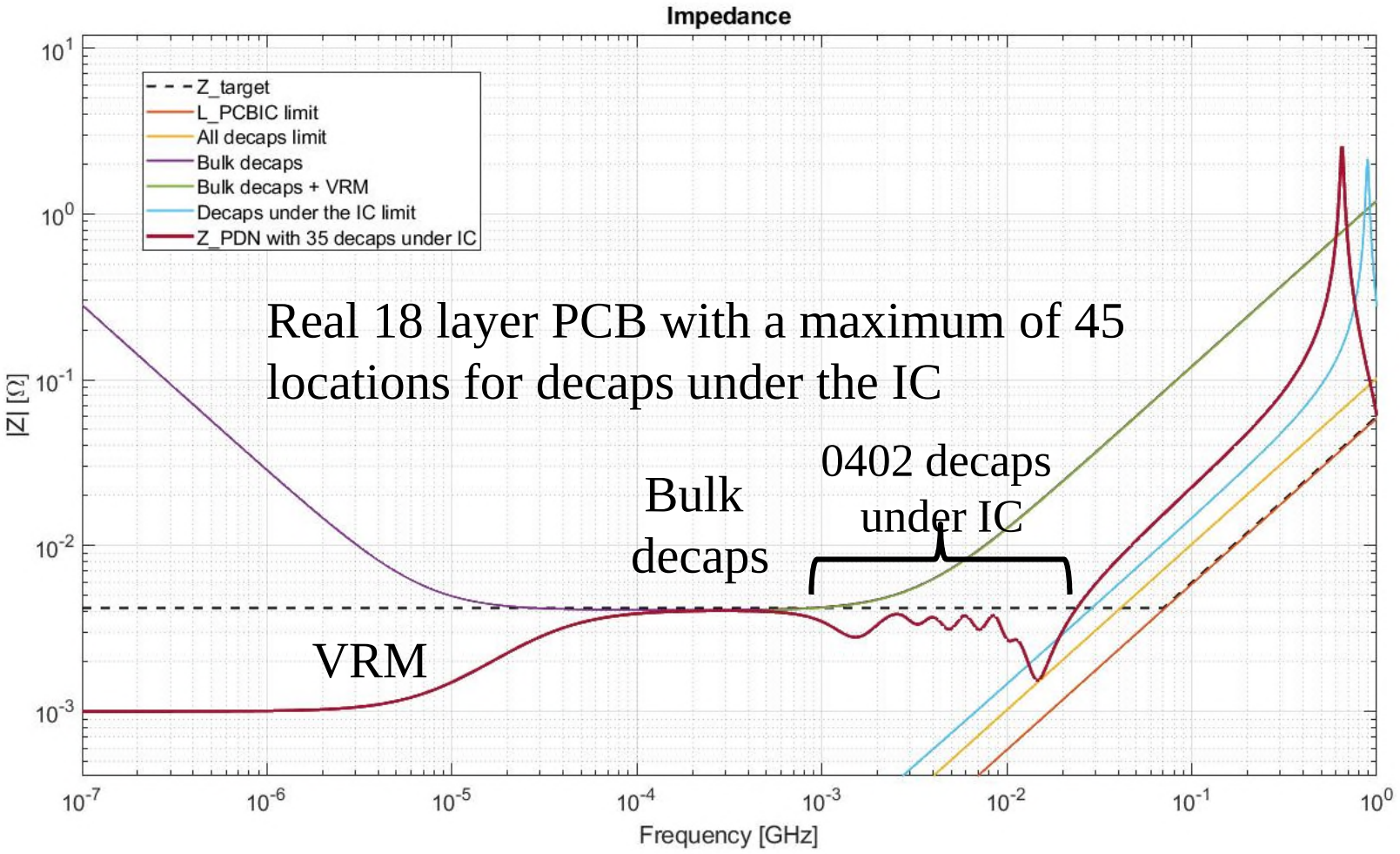


Optimizing Algorithm –10 decaps

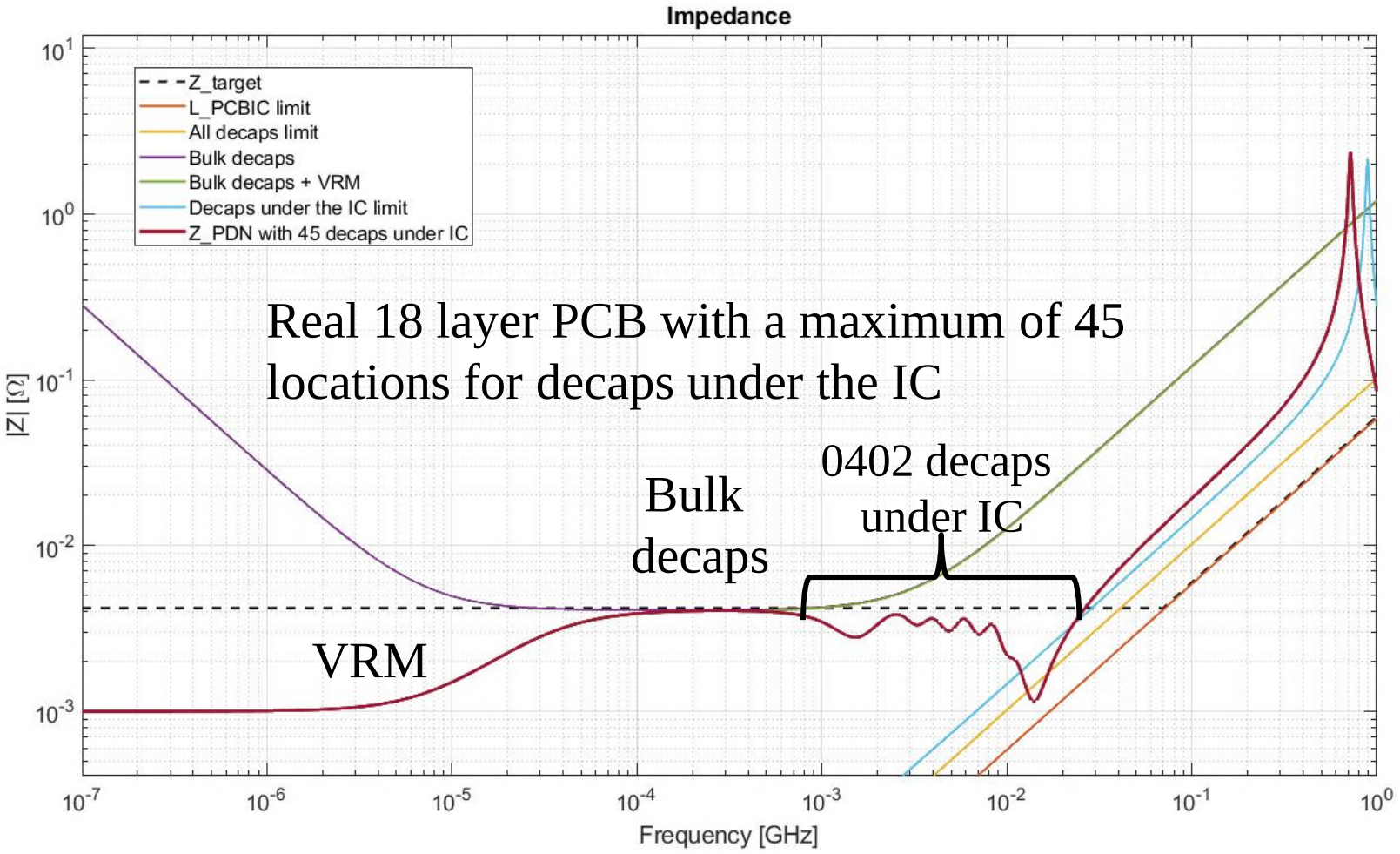
	C(uF)
U1	10
U2	4.7
U3	2.2
U4	1.0
U5	0.47
U6	0.22
U7	0.15
U8	0.1



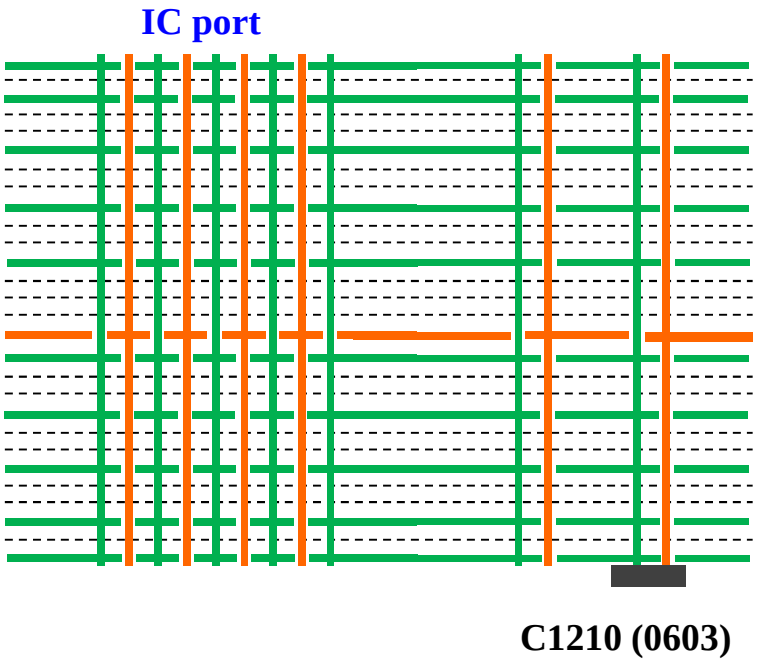
Optimizing Algorithm –35 decaps

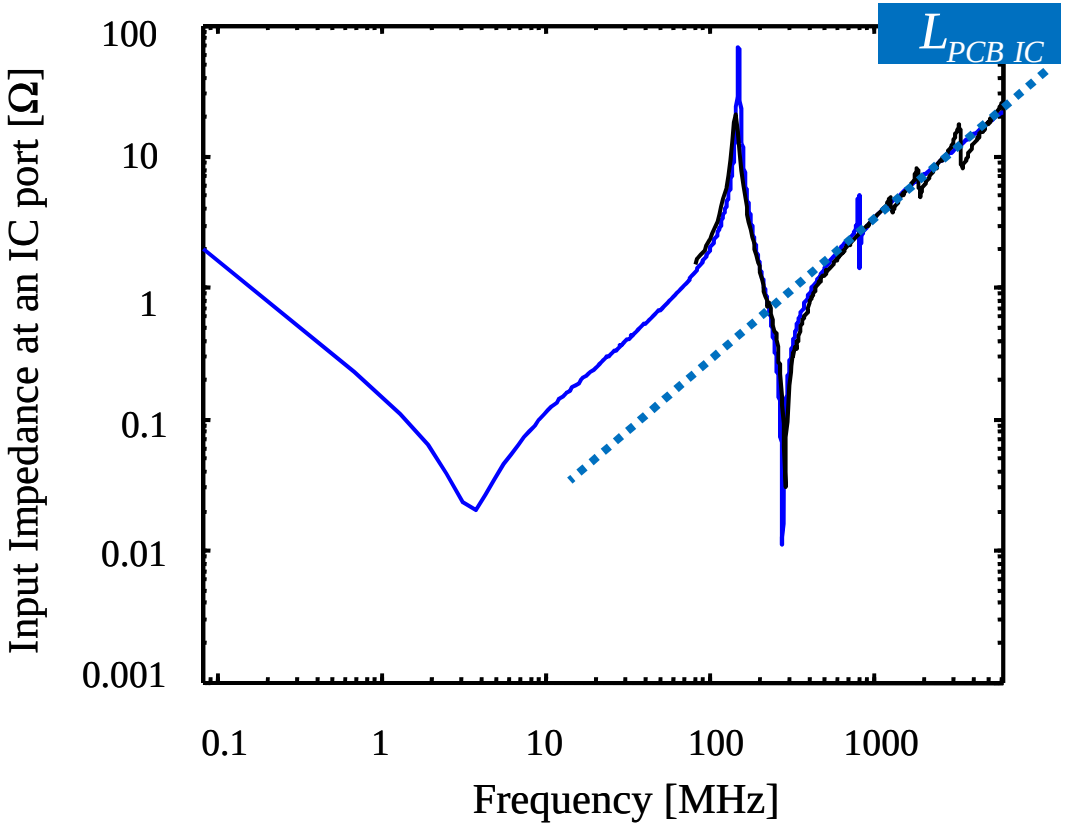


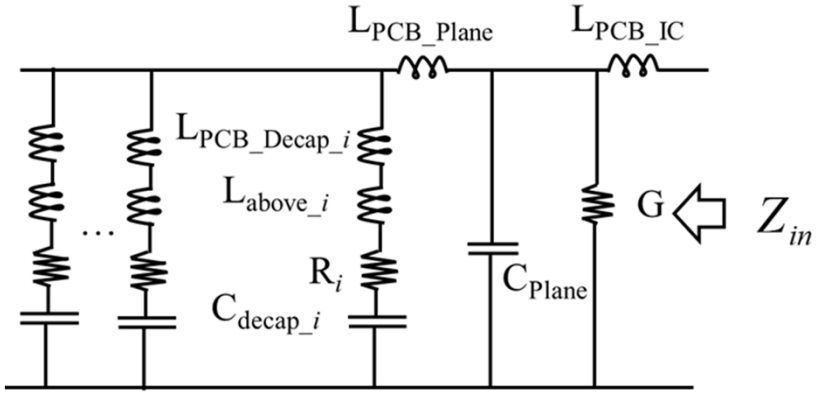
Optimizing Algorithm –45 decaps



28 Layer Real PCB Design: 1 Capacitor



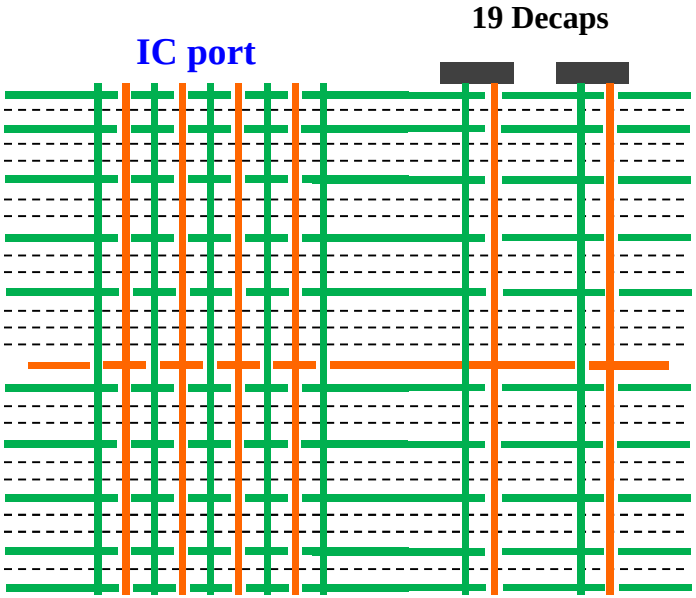


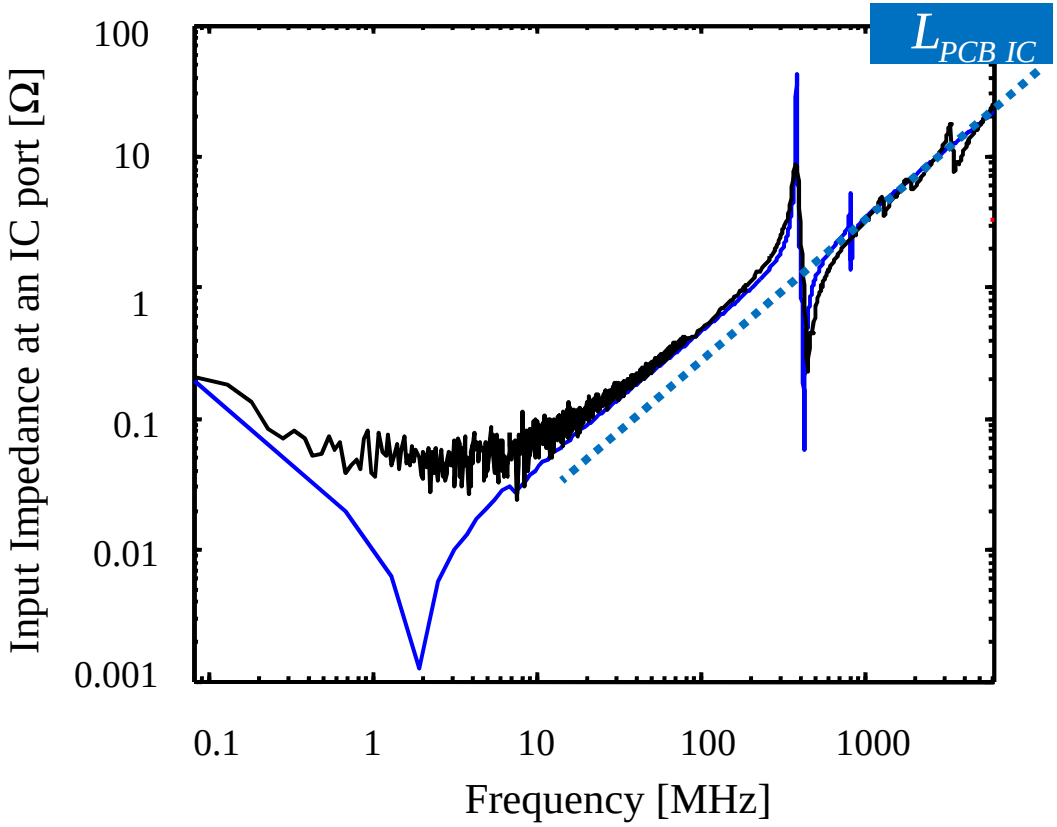


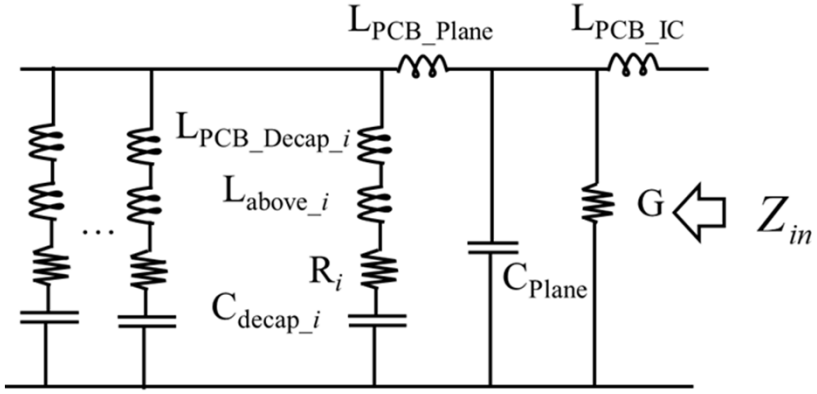
Measurement

Circuit Model

28 Layer Real PCB Design: 19 Capacitors



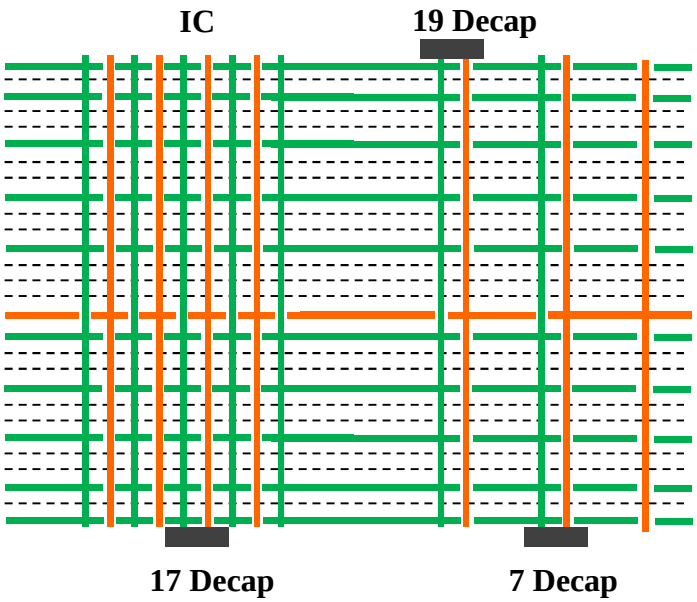


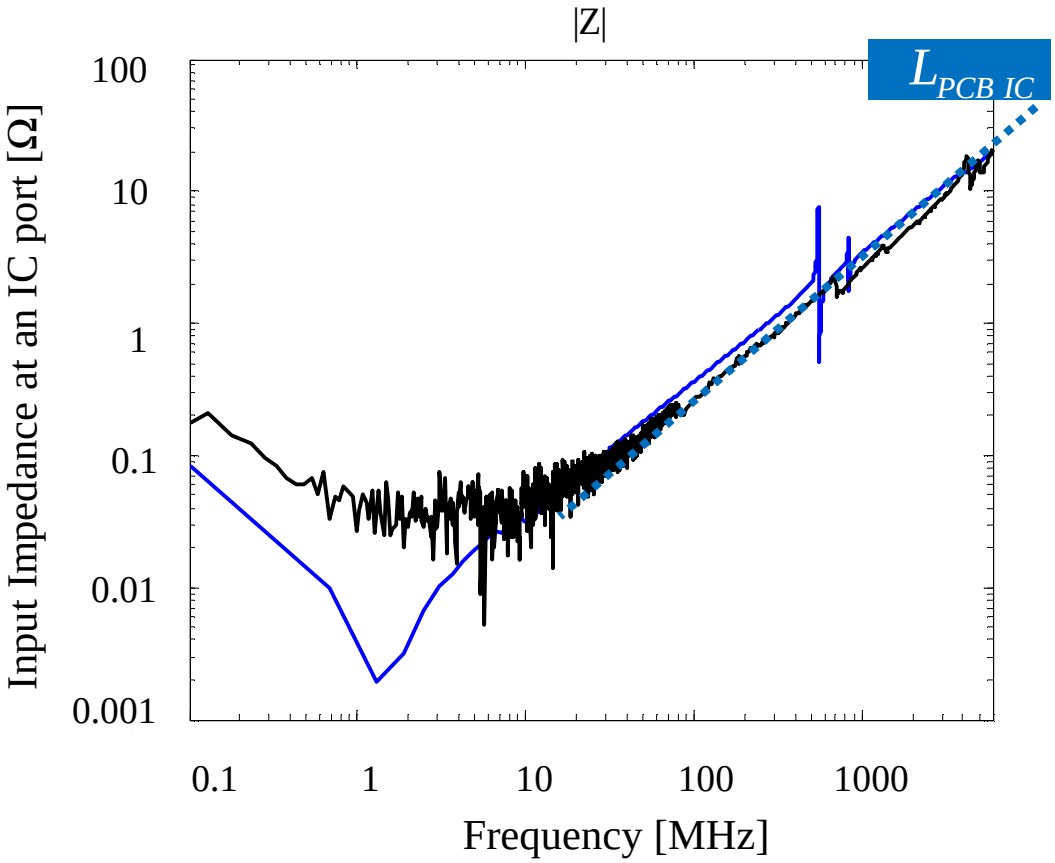


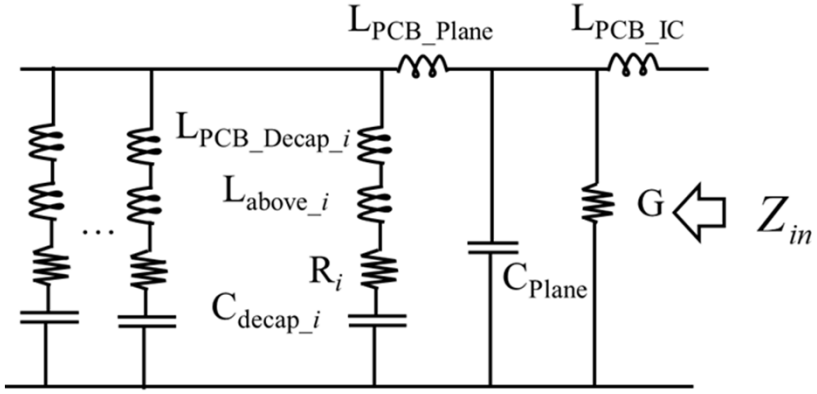
Measurement

Circuit Model

28 Layer Real PCB Design: 43 Capacitors





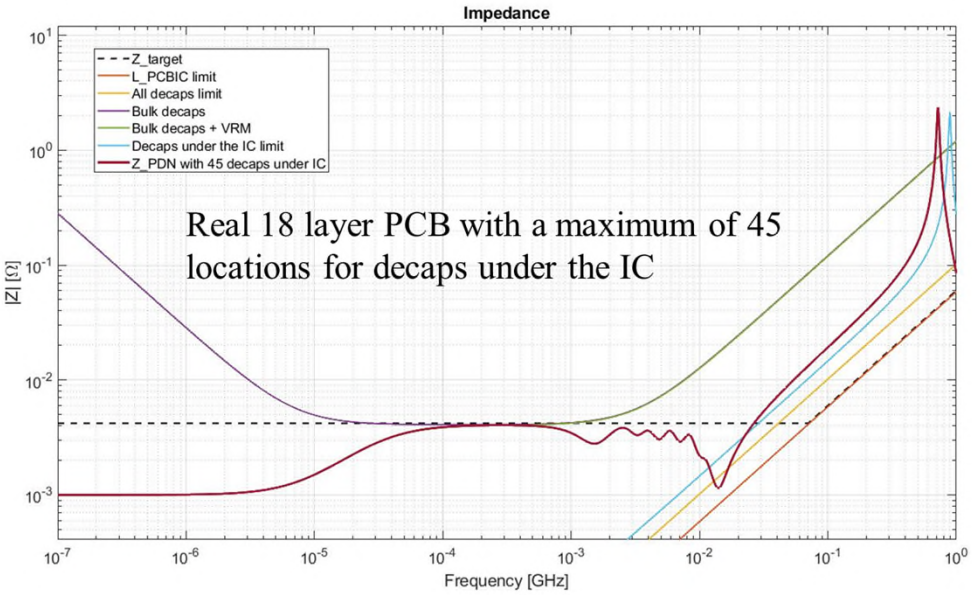


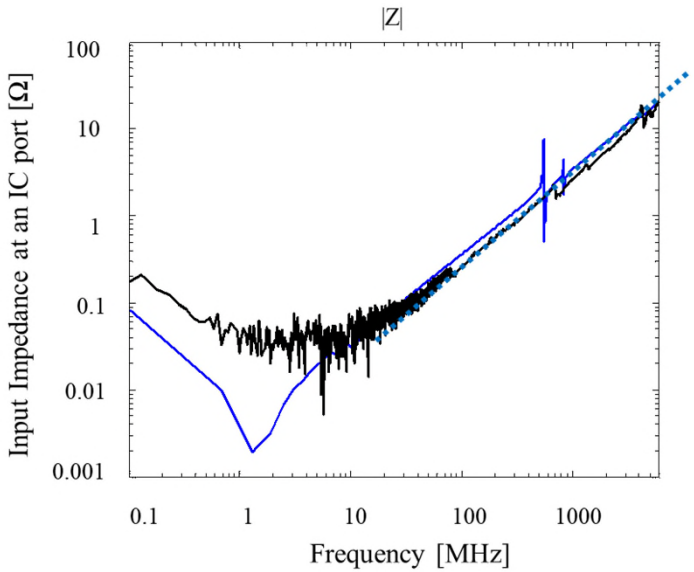
Measurement

Circuit Model

Key Points

- Decoupling capacitors can be added using several values in a given decade to decouple over wide frequency ranges
- Decoupling capacitors can be added as the largest value in a package size to achieve a target impedance as well.





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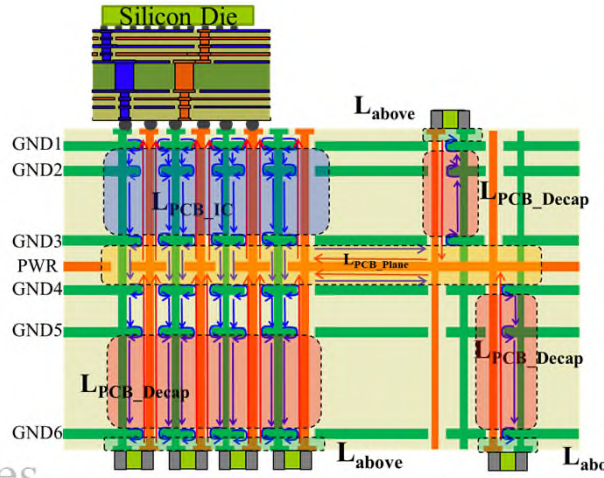
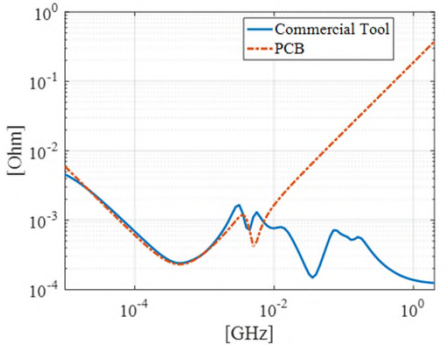
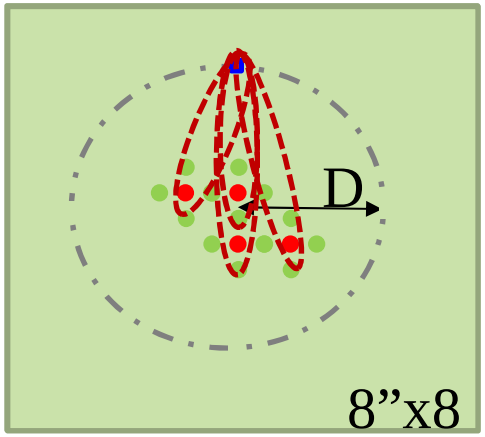
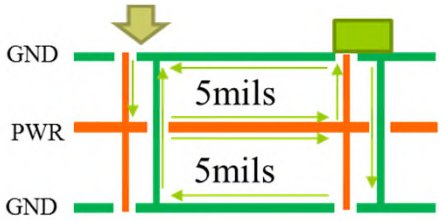
  - Convergence of $L_{PCB\ Decap}$ for large number of decaps

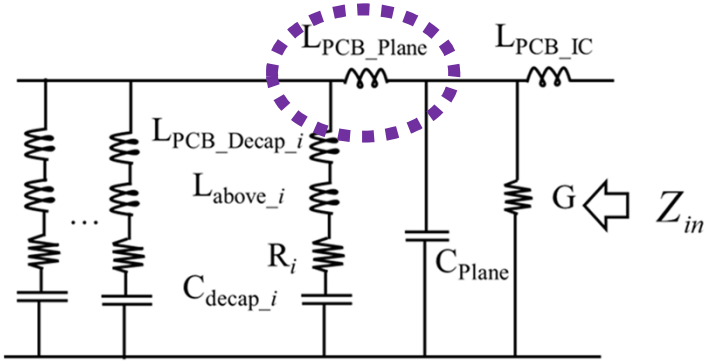




L_{PCB_Plane} Current Physics and Inductance



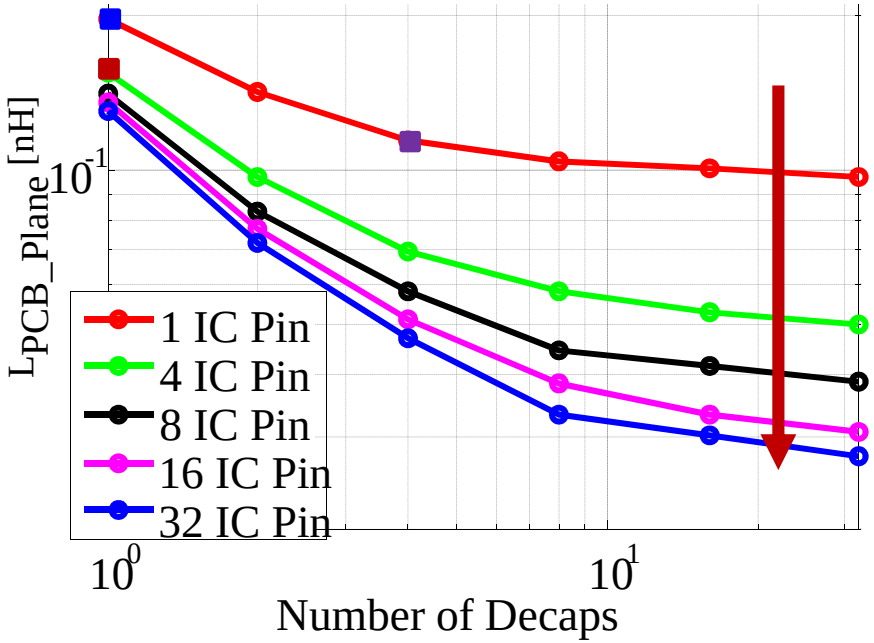


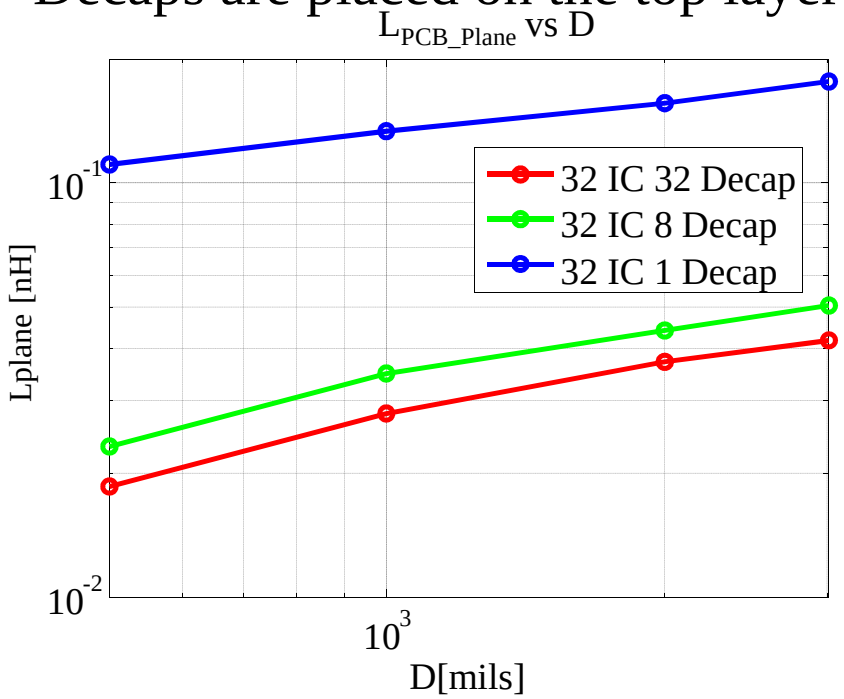


D=1’’, Pitch = 1mm

Decaps are placed on the top layer

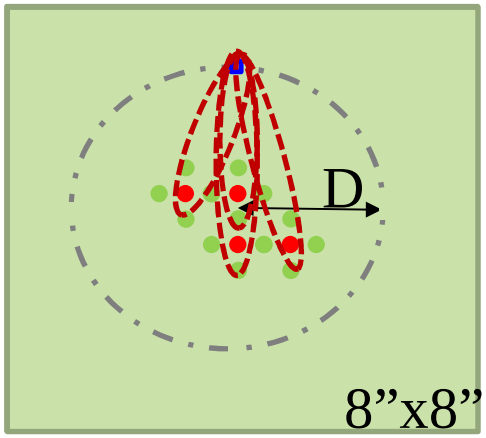
L_{PCB_Plane} decreases with multiple parallel paths

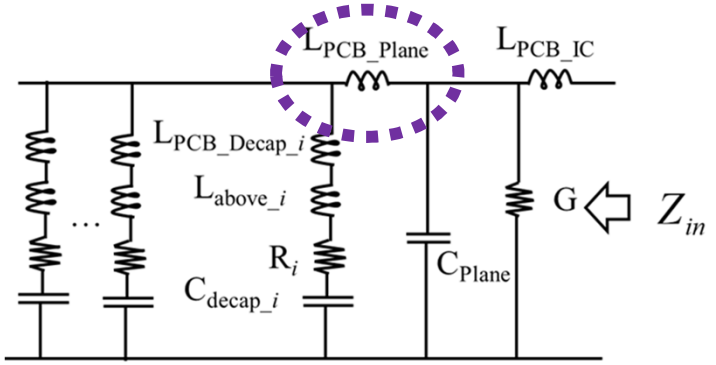


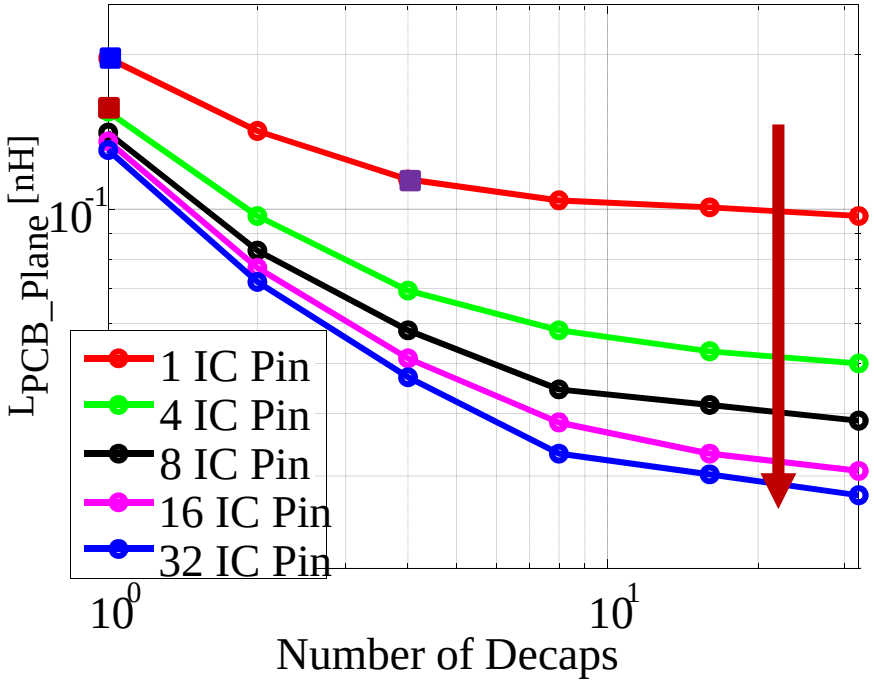


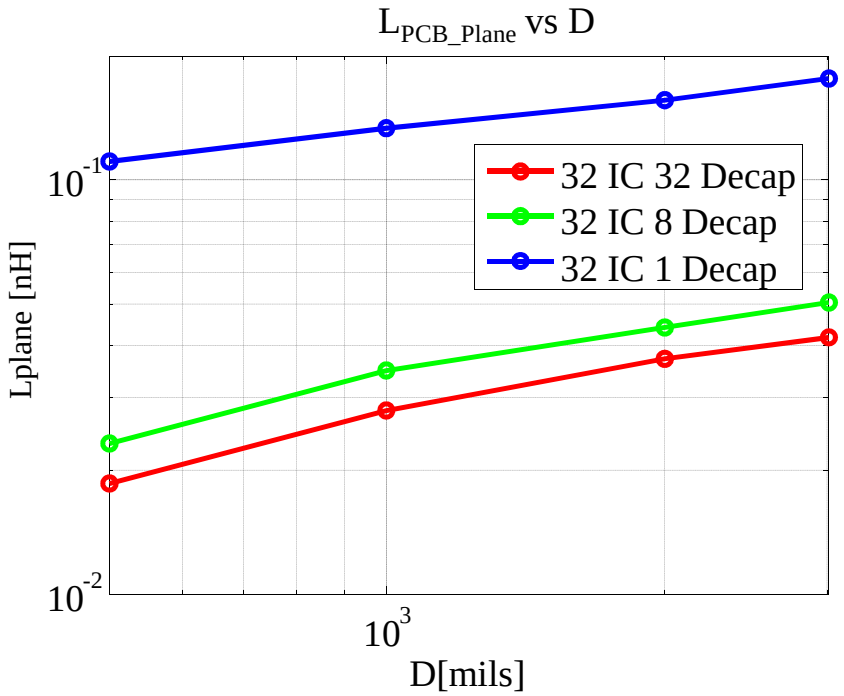
L_{PCB_Plane} Current Physics and Inductance

Q: When is placing capacitors in a ring around the IC most beneficial?

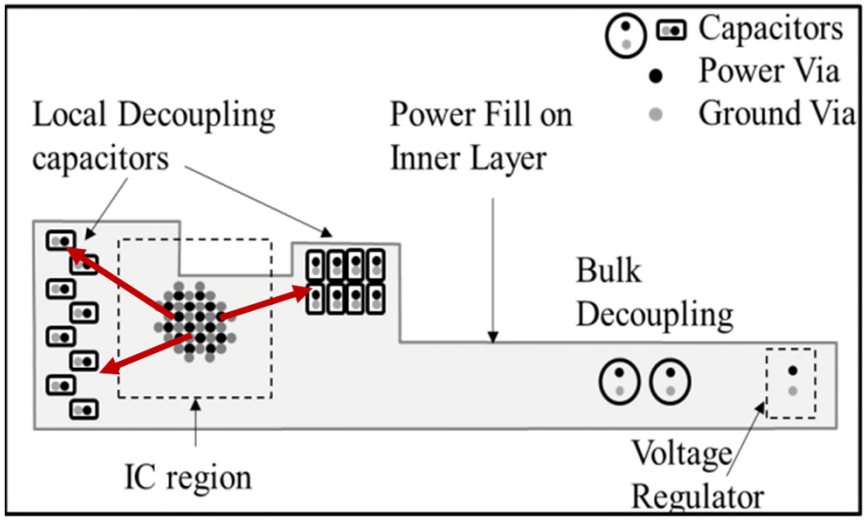


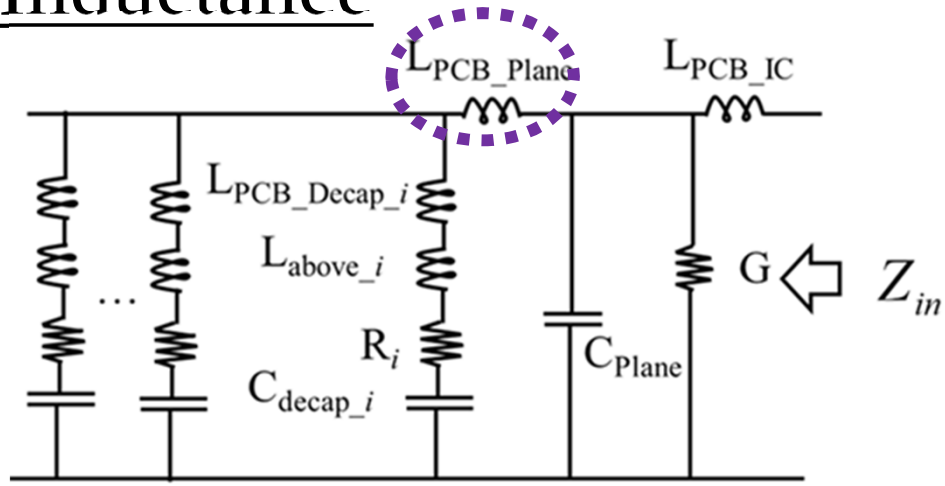


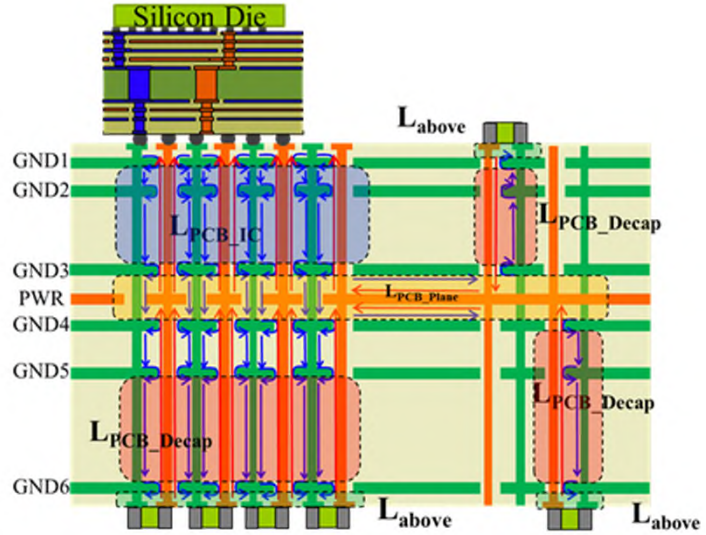




Current Path, and Inductance



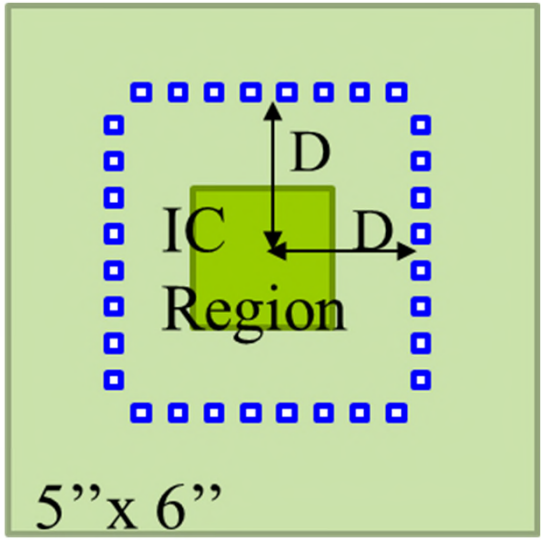


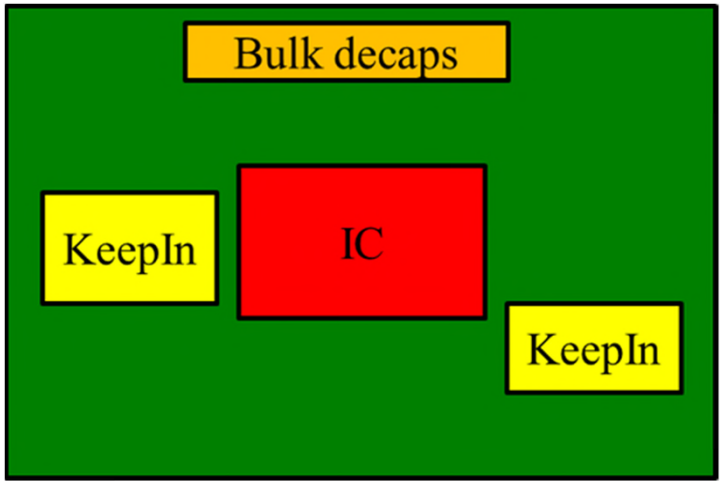


Q: If the current path from IC to the decaps is not in direct line (e.g., crosses a cutout or slot, goes around a corners, etc.), which portion of the inductance is affected, and can potentially become dominant?

Key Points

- If $L_{PCB\ Plane}$ is dominant, e.g., when the power net area fill is near the top, and the decaps are placed on the top layer, then placing the capacitors in a ring around the IC can minimize $L_{PCB\ Plane}$
- In general, $L_{PCB\ Plane}$ is typically not the limiting factor, and decaps are often limited to “keep-in” regions where signal routing channels are not compromised.





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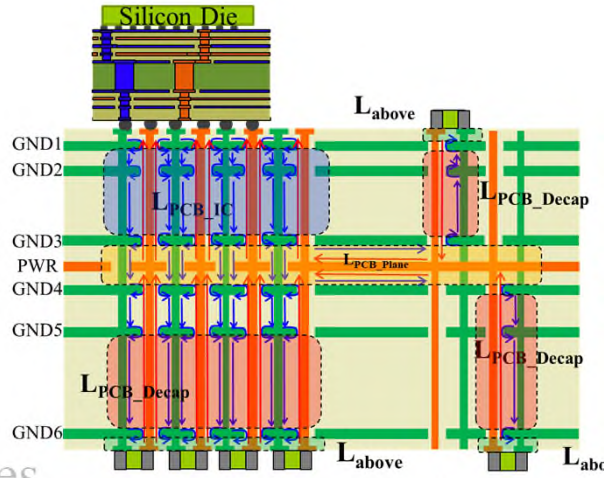
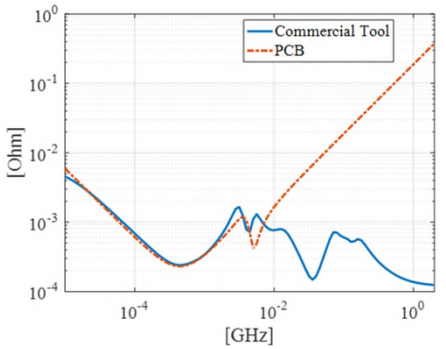
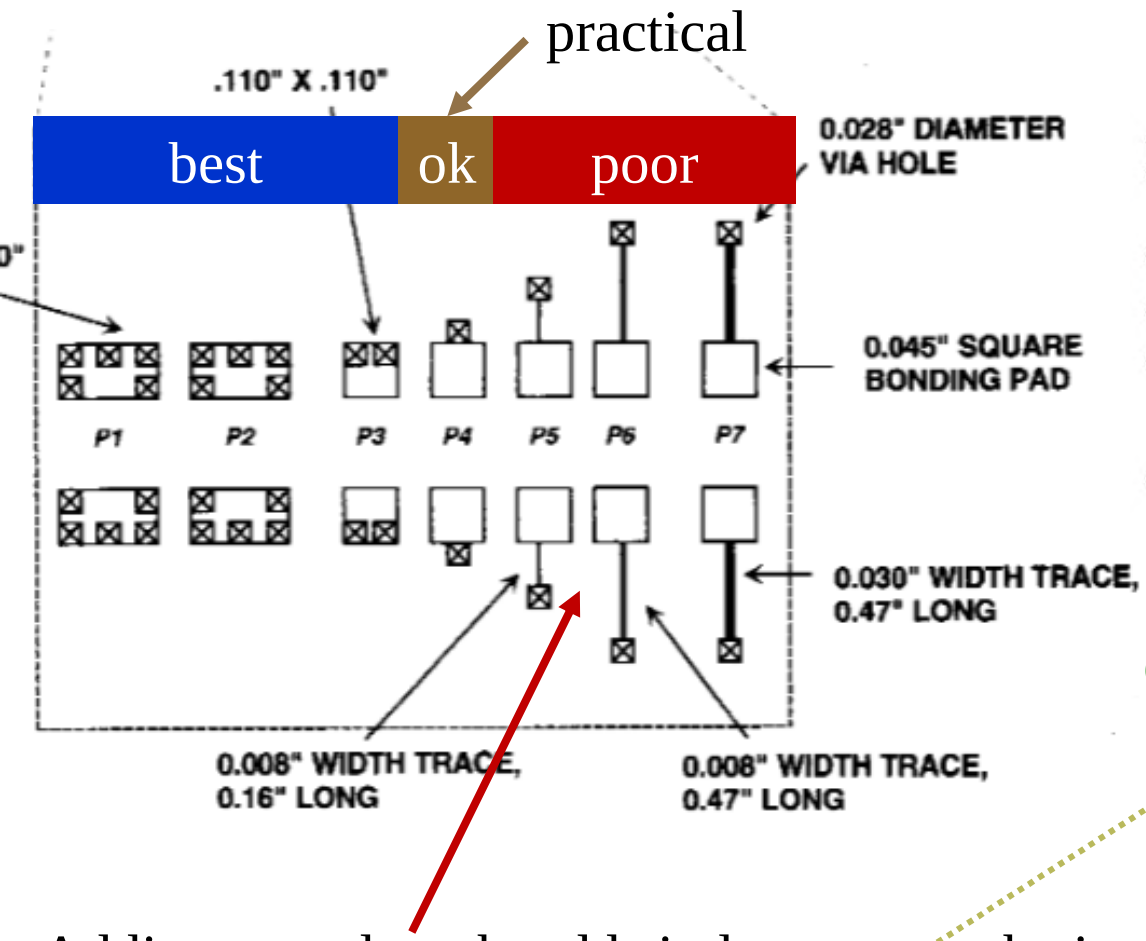
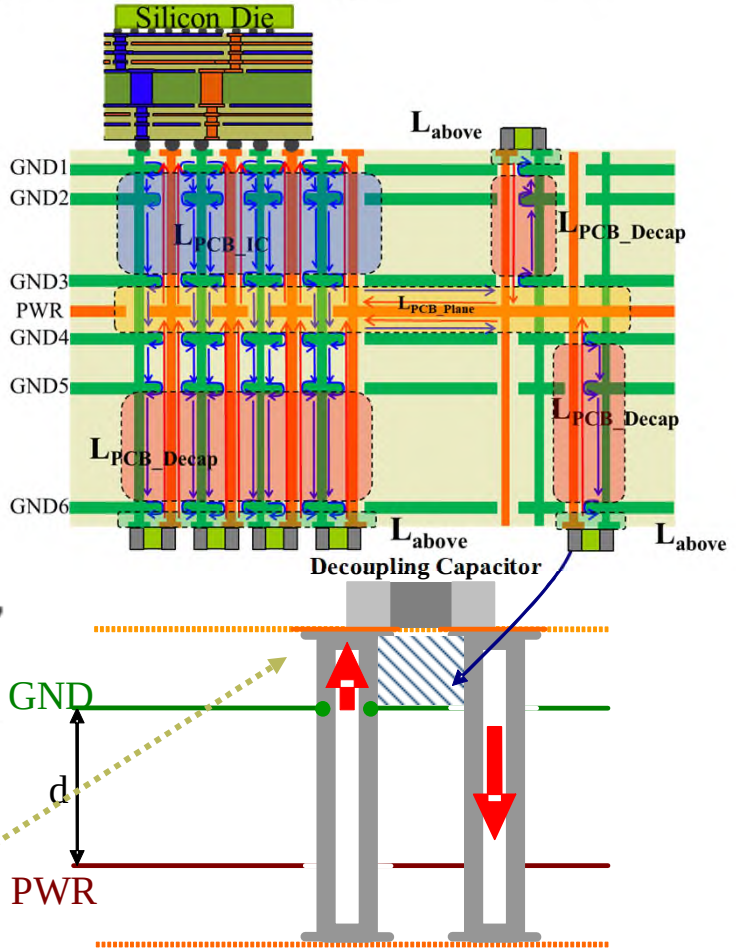




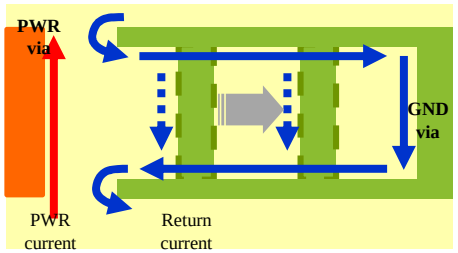
Practices for Mounting SMT Capacitors





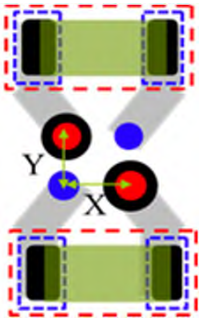
Adding trace length, adds inductance to the interconnect:

- "loop area" above the planes – L_{above}
- Area between the power and GND return vias vertically connecting to the PWR planes

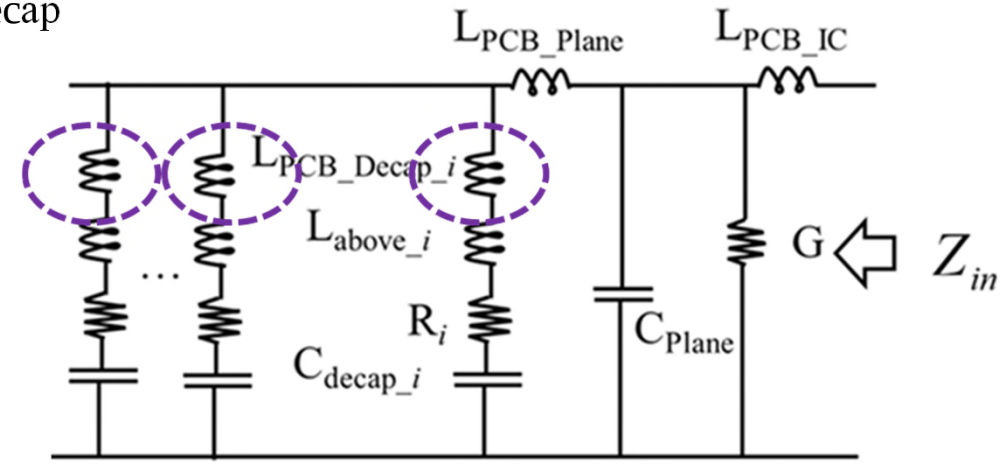


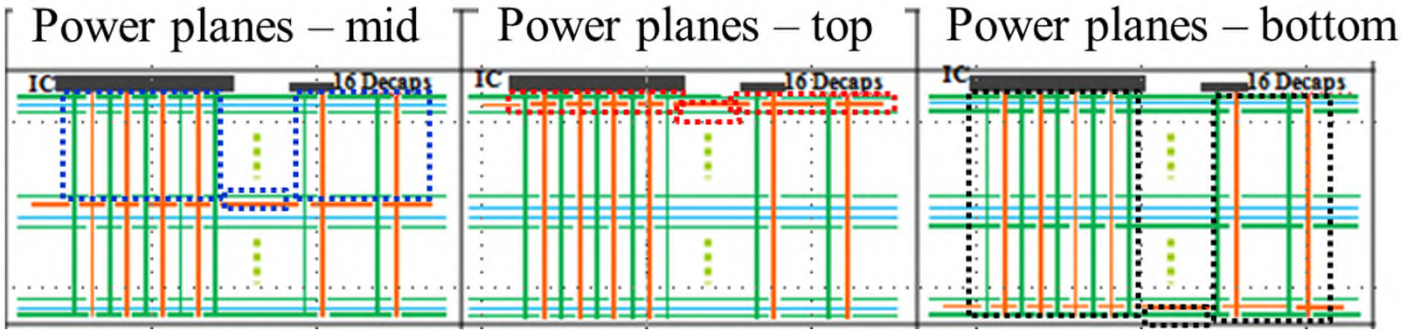
Example 1: The Doublet – Minimizing $L_{PCB\ Decap}$

Placing decaps on in pairs allows to use mutual inductance to minimize overall $L_{PCB\ Decap}$



- GND via
- PWR via

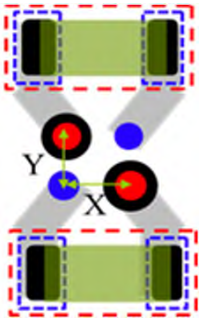


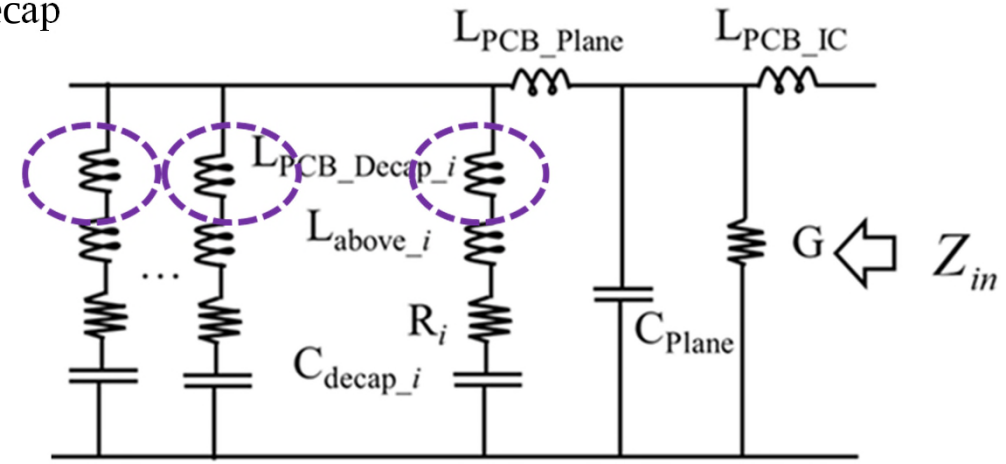


Q: If $L_{PCB\ IC}$ is negligible, in which cases can the doublet configuration be beneficial? Which cases less so.

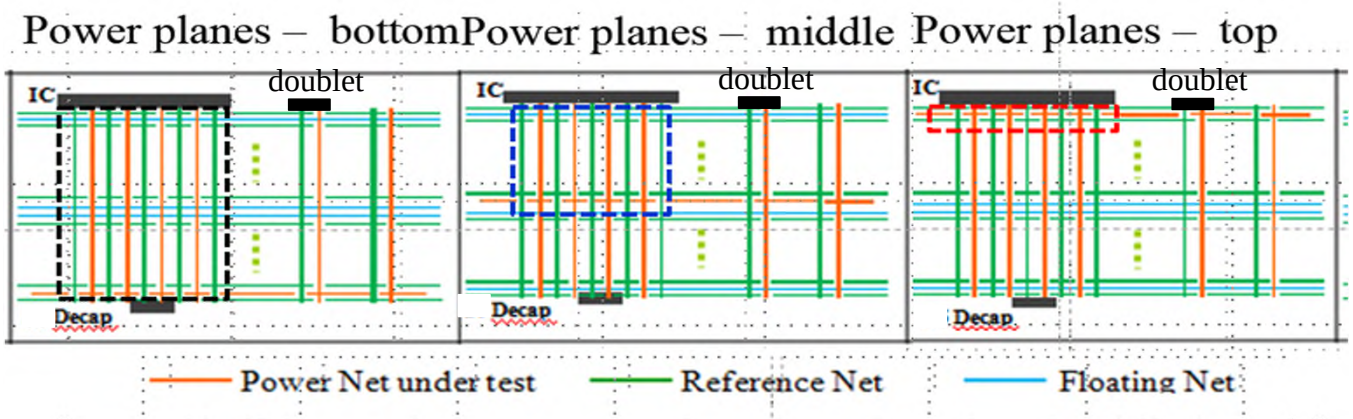
Example 2: The Doublet – Minimizing $L_{PCB\ Decap}$

Placing decaps on in pairs allows to use mutual inductance to minimize overall $L_{PCB\ Decap}$





- GND via
- PWR via



Q: If $L_{PCB\ IC}$ is negligible, and decaps can be placed under the IC, in which cases can the doublet configuration be beneficial? Which cases less so.

Q: Which of these cases is not well chosen for the decap location?

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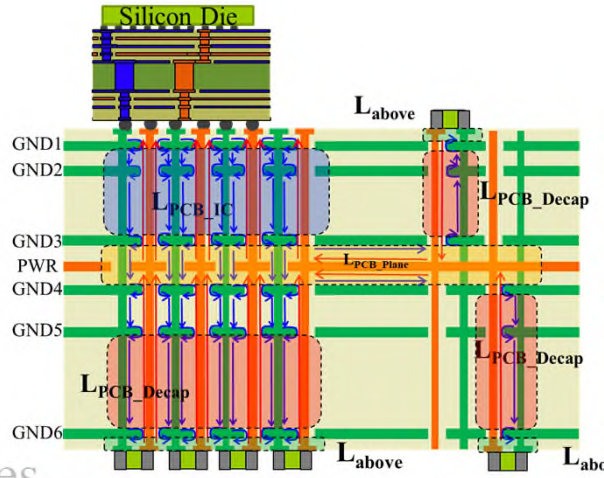
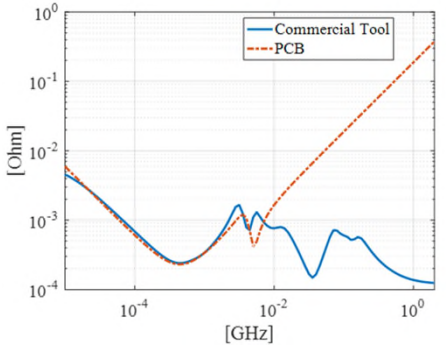
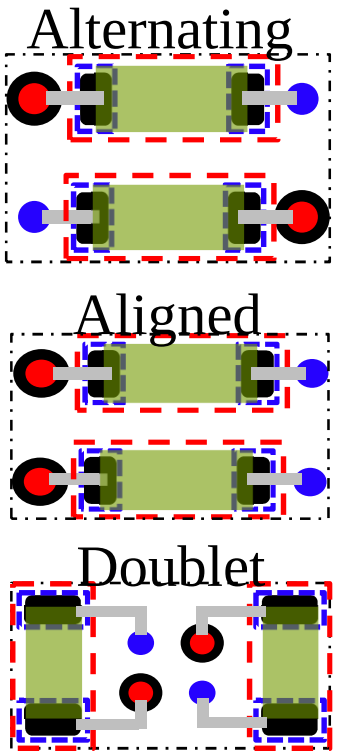
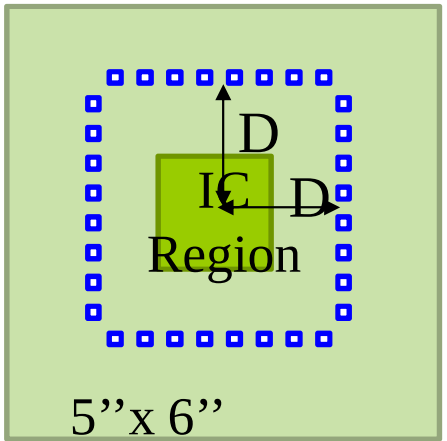
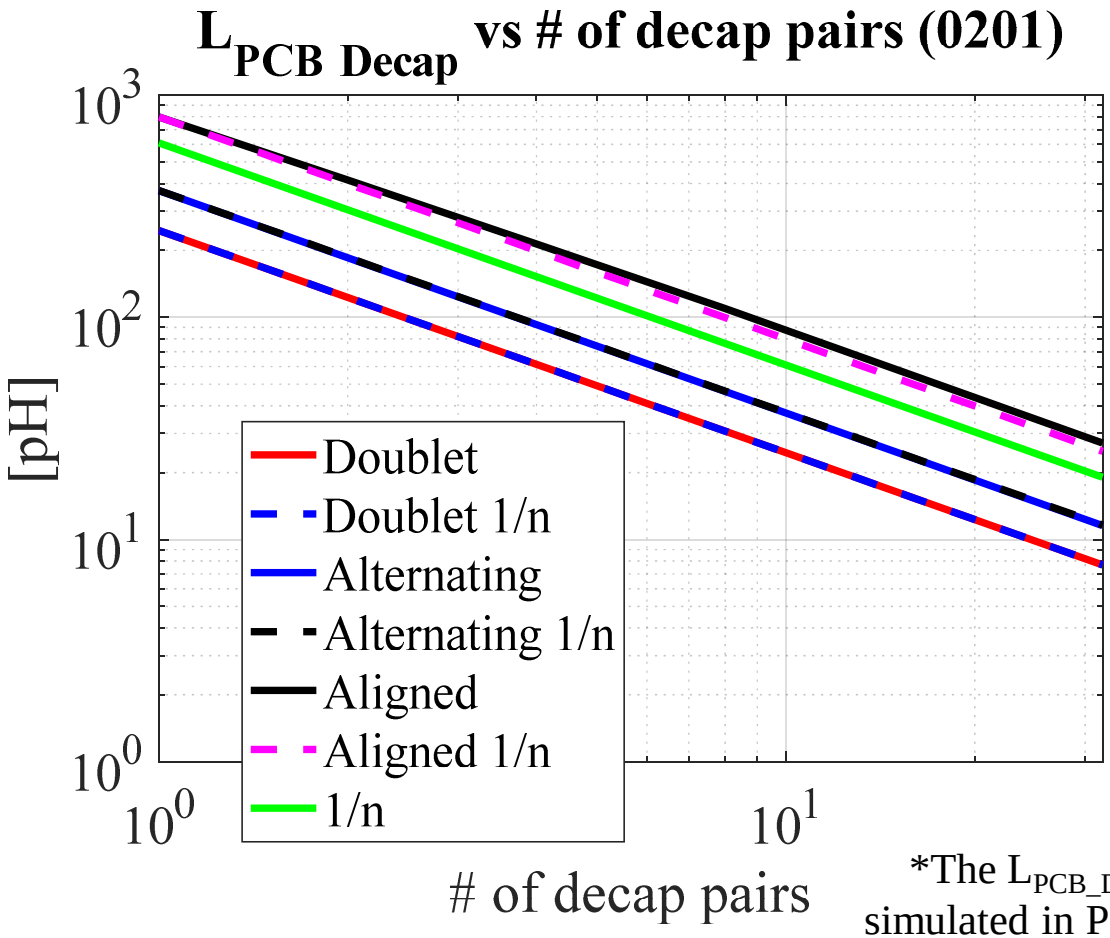




L_{PCB_Decap} Convergence



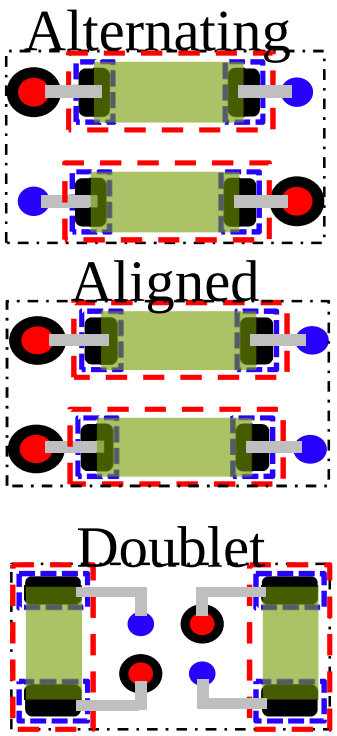


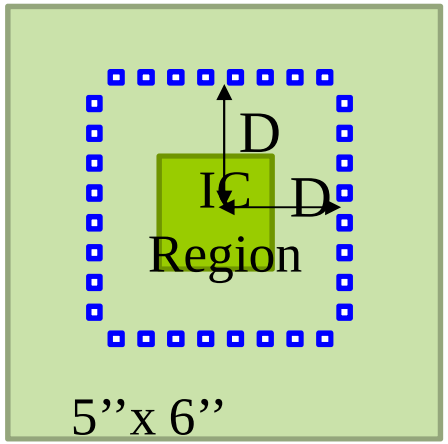


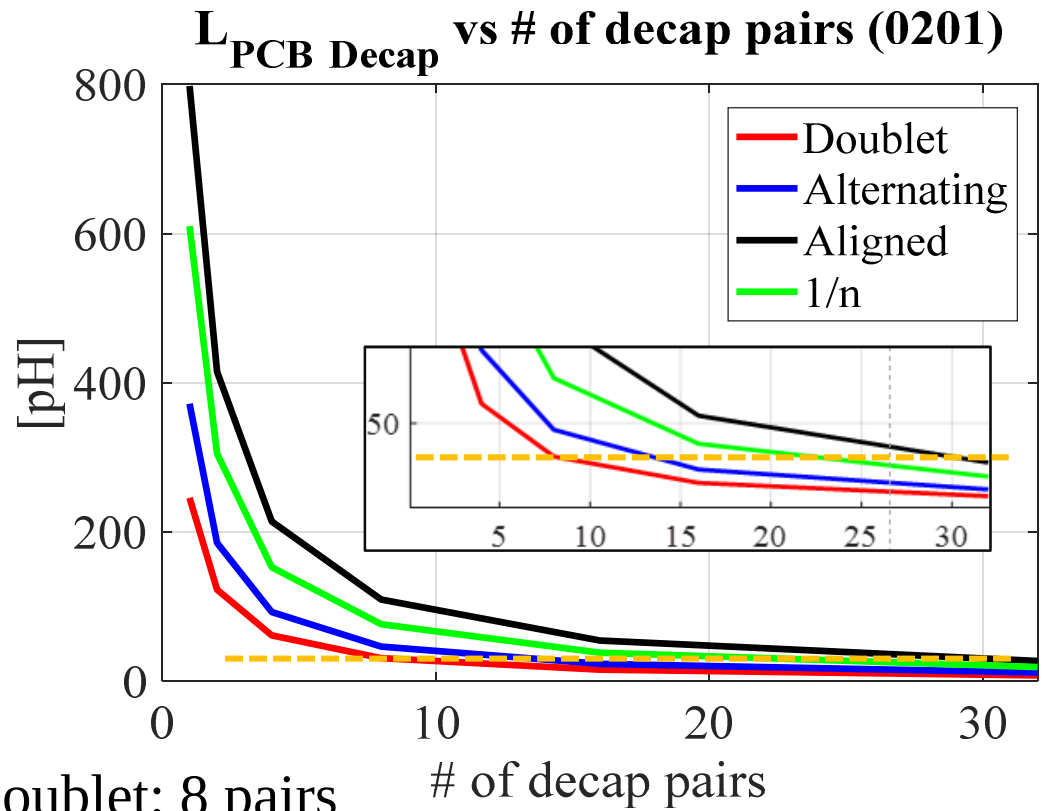
$$\frac{1}{n_{pair}}$$ convergence rate for all SMT package sizes

*The L_{PCB_Decap} is simulated in PDN Tool and the inductance is extracted from $|Z_{PDN}|$.

L_{PCB_Decap} Capacitor Configuration Example



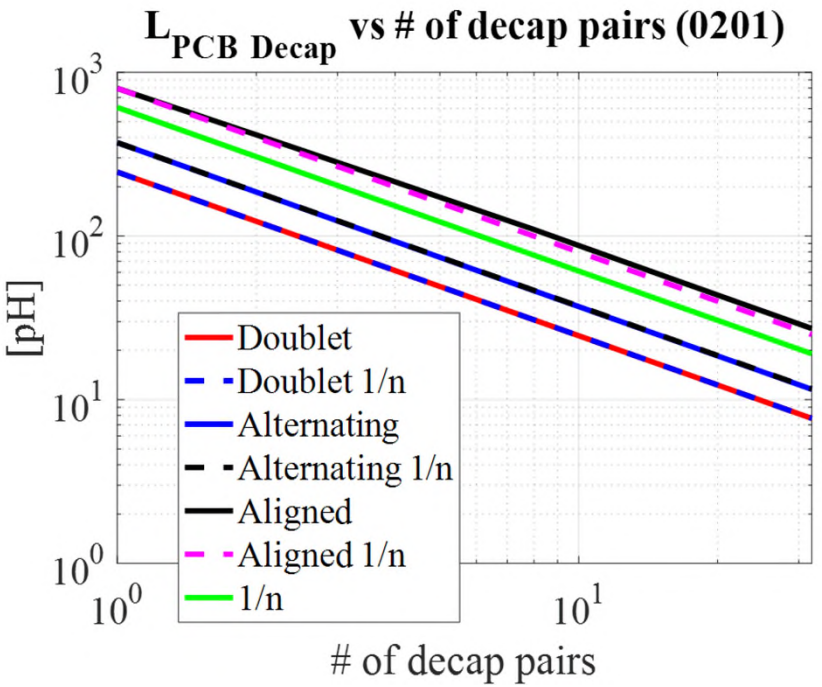


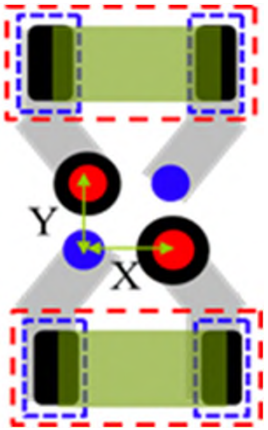


- Doublet: 8 pairs
- Alternating: 14 pairs
- 1/n: 25 pairs (no mutual coupling between individual decaps)
- Aligned: 30 pairs

Key Points

- Adding capacitors decreases $L_{PCB\ Decap}$ as 1/n
- Geometries such as the Doublet or 3-terminal capacitors reduce inductance over geometries where there is no benefit of mutual inductance.





Design Implications

- Use the impedance equivalent circuit model to try to identify what component is dominant and use it to guide meeting the target impedance.
- PWR/GND plane pair nearer to the IC in stackup will minimize L_{PCB_IC} from package balls to power net area fill (smaller loop)
- PWR/GND plane pairs closely spaced will reduce L_{PCB_plane}.
- Place caps close to the power layer to minimize the inductance from the capacitor to the power net area fill layer, i.e., L_{PCB_decaps}. (minimize the loop)
- Placing caps on the underside of PCB opposite package can benefit the design
  - The space is available and requires no additional vias
  - If the pkg/planes/decap path is shorter due to PWR/GND near package in stackup decaps around the IC will be more effective
- Power and ground vias placed adjacent to the caps reduces the inductance in the current return path (or in the bonding pads). (smaller loops)
- Capacitor arrangements that utilize mutual inductance, e.g., doublet, or 3-terminal capacitor, can significantly reduce L_{PCB_decaps}.

Thank you!

Power Integrity for High-Speed Design on Multi-Layer PCBs

Concepts and Physics

James L. Drewniak

Clear Signal Solutions and

Missouri S&T EMC Laboratory

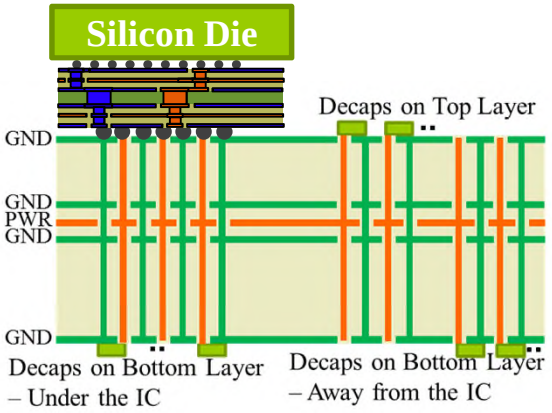
james.drewniak@clearsig.com

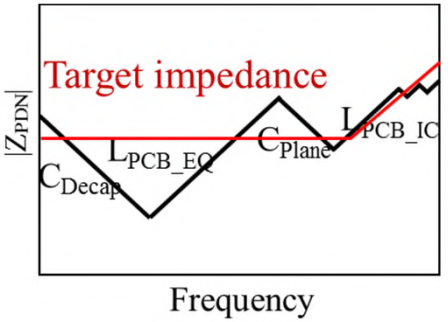
Contributors

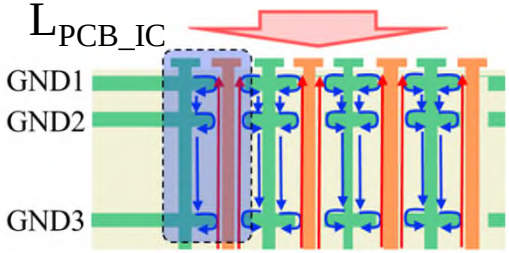
- IBM – B. Archambeault, S. Connor, M. Cocchini, W. Becker, M. Cracraft, A. Ruehli
- Cisco – B. Achkir, S. Scearce, Q. Gaumer, M. Sapazhnikov
- Missouri S&T – B. Zhao, S. Bai, S. Liang, X. Zhu, K. Shringapure, S. Pan, J. Xu, J. Fan

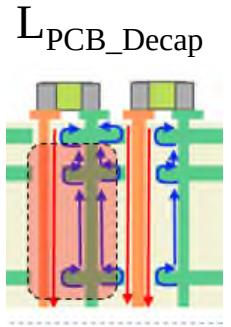
Overview – Pre-layout Methodology

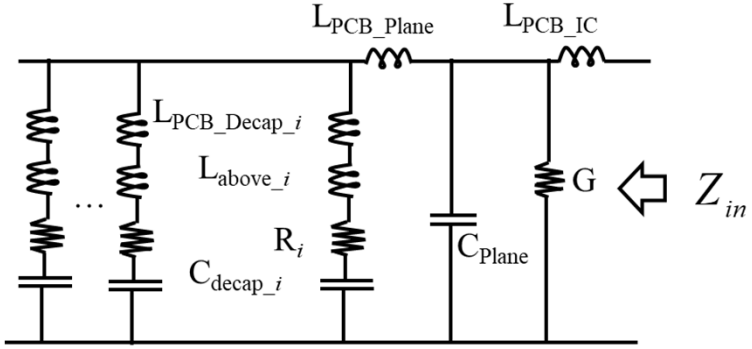
- Problem and concepts
- PDN pre-layout design methodology
- Circuit model
- Example

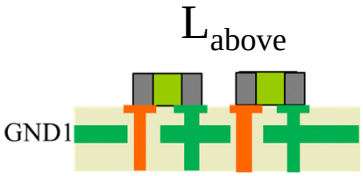




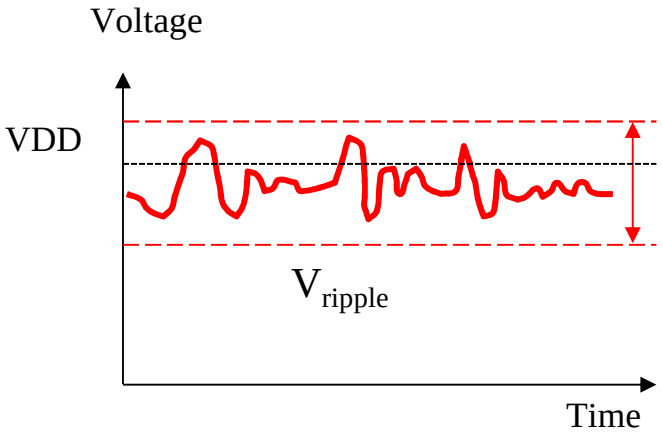


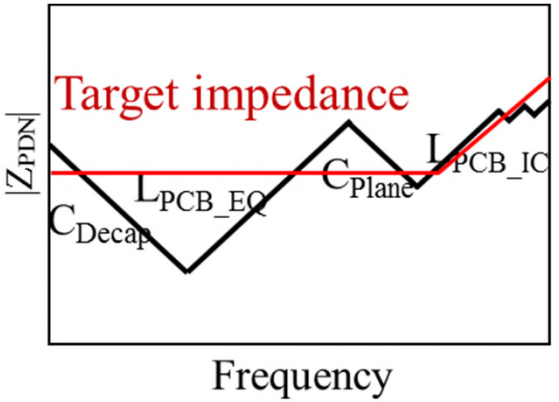


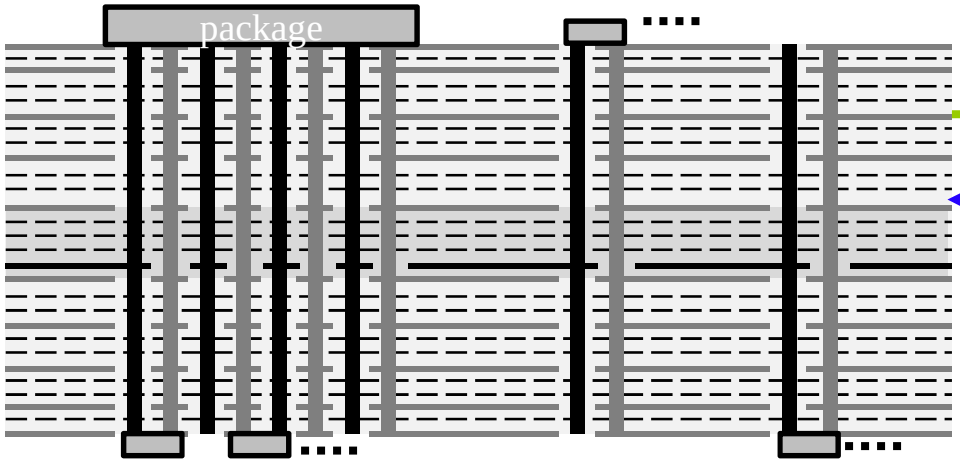




Problem Introduction

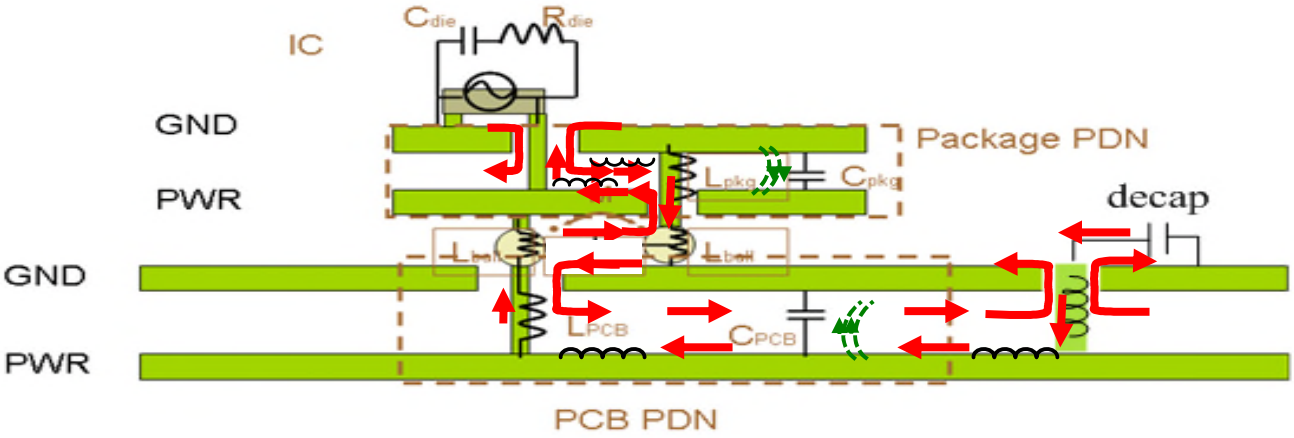


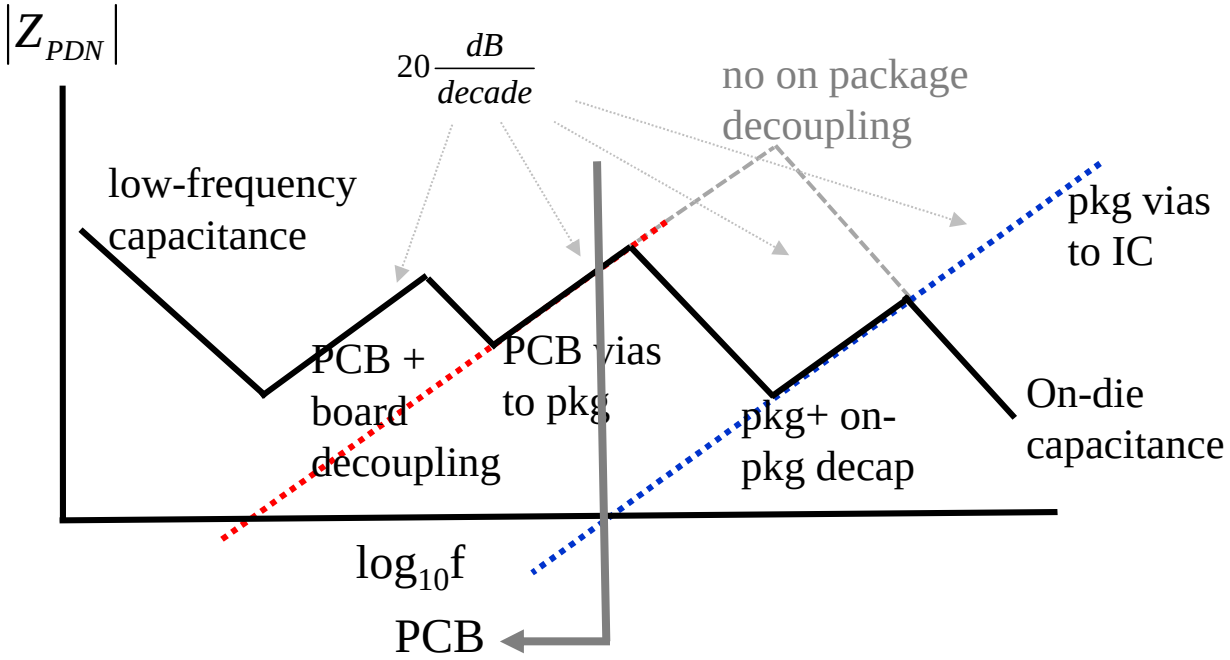




PowerSI
SIwave
PiPro

A Systematic Approach for Achieving PI



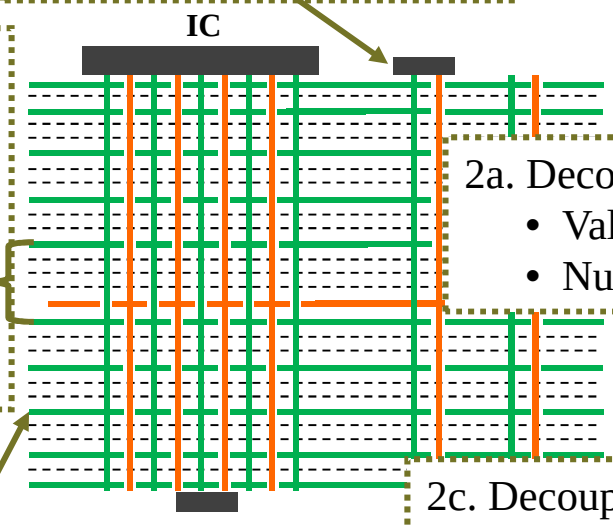


PDN Design Considerations

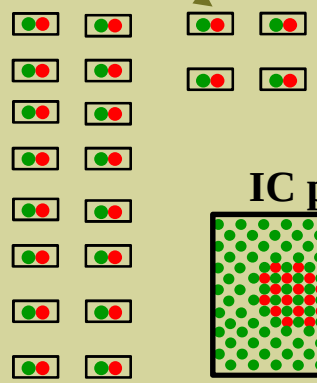
2a. Decoupling capacitors
- Top
- Bottom,
- Beneath IC?

2b. Decoupling capacitor connection -
- PWR/GND via geometry
- Package size

1. Power/ground net area fill
- Location in stack
- Spacing to power return plane
- Total area fill
- Special materials



2a. Decoupling capacitors
- Value(s)
- Number (total C)



Effect of other ground/reference planes?

PWR
GND

2c. Decoupling capacitor layout
- How close to IC?
- Shape – ring IC, on one side?

3. IC PWR/GND
- Number pins
- Pin pattern
- Pitch
- On-package decaps

The pre-layout methodology is for multi-layered PCB PDN geometry.

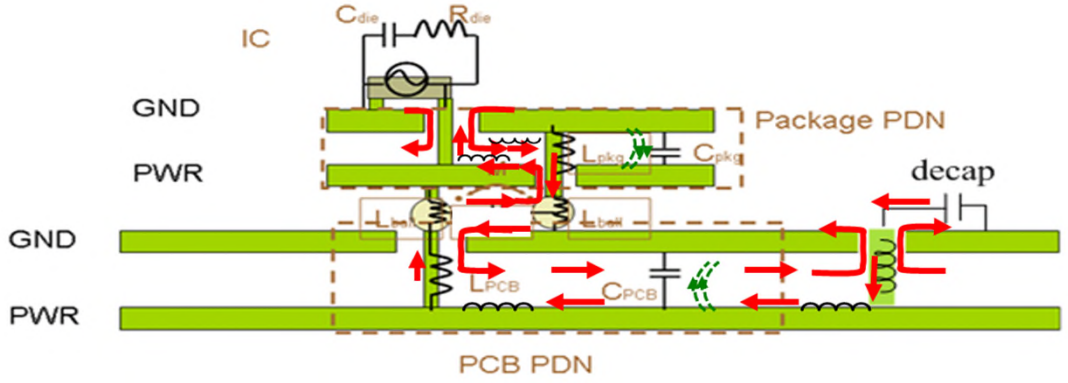
PI Design Flow – Package

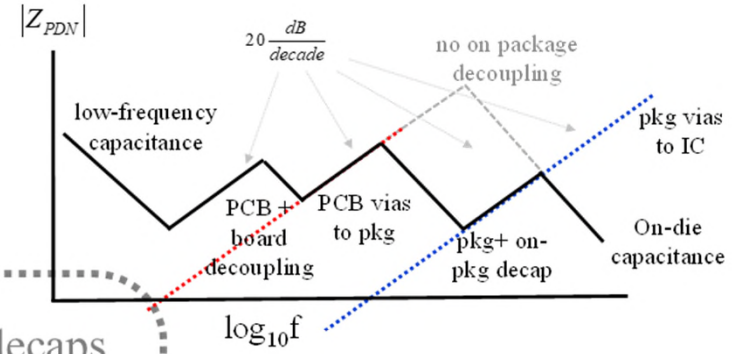
DC power determines minimum number power interconnects (IR drop, current)

Package ball **pitch** determines minimum achievable high-frequency Z_{target}

Choose **number (and pattern)** PWR/GND vias to meet high-frequency target impedance for specified PCB power area fill layer* → $L_{PCB\ IC}$

Trade-off



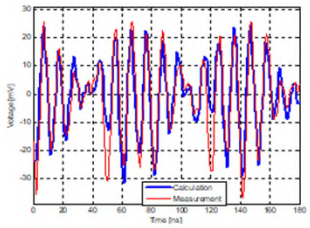


On-package decaps reduce minimum overall achievable high-frequency target impedance seen by IC

* PCB/package co-design step

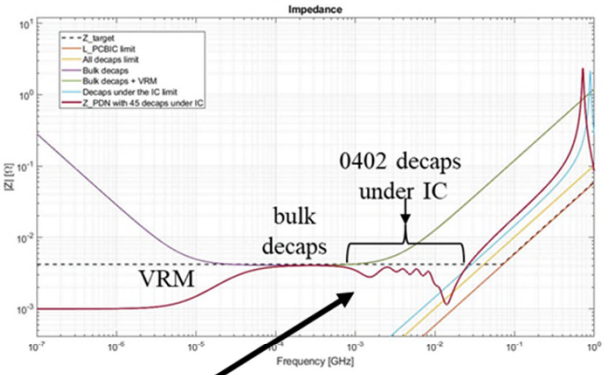
Design Flow – PCB

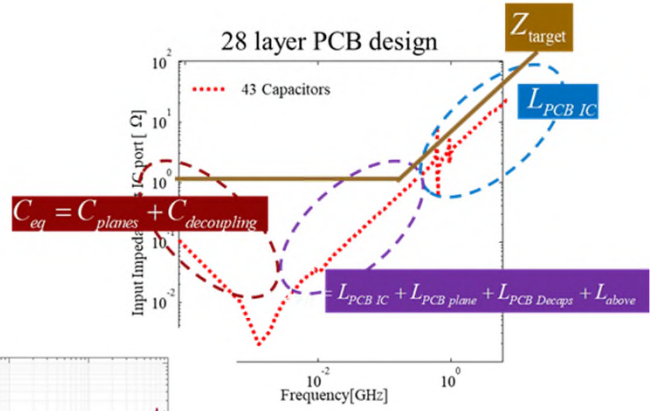
Peak **voltage ripple/droop** determines Z_{target}



IC/ASIC PWR/GND **pin-out number (and pattern)** determines minimal→ $L_{PCB\ IC}$

Choose PWR/GND area fill **layer** to meet high-frequency target impedance→ $L_{PCB\ IC}$

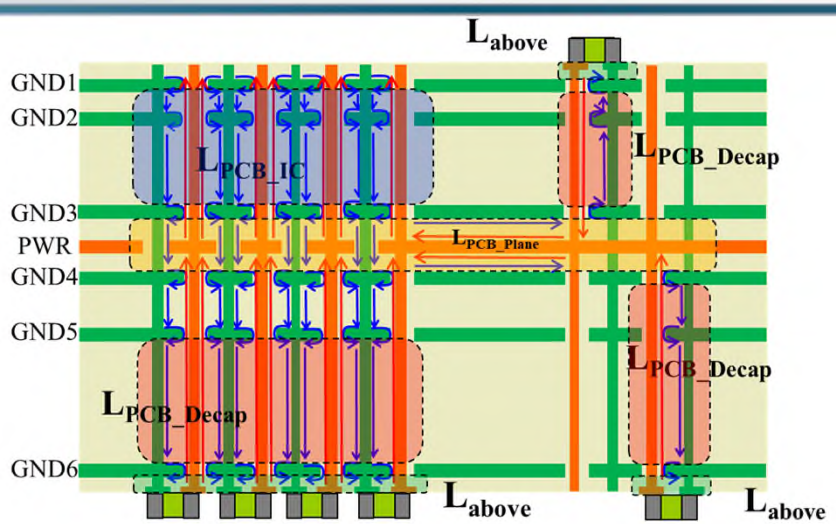




Number of decaps and placement determines → L_{EQ}

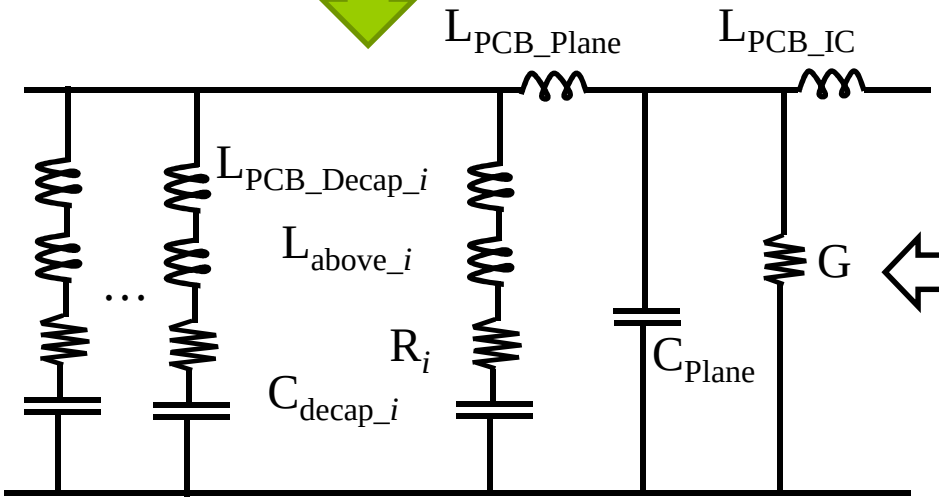
→ **value of decaps** to meet Z_{target}

Objective: PCB Impedance Equivalent Circuit

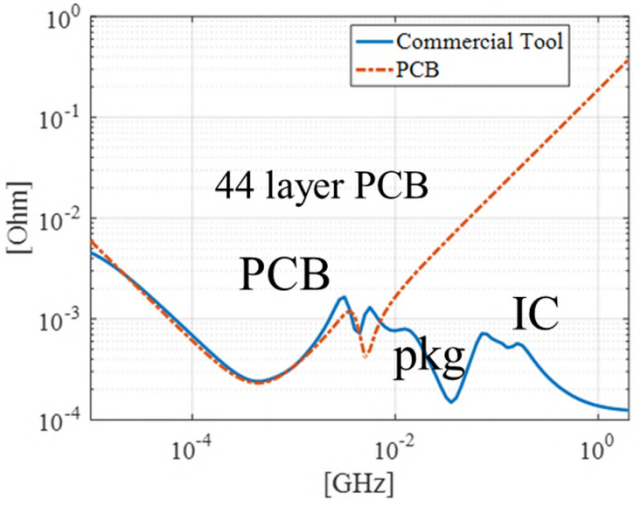


Objective: Determine the values for:

- L_{PCB_IC} calculation
- L_{PCB_plane} calculation
- L_{PCB_decap} calculation
- L_{above} calculation
- Calculate Z_{PND} and voltage ripple



Z_{in}

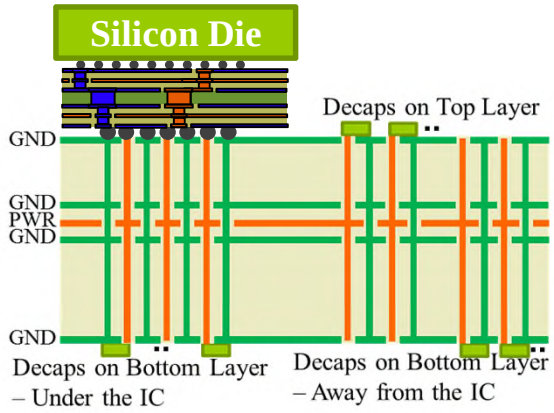


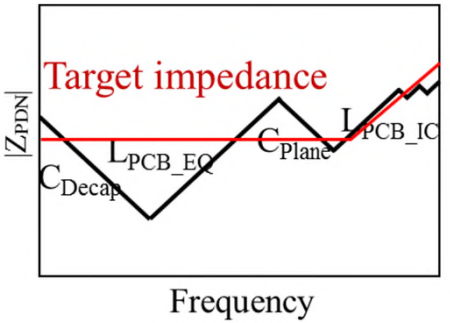
Can add package, IC, and VRM models to this

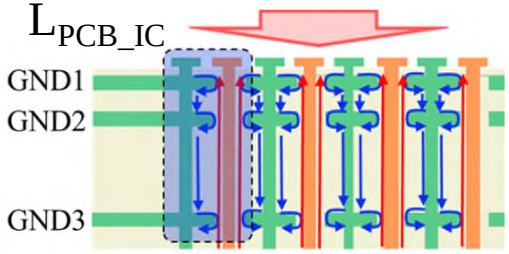
Overview – Pre-layout Methodology

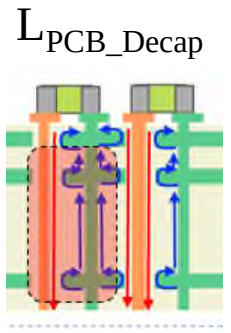
- Problem and concepts

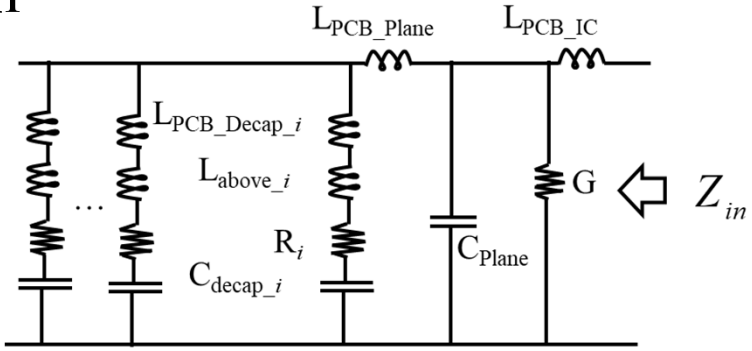
- PDN pre-layout design methodology
  - **Example geometry**
  - L_{PCB_IC} calculation
  - L_{PCB_decap} calculation
  - L_{PCB_plane} calculation
  - L_{above} calculation

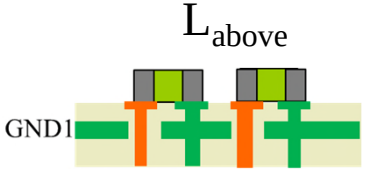




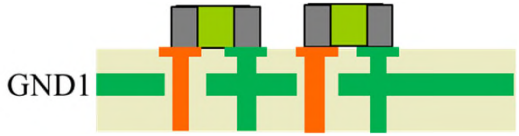


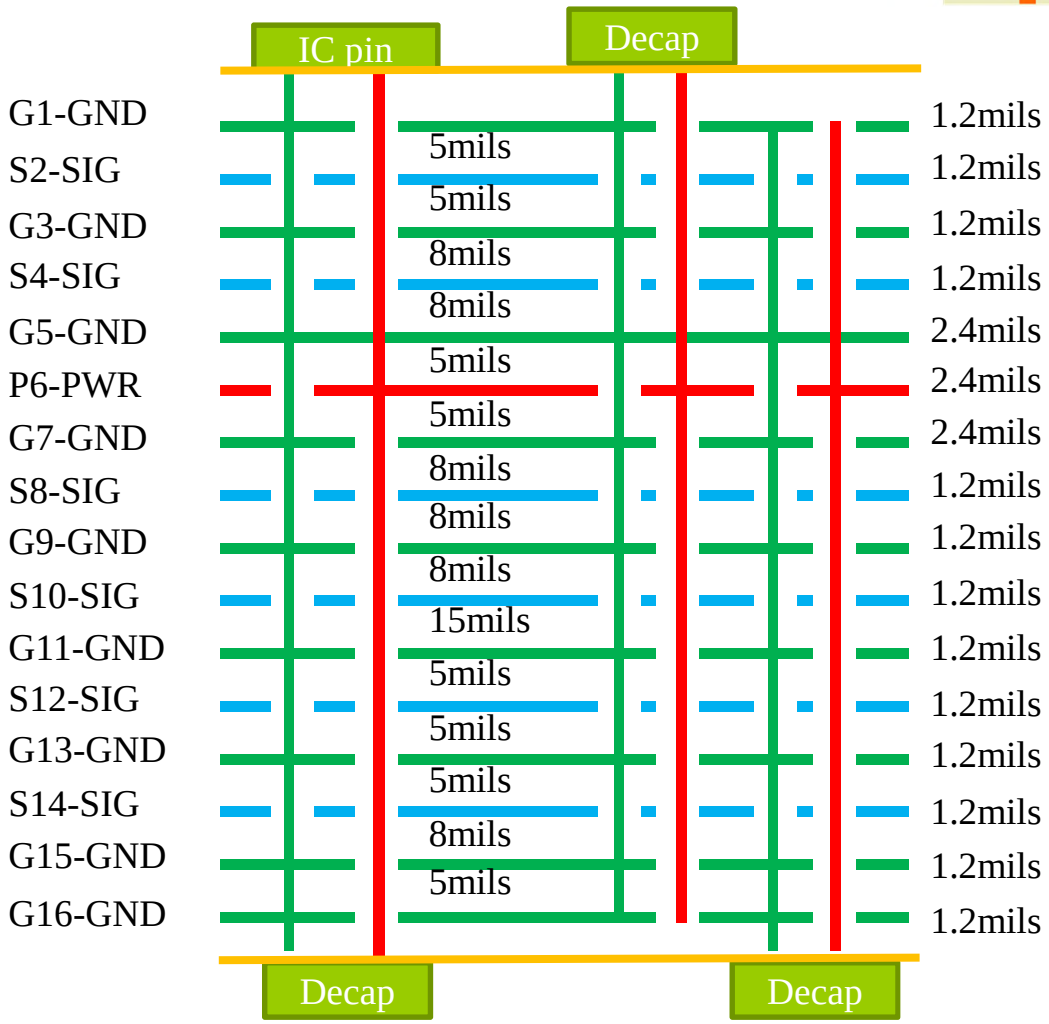


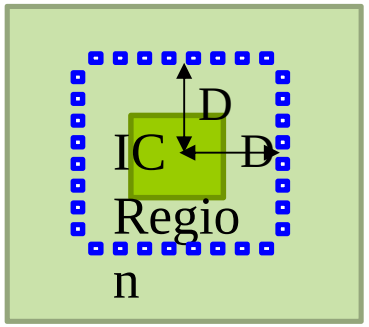




PCB PDN Example - Geometry

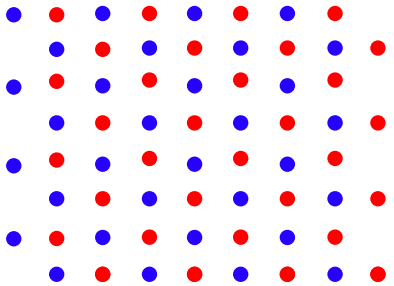




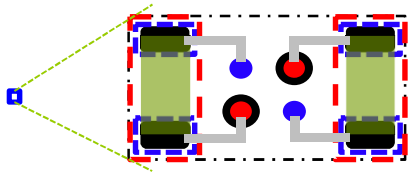


5”x 6”

Alternating

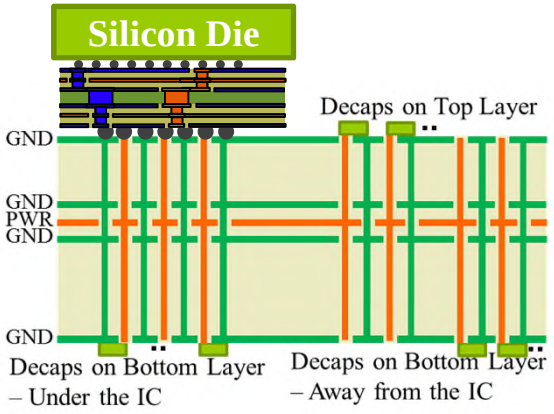


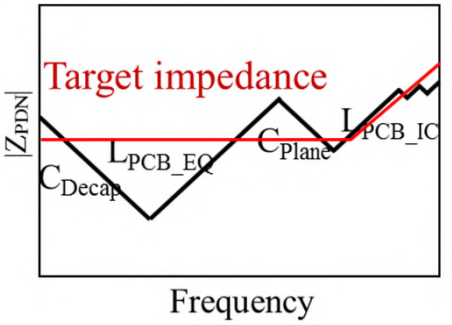
Doublet

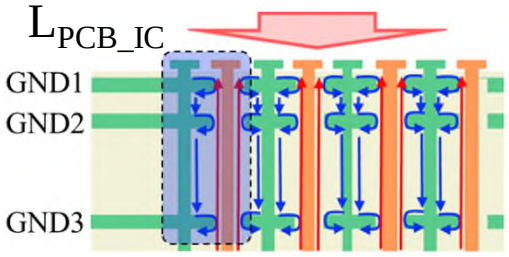


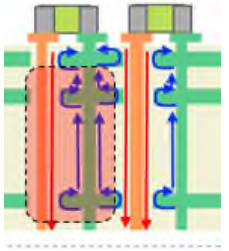
Overview – Pre-layout Methodology

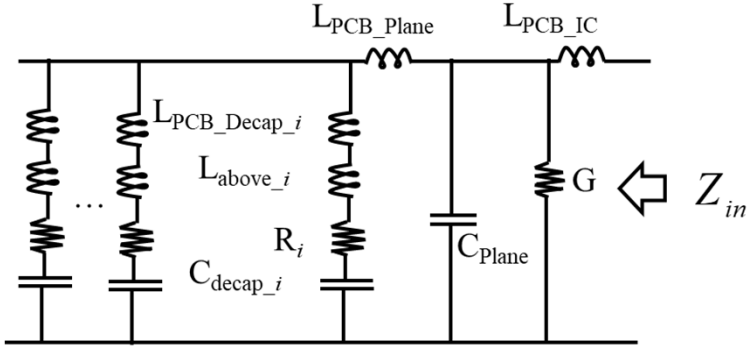
- Problem and concepts
- PDN pre-layout design methodology
  - Example geometry
  - **L_{PCB_IC} calculation**
  - L_{PCB_decap} calculation
  - L_{PCB_plane} calculation
  - L_{above} calculation

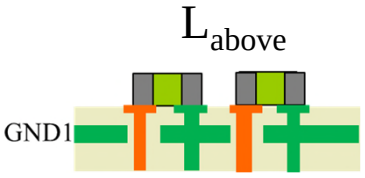




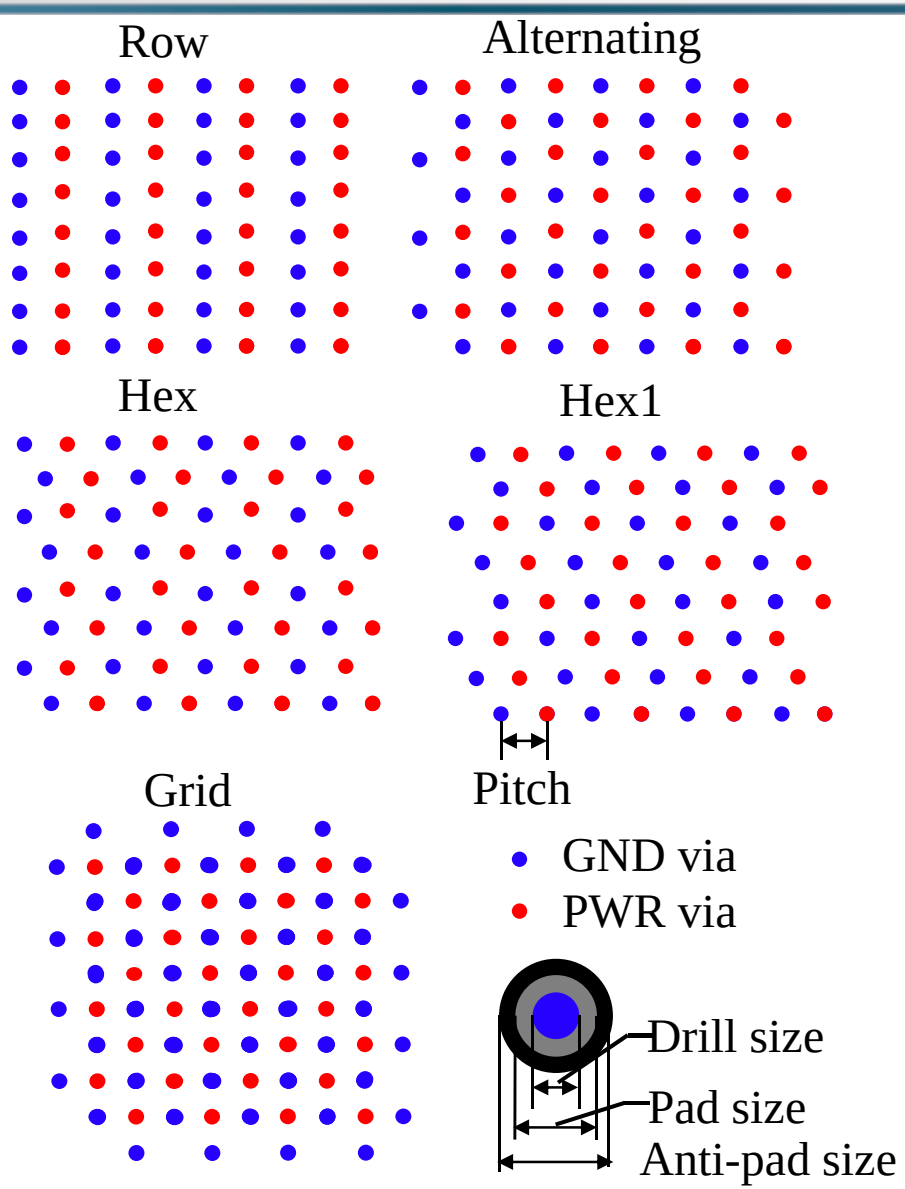


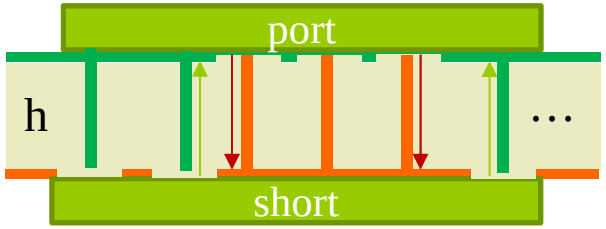






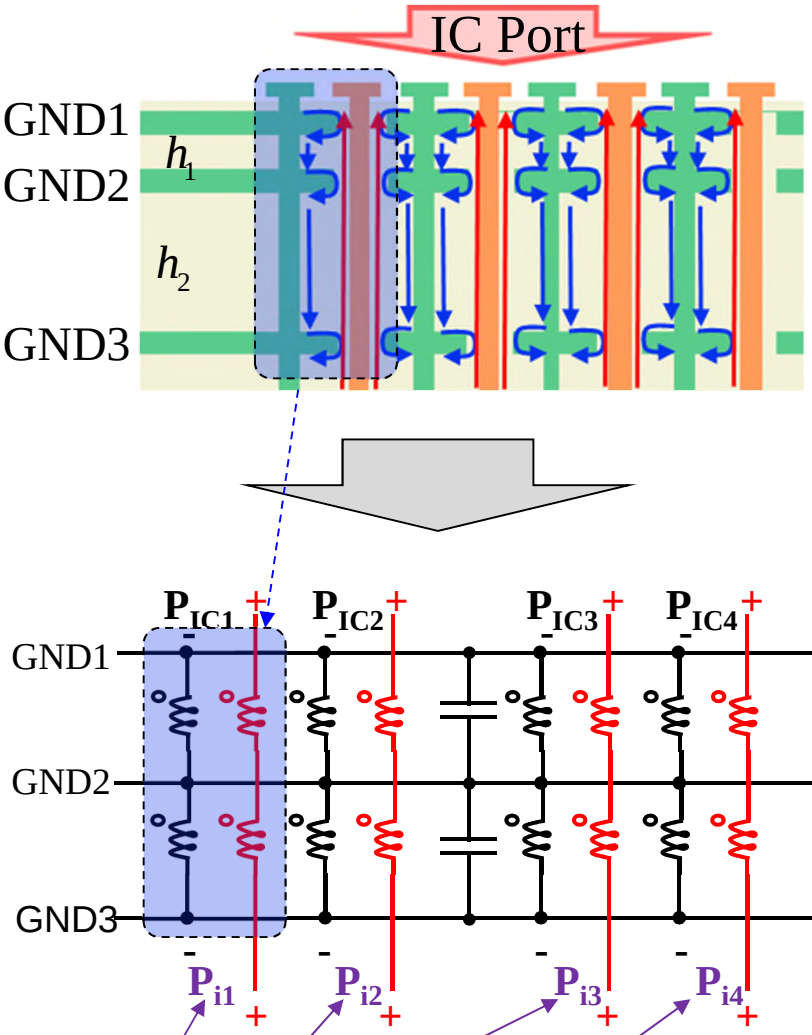
L_{PCB_IC} Geometry



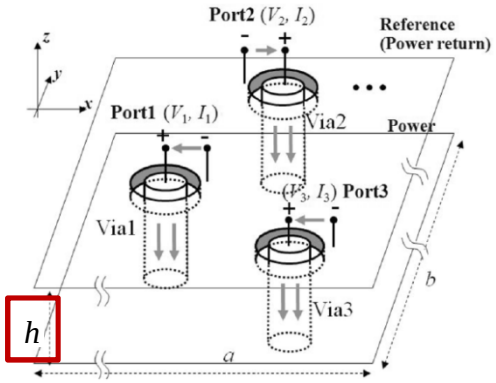


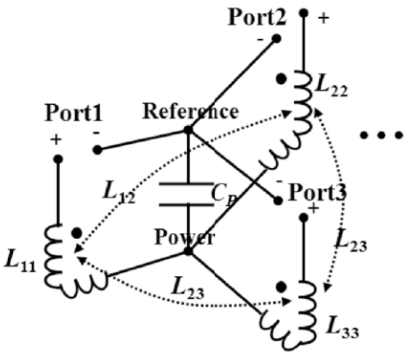
Pitch	Drill size	Anti-pad size
1 mm	8mils	20mils
	12mils	32mils
	15mils	39mils
0.8 mm	8mils	20mils
	12mils	20mils

L_{PCB_IC} Inductance Physics – goes as *h*



Cavity Model





$$L_{ij} = \frac{\mu h}{ab}\sum_{m=0}\sum_{n=0}\frac{\varepsilon_m^2\varepsilon_n^2}{k_{mn}^2} f(x_i, y_i, x_j, y_j)\Big|_{(m,n)\neq(0,0)}$$

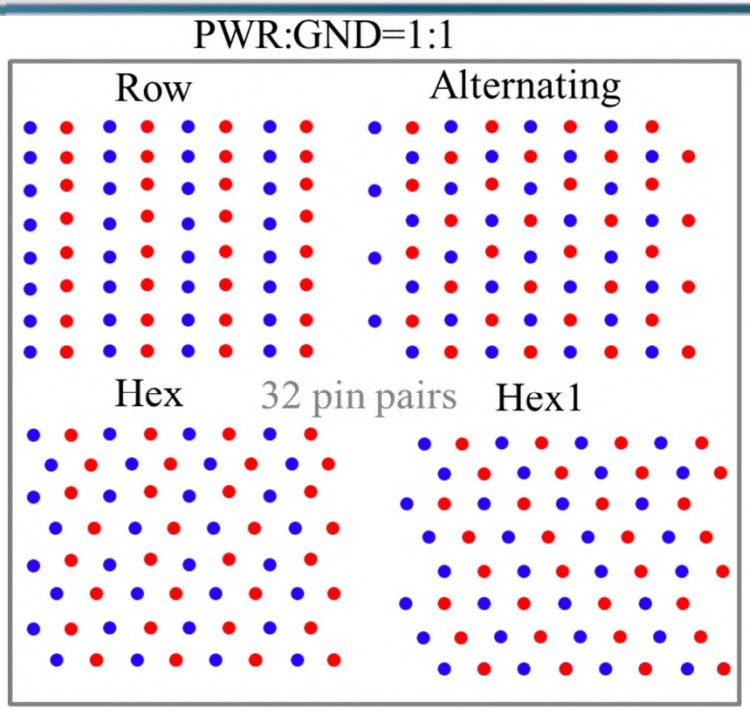
$$h = h_1 + h_2$$

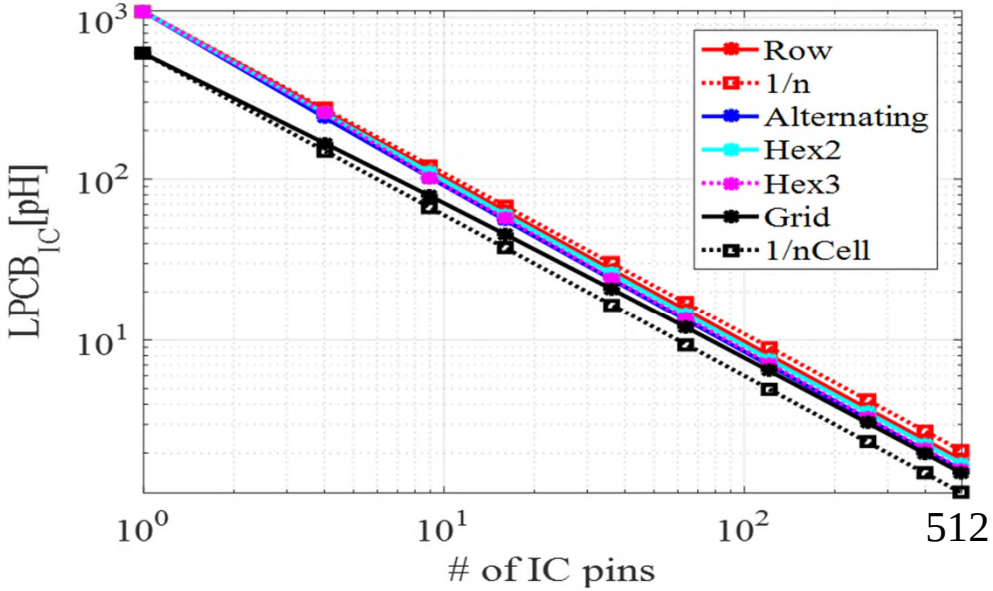
$$L_{PCB\_IC\_grid} = h\left(\frac{L_{self\_PUL,1unitcell}}{n_{ICpin}} + L_{Mutual,unitcell\_PUL}\right)$$

$$L_{self\_PUL,1unitcell} = L_{self,PWR} + \frac{L_{self,GND}}{4} - 2M_{PG} + \frac{M_{GG1}}{2} + \frac{M_{GG2}}{4}$$

Calculate a per-unit-layer inductance

L_{PCB_IC} Convergence for 1mm Pitch





$L_{PCB\ IC}$ [pH] WHEN THE DRILL DIAMETER IS 8 MILS AND THE THICKNESS FROM THE IC TO THE POWER CAVITY IS 40 MILS

IC power pin #	Cavity Model	CST
72 (6 rows by 12 cols)	12.3	12.5
200 (10 rows by 20 cols)	4.2	4.1

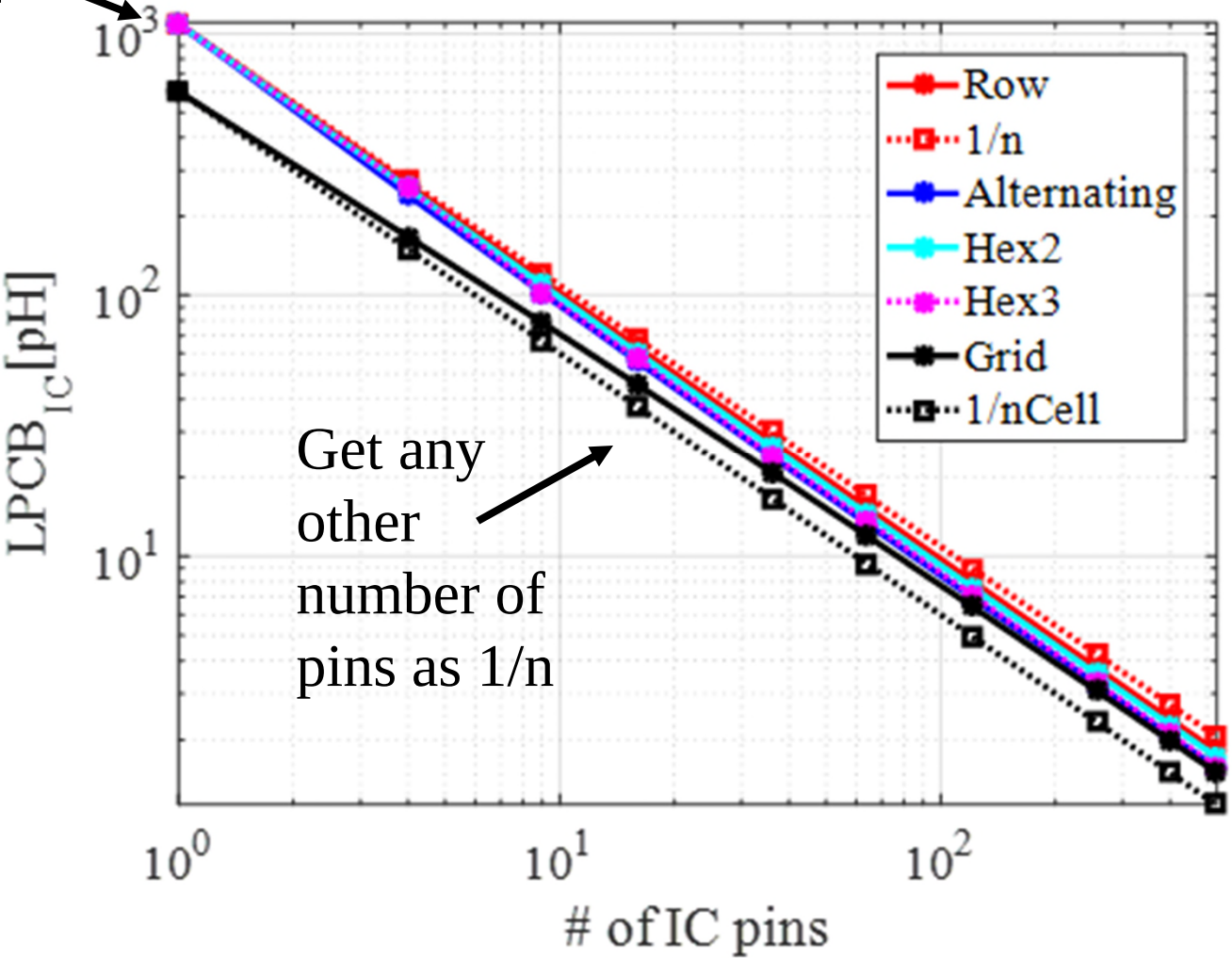
Additional pin pairs or unit cells converges as

$$\frac{1}{n} \text{ or } \frac{1}{n_{unit\ cell}}$$

*The L_{PCB_IC} is simulated in PDN Tool and the inductance is extracted from $|Z_{PDN}|$.

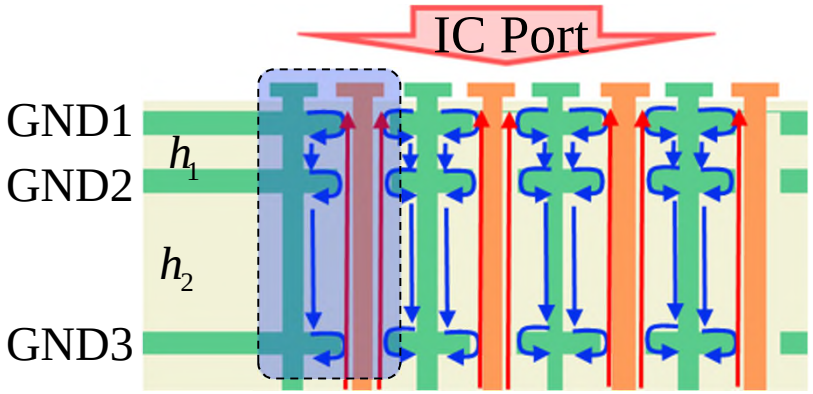
L_{PCB_IC} Caclulation

Calculate inductance of 1 cell



L_{PCB_IC} Design Calculations

Layers are “in series”



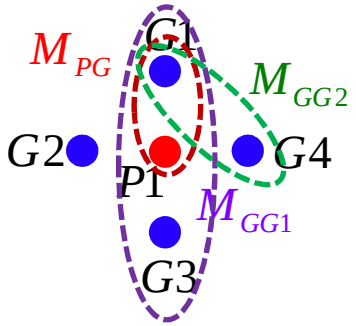
$$h = h_1 + h_2$$

$$L_{PCB\_IC} = h \times \frac{L_{self\_PUL,1pin}}{n_{ICpin}}$$

All mutual inductances are accounted for

L_{PCB_IC} per mil for one IC pin [pH]

Pitch	Drill size	1/n	$1/n_{UnitCell}$
1 mm	8mils	24.5	13.5
	12mils	20.4	11.0
	15 mils	18	9.5
0.8 mm	8mils	22.0	12.0
	12mils	17.9	9.5



L_{PCB_IC} Design Calculations per-unit-layer

TABLE II
IC PIN DESIGNS WITH DIFFERENT PITCH SIZES AND VIA-PADSTACK SIZES

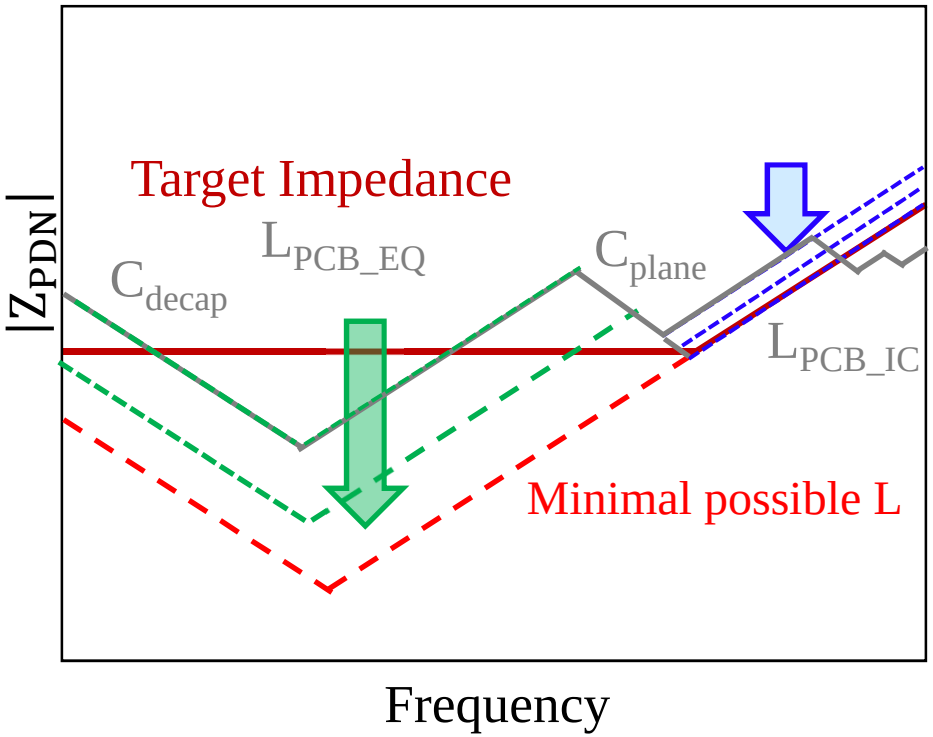
Pitch Size	Drill (Diameters)	Anti-pad (Diameters)
1 mm	8 mils	20 mils
	10 mils	30 mils
	12 mils	32 mils
0.8 mm	8 mils	20 mils
	12 mils	20 mils
0.5mm	8mils	20mils

TABLE III.
$L_{PCB\ IC}$ [PH/MIL] FOR THE UNIT CELL.

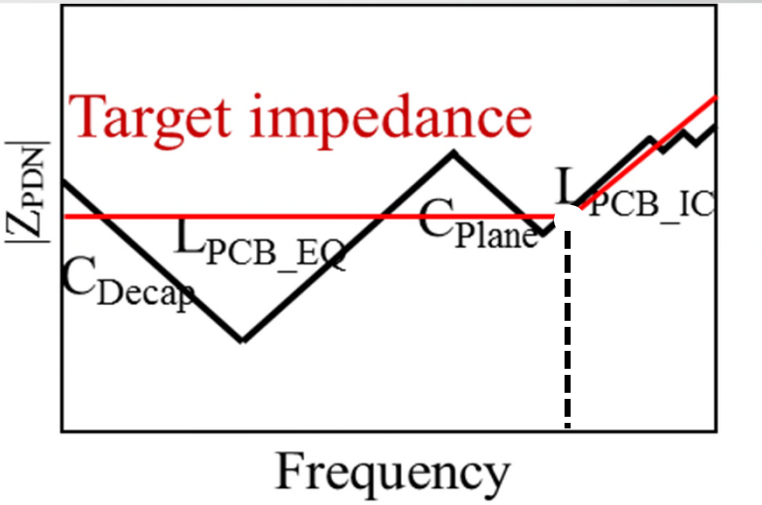
Pitch [mm]	Drill [mils]	PG pair. formula	CST	Grid unit cell formula	CST
1	8	24.5	24.0	13.5	12.9
	10	22.2	21.8	12.1	11.5
	12	20.4	20.0	11.0	10.2
0.8	8	22.0	21.8	12.0	11.3
	12	17.9	17.3	9.5	8.6

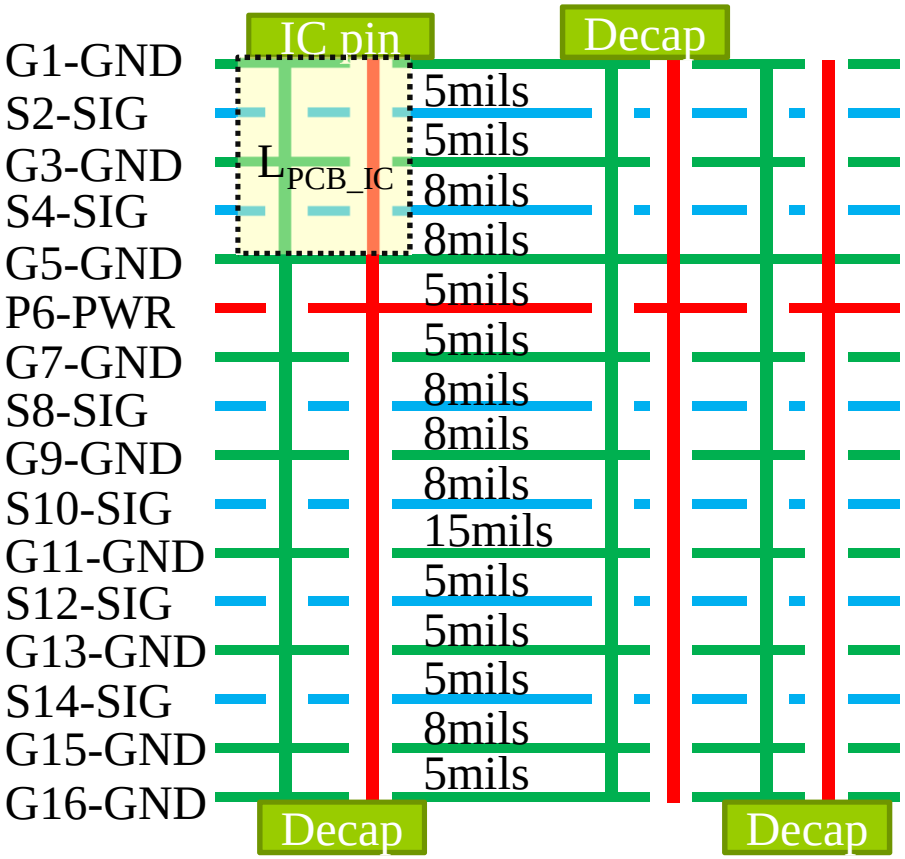
L_{PCB_IC} Design Flow

- Use the IC pin placement with the lowest n=1 inductance
- Adjust the stack-up to reduce the height from the IC port to the power net area fill
- Approximate the range of the L_{PCB_IC} using the 1/n and $1/n_{UnitCell}$ value to meet the high-frequency target impedance
- Calculate the # of IC pins needed according to the 1/n and $1/n_{UnitCell}$ curve for the geometry

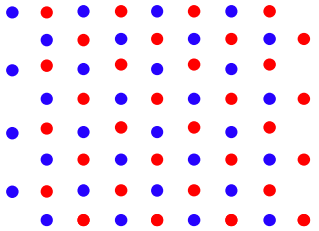


L_{PCB_IC} Example





Alternating



Drill size = 15mils,
Anti-pad size = 39mils,
Pitch = 1mm.

Requirement:

$$|Z_{PDN}| < 50m\Omega, \ when \ f = 100MHz$$

$$\Rightarrow 2\pi fL < 50m\Omega \quad L_{requrement} < 79.6pH$$

$$L_{PCB\_IC\_needed} = h \times \frac{L_{self\_PUL,1pin}}{n_{ICpin}}$$

$$L_{self\_PUL,1pin} = 18pH / mils$$

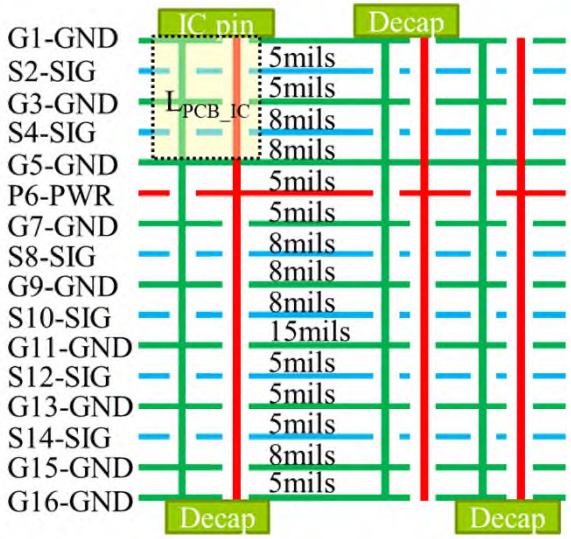
$$h = 26mils$$

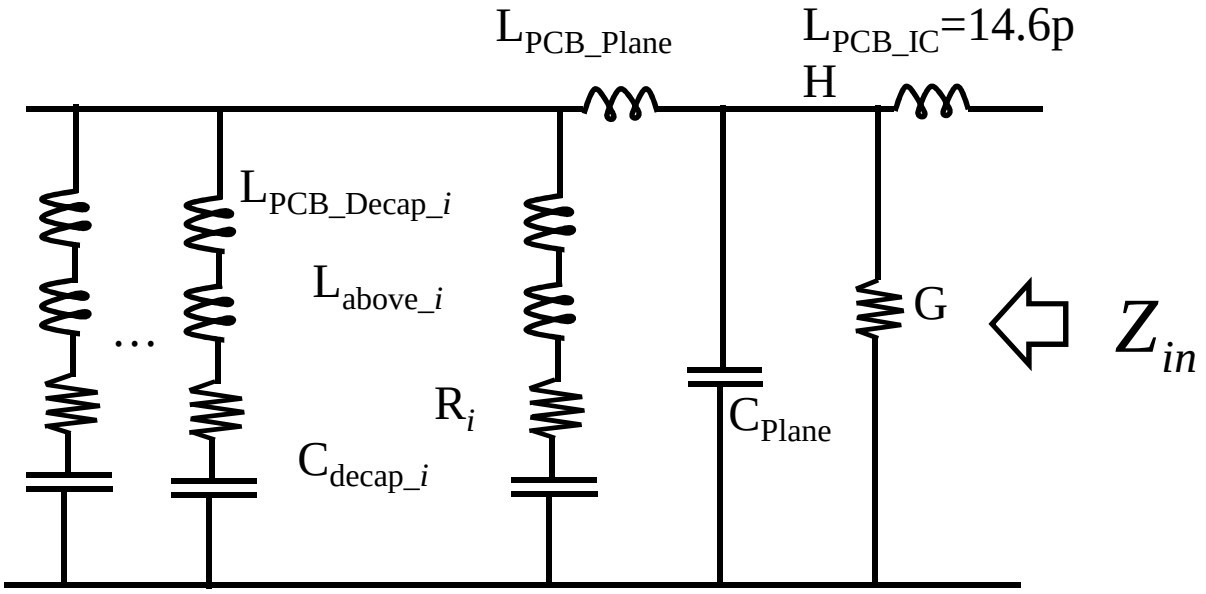
$$L_{PCB\_IC\_needed} = \frac{468pH}{n_{ICpin}} < 79.6pH \Rightarrow n_{ICpin} \geq 6$$

The IC pin # is 32, given by package designer.

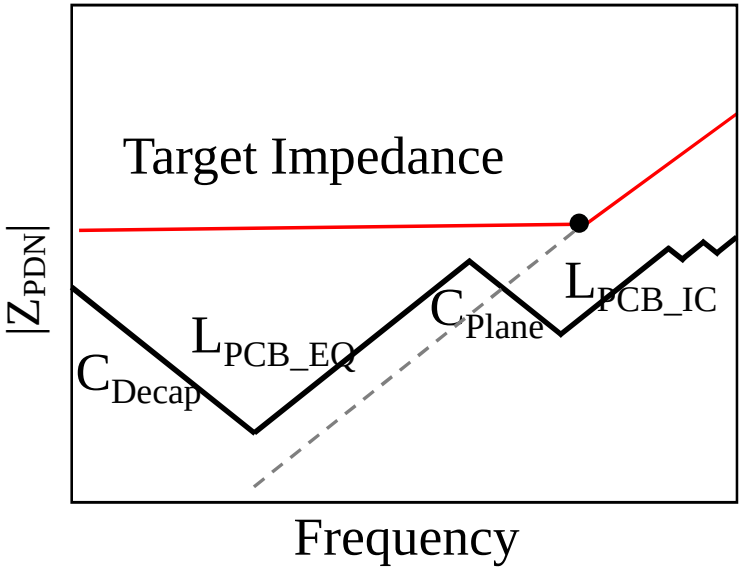
$$L_{PCB\_IC} = h \times \frac{L_{self\_PUL,1pin}}{n_{ICpin}} = \frac{468pH}{32} = 14.6pH$$

Impedance Equivalent Circuit





L_{PCB_EQ} Components Approximation



L_{high_needed}=79.6 pH ➡ $L_{PCB\_EQ\_min}$=79.6pH

L_{PCB_IC}=14.6 pH

$$L_{PCB\_EQ} = L_{PCB\_IC} + L_{PCB\_Decap} + L_{PCB\_Plane} + L_{above} \le 79.6\,pH$$

Assume: L_{PCB_Decap} is the similar to L_{above}, L_{PCB_Plane}

L_{PCB_Decap} = 22pH,

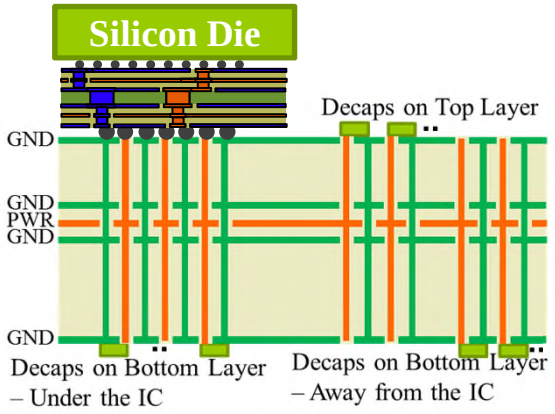
L_{PCB_above} = 22pH,

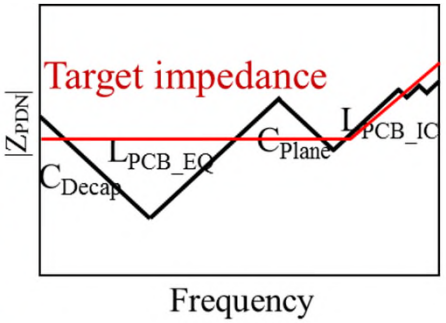
L_{PCB_Plane} = 22pH.

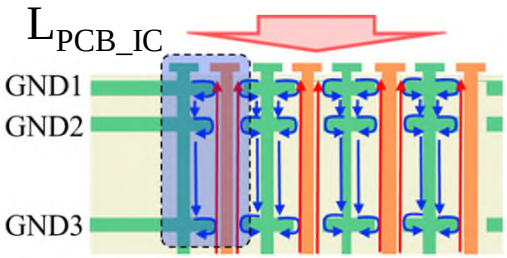
Overview – Pre-layout Methodology

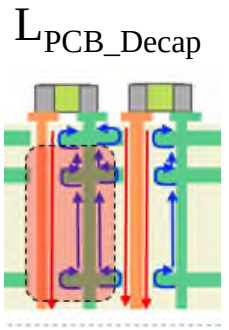
- Problem and concepts

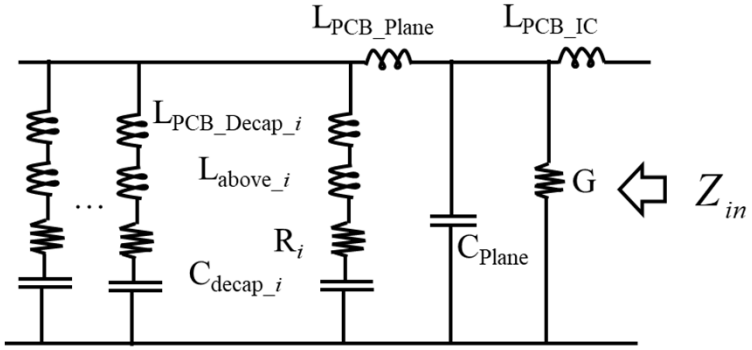
- PDN pre-layout design methodology
  - Example geometry
  - L_{PCB_IC} calculation
  - **L_{PCB_decap} calculation**
  - L_{PCB_plane} calculation
  - L_{above} calculation

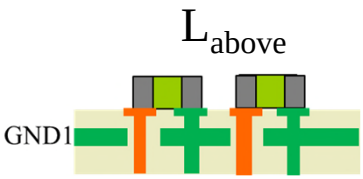






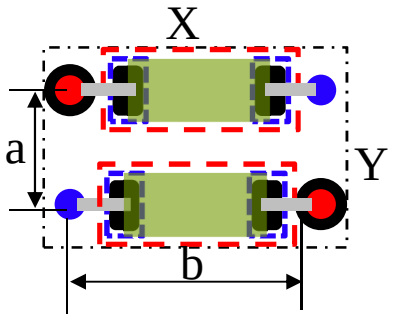




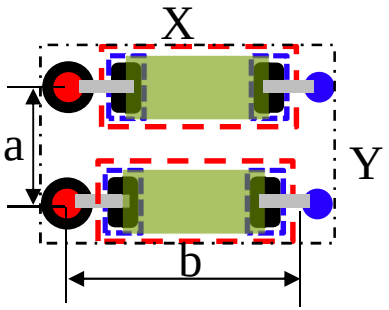


L_{PCB_Decap} Geometry

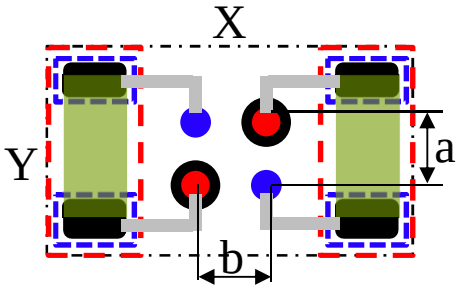
Alternating



Aligned

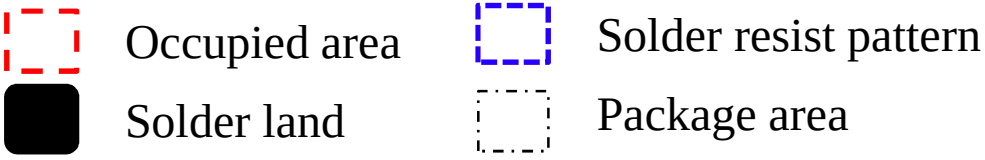


Doublet

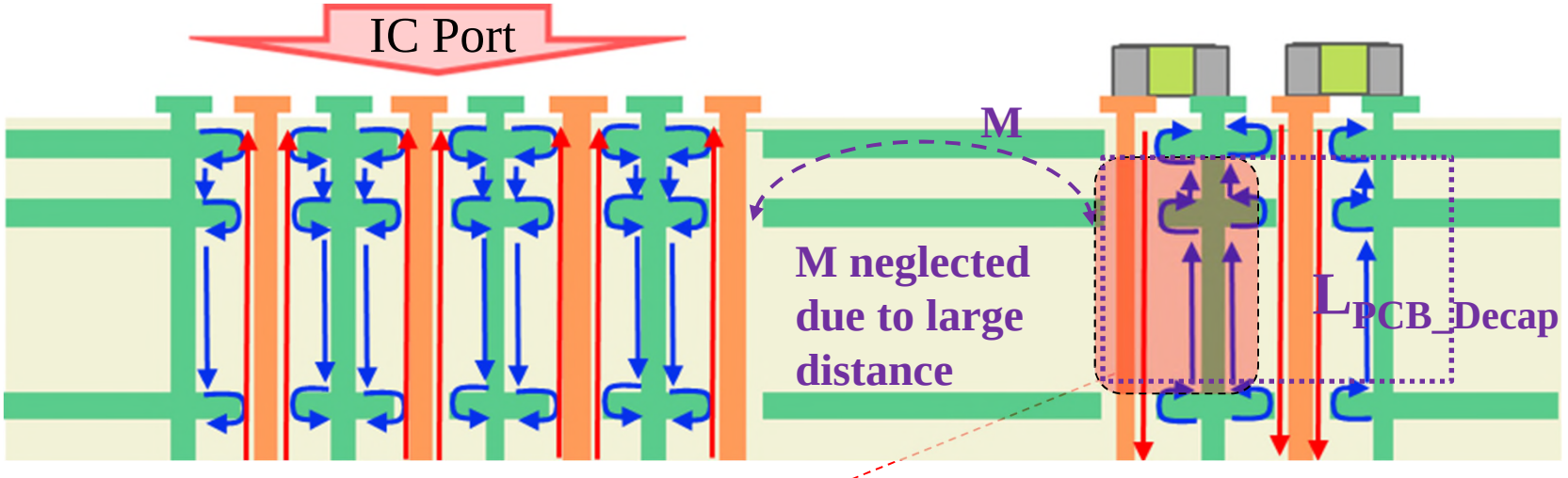


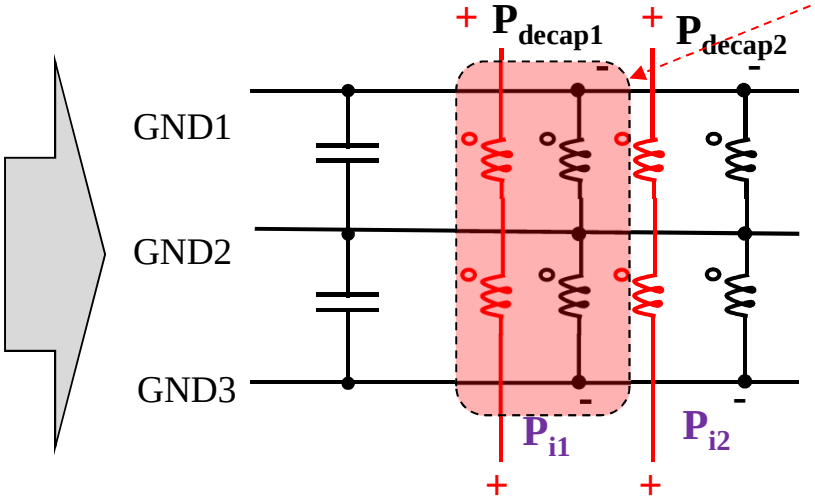
Relative via locations and package size ([mils]) of the three decoupling capacitor placement patterns

Placement pattern	Size	a	b	X	Y
Alternating/ Aligned	0201	45	120	159	85
	0402	53	136	175	101
	0603	88	207	246	171
	0805	108	223	262	211
Doublet	0201	32	32	149	71
	0402			165	87
	0603			235	158
	0805			275	174



L_{PCB_Decap} Inductance Physics

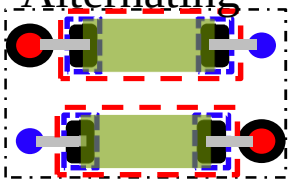




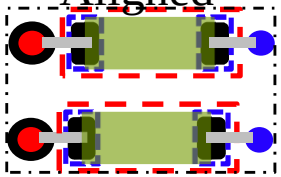
- Coupling between IC via and decap via neglected
- IC vias and decoupling capacitor vias can be modeled separately

L_{PCB_Decap} Inductance Physics

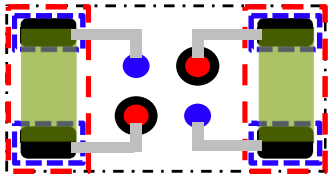
Alternating



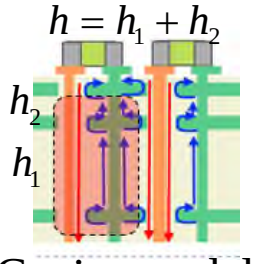
Aligned



Doublet



$$L_{PCB\_Decap} = \frac{L_{PCB\_Decap\_PUL}\big|_{n_{(decap\ pair)}=1}}{n_{(decap\ pair)}} \times h$$



Cavity model

$$L_{PCB\_Decap\_PUL}\big|_{n_{(decap\ pair)}=1} =$$

$$\frac{1}{2}(L_P + L_G \ominus 2M_{PiGi} \oplus M_{P1P2} \oplus M_{G1G2} \ominus M_{P1G2} \ominus M_{P2G1}),$$

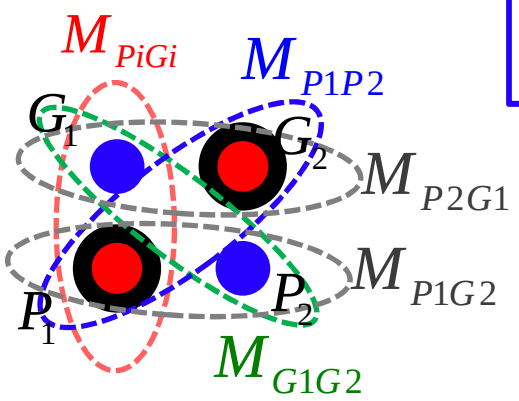
$$i = 1 \text{ or } 2$$

The sign shows the contributions of the mutual inductances

Mutual inductance between the PWR and GND vias for one decap

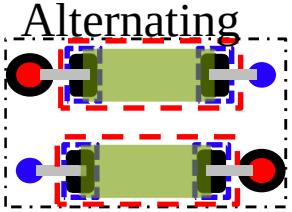
Mutual inductance between the PWR and PWR, or between GND and GND vias in different decaps

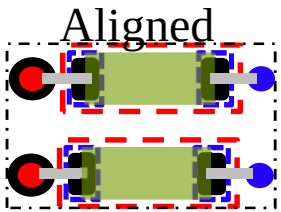
Mutual inductance between the PWR and GND, or between PWR and GND vias in different decaps

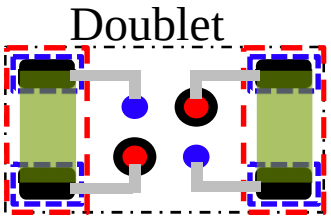


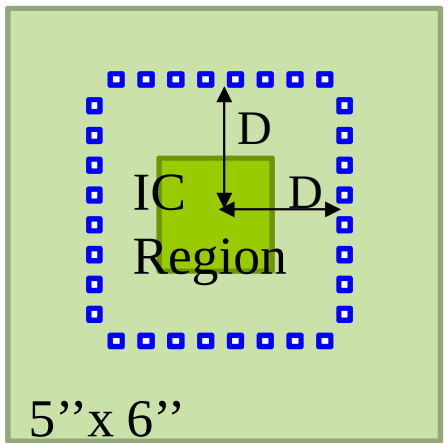
Decap 0201, h=40mils	Aligned	Alternating	Doublet
$L_{PCB\_Decap}\|_{nDecapPair=1}$	798pH	372pH	246pH

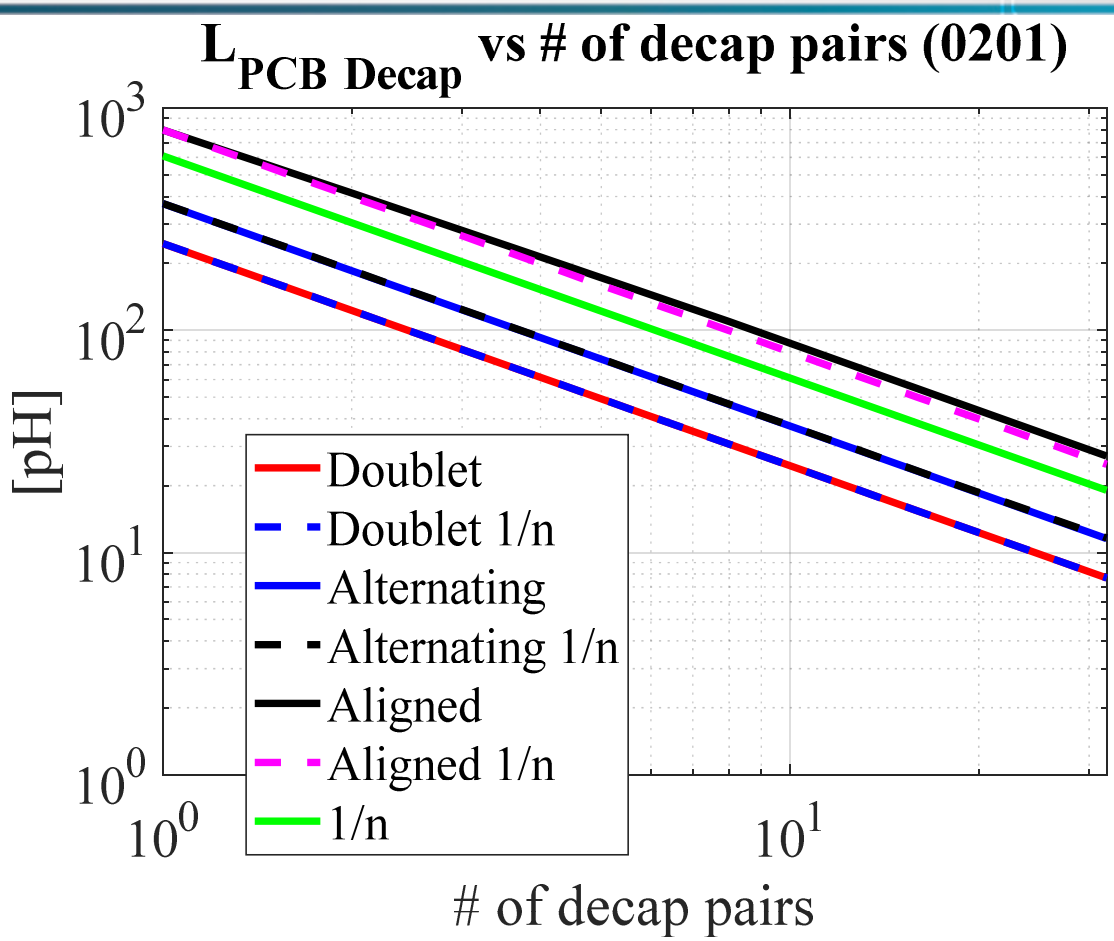
L_{PCB_Decap} Functional Variation









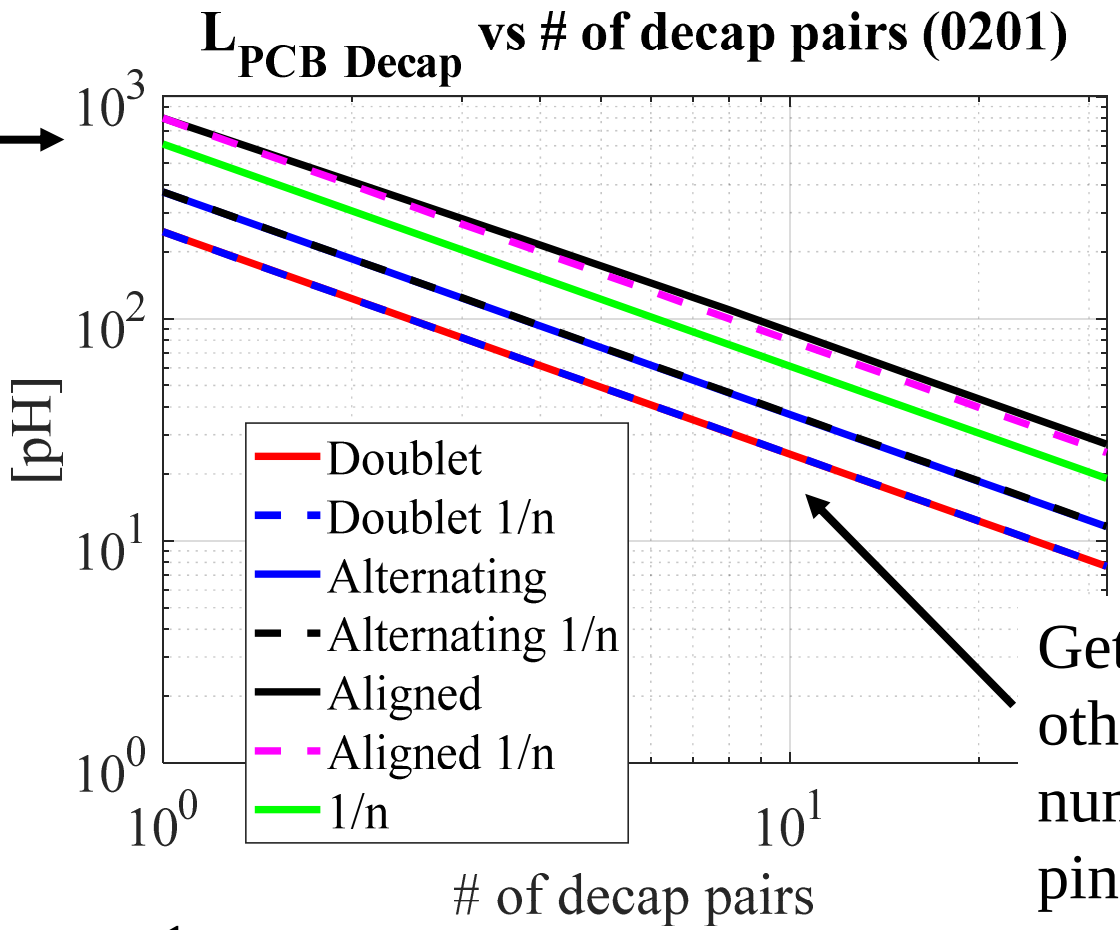


$$\frac{1}{n_{pair}}$$ convergence rate for all SMT package sizes

*The L_{PCB_Decap} is simulated in PDN Tool and the inductance is extracted from $|Z_{PDN}|$.

L_{PCB_Decap} Convergence

Calculate inductance of 1pair

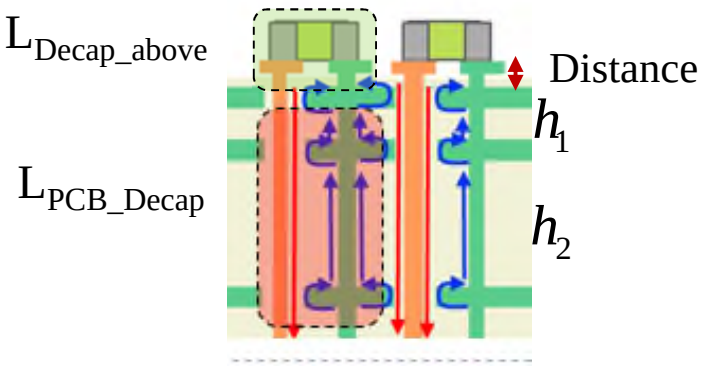


Get any other number of pins as 1/n

$$\frac{1}{n_{pair}}$$

convergence rate for all SMT package sizes

L_{PCB_Decap} Design Calculations



$$L_{Decap\_total\_1pair} = L_{Decap\_above} + L_{PCB\_Decap}$$

$$L_{PCB\_Decap\_1pair} = h \times L_{PCB\_Decap\_PUL}\big|_{npair=1}$$

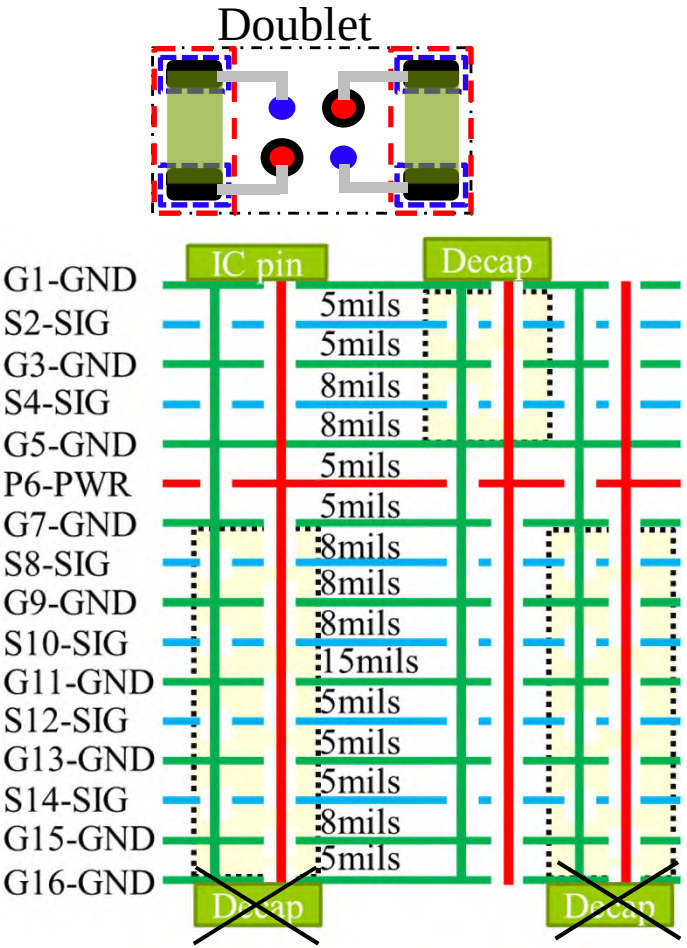
$$h = h_1 + h_2$$

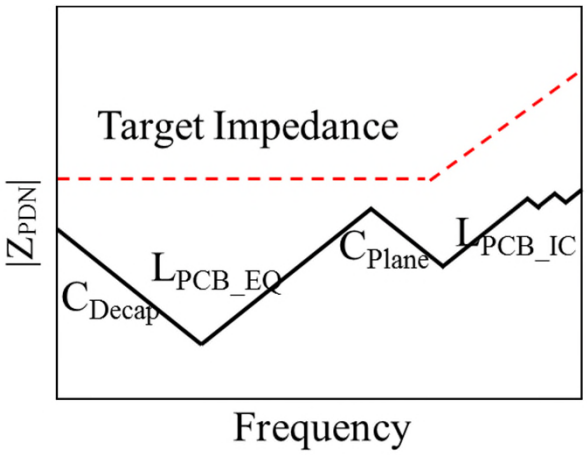
L_{PCB_Decap} per mil for one decap pair [pH]

$L_{PCB\_Decap\_PUL}\|_{npair=1}$	Aligned	Alternating	Doublet	Single decap /2
0201	20.8	11.3	6.8	14.6
0402	21.4	11.8	6.8	15.3
0603	23.4	14.6	6.8	17.4
0805	23.4	15.5	6.8	17.8

L_{PCB_Decap} Design Considerations

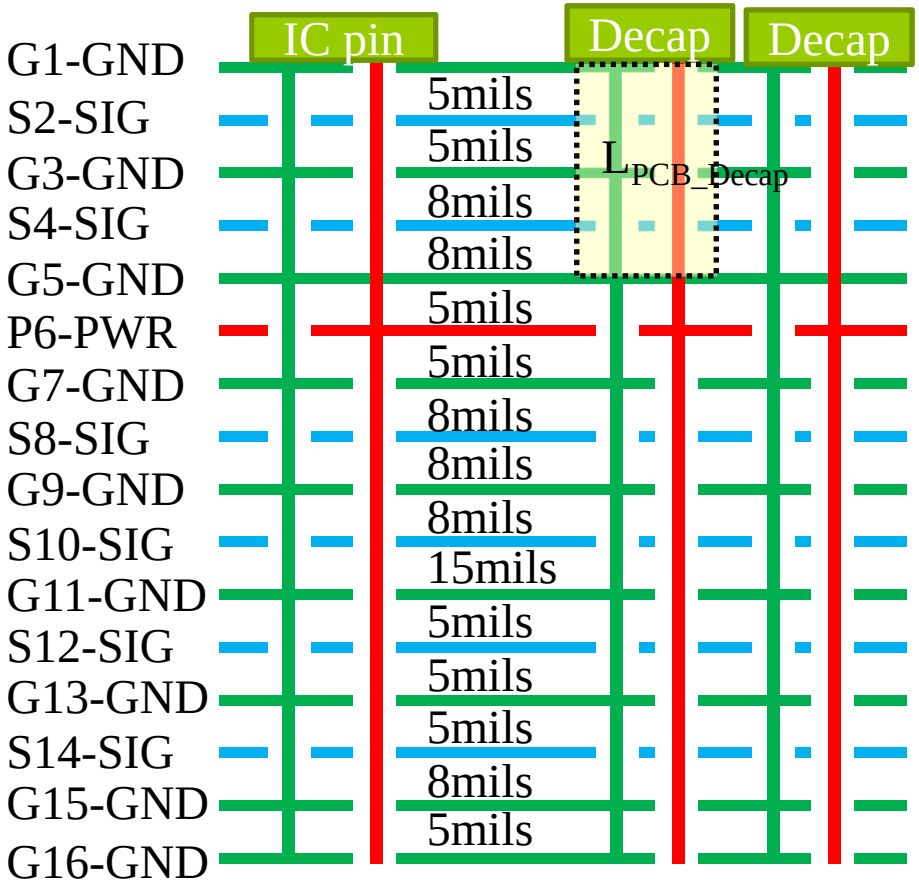
- Use the decap placement with the lowest L_{PCB_Decap} value
- Based on the stack-up, place the decaps on bottom or top layer closer to the power net area fill layer (to make the loop area of the decap interconnect smallest)
- Calculate the # of decaps needed to achieve L_{PCB_EQ} below the target impedance

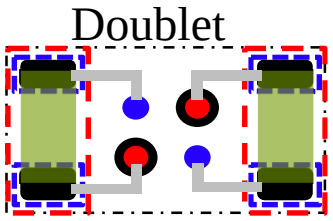




$$L_{PCB\_EQ} = L_{PCB\_IC} + L_{PCB\_Decap} + L_{PCB\_Plane} + L_{above}$$

L_{PCB_Decap} Design Example





Requirement

L_{PCB_Decap} <= 22 pH

$$L_{PCB\_Decap\_1pair} = h \times L_{PCB\_Decap\_PUL}\big|_{npair=1}$$

$$L_{PCB\_Decap\_PUL}\big|_{npair=1} = 6.8\,pH/mil$$

$$h = 26mils$$

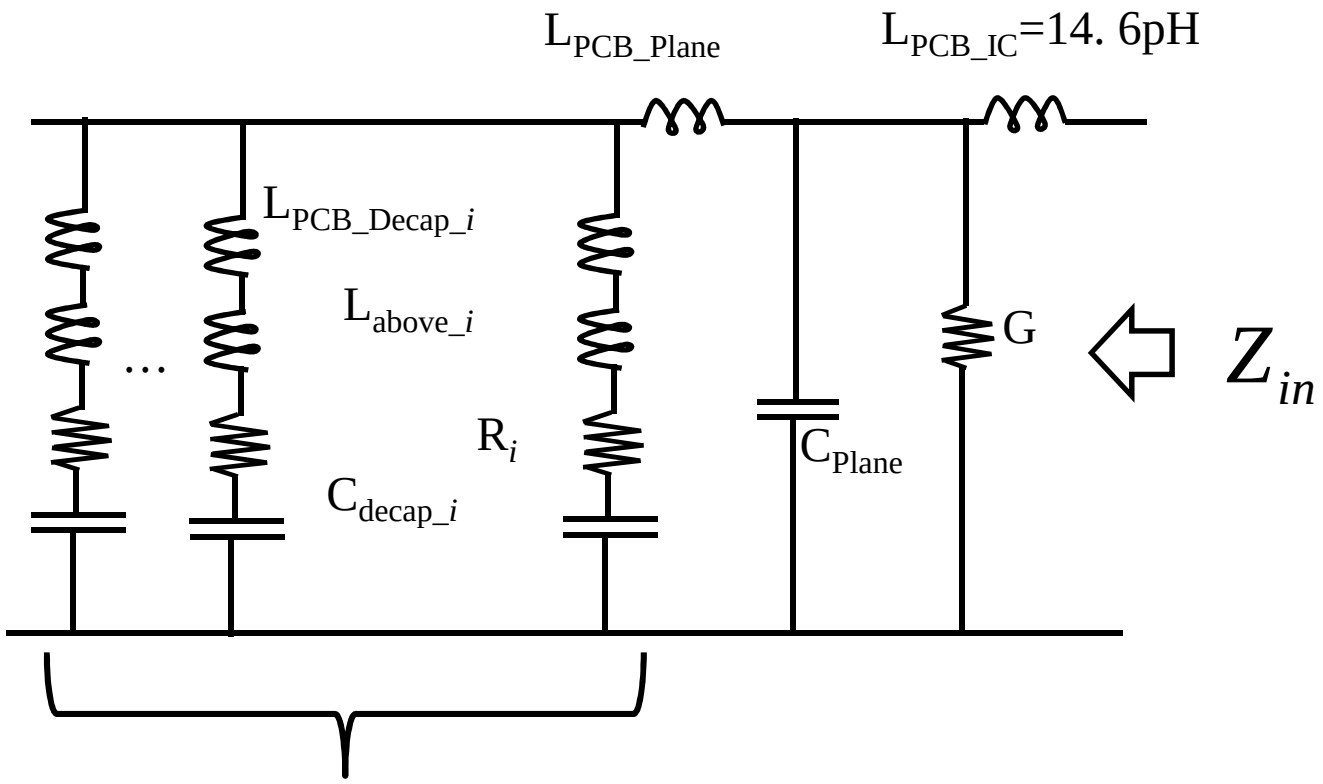
$$L_{PCB\_Decap\_1pair} = 177\,pH$$

$$L_{PCB\_Decap} = \frac{L_{PCB\_Decap\_PUL}\big|_{n_{(decap\ pair)}=1}}{n_{(decap\ pair)}} \times h$$

$$\frac{177\,pH}{n_{(decap\ pair)}} < 22\,pH$$

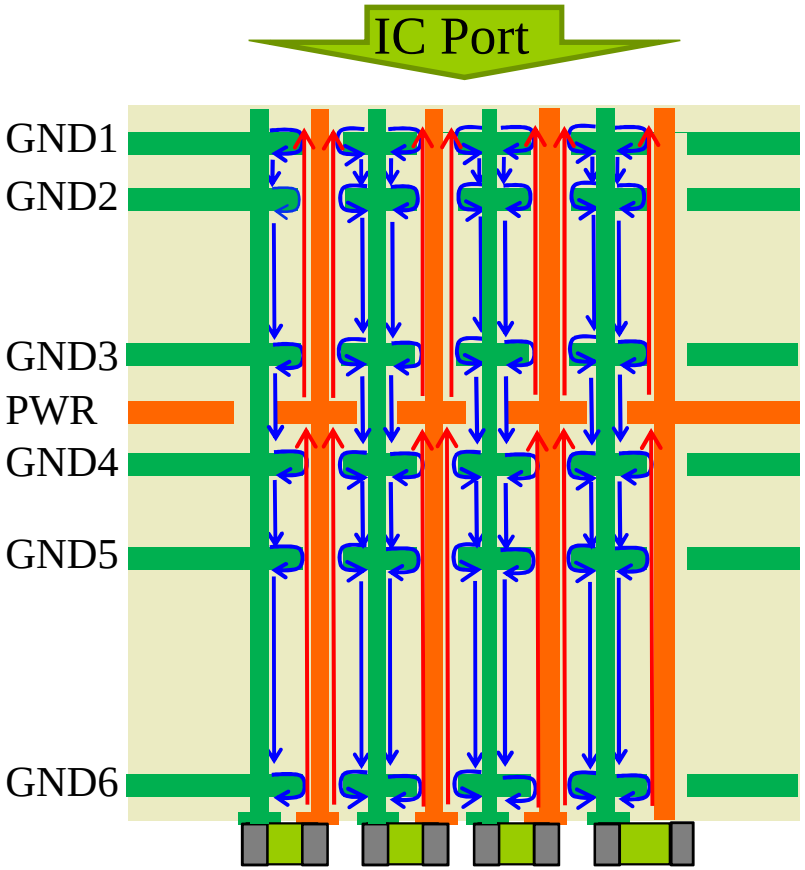
$$n_{(decap\_pair)} \geq 8$$

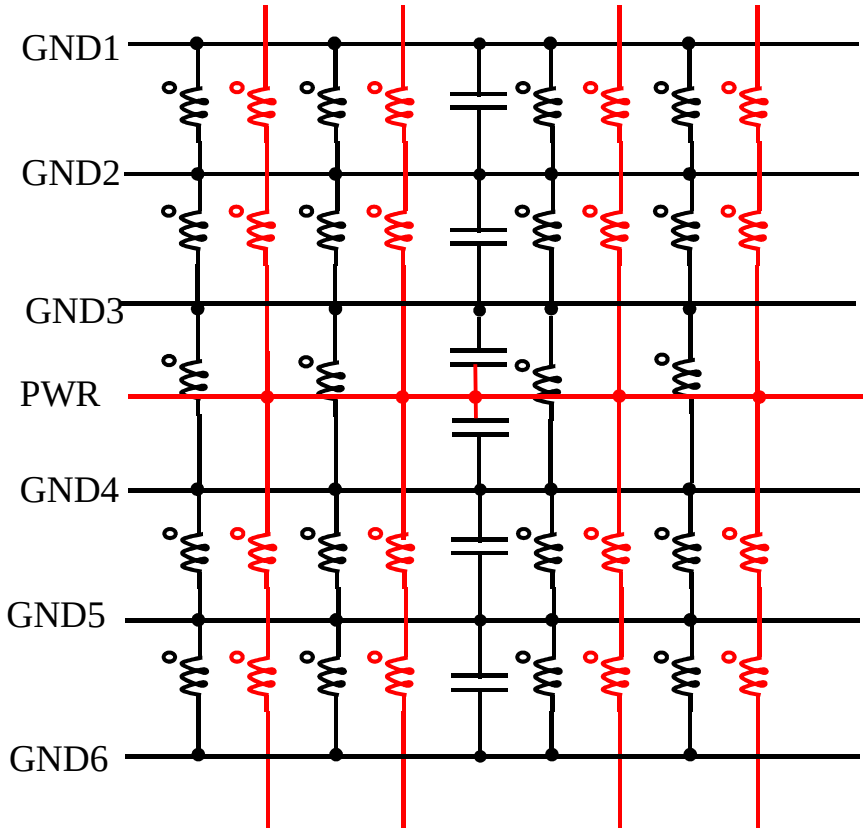
Impedance Equivalent Circuit



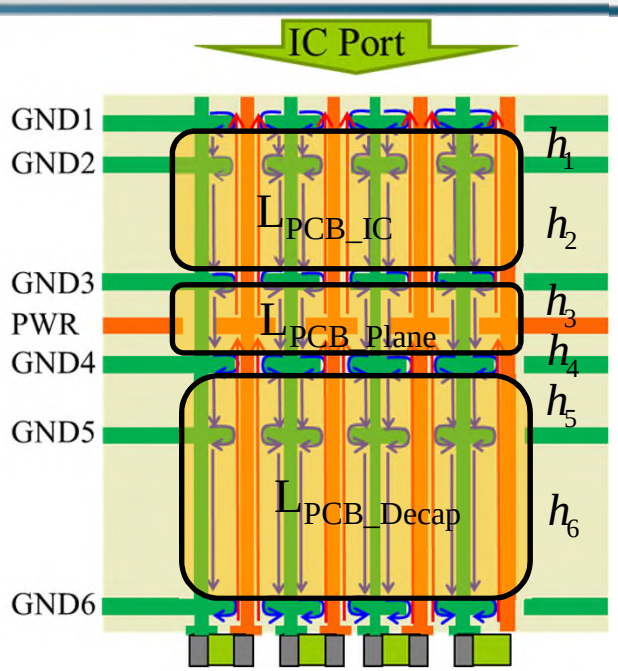
$L_{PCB\_Decap\_i}$=177 pH (pair)

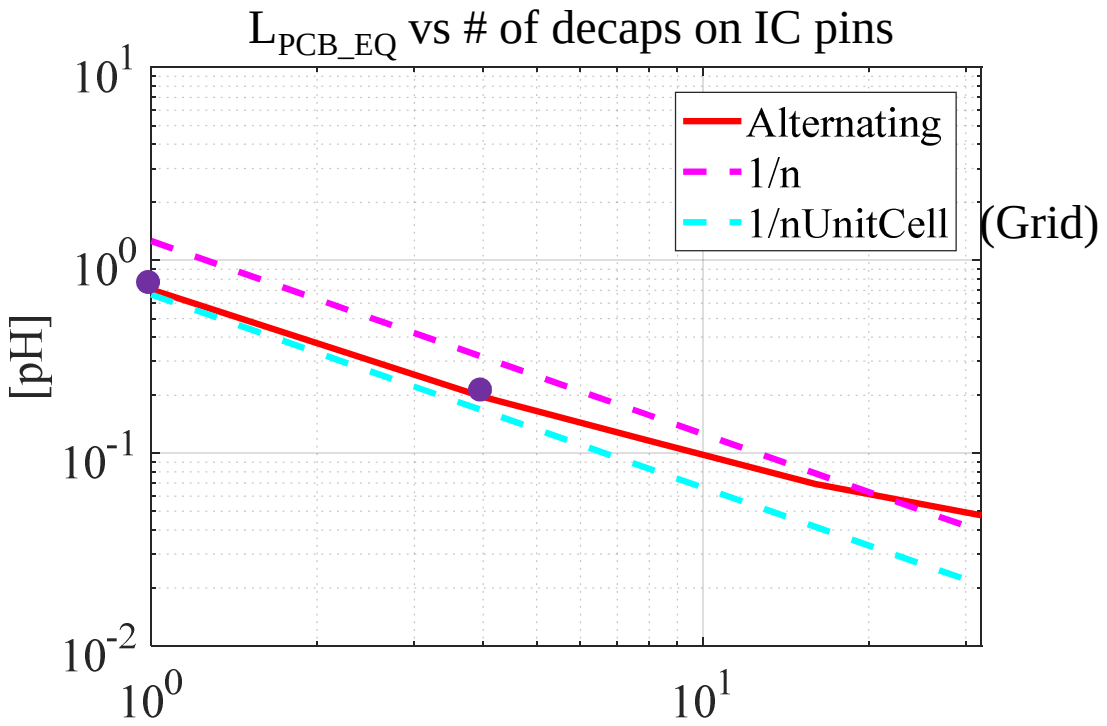
Decaps Under the IC

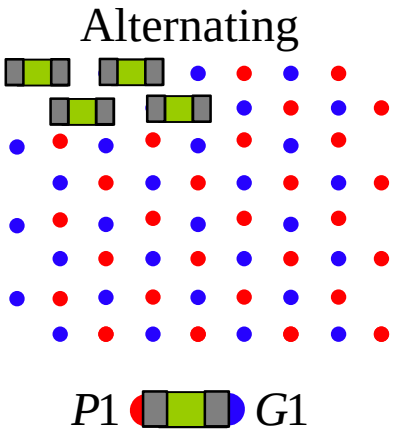


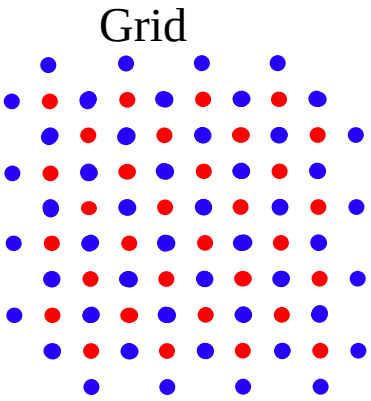


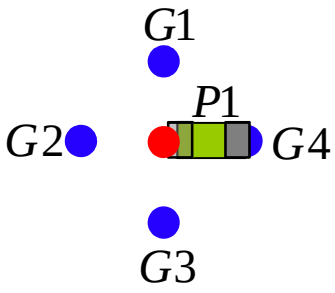
L_{PCB_EQ} Variation for Decaps Under the IC





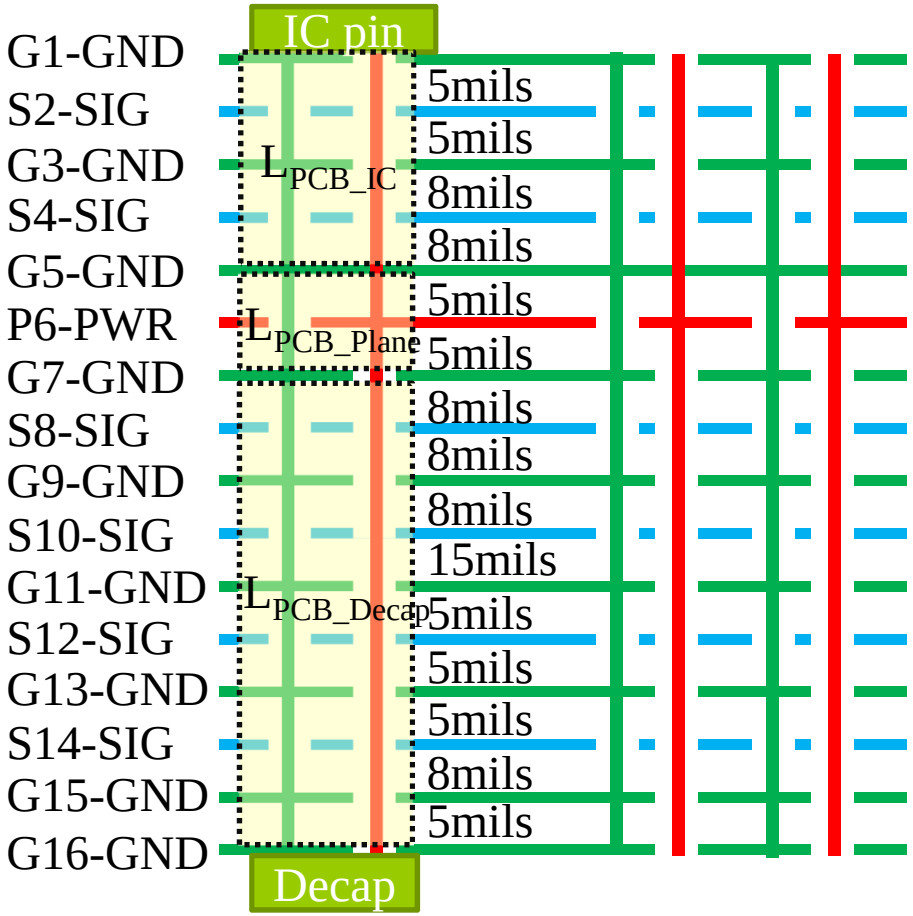




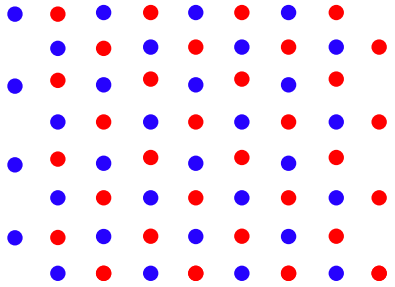


*The L_{PCB_EQ} is simulated and the inductance is extracted from $|Z_{PDN}|$.

L_{PCB_EQ} Example for Decaps Under the IC



Alternating



Drill size = 15mils,
Anti-pad size = 39mils,
Pitch = 1mm.

$$L_{PCB\_IC} = h \times \frac{L_{self\_PUL,1pin}}{n_{ICpin}},$$

$$L_{PCB\_Plane} = h_{Plane} \times \frac{L_{self\_PUL,1pin}}{n_{ICpin}}$$

$$L_{self\_PUL,1pin} = 18\,pH/mils$$

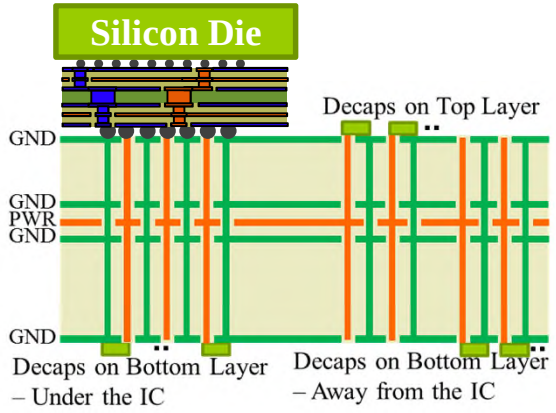
$$h = 26mils, h_{Plane} = 10mils$$

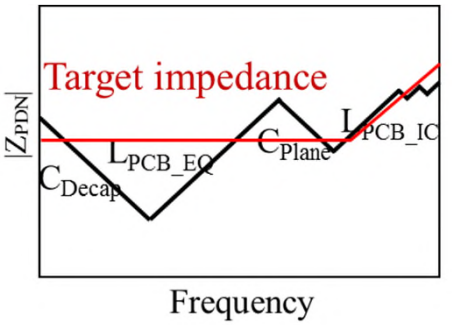
$$L_{PCB\_IC} + L_{PCB\_Plane} = \frac{648\,pH}{n_{ICpin}}$$

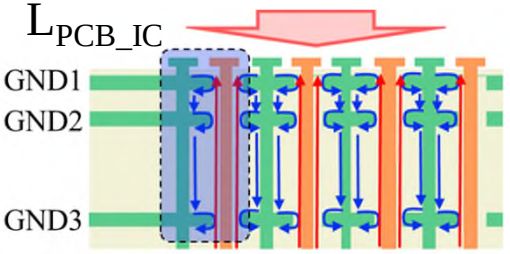
L_{PCB_Decap} ➡ Design Library (under development)

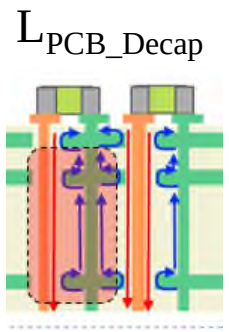
Outline

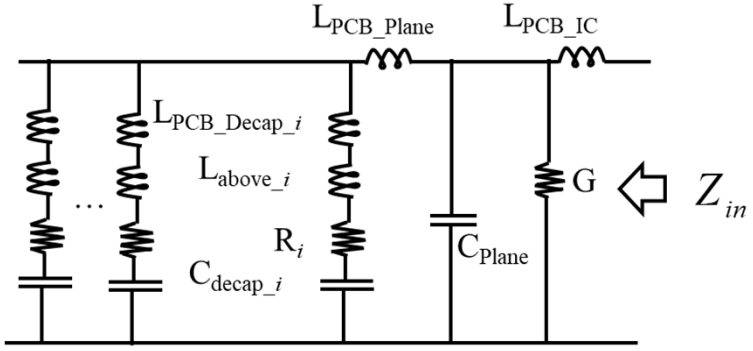
- Problem and concepts
- PDN pre-layout design methodology
  - Example geometry
  - L_{PCB_IC} calculation
  - L_{PCB_decap} calculation
  - **L_{PCB_plane} calculation**
  - L_{above} calculation

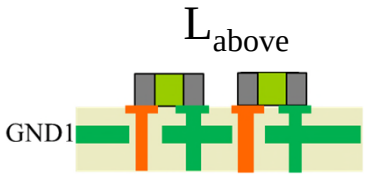




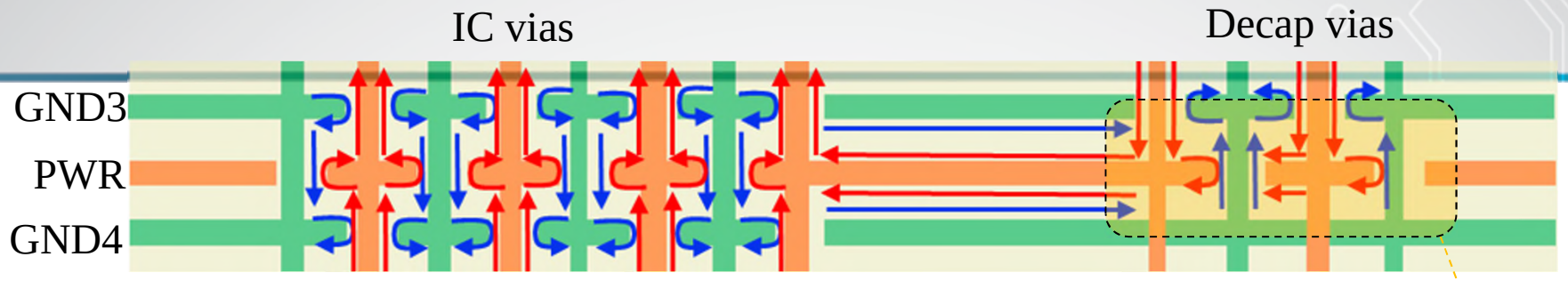




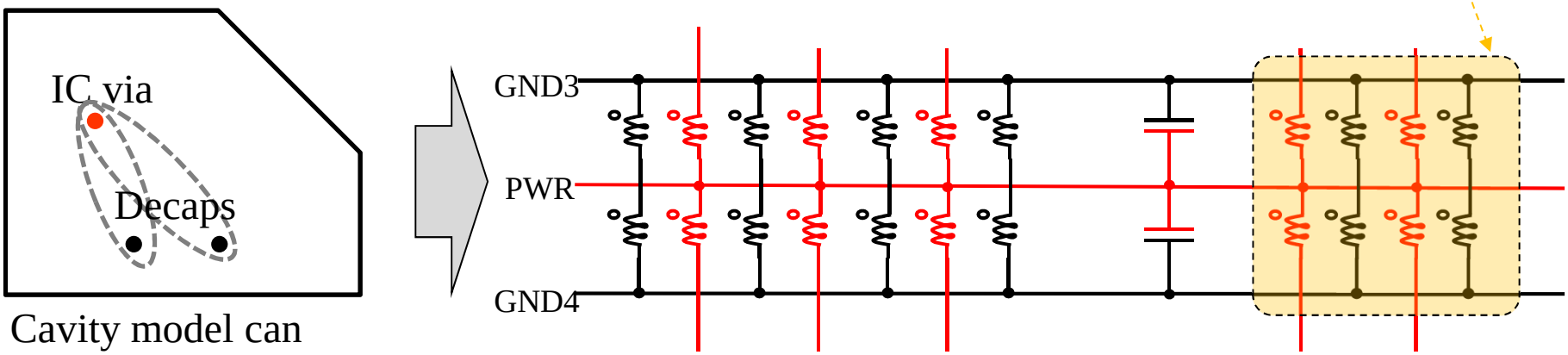




L_{PCB_Plane} Geometry

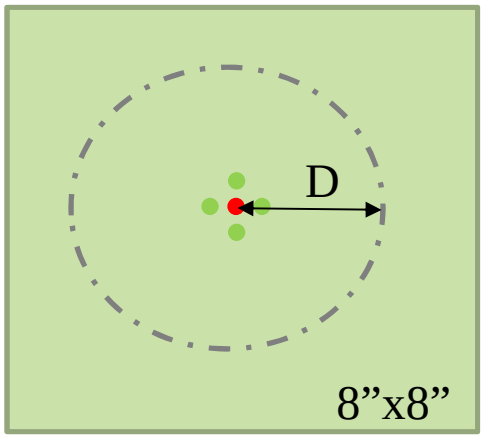


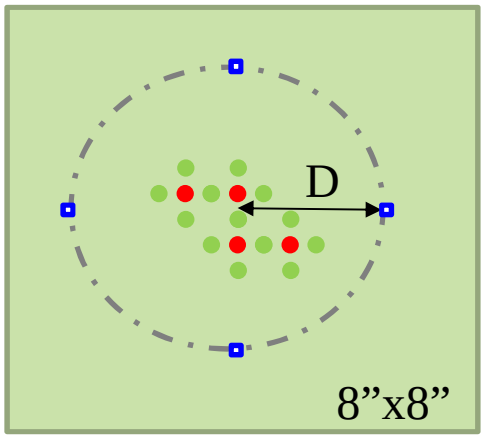
- If the current path on the power net is direct to decaps and L is not significantly changed due to power net voids, the following design curves are used.
- Horizontal inductance and vertical inductance are merged in the model and final equivalent circuit model is constructed as below.



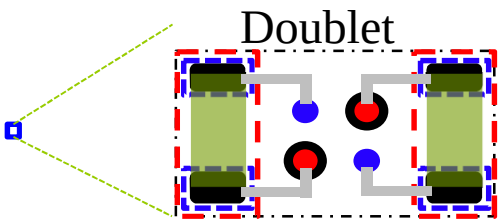
Cavity model can well estimate the inductance.

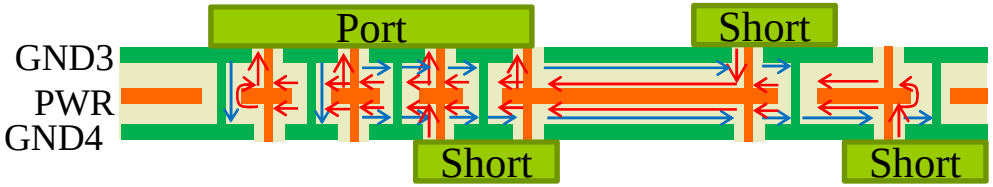
L_{PCB_Plane} Geometry



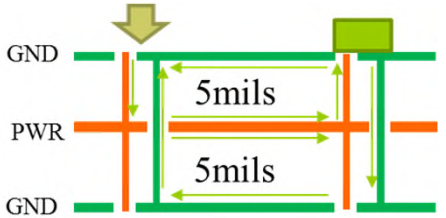


Decaps





Stack-up

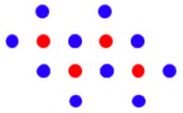


IC Region

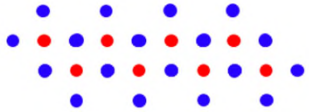
D=1”, Pitch = 1mm

1 IC Pin

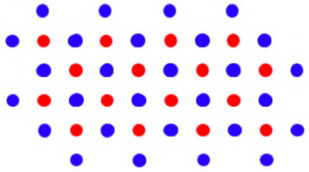
4 IC Pin



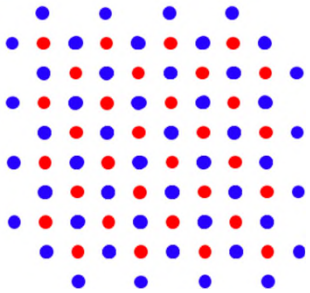
8 IC Pin



16 IC Pin

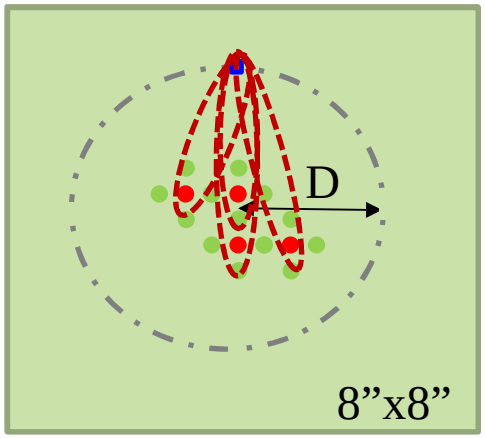


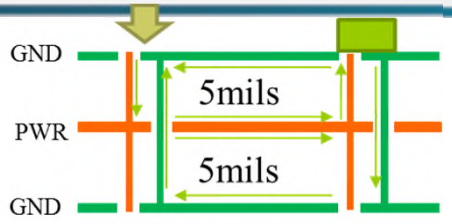
32 IC Pin



- GND via
- PWR via

L_{PCB_Plane} Current Physics and Inductance

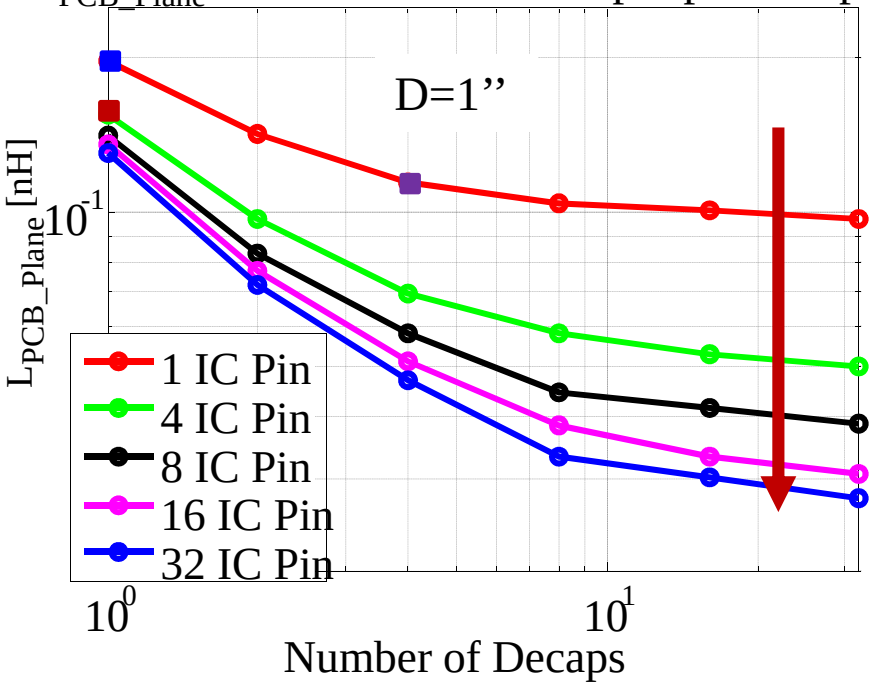




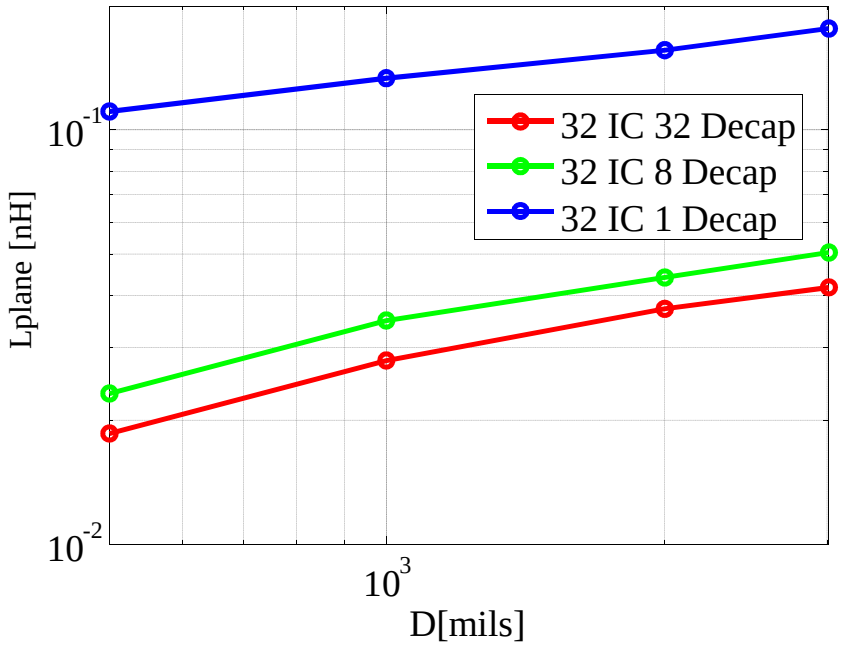
Pitch = 1mm

Decaps are placed on the top layer

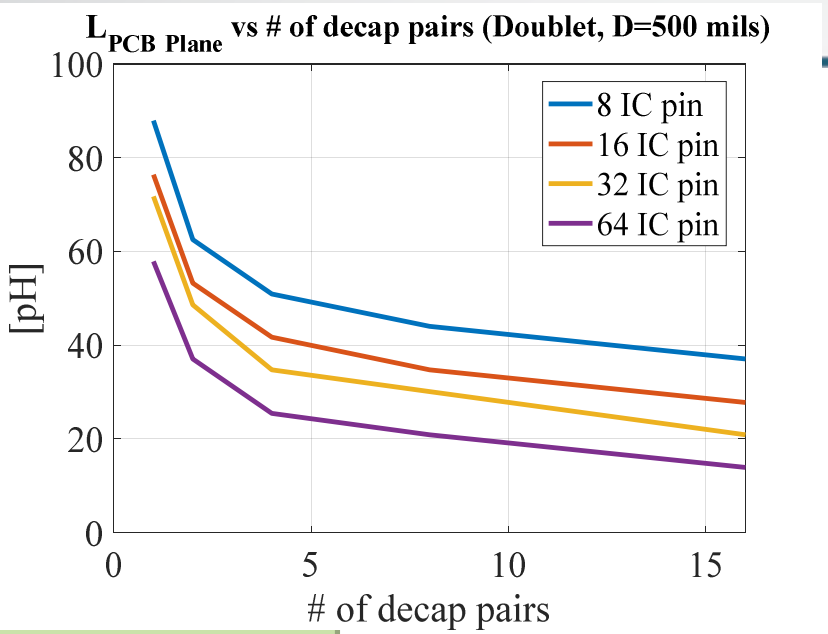
L_{PCB_Plane} decreases with multiple parallel paths

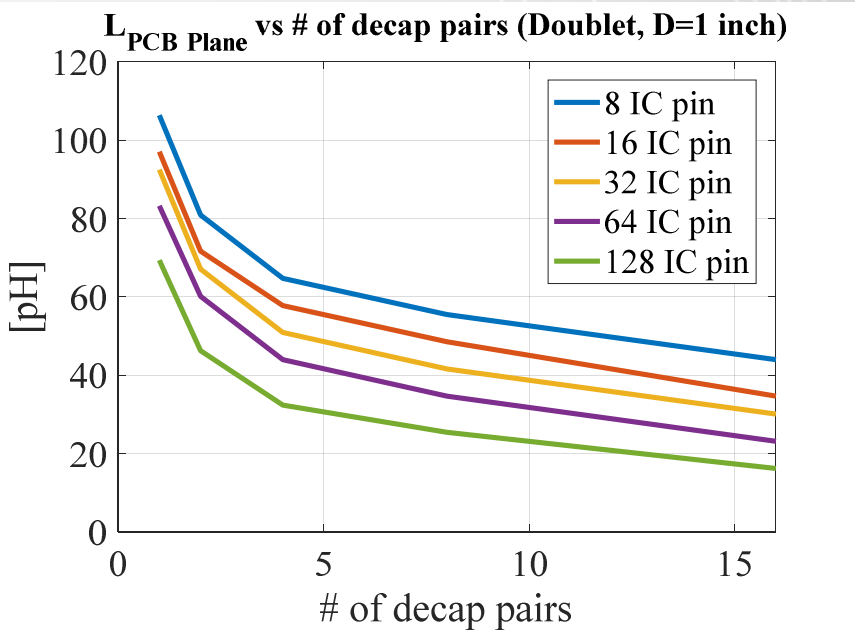


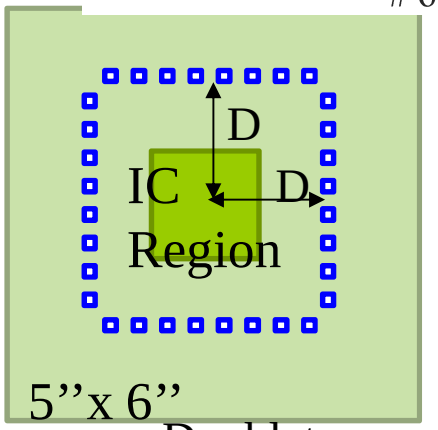
L_{PCB_Plane} vs D

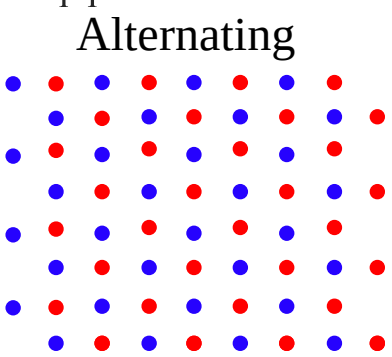


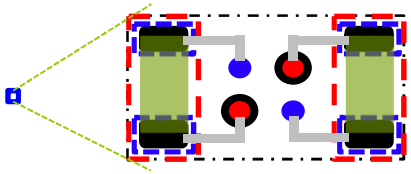
L_{PCB_Plane} Design Curves

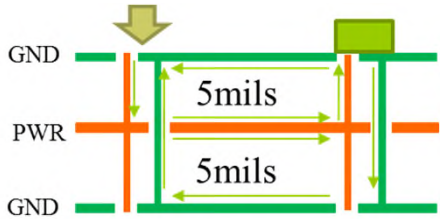


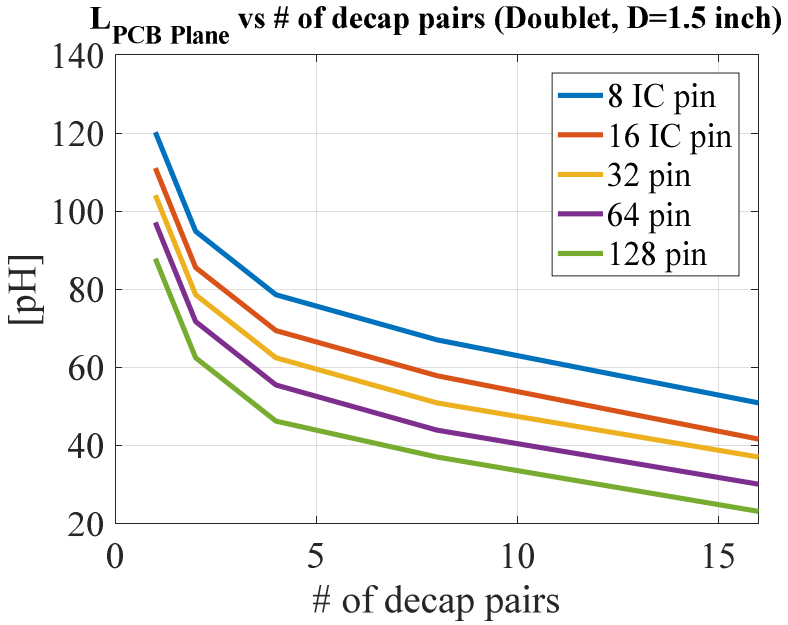




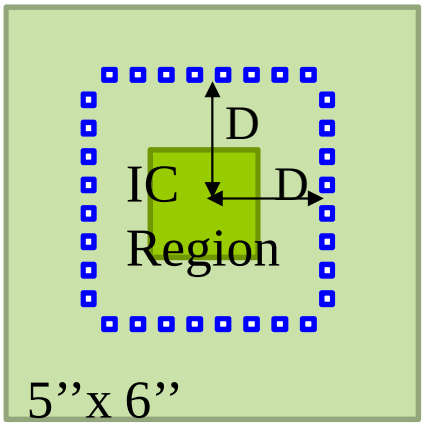








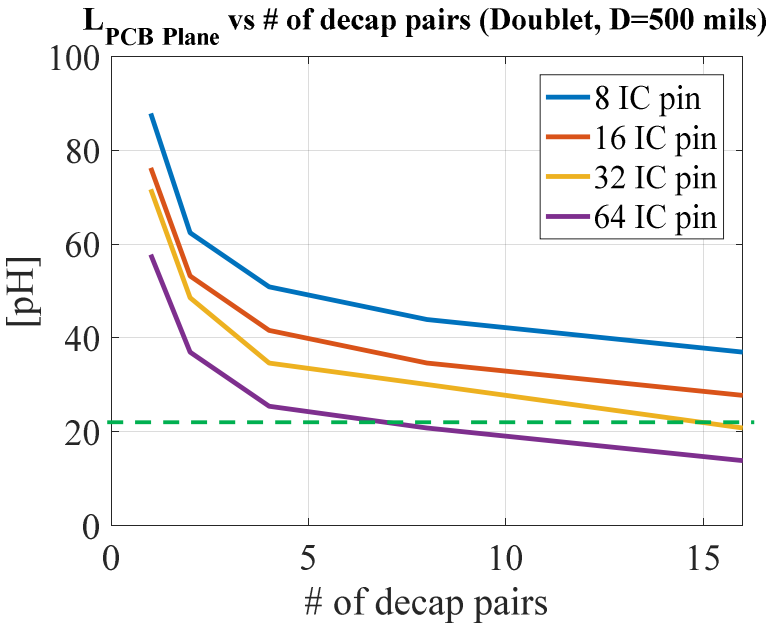
L_{PCB_Plane} Example



Requirement: L_{PCB_Plane} <=22 pH

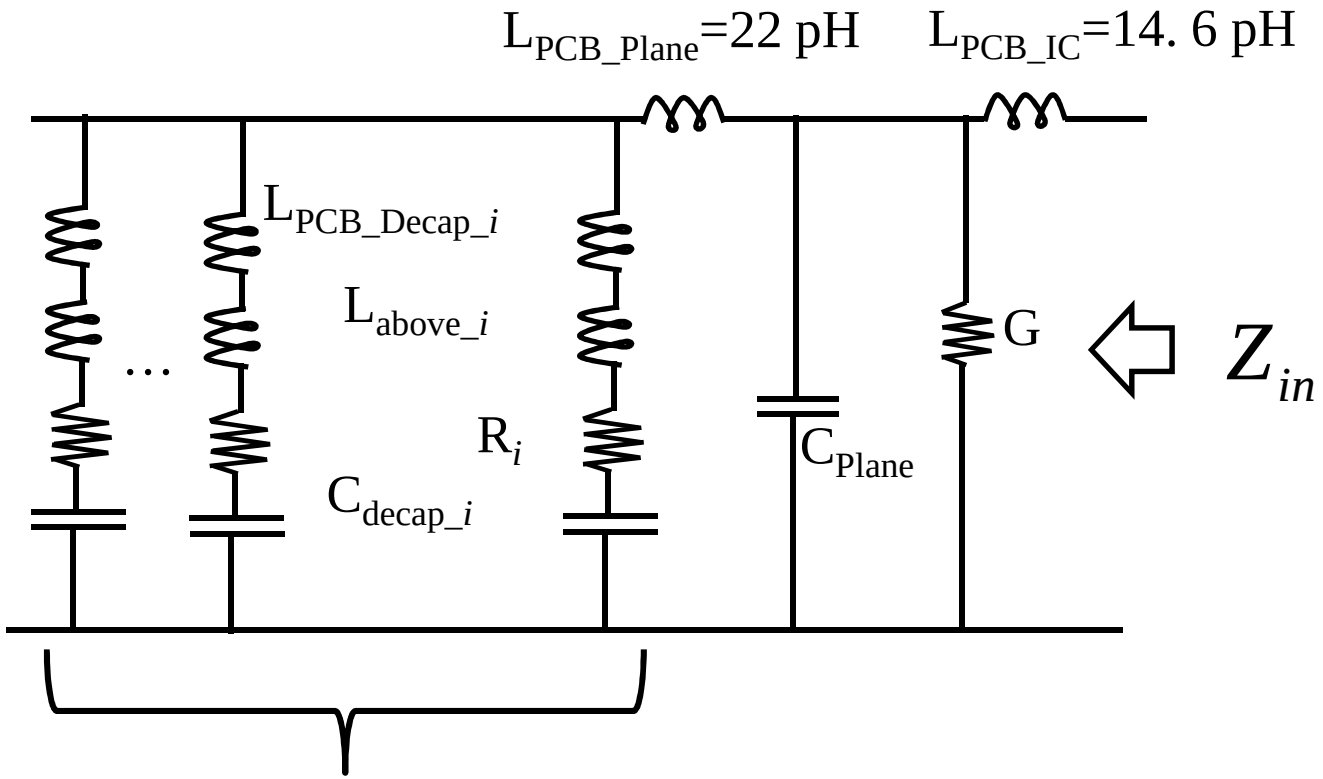
From the design curves, D=500mils, n_{Decap_Pair} >=16.

Combine the requirement from L_{PCB_IC}, L_{PCB_Decap}, n_{ICpin} >=6, n_{Decap_Pair} >=8



n_{ICpin} =32, n_{Decap_Pair} >=16

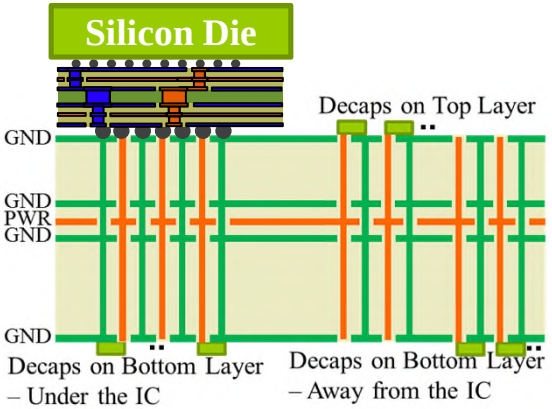
Impedance Equivalent Circuit

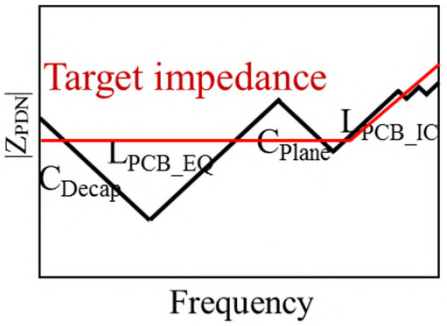


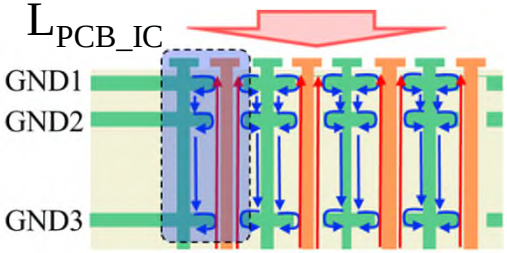
$L_{PCB\_Decap\_i}$=177 pH (pair)

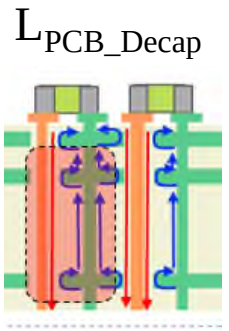
Outline

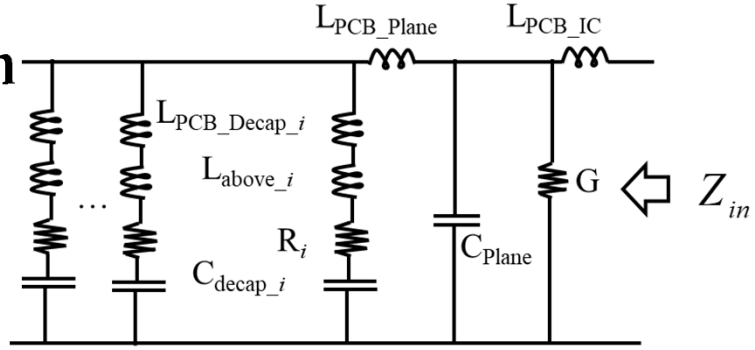
- Problem and concepts
- PDN pre-layout design methodology
  - Example geometry
  - L_{PCB_IC} calculation
  - L_{PCB_decap} calculation
  - L_{PCB_plane} calculation
  - **L_{above} calculation**

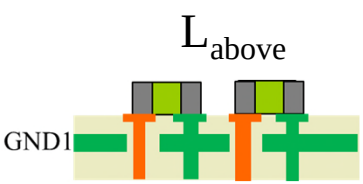




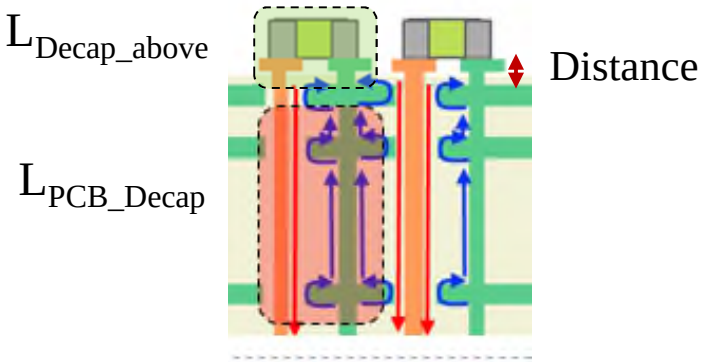




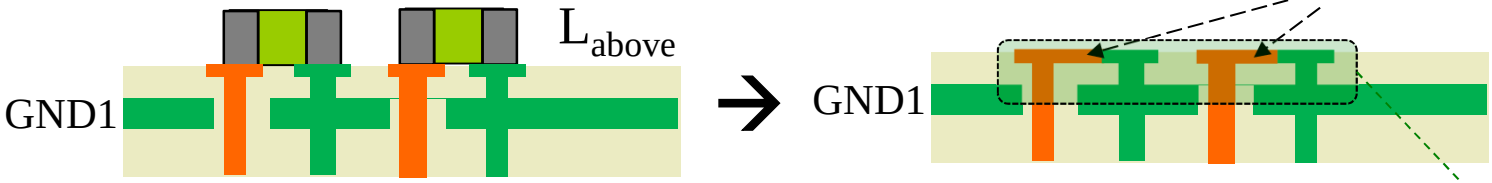




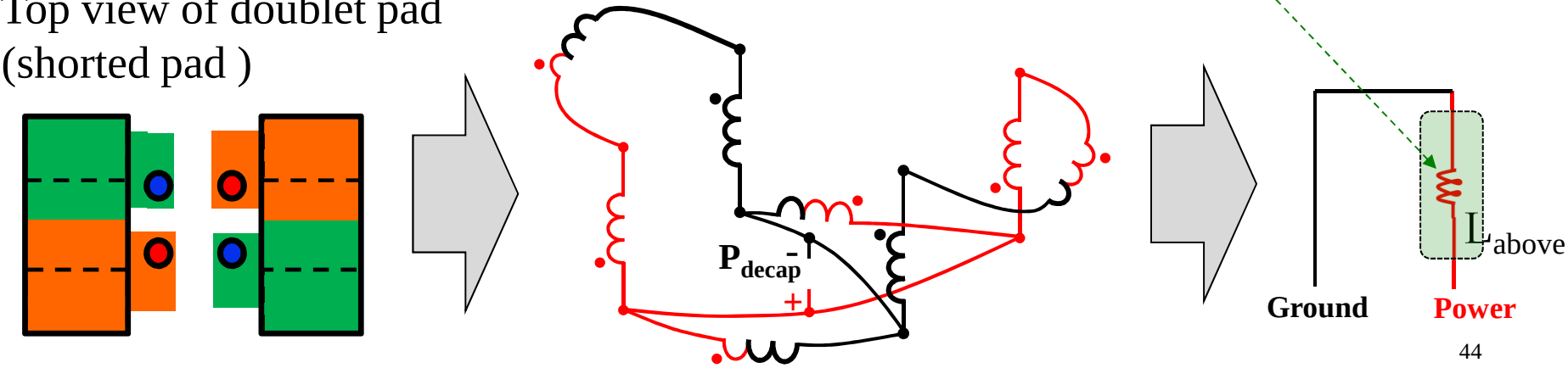
L_{above} Geometry



- PEEC method used to calculate decap pad inductance
- Get a single inductance

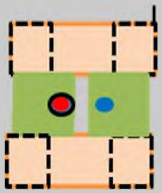
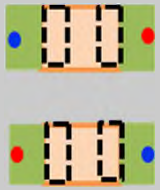
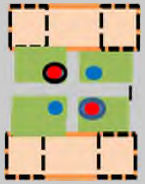
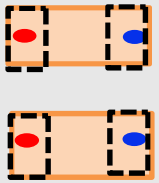
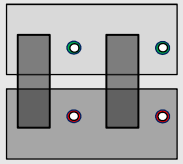
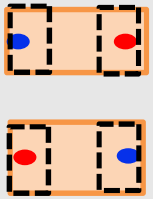
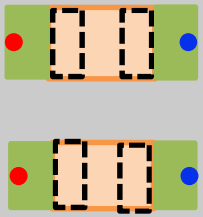
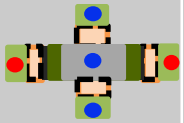
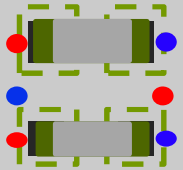


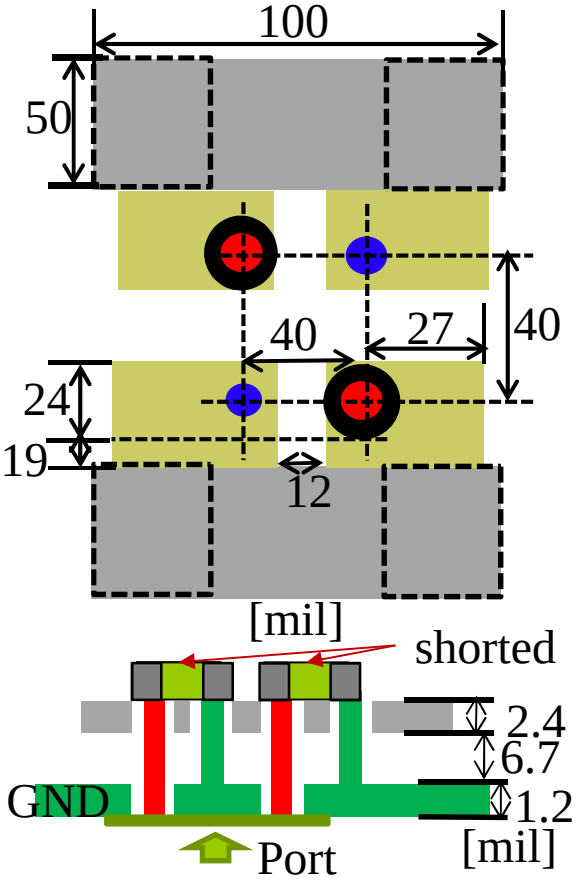
Top view of doublet pad (shorted pad)



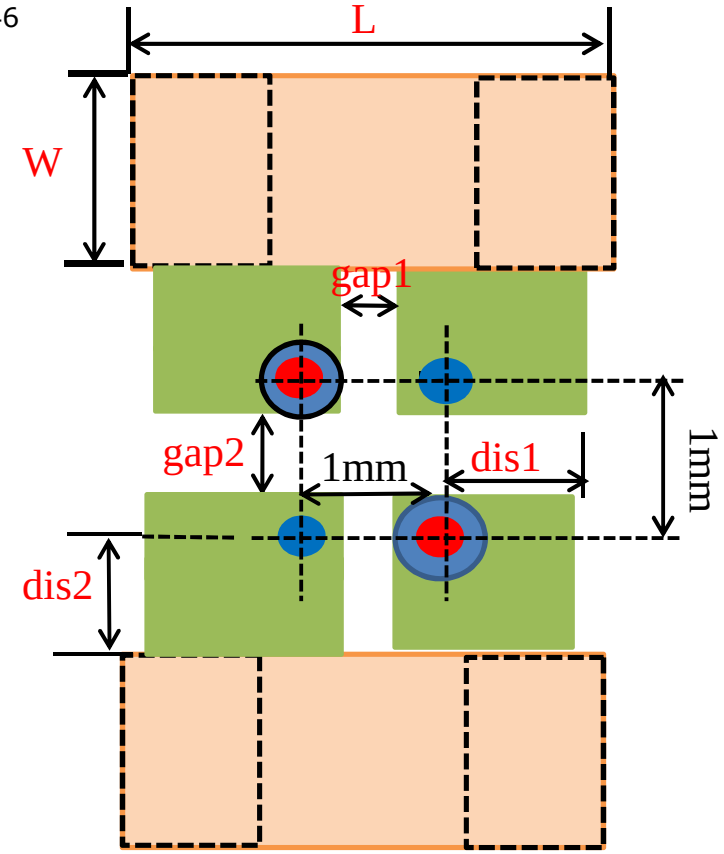
L_{above} Geometries

Decoupling capacitor of sizes 0805/0603/0402/0201 for L_{above} design space

#	Name	Figure	#	Name	Figure	#	Name	Figure
1	Shared Via		2	Power Via Alternating		3	Doublet	
4	Via in Pad		5	Shared Pad		6	Via in pad alternating	
7	PWR via in Line		8	3-terminal		9	Multi-via	



L_{above} Design Library - Doublet



Anti-Pad Diameter: 0.762mm
Pad Diameter: 0.538mm
Via Diameter (drill size): 0.25mm

With Different package sizes,

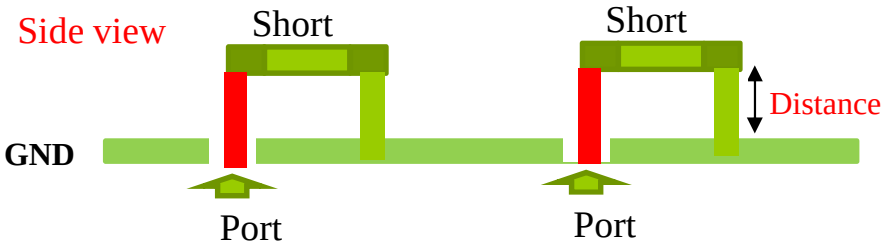
- 0201, 0402, 0603, 0805

Using wider trace to minimize inductance

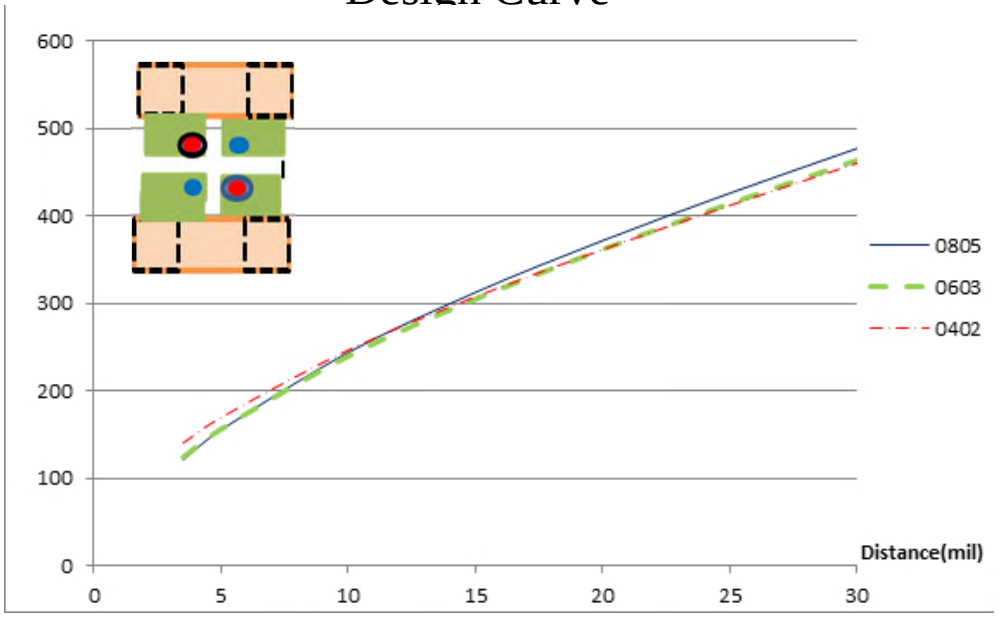
What will change	0201	0402	0603	0805
L		56 mil	78 mil	100 mil
W		20 mil	30 mil	50 mil
gap1		18 mil	18 mil	12 mil
gap2		15 mil	15 mil	21 mil
dis1		12 mil	20 mil	31 mil
dis2		17 mil	22 mil	30 mil

What will not change	0201, 0402, 0603, 0805
pitch	1 mm

L_{above} Design Library - Doublet



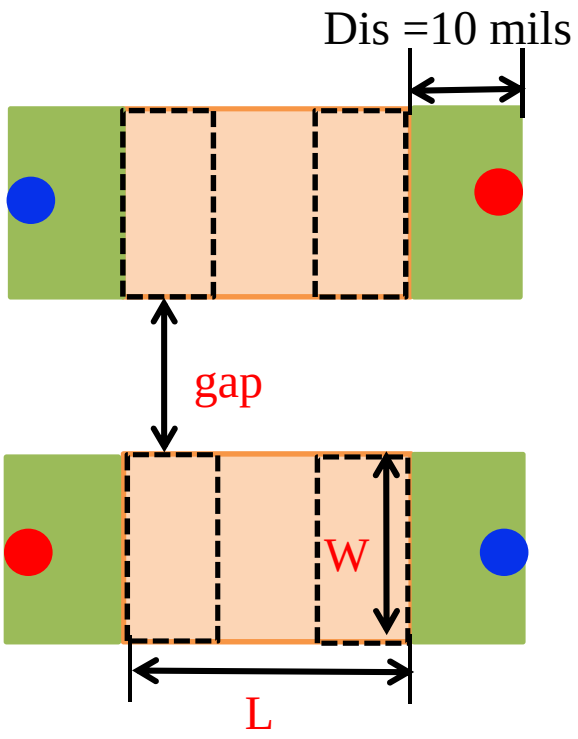
Design Curve



L_{above} for doublet layout [pH]

Distance (mil)	0805	0603	0402
3.5	125.6	123.8	132.9
5	161	157.4	166.2
10	248.2	239.9	244.6
15	313.2	301.4	302.2
20	368.4	354.3	352.3
25	419.2	403.4	399.4
30	467.5	450.4	445

L_{above} Design Library – Power Via Alternating



Power Via

Ground Via

Anti-Pad Diameter: 0.762mm
Pad Diameter: 0.538mm
Via Diameter (drill size): 0.25mm

With Different package sizes,

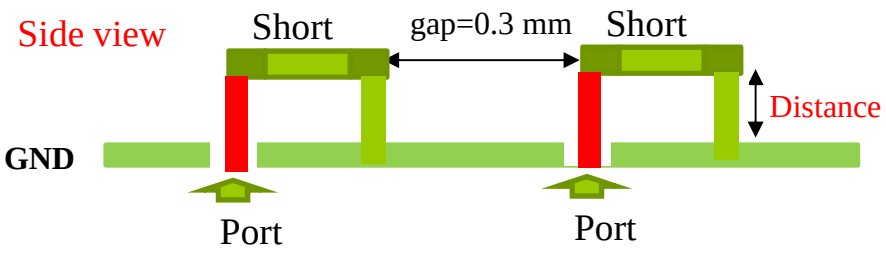
- 0201, 0402, 0603, 0805

Using wider trace to minimize inductance

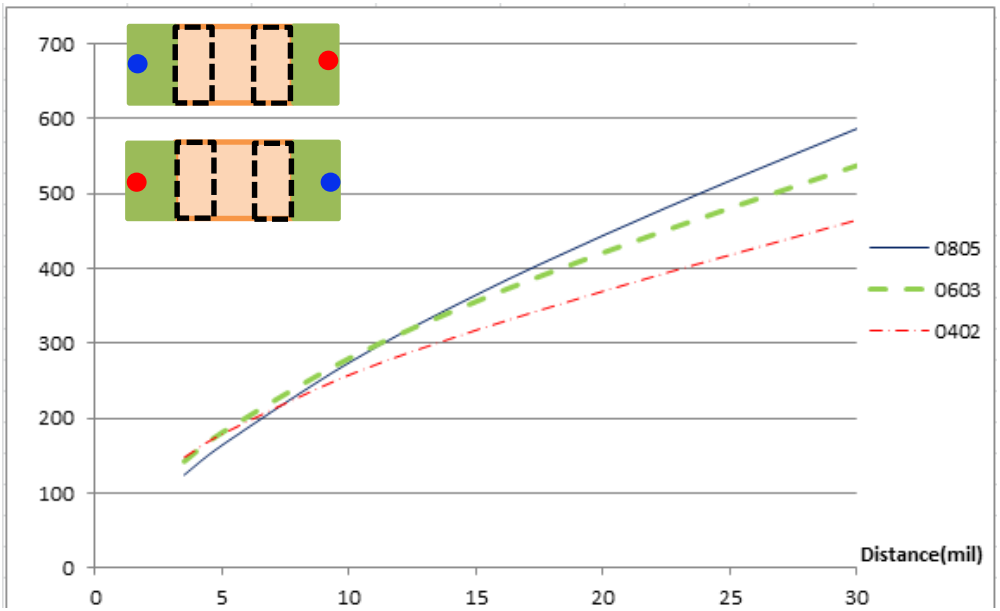
What will change	0201	0402	0603	0805
L		56 mil	78 mil	100 mil
W		20 mil	30 mil	50 mil
gap		10.5 mil	11 mil	11 mil

What will not change	0201, 0402, 0603, 0805
Dis (Pad Edge to Via)	10 mils (0.25 mm)

L_{above} Design Library – Power Via Alternating



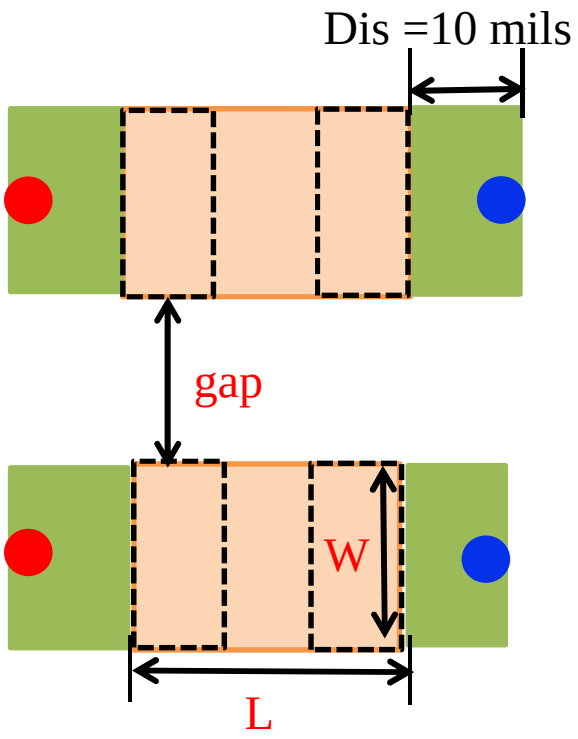
Design Curve



L_{above} for alternating layout [pH]

Distance (mil)	0805	0603	0402
3.5	124.3	142.4	147.7
5	164.2	181.1	179.1
10	274.5	280.1	257.9
15	364.7	355.9	317.7
20	444.1	421.1	369.6
25	517.2	480.8	418.2
30	586.8	537.4	464.7

L_{above} Design Library – Power Via Aligned



Power Via

Ground Via

Anti-Pad Diameter: 0.762mm
Pad Diameter: 0.538mm
Via Diameter (drill size): 0.25mm

With Different package sizes,

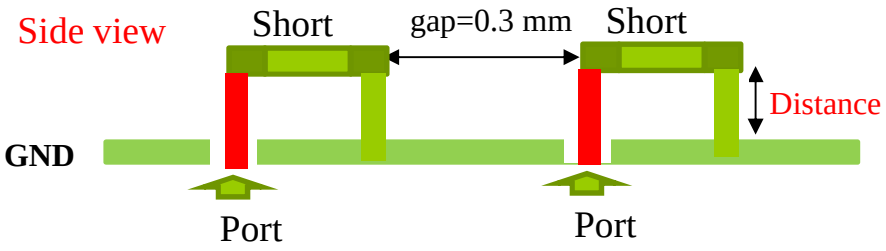
- 0201, 0402, 0603, 0805

Using wider trace to minimize inductance

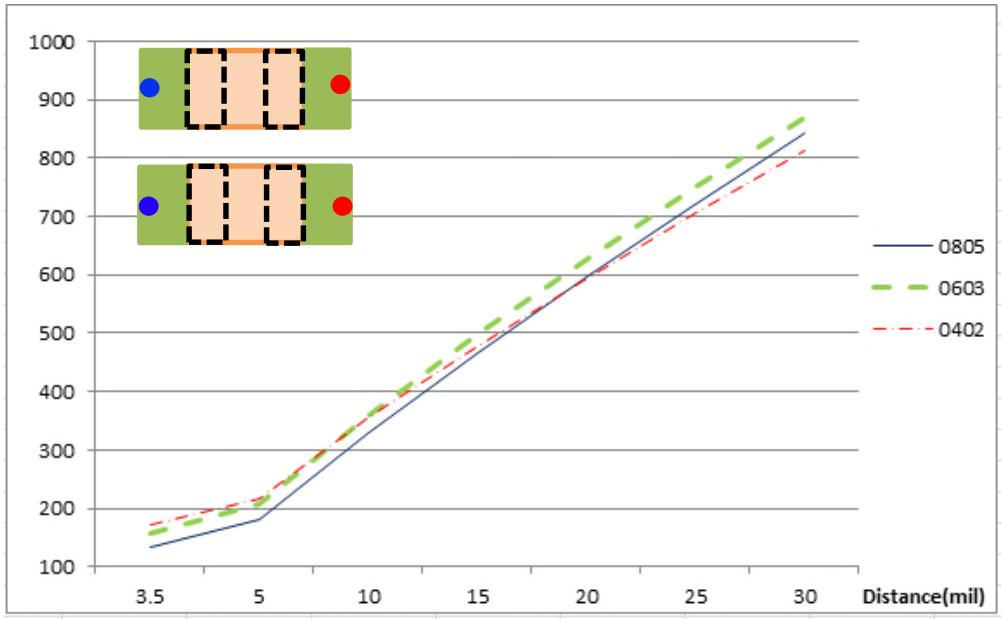
What will change	0201	0402	0603	0805
L		56 mil	78 mil	100 mil
W		20 mil	30 mil	50 mil
gap		10.5 mil	11 mil	11 mil

What will not change	0201, 0402, 0603, 0805
Dis (Pad Edge to Via)	10 mils (0.25 mm)

L_{above} Design Library – Power Via Aligned



Design Curve

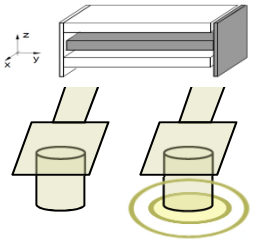


L_{above} for aligned layout [pH]

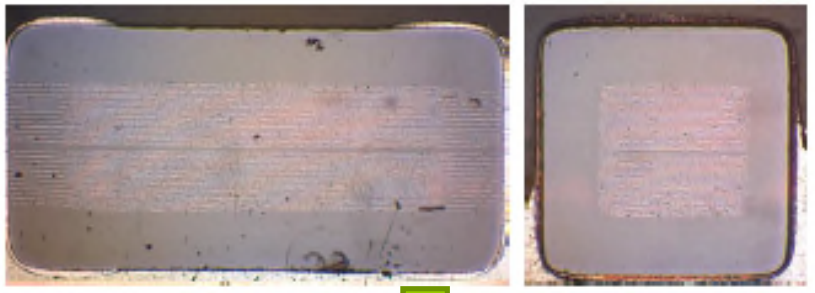
Distance (mil)	0805	0603	0402
3.5	132.4	157.3	172.4
5	180.1	208.1	217.8
10	327.8	360.3	354.8
15	464.7	497.8	478.4
20	595	626.8	594.5
25	721.3	749.8	705.4
30	842.8	868.8	812.9

L_{above} Modeling with Decaps

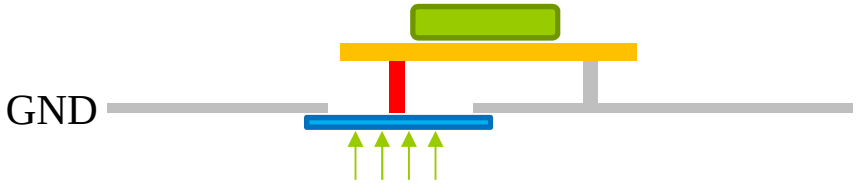
Via, pad, trace, one decap

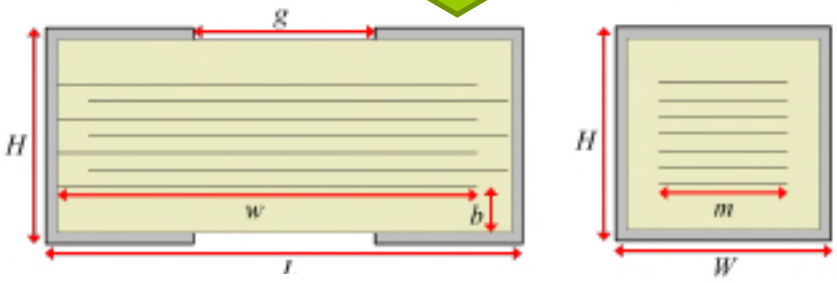


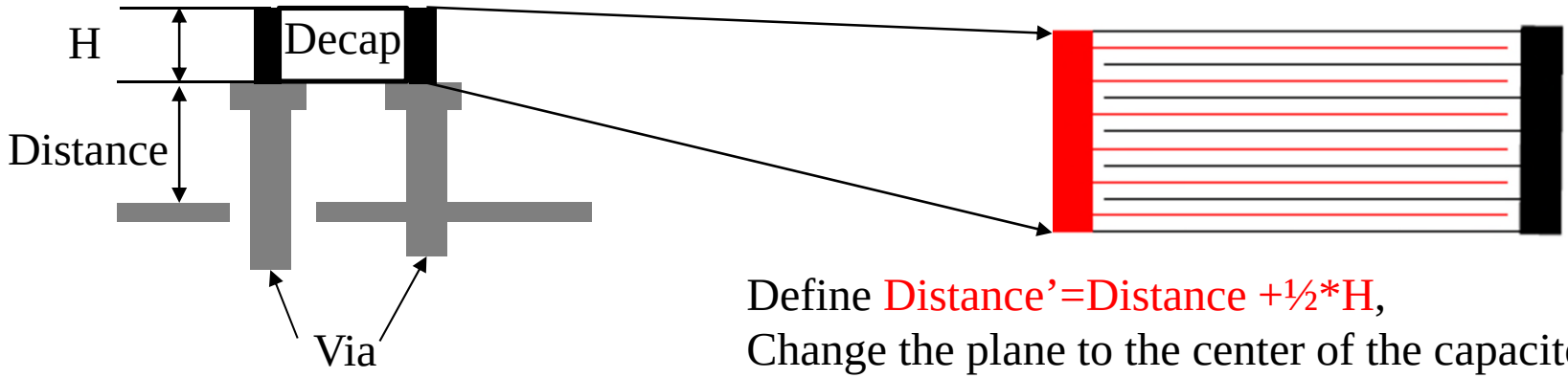
Decoupling capacitor model



Decoupling capacitor







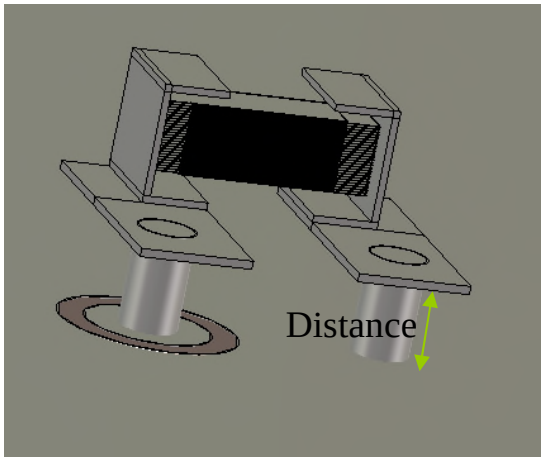
Define Distance'=Distance +½*H,
Change the plane to the center of the capacitor (without including Decap in the model).

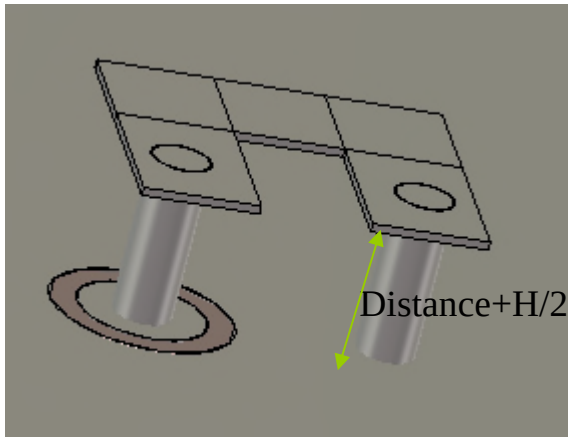
L_{above} Modeling

0402 Type Decap

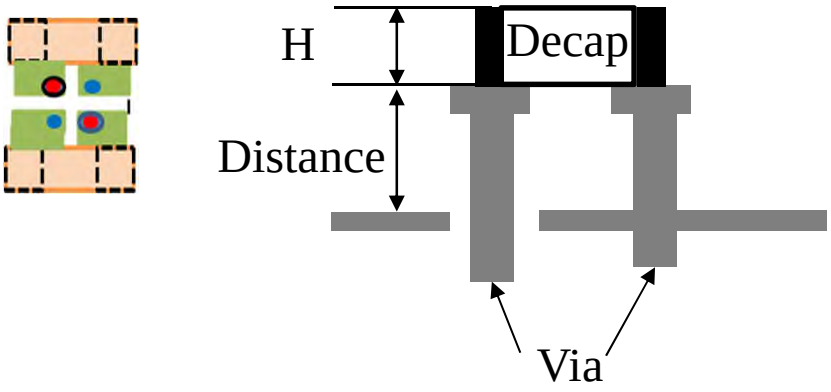
Distance (mil)	Inductance (pH)	Distance'	Inductance (pH)	Difference
5	615.34	5+H/2	602.32	2.12%
8	677.26	8+H/2	655.07	3.26%
15	883.43	15+H/2	828.04	6.27%

CST Model





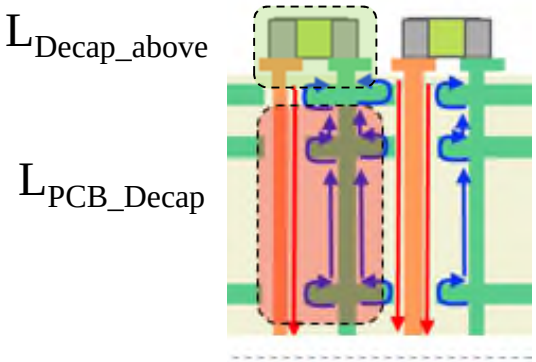
L_{above} Example



$$L_{PCB\_Decap\_1pair} = 177\,pH$$

Pick doublet 0805 layout for L_{above} calculation with distance = 5mils, and decap body height H = 10mils. Then distance + H/2=10mils. From the library, the L_{above} for one decap is

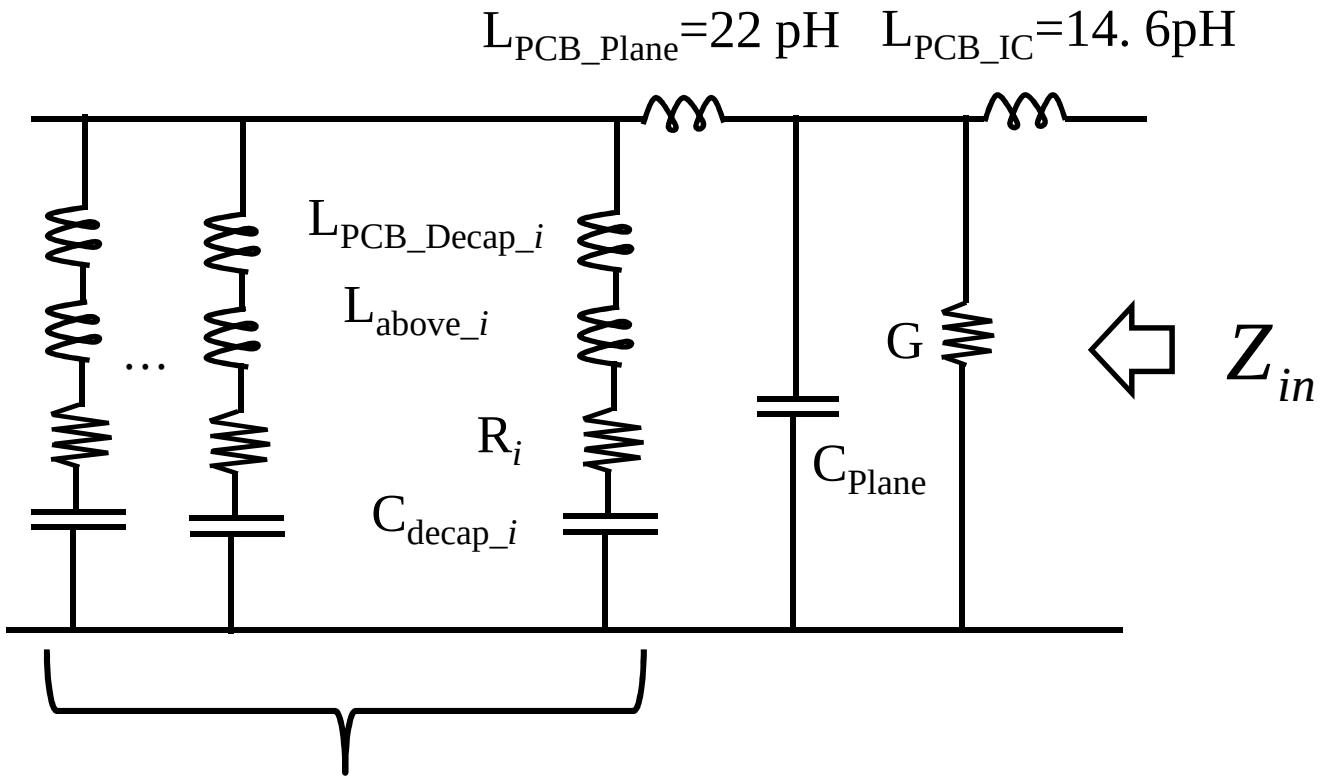
$$L_{Decap\_above\_1pair} = 248\,pH$$



From previous design: n_{ICpin} =32, n_{Decap_Pair} >=16,

Requirement: L_{PCB_Decap} +L_{above} = 22pH+22pH=44pH

Impedance Equivalent Circuit

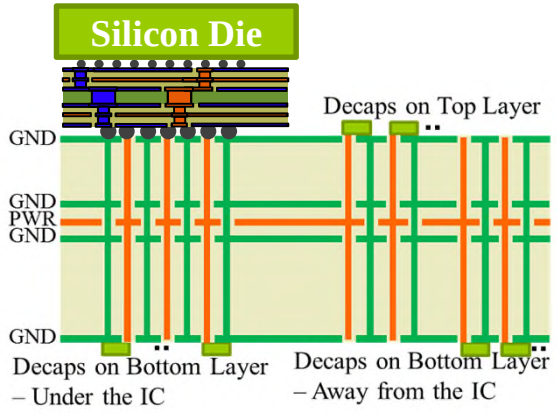


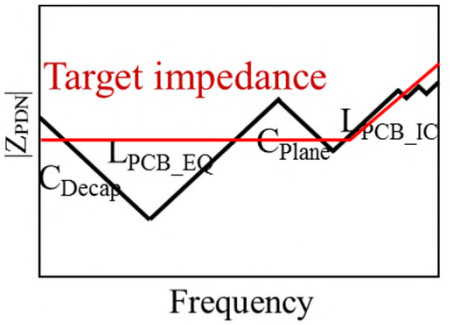
$L_{PCB\_Decap\_i}$=177 pH (pair)

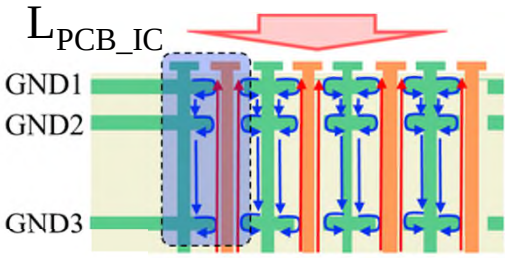
L_{above_i}= 248 pH (pair)

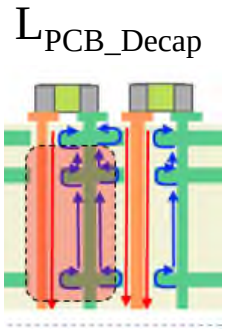
Outline

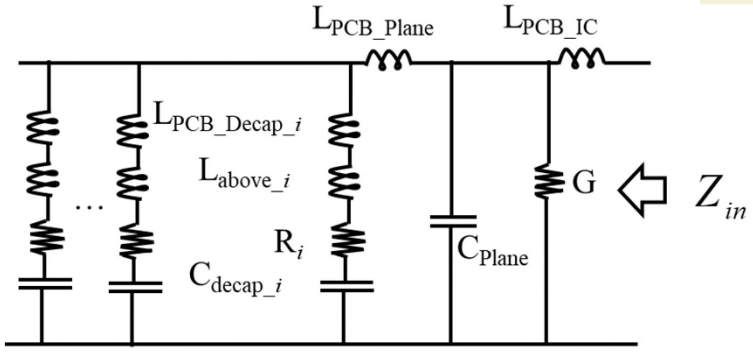
- Problem and concepts
- PDN pre-layout design methodology
- Circuit model and example

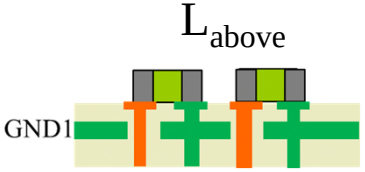




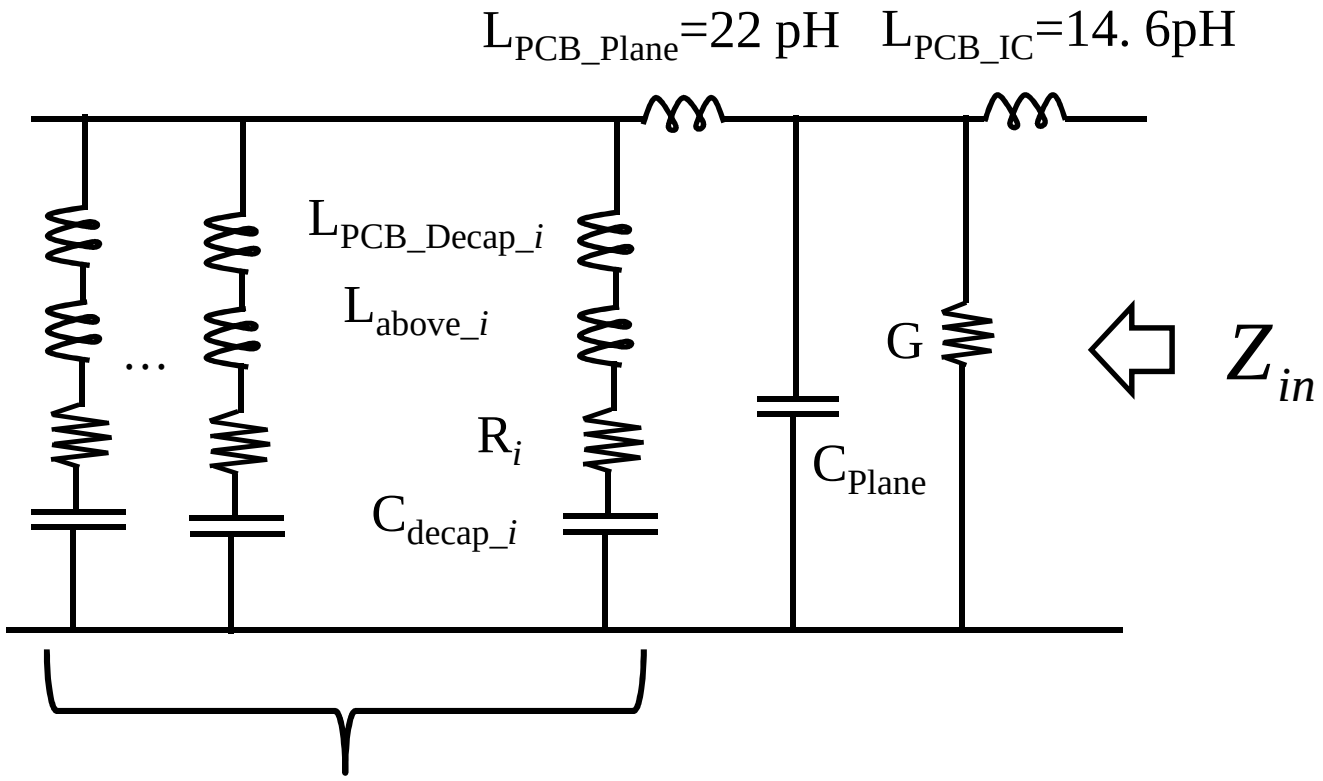








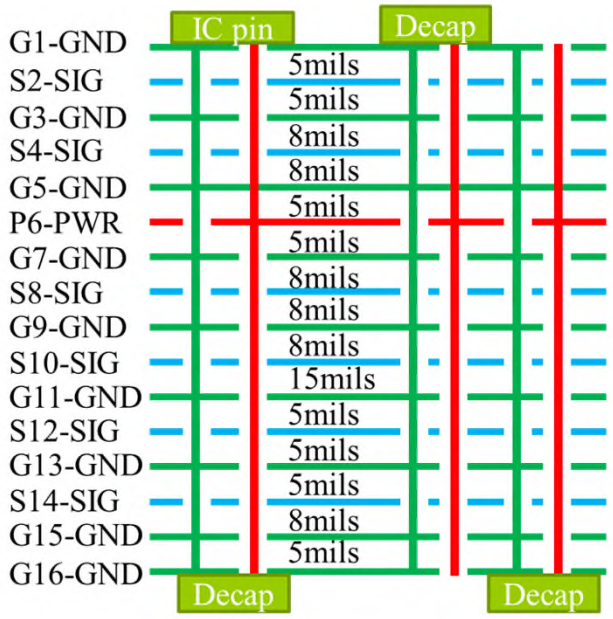
Impedance Equivalent Circuit

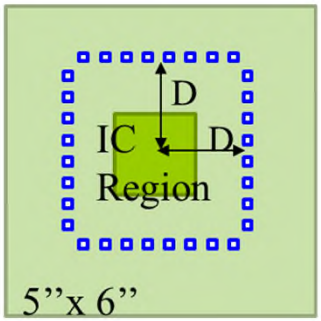


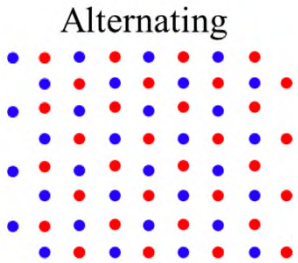
$L_{PCB\_Decap\_i}$=177 pH (pair)

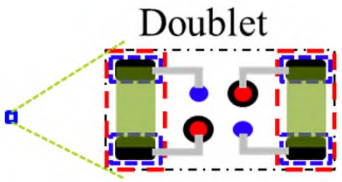
L_{above_i}= 248 pH (pair)

PCB Example







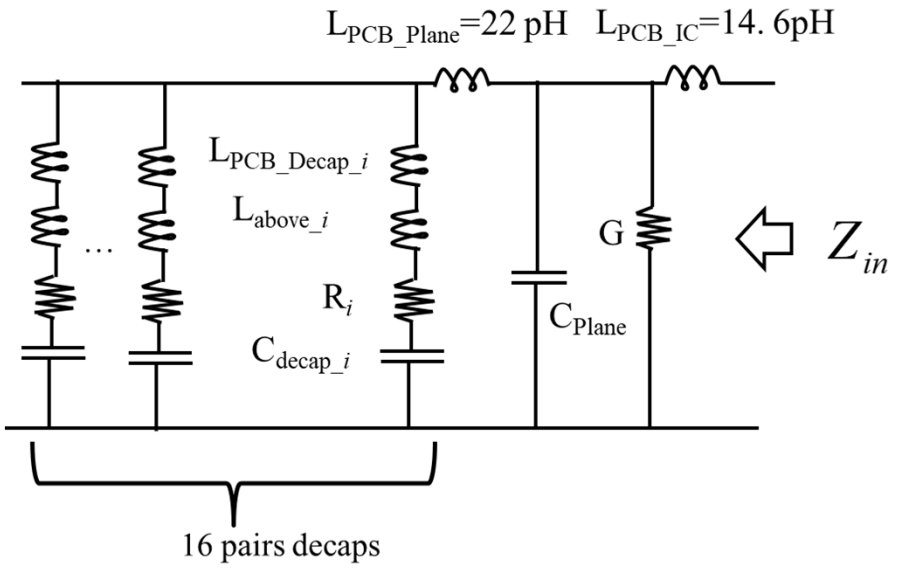


PCB PDN Design:

32 IC pins

D = 500mils

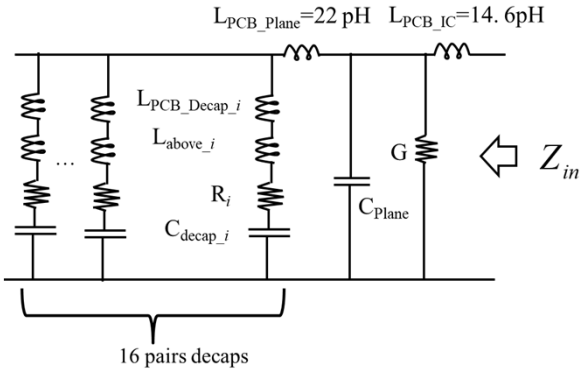
16 pairs of decaps using doublet layout on the top layer



$L_{PCB\_Decap\_i}$=177 pH (pair)

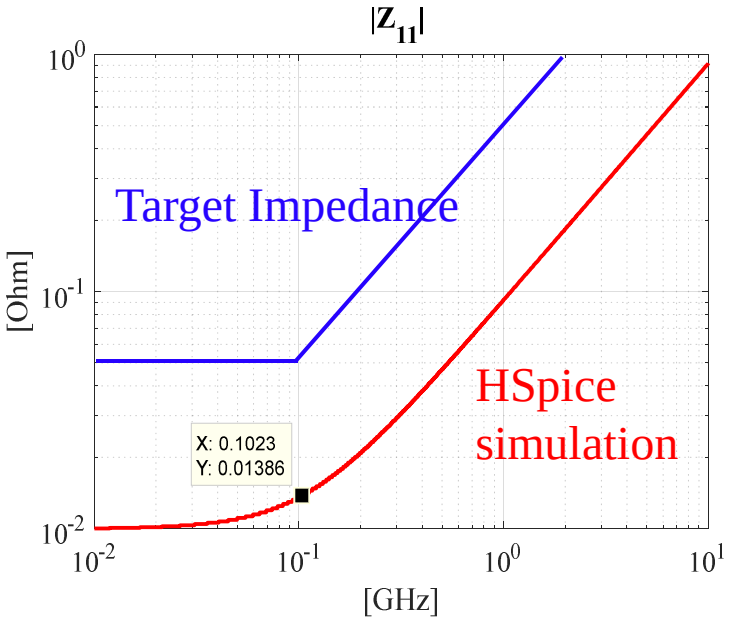
L_{above_i}= 248 pH (pair)

PCB Example Input Impedance



$L_{PCB\_Decap\_i}$=177 pH (pair)
L_{above_i}= 248 pH (pair)

L_{PCB_EQ} = 60pH
L_{PCB_IC} = 14.6pH
For 0805 decap, ESR =30mOhm
For 16 decap pairs, R_{EQ} is around 30mOhm/32 =0.94mOhm.

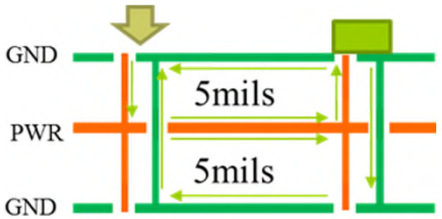


G_{diel} = 0.1S from real board measurement
R_{IC} = 0.01Ohm from real board measurement
Assume the decap is 100nF, C_{Decap} = 3.2uF

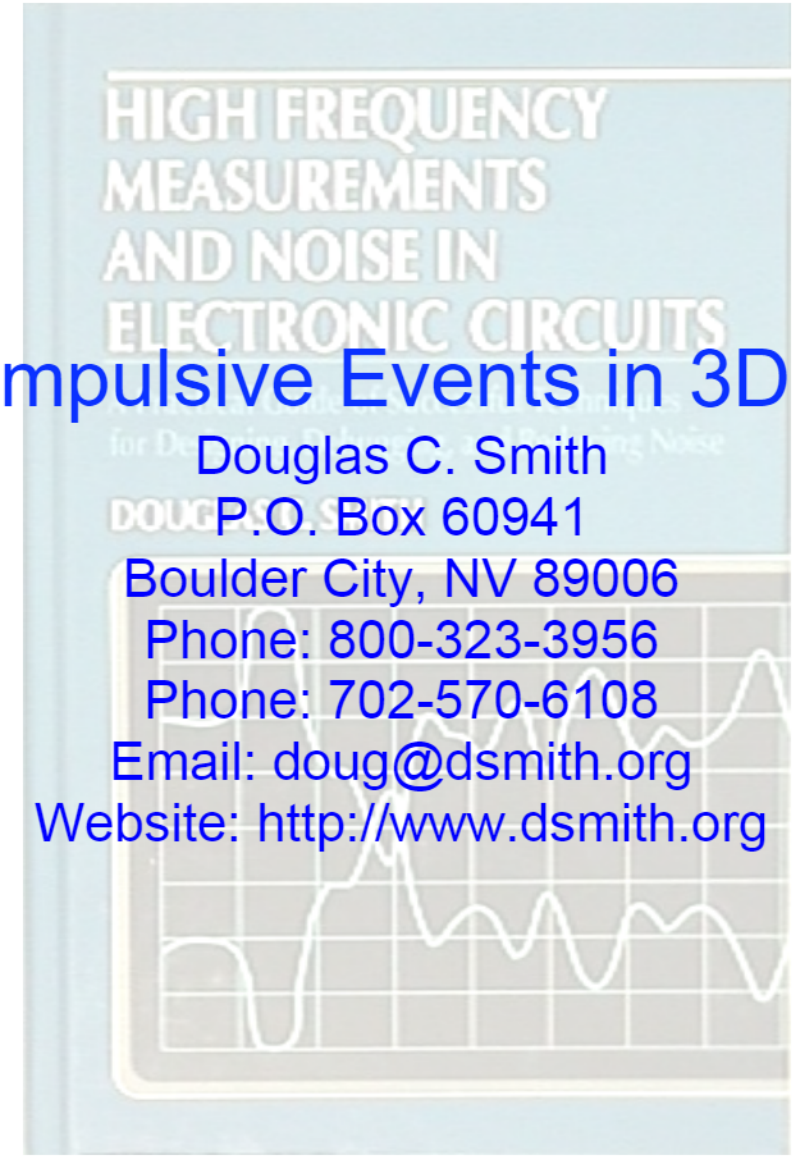
$$C_{Plane\_perCavity} = \frac{\varepsilon A}{d} =$$

$$\frac{8.85\times10^{-12}\times5000\times2.54\times10^{-5}\times6000\times2.54\times10^{-5}}{5\times2.54\times10^{-5}} = 1.35nF$$

C_{Plane} = 2.7 nF



Thank You!



Locating Impulsive Events in 3D Space

Douglas C. Smith
P.O. Box 60941
Boulder City, NV 89006
Phone: 800-323-3956
Phone: 702-570-6108
Email: doug@dsmith.org
Website: http://www.dsmith.org

EXAMPLES OF CHAIRS

Standard Office Chair

ESD Controlling Chair

Phone: 1-800-323-3956, 1-408-356-4186
http://www.dsmith.org doug@dsmith.org

Test Setup to Measure Number of ESD Events

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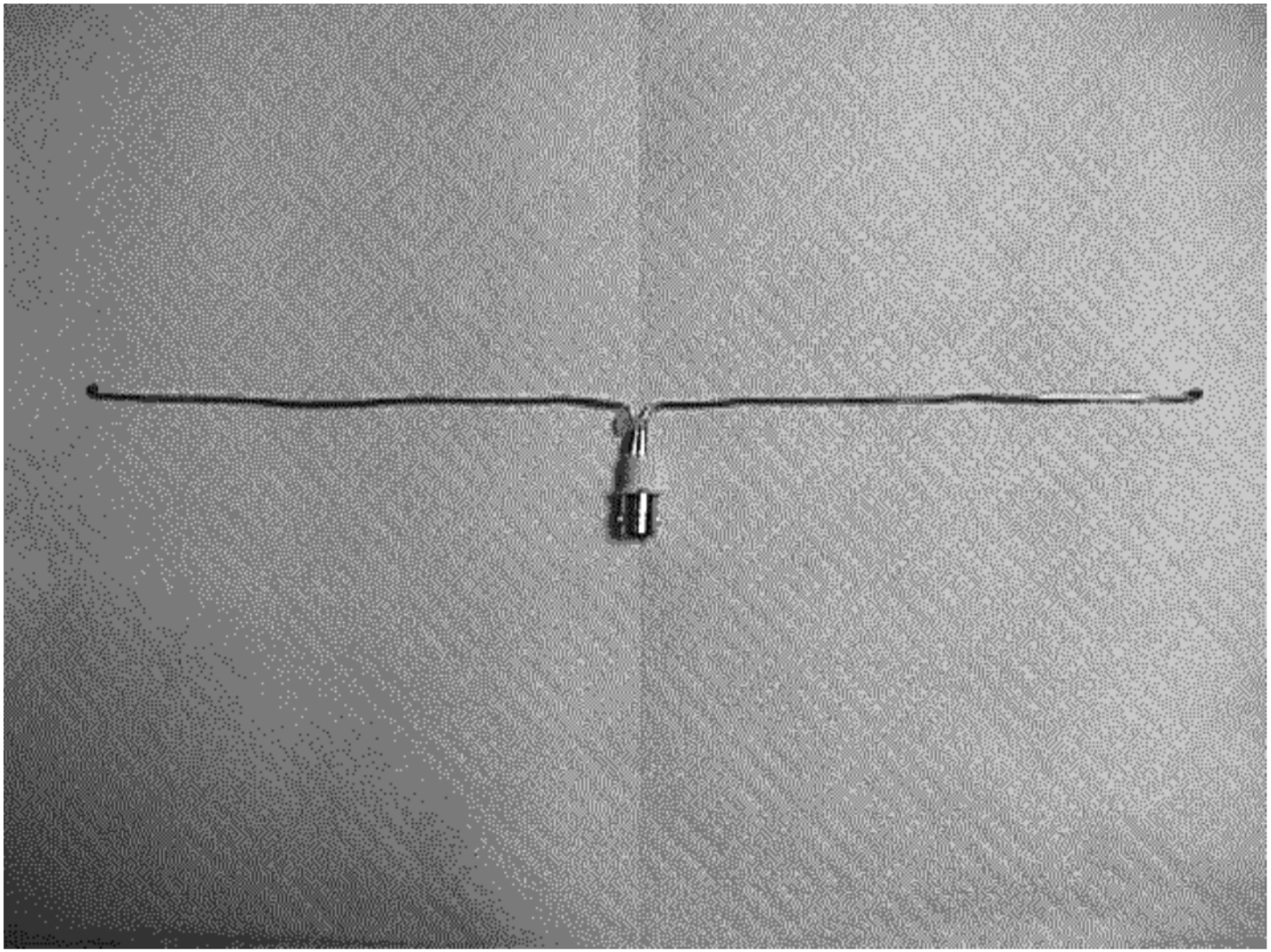
Phone: 1-800-323-3956, 1-408-356-4186
http://www.dsmith.org doug@dsmith.org

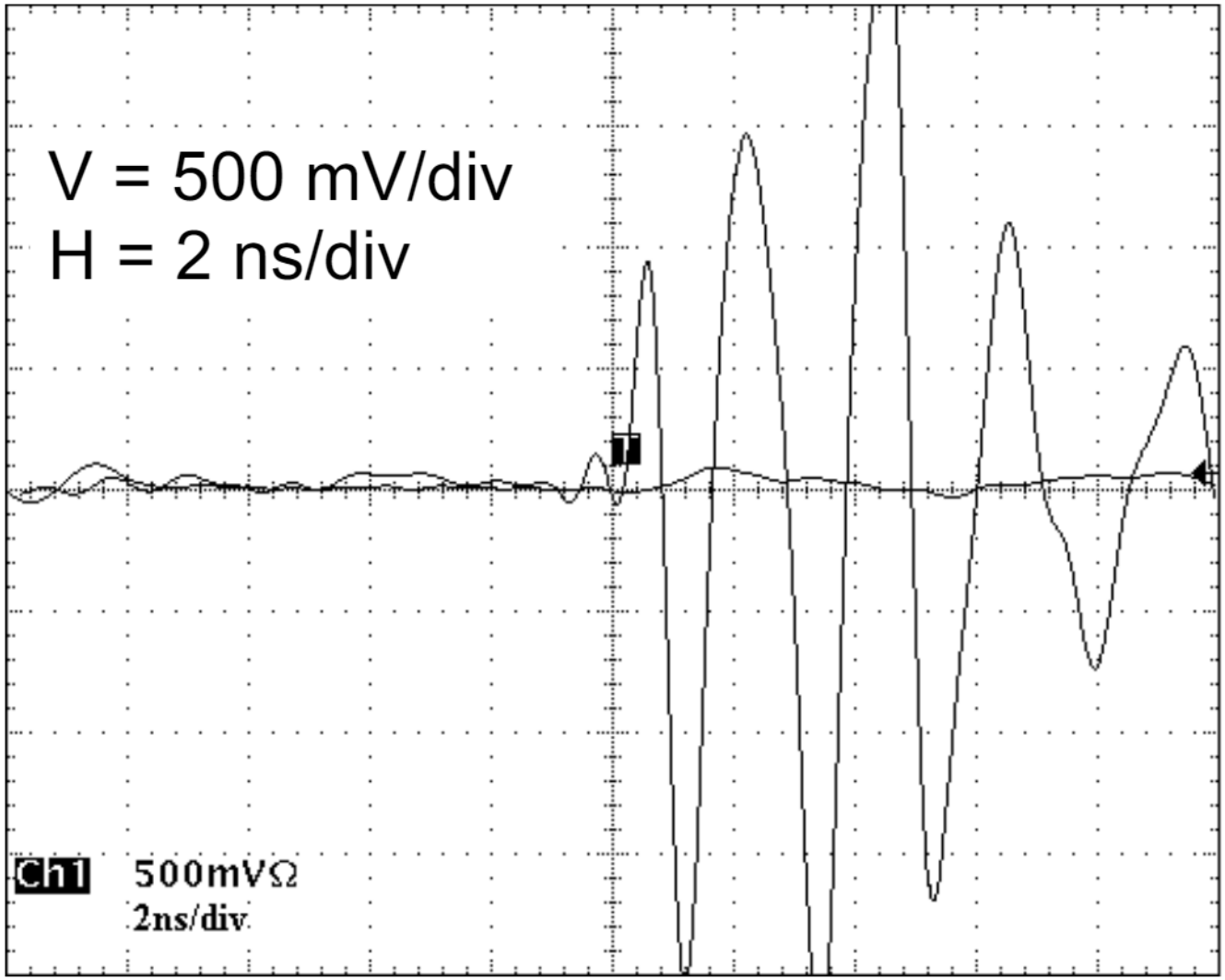
Event Count After Rising From Chair

Phone: 1-800-323-3956, 1-408-356-4186
http://www.dsmith.org doug@dsmith.org



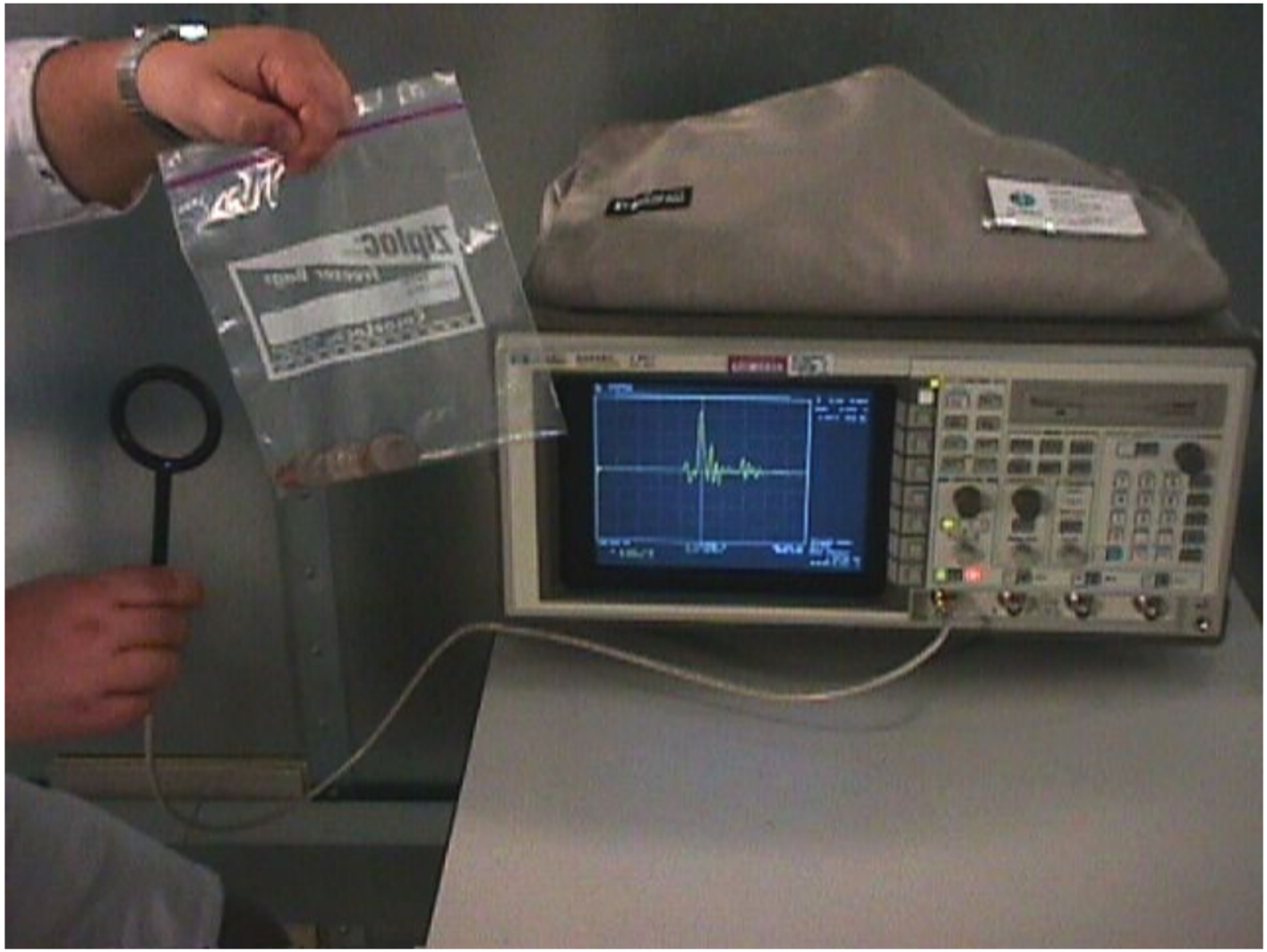
30 Cm Dipole for Receiving Chair ESD Radiation

Phone: 1-800-323-3956, 1-408-356-4186
http://www.dsmith.org doug@dsmith.org

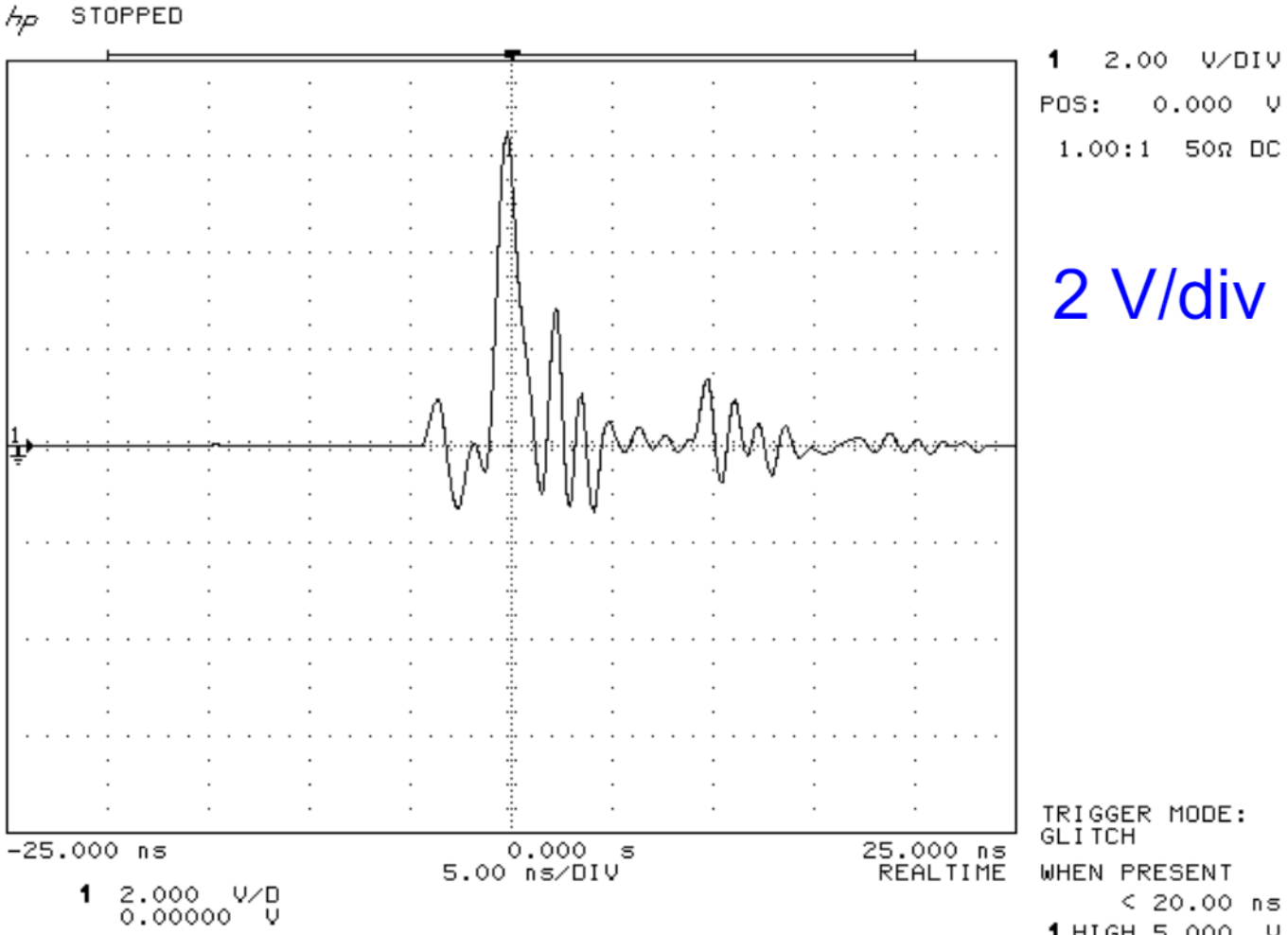


EMI Picked up by a 30 Cm Dipole Near Chair

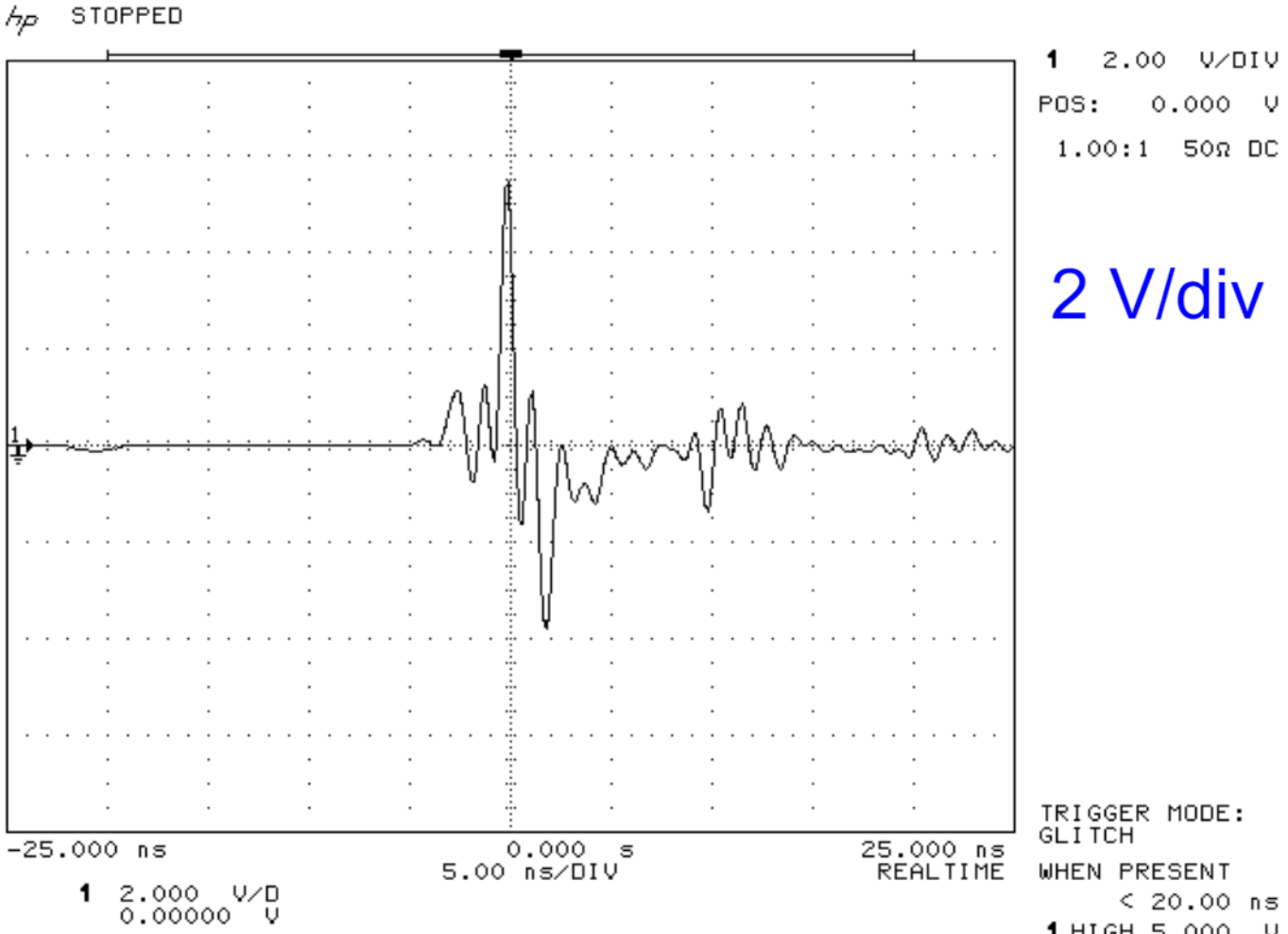
Phone: 1-800-323-3956, 1-408-356-4186
http://www.dsmith.org doug@dsmith.org



Jingling Change Test Setup



Loop Output Caused by Jingling Change: Case 1



Loop Output Caused by Jingling Change: Case 2

Locating Impulsive Events

- Faster circuits ⇒ problems from environment

  Noise sources that have always been around are now causing problems.

- Locating and characterizing noise generating events can dramatically shorten resolution time of problems.

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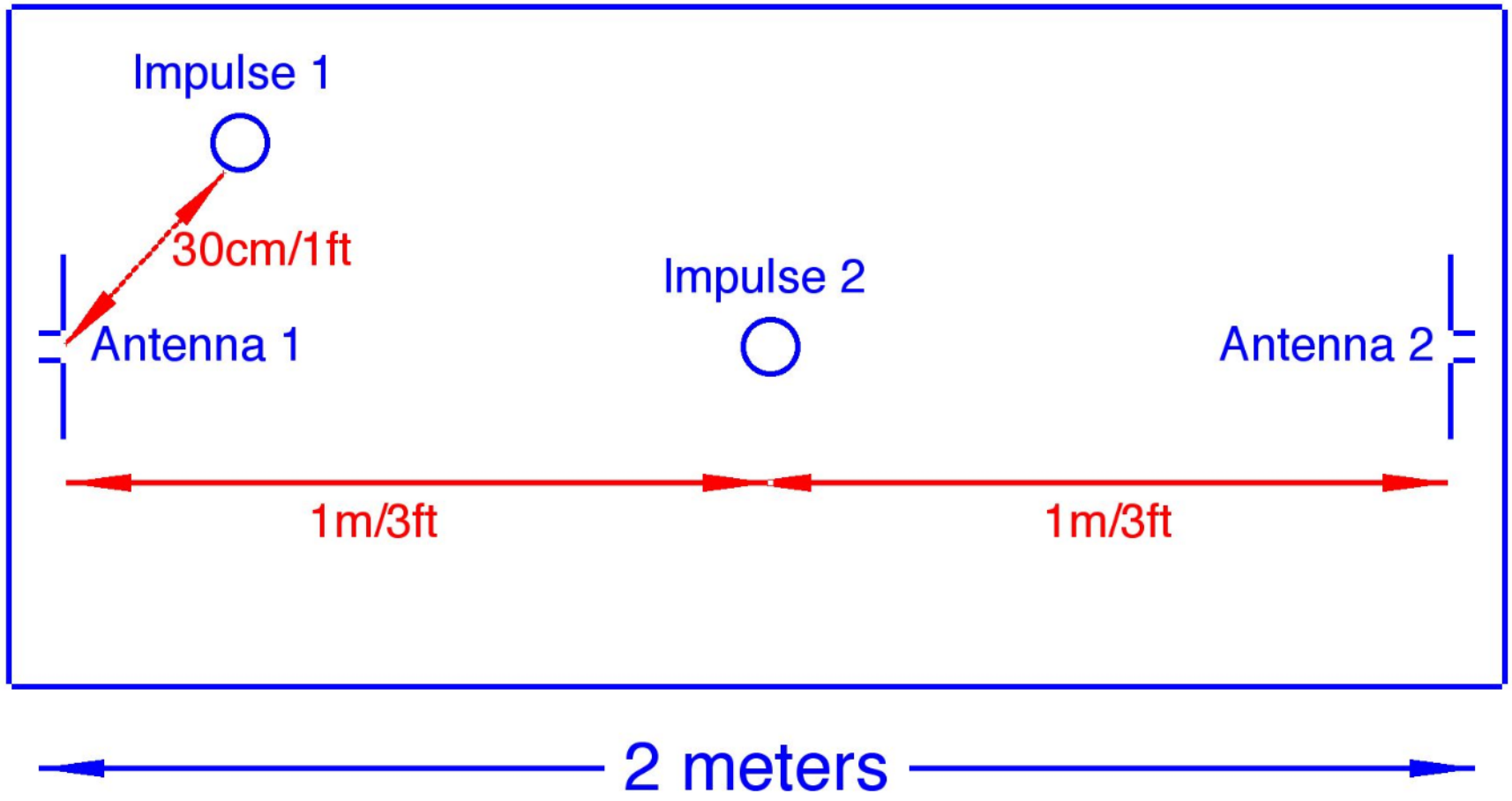
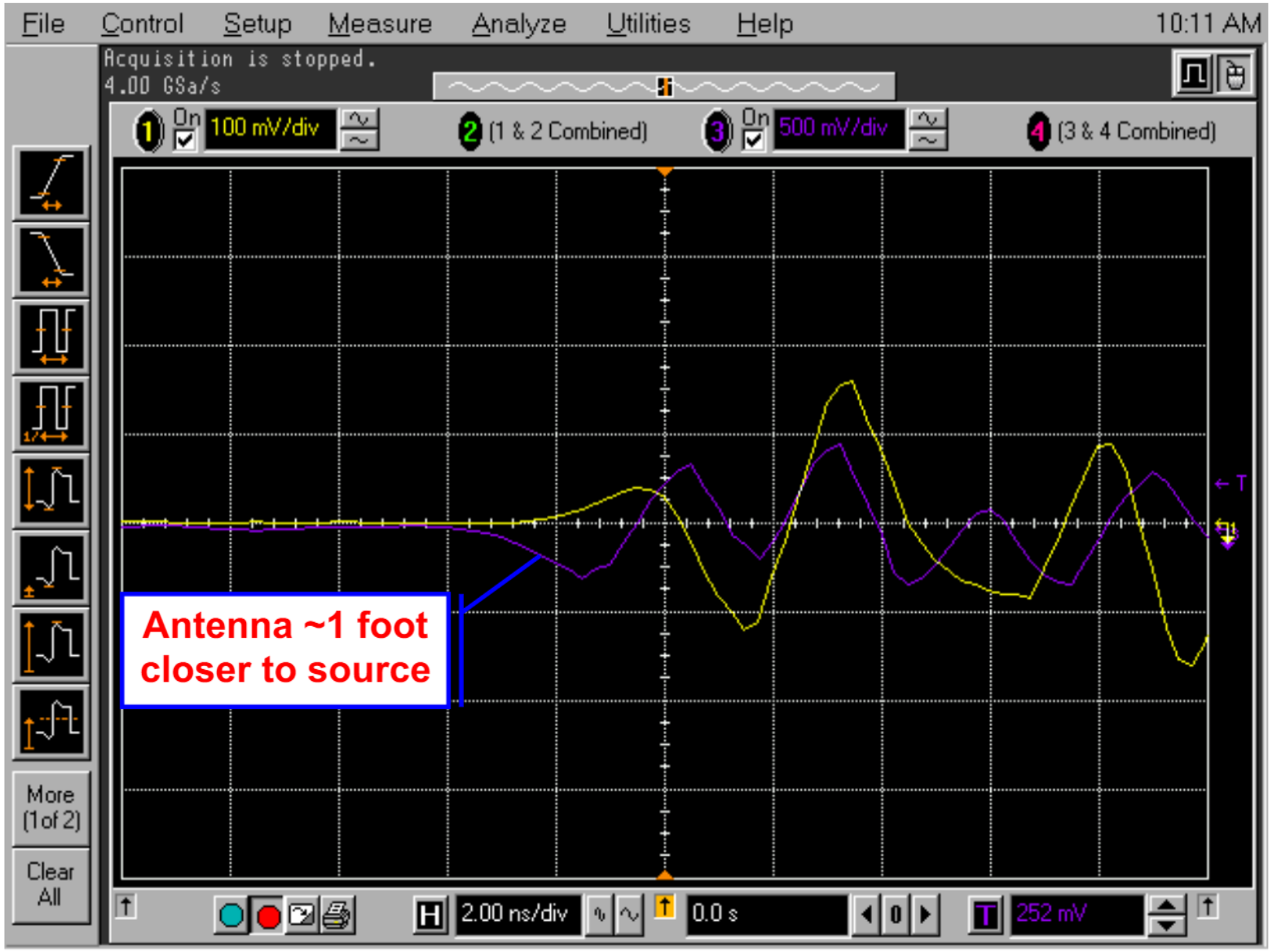
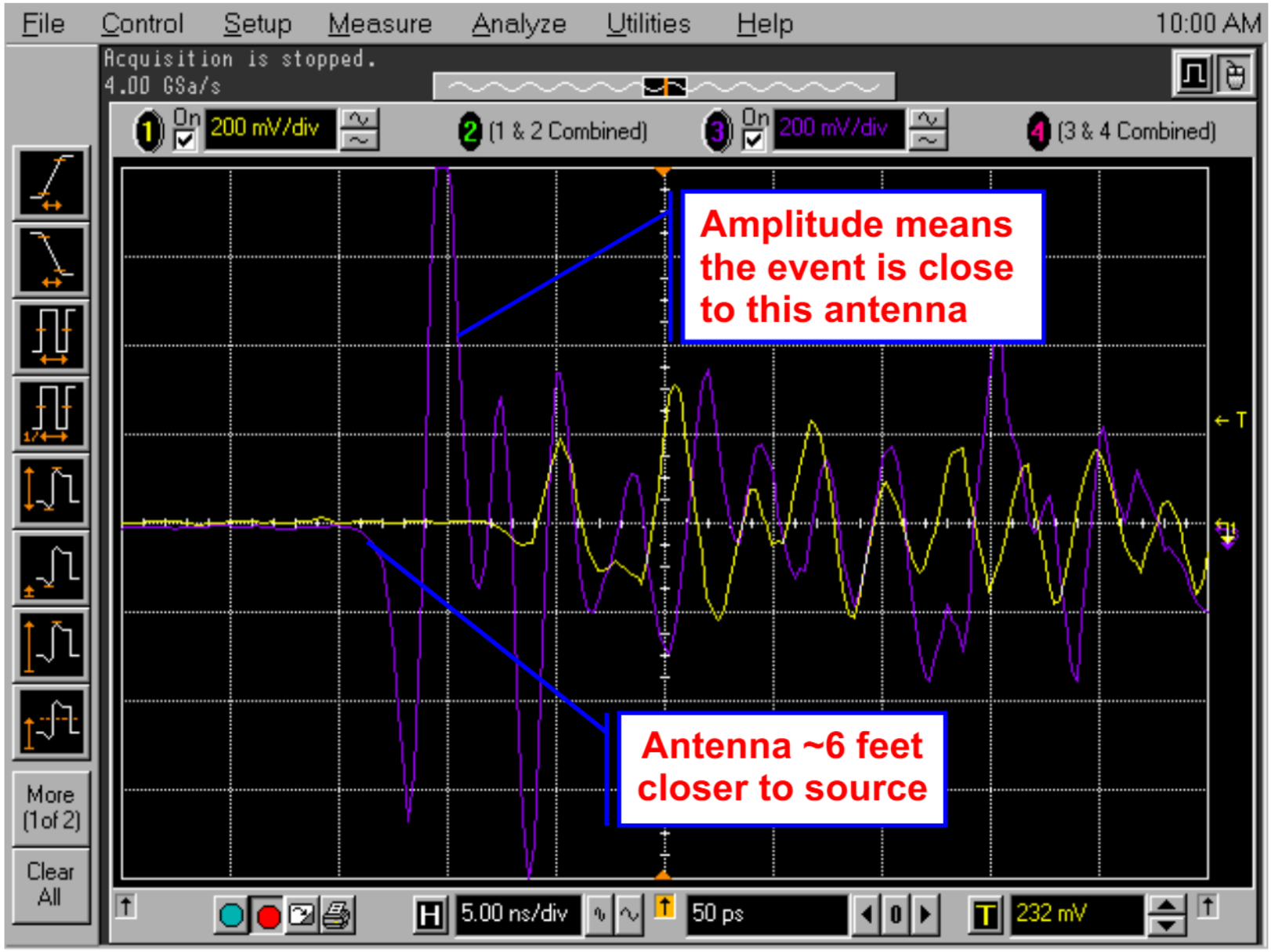
Example of Event Location



Case #1



Case #2



Observations

- Time delay indicates direction or surface of event location
- Relative amplitudes indicate distance from antennas
- Absolute amplitudes combined with above give information on strength of event
- Risetime gives indication of nature of event (low or high voltage)

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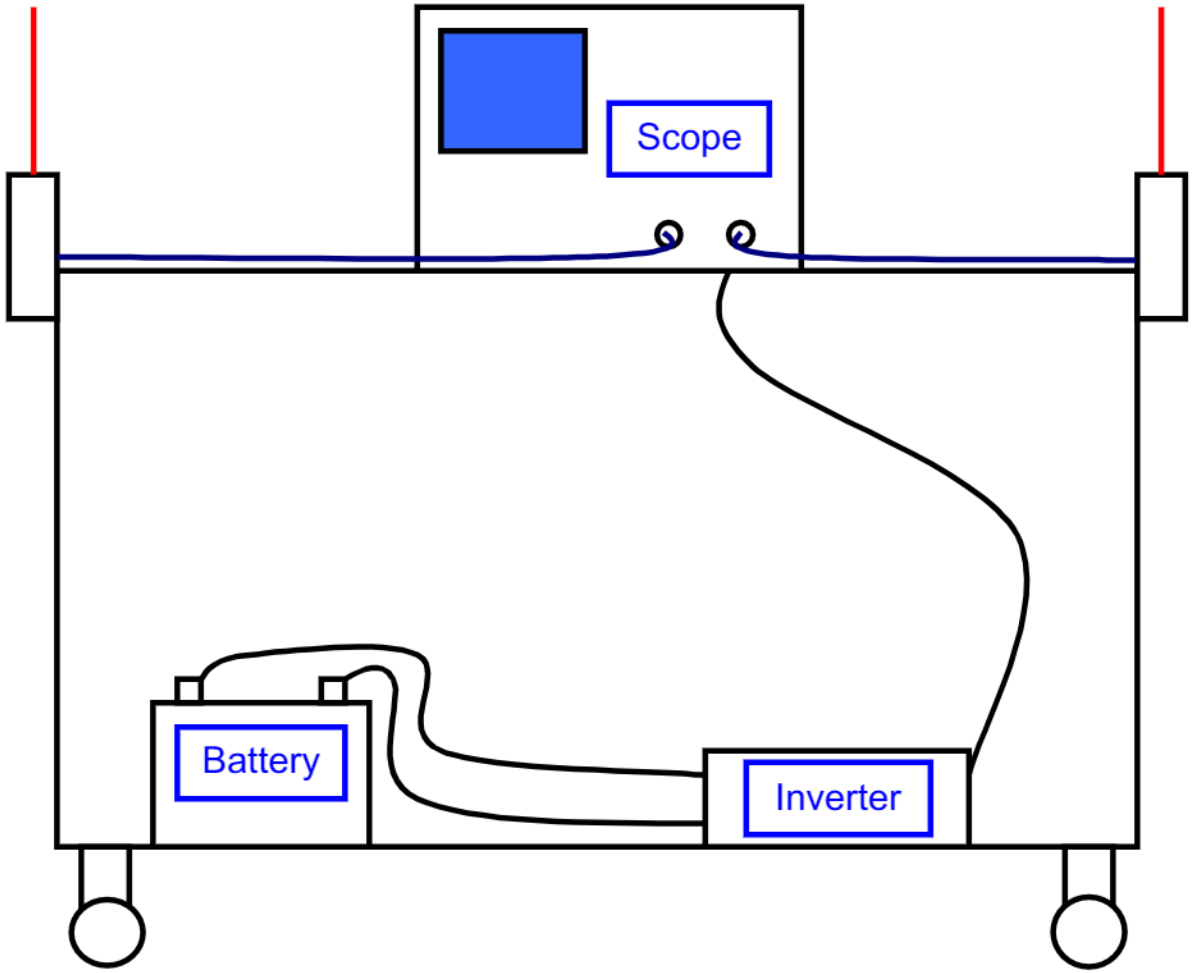
Mobile Event Finder

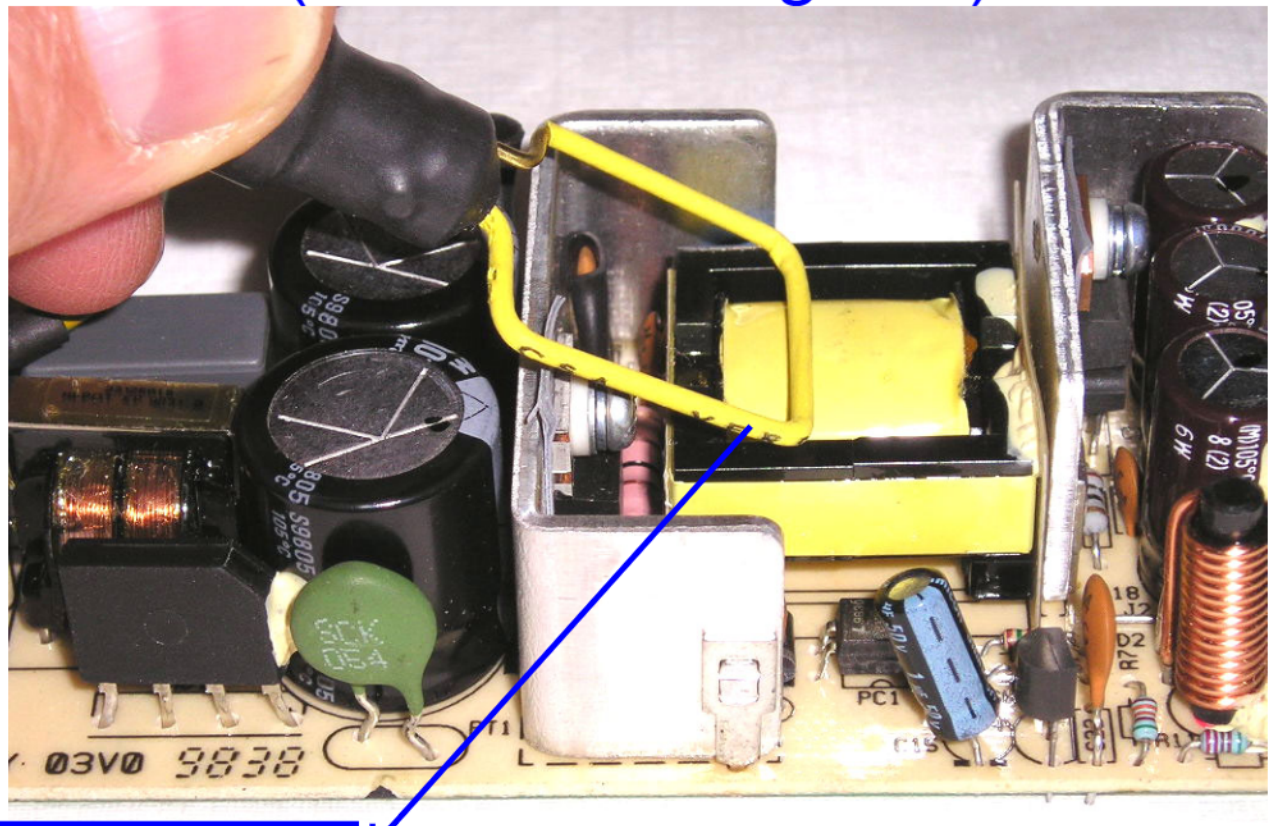


Finding a Noise Source Within a System (continuous signals)

To find the source of noise out of several possibilities, loops can be used to determine time correlation. There are two cases for continuous signals:

- Finding how a known source manifests itself at several locations around a system.
- Observing a noise at one point in a system and finding the source.

Method: Finding Effects of a Source (continuous signals)



Position the loop close to source and trigger scope from the loop.

With the scope triggered by the source of noise, use another loop or voltage probe to find effects of the noise source around the system. The loop is an ideal trigger source since it can pick up a signal without having to connect to the noise source.

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Method: Finding a Source of Noise (continuous signals)

- Trigger the scope from the measured noise at a point in the system by any means (loop, voltage probe, etc.).
- Move a loop around the system to find a source that is correlated in time to the measured noise. A loop is ideal since it can be moved around quickly without need for connection to the circuit.

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Using Loops to Find a Noise Source (pulsed signals)

Using time delays between probes, much like a miniature version of the mobile cart for finding ESD events in a room, a source of noise in a system can be located.

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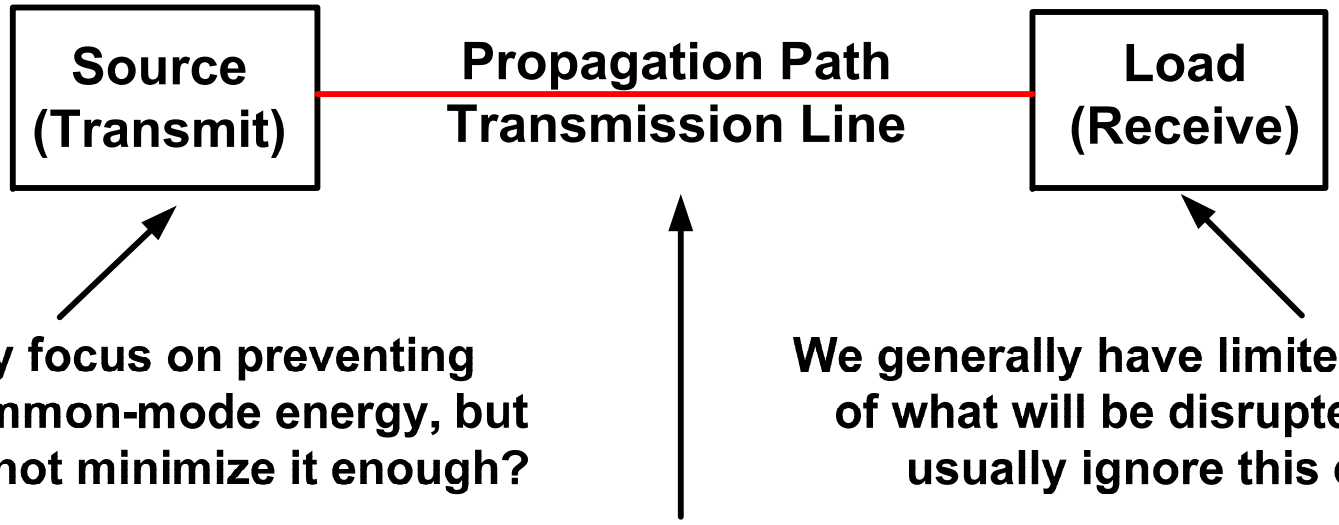
http://www.dsmith.org doug@dsmith.org

Electromagnetics Made Simple
Maxwell Without the Math

Mark Montrose
Principle Consultant
Montrose Compliance Services, Inc.
mark@montrosecompliance.com
www.montrosecompliance.com
(408) 247-5715

Basis of Electrical Engineering



We generally focus on preventing creation of common-mode energy, but what if we cannot minimize it enough?

We generally have limited knowledge of what will be disrupted thus, we usually ignore this element

If we prevent losses in the propagation path, or remove it from the model, we have compliance (EMC Made Simple)

Electromagnetics Made Simple

Using Simple Algebra

Maxwell Made Simple®

Maxwell's four equations describe the relationship of electric and magnetic fields, derived from Ampere's Law, Faraday's Law, and two from Gauss.

To overly simplify Maxwell, ***conceptually*** use ***Ohms law*** to convert frequency domain aspects of Maxwell's equations into the time domain.

Ohms Law (Time domain - DC currents)

$$V = I\,R$$

Maxwell's Equations (Frequency domain - AC currents)

$$V_{rf} = I_{rf}\,Z$$

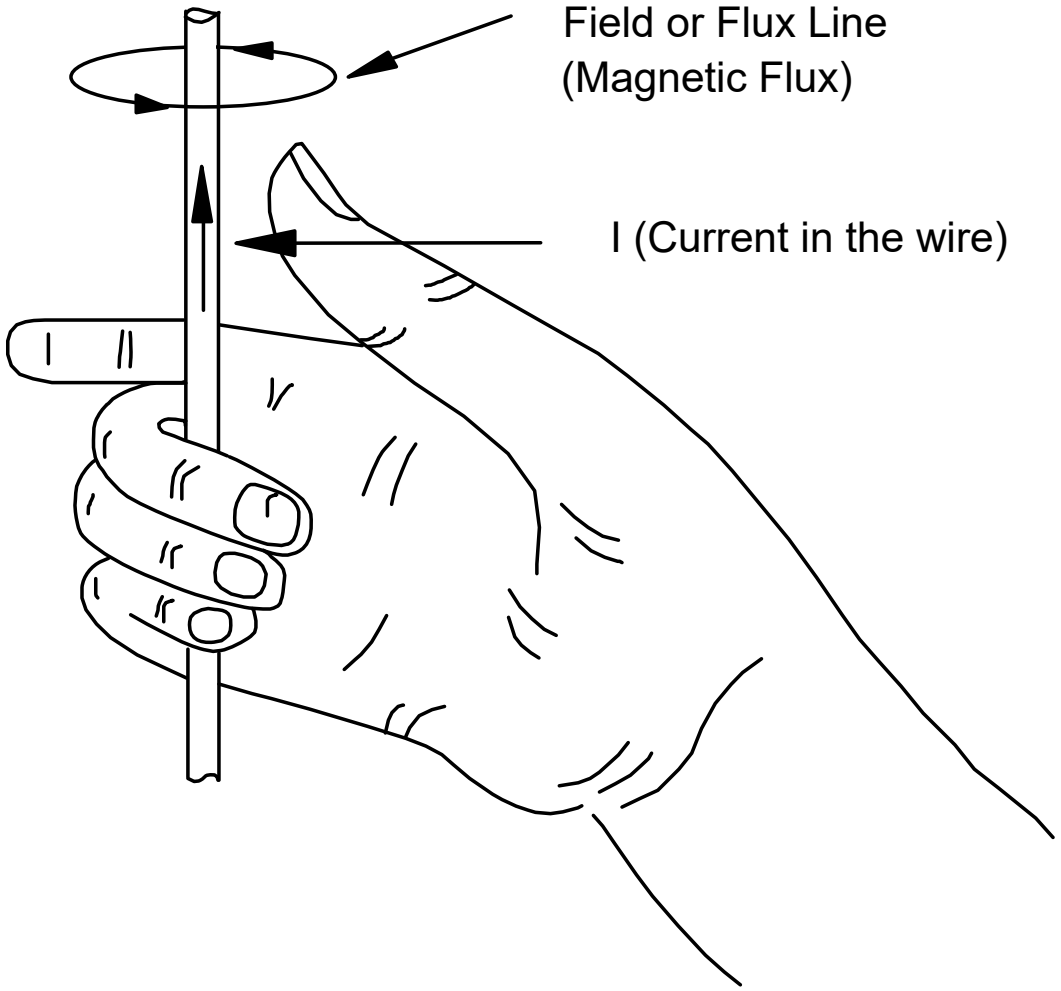
$$Z = R + j|X|$$

where

$$X_L = 2\,\pi f\,L$$

$$X_c = 1/(2\pi f\,C)$$

Right Hand Rule
(Faraday's Law)



Where is the electric field? In the direction of current flow.
Only the magnetic field is shown as a flux line.

Maxwell's Equations - Simplified

(For Reference Purposes)

First Law : Electric Flux (from Gauss)

$$\nabla \bullet \mathrm{D} = \rho \qquad \varphi_e = \oint_s \mathrm{D} \bullet ds = \int_v \rho \, dv = 0$$

The math that explains how a Faraday shield works for electric fields, simplified.

Second Law : Magnetic Flux (from Gauss)

$$\nabla \bullet B = 0 \qquad \varphi_m = \oint_s \mathrm{B} \bullet ds = 0$$

The math that explains how a Faraday shield works for magnetic fields, simplified.

Third Law : Electric Potential (from Faraday)

$$\nabla \times \mathrm{E} = -\frac{\partial \mathrm{B}}{\partial t} \qquad \oint \mathrm{E} \bullet dl = -\int_s \frac{\partial \mathrm{B}}{\partial t} \bullet ds$$

Time varying current in a transmission line creates time varying magnetic flux, which in turn creates an electric field, the combination of which creates an electromagnetic field.

Fourth Law : Electric Current (from Ampere)

$$\nabla \times \mathrm{H} = \mathrm{J} + \frac{\partial \mathrm{D}}{\partial t} \qquad \oint \mathrm{H} \bullet dl = \int_s \left(J + \frac{\partial \mathrm{D}}{\partial t} \right) \bullet ds = I_{total}$$

Current must flow in a loop, simplified.

DO NOT WORRY ABOUT SOLVING CALCULUS EQUATIONS

UNDERSTAND WHAT THE EQUATIONS TELL US!

Electric and Magnetic Field Impedance

A plane wave is a combination of both electric and magnetic field components (Poynting vector). Fields propagate from a field source near the velocity of light.

$$c = 1/\sqrt{\mu_o \varepsilon_o} = 3 \times 10^8$$

where $\mu_o = 4\pi * 10^{-7}$ H/m

$\varepsilon_o = 8.85 * 10^{-12}$ F/m

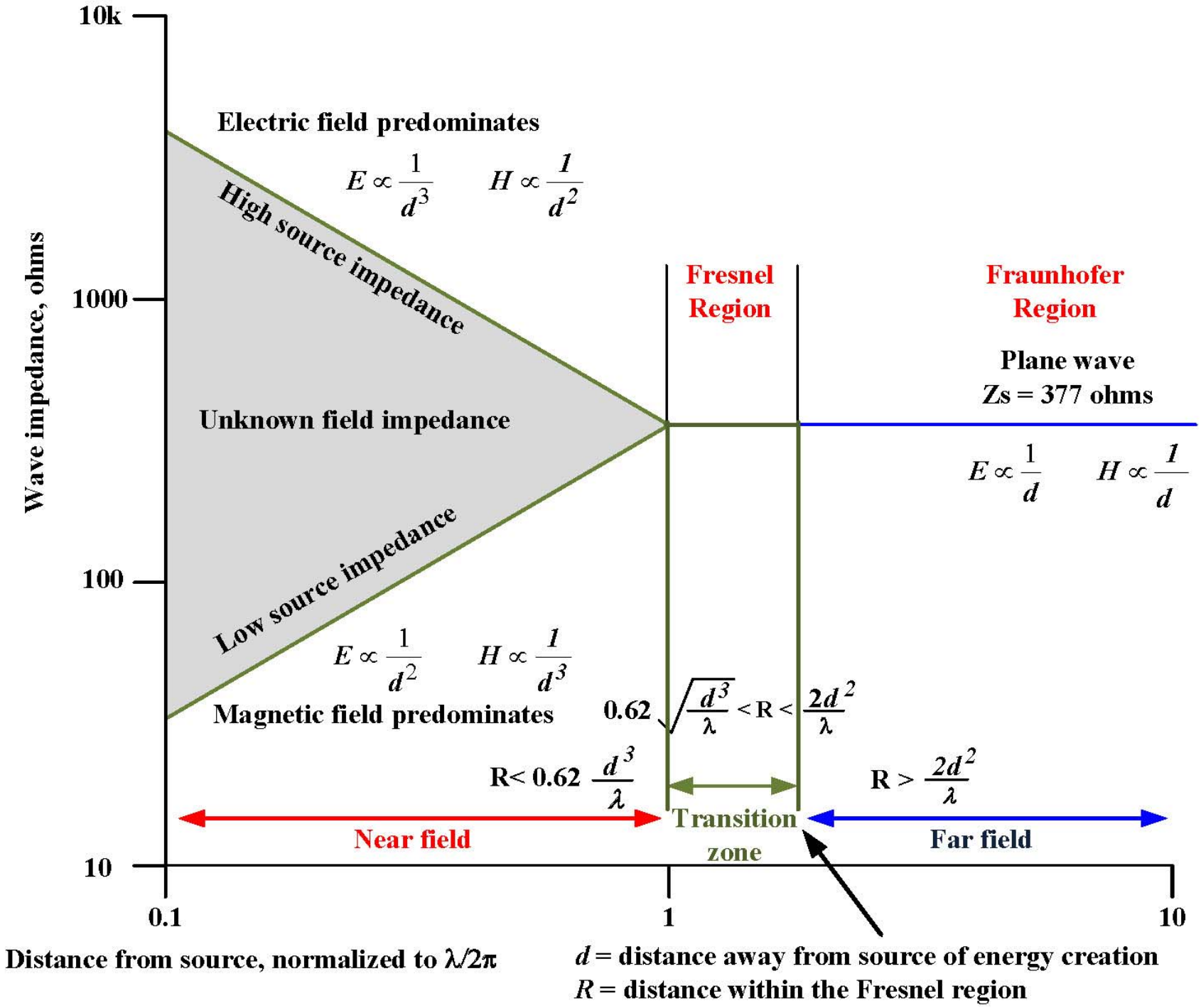
Electric field component is measured in volts/meter *(Note-voltage)*
Magnetic field component is in amps/meter *(Note-current)*

The ratio of both electric field (***E***) to magnetic field (***H***) is identified as the "impedance" of free space. This impedance ratio is described by:

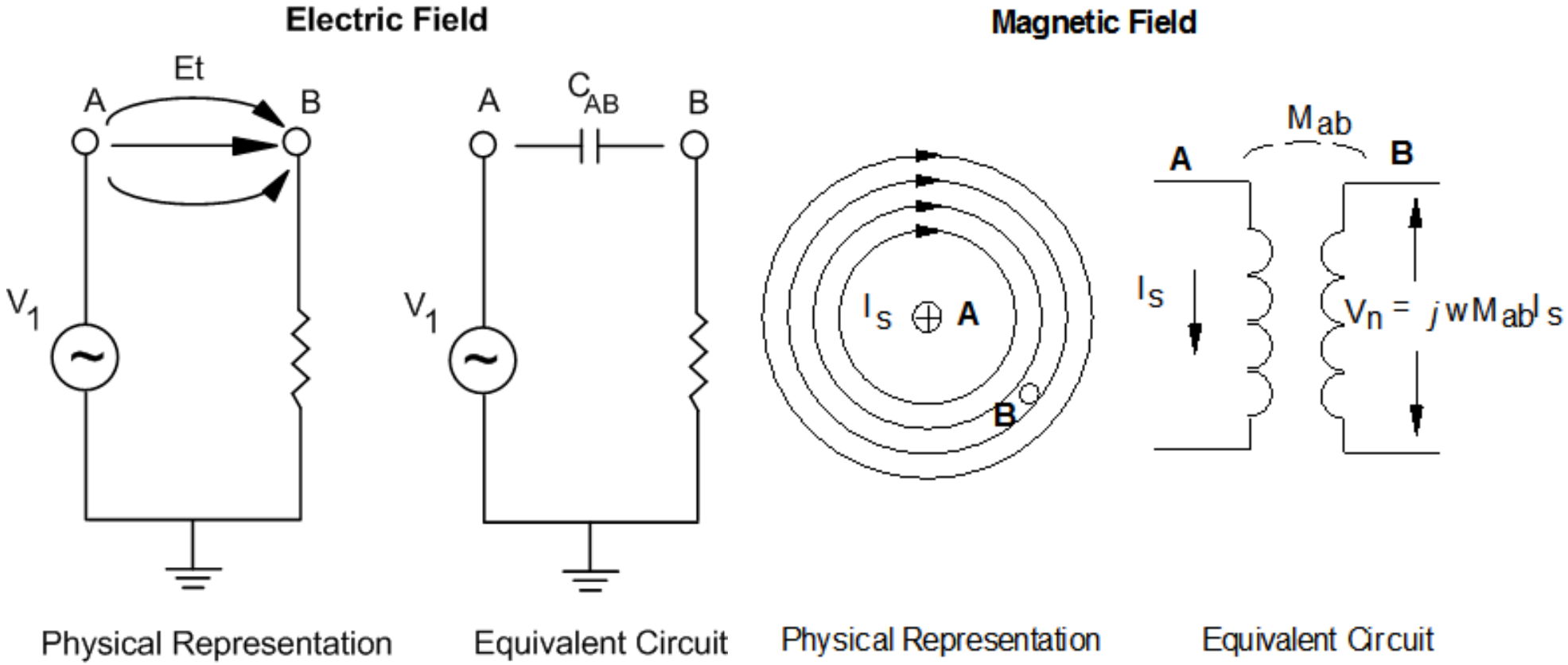
$$Z_o = E \times H = \sqrt{\mu_o / \varepsilon_o} = 377 \text{ ohms}$$

Energy carried in the wave front is measured in Watts/meter^2 (Note-power)

Ohms Law Applied to Field Propagation: P=VI



Magnetic and Electric Field Representation

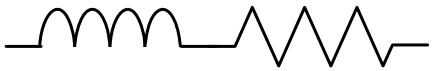
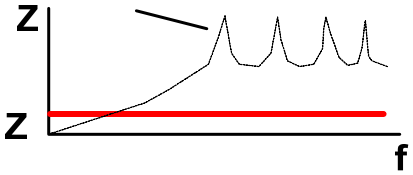
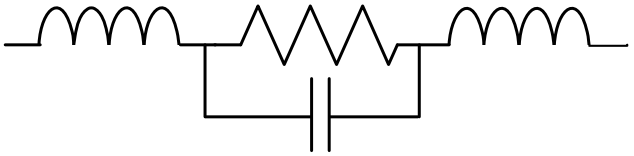
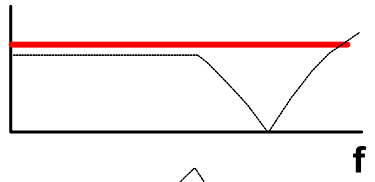
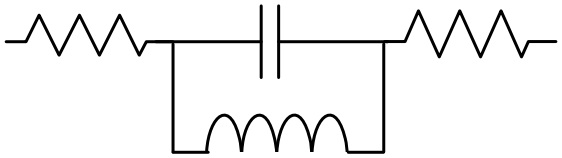
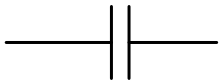
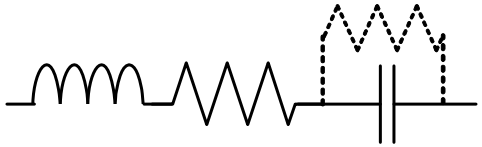
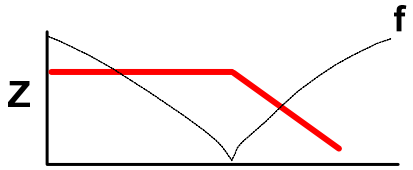
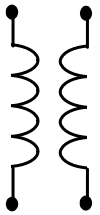
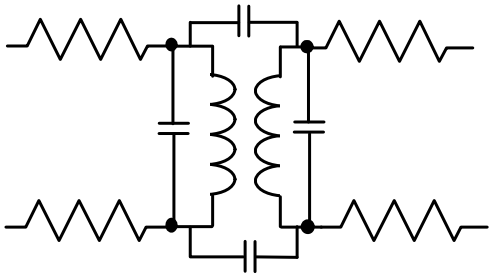
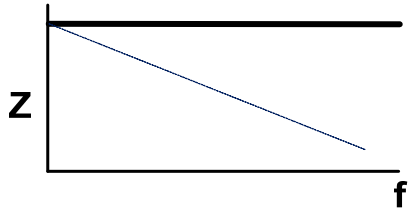


Dipole Antenna Configuration

Loop Antenna Configuration

Component Characteristics at RF Frequencies

(The Hidden Schematic)

COMPONENT	LOW FREQUENCY BEHAVIOR	HIGH FREQUENCY BEHAVIOR (Lumped version)	RESPONSE
WIRE			resonance wavelength at high frequencies 
RESISTOR			
INDUCTOR			
CAPACITOR			
TRANSFORMER			

Response curves

Solid line is low frequency behavior

Solid line is high frequency behavior

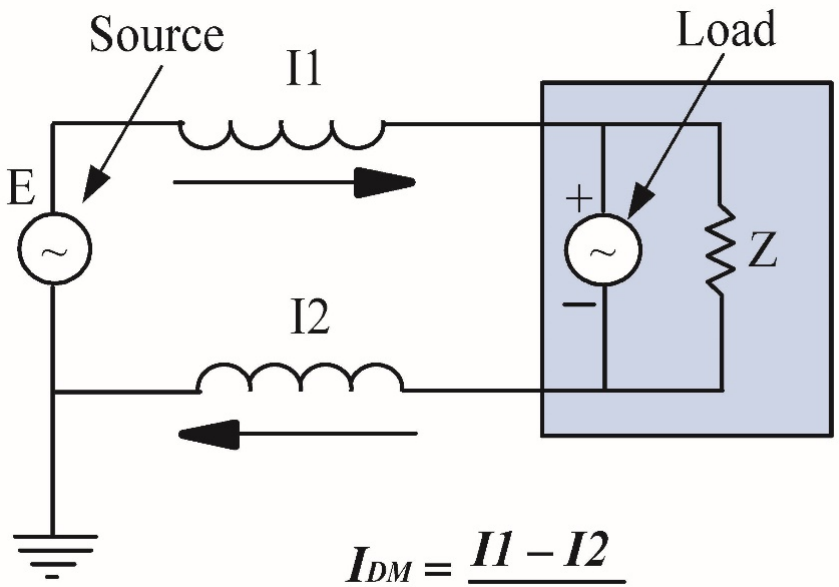
Common-Mode and Differential-Mode Currents in Transmission Lines

Differential-mode

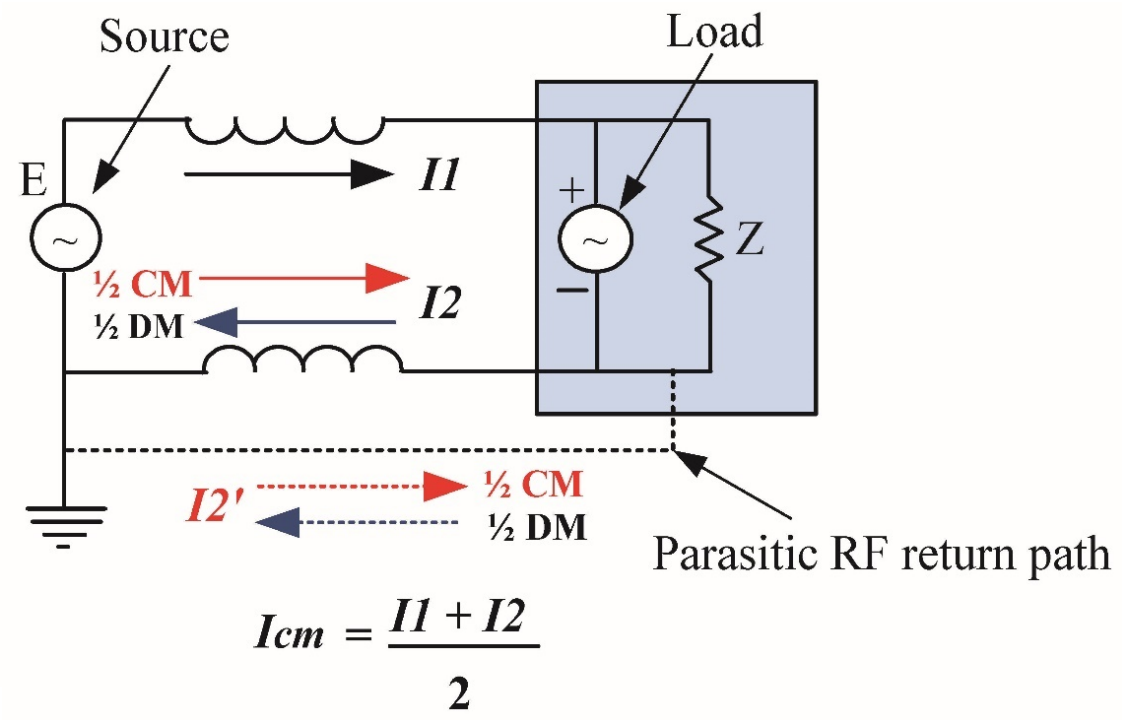
1. Conveys desired information.
2. Does not cause interference. Fields generated oppose each other and cancel.

Common-mode

1. The major source of cable radiation.
2. Contains no useful information.
3. Has no useful purpose.
4. Causes a system (traces, cables, etc.) to radiate.



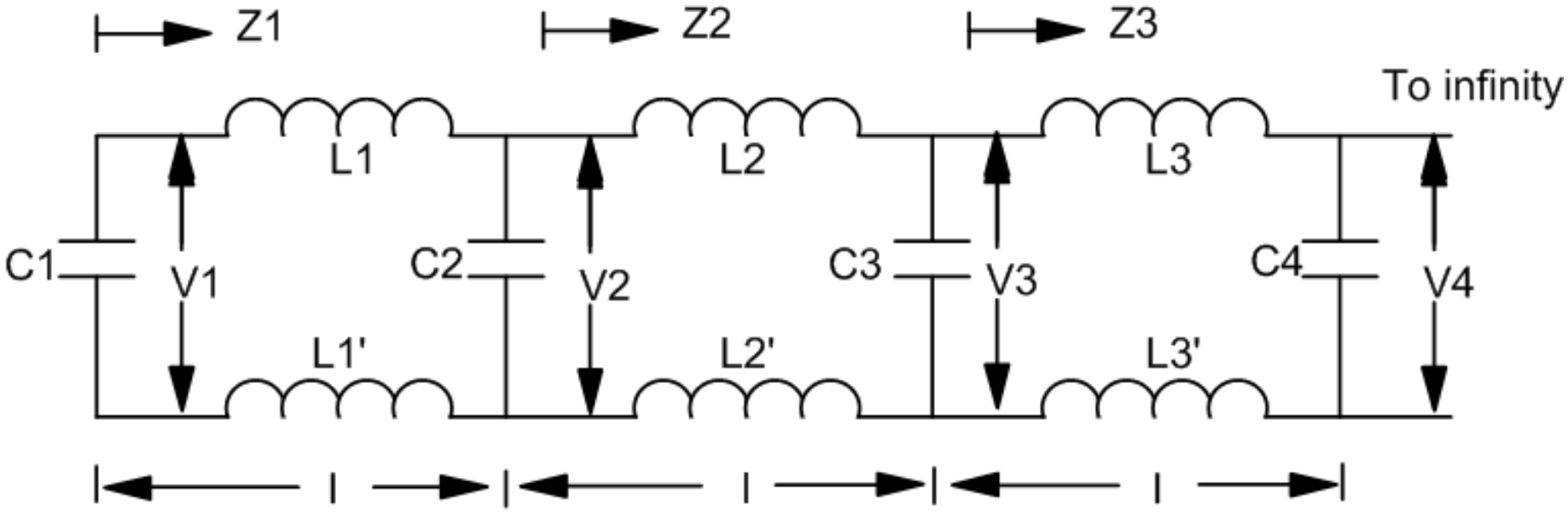
$$I_{DM} = \frac{I1 - I2}{2}$$



$$Icm = \frac{I1 + I2}{2}$$

Transmission Line Theory Made Simple

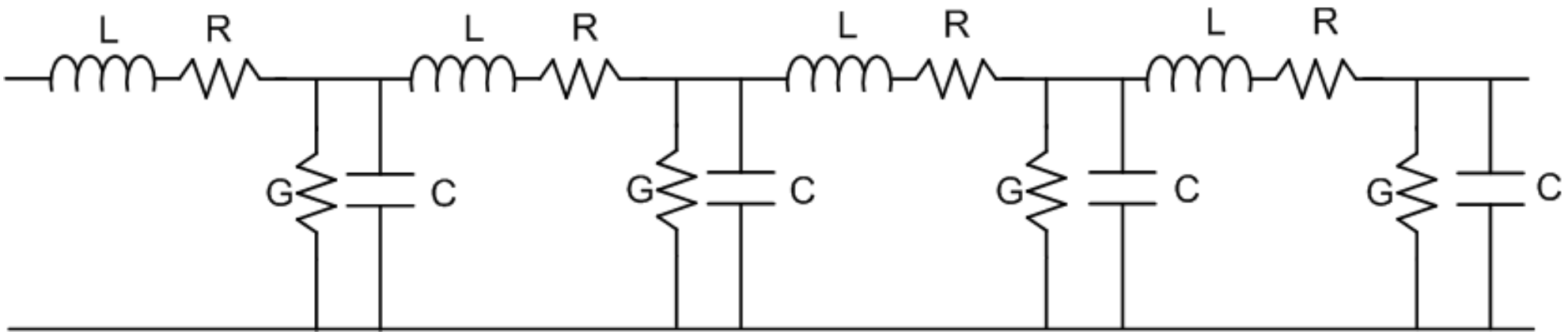
Lossless Transmission Line Equivalent Circuit Within a PCB



$$Z_o = \sqrt{\frac{L_o}{C_o}} = \frac{V(x)}{I(x)}$$

$$t_{pd} = \sqrt{L_{total} C_{total}}$$

Lossy Transmission Line Equivalent Circuit Within a PCB



$$V(\omega, x) = Vo\ \exp(-\Gamma x)\ \exp(jt)$$

$$\Gamma = \alpha + j\beta = \sqrt{(RL + j\omega LL) + (GL + j\omega CL)}$$

$$Zo = \sqrt{\frac{(RL + j\omega LL)}{(GL + j\omega CL)}}$$

$Zo =$ *characteristic impedance*

$L =$ *line length*

RL, GL *may vary with frequency*

Lossy Transmission Lines

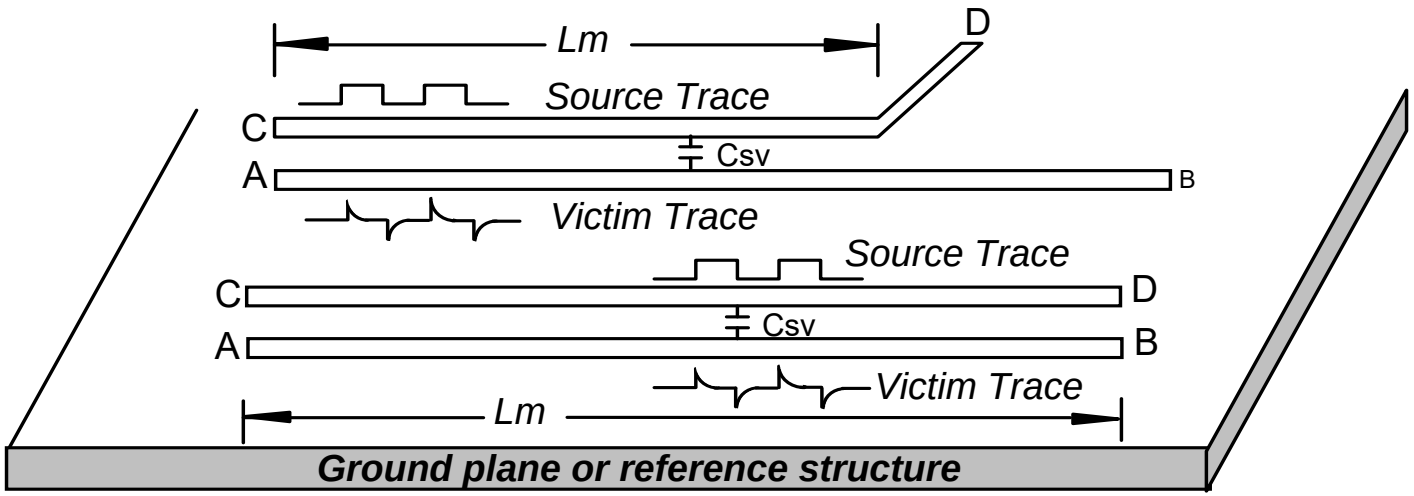
1. **Resistive losses.** Constant with frequency. Ideal resistors have a constant value with frequency. Attenuation, usually measured in dB/unit distance is proportional to the resistance per unit length of the conductor.

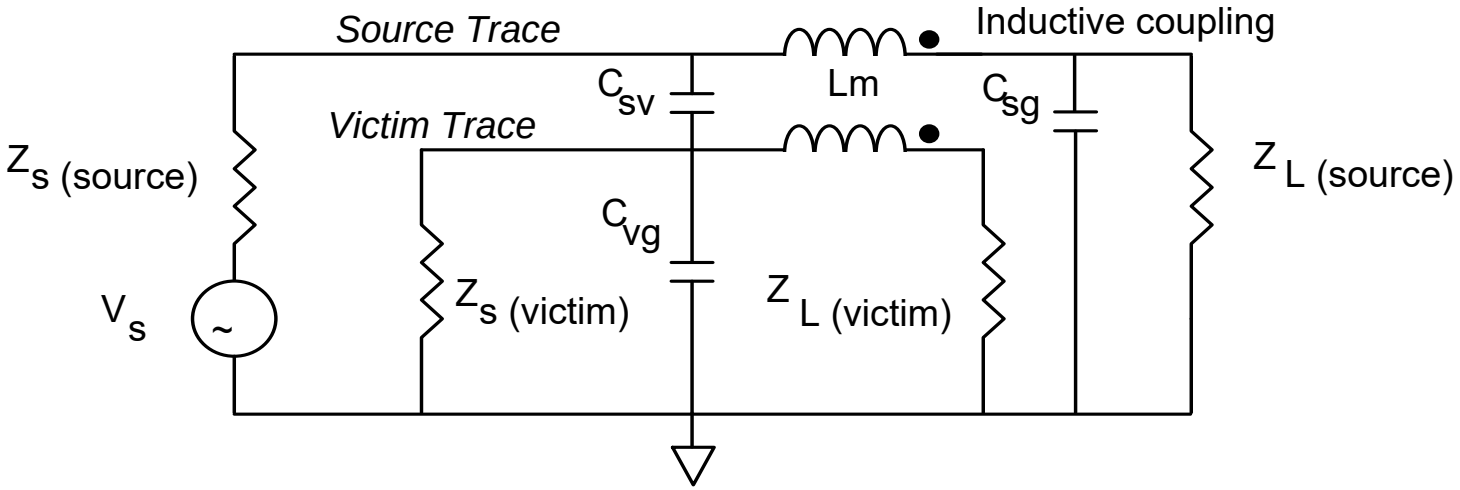
2. **Skin effect losses.** Proportional to the square root of frequency. As the signal frequency increases, current flow retreats to the surface of the conductor flowing in a "skin" which becomes thinner with increasing frequency.

3. **Dielectric losses.** The PCB material (core and prepreg) absorbs some of the electric field energy, which is directly proportional to frequency. A high dissipation factor material means it will absorb a lot of propagating electromagnetic energy.

4. **Resonances.** Typically caused by improperly terminated traces and split planes in addition to the lumped magnitude of both capacitance and inductance within power distribution networks.

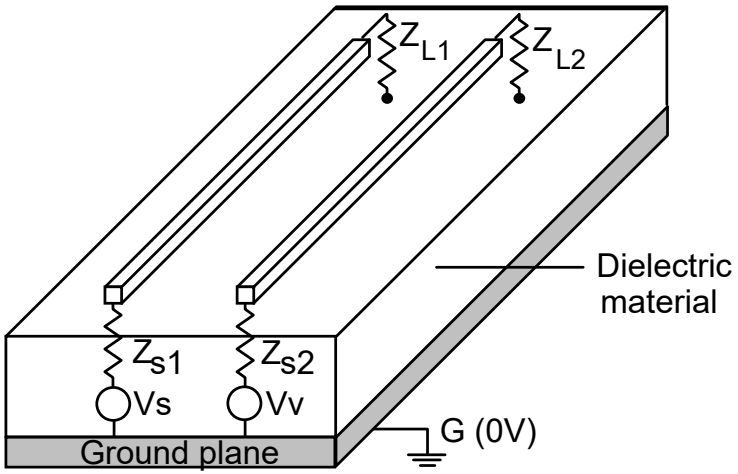
Crosstalk (a.k.a. – EMI at the Microscopic Level)



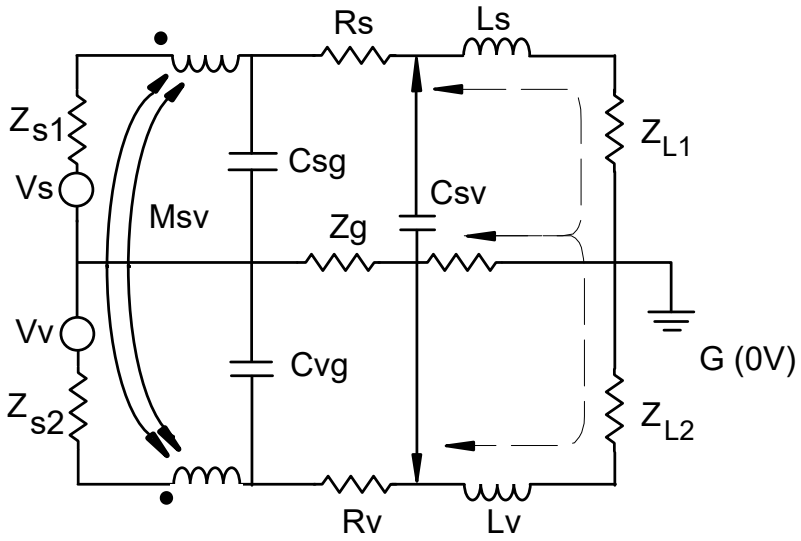


$$Z_V = \frac{Z_{s\,(v)} \times Z_{L\,(v)}}{Z_{s\,(v)} + Z_{L\,(v)}}$$

C_{sv} = Capacitance between source trace and victim trace
C_{vg} = Capacitance between victim trace and ground
C_{sg} = Capacitance between source trace and ground

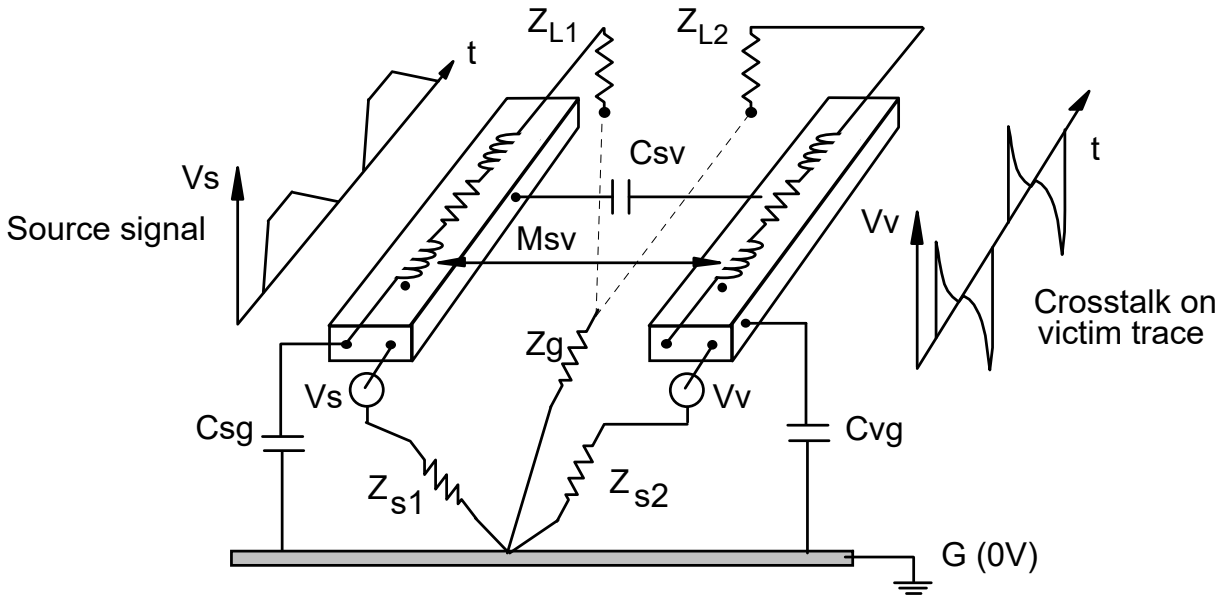


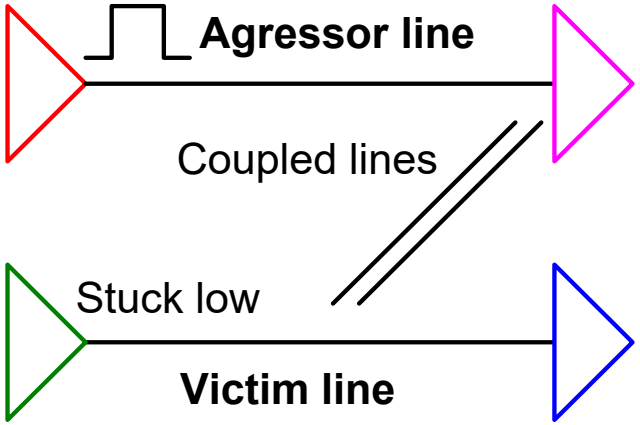
Parallel traces over a ground plane

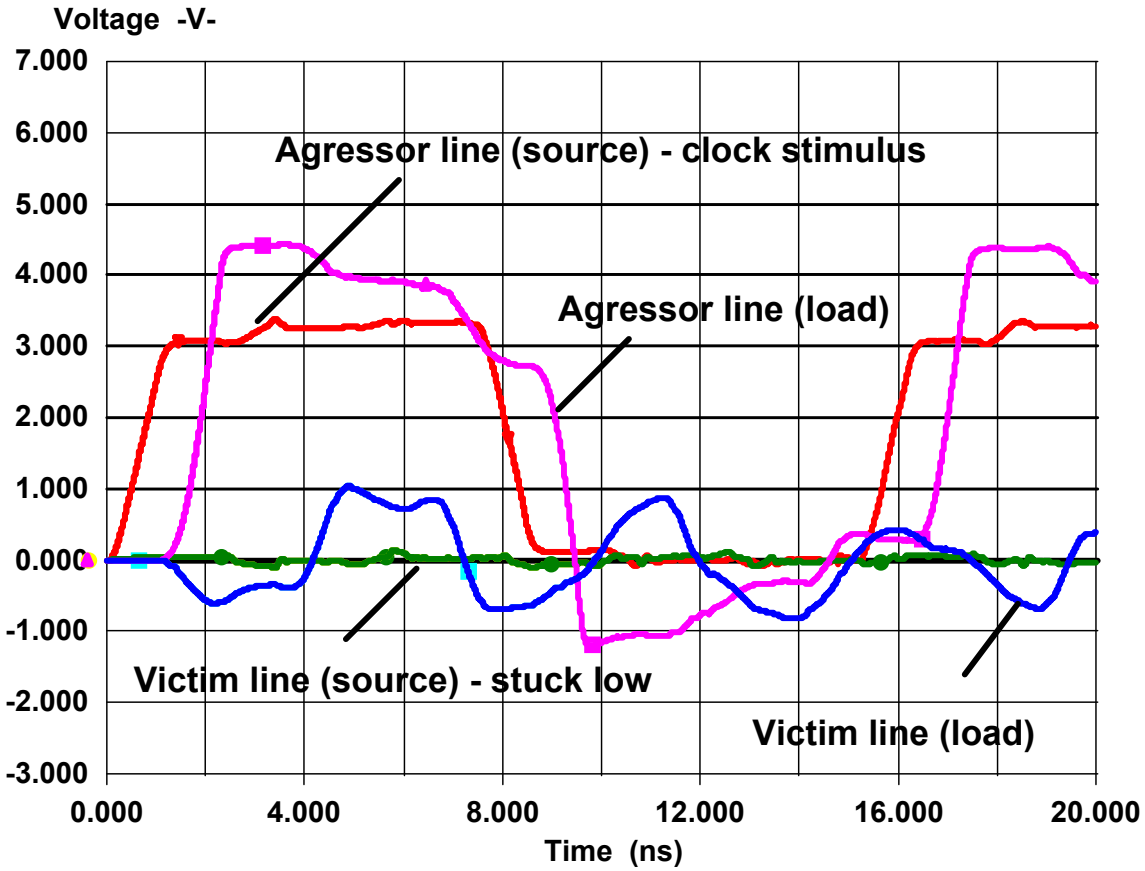


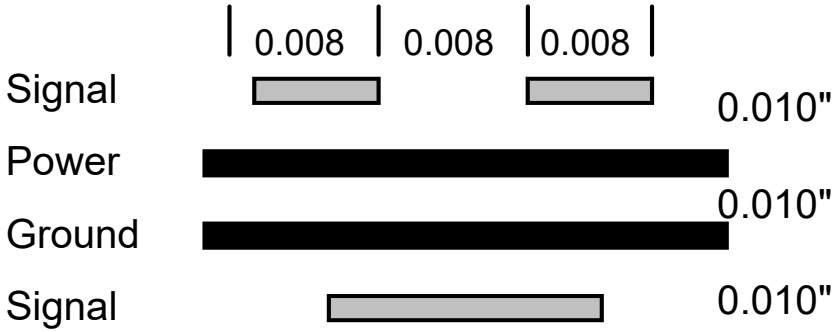
Schematic representation of a three wire circuit

C_{sv} = Capacitance between source trace and victim trace
C_{vg} = Capacitance between victim trace and ground
C_{sg} = Capacitance between source trace and ground





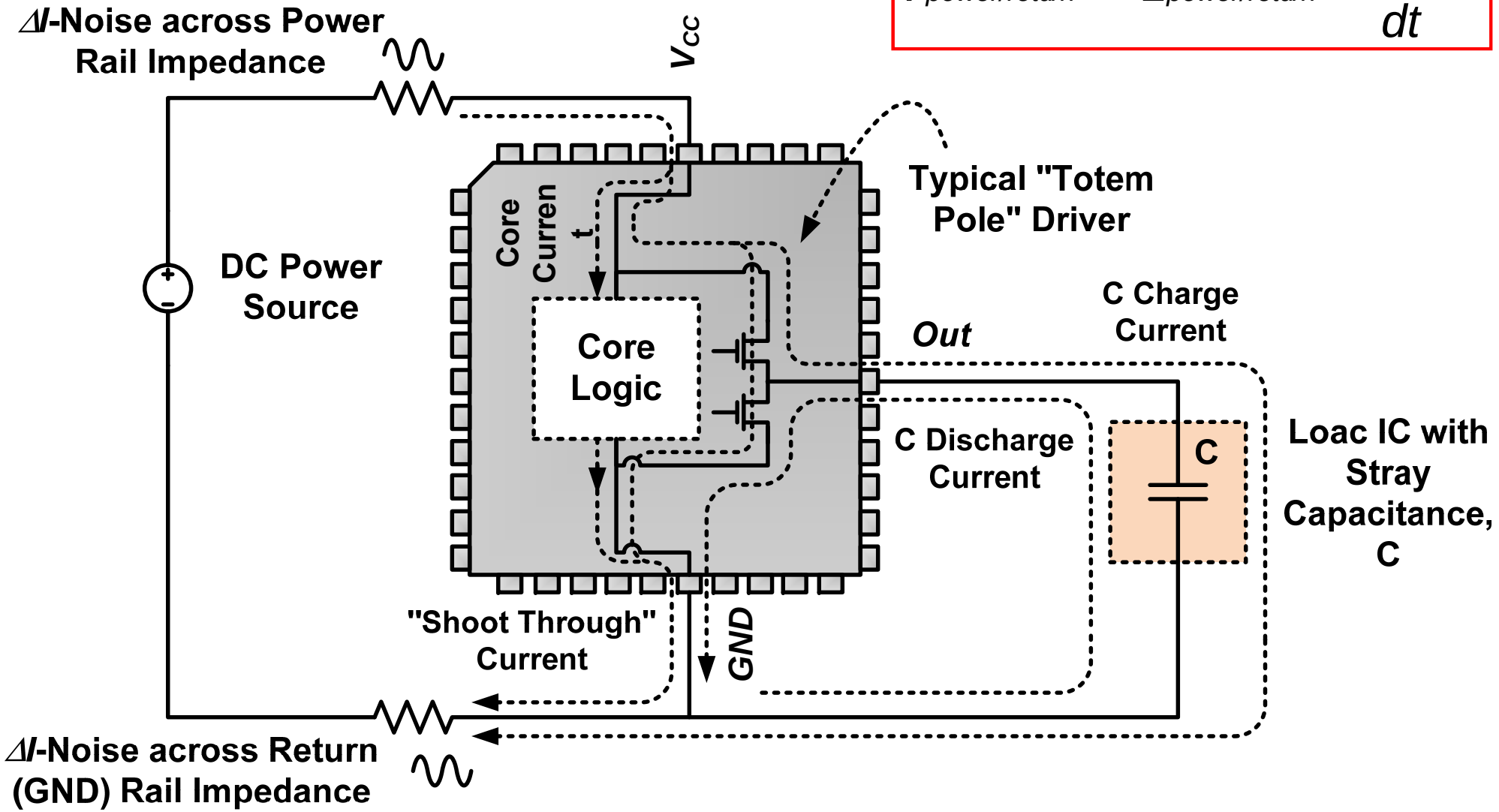




8.0 inches (20.3 cm) long, 72.1 ohms
Propagational delay: 1.126 ns
Oscillator: 66 MHz, 49% duty cycle
CMOS, 3.3V, Fast
Traces: 0.008" wide and 0.008" apart (.20mm)
Distance to reference plane: 0.010" (.25mm)

Power and/or Return Plane Bounce

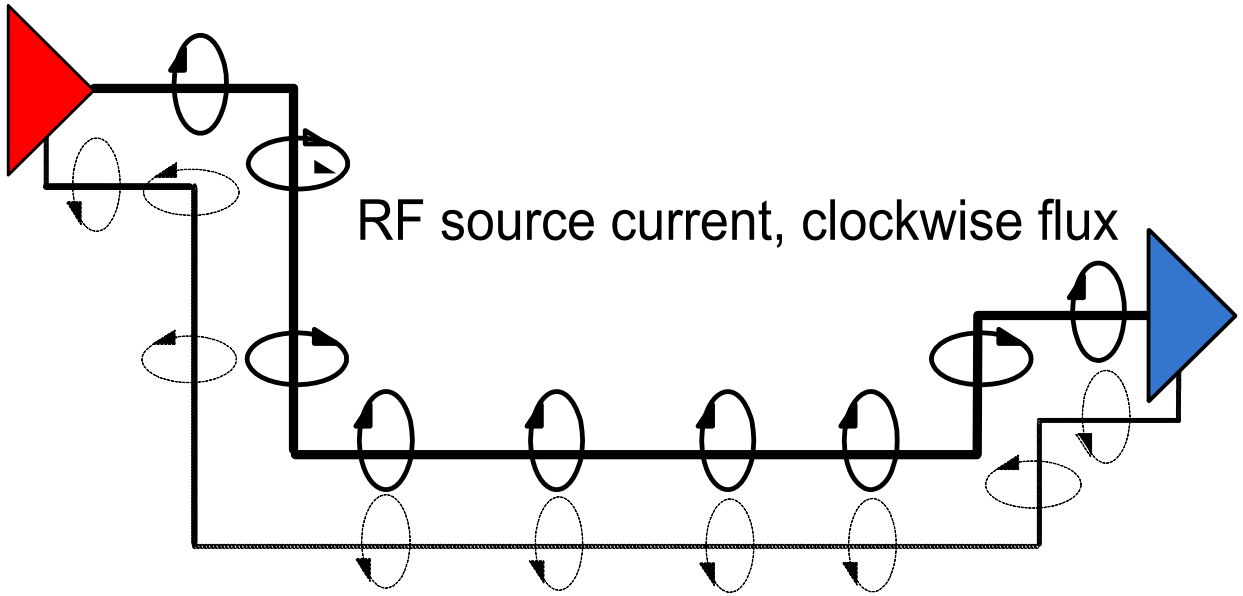
$$V_{power/return} = - L_{power/return} \frac{dI_{discharge}}{dt}$$



RF Signal and Return Current Propagation

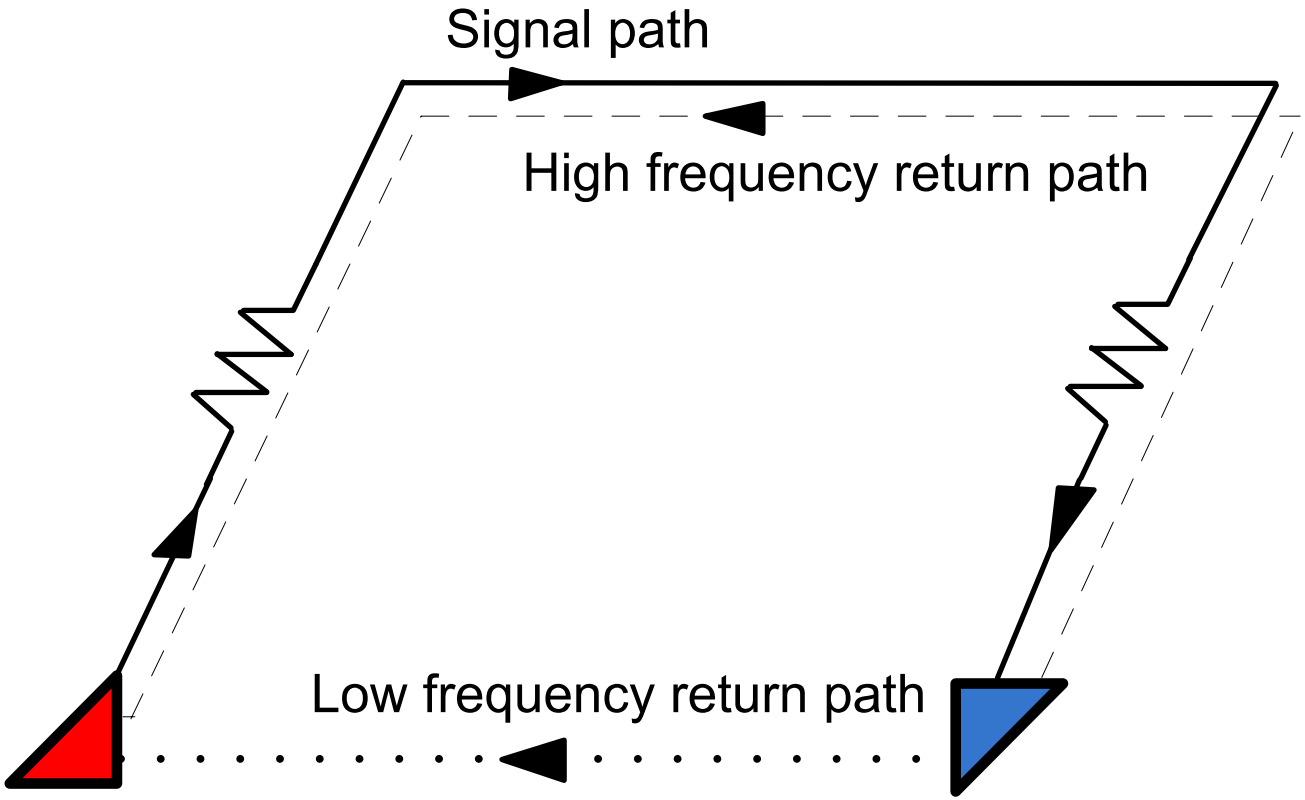
RF Current Return and Flux Cancellation

The closer we bring the RF return path to the RF source path, enhanced coupling occurs, producing less RF energy

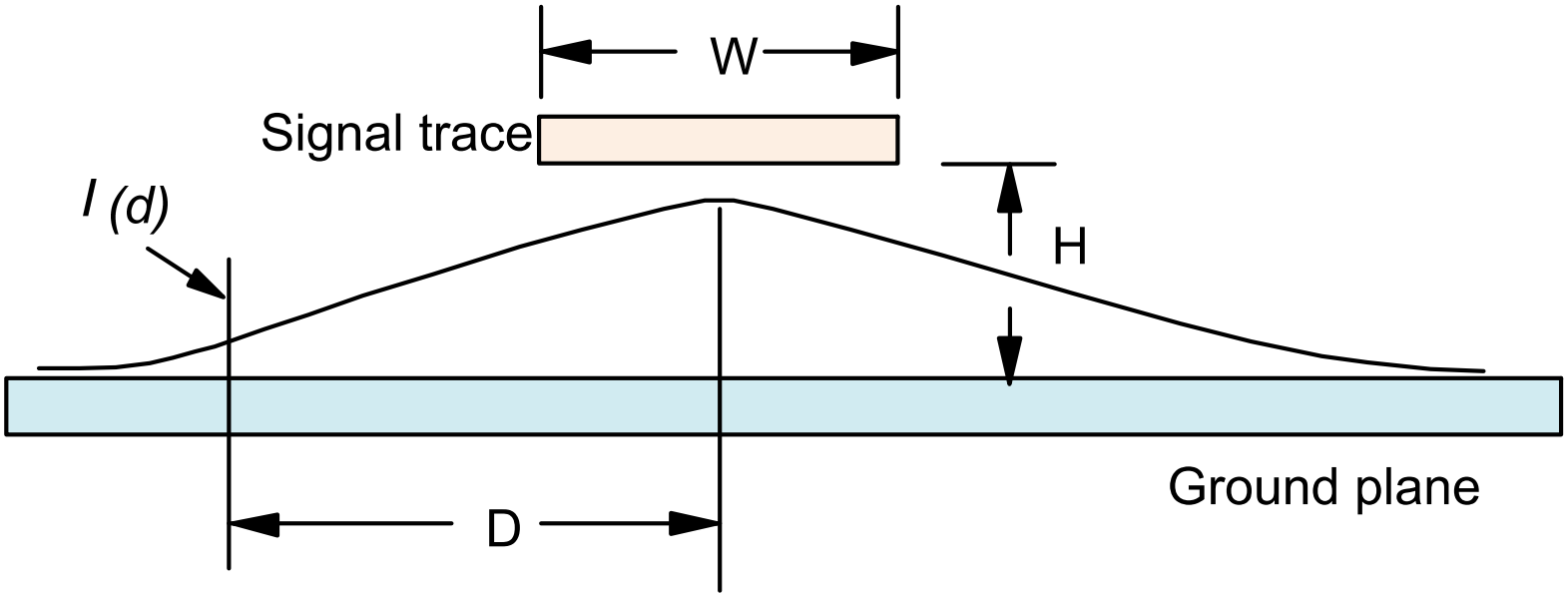


RF Signal Return Path Propagation (High and Low Frequency)

- A layer of metal, generally copper at either voltage or return potential, physically adjacent to a signal routing layer.
- Solid planes provide a low impedance path for RF currents to return to their source (*optimal flux return).*
- If both transmission lines are closely coupled or near to each other, magnetic flux between both transmission lines will cancel out.



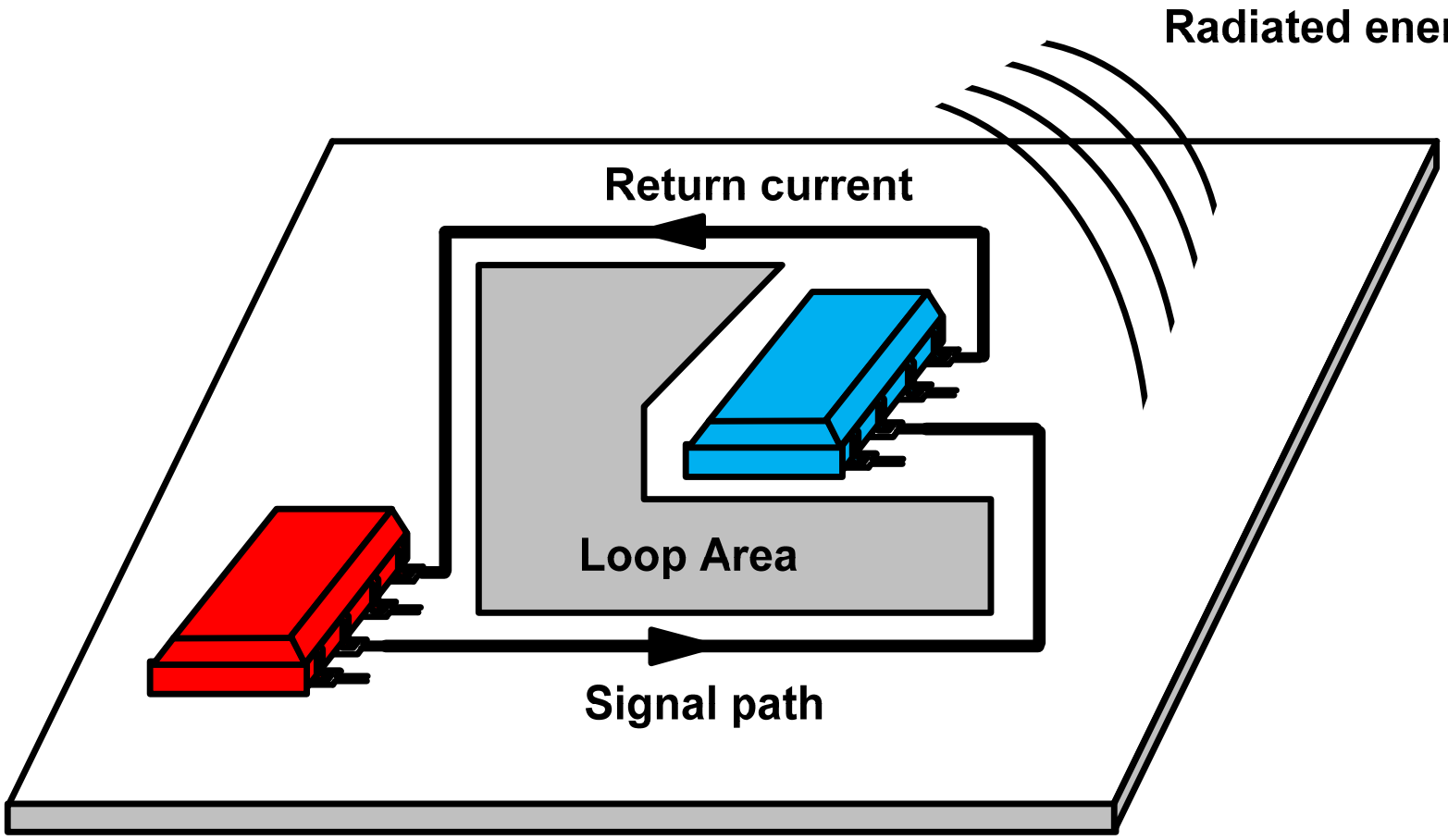
RF Current Density Distribution



$$I(d) = \frac{Io}{\pi H} \cdot \frac{1}{1 + \left(\frac{D}{H}\right)^2}$$

where: *I(d)* = signal current density, (A/inch or A/cm)
Io = total current (A)
H = height of the trace above the ground plane (in. or cm)
D = perpendicular distance from the center line of the trace (in. or cm)

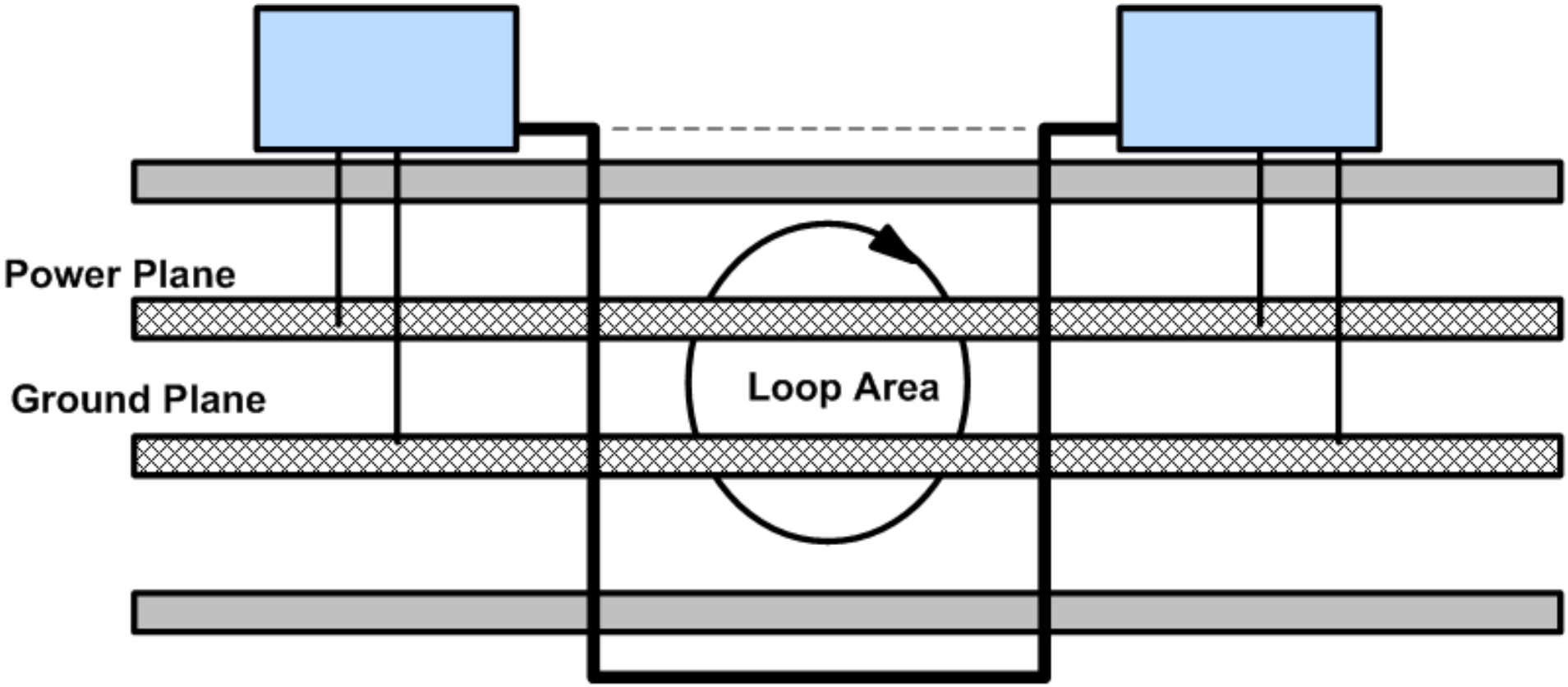
Loop Area Between Circuits or Components – Same Layer



This configuration is for a single- or double-sided PCB.

For a multi-layer PCB, loop area is in the plane directly below the signal path.

Loop Area Between Circuits or Components – Different Layers



The real loop area is longer than shown, as the transmission line must have both a source and return path. Only the source path is shown. The return path is through either the power or ground plane, depending on application.

Calculating the RF Field from the Loop Area Between Components

EMI is created from currents flowing between components. A small loop is one whose dimensions are smaller than a quarter wavelength ($\lambda/4$) at a particular frequency of interest.

Maximum electric field strength from a loop ***in free space***

$$E = 131.6 * 10^{-16} (f^2 * A * I_S)\left(\frac{1}{r}\right) \text{ volts per meter}$$

where A = loop area in cm^2, f (MHz) is the frequency of I_s, the source current in *mA* and r is the distance from the radiating element to the receiving antenna.

Differential-mode radiation from a cable affixed to the PCB with a ***return path***

$$E = 263 * 10^{-16} (f^2 * A * I_S)\left(\frac{1}{r}\right) \text{ volts per meter}$$

Common-mode radiation from a cable affixed to the PCB with a ***return path***

$$E = 1.27 * 10^{-6} (f * L * I_S)\left(\frac{1}{r}\right) \text{ volts per meter}$$

Capacitive Loading Effects on Every Transmission Line

- Capacitive loading affects trace impedance
- Unloaded propagation delay for a transmission line is defined by

$$t_{pd} = \sqrt{LoCo}$$

With increased capacitive loading, propagation delay of the signal will increase by:

$$t_{pd}' = t_{pd}\sqrt{1+\frac{C_d}{C_o}} \quad ns/length$$

Characteristic impedance of a transmission line, altered by gate loading, Z'_o is lowered by:

$$Z'_o = \frac{Z_o}{\sqrt{1+\frac{C_d}{C_o}}}$$

where

Z_o = Original unloaded line impedance (ohms)

Z'_o = Modified line impedance (ohms)

C_d = Input gate capacitance of all loads

C_o = Characteristic capacitance of the unloaded transmission line

Calculating Trace Lengths to Determine if Termination is Required

Assuming velocity of propagation 60% speed of light (FR-4), the maximum permissible un-terminated round trip considering the ***two-way propagation delay*** (source-load-source) is:

$$L_{\max} = \frac{t_r}{2t'_{pd}}$$

where t_r is in nanoseconds, t'_{pd} is propagation delay, and L_{max} is actual routed length.

- A simple equation is available to ***approximate*** length of an electrically long line trace.
- If the routed trace is longer the L_{max}, termination is required.
- Note: Think in the ***time domain - not frequency domain!***

$$L_{max} = k * t_r$$

$L_{max} = 9 * t_r$ *(for microstrip topology - in cm.)*
$L_{max} = 3.5 * t_r$ *(for microstrip topology - in inches)*

$L_{max} = 7 * t_r$ *(for stripline topology - in cm.)*
$L_{max} = 2.75 * t_r$ *(for stripline topology - in inches)*

Example

If a signal edge is 2 ns, the maximum unterminated trace length when routed microstrip is:

$$L_{max} = 9 * t_r = 18 \text{ cm } (7")$$

For stripline, the maximum unterminated trace length is: $L_{max} = 7 * t_r = 14$ *cm (5.5")*

Calculate trace length to minimize reflections and enhance signal integrity.

$$L_d < L_{max}$$

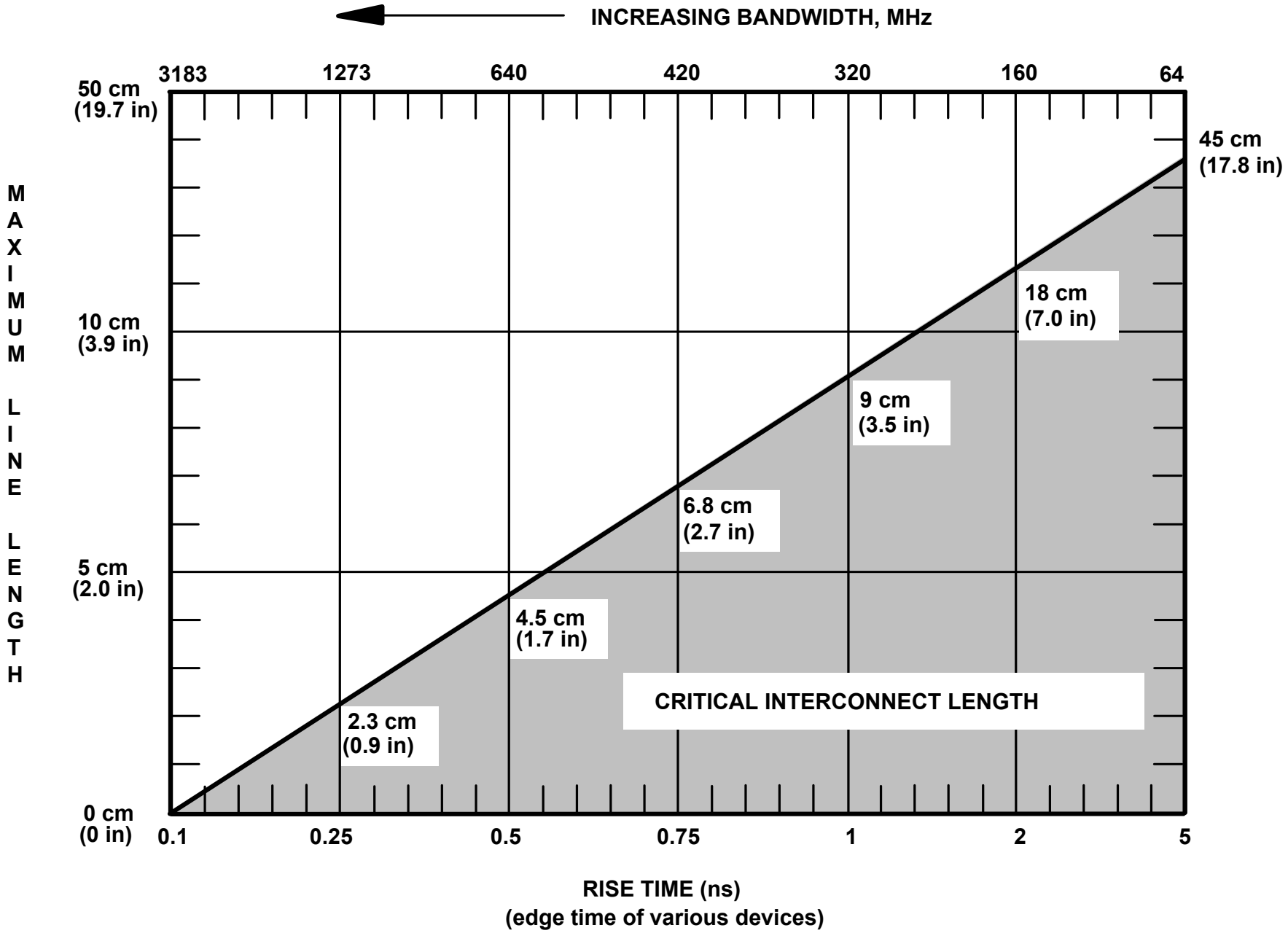
where L_{max} is calculated maximum length and L_d the actual length of the trace.

- To calculate the "*k*" factor for determining if a transmission line is electrically long, using a different value for the dielectric constant, the following equation is provided $$k = x\left(\frac{a}{t_{pd}}\right)$$

where k = constant factor for transmission line length determination
a = 30.5 for cm, 12 for inches
x = 0.5 (converts transmission line to one way path)

Example: for ε_r = 4.1, L_{max} = 8.87 for microstrip (in cm) or 3.49 (in inches)
L_{max} = 6.99 for stripline (in cm) or 2.75 (in inches)

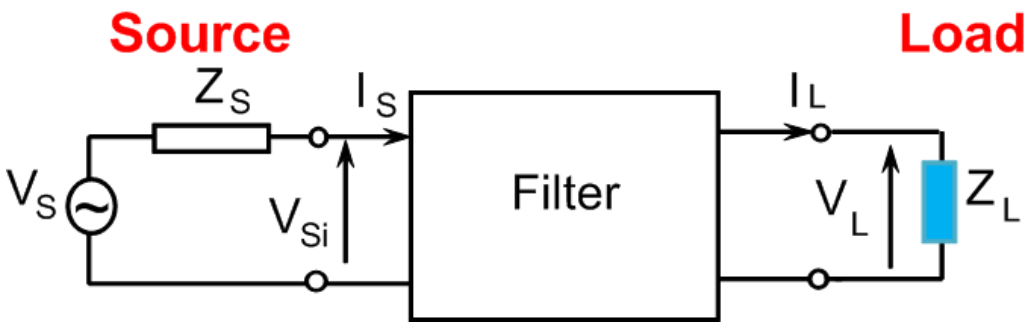
Maximum Unterminated Line Length vs. Signal Edge Rate



Note: Above calcuations are for a microstrip topology with a dielectric constant of 4.1.
Actual distance will differ based on the dielectric material used within the board assembly.

Simplified Introduction to Filtering Related to Transmission Lines Carrying Common-Mode RF Energy

What is a Filter?



A filter is simply a two-port device, with the following transfer function, *H(f)*:

$$H(f) = \frac{E_L(f)}{E_{Si}(f)}$$

Filters are characterized by: **Insertion Loss**

$$IL(f) = 20 \cdot Log \frac{E_{L1}(f)}{E_{L2}(f)} = 20 \cdot Log \frac{E_L(f) \text{ w/ Filter Inserted}}{E_L(f) \text{ w/o Filter Inserted}}$$

Basic Filter Configurations

Two basic types of RF filter methods exist; *capacitive and inductive*

Different applications require one, the other or both. Most lower bandwidth (≤ 10 MHz) circuits will benefit from use of filtering, which are not effective unless their placement is exactly adjacent to their interconnect.

Capacitive bypass filtering is used to shunt high frequency RF currents to an appropriate 0-V reference or chassis.

Inductive filters blocks RF fields from either leaving the system as an output signal, or prevents incoming RF from corrupting circuits on the PCB.

Basic Filter Characteristics

Simplest type (first-order filter) contains a single reactive component.

- Capacitive reactance, X_C, will decrease with an increase in frequency.
- Inductive reactance, X_L, will increases with an increase in frequency.

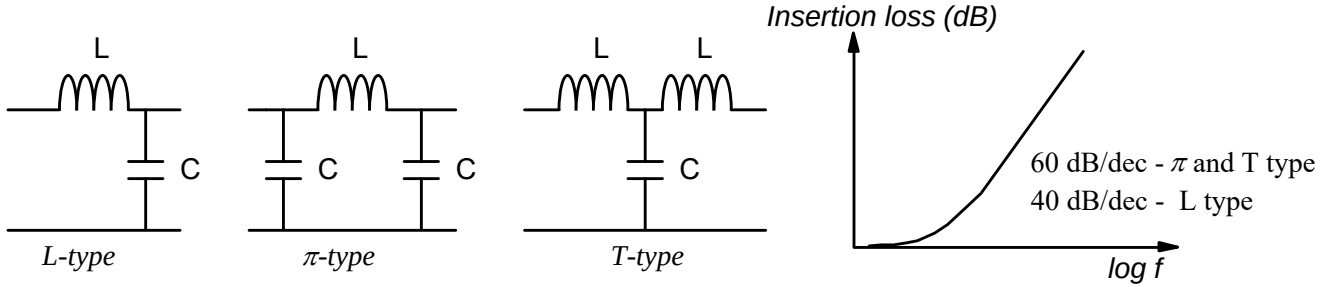
$$X_C = \frac{1}{2\pi fC} \;; \qquad X_L = 2\pi fL$$

- Capacitors shunt noise current away from a load while inductors block or reduce noise in the transmission line.
- Single component filters are not very useful as their attenuation only changes at a rate of 6 dB/octave or 20 dB/decade.

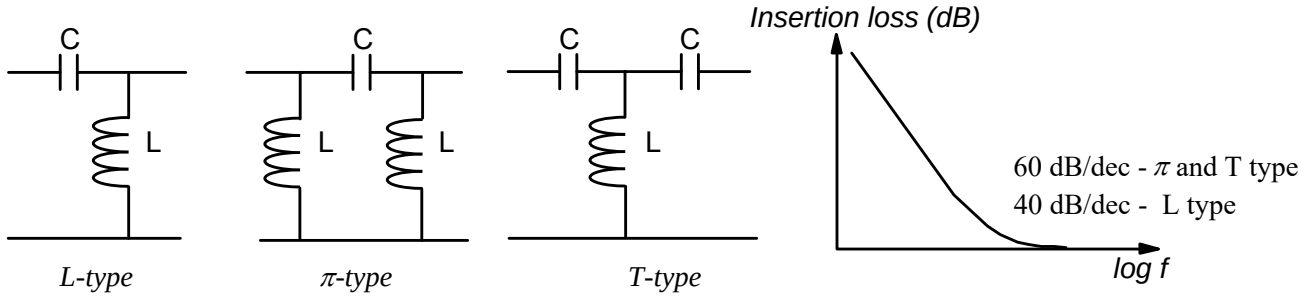
To achieve greater attenuation, a second or higher-order filter consisting of two reactive components or more is required. This filter provides 12 dB/octave or 40 dB/decade attenuation.

Signal and Power Line Filter Configurations

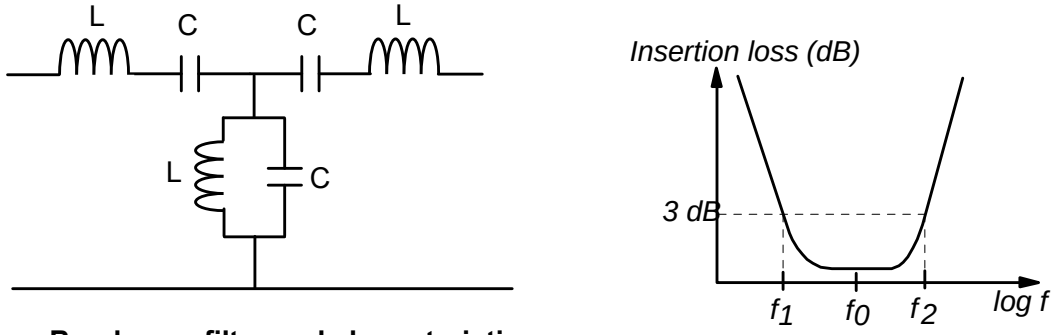
- **Low pass** – Rejects undesired RF energy above a desired set point, passing frequencies below this point with little or no attenuation. AC line filters are typically of the low pass variety.
- **High pass** – Rejects undesired RF energy below a desired set point, passing frequencies above this point with little or no attenuation.
- **Band pass** – Passes a range of desired frequencies with little or no attenuation, rejecting frequencies outside this specific range.
- **Band reject** – Rejects a range of frequencies within a particular frequency band of operation while passing all other frequencies outside this band.



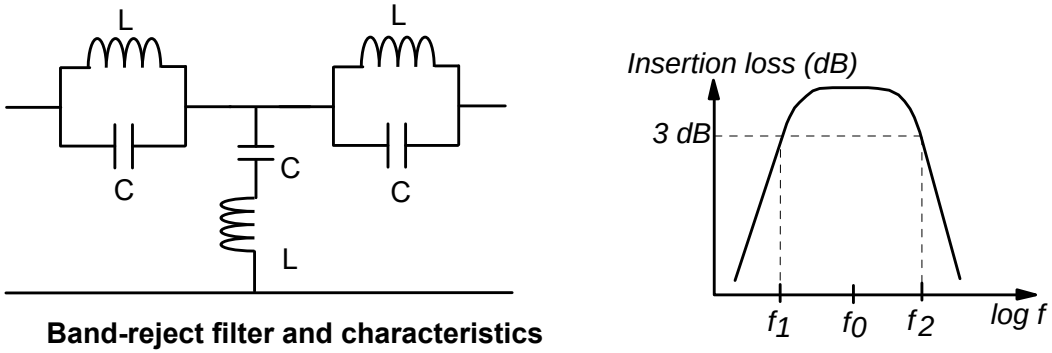
Low-pass filter and characteristics



High-pass filter and characteristics



Band-pass filter and characteristics



Band-reject filter and characteristics

Common Mode Chokes

Large amounts of capacitance cause the following problems

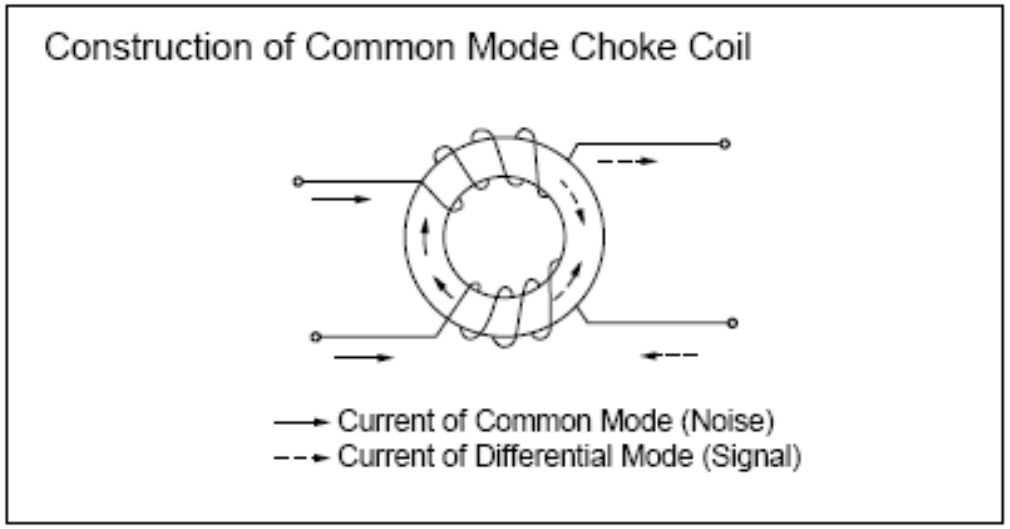
- Leakage current in power supply circuits may violate product safety requirements against the hazard of electric shock
- Capacitance limits the desired signal bandwidth for data signals

Large inductors cannot be used

- Large DC currents may saturate the magnetic core of the inductor in power line filters, decreasing performance capability
- Large inductance provides little effect on limiting unwanted noise both above and below the desired bandwidth of a signal trace

Common Mode Chokes

- Affect only common-node RF noise with virtually no effect on DM signals
- Provide high common-mode signal losses



Summary

Designing for EMC is easy *if* one thinks about the overall objective *before* any design aspect of a system occurs.

1. Understand requirements to meet; emissions and/or immunity.
2. Understand the environment the system must operate within.
3. Simplify complex theory into easy-to-use concepts.
4. There is no difference between time and frequency domain.
5. The key item to remember is minimizing development of unwanted magnetic field flux and to keep all transmission lines balanced (prevents creation of common-mode currents).
6. Systems must be self-compatible; does not cause harm to itself.
7. Use secondary means of flux removal by implementing an optimal referencing/grounding methodology, use of proper gasket material for shielding (if required) and incorporating filters correctly.
8. Take time in analyzing an EMI situations. A quick fix may not solve the problem.
9. Test and analyze early and often. Simulation is now required for due to advances in semiconductor technology.
10. Keep current with technological advances with education.

EMC Challenges in Telecommunication Equipment

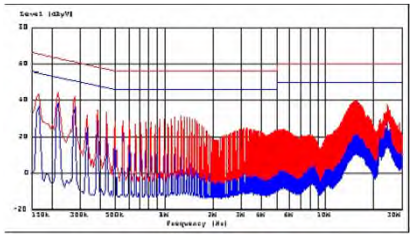
Philippe Sochoux, Sr. Manager, Juniper Networks

Alpesh Bhobe, Sr. Manager, Cisco Systems

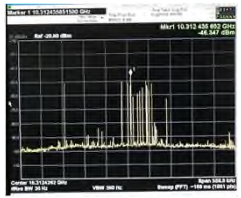
Oct 3, 2019

Agenda

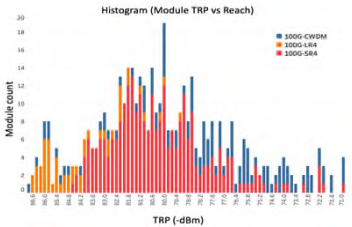
1. Introduction and problem statement
2. Early collaboration/engagement with suppliers to maximize repeatability in CE for PSUs



3. HW scaling to save cost and time



4. Early collaboration/engagement with optical vendors for Radiated Emissions



Introduction

EMC team must deliver Routers and Switches that meet legal, quality and customer requirements on budget and on time

What are and where are the challenges (specific to networking equipment)?

MX2020
20 Line Cards
18 x 2.5kW modules

ASR9922
20 Line Cards
12 x 6kW AC
Modules

Problem Statement - Regulatory requirements

Key regulatory limits (radiated and conducted emissions, ESD) have not changed much since the 1980s when the PC was introduced. Regulatory bodies (IEC/FCC) are not planning to relax the limits.

1983 – Apple IIe, 1.023MHz 65C02 CPU, 64KB RAM (up to 1MB), DOS 3.3, 5 ¼” floppy disk

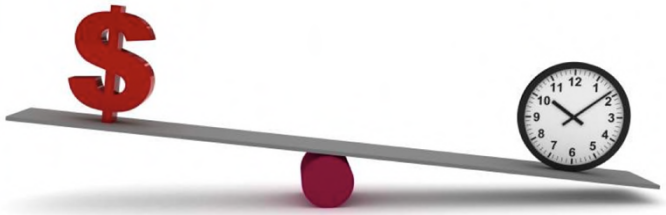
Speeds, densities and power requirements continue to increase, driven by bandwidth demands around the world as new technologies are introduced (4K/8K/16K videos, 5G, etc.)

NETFLIX

Year	Global Internet Traffic
1992	100 GB per day
1997	100 GB per hour
2002	100 GB per second
2007	2,000 GB per second
2017	46,600 GB per second
2022	150,700 GB per second

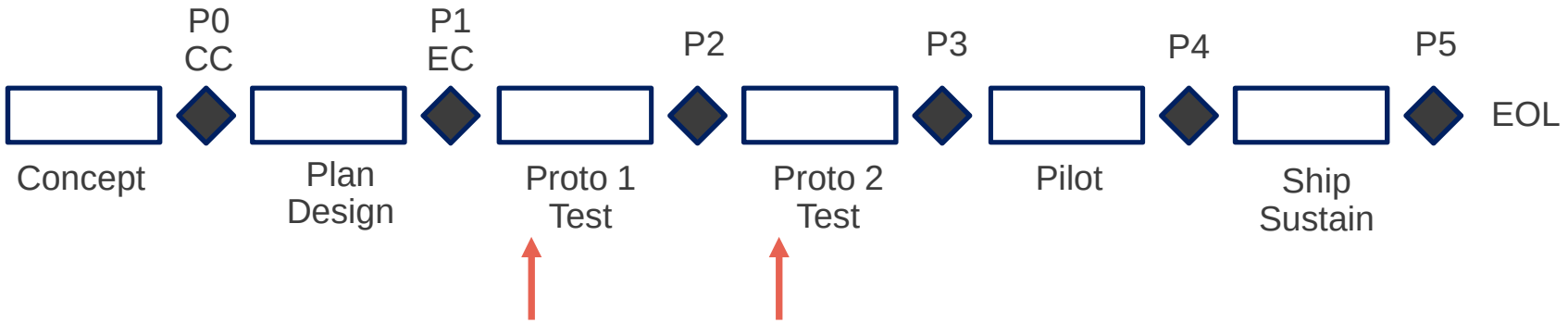
Source: Cisco VNI, 2018.

Problem Statement - Budget versus Time



- We prioritize time (schedule) over budget
- Designs are increasingly complex
- Unplanned modifications can cancel a project
- Schedules are not increasing even if design complexities increase
- Primary challenge is schedule predictability
- How do we mitigate schedule risk?

Risk mitigation vs schedule



Best practices, rule checking — Up to early 2000's

Ad-hoc simulations + Early 2000-2010s

3D simulations + reverb chamber, early partnerships w/ vendors, enhanced supplier specifications + 2010+

Maximize repeatability for CE in PSUs

Issue: Large variations (>10dB) in CE measurement results between labs increasing schedule risk

Goal: Root cause sources of variations and establish a deterministic testing process at the PSU level

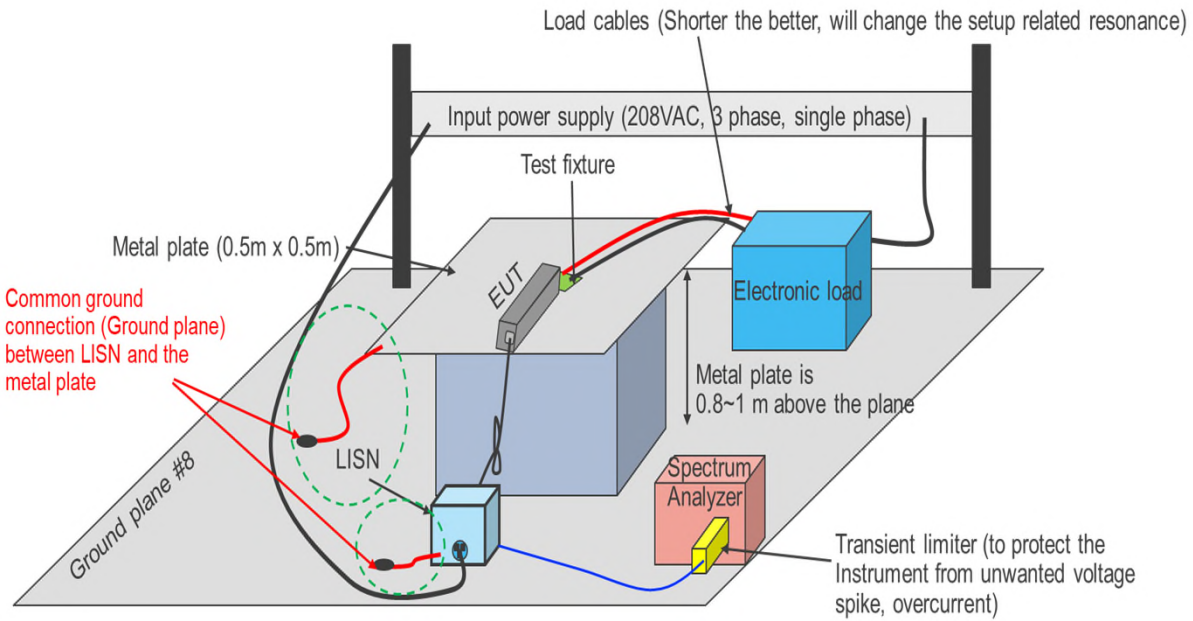
Reference paper:

A Multi-mode Noise Reference Source for Verifying Different Conducted Emission Setups

Wei Zhang[1], Rui Mi[1], Javad Meiguni[1], Shubhankar Marathe[1], Kaustav Ghosh[2], Angela Li[2], Qian Liu[2], Jacques Rollin[2], Philippe Sochoux[2], David Pommerenke[1]

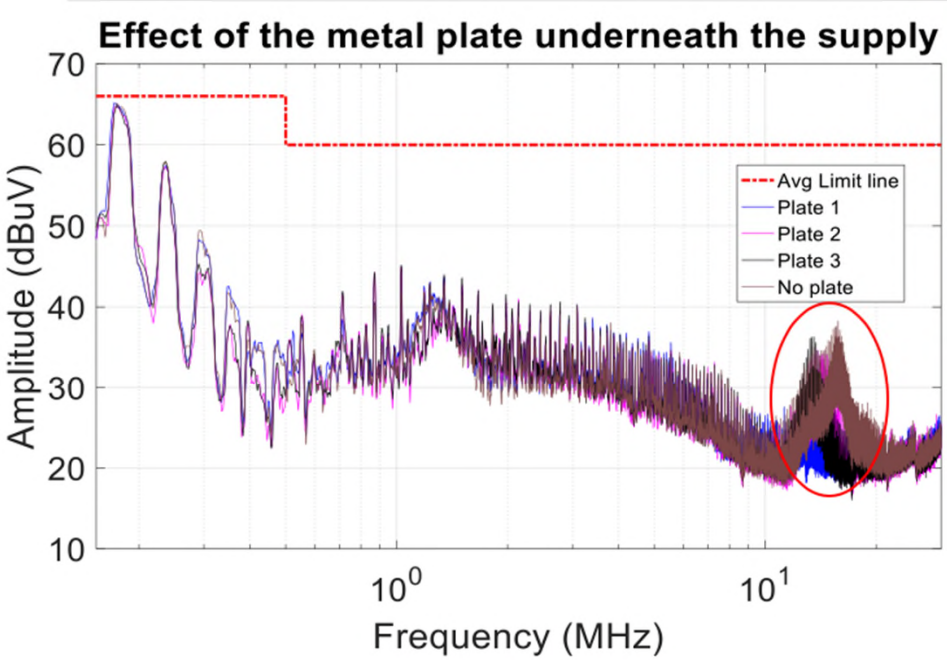
[1]EMC Laboratory, Missouri University of Science & Technology
[2]Juniper networks

CE Bench Setup



No standard exists to define PSU CE bench level testing

Setup related emission variations – plate size



LISN measurement

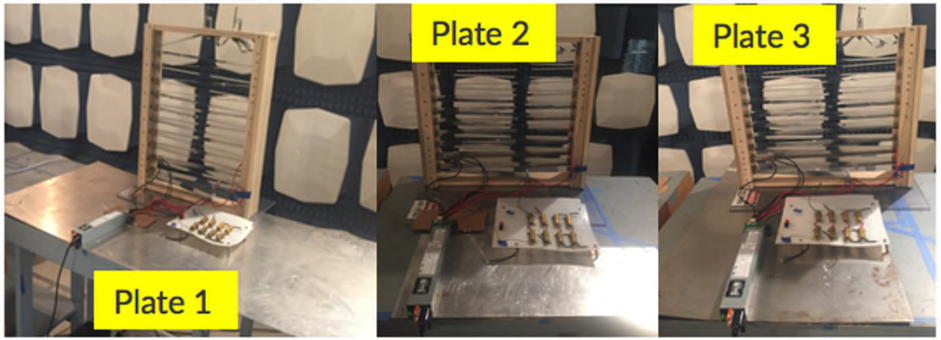
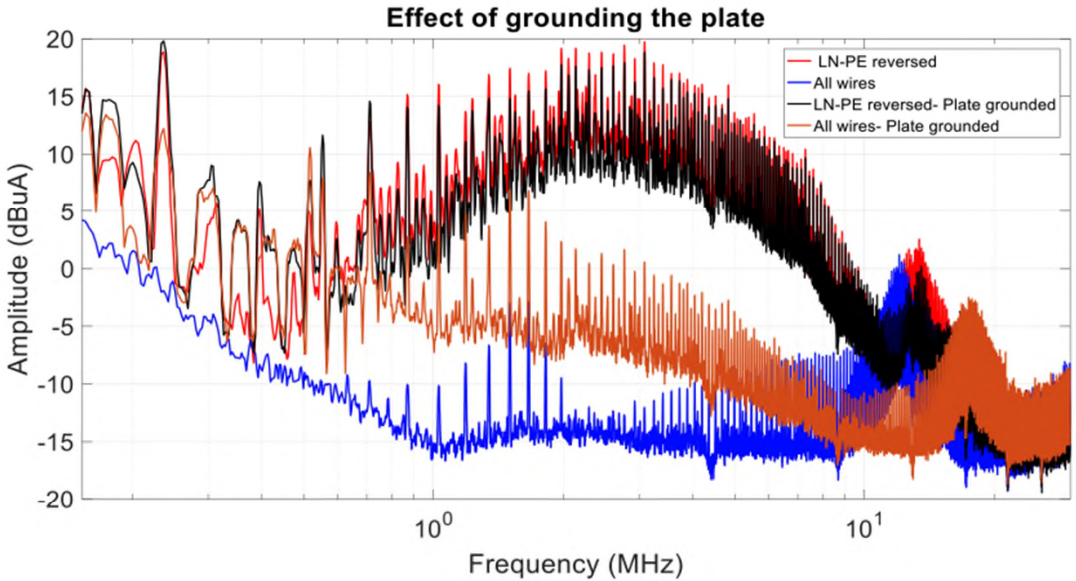
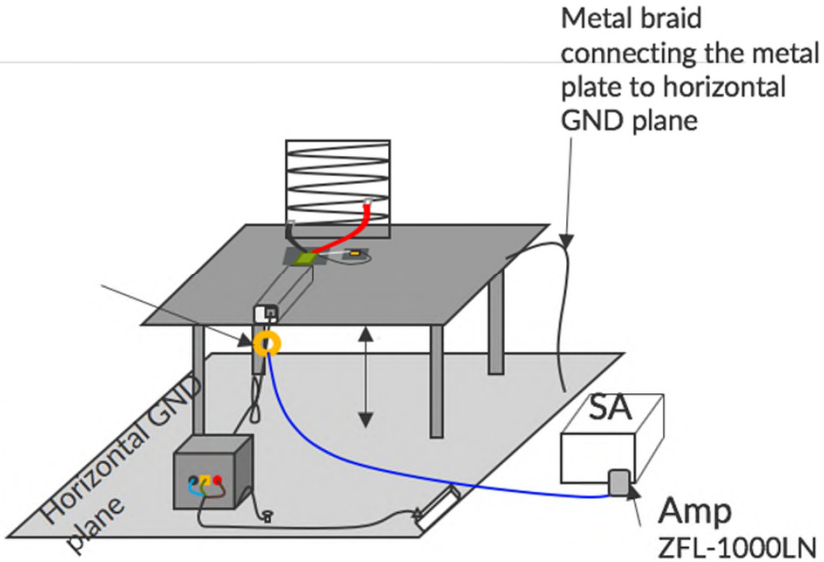


Plate 1> Plate 3 > Plate 2

- The resonance around 10 MHz is due to the combined size of the plate and the load.
- Changing the size of the plate changes the capacitance and produces L-C resonance in the setup structure as a result of which the resonance shifts for different plate sizes.

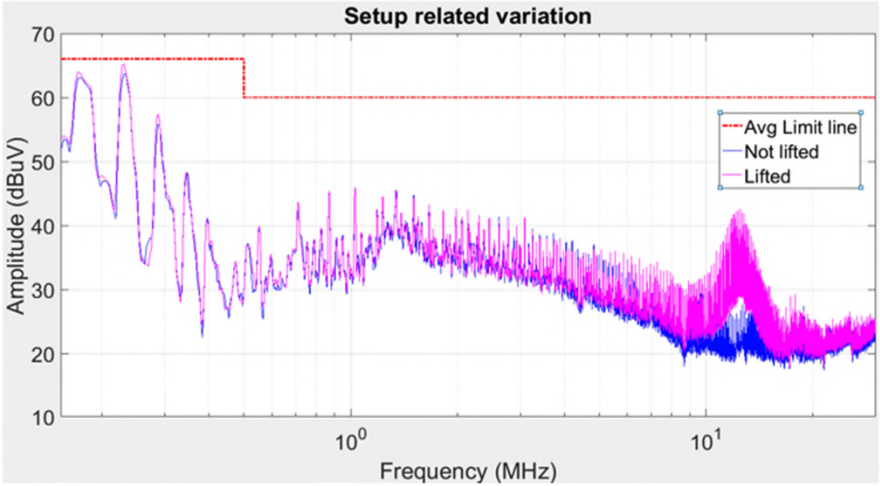
Setup related emission variations – grounding the plate





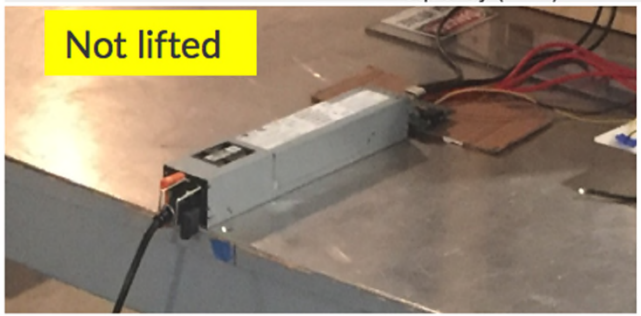
Current clamp measurement

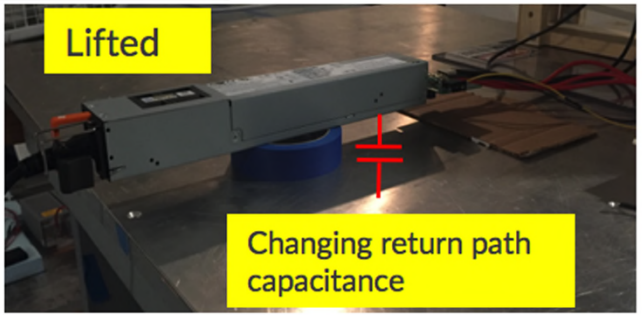
Setup related emission variation – CM return path capacitance



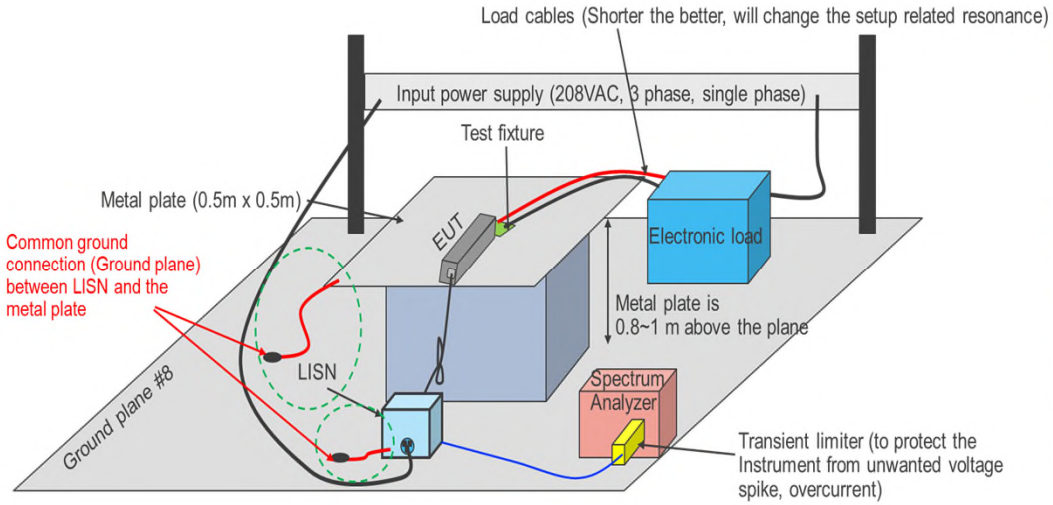
Therefore, the resonance around 10 MHz is setup dependent.

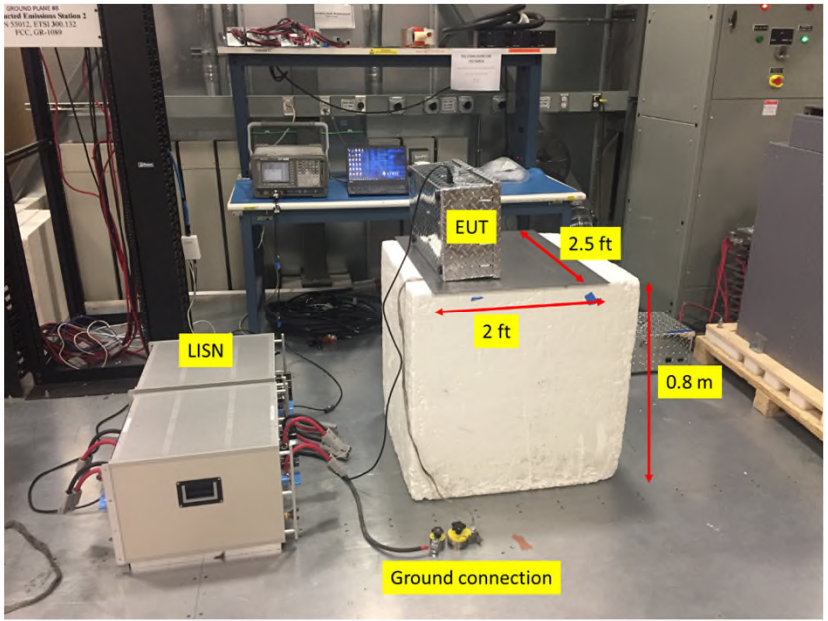
Lifting up the supply changes the parasitic capacitance which is the CM current return path.



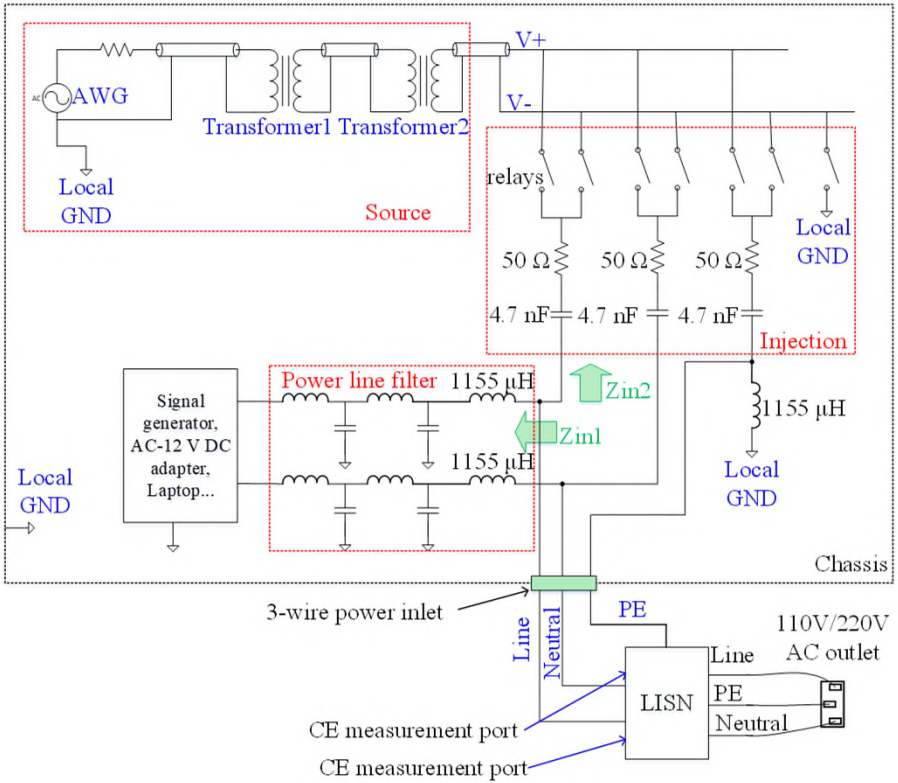


Conducted Emission Specification





Conducted Emission Specification



HW quantity optimization for Radiated Emissions (scaling)

Issue: Early prototypes are very costly and time consuming to manufacture. RE testing requires a full chassis

Goal: Reduce prototype quantities using known and verified extrapolation curves (scaling)

Juniper
QFX10008

Juniper
QFX10016

Juniper
MX2020

Cisco
ASR 9906

Cisco
ASR 9912

Cisco
ASR 9922

Growth of Radiated Emission in Multi-Modular Systems

Kaustav Ghosh[1], Wei Zhang[1], Javad Meiguni[1], Abhishek Patnaik[1], David Pommerenke[1], Philippe Sochoux[2], Jacques Rollin[2], Angela Li[2], Qian Liu[2], and Girish M H[2]

EMI Prediction of Multiple Radiators

Javad Meiguni[1], Wei Zhang[1], Morten Soerensen[1], Kaustav Ghosh[1], Ahmad Hosseinbeig[1], Abhishek Patnaik[1], David Pommerenke[1], Jacques Rollin[2], Angela Li[2], Qian Liu[2], and Philippe Sochoux[2]

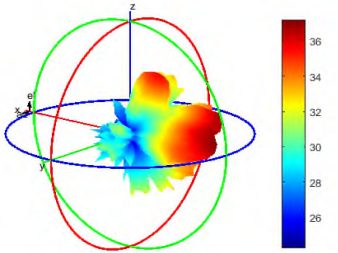
[1]EMC Laboratory, Missouri University of Science & Technology [2]Juniper networks

Investigation plan

3 independent methods were used to to validate the proposed approach:

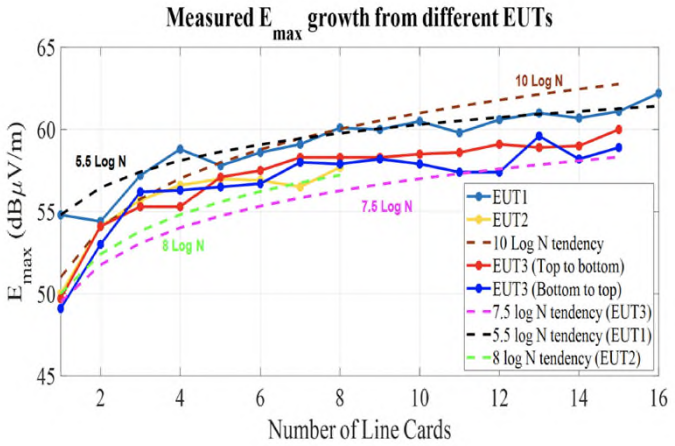
Chassis mockup
A HW mockup with patch antennas representing optics to measure scaling effects in a controlled environment.

Measurements show 10logN tendency



Monte Carlo Analysis
A full chassis populated with 498 radiating elements (optics) representing a large phased array was simulated using random sampling (phase & amplitude) to obtain scaling curves.

Simulations show 10logN tendency



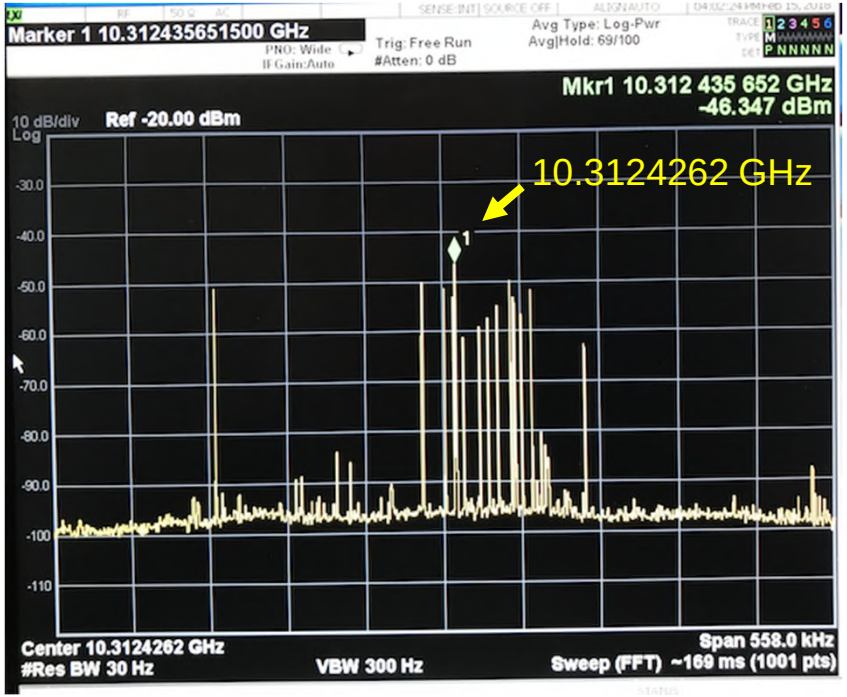
Scaling study of Juniper HW
PTX3K, PTX5K, Ultimat 8, Ultimat 16 scaling studies were done at Juniper JET facility.

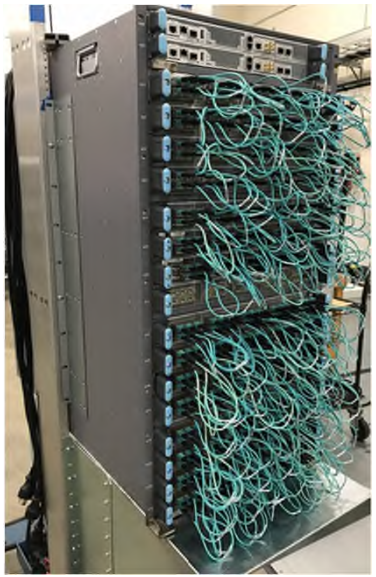
Measurements show between 5logN and 7.5logN tendency.

Why?

Why 7.5logN (measurements @ JNPR) vs 10logN (expected)? Unsynchronized linecards

- Frequencies are equal on a same linecard
- Frequencies are different between linecards

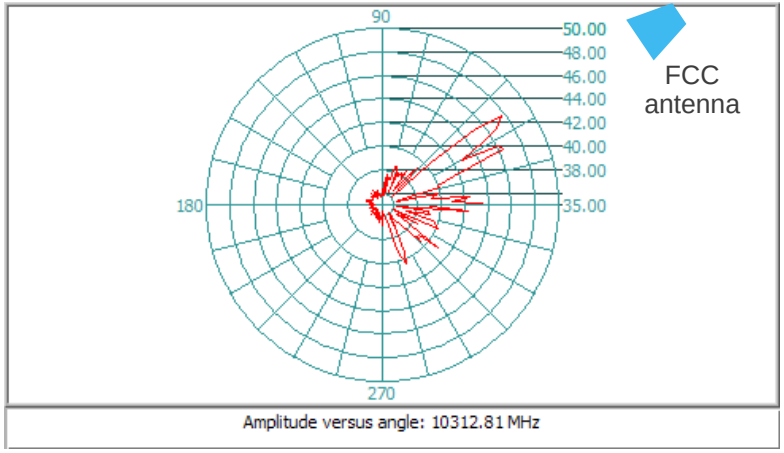




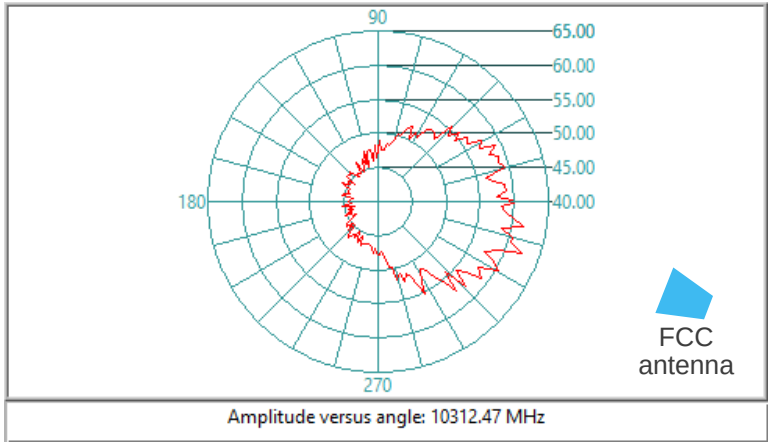
Each linecard radiates at a slightly different frequency (~10-100KHz)

Why 7.5logN (measurements @ JNPR) vs 10logN?
Antenna pattern

- As linecards are added to the chassis, antenna array gain does not increase with constructive interference
- Pattern for one linecard has narrow lobes. Addition of linecards broaden the lobes more than increasing the directivity as expected if the frequencies were the same
- The measuring antenna beam width does not capture all of the energy at the same time (eq. to 4 “slices” of the polar plot)
- As a result, 7.5logN vs 10log N tendency is observed
- 5logN – 7.5logN consistently observed on Juniper HW measurements (PTX, QFX)



1 linecard
1 MHz RBW



16 linecards
1 MHz RBW

Optical Pre-qualifications

Issue: Radiated Emission optic qualification requires ~3 weeks of testing, ~15% failure rate on new optics, +2 weeks for every failure, $3K/day

Goal: Establish a deterministic process between optic supplier and system integrator for Radiated Emission testing

Juniper's QFX10016

Cisco's ASR9922

Reference paper:
A statistical-based approach to pre-qualify optical modules for Radiated Emission testing

Philippe Sochoux[2], Angela Li[2], Wei Zhang[1], David Pommerenke[1]

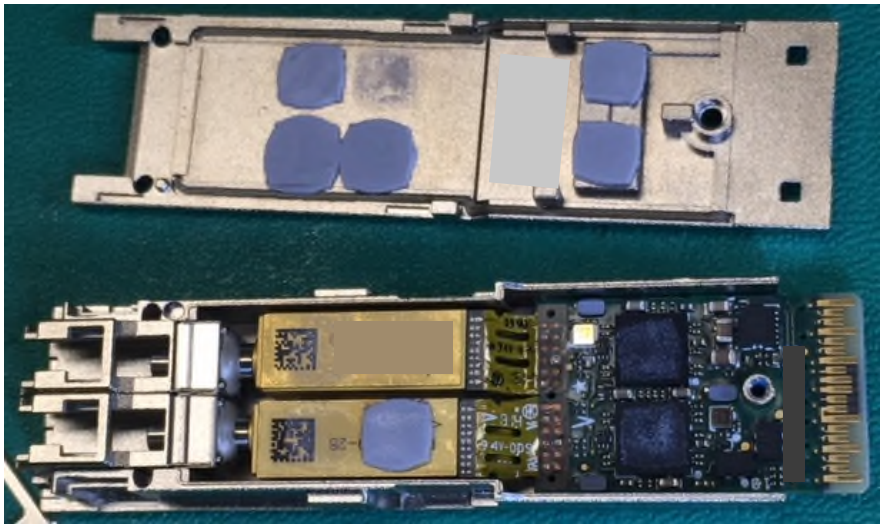
[1]EMC Laboratory, Missouri University of Science & Technology
[2]Juniper networks

Optical modules and EMC

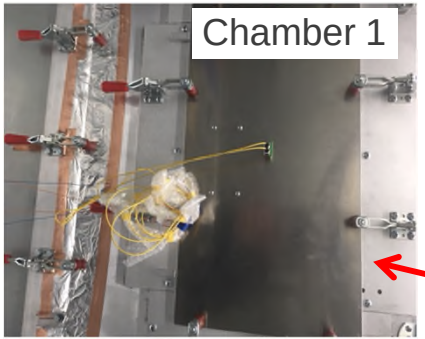
x dB below class B requirement on a single optic doesn’t guarantee consistent system level margin

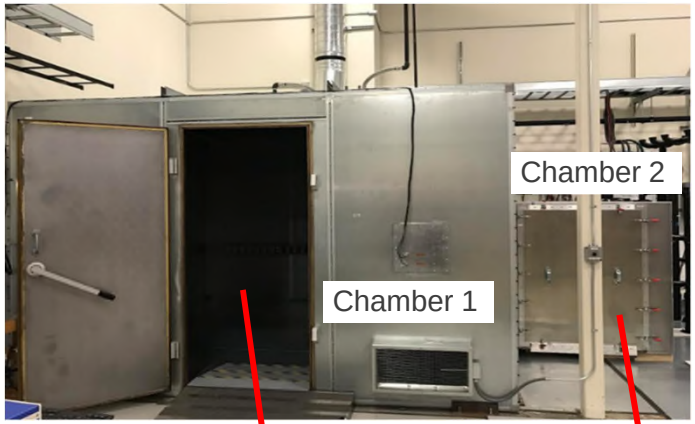
Factors that influence EMC:

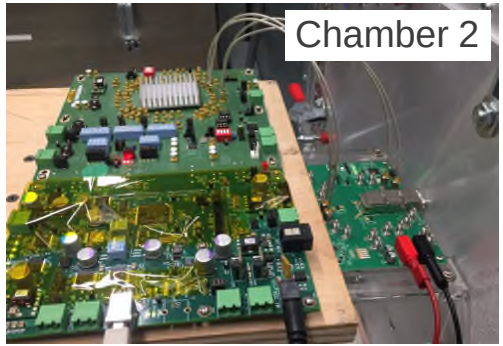
- Electrical design and PCB layout
- Mechanical enclosure (gasket)
- Manufacturing
- Many vendors, speeds (40G, 100G, 200G, 400G) and reaches (LR4, SR4, CWDM, etc) – huge quantities to qualify



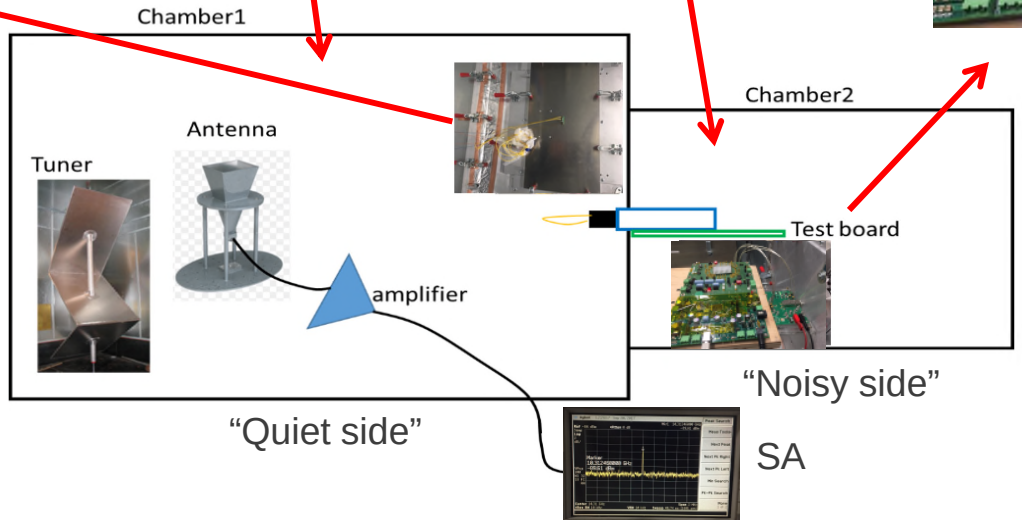
Dual-reverberation chamber measurements







Only the optic protrudes in the “quiet side” (chamber 1) which allows the TRP (Total Radiated Power) from the optic to be measured



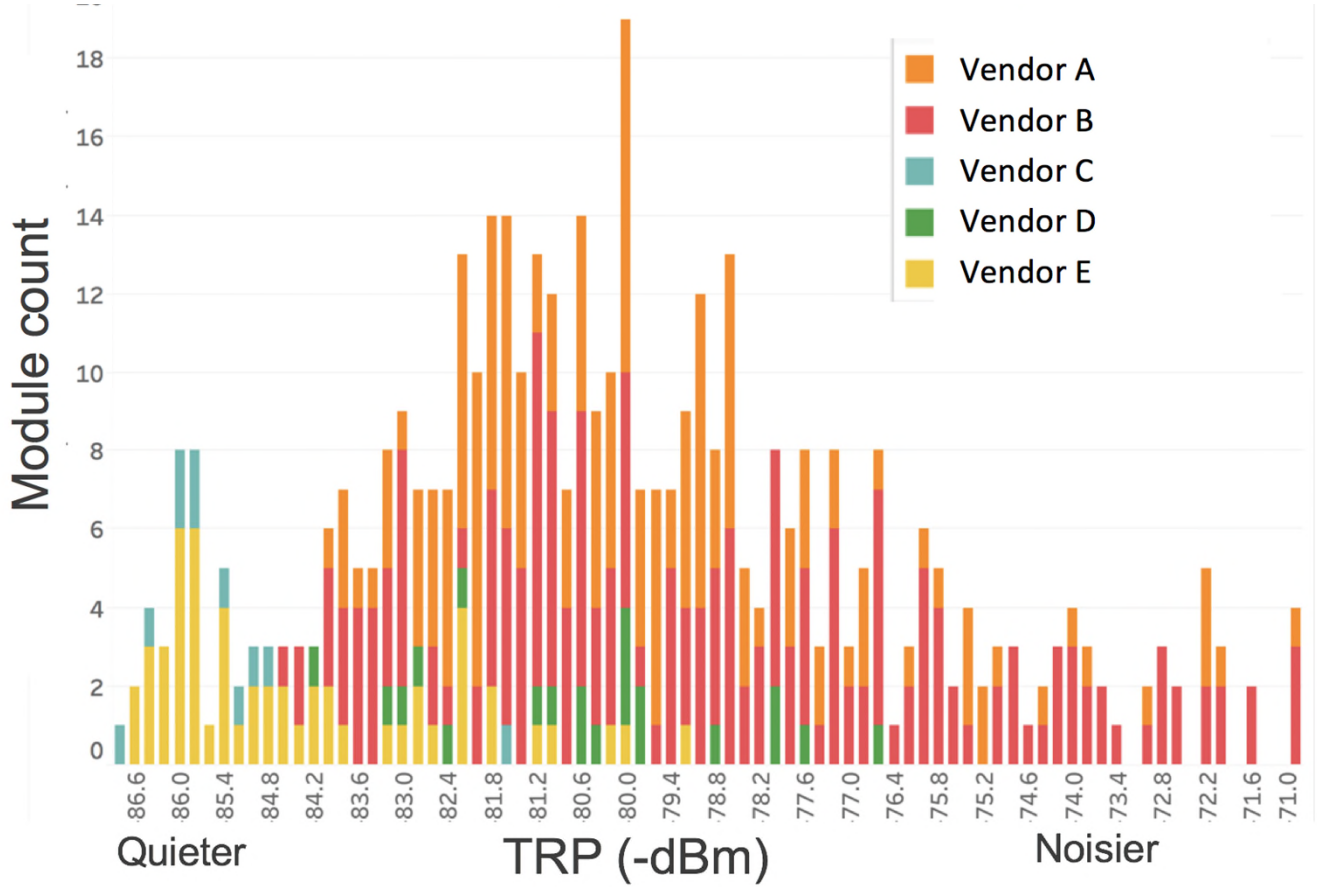
“Quiet side”

“Noisy side”

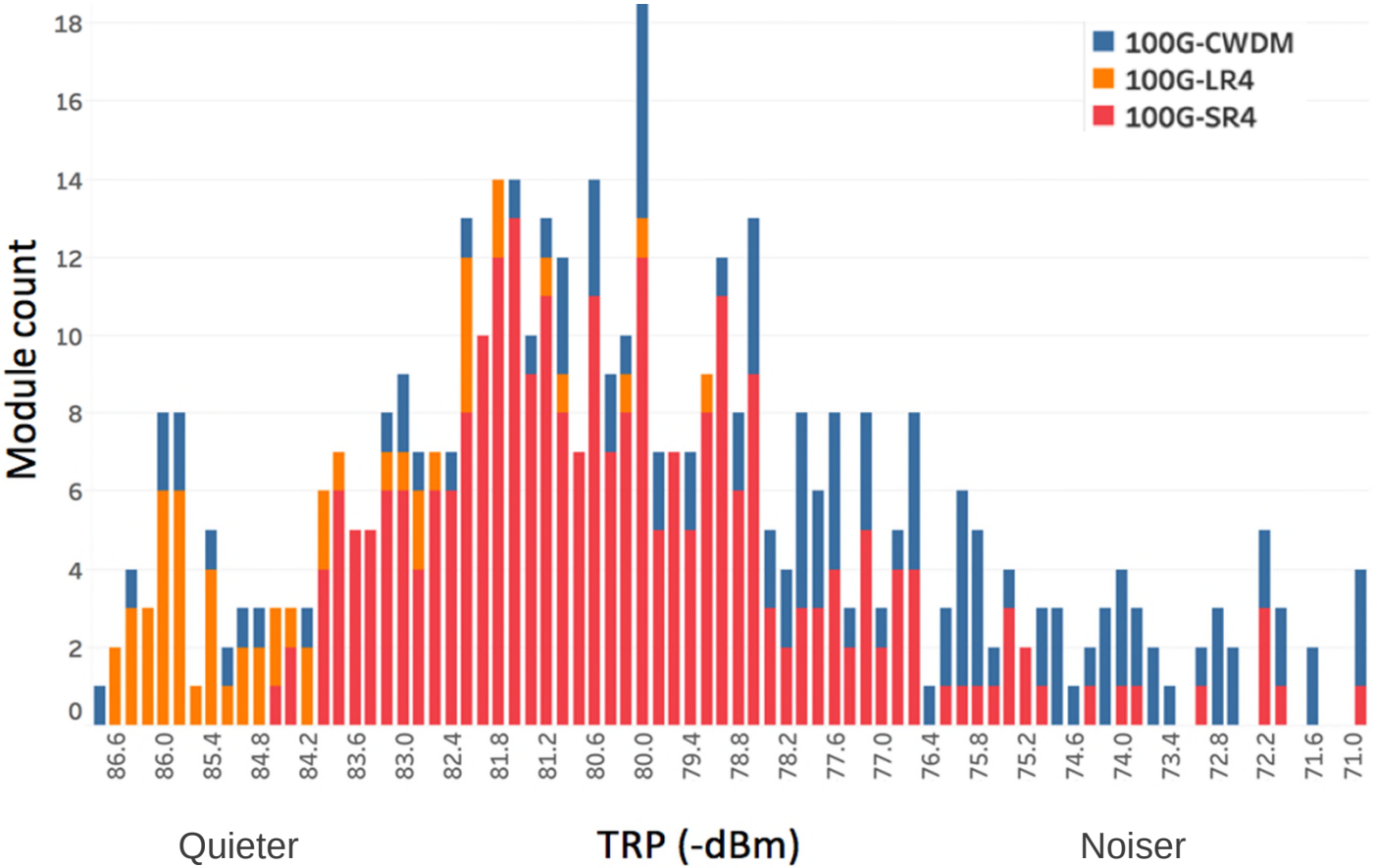
SA

Compliant board is placed in the “noisy side” (chamber 2)

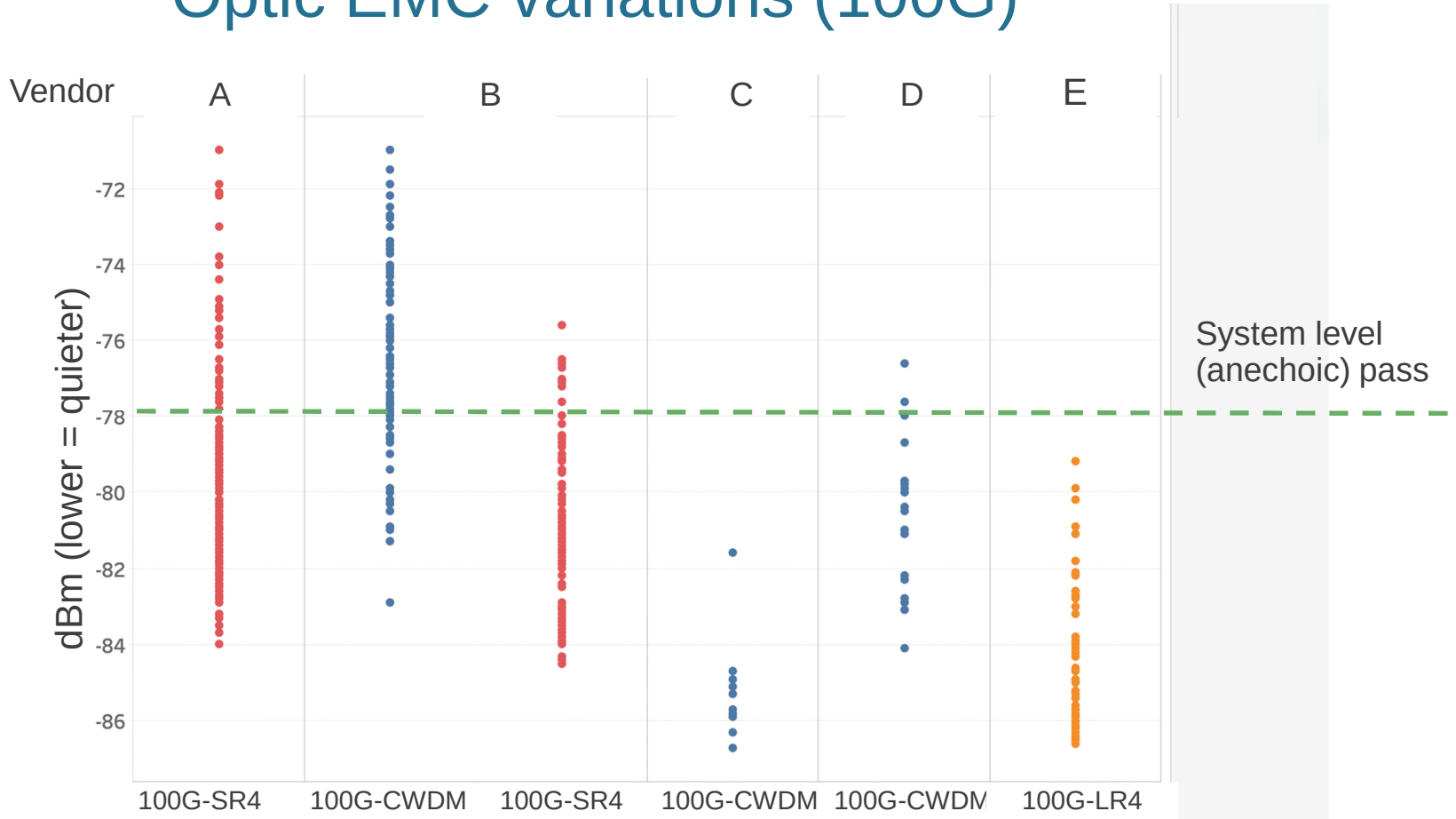
Histogram (100G Optical Module TRP)



Histogram (TRP vs Reach)



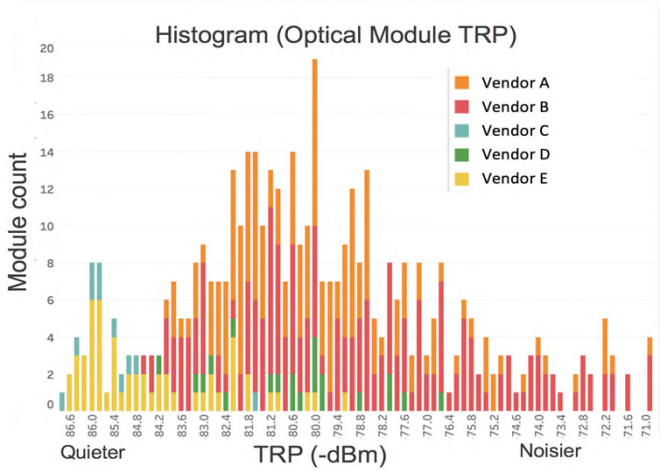
Optic EMC variations (100G)



~6-7dBuV variation at system level

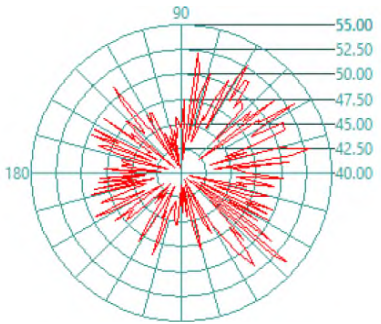
Reverberation and anechoic chamber correlation

- Process of elimination to determine “passing” TRP
- Select 32 noisiest optics and measure at system level
- Repeat with second to noisiest 32 optics
- Repeat until passing margin within range
- Fine tune with individual optics



	Worst optics	Second worst	3rd worst	Best optics	Optimized selection
FCC margin from 32 modules in a Switch (dBuV/m)	+2.6	+0.6	-1	-4	0

$\mu_{pass} \triangleq$ -78dBm (Juniper specific)

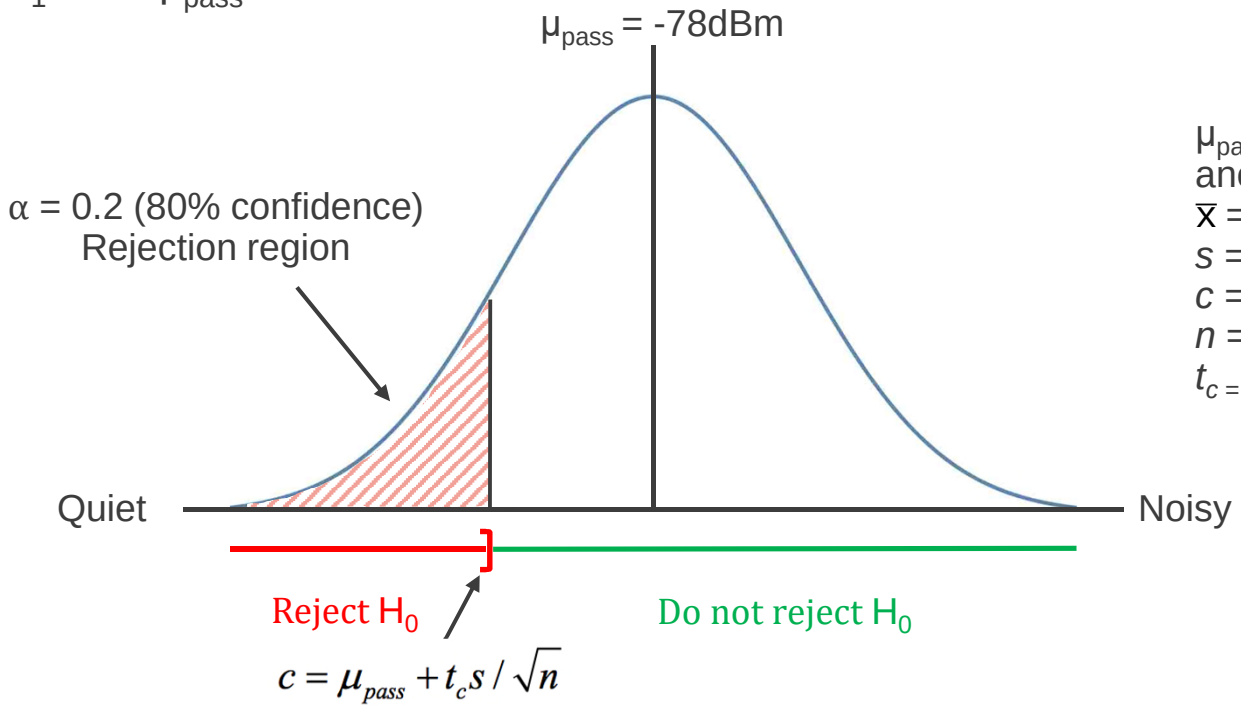


Amplitude vs angle @ 25 GHz

Hypothesis testing

Optic sample's average TRP must be less than μ_{pass} at 80% confidence level

H_0: $\bar{x} \geq \mu_{pass}$ Null hypothesis states that vendor's samples will fail (greater than -78dBm)
H_1: $\bar{x} < \mu_{pass}$



μ_{pass} = average TRP that pass in anechoic chamber
$\bar{x}$ = sample average
s = sample standard deviation
c = critical value
n = sample size
t_c = Student table critical value

Next steps

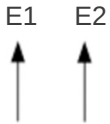
Proposal

Form a consortium of companies (e.g., Optical Internetworking Forum) to draft a common specification for testing optical modules for radiated emissions. The specification will specify the testing methodology and equipment for optical modules in a reverberation chamber environment.

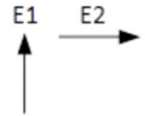
BACKUP

Theory (identical frequency)

Emissions are vectors and must be summed using vectorial math.



$$|Etotal| = |E1| + |E2| = |E1| + 20 \text{ Log } 2$$



$$|Etotal| = \sqrt{(E1^2 + E2^2)} = |E1| + 10 \text{ Log } 2$$

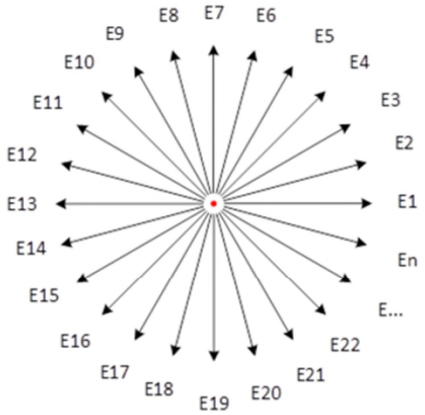
For identical hardware that is synchronized (in phase) we expect the worst case summation for the addition of "n" more hardware:

$$Emax = \Sigma\,(E1 + E2 + E3 + \ldots En) \qquad Emax = E1 + 20 \text{ Log } n$$

For identical hardware that is NOT synchronized (not in phase) we expect a random distribution and summation for the addition of "n" more hardware:

$$Emax = \sqrt{(E1^2 + E2^2 + E3^2 + \ldots En^2)}$$

$$Emax = E1 + 10 \text{ Log } n$$



Taking in consideration space distribution of the noise source and beamwidth of received antenna, the summation is less than the expected 10 Log n

Theory predicts 10logN for electric fields with random distribution

References

Henry Ott, Electromagnetic Compatibility Engineering, pages 340-342

Keith Armstrong, Adding Up Emissions Using the Root Sum Square (RSS) Method Can Help You More Easily Achieve Compliance With EU Emissions Requirements, CEng MIEE MIEEE

Regulatory requirements

International requirements

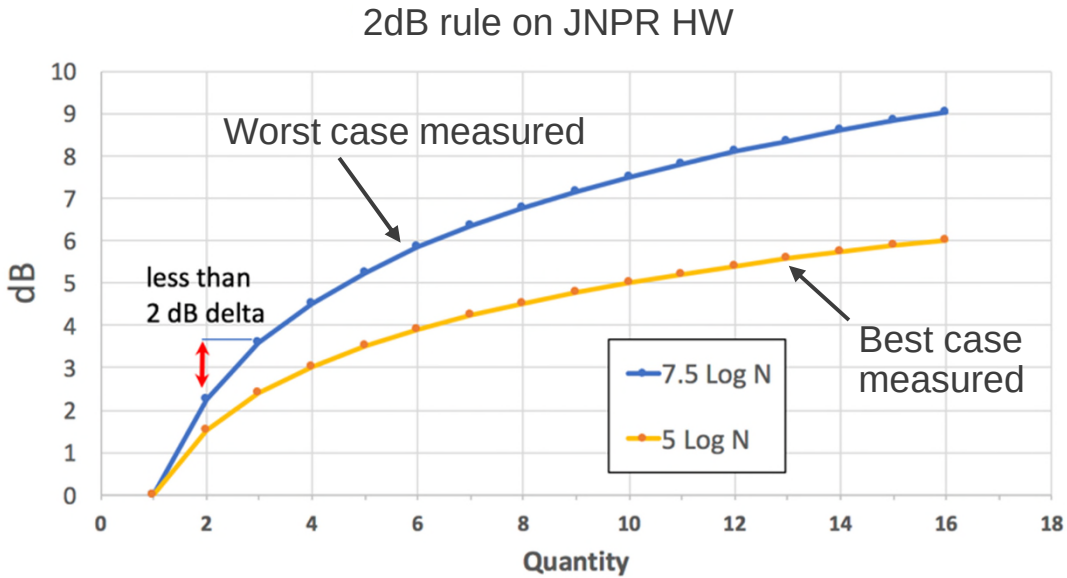
CISPR 32 and FCC part 15 (ANSI C63.4) both propose a 2 dB rule when dealing with large quantities. The worst case quantity to test is reached when the addition of one more unit produces an increase of less than 2 dB in emissions.

EN 300 386, the regulatory requirement in Europe for telecom products refers to CISPR 32 for emissions testing and EN 300 127 for large systems (both Normative). The 2dB methodology of CISPR 32 is therefore applicable to telecom products in Europe.

Customer requirements

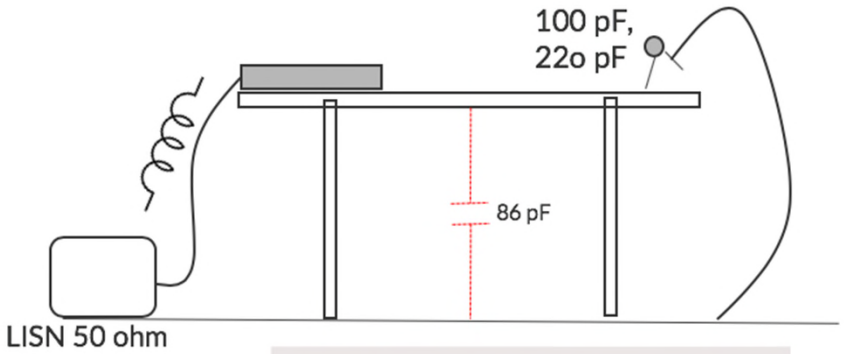
Telcordia GR 1089-CORE does mention growth of systems and allows analysis to prove compliance. GR-1089-CORE references FCC and ANSI C63.4 for emissions testing. Therefore the 2 dB rule applies to GR-1089-CORE.

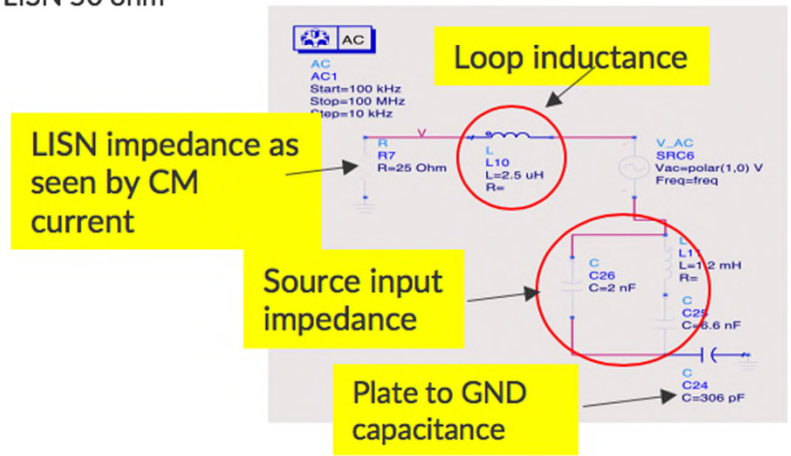
See **Emissions Scaling for Multiple Identical Units**, Jacques Rollins for more information on regulatory requirements

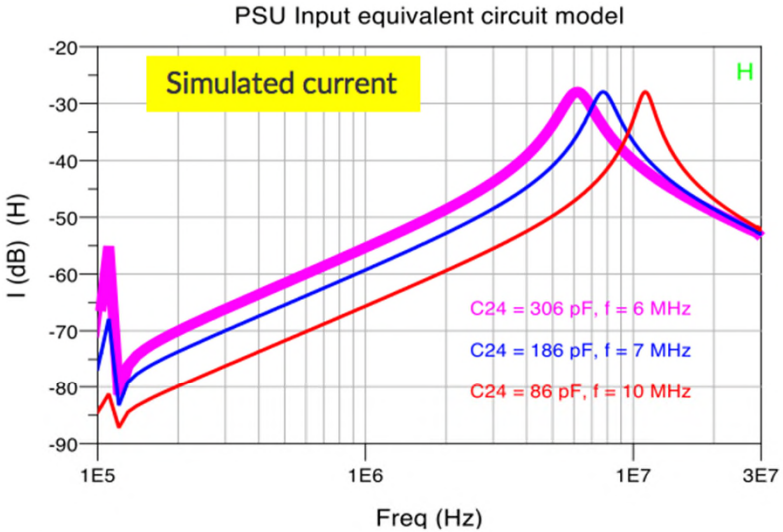


Addition of a third linecard increases emissions by less than 2dB using the 7.5logN (worst case @ JNPR) curve

Setup related emission variation – Plate size/CM return capacitance



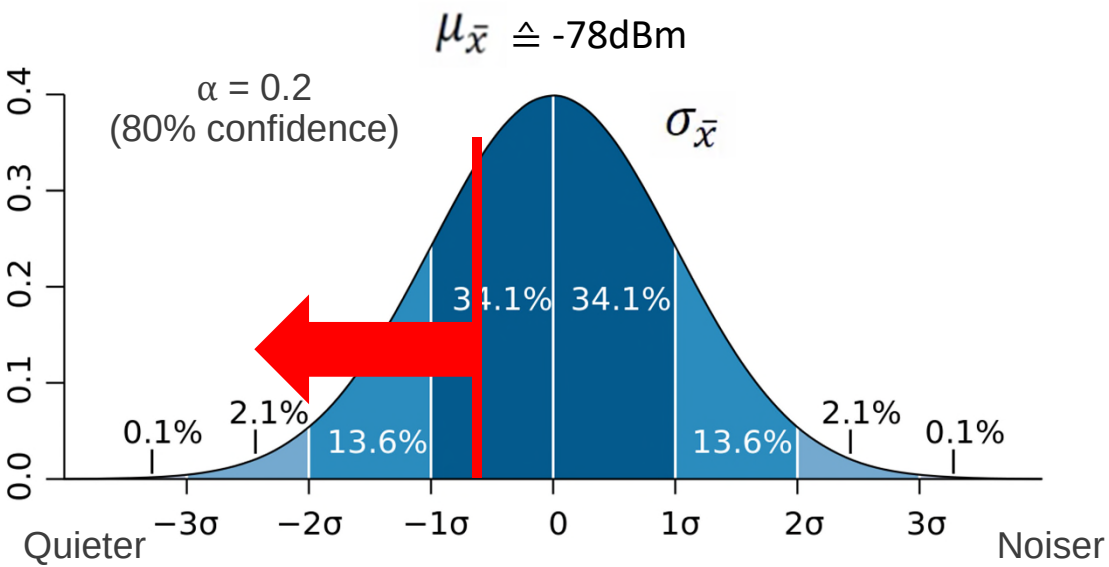




Current clamp and LISN measurement shows a resonance around 10 MHz. The measured resonance of the metal plate to GND is 86 pF, the power cord loop inductance is around 3uH approx. as per the loop size assumed.

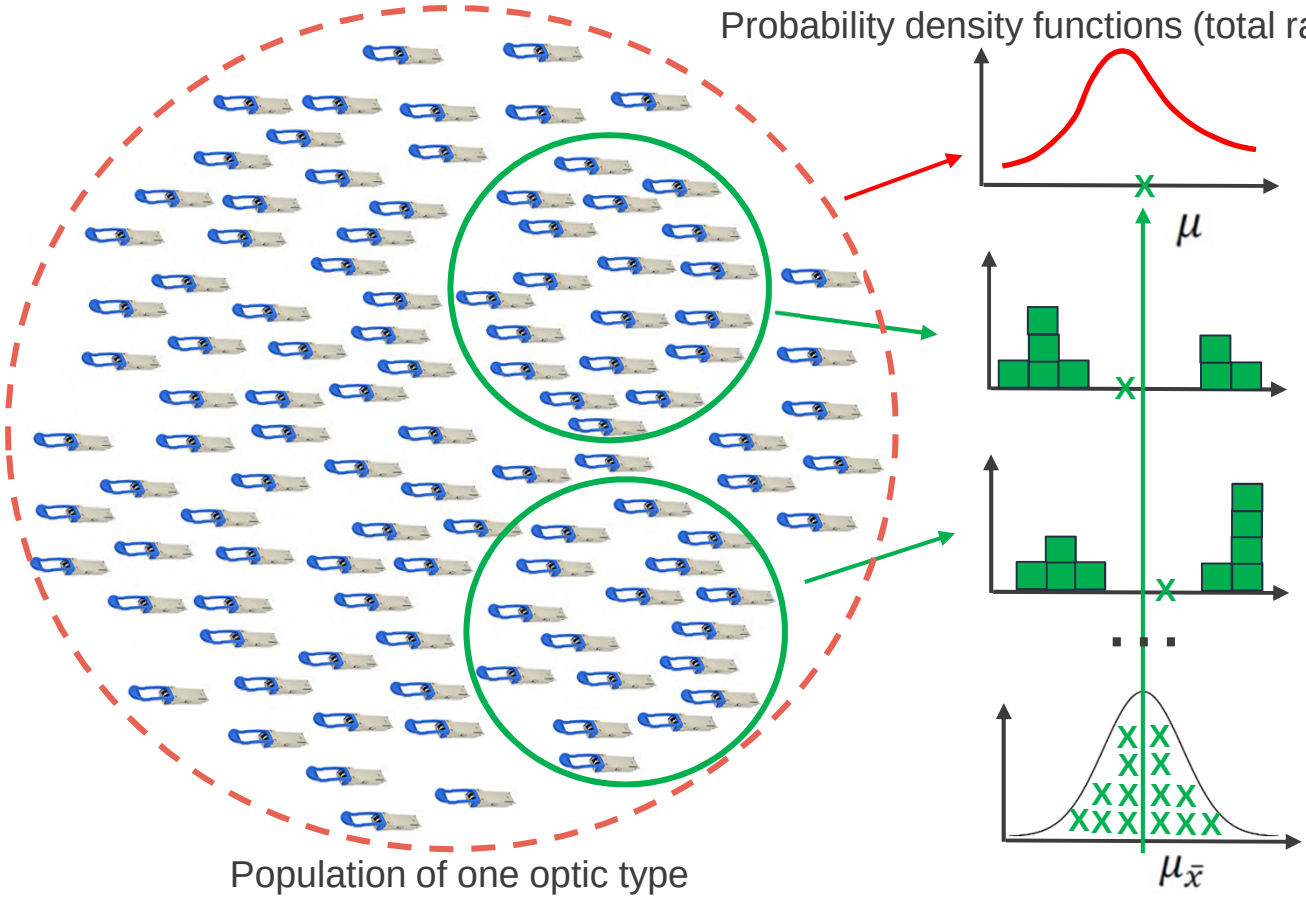
The values are not exact but roughly assumed based on geometry and measurements.

Statistical significance α

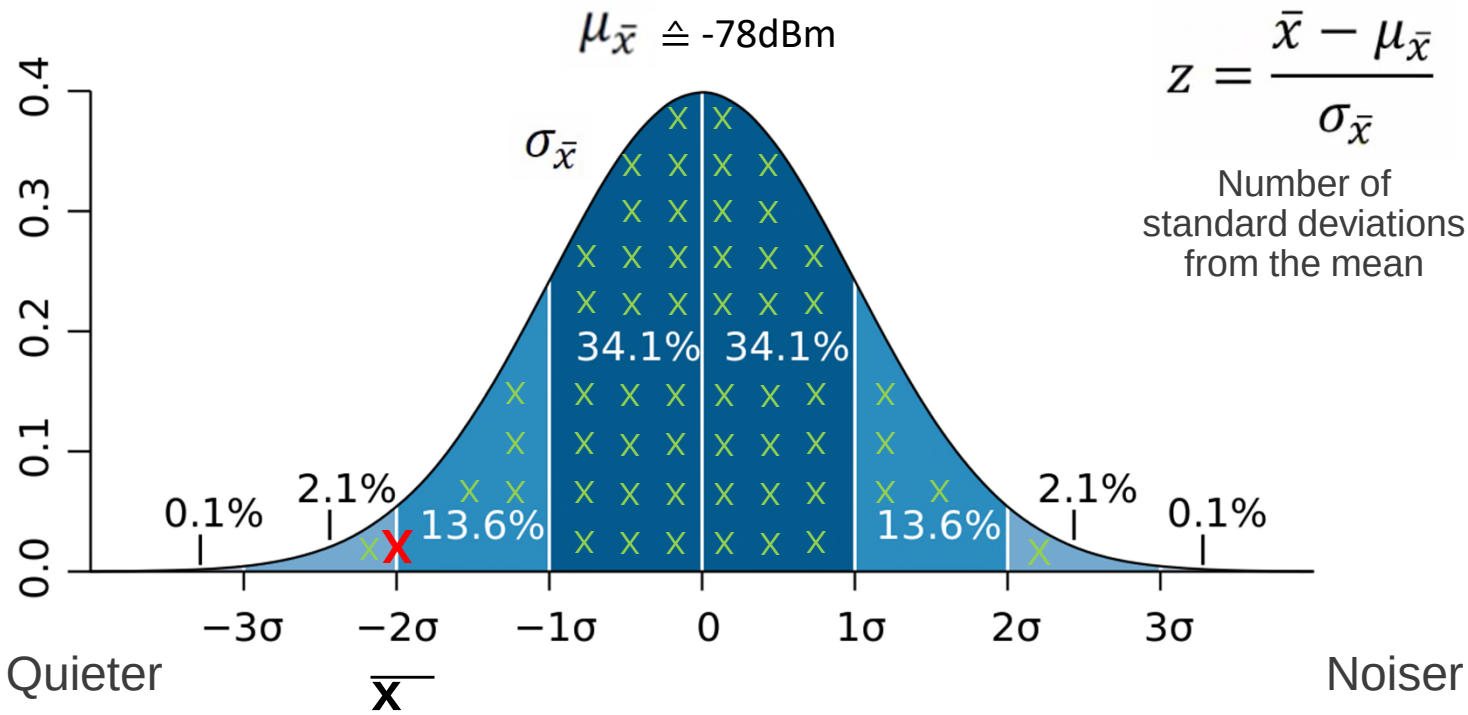


- A statistically significant result is a result that's not attributed to chance
- Selected α = 80% in line with CISPR's 80/80 rule

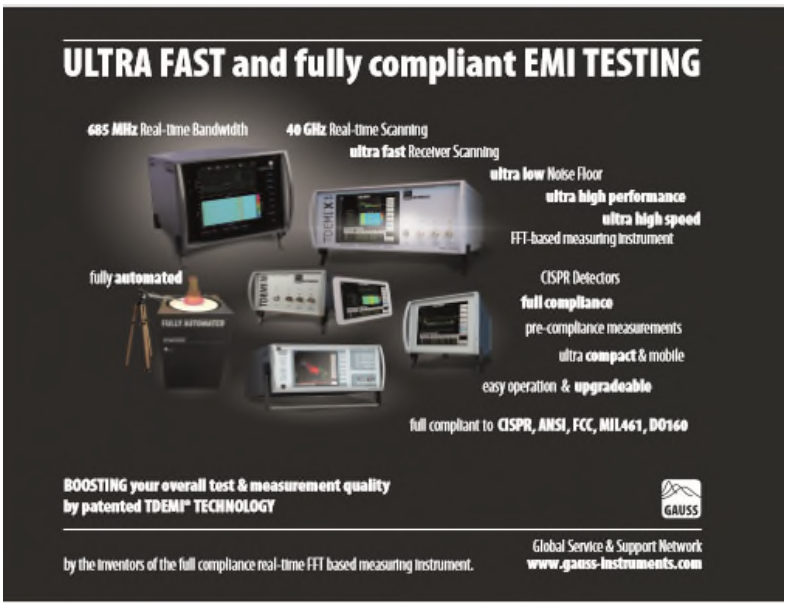
Central Limit Theorem applied to EMC

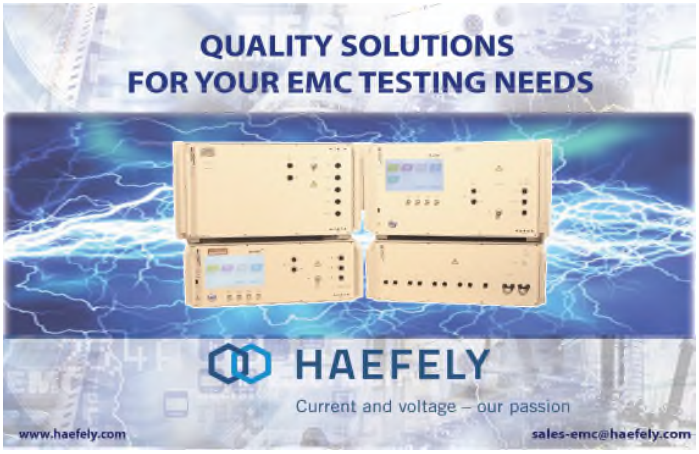


Hypothesis Testing



Example: probability of selecting a sample with mean $\overline{x}$ (denoted by X) two standard deviations the left of the population mean is 2.2% (P-value)





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