Advanced Patterning Techniques for 22nm HP and beyond

An Overview

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Intel Corporation
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IEEE LEOS (Bay Area)
Outline

• The Challenge
• Advanced (optical) lithography overview
• Flavors of 193i
• Double Patterning concepts
• Source Mask Optimization
• Cost of Ownership (COO)
• Summary
Outline

• The Challenge
  – The ‘shrinking’ transistor
  – Imaging & process metrics
  – Resist issues

• Next Generation Lithography (NGL) schemes

• Advanced (optical) lithography overview

• Flavors of 193i

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• Summary
ITRS 2007 Lithography Roadmap

Sub-22nm options
- DPL immersion
- EUV
- Nanoimprint
- ML2
- …
Marching to the beat of “Moore’s Law”

Updated chart from SPIE’06 plenary talk by Y. Borodovsky (Intel)
Outline

• The Challenge
• Next Generation Lithography (NGL) schemes
  – 193 & 193i
  – EUVL
  – E-beam direct-write
  – Nano-imprint
• Advanced (optical) lithography overview
• Flavors of 193i
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Advanced Patterning: Overview

Metrics of success for a litho technology:

- What is the patterning depth of focus?
- What is the process-window?
- What is the cost of ownership?

**Key Topics**

**Next Gen Litho**

- EUV Litho
  - Sub 22nm patterning
  - Reticles
  - Resists
  - Process integration

**Optical Litho**

- Patterning down to 22nm
- 193 immersion extensions
- Source-Mask-Optimization
- Computational Lithography

**Resist / Metro**

- OCD, AFM, CD-SEM calibration
- LWR improvements
- Freezing process
- Dual-tone PR development
Elements of a ‘dry’ optical system

Ultimate resolution depends on:

- **Illumination source**
  - Coherence, OAI, polarization, BW

- **Mask**:
  - Type (APS, BIM, Chrome-less)
  - Edge-effects
  - Polarization

- **Lens**:
  - Flare, Aberration, birefringence

- **Wafer**:
  - Resist
  - LER
  - Flatness
Fundamentals of optical lithography

• Resolution can be improved by:
  – Decreasing wavelength of light source ($\lambda$)
  – Increasing projection optic numerical aperture (NA)
  – Tuning the $k_1$ “knob” using various resolution enhancement techniques (AltPSM, Chrome-less masks), OPC, and source itself

• Guiding equations:
  – Resist CD (image) = $k_1 \times \frac{\lambda}{NA}$
  – Optical Resolution = $\frac{1}{2} \times \frac{1}{1+\sigma} \times \frac{\lambda}{NA}$

• Process metrics
  – Depth of focus
  – Exposure latitude
Process metrics: $k_1$ factor

- Resolution as a function of $k_1$
  - $k_1$ indicates process complexity
  - Lower $k_1$ is achieved by resolution enhancement techniques and improvements in resists

\[
HP = k_1 \frac{\lambda}{NA}
\]

\[
DOF = k_2 \frac{\lambda}{NA^2}
\]
The ‘immersion’ advantage

• Improvement in **Numerical Aperture**
  – \( NA = n_f \cdot \sin(\theta_f |_{\text{Max}}) = n_o \cdot \sin(\theta_o |_{\text{Max}}) \)
  – Increasing the fluid index, improves the captured angles of light that can reach resist
  – Water refractive index at 193nm is 1.44
  – Possible to achieve \( NA \approx 1.35 \) with immersion scanners

• Increased Depth of Focus \((\alpha n_f)^*\)

\[
DOF = k_2 \frac{\lambda}{n_f (1 - \cos \theta_f)} = k_2 \frac{\lambda}{n_f - \sqrt{n_f^2 - NA^2}}
\]

\( NA \) limited by \( \min[n_{\text{glass}}, n_{\text{fluid}}, n_{\text{resist}}, n_{\text{BARC}}] \)

*non-paraxial approx: necessary at high NA
(Ref: Burn Lin, JM3 v1, no.7)
A simple L/S patterning example

• Printing a 65nm CD on 200nm pitch pattern
  – Immersion advantage is clear
• What else can we do?
  – Add scatter bars
  – Optimize illumination
    – Conventional -> Dipole
    – Polarize light
  – Reduce aberrations
  – Improve resist MTF
• Study process margin...
193nm "Wet" Lithography (water)

65/200nm Focus Exposure Matrix

Area = 3.3152  
Center = (0.0, 0.3201)  
X-Diam = 167.2739  
Y-Diam = 0.0252  
Y-Diam% = 7.8822

Process Window
65nm CD / 200nm pitch

Exposure Latitude Percent

Depth of focus (nm)

Aug 4th, 2009: Adv. Lithography for 22nm HP patterning - Yashesh A. Shroff (yashesh.a.shroff@intel.com)
Off-Axis Illumination – case study

• Advantage of setting the right illumination condition
  – We review with the same Line/Pitch = 65/200nm; with
    1. conventional sigma (disk illumination, s=0.7) and
    2. quad-pole, radius=0.2, and displacement=

\[
\frac{\sqrt{2}\lambda}{2 \times p \times NA} = 0.51
\]
OAI – Process Window

- Improved process margin with optimized off-axis illumination
  - Better depth of focus
  - Better exp latitude

![Disk illumination graph](image)

![C-QUAD illumination graph](image)
Low k1 challenge

- Off-axis illumination can get us only so far...
  - k1 limited to > 0.25

\[
\frac{p}{2} = k_1 \frac{\lambda}{NA}
\]

\[
NA_{(\text{max})} = 1.35
\]
\[
k_1(\text{min}) \sim 0.28
\]
\[
\Rightarrow p_{(\text{min})} \sim 80 \text{ nm}
\]

Low k1: 0.5 > k1 > 0.25

Only 2 diffracted orders form image at wafer plane

k1 < 0.25

Only 1 diffracted order captured
No modulation at wafer plane
### k1 scaling roadmap for lithography

<table>
<thead>
<tr>
<th>ITRS Year</th>
<th>Half Pitch</th>
<th>k1 Factor</th>
<th>ArF (193 nm)</th>
<th>EUV (13.5nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2010</td>
<td>45nm</td>
<td>0.92</td>
<td>1.30</td>
<td>1.55</td>
</tr>
<tr>
<td>2010</td>
<td>40nm</td>
<td>0.21</td>
<td>0.30</td>
<td></td>
</tr>
<tr>
<td>2013</td>
<td>32nm</td>
<td>0.15</td>
<td>0.22</td>
<td>0.26</td>
</tr>
<tr>
<td>2016</td>
<td>22nm</td>
<td>0.15</td>
<td>0.18</td>
<td>0.19</td>
</tr>
<tr>
<td>2019</td>
<td>16nm</td>
<td>0.15</td>
<td>0.30</td>
<td></td>
</tr>
</tbody>
</table>

- **Double patterning / pitch-splitting**
- **High-index immersion fluid research halted**
- **NA >0.30 required**

Source: Nikon (LithoVision 2009)
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• Next Generation Lithography schemes
• Advanced optical lithography overview
• Flavors of 193\textit{i}
  – SE, DE
• Double Patterning concepts
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SE / DE process flow chart

ArF Single Exposure
- Deposit Hardmask(s)
- Coat, expose, develop
- Transfer to hardmask
- Transfer to IC layer
- Remove hardmask

Double Exposure
- Deposit Hardmask(s)
- Photoresist exposure 1
- Photoresist exposure 2
- Photoresist develop
- Transfer to hardmask
- Transfer to IC layer
- Remove hardmask
- Remove hardmask
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  – Techniques
  – Overlay challenge
  – Resist challenge
  – Tool status
  – Modeling results
  – Adoption timeline & key challenges summary
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A word about DPL

• Leading candidates:
  – LELE: Final pattern created in two separate, interdigitated litho/etch steps
  – Spacer: Self-aligned sacrificial pattern used to create a final pattern after deposition of sidewall spacers on it. Requires one critical litho+etch step for sacrificial pattern followed by 1 or 2 more L/E using trim masks (less critical)
  – LFLE: Resist freeze process; Huge amount of interest in 2008-09 from resist suppliers & now a leading candidate DPL technology
    – Best for Bright Field (transistor gate) layers

• Issues
  – Resist pattern collapse is becoming a critical issue
  – Overlay / CDU improvements needed faster than Moore’s law scaling of minimum feature size
Litho Etch Litho Etch Double Patterning

**LELE (line)**

1. Etch hardmask 2, Strip resist
2. Coat, expose, develop
3. Etch hardmask 1
4. Remove resist and hardmask

**LELE (trench)**

1. Etch hardmask, Strip resist
2. Coat, expose, develop
3. Etch hardmask 1, Remove resist
4. Remove hardmask 2
Litho Options Summary

ArF SE
- Deposit Hardmask(s)
- Coat, expose, develop
- Etch hardmask, Strip resist
- Coat, expose, develop

LELE (line)
- Deposit spacer, Etch back spacer
- Remove hard-mask lines

LFLE (Freeze)
- Etch hardmask

DPL
- Coat, expose, develop

Spacer

EUV
- Deposit spacer, Etch back spacer

Schematic design courtesy: A. Hazelton, Nikon

Aug 4th, 2009: Adv. Lithography for 22nm HP patterning - Yashesh A. Shroff (yashesh.a.shroff@intel.com)
Comparative analysis of DPL techniques

- **LELE (Litho Etch / Litho Etch):**
  - Requires tight overlay, additional etch steps

- **LFLE (Litho Freeze Litho Etch)**
  - Track based process change to “freeze” resist from developing during 2nd exposure

- **Spacer Based ➔ Current favorite**
  - Thin film deposition after exposure.
  - Etch process = initial pitch/2
  - CD and CD uniformity determined by thin film/etch uniformity
The problem with conventional way of thinking about "Double Exposure"

Requires a development step between exposures (~double imaging)

Can we do DE without removing the wafer from the chuck?

At minimum pitch resolution capability of the optics, two ‘offset’ exposures yield will zero contrast.

\[ I = \cos^2(p\times x / \text{pitch}) + \sin^2(p\times x / \text{pitch}) = 1 \]
Effective $k_1<0.25$: Pitch splitting

- Sub-0.25 $k_1$ factor is achieved both at the layout end & process end.
- CAD products from Synopsys, Mentor have started including GDS split along with OPC, flare packages

Source: Wallow, GF
CD uniformity is not so simple with DP

1st exp.
- Overlay error

2nd exp.
- CD error
- Position error

Overlay error → Space CD error
CD error → Space position error
CD and overlay for DP

- CD difference in the two patterning steps is important – overall increase in CD non-uniformity.
- Likewise, overlay is important too.

\[
\Delta CD_{line} = \sqrt{\Delta CD^2 + \left[\frac{3}{2} (\bar{L}_1 - \bar{L}_2)\right]^2}
\]

\[
\Delta CD_{space} = \sqrt{\left(\frac{\Delta CD^2}{2}\right) + (\Delta OL_{line}^2) + [3(\bar{m}_1 - \bar{m}_2)]^2}
\]

Ref: Model created by A. Hazelton; Verified experimentally by CET/LETI-Nikon
Double Patterning examples from industry

- **40nm** HP with $k_1=0.2$ achieved with **0.93 NA 193nm tool using double patterning** (B. Arnold, ASML)

- **32nm** HP with $k_1=0.14$ achieved with **0.8NA dry 193nm tool using double patterning** (CEA-LETI/Nikon)

- **20nm** HP with $k_1=0.135$ achieved with **1.30 NA 193nm tool using double patterning** (LithoVision 2009, Nikon)
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  – Computing our way through
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Masks

• 193nm Mask Considerations:
  – Model-based Optical Proximity Corrections for mask patterns = long write times & demand for faster turn-around
  – Multiple masks for double patterning could have hidden costs
    – 50% increase in mask cost + 50%+ adder for Double Pattern Lithography
    – Overlay of multiple masks a challenge
  
  – Source-Mask-Optimization (SMO)
    – Constrained optimization to reduce k1 factor.
    – Use of pixilated sources significantly improves process window
Source-Mask-Optimization (SMO)

Solving the Inverse “Hopkins” Equation

- Brickwall structure,
  - NA=1.2, \( \lambda = 193\text{nm} \), CD=45nm, P=90nm \( (k_1=0.28) \)

Ref: M. Dusa (ASML)
Source-Mask-Optimization in Practice

- Simultaneous optimization of illumination & mask features
- Following example shows capability to achieve $k_1 = 0.29$ with $l = 248\text{nm}$, $NA = 0.8$, 90nm HP

Ref: Kim, SPIE vol. 5754 (‘05)
Resists

- A lot of work to optimize resists for pitch division from major suppliers: JSR and TOK
- resolution of 193nm chemically amplified resists has not yet hit a wall to at least 20nm
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## Tool cost v/s throughput

<table>
<thead>
<tr>
<th></th>
<th>45 nm HP</th>
<th>22 nm HP</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>ArFi SE</td>
<td>ArFi DPL</td>
</tr>
<tr>
<td></td>
<td>LELE</td>
<td>LLE</td>
</tr>
<tr>
<td>throughput (wph)</td>
<td>125</td>
<td>200</td>
</tr>
<tr>
<td>tool price</td>
<td>$40M</td>
<td>$52M</td>
</tr>
<tr>
<td>consumables (/year)</td>
<td>$3.4M</td>
<td>$5.0M</td>
</tr>
<tr>
<td>reticle cost per layer (rigorous model)</td>
<td>$200k</td>
<td>$1166k</td>
</tr>
<tr>
<td>reticle cost per layer (CW model)</td>
<td>$200k</td>
<td>$600k</td>
</tr>
</tbody>
</table>

Source: A. Wüest, A. Hazelton, SPIE 7271
22nm HP Cost of Ownership

- COO is the driving factor behind technology insertion

- Driven by many factors:
  - # wafers / mask
  - Mask / resist cost
  - Technology maturity
  - ...

- Compared to 45nm SE using 193nm, EUV at 22nm HP is best;

- Due to its larger volume than logic, memory will likely adopt DPL more aggressively than logic IC manufacturers.

Source: A. Wüest, A. Hazelton, SPIE 7271
Immersion scanners

• ASML & Nikon provide custom illumination schemes
  – Many aspects of computational litho increasingly feasible
  – JD with Mentor, Toshiba, IBM

• 1270 leading tools:
  – Nikon’s S620, 90W source, Q4 2009
  – ASML’s NXT1950i, 60W source, Q2 2009

• Immersion readiness:
  – Moving into production phase with equivalent expected quality as dry lithography
  – No ‘simple’ ArF pitch-division solution <20nm HP
Competing Next Gen Litho Candidates

EUV (13.5nm light source):
- All reflective optics
- Key issues
  - Light source power
  - Reticle defects
- Promise:
  - Capability of <16nm L/S

Nanoimprint lithography
- No optics!
- Key issues
  - Template defects
  - Low throughput
- Promise:
  - Capability of <11nm L/S
  - Targets SSD & memory
- Toshiba: 2nm LER, 1nm ΔCD @ HP = 20nm
Maskless technologies

- **Mapper (E-Beam direct write)**
  - <25m spot size
  - 2.25nm grid
  - 1.3 x 1.3 m² tool footprint

- **Projection Maskless Lithography**
  - 5mm/s scan α-tool developed
  - 0.26M beams (10M needed)
  - Currently, at 32nm node, they can write one 25mm² die in 30mins (with 43k beams).
Overall DP assessment

Memory Manufacturers lead these developments and have put them to use in production

LELE/LFLE/Spacer techniques have really matured over the past year
• Spacer based DP in manufacturing in memory
• Resist mfg are working on multiple Litho Freeze techniques
• Maintaining process window is going to be hard in volume production

Computational litho/Mask/illumination optimization
• Requires excellent OPC models, understanding of scanner capability
• Mask cost could be barrier for many markets
• Computational litho is a focus area for IBM and the IBM Alliance

Focus on DfM, strong OPC/RETs, with good research programs on litho tool friendly technologies like LFLE are necessary.

Finally, challenges / advantages for each DP technique for logic and memory will be different, so it will be interesting to see how each strain of DP will evolve.
Acknowledgements

This talk would not have been possible without insights gained from several leading lithographers in the industry. In particular, thanks to teams from ASML, IMEC, Nikon, JSR whose published work has been used to highlight the development track of 193i Double Patterning techniques.

Modeling work has been done using Panoramic Technology’s Hyperlith EM-Suite software which provides very good rigorous 3-D E-M simulation TCAD capability.