5.5: A 3.2 to 4GHz, 0.25μm CMOS Frequency Synthesizer for IEEE 802.11a/b/g WLAN

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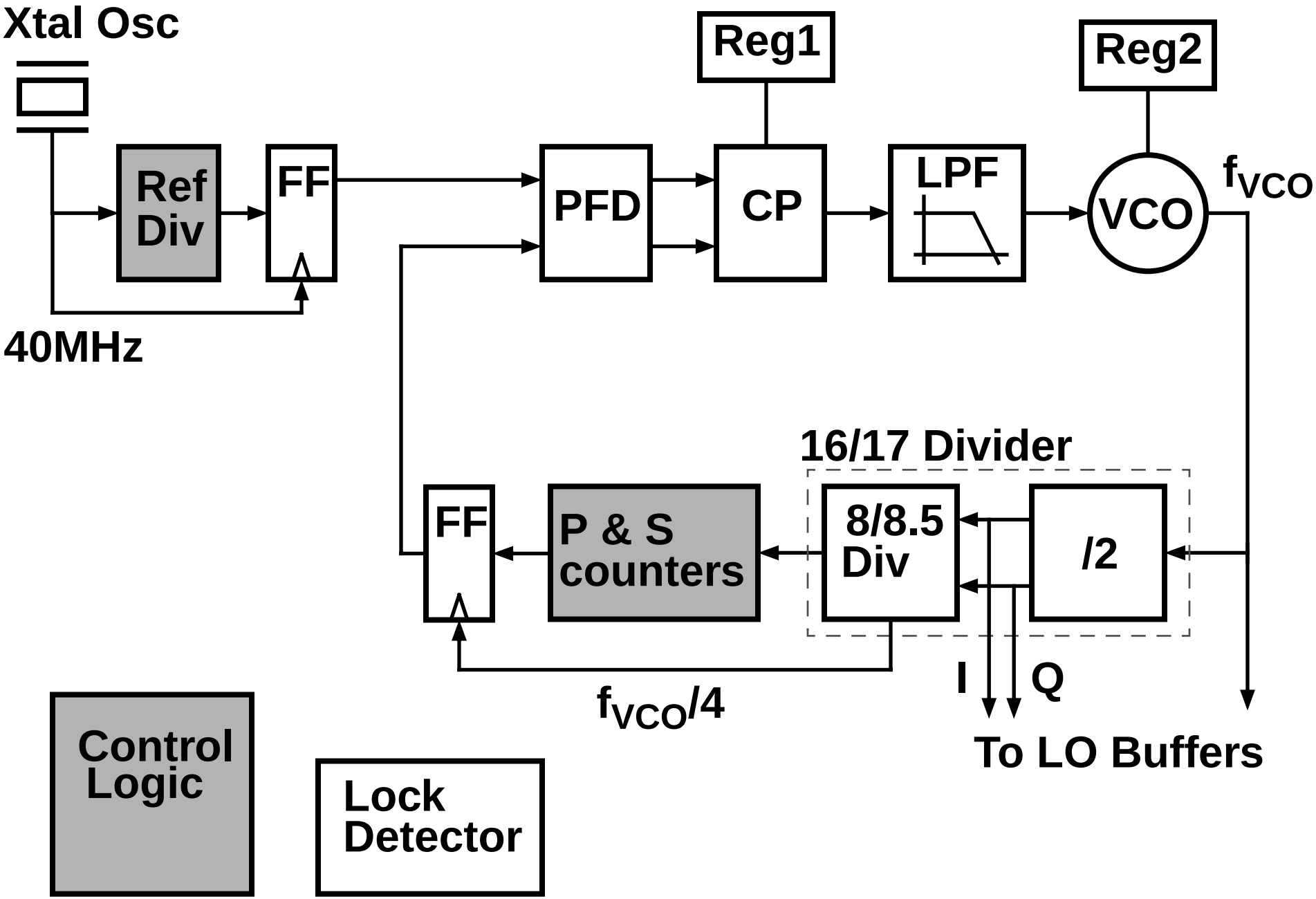
Outline

- System Requirements
- Architecture and Circuit Description
- Measurements
- Conclusions

Design Goals

- Tuning Range 3.2 - 4.0 GHz
- Reference Frequencies:
  13.33M, 6.66M, 3.33M, 10M
- Drive LO Buffers at f_{VCO} and
  I,Q LO Buffers at $f_{VCO}/2$
- Low Phase Noise
- Low Spurs

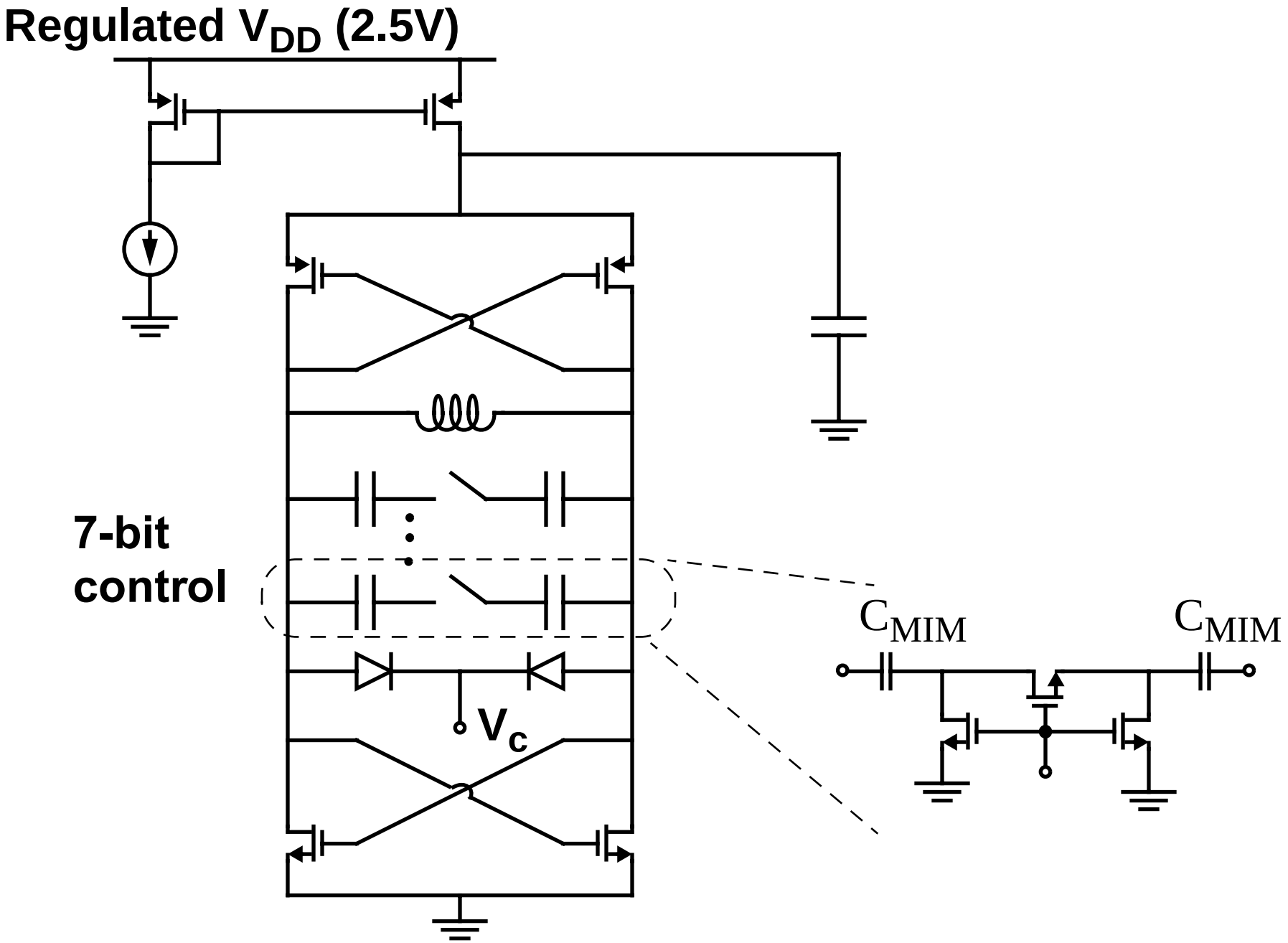
Synthesizer Block Diagram



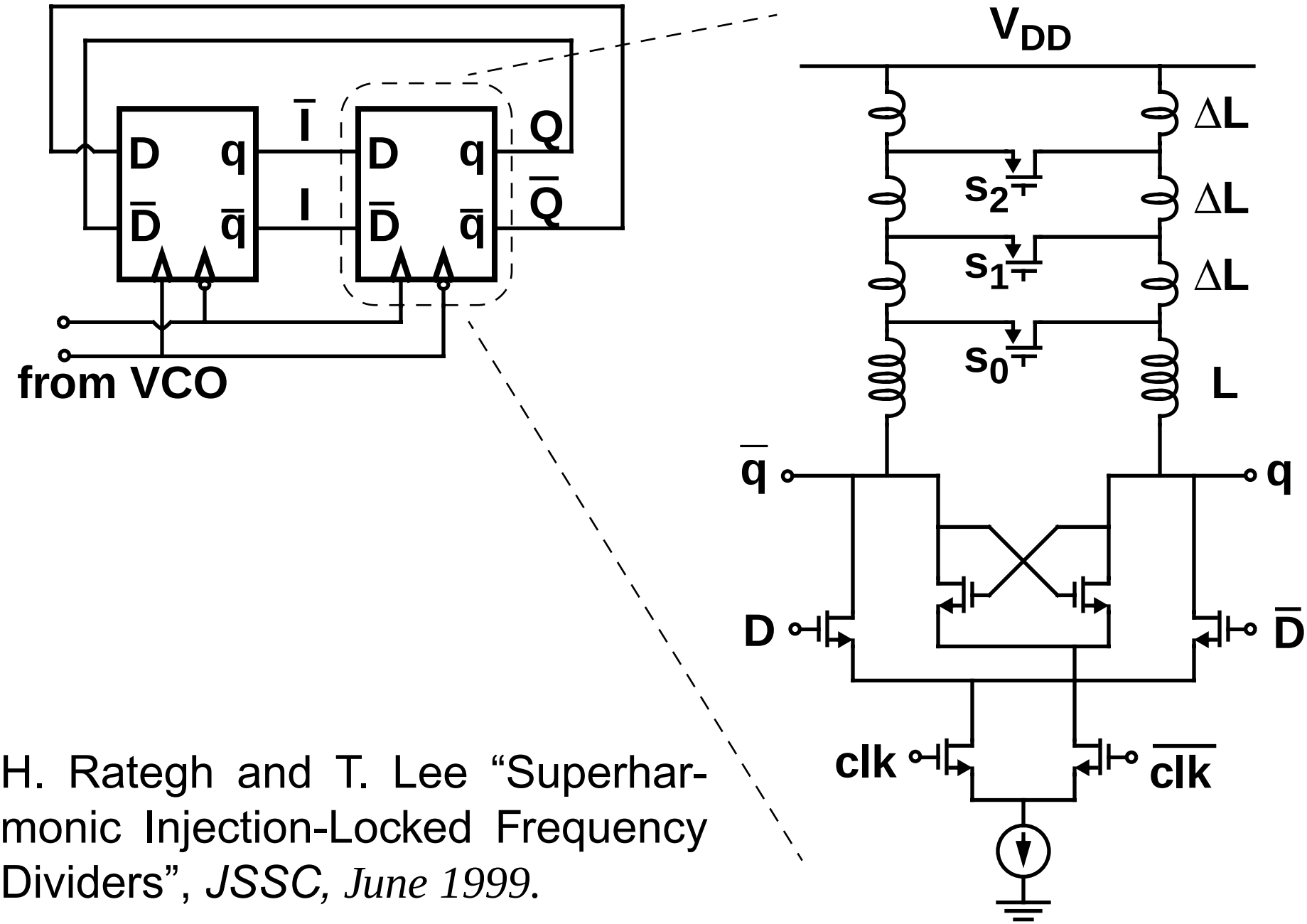
Design Choices

- **Low VCO gain**
  - Good VCO phase noise
  - Low LPF resistor noise contribution
- **High charge pump current**
  - Low LPF resistor noise contribution
  - Low charge pump noise

Voltage Controlled Oscillator (VCO)



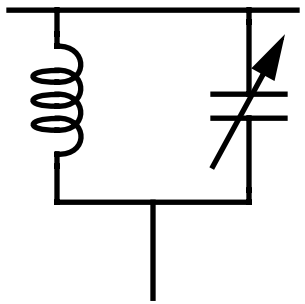
High-Frequency Divide-by-2



H. Rategh and T. Lee “Superharmonic Injection-Locked Frequency Dividers”, *JSSC, June 1999*.

Adjustable Tuning

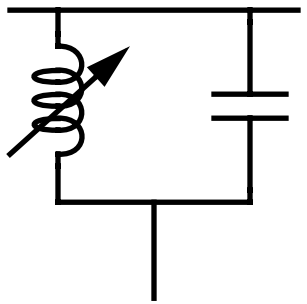
Adjustable C

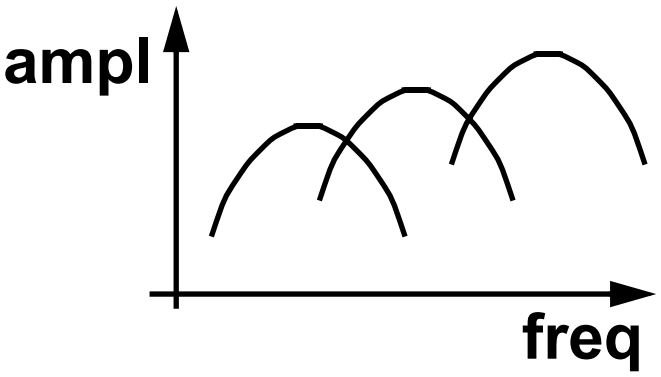


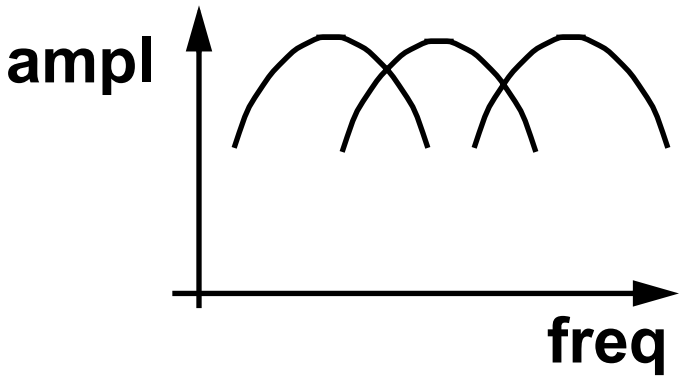
$R_p = L\omega Q$

Equivalent parallel resistance

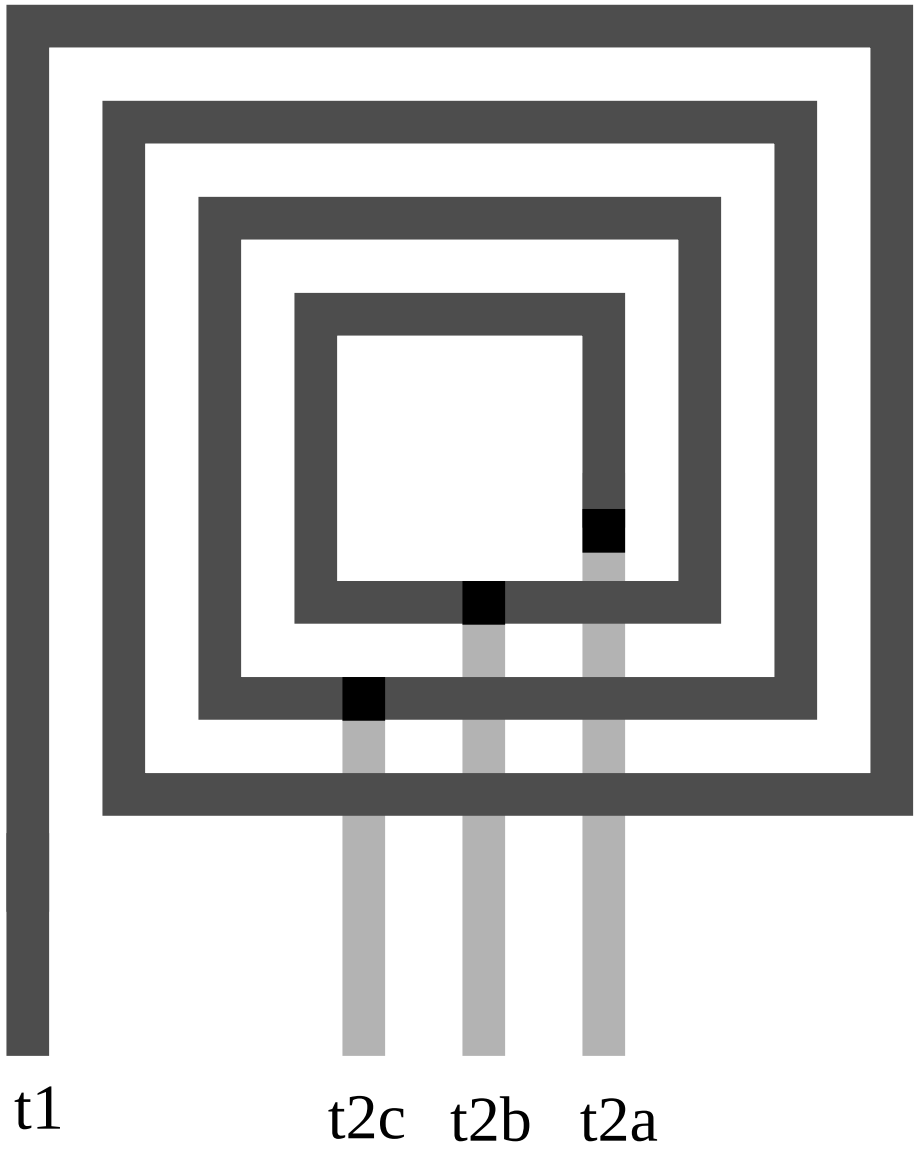
Adjustable L



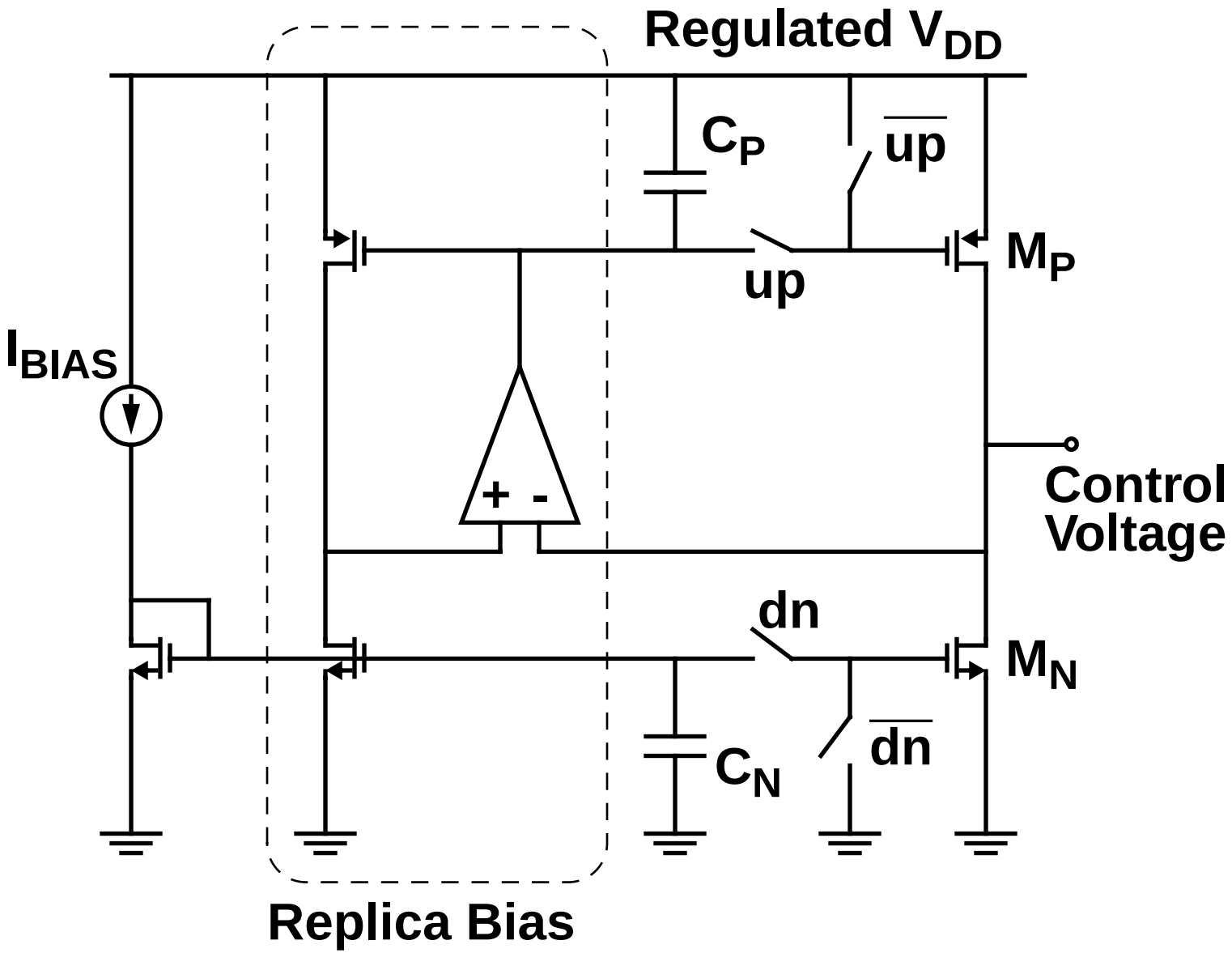




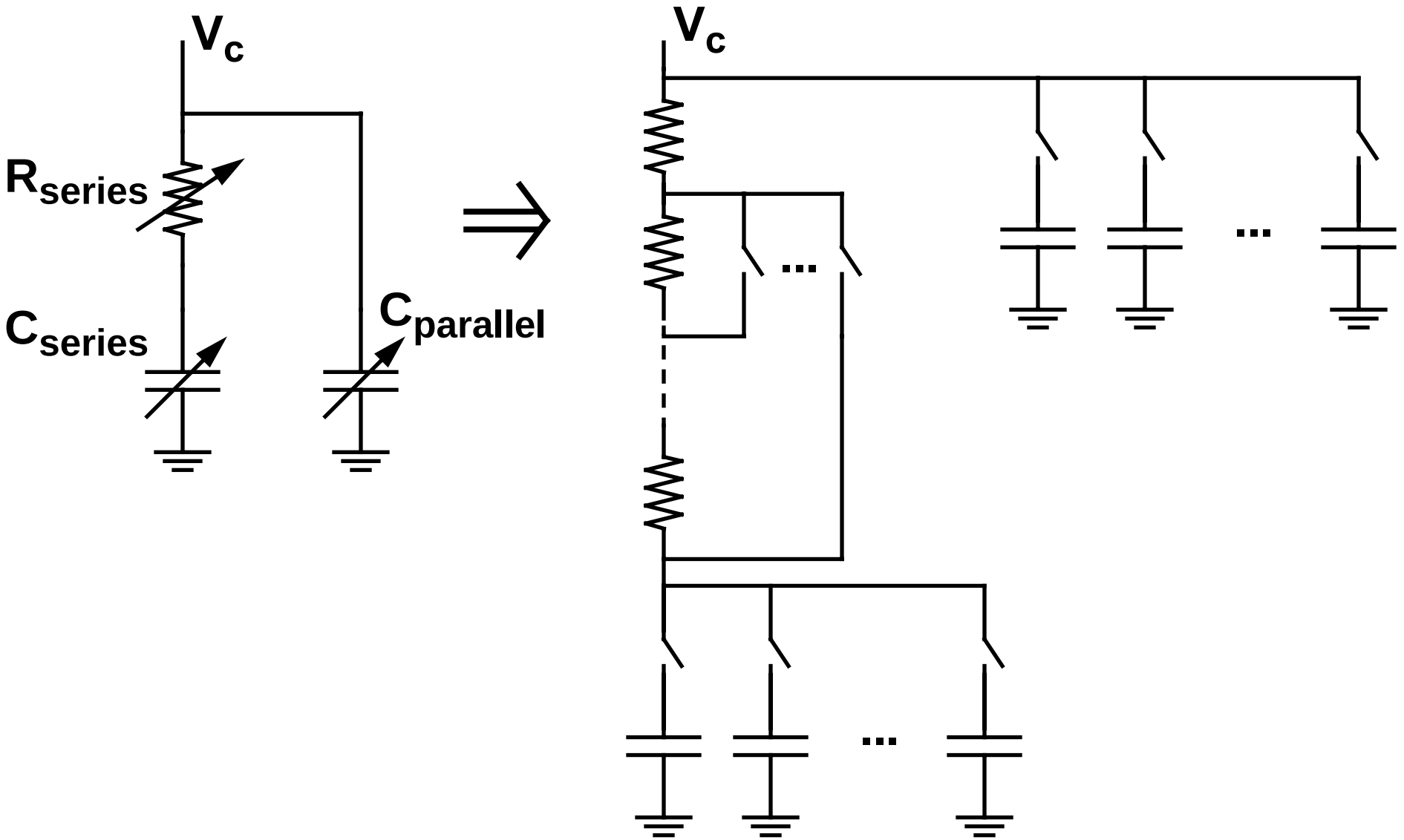
Multi-tap Inductors



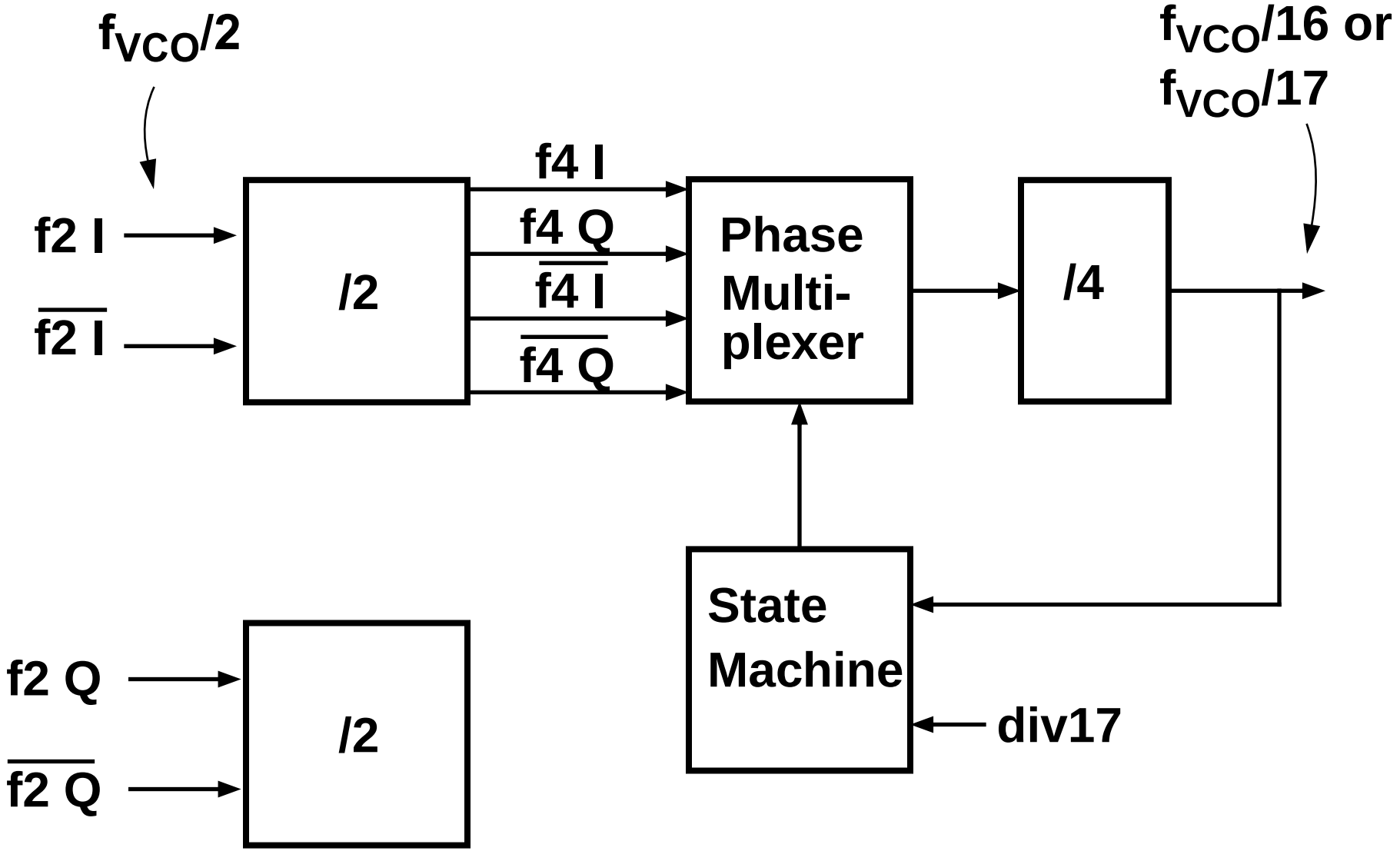
Charge Pump


Regulated V_{DD}
C_P
$\overline{up}$
up
M_P
I_{BIAS}
+ -
Control Voltage
dn
M_N
C_N
$\overline{dn}$
Replica Bias

Programmable Integrated LPF

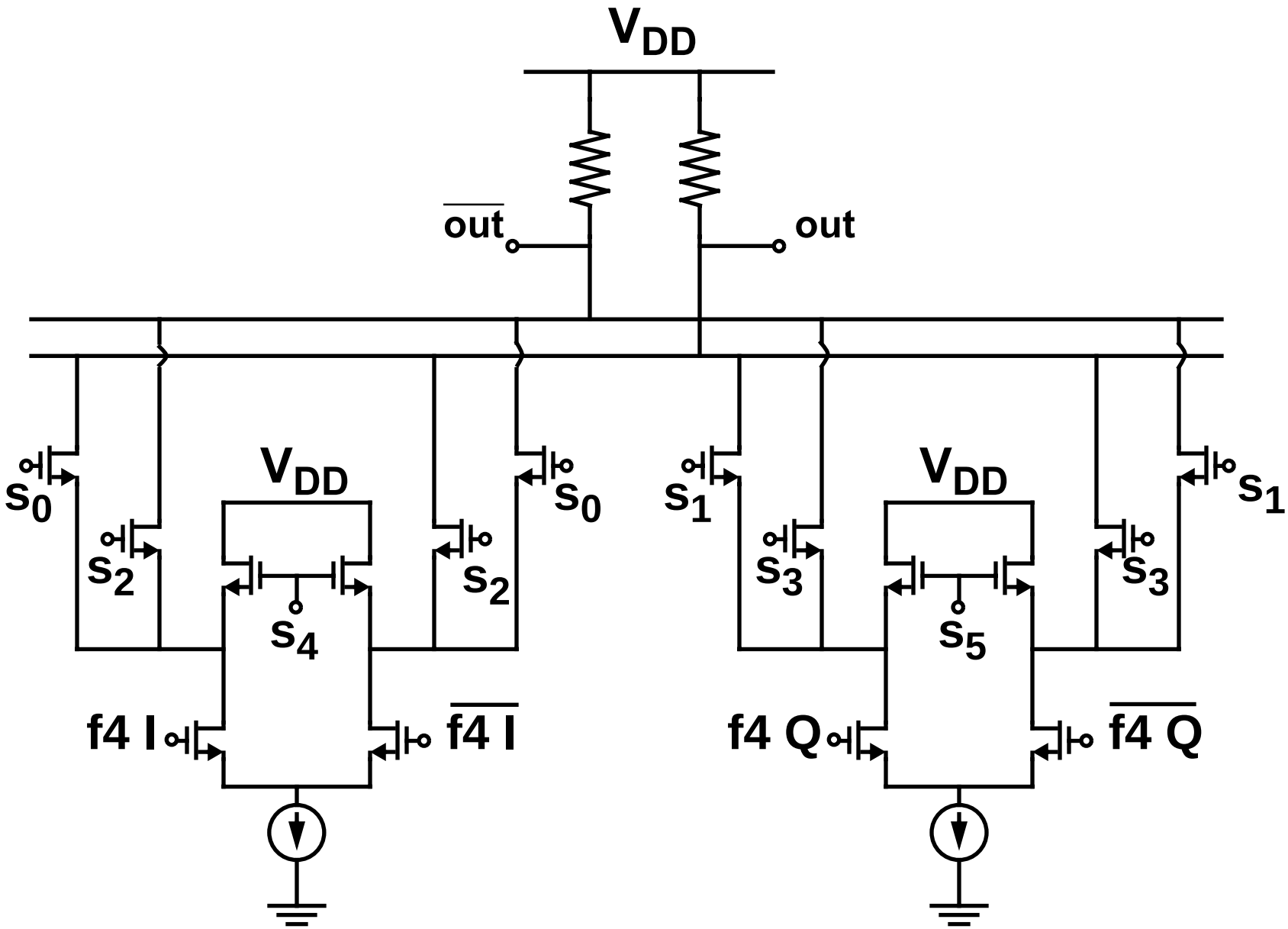


8/8.5 Dual Modulus Divider



J. Craninckx, M. Steyaert “A 1.75-GHz/3-V Dual-Modulus Divide-by-128/129 Prescaler in 0.7-μm CMOS”, *JSSC, July 1996*.

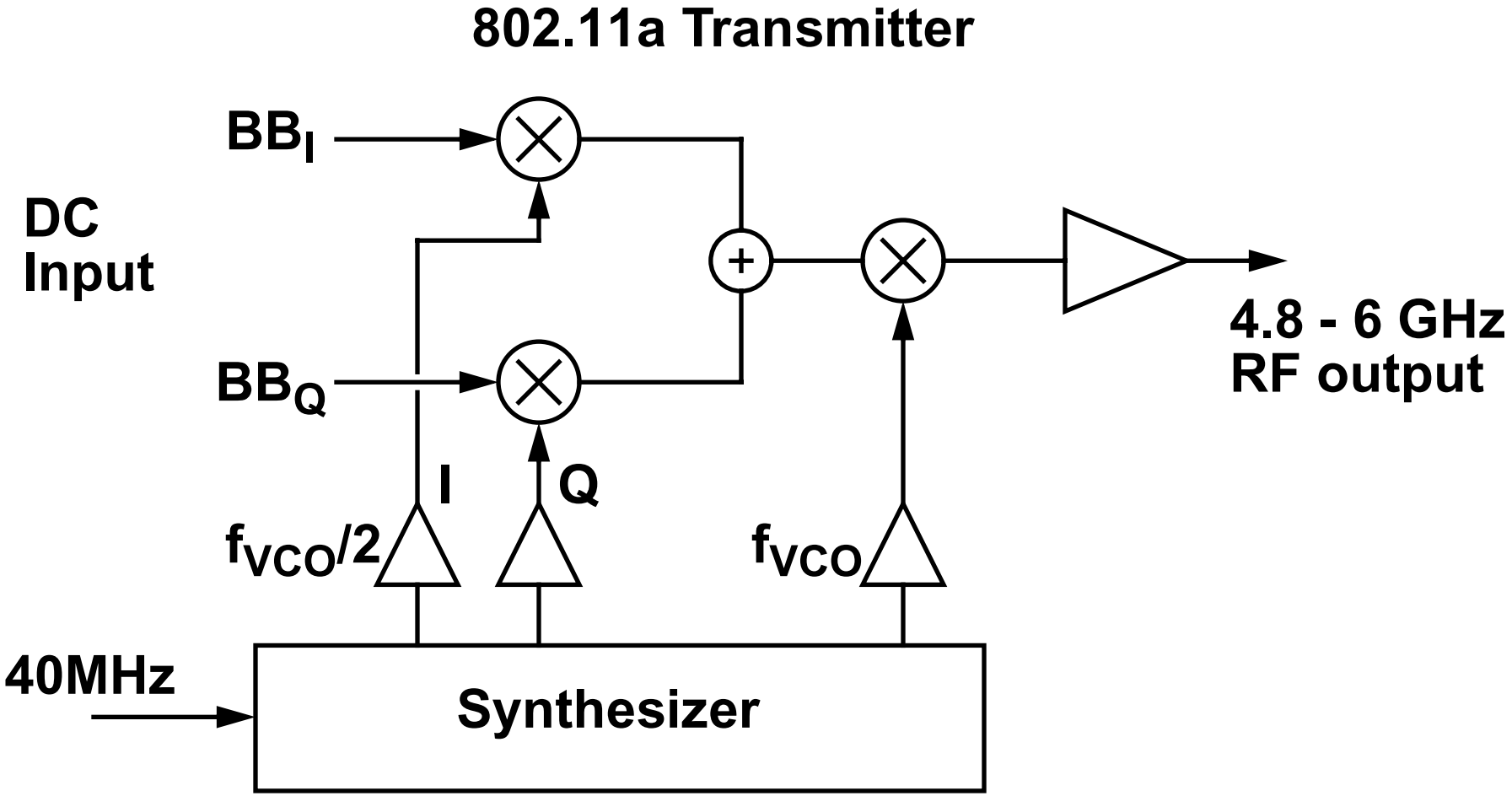
Phase Multiplexer



Control Logic

- Successive approximation search for the 7 bits that control the VCO tuning capacitors
- Coarse digital alignment of the feedback clock with the reference clock
- Optimize for the control voltage value
- Take corrective action when the control voltage drifts out of the acceptable range or when no-lock is detected

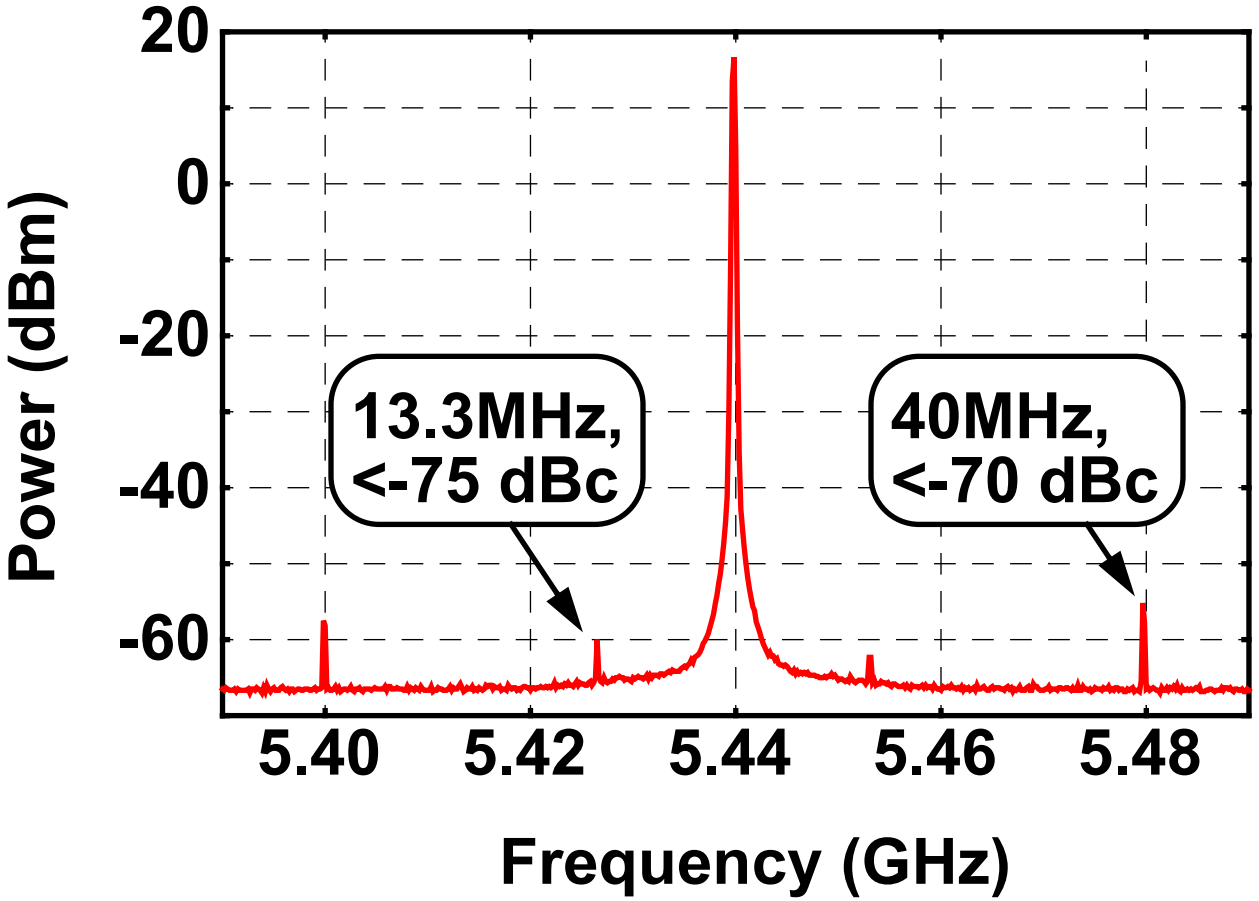
Measurement Setup



- Measured Phase Noise at RF output is ~3.5 dB higher than at the VCO frequency.

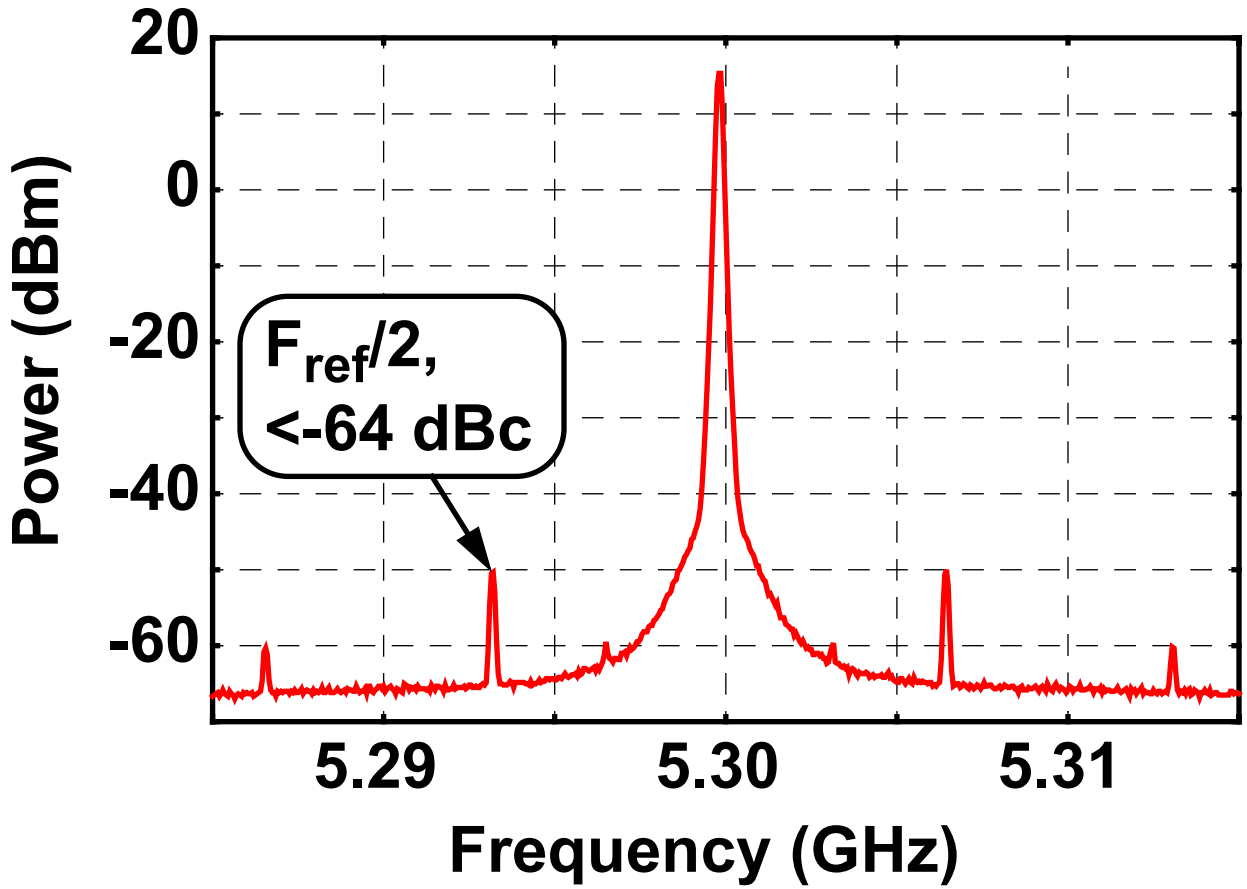
Output Spectrum (1)

F_o=5.44GHz, F_{ref}=13.3MHz, (S=0)



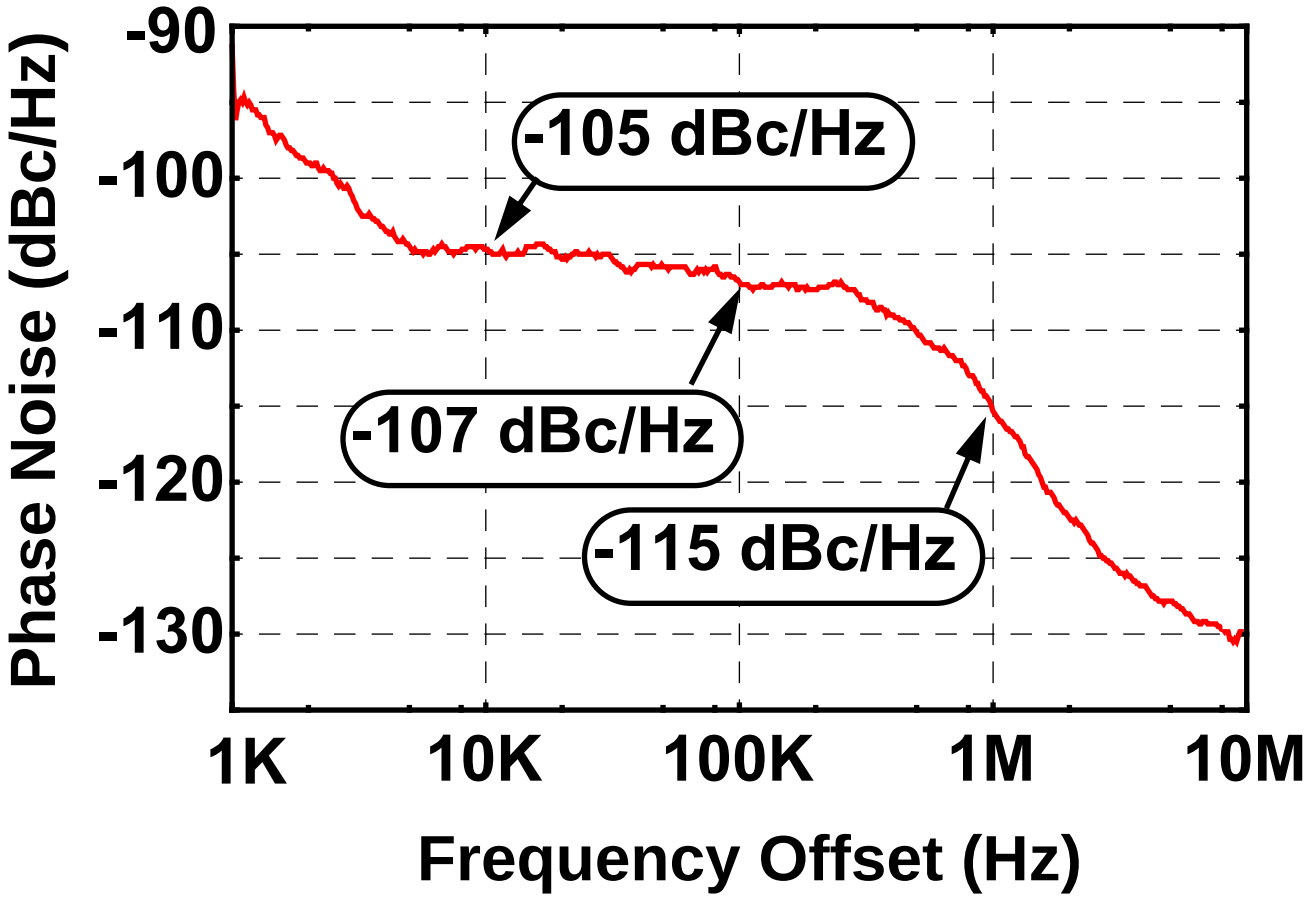
Output Spectrum (2)

F_o=5.30GHz, F_{ref}=13.3MHz, (S=9)



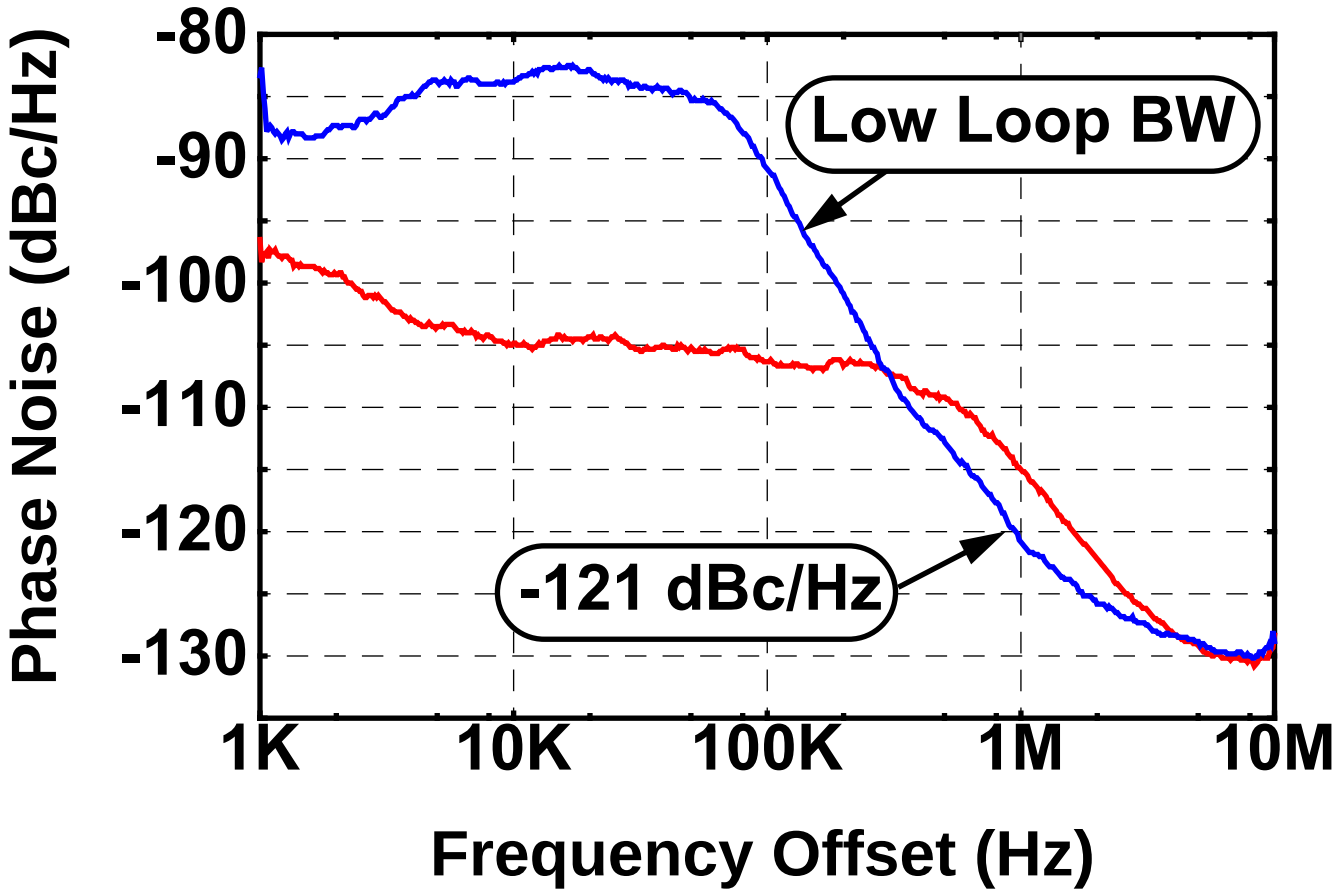
Measured Phase Noise (1)

F_{out}=5240MHz, F_{ref}=13.3MHz



Measured Phase Noise (2)

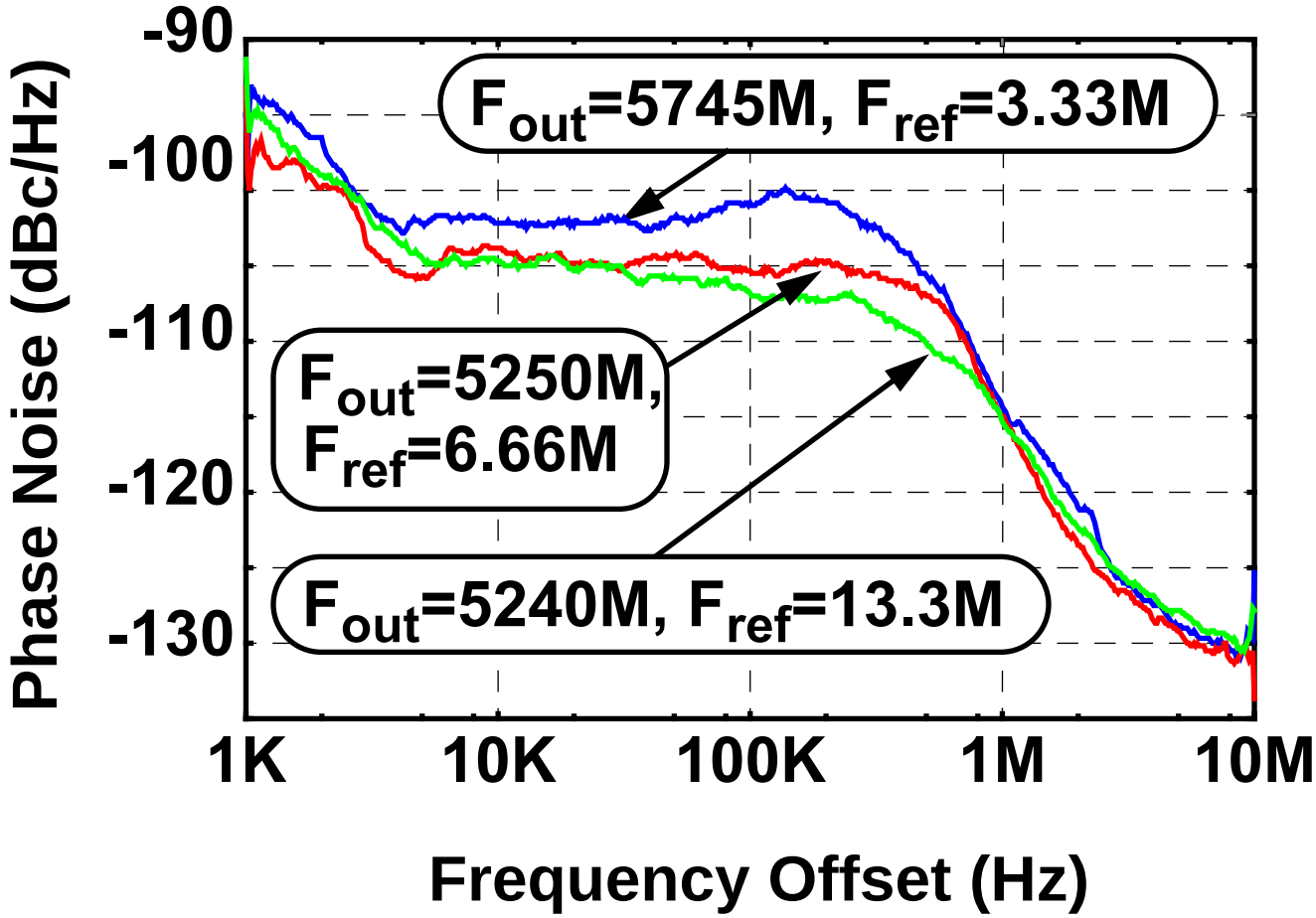
F_{out}=5240MHz, F_{ref}=13.3MHz



VCO Phase Noise: -121 dBc/Hz

@ 1MHz offset, 5.24 GHz carrier

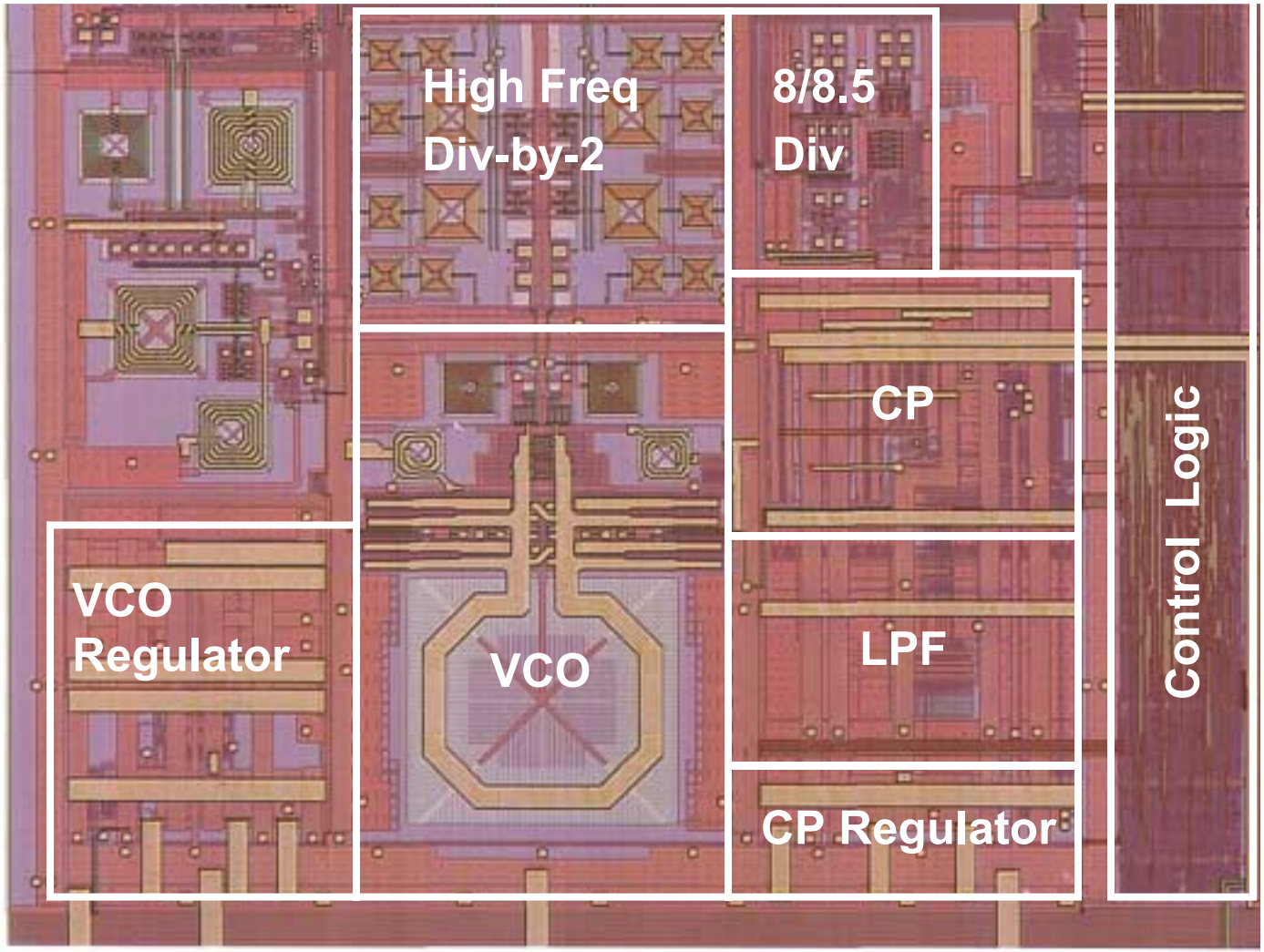
Measured Phase Noise (3)



Performance Summary

Technology	0.25 μm CMOS, 1P5M, MIM capacitors
Power Dissipation	93 mW
Area	1.7 mm^2
Spot Phase Noise F_{out}= 5240MHz, F_{ref}=13.3 MHz	-105/-107/-115 dBc/Hz @ 10K/100K/1M
Integrated PN (from 1K to 10M) F_{out}= 5240MHz, F_{ref}=13.3 MHz F_{out}= 5250MHz, F_{ref}=6.66 MHz F_{out}= 5745MHz, F_{ref}=3.33 MHz	 -45.3 dBc (0.31°) -43.3 dBc (0.40°) -40.9 dBc (0.54°)
Spurs	<-64dBc
Settling Time	<150μs

Synthesizer Micrograph



Conclusions

- **Fully integrated, wideband, 0.25μm CMOS synthesizer**
- **Excellent phase noise, spur performance and settling time**
- **Design highlights:**
  - **On-chip voltage regulation**
  - **Tuning with switching inductors**
  - **Low noise VCO**
  - **Charge pump topology**

Acknowledgment

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