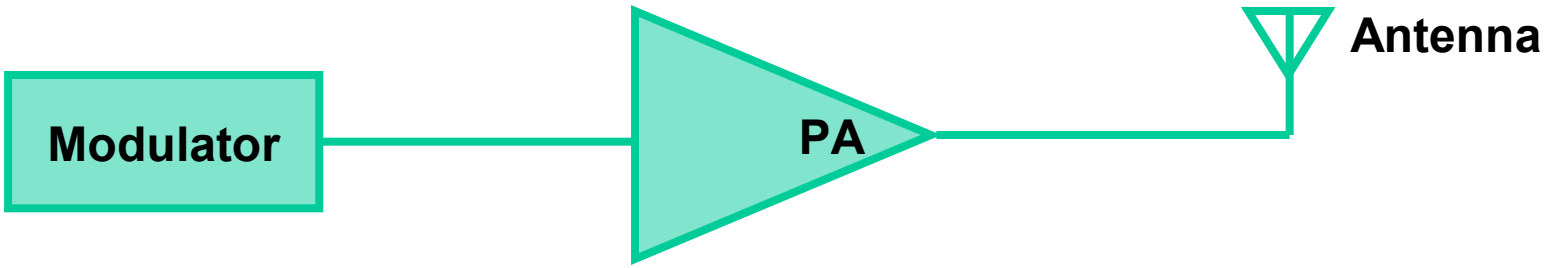
A Digitally Modulated Polar CMOS PA with 20MHz Signal BW

Amirpouya Kavousian

Stanford University

RF Power Amplifiers



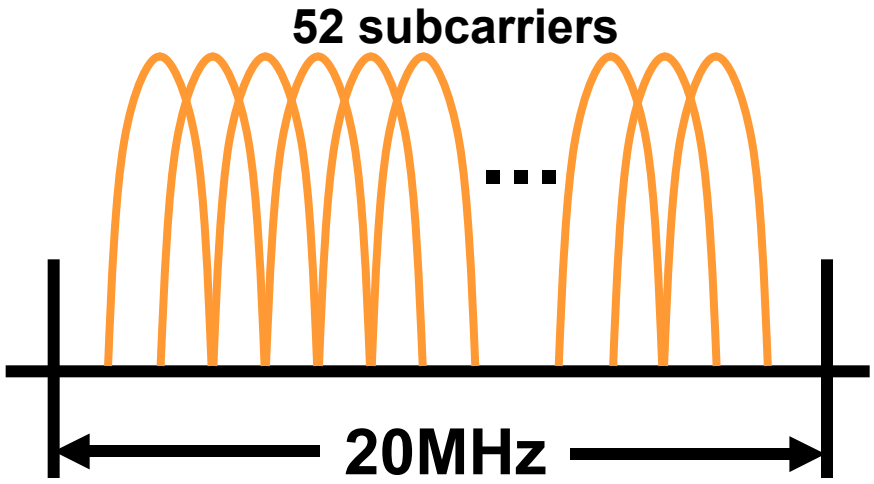
- Generate a high power replica of modulator output
  - Accuracy of replication → Linearity
- Convert DC energy to RF energy
  - Efficiency of this conversion → Efficiency

Linearity and Efficiency Trade-off

- Higher efficiency:
  - Battery lifetime
  - Thermal management
- Higher linearity:
  - Sophisticated modulation
  - Spectral efficiency
  - Data rate
- There is a trade-off between efficiency and linearity
- Goal: higher efficiency linear amplifiers

Target Application

- IEEE 802.11g for WLAN
  - Orthogonal Frequency Division Multiplexing (OFDM)
  - 2.4 GHz
  - Peak-to-average-power-ratio (PAPR) = 52 (17dB)
  - 16.6MHz signal bandwidth



CMOS RF Power Amplifiers

- Usual technologies: GaAs HBT, SiGe HBT, Si BJT, …
- Advantages of CMOS:
  - Low cost, high yield
  - Possibility of integration with the transceiver
  - Possibility of new architectures
- Disadvantages of CMOS:
  - Low gain
  - Low breakdown voltage
  - Substrate effects

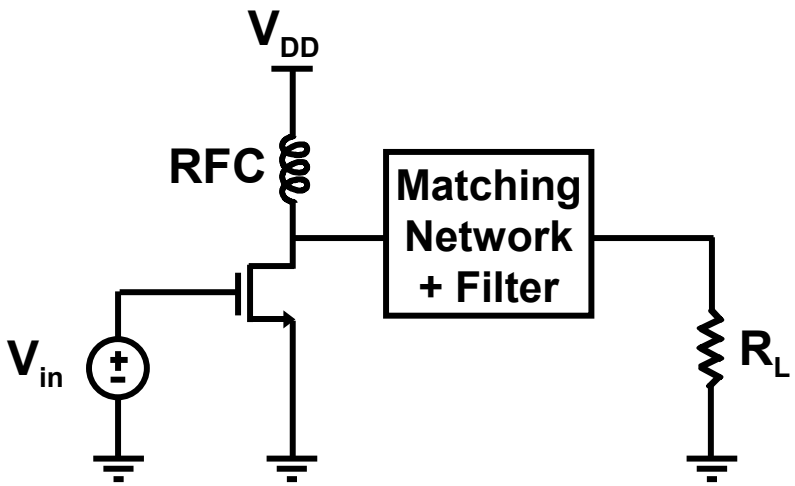
Research Goal

Explore new architectures to improve efficiency of linear power amplifiers in a 0.18μm standard CMOS technology with a focus on IEEE 802.11g as the target application

Outline

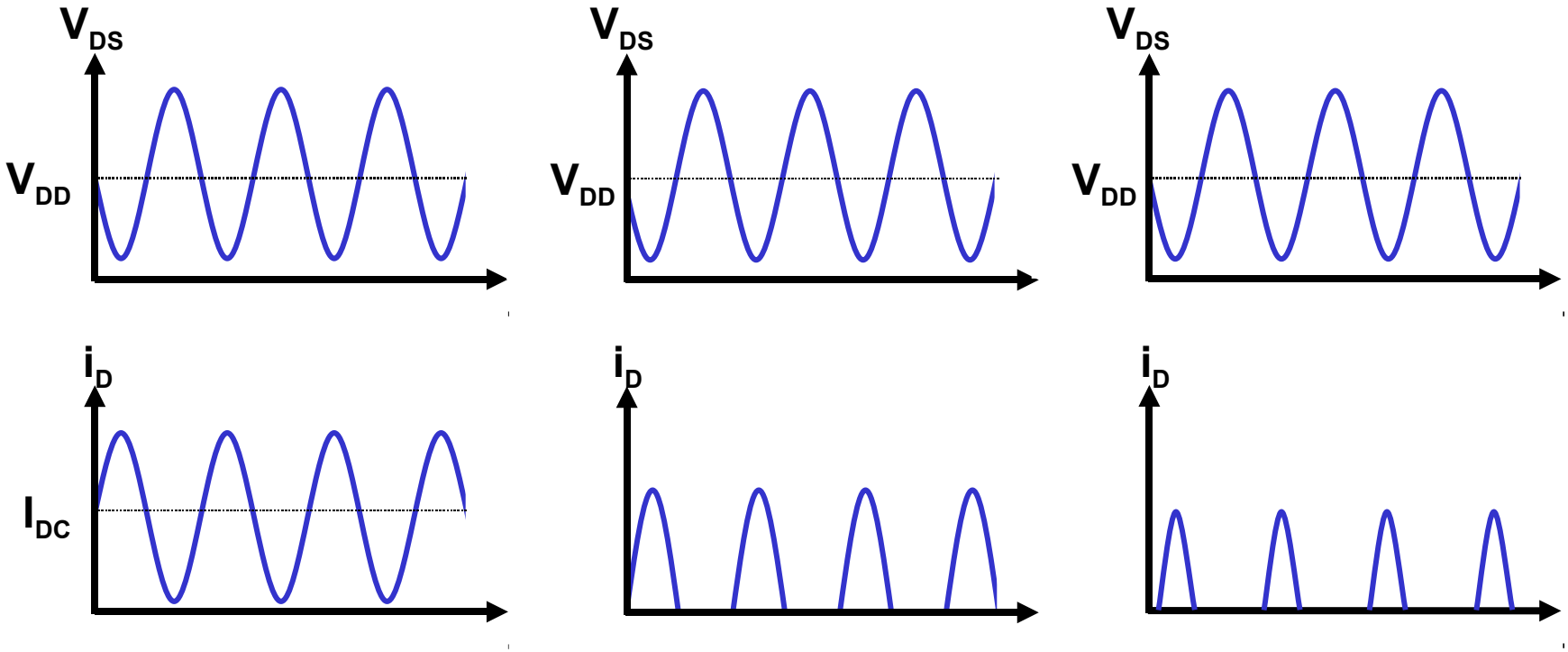
- RF power amplification
- Proposed power amplifier architecture
- Implementation
- Experimental results
- Conclusions

General Model of RF Power Amplifiers



- Transconductance mode
  - Class A-C
- Switch mode
  - Class D-F

Transconductance Amplifiers



Class-A
Eff = 50%

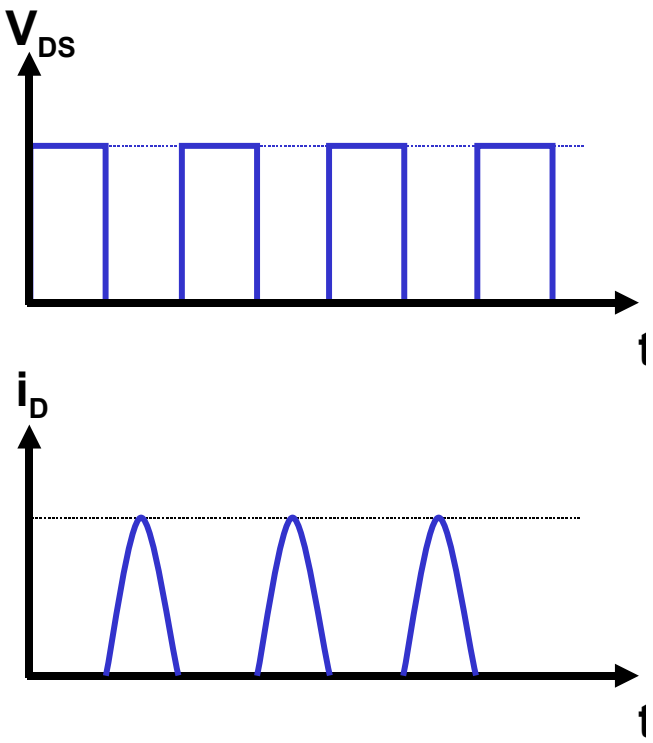
Class-B
Eff = 78%

Class-C
Eff → 100%

Efficiency

Linearity

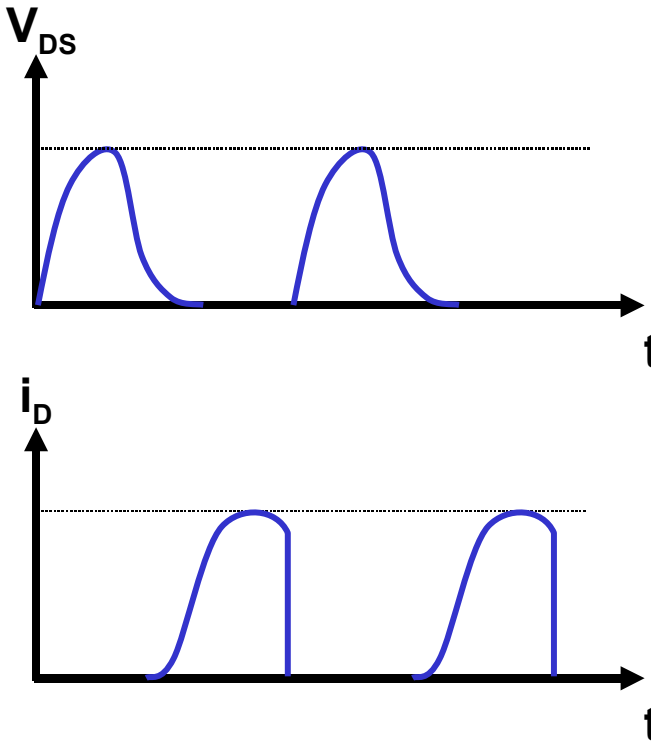
Switch-mode Amplifiers



Class-D, F

Eff → 100%

Nonlinear



Class-E

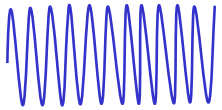
Eff → 100%

Nonlinear

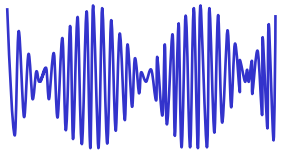
Summary of Classic PA's Performance

Class	Mode	Maximum Efficiency	Linearity
A	Trans-conductance	50%	Good
B		78.5%	Moderate
C		100%	Poor
D	Switch	100%	Poor
E		100%	Poor
F		100%	Poor

Wireless Communication Signals

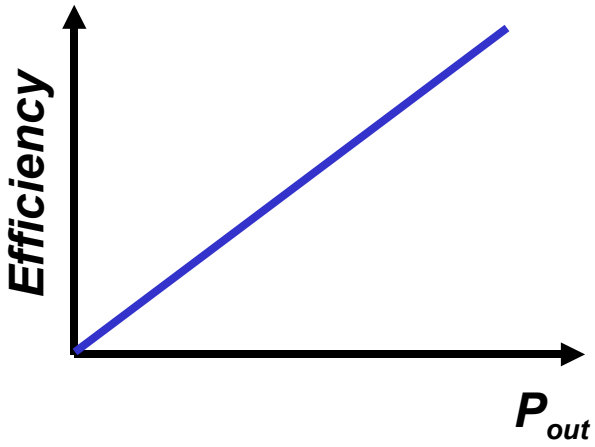


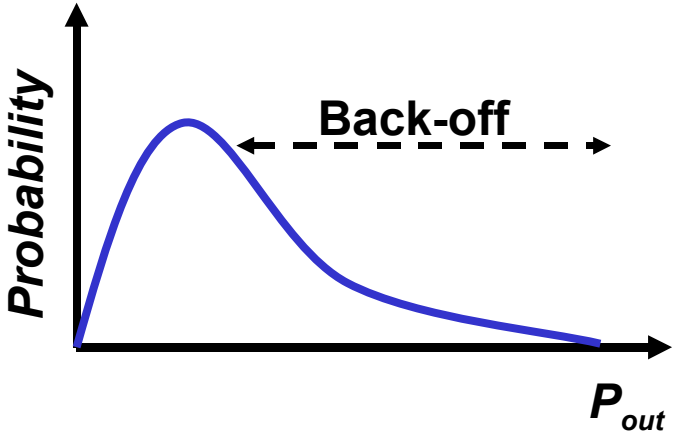
- **Constant-envelope**
  - No amplitude information - phase-only modulation
  - Example: GSM
  - Nonlinear power amplifiers such as class C, E, F
  - Spectral efficiency traded for power efficiency



- **Non-constant envelope**
  - Amplitude and phase modulation
  - Examples: Mobile 2.5G, 3G, and 4G and IEEE 802.11g
  - Linear power amplifiers such as class-A.

Average Power Efficiency

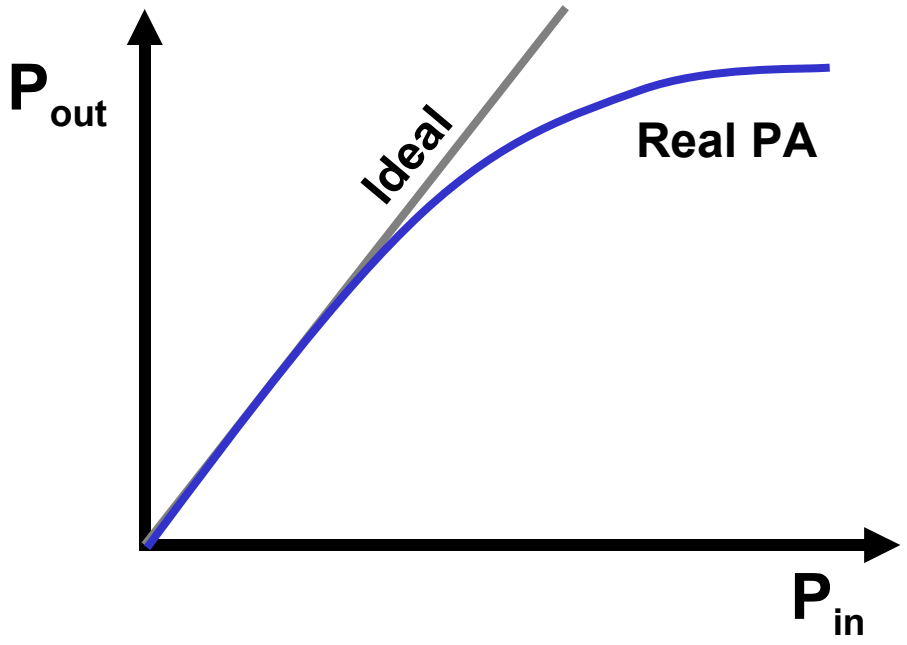




$$< \eta > = \int_0^{max\ power} \eta(p) f(p) dp$$

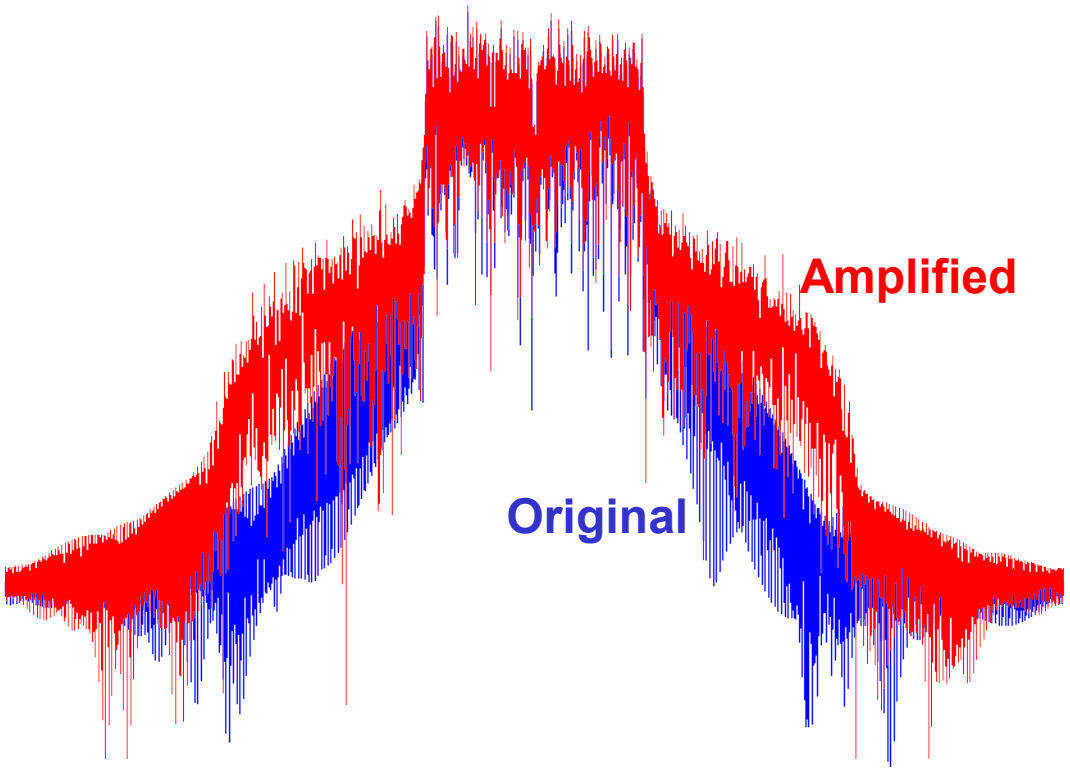
- Low average power efficiency
  - 10dB back-off for class-A → 5% maximum average efficiency

Effects of Nonlinearity



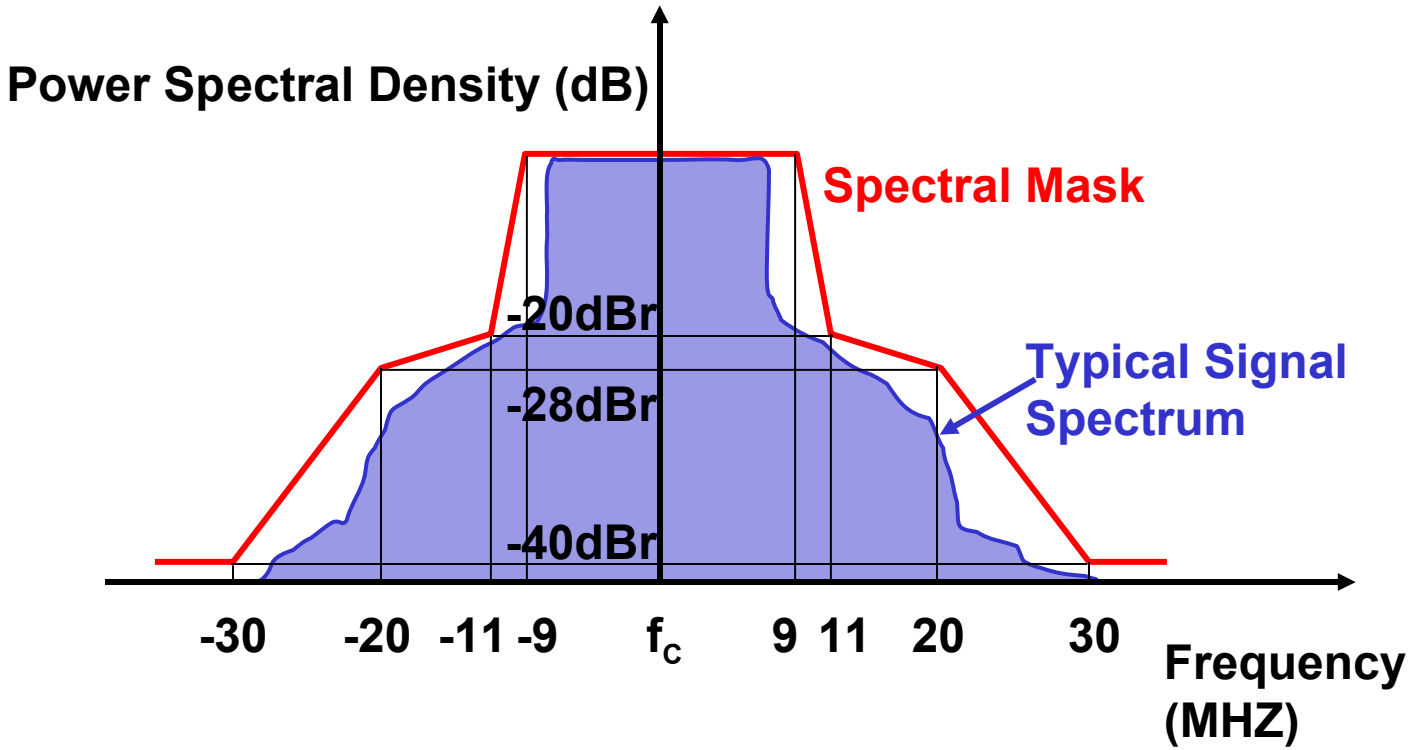
- Spectral regrowth
- Constellation error

Spectral Regrowth



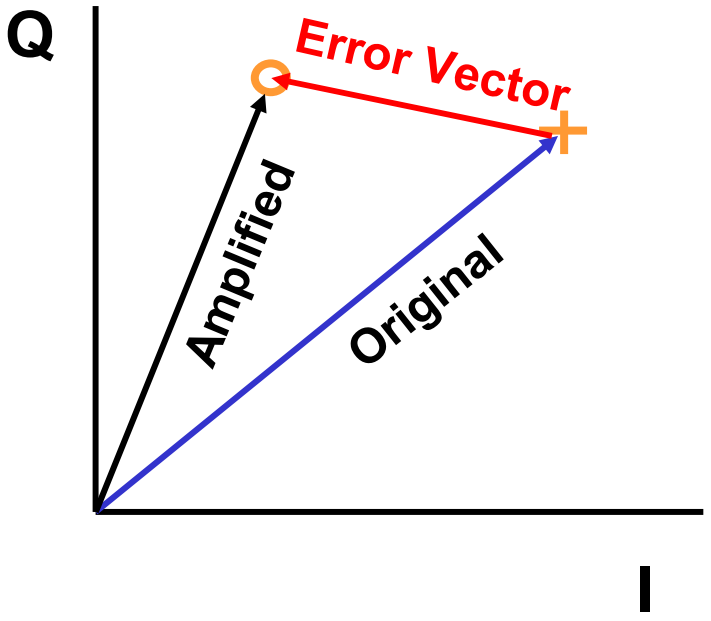
- Nonlinearity → Spectrum spreading into adjacent channels

Spectral Mask



- IEEE 802.11g spectral mask
- Output should not exceed the mask

Constellation Error



- Deviation from the ideal constellation point in I/Q plane

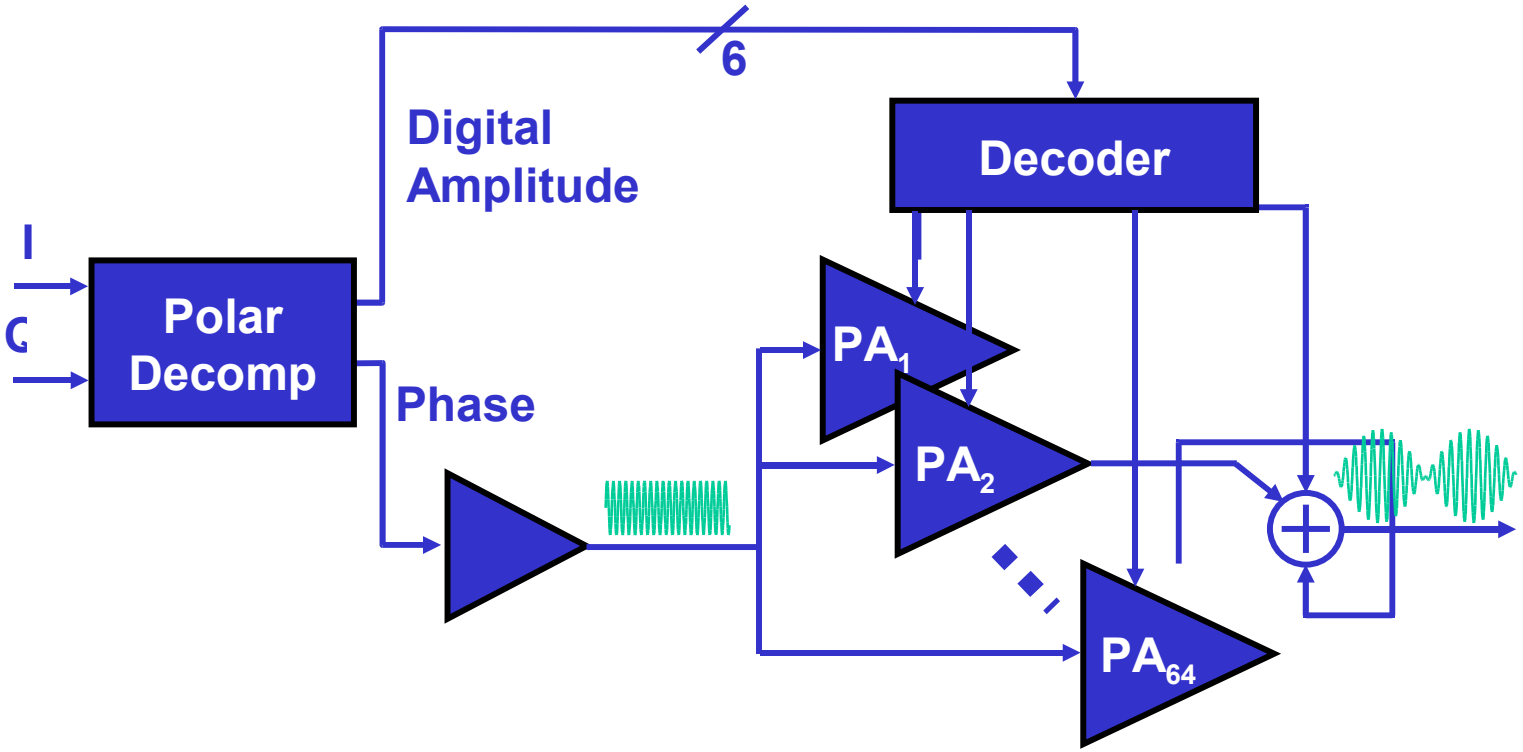
Error-vector-magnitude (EVM)

- **Definition: ratio of the root mean square (RMS) power of the error vector to the RMS power of the reference**

EVM Requirements of IEEE 802.11g

Modulation	Data rate (Mbits/s)	EVM (dB)
BPSK	6	-5
	9	-8
QPSK	12	-10
	18	-13
16-QAM	24	-16
	36	-19
64-QAM	48	-22
	54	-25

Proposed Integrated Polar Transmitter



- Efficient constant-envelope amplification, followed by amplitude modulation with selectively switching unit amplifiers

Equal-Weighted Unit Amplifiers

- **Advantages compared to binary-weighting:**
  - **Better matching and better DNL**
  - **Better dynamic performance**

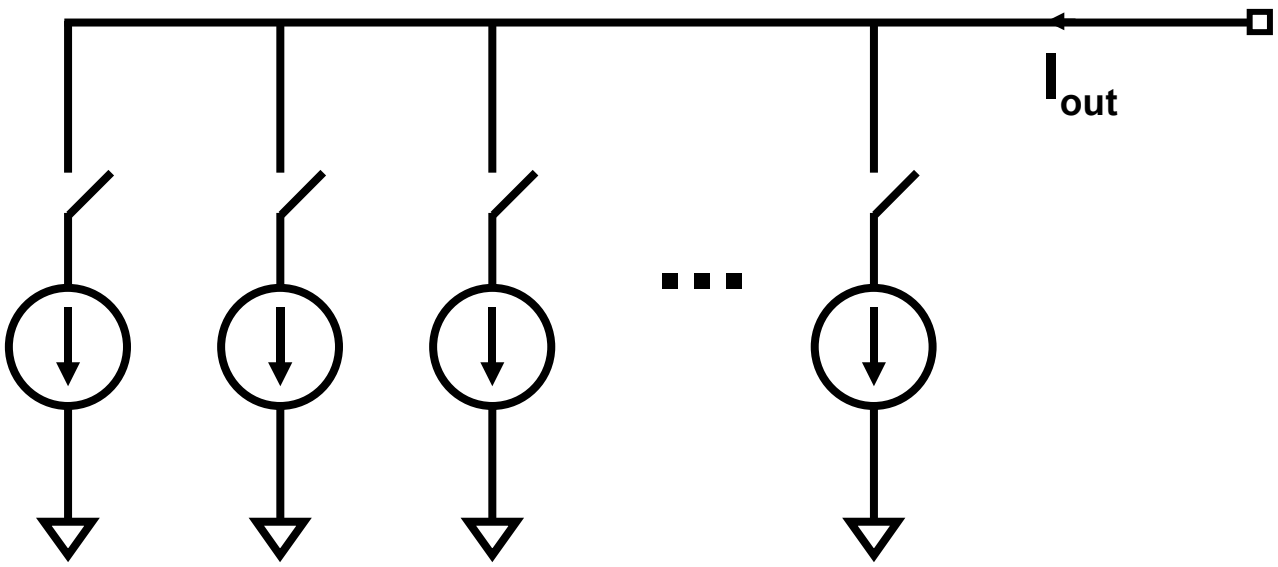
- **Challenges:**
  - **Thermometer-decoding → increased area**
  - **Need to combine RF power from multiple devices**

Power Combining

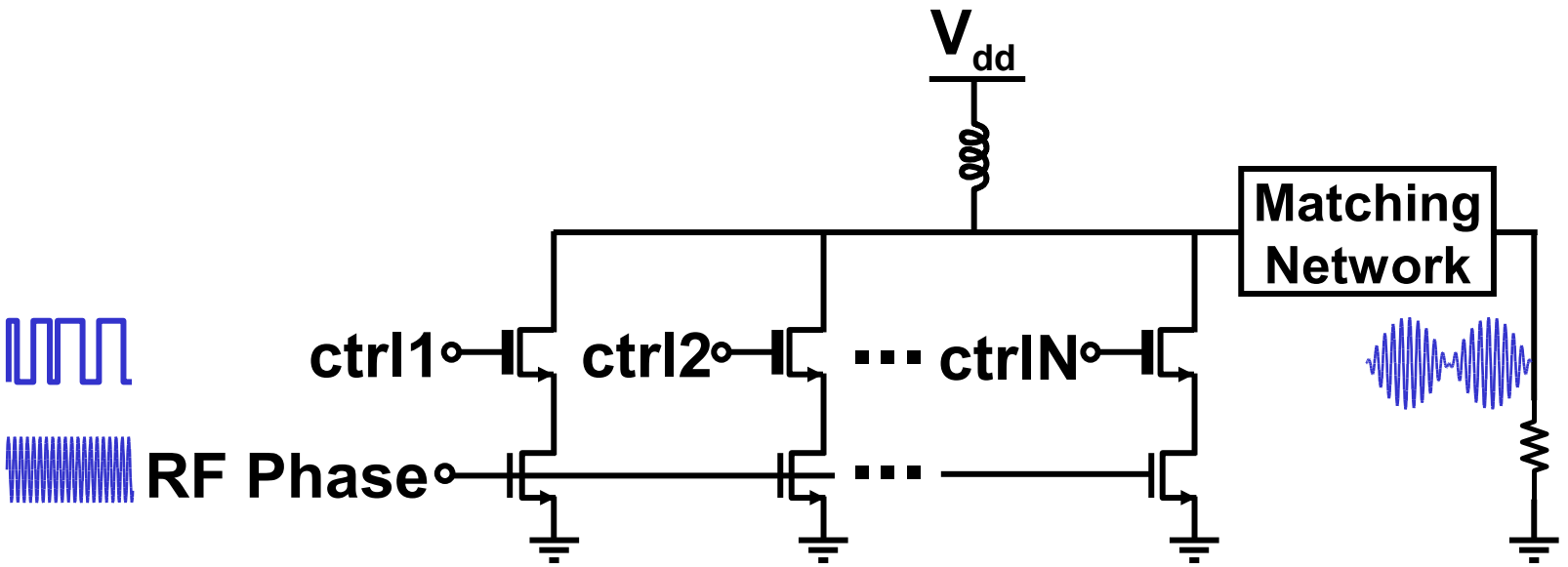
- Transmission-line-based combiners
  - Too large to integrate on chip at 2.4GHz
  - Difficult to match paths
- Lumped-element combiners
  - Large area for large number of amplifiers
  - Low power efficiency
  - Low bandwidth
- Transformer-based combiners
  - Low power efficiency
  - Difficult to implement large numbers

Current-mode Power Combining

- On-chip
- Power and area efficient
- Requires transconductance amplifiers (which are class A)



Circuit Topology



- Current source PA's, wired in parallel at drains
- Thick-oxide cascode transistor acts as switch
  - Thick-oxide transistors allow higher power supply

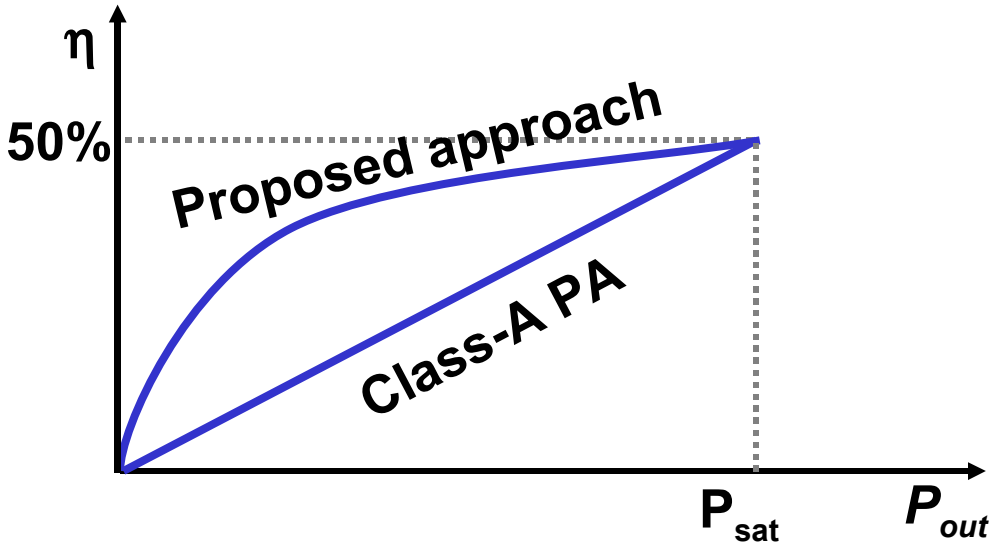
Efficiency

- For a traditional class-A :
  - Linear relationship with P_{out}

$$\eta = \frac{i_{RF}^2 \times R/2}{I_{DC} \times V_{DD}} \propto P_{out}$$

- For this approach :
  - Square-root relationship with P_{out}

$$\eta = \frac{I_{DC}}{I_{DC}} \cdot \frac{i_{RF} \times R/2}{V_{DD}} \propto \sqrt{P_{out}}$$



Average Efficiency

- **For a non-constant amplitude signal, the average efficiency is:**

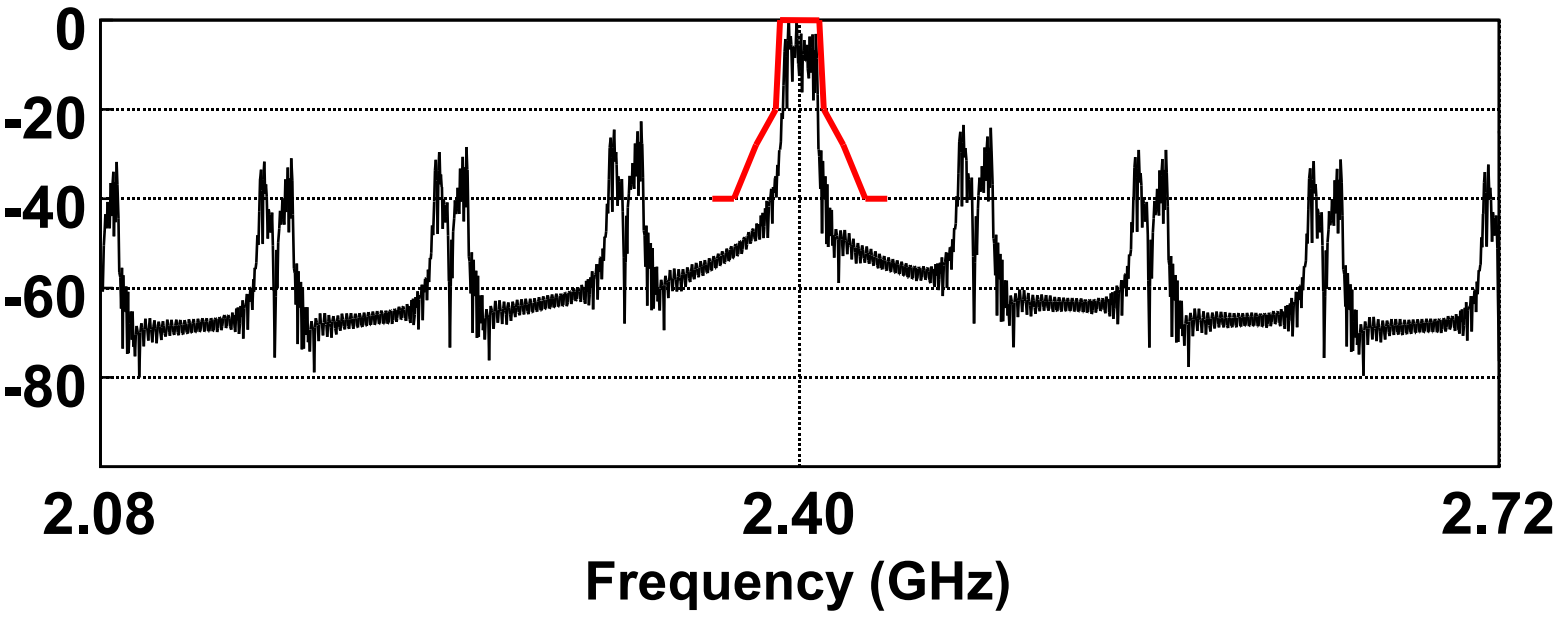
$$< \eta > = \int_0^{max\ power} \eta(p) f(p) dp$$

Power backoff	Efficiency for traditional ideal class-A PA	Efficiency for proposed approach with class-A stages
6 dB	14.2 %	23.2 %
10 dB	5.0 %	14.0 %
12 dB	3.1 %	11.1 %

- ~2-3x improvement in average efficiency

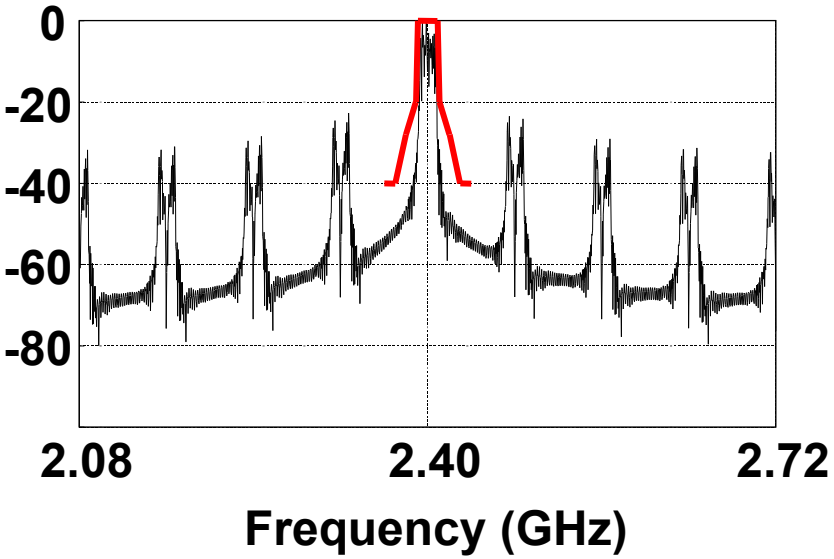
Spectral Images

- Result from the discrete-time to continuous-time conversion
- Can violate spectral mask or requirements on maximum out-of-band emission

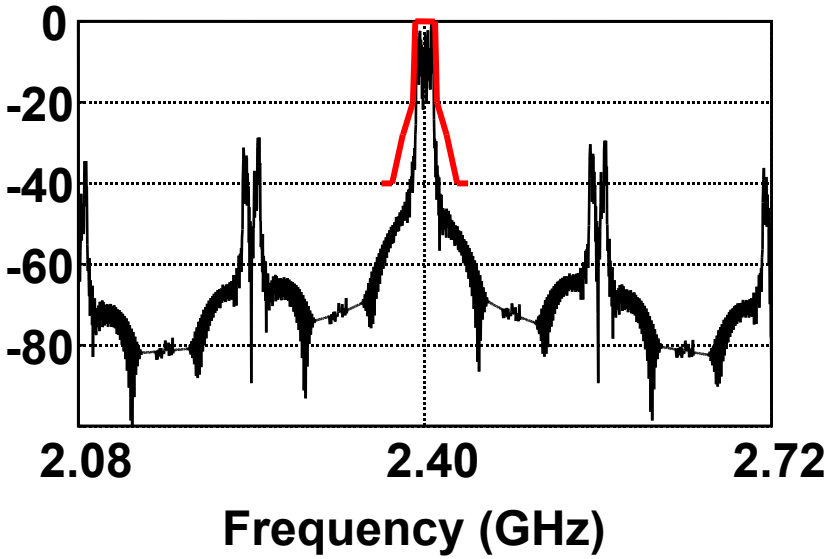


Spectral Image Suppression

- May use oversampling at input



4x oversampling
80MHz clock

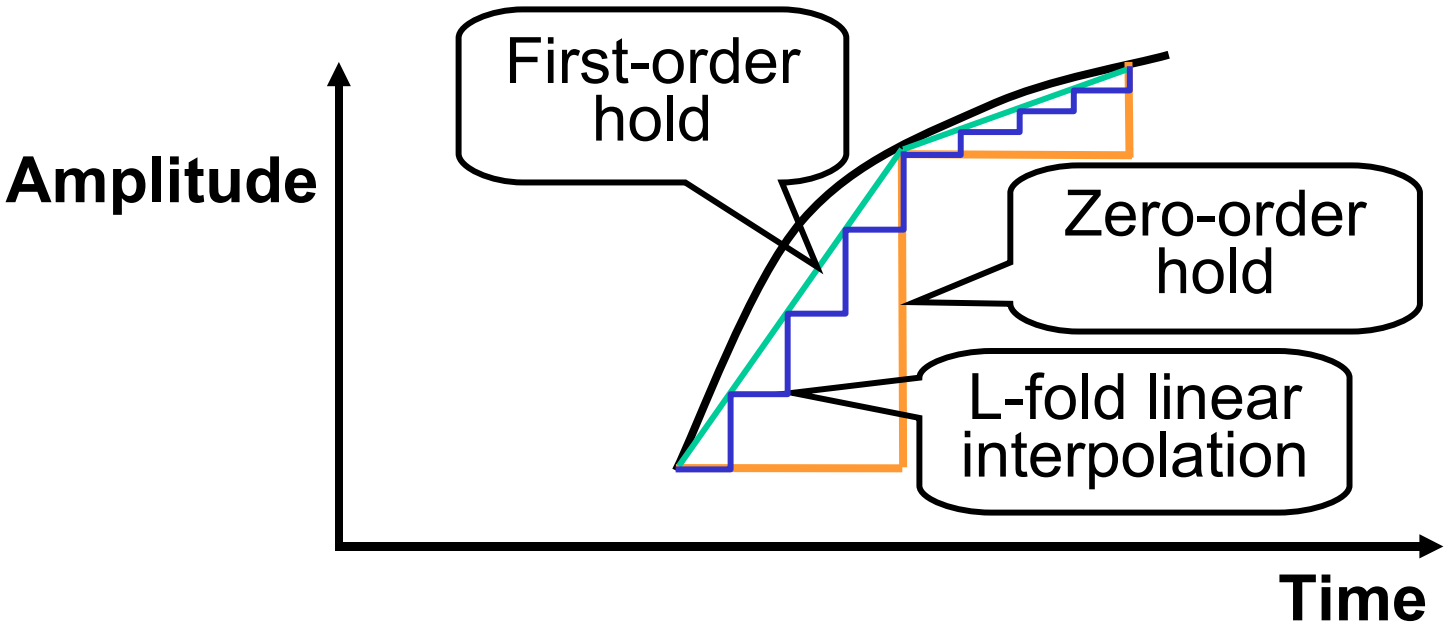


8x oversampling
160MHz clock

- Needs still higher oversampling ratio

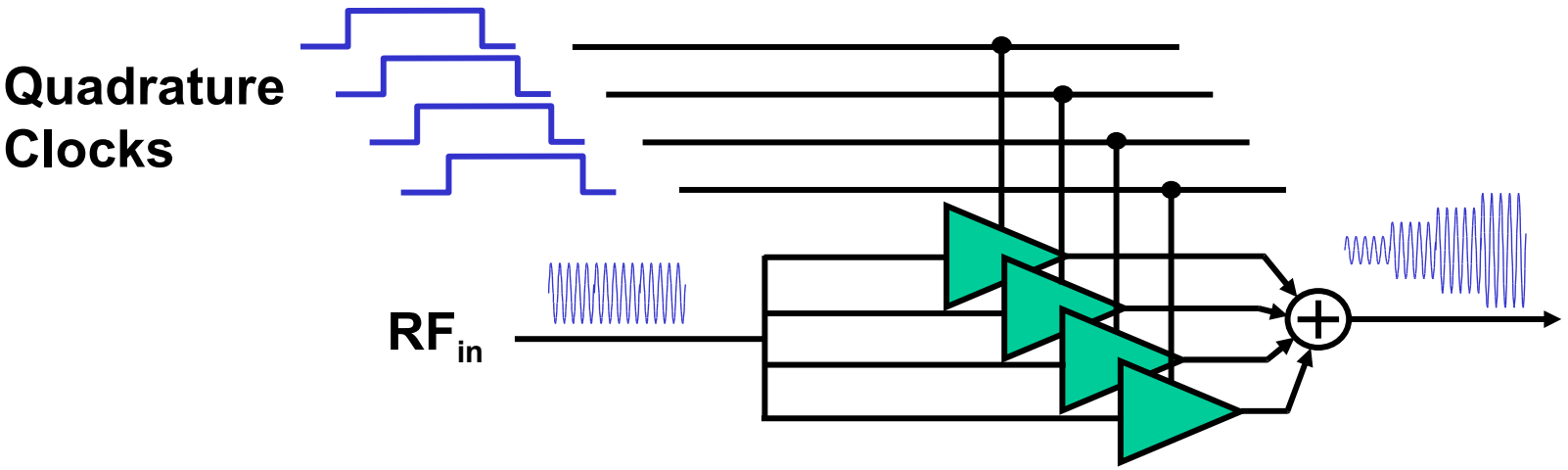
L-fold Linear Interpolation

- **L-fold linear interpolation* to suppress spectral images**
  - **Approximates linear interpolation**



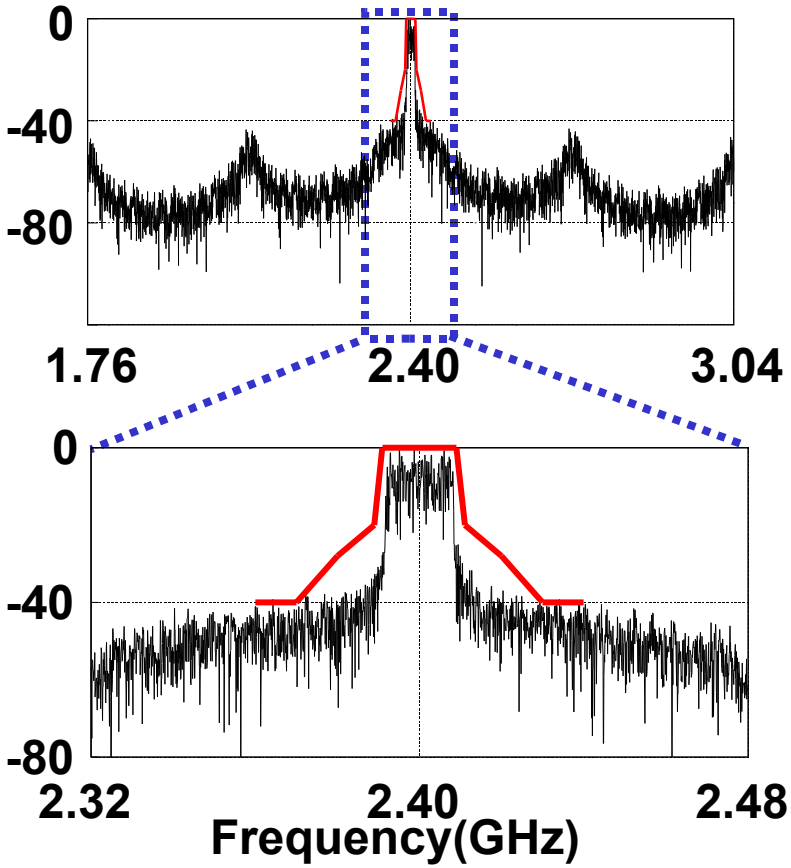
***Ref:** Y. Zhou and J. Yuan, JSSC, Vol. 38, pp. 1182-1188

L-fold Interpolator Implementation

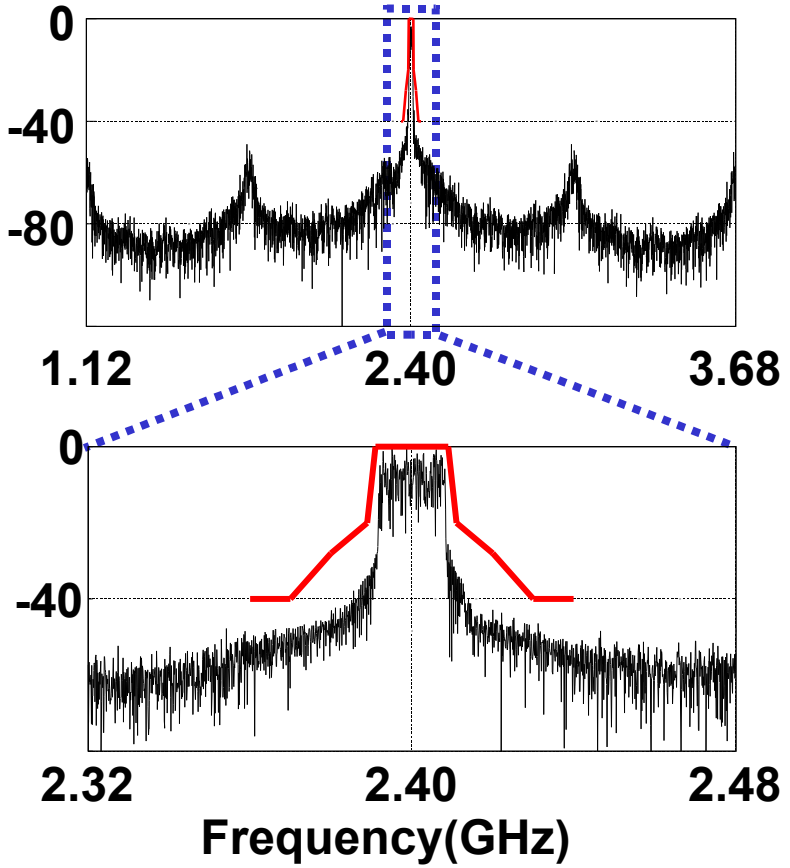


- The amplifier is divided into four sections that are clocked sequentially
- Challenge: introduces nonlinearites
  - Can remove completely by phase compensation (which requires an increased clock rate)
  - Can remove partially by oversampling

System Simulation Results

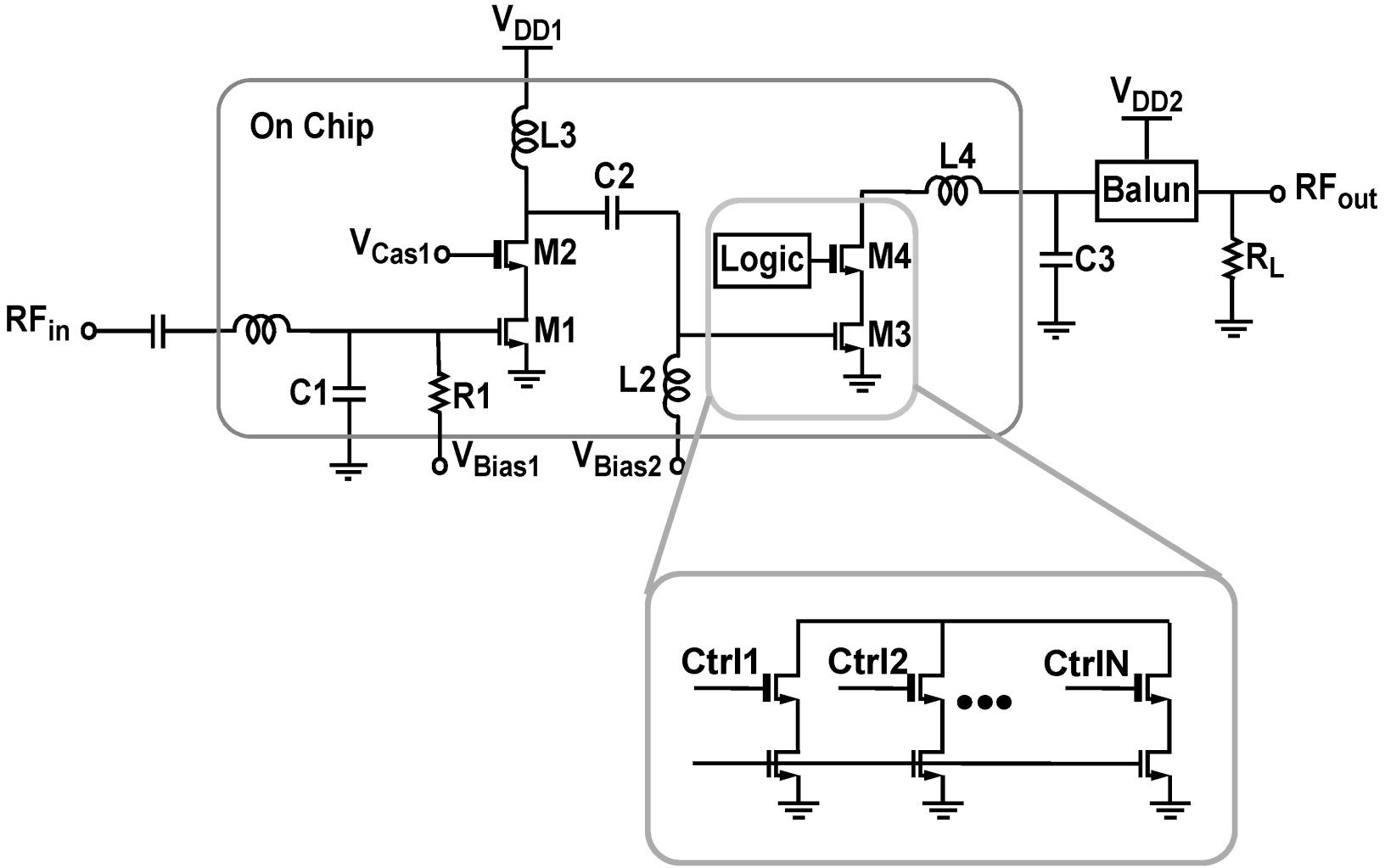


4x oversampling
+ 4-fold interpolation



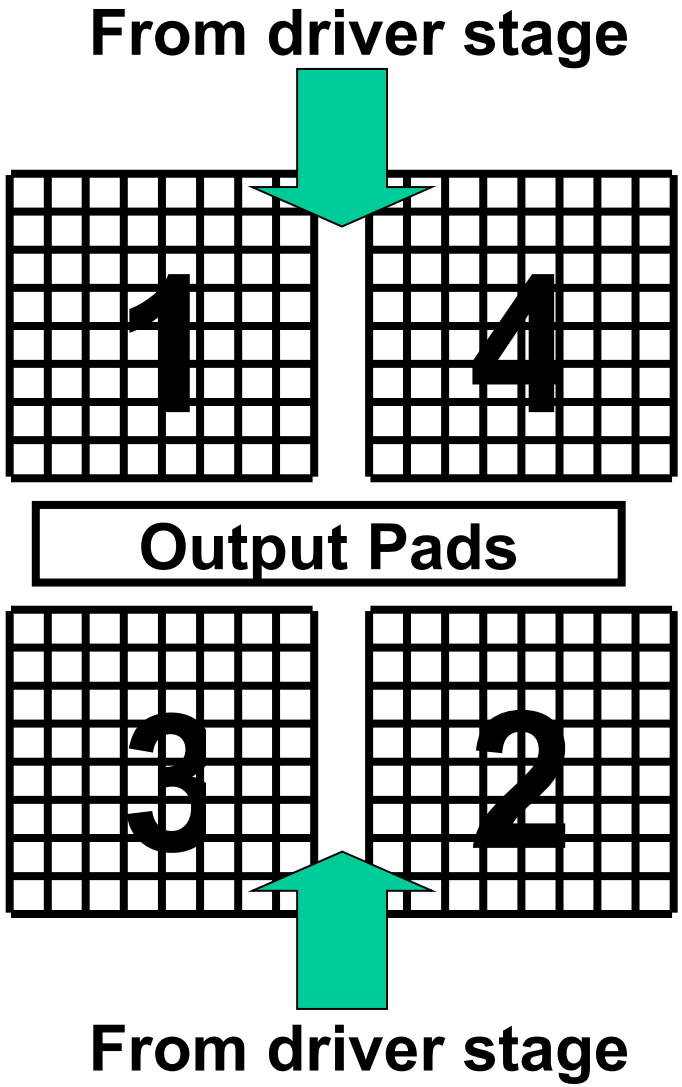
8x oversampling
+ 4-fold interpolation

Circuit Schematic



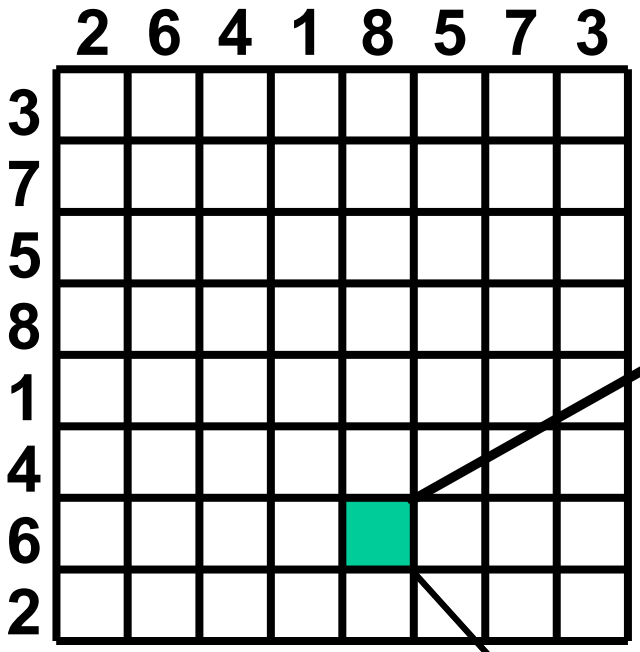
Note: actual circuits are fully differential

Output Stage Layout

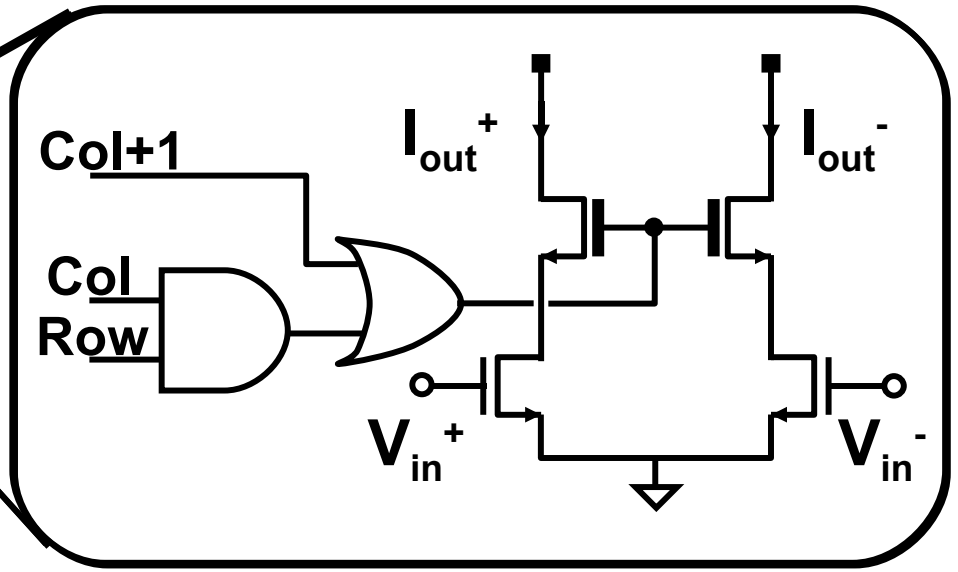


- 4 sections of 64 unit cells each
- Quadrature-phased clocks for the sections
- Output pads in center

Unit Amplifier Layout

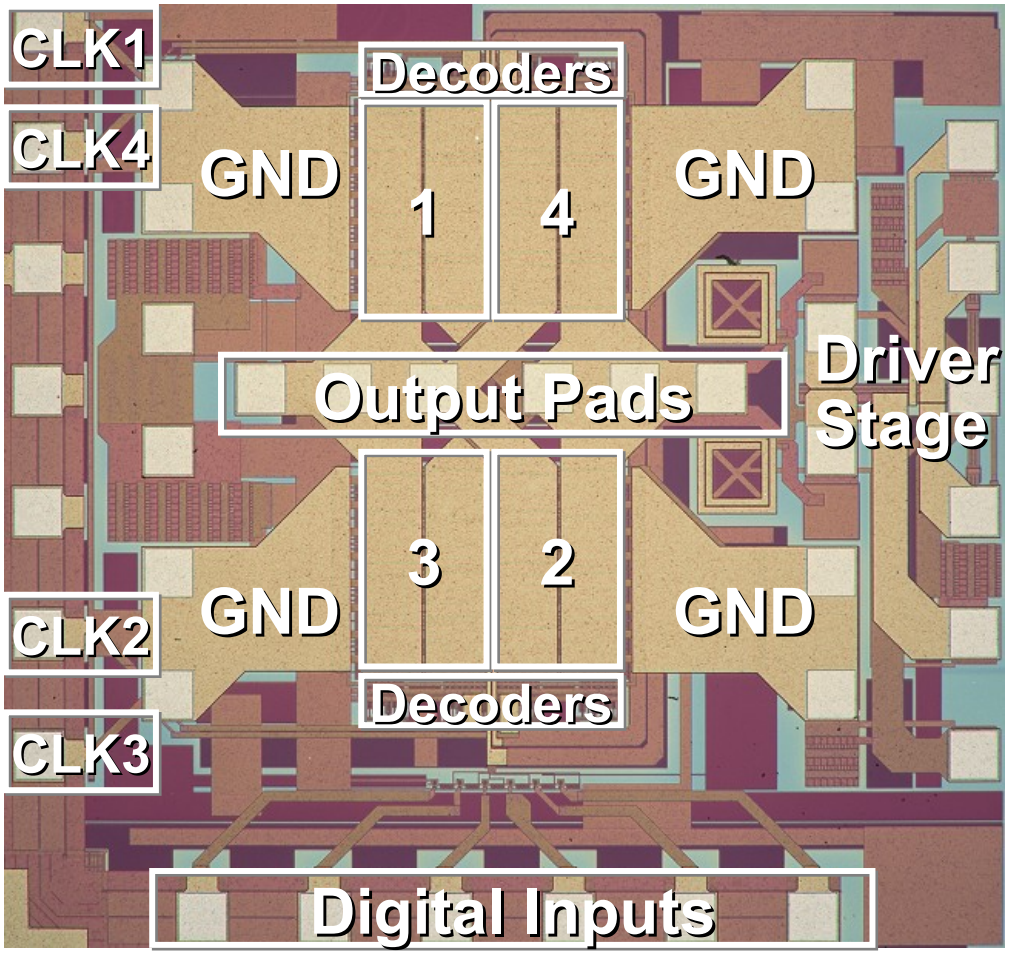


- Thermometer decoding
- $2^6 = 64$ unit cells
- Randomized switching
- Current combination



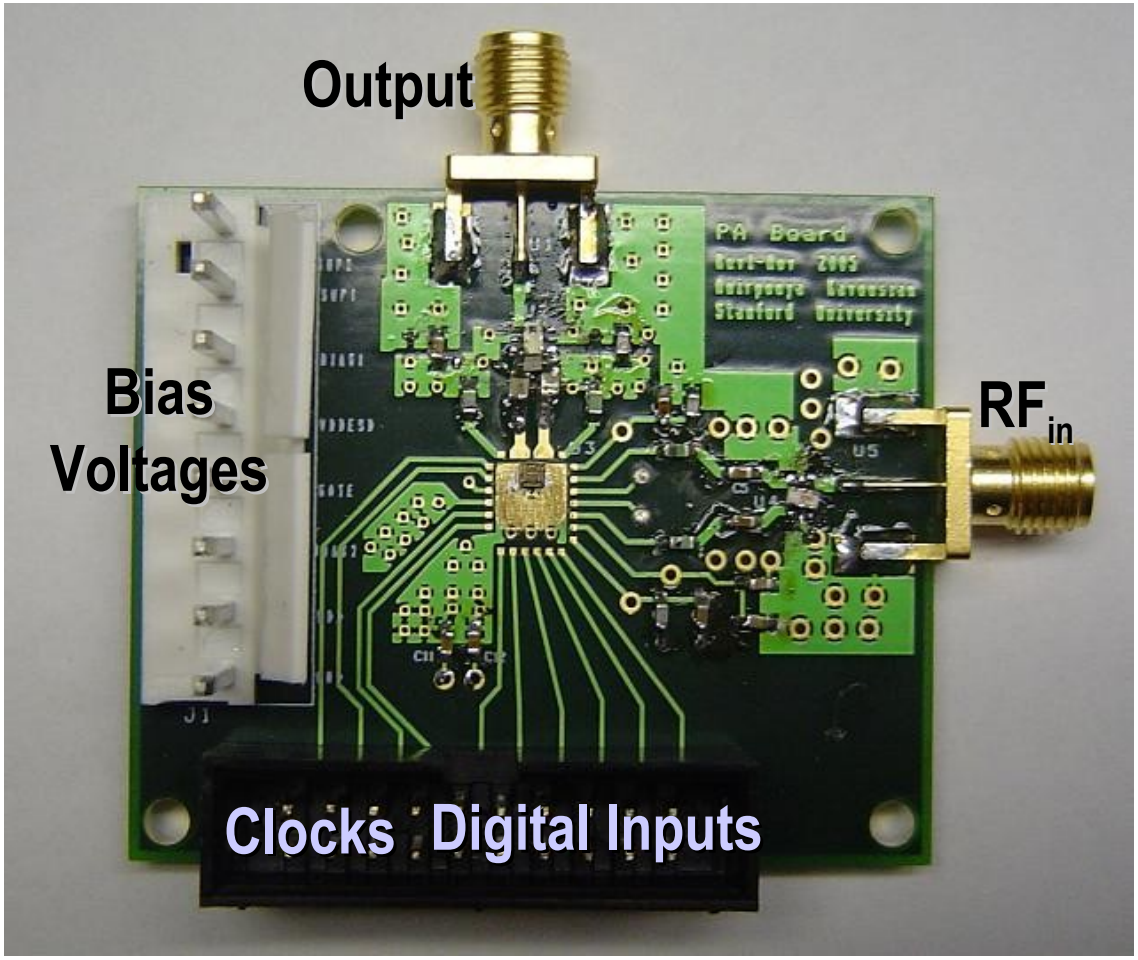
Unit Cell

Chip Micrograph



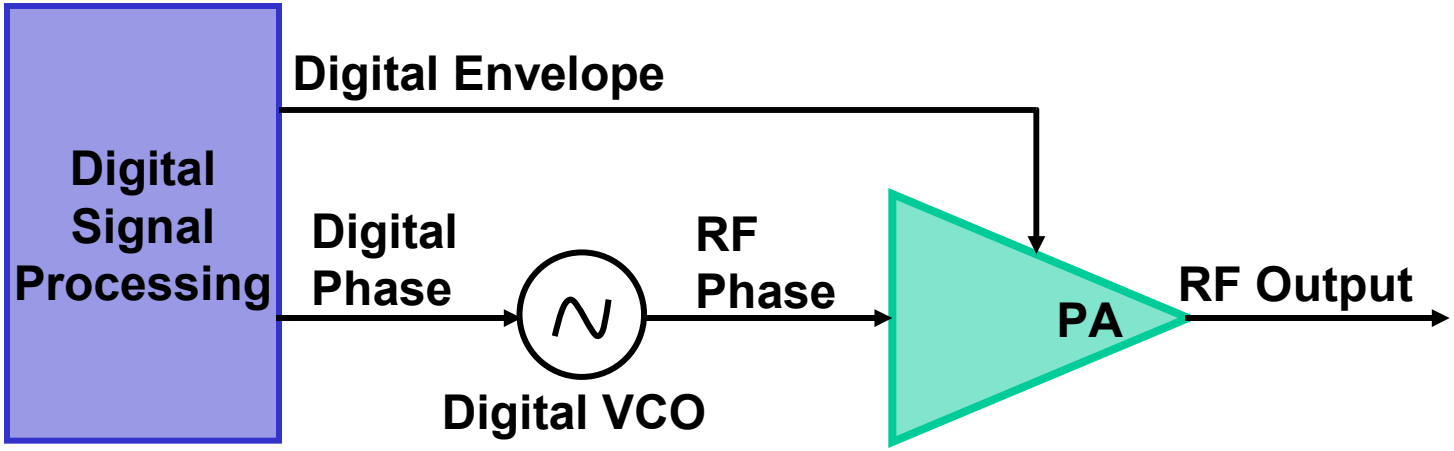
1.3x1.4mm² in 0.18µm CMOS

Test Board

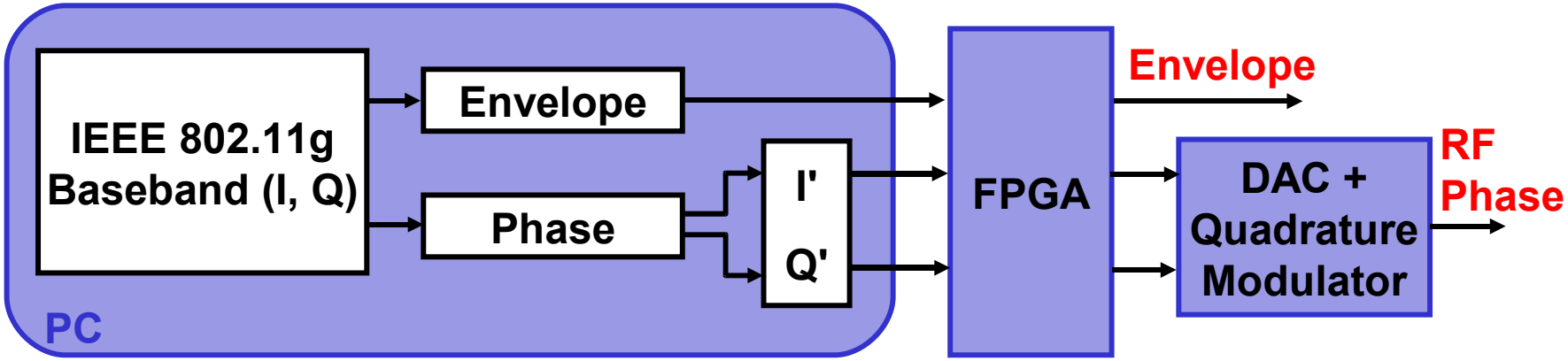


4x5cm², 4-layer FR-4 board

Generating Phase and Envelope Signals

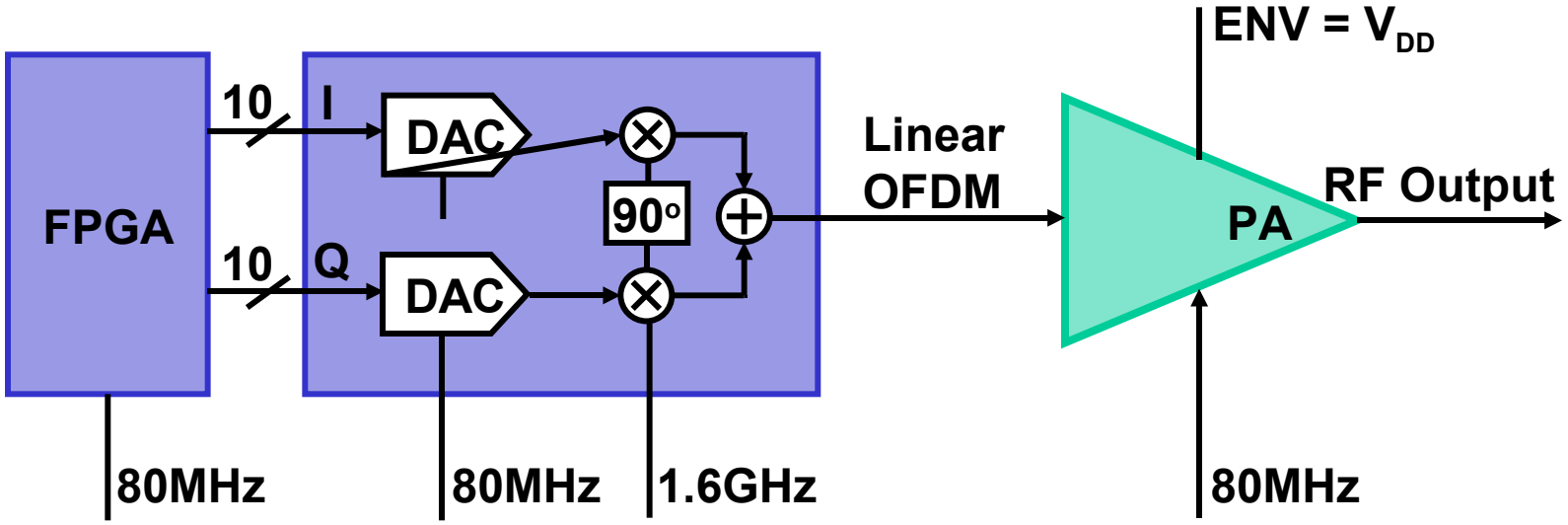


Generating Signals Off-chip



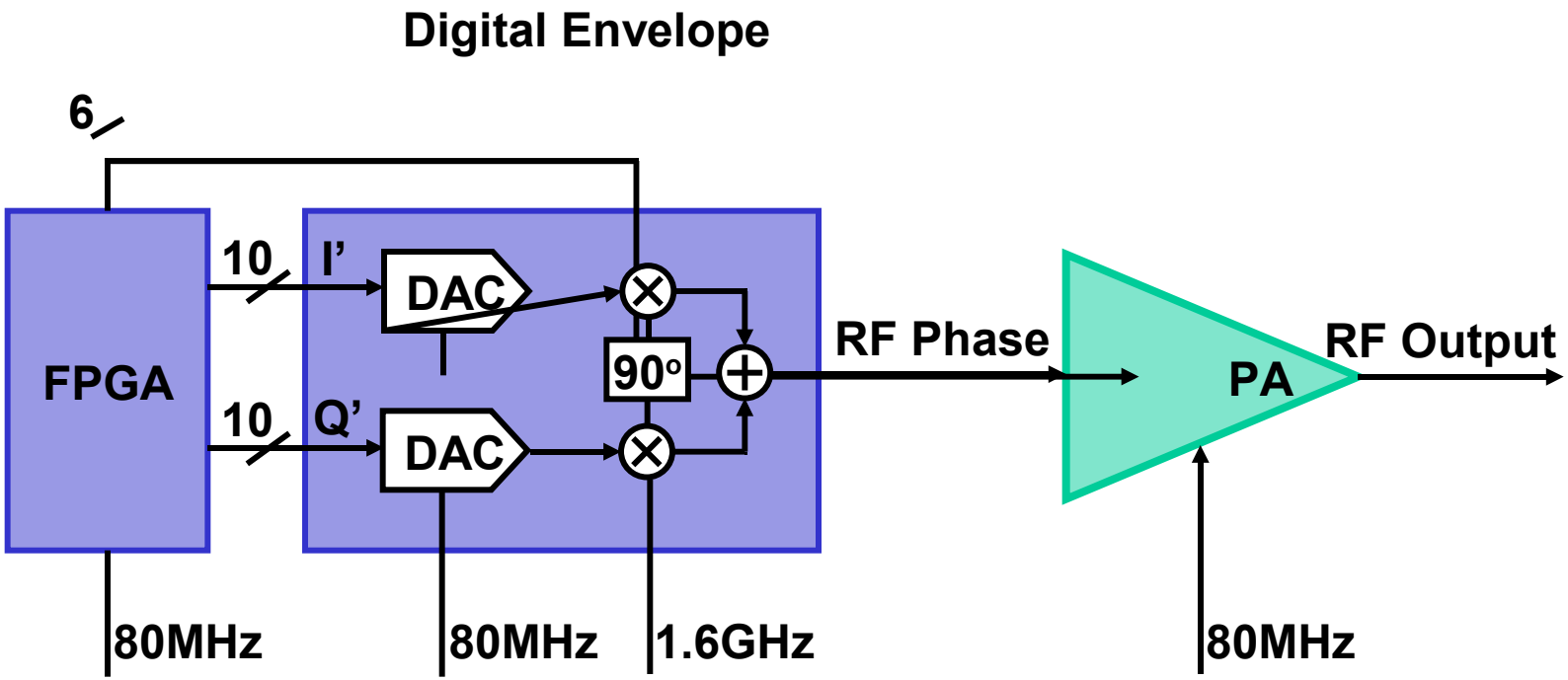
- Decompose packet into phase-only modulated and envelope
- Decompose the phase signal into I' and Q'
- Load the phase (I' and Q') and Envelope onto FPGA
- A Dual-channel DAC followed by a Quadrature modulator converting I' and Q' to RF phase
- Directly drive the digital envelope input

Demonstration System : Class-A Operation



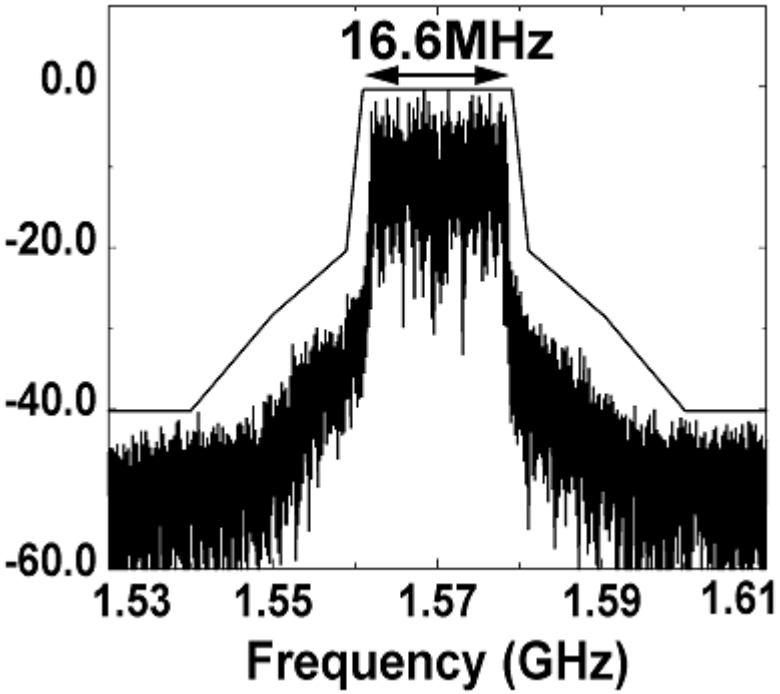
- PAE = 3.1%

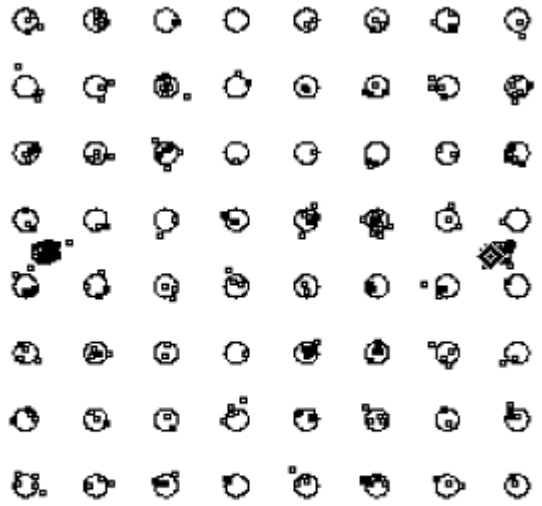
Demonstration System: Polar Operation



- Single Clock at 80MHz

Measurement Results

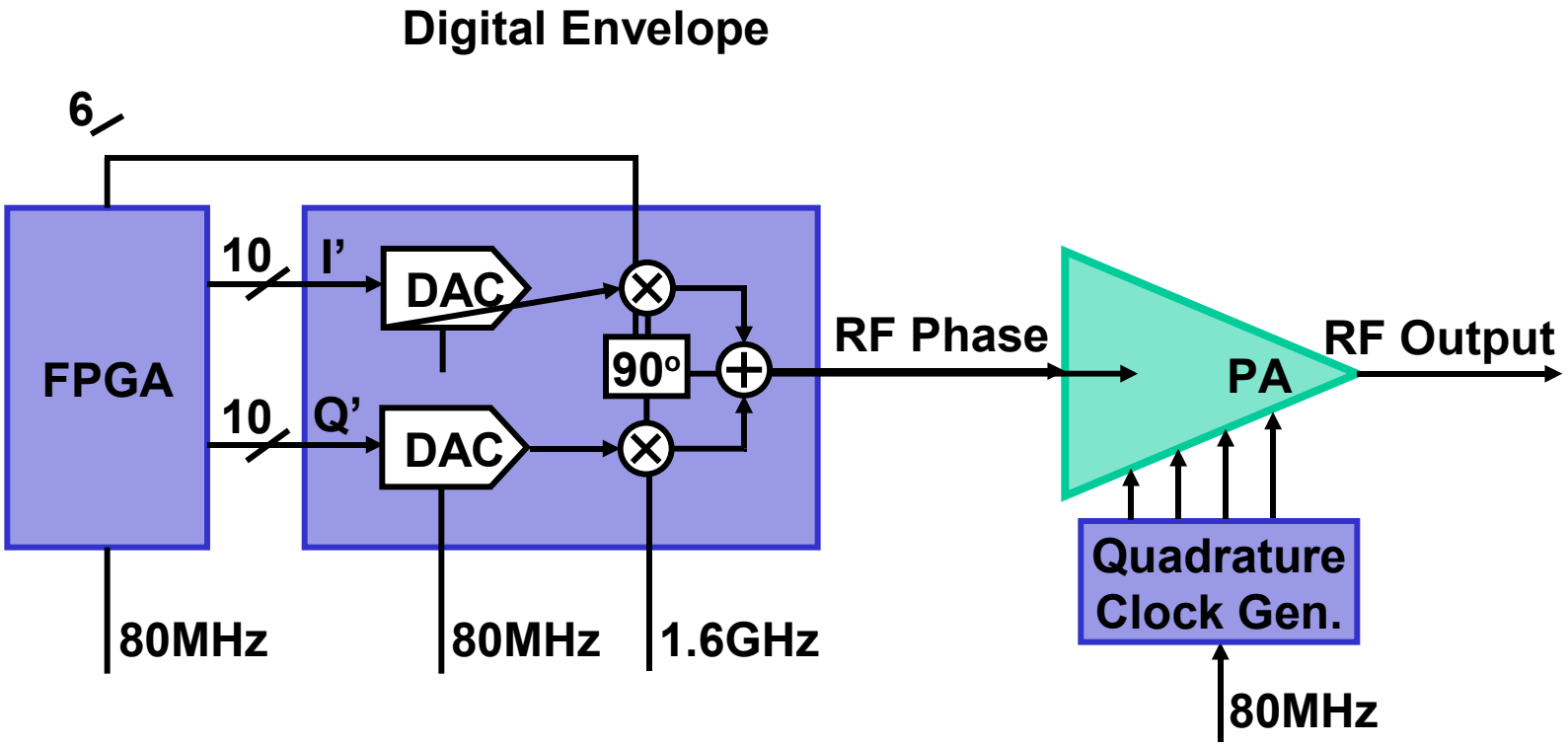




EVM = -26.8dB

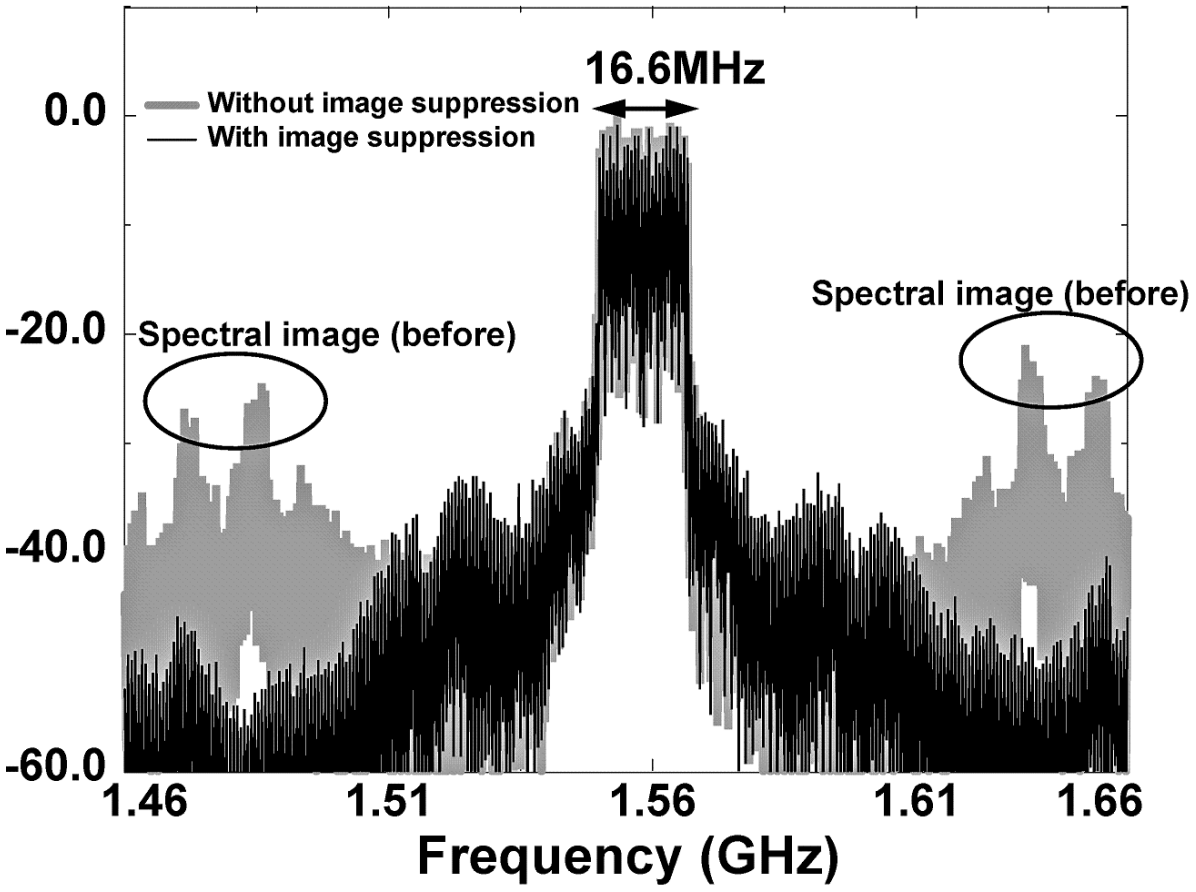
- P_{out} = 14.7dBm (13.6dBm including balun loss)
- PAE = 8.9% (6.7% including balun loss)
- More than double the efficiency of class-A mode

Demonstration System: Image Suppression



- Quadrature-phased clocks

Image Suppression Measurement



Performance Summary

Technology	0.18μm CMOS, 2P5M
Supply Voltage Digital Hardware Driver Stage Output Stage	 1.8V 2.2V 1.7V
Linear 64 QAM OFDM Output Power	14.7dBm 13.6dBm (balun included)
EVM for 64 QAM OFDM	– 26.8dB
Dissipated Power Output Stage Driver Stage Digital	 247mW 66mW 3.4mW
PAE (for 64QAM OFDM)	8.9% 6.7% (baluns included)
Center Frequency	1.56GHz
Total Chip Area	$1.8mm^2$

Conclusions

- Demonstrated a polar power amplifier with more than 20-MHz bandwidth
- Digitally modulated RF power amplification architecture
- Meet the linearity required of 64QAM IEEE 802.11g signals
- Better than 2x improvement in power efficiency compared to backed-off class-A design
- L-fold linear interpolation used to suppress spectral images from the digital-to-RF power conversion

Acknowledgements

- Professor Bruce Wooley and Dr. David Su
- Mohammad Hekmat, Dr. Pelgrom, Dr. Shirvani
- C2S2 MARCO Focus Center
- National Semiconductor

Thank You!