The Road to 60 GHz Wireless CMOS

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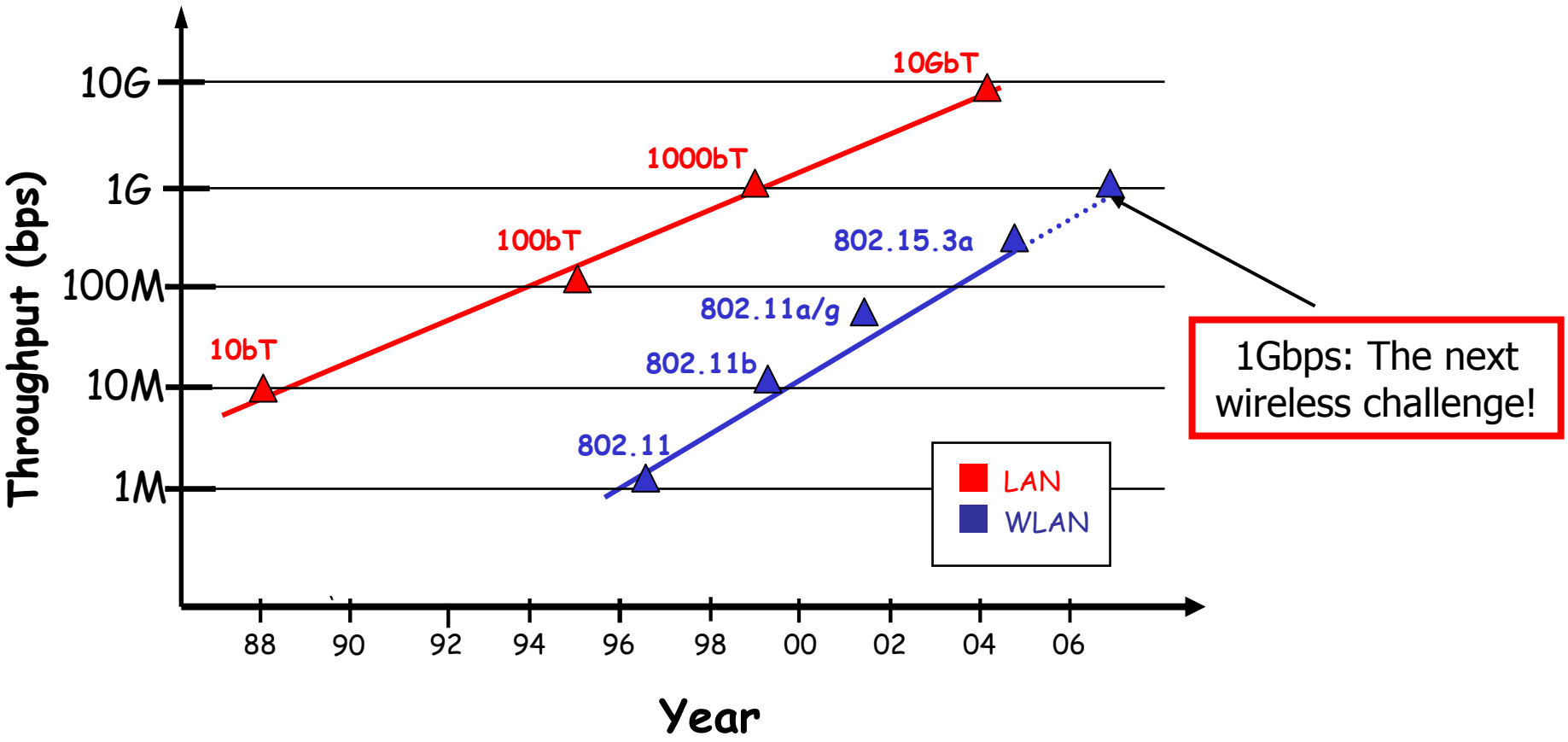
Presentation Outline

- Research Focus Areas
- Motivation
- Passives
- Actives
- Circuits
- Systems
- Summary

LAN/WLAN Demand for Bandwidth



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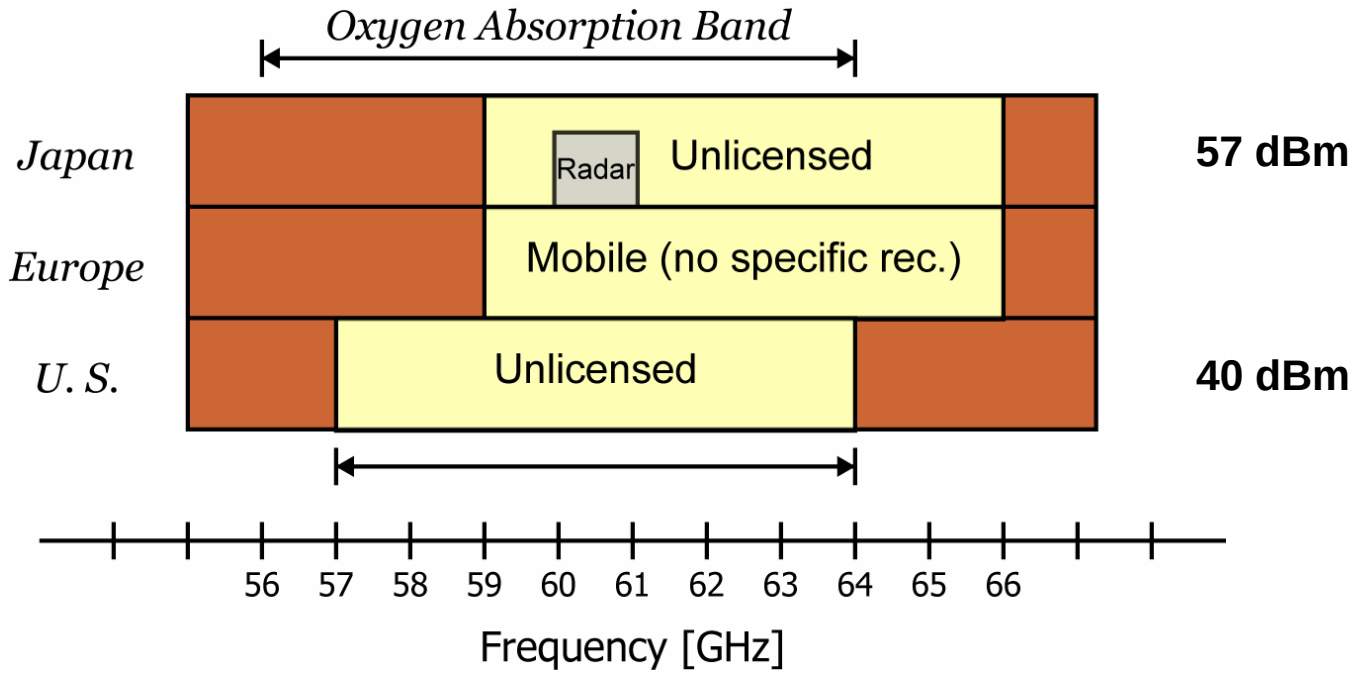
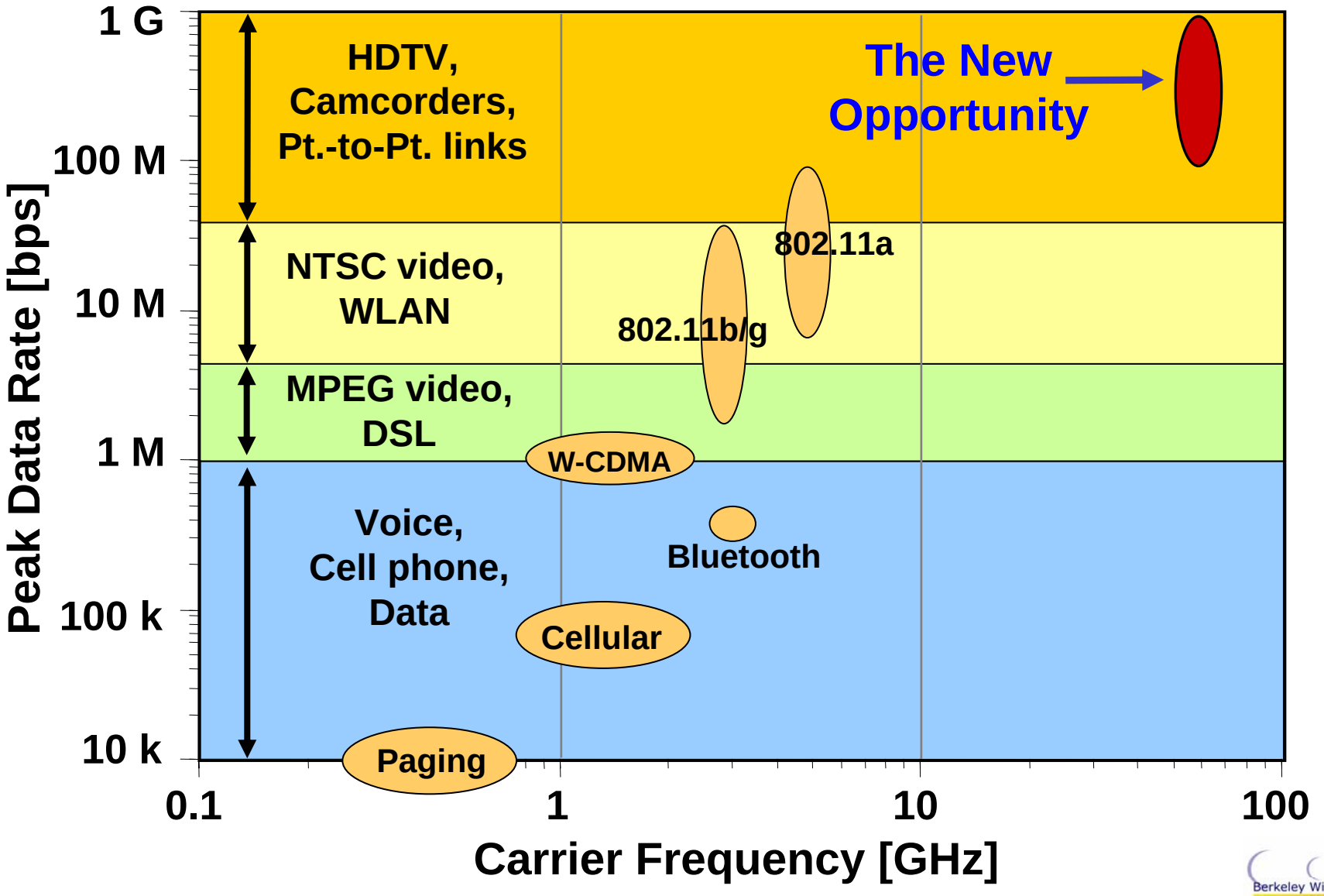
Why is operation at 60 GHz interesting?



Lots of Bandwidth!!!

- 7 GHz of unlicensed bandwidth in the U.S. and Japan
- Same amount of bandwidth is available in the 3-10 UWB band, but the allowed transmit power level is 10^4 times higher !

Higher Frequencies – Higher Data-Rates



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Challenges and Solution

- Major Challenges:
  - High path loss at 60 GHz (relative to 5 GHz)
  - Silicon substrate is lossy – high Q passive elements difficult to realize
  - CMOS building blocks at 60 GHz
  - Need new design methodology for CMOS *mm*-wave
  - Low power baseband architecture for Gbps communication

- Solution:
  - CMOS technology is inexpensive and constantly shrinking and operating at higher speeds – multiple transceivers can be integrated in a single chip
  - Antenna elements are small enough to allow integration into package
  - Beam forming can improve antenna gain, spatial diversity offers resilience to multi-path fading
  - Due to spatial power combining, individual PAs need to deliver only ~ 50 mW

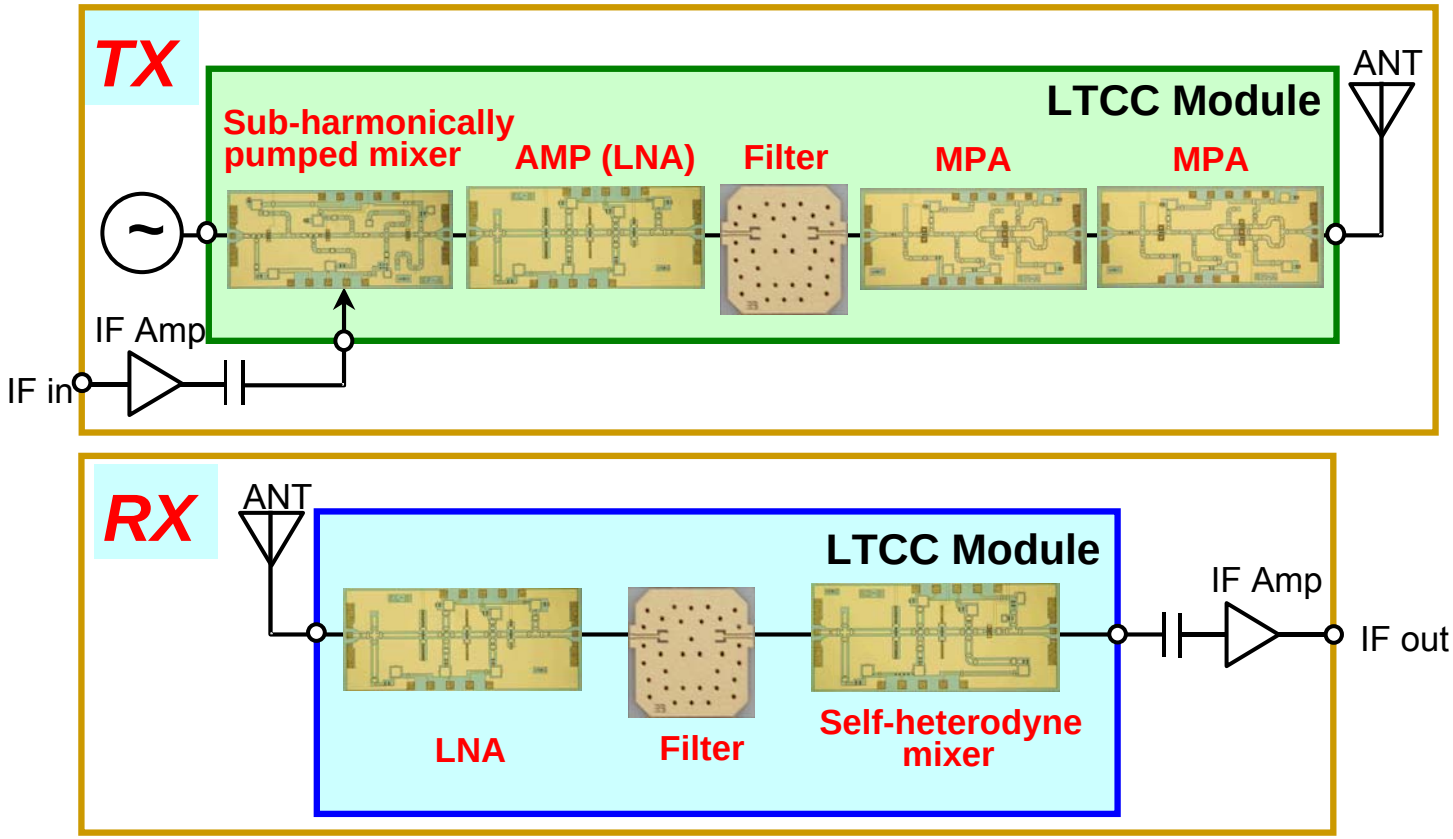
Material Absorption at 60 GHz

	60 GHz	2.5 GHz
Pine board – ¾ ”	8 dB	1.5dB
Clay Brick	9 dB	2 dB
Glass with wire mesh	10.2 dB	7.7 dB
Asphalt shingle	1.7 dB	1.5 dB
Drywall – 1”	6 dB	5 dB
Clear glass	3.6 dB	6.4 dB

*What about **oxygen absorption**?*

Atmosphere per 100m	**1.5 dB**	**0 dB**

Present 60-GHz links are expensive…

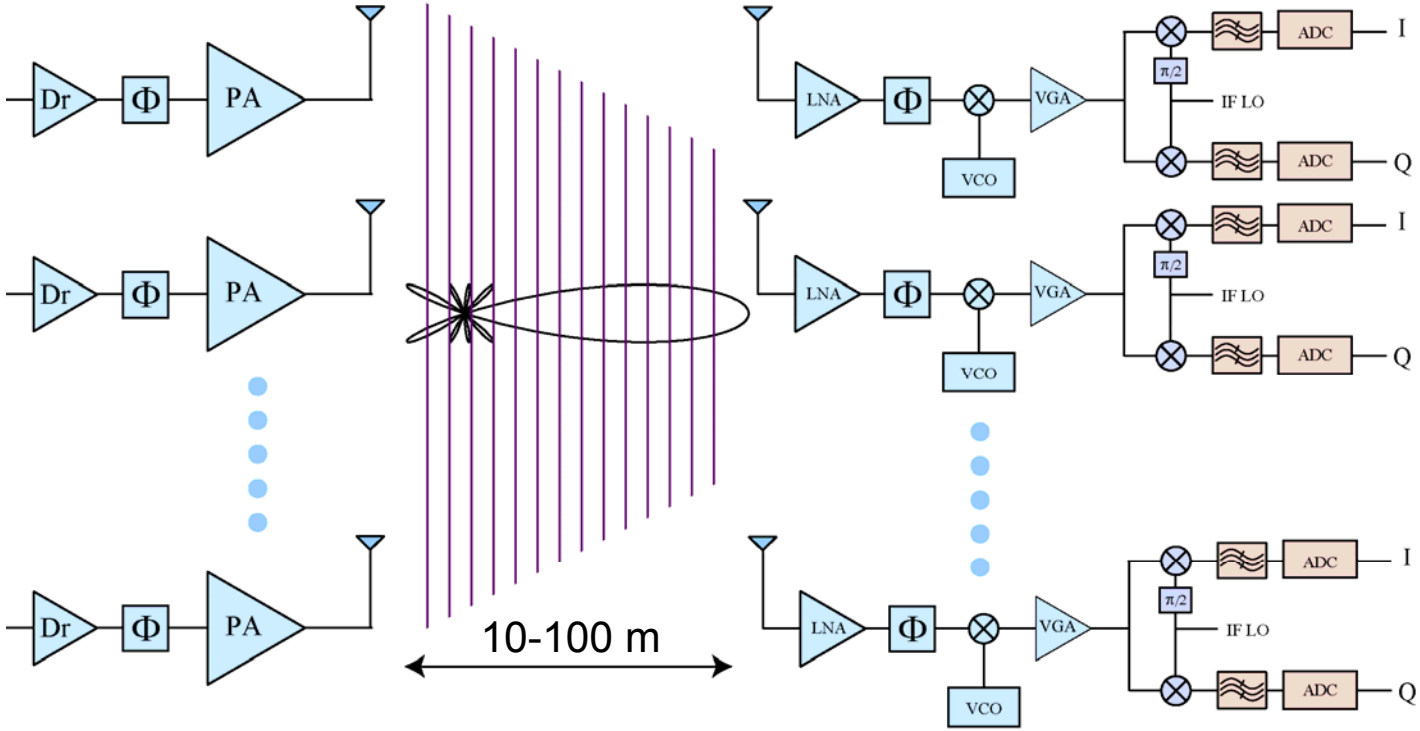


[Reference: "Millimeter-Wave Ad-hoc Wireless Access System II (6)", TSMMW'03 Technical Digest, pp. 61–64, March 2003]

Source: 802.15.3 Standards Proposal

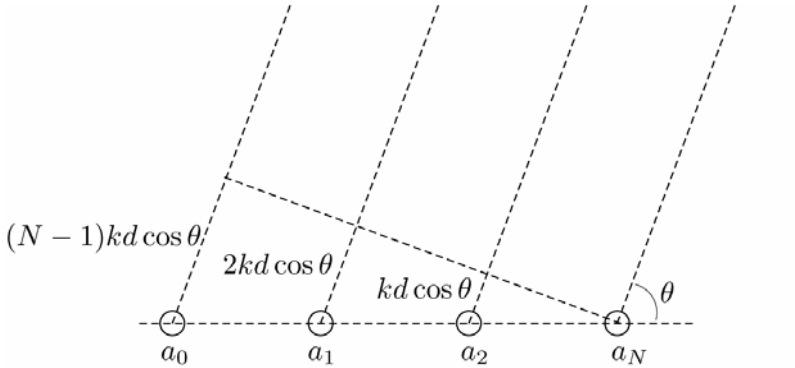
So can we do it in standard CMOS?

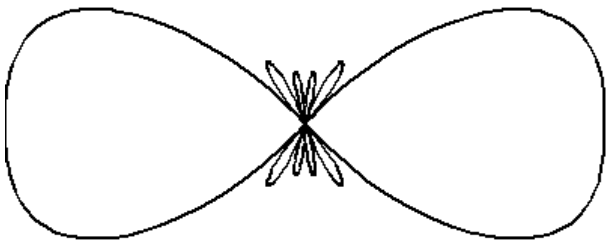
60 GHz CMOS Wireless LAN System



- Objective: Enable a fully-integrated low-cost Gb/s data communication using 60 GHz band.
- Approach: Employ emerging standard CMOS technology for the radio building blocks. Exploit antenna array for improved gain and resilience.

Advantages of Antenna Array





- Antenna array is dynamic and can point in any direction to maximized the received signal
- Enhanced receiver/transmitter antenna gain (reduced PA power, LNA gain)
- Improved diversity
- Reduced multi-path fading
- Null interfering signals
- Capacity enhancement through spatial coding
- Spatial power combining means
  - Less power per PA (~10 mW)
  - Simpler PA architecture
  - Automatic power control

$$f(\theta) = a_0 e^{j(N-1)\overbrace{kd\cos\theta}^{\Psi}} + a_1 e^{j(N-2)\Psi} + \cdots + a_N$$

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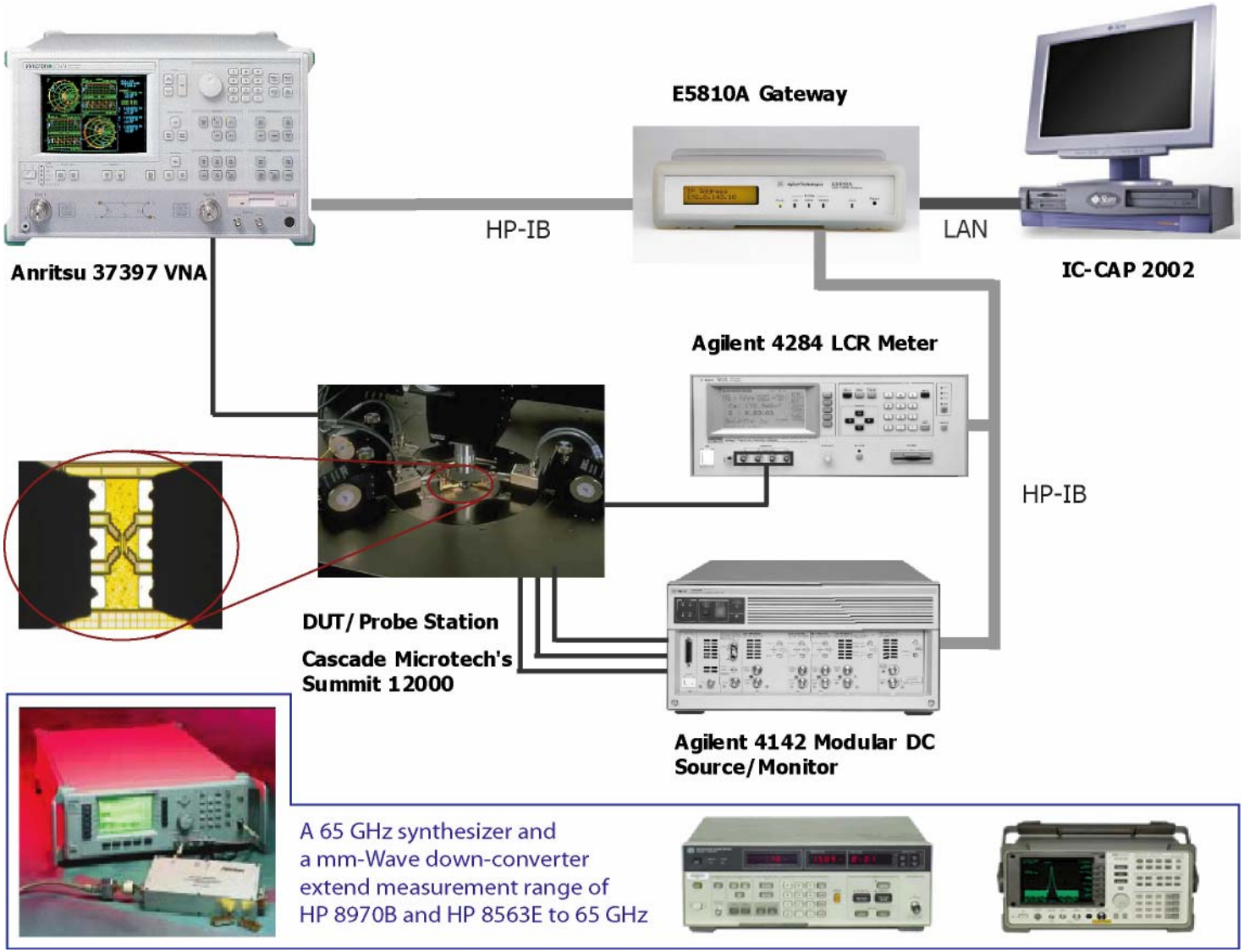
Importance of Modeling at 60 GHz

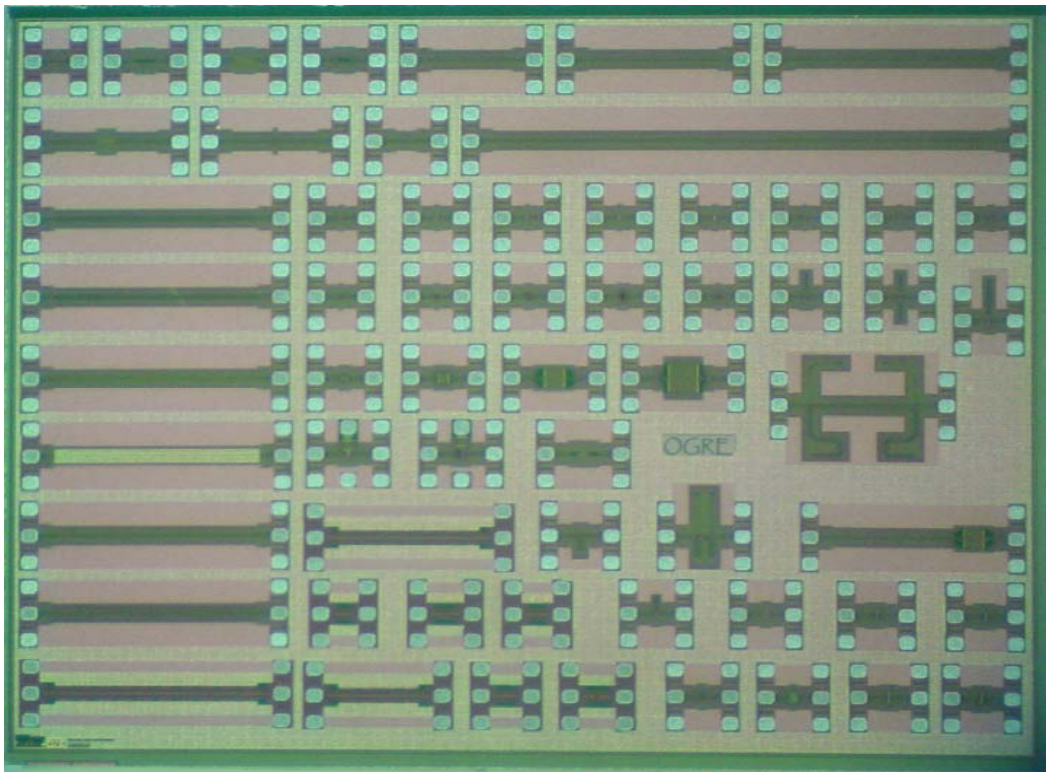
- Transistors
  - Compact model not verified near f_{max}/f_t
  - Table-based model lacks flexibility
  - Parasitics no longer negligible
  - Highly layout dependent
- Passives
  - Need accurate reactances
  - Loss not negligible
  - Scalable models desired
  - Allows comparison of arbitrary structures

Accurate models required for circuits operating near limit of process

Measurement Setup



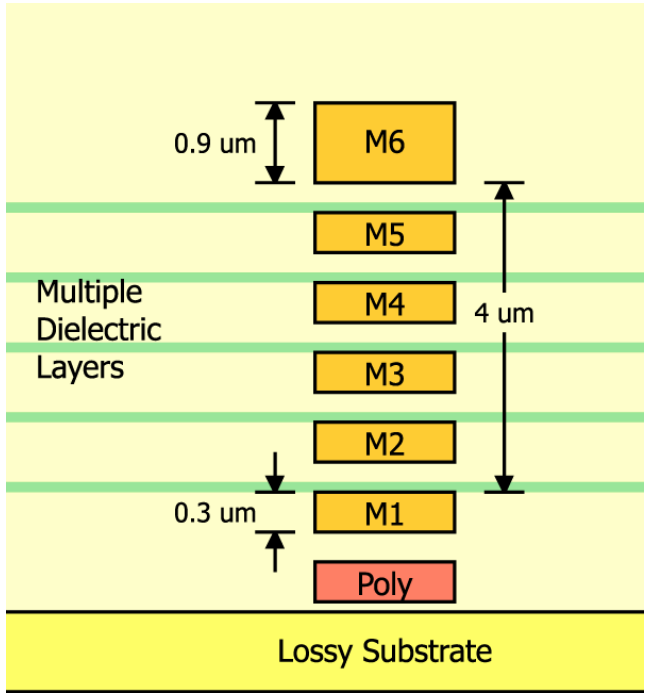
Device Test Chip

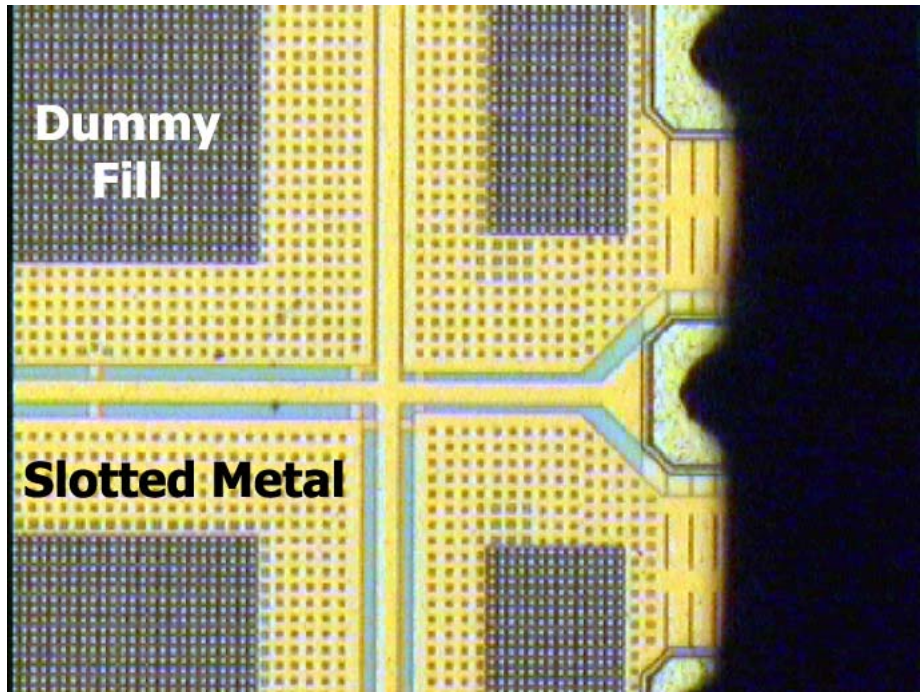


Test Chip Includes:

- Multi-line TRL calibration
- Transmission lines
  - Coplanar (CPW)
  - Microstrip
- Fingered capacitors
  - Coupling
  - Supply bypass
- Poly/N-well caps
- Passive filters
- RF NMOS layout with varying W_F, N_F

Modeling challenges for modern CMOS

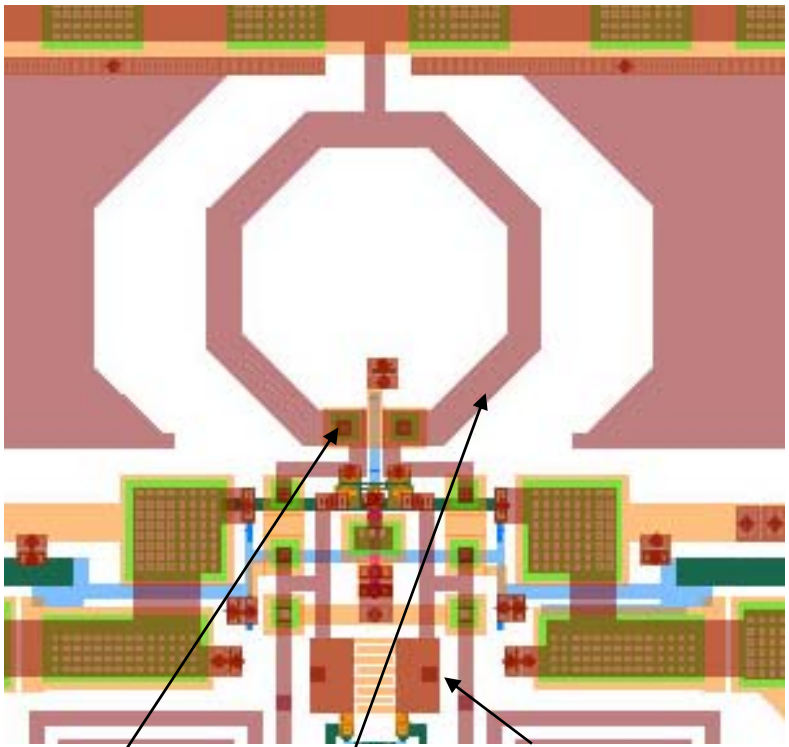


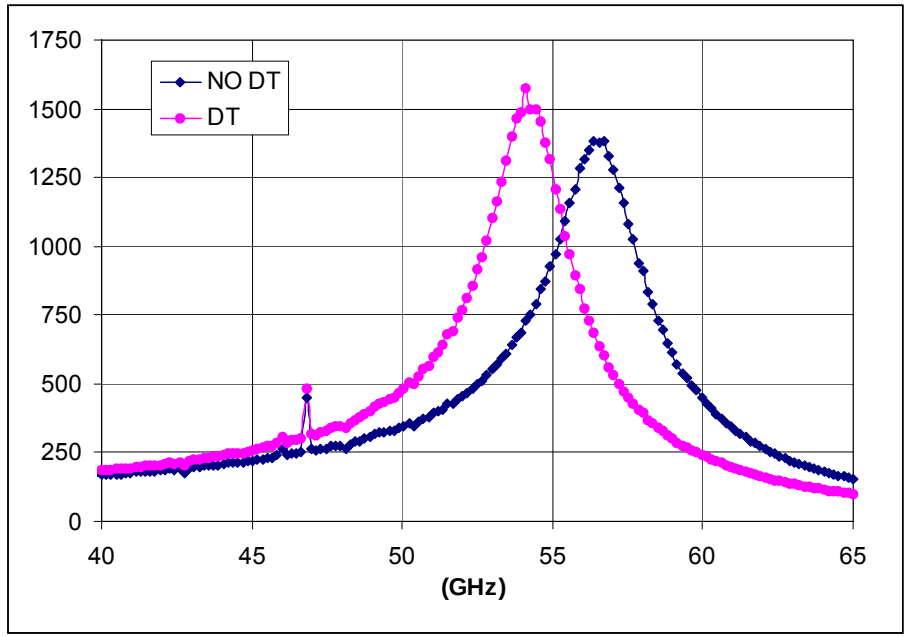


- Lossy substrate (~10 Ω-cm)
- 6–8 metal levels (copper)
- Chemical mechanical planarization (20-80% metal density)
  - Slots required in metal lines
  - Fill metal in empty areas
- Multiple dielectric layers

Ring Inductors Measurements

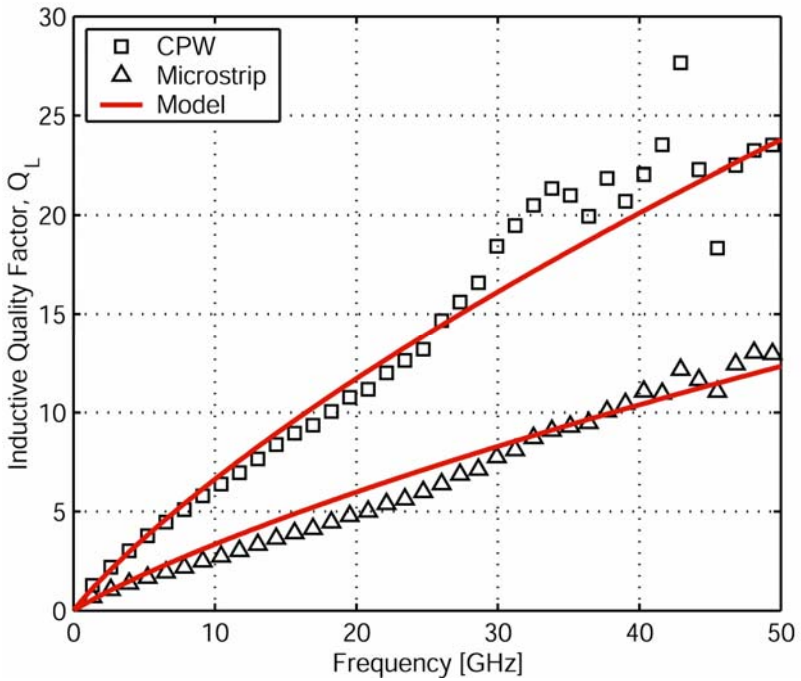
Low Loss MIM Cap and Inductor Ring
Tightly Coupled for Low Loss





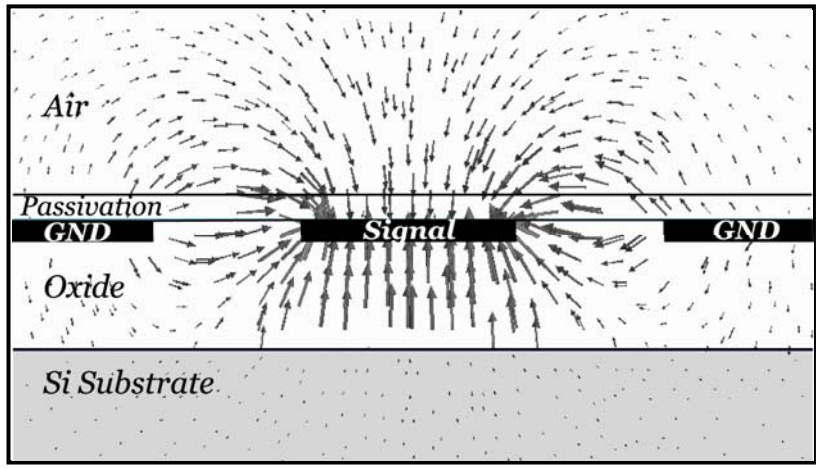
- Tank resonates at design frequency (56 GHz)
- Tank with DT (deep-trench) array has slightly higher Q but lower SRF
- Loaded Q > 20 encouraging measurement

Co-planar (CPW) and Microstrip T-Lines

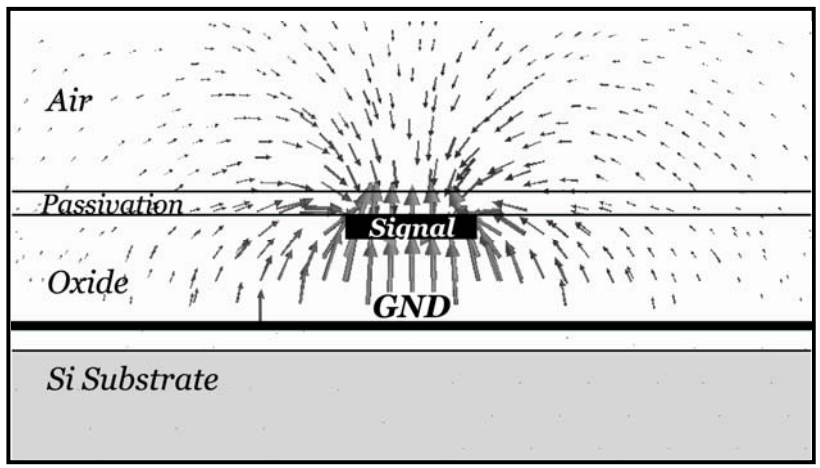


- Microstrip shields EM fields from substrate
- CPW can realize higher Q inductors needed for tuning out device capacitance
- Use CPW

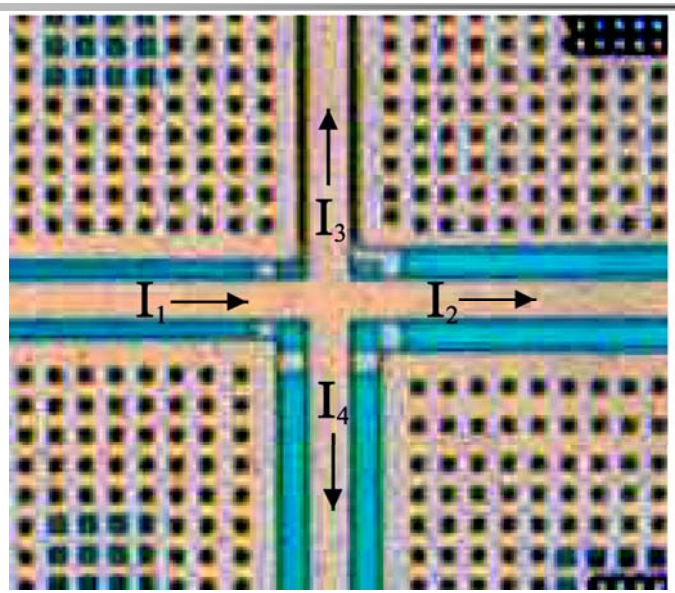
CPW

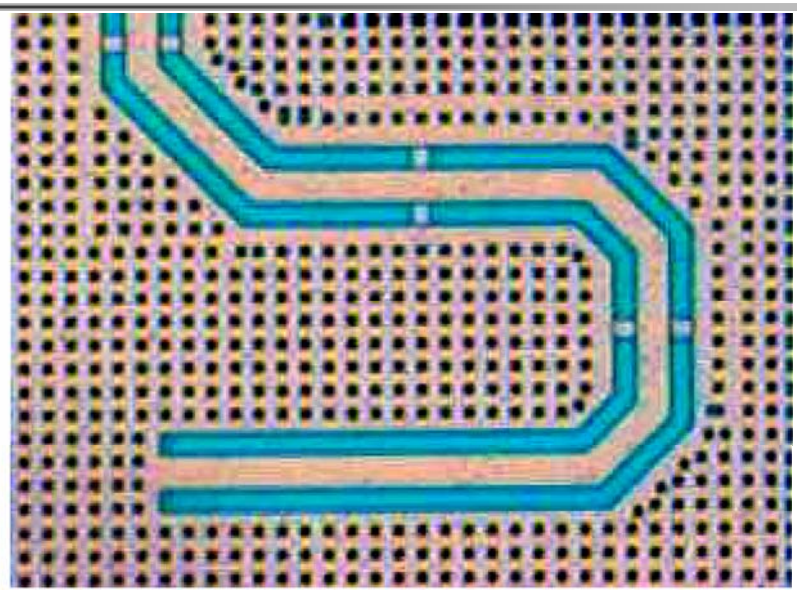


Microstrip



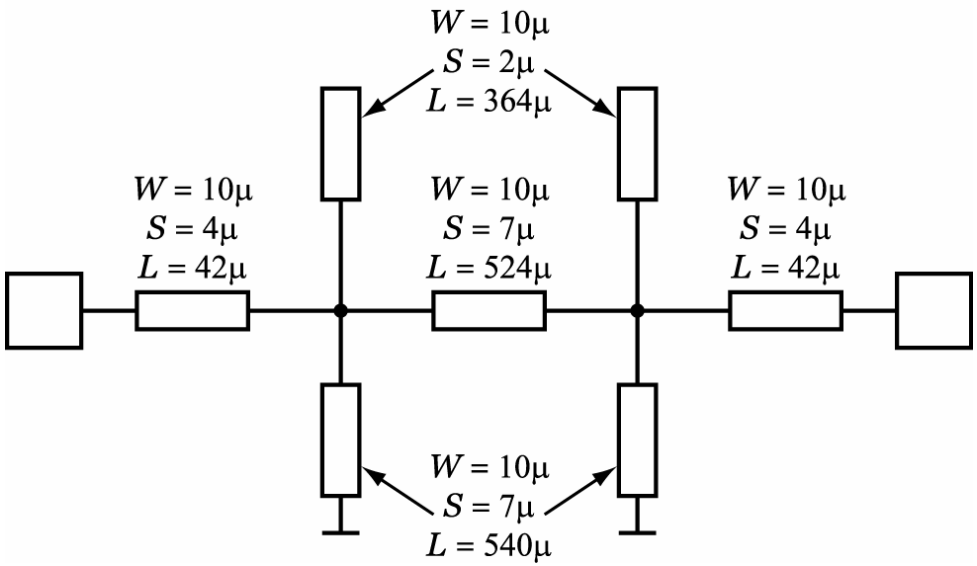
Co-planar waveguide layout issues

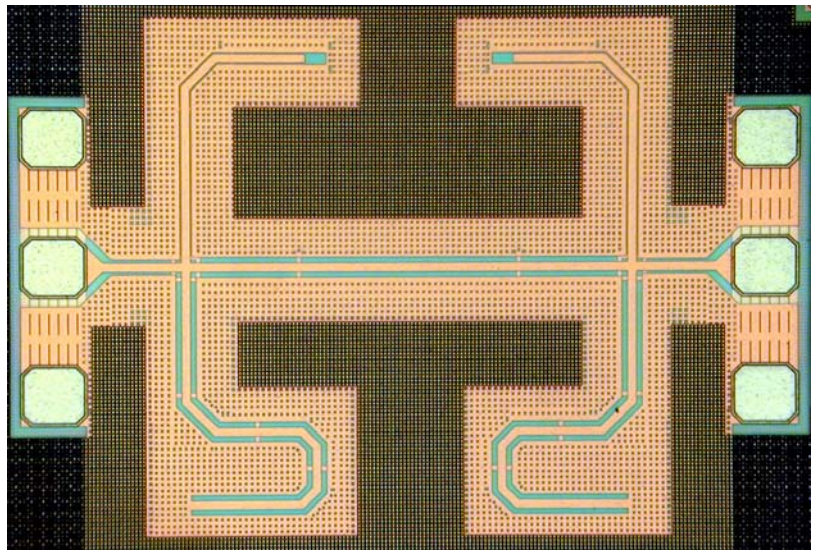




- Bridges suppress odd-mode propagation
  - Keep ground currents ***balanced***
  - Advantage of the multi-layer metallization in CMOS
- Signal-to-ground spacing
  - Used to set Z_0
  - Helps confine EM fields
  - Effects of bends are reduced

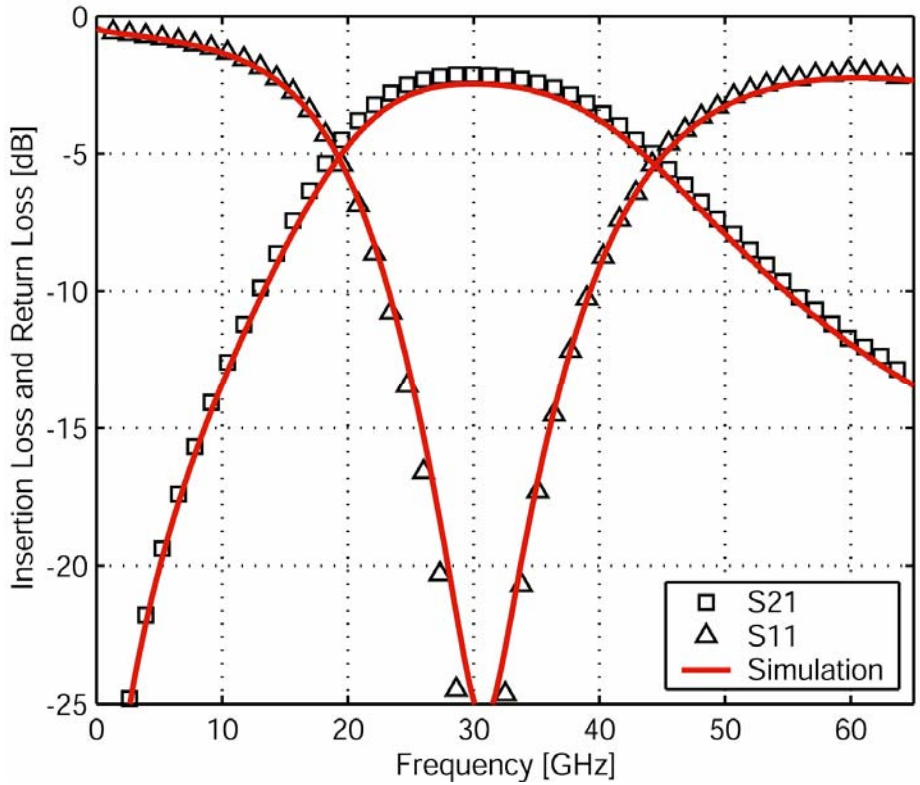
30-GHz Co-Planar Waveguide Filter





- 30-GHz center frequency
- Composed of scalable transmission lines
- Tests accuracy of transmission line modeling

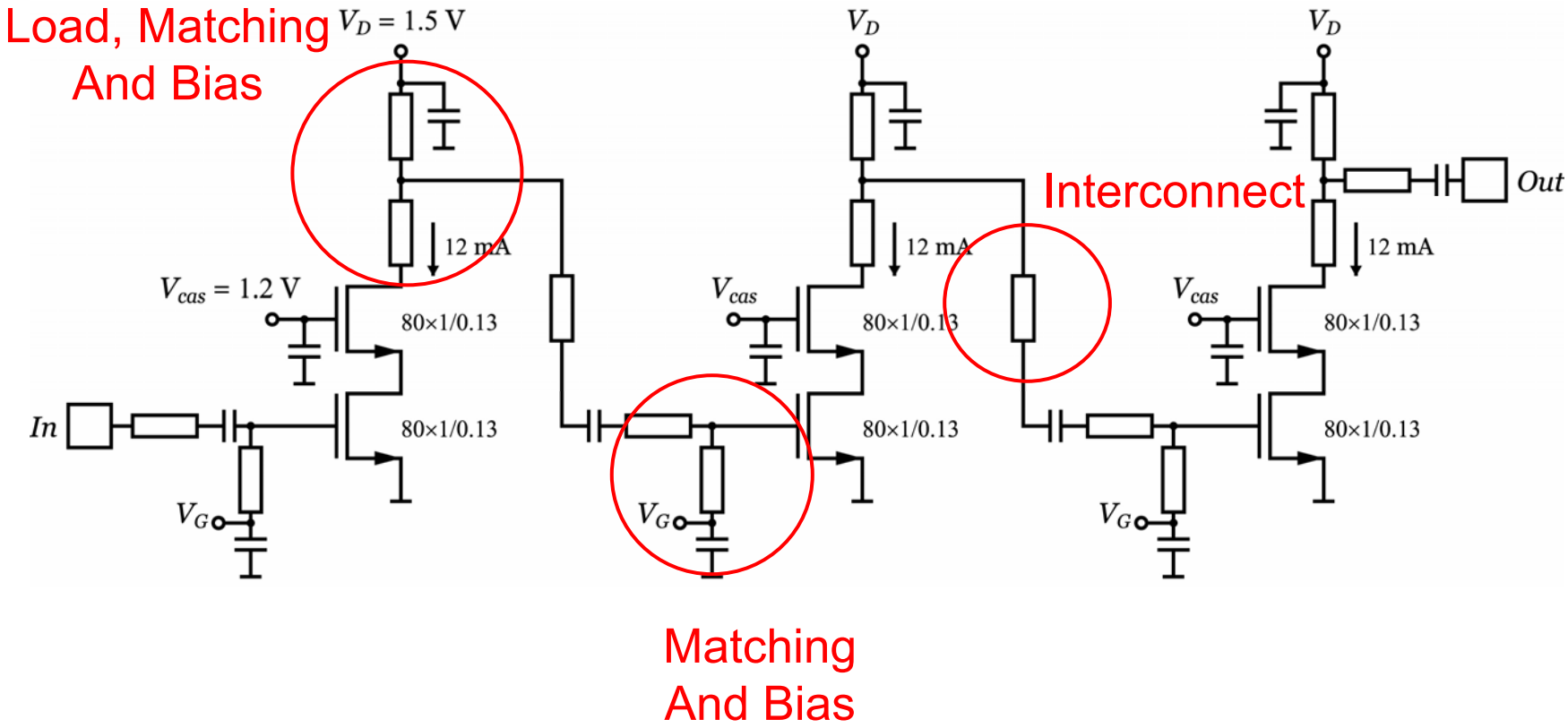
Filter Measurements vs. Models



From the accurate modeling we can conclude

- Negligible coupling between lines
- Bends, junctions, bridges have small effect

Key Passive Devices



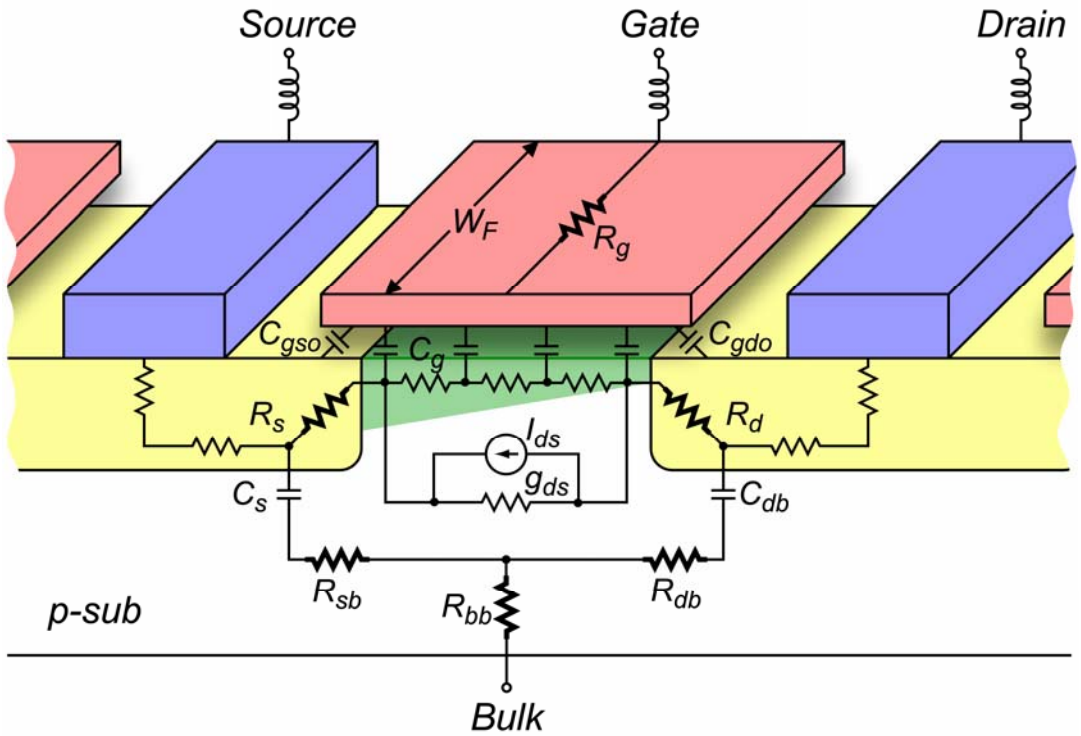
- Short transmission lines (T-lines) are used as inductors (to tune out FET parasitics)
- T-lines are also used for impedance matching, interconnect, and biasing
- Bypass and coupling capacitors and varactors also characterized at 60 GHz

How fast is standard 130-nm CMOS?

First what is the best metric, f_{max} or f_t ?

- f_t , the unity current gain, is useful for estimating circuit bandwidths at low frequency
  - Ignores the parasitic resistive losses
  - Doesn't assume optimal matching
  - Affected by wiring capacitance
- f_{max} , the frequency when the device becomes passive, describes the real limitation
  - Fundamental property of the device
  - Limited by resistive losses that reduce power gain
  - Requires an optimized layout

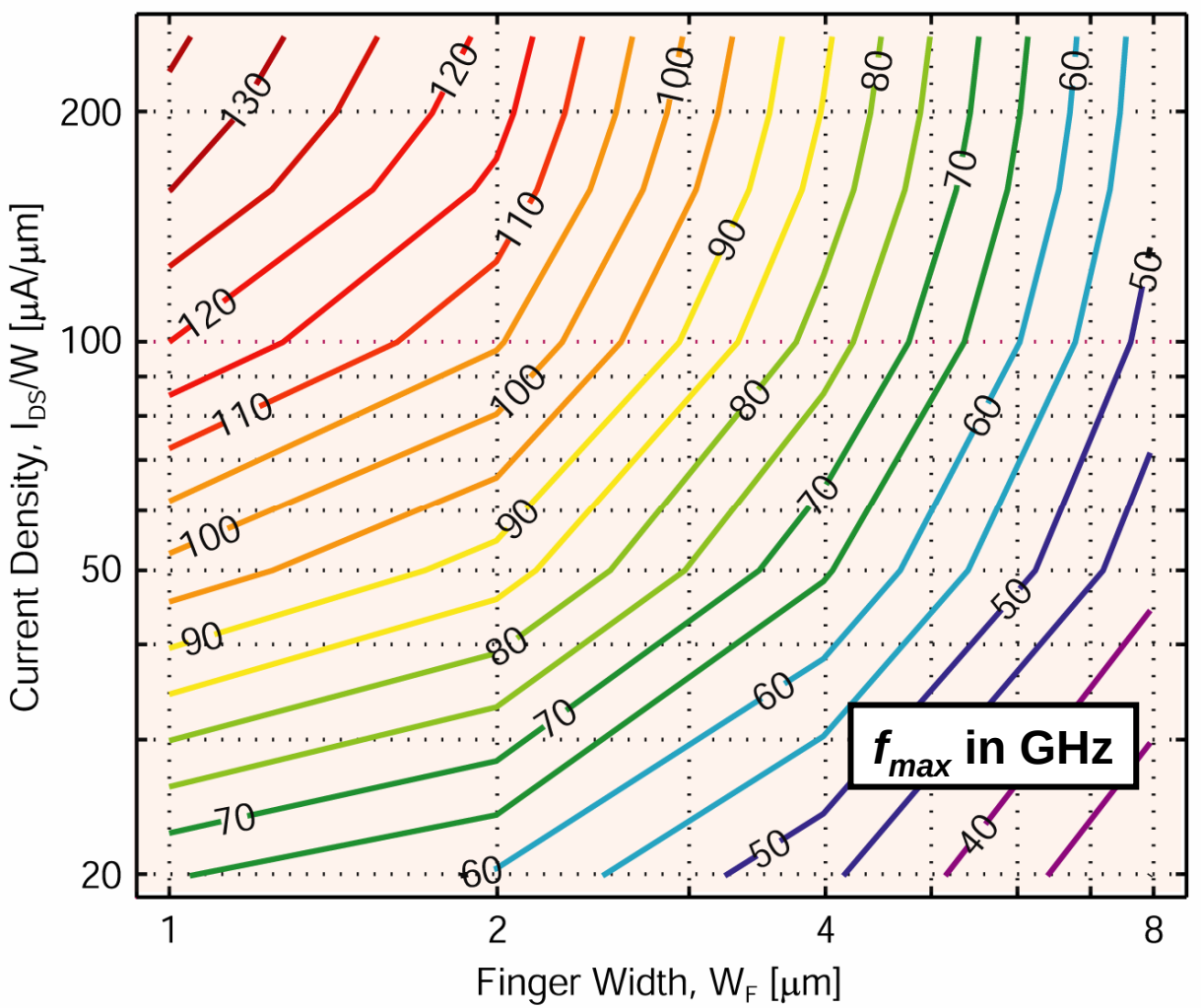
Layout for Maximizing f_{max}

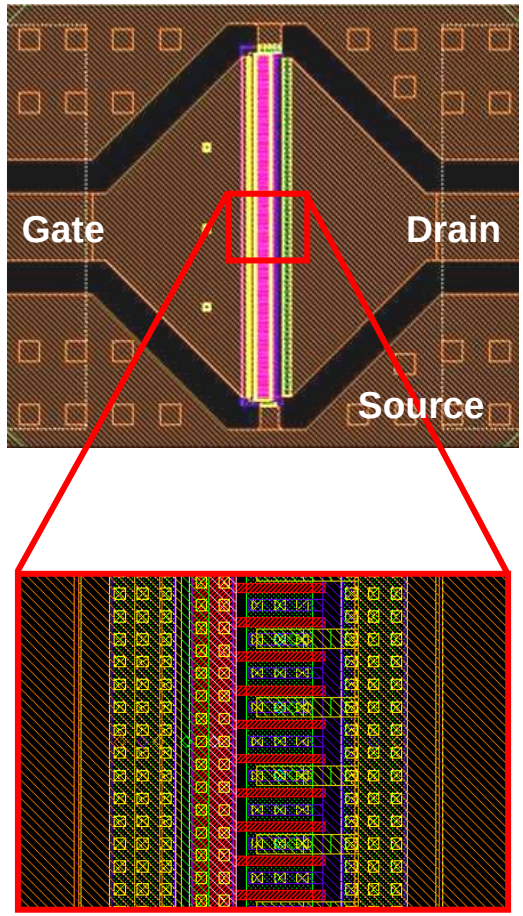


Minimize all resistances

- R_g – use many small parallel gate fingers, <1 μm each
- R_{sb}, R_{db}, R_{bb} – substrate contacts <1–2 μm from device
- R_s, R_d – don't use source/drain extensions to reduce L

f_{max} vs. finger width





Increasing gate resistance →

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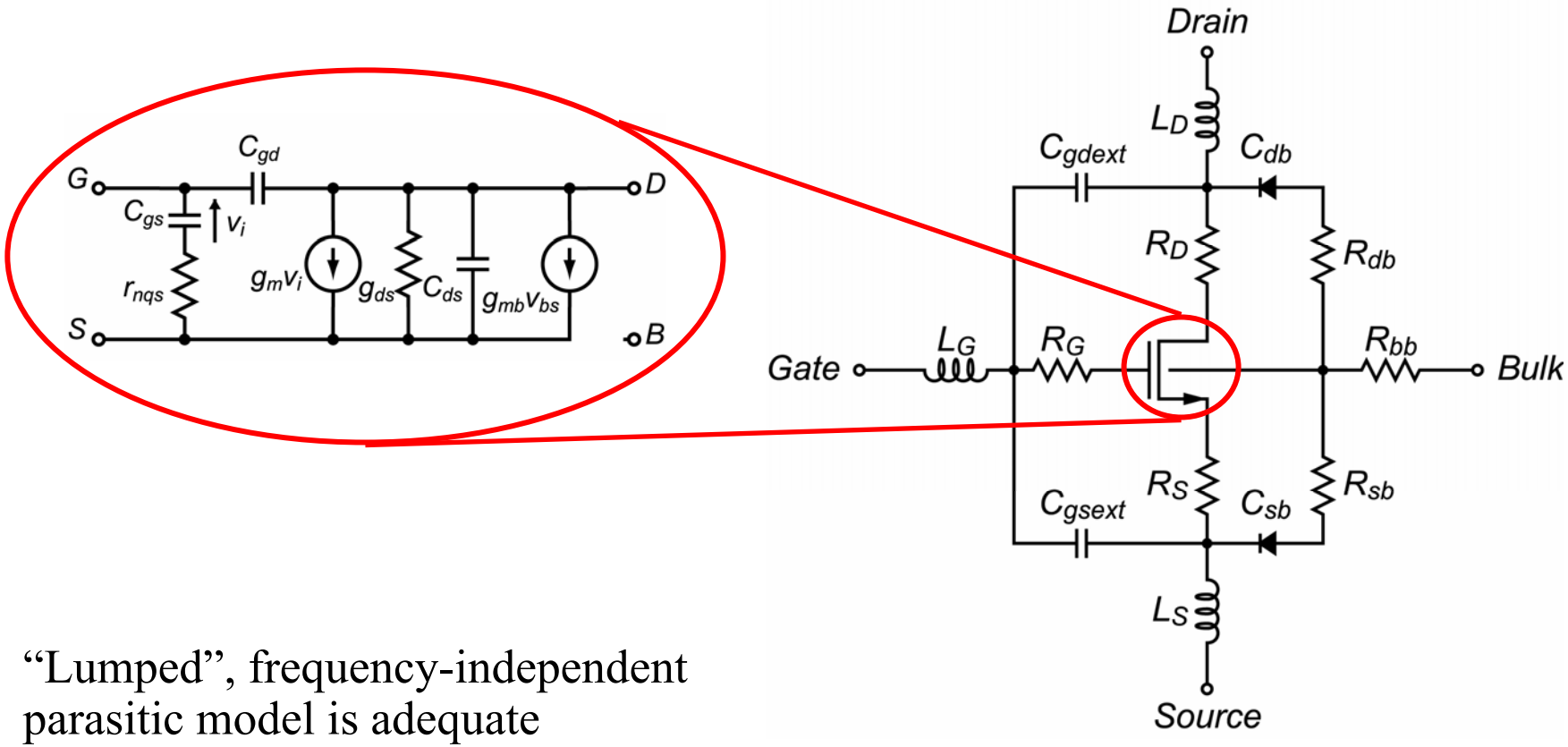
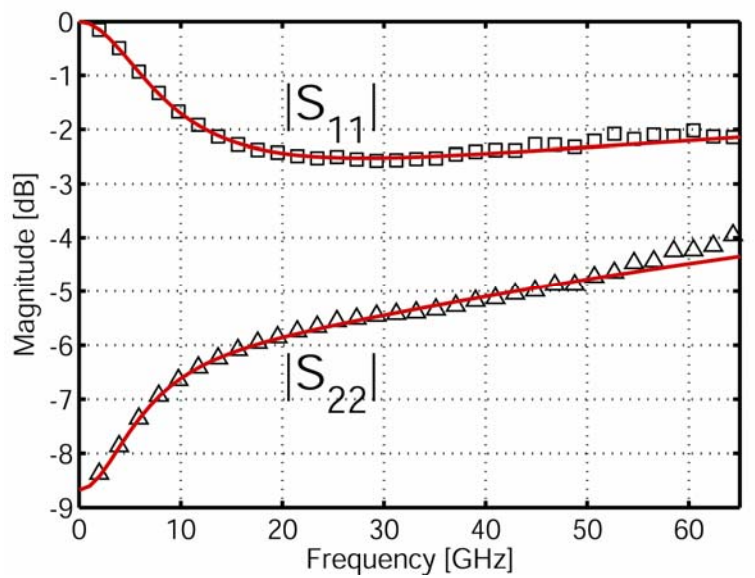
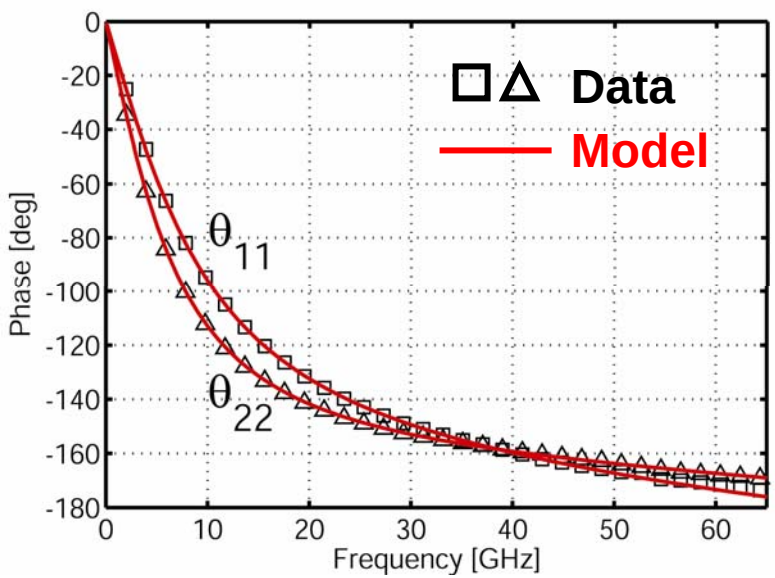
Extended Transistor Modeling

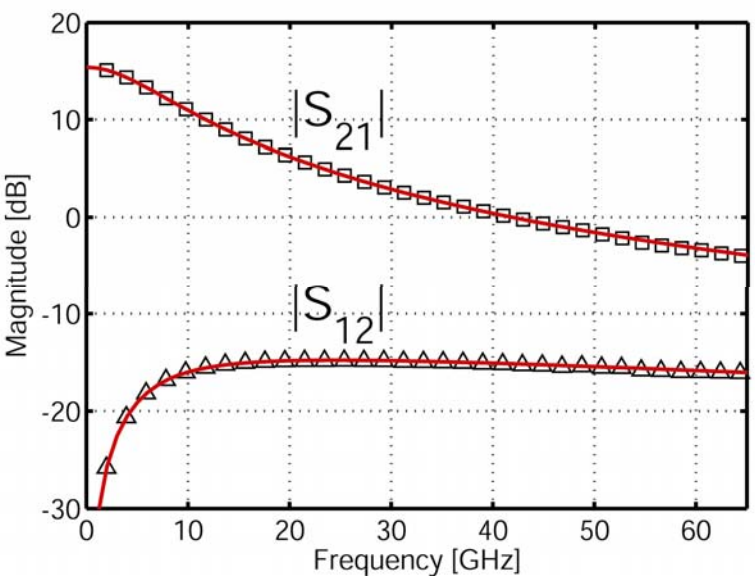


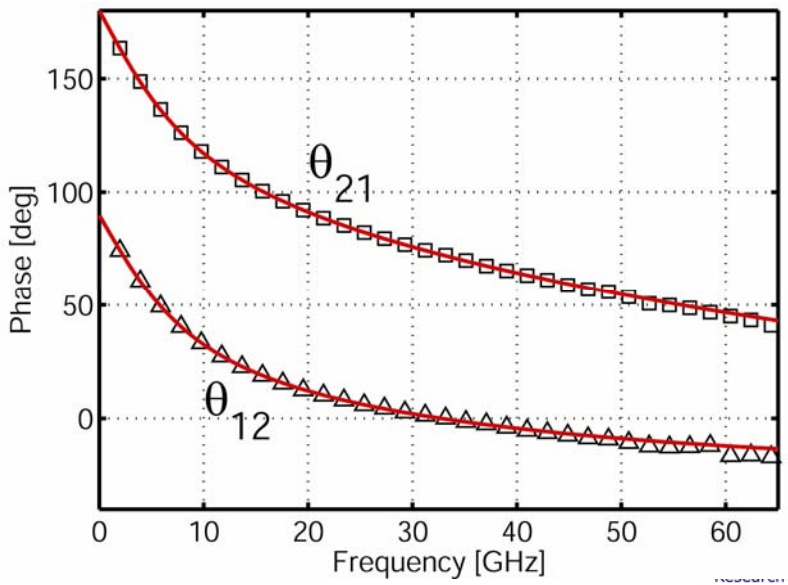
- "Lumped", frequency-independent parasitic model is adequate
- Bias-dependent small-signal transistor model for highest accuracy
- Large-signal BSIM3v3 model for nonlinearities and bias dependence

Small-signal model fitting – 0–65 GHz

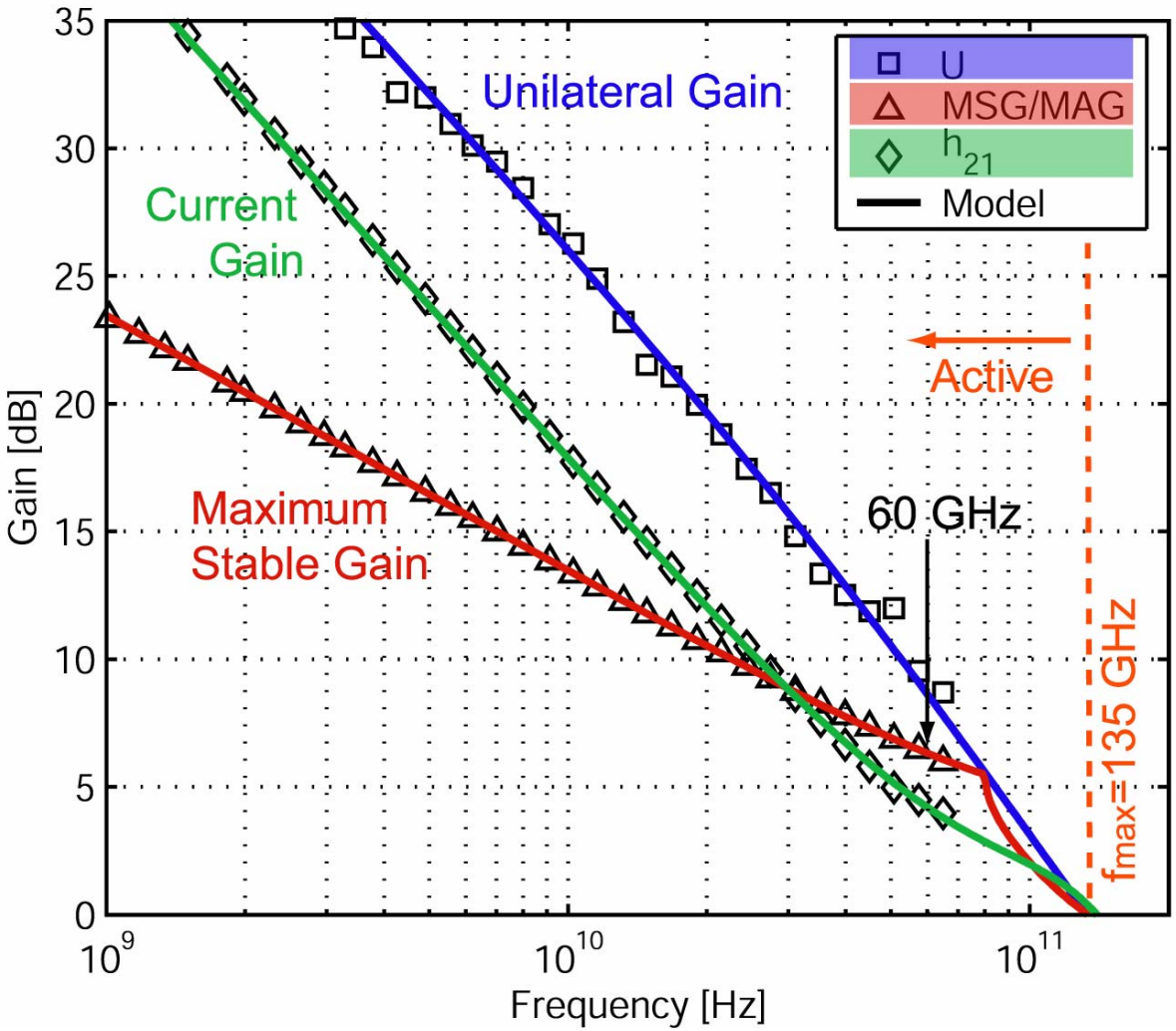


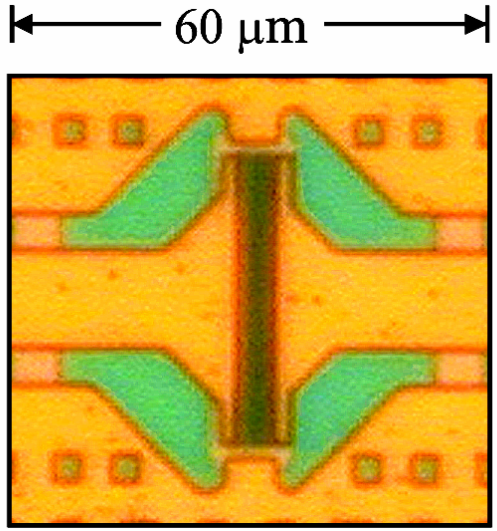






130-nm CMOS Device Performance





V_{GS} = 0.65 V

V_{DS} = 1.2 V

I_{DS} = 30 mA

W/L = 100x1u/0.13u

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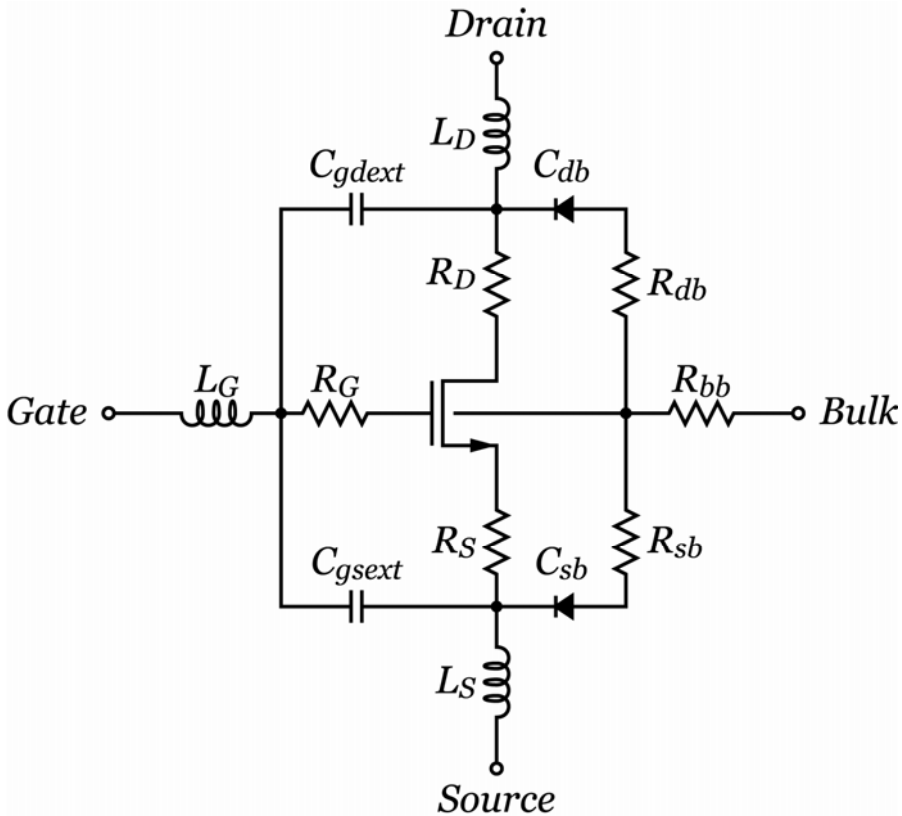
mm-Wave BSIM Modeling

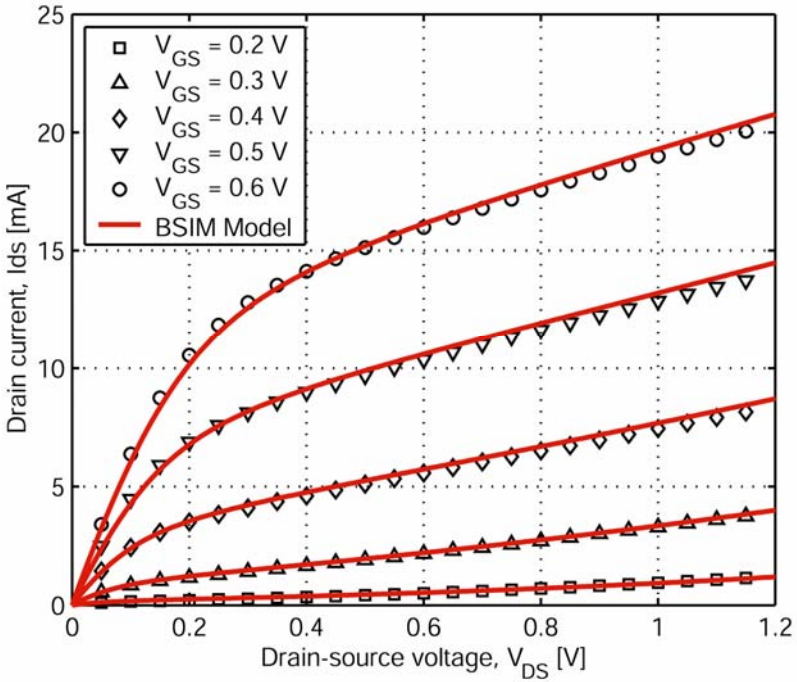
- Compact model with extrinsic parasitics
- DC I-V curve matching
- Small-signal S-params fitting
- Large-signal verification

- Challenges:
  - Starting with a sample which is between typical and fast
  - Millimeter-wave large-signal measurements
  - Noise
  - 3-terminal modeling

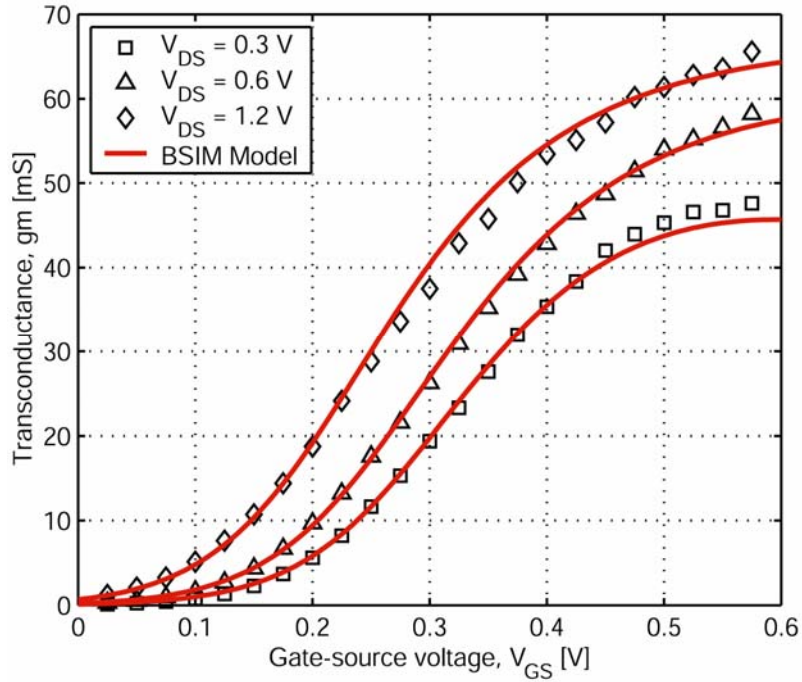


Reference: "Large-Signal Millimeter-Wave CMOS Modeling with BSIM3", RFIC'04
Sohrab Emami, Chinh H. Doan, Ali M. Niknejad, and Robert W. Brodersen

DC Curve Fitting



Measured and modeled IDS vs. VDS.

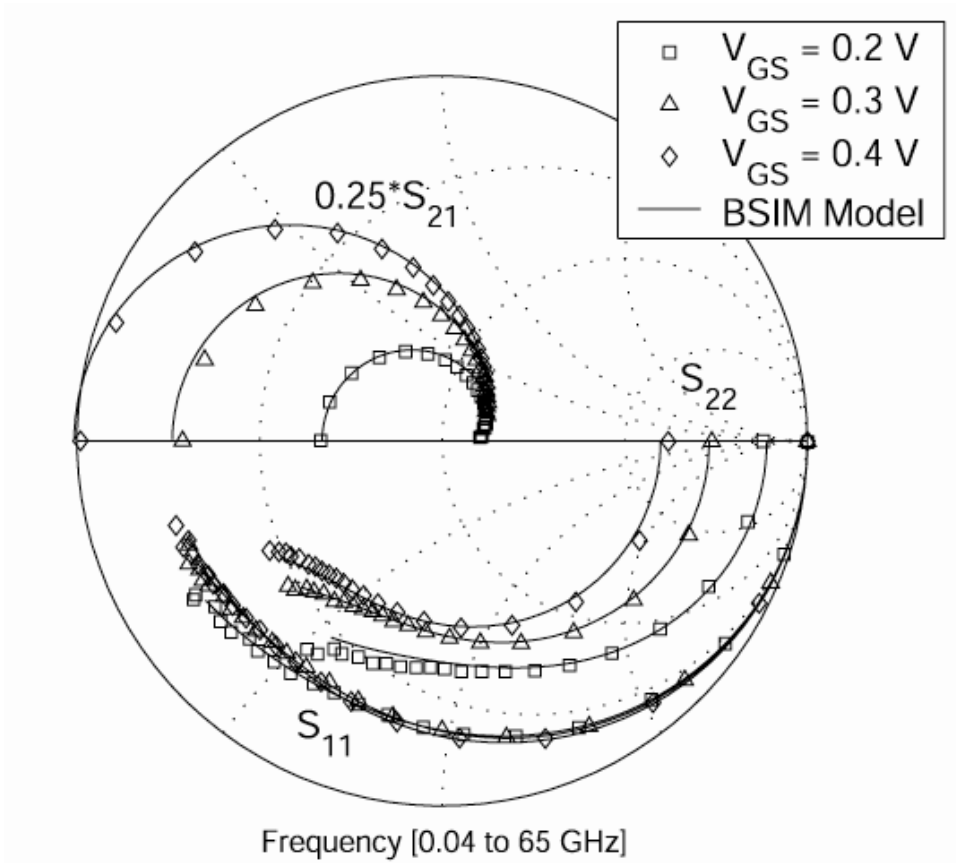


Measured and modeled gm vs. VGS.

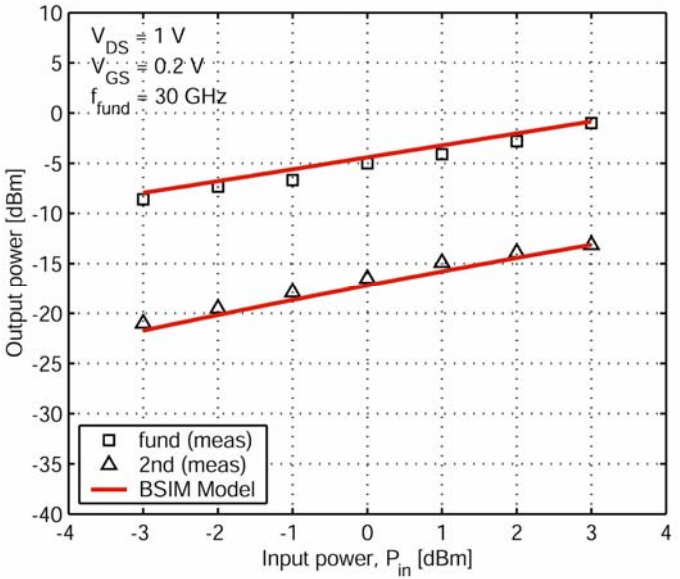
- I-V measurements were used to extract the core BSIM parameters of the fabricated common-source NMOS.

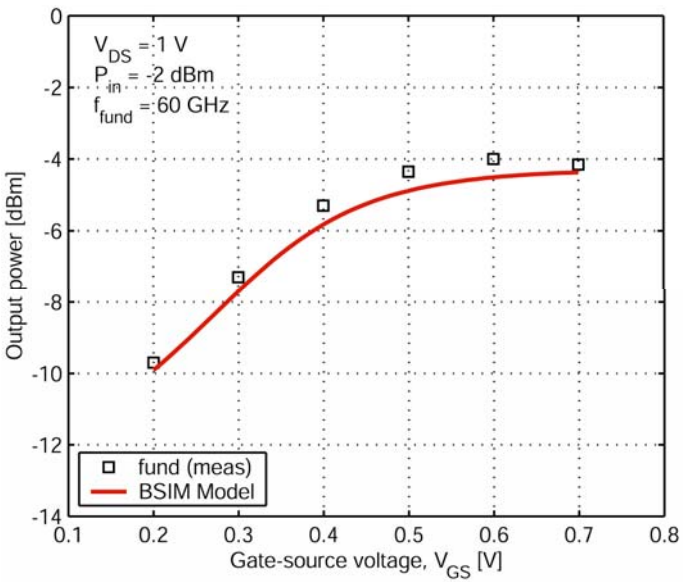
Model Extraction: Small-Signal

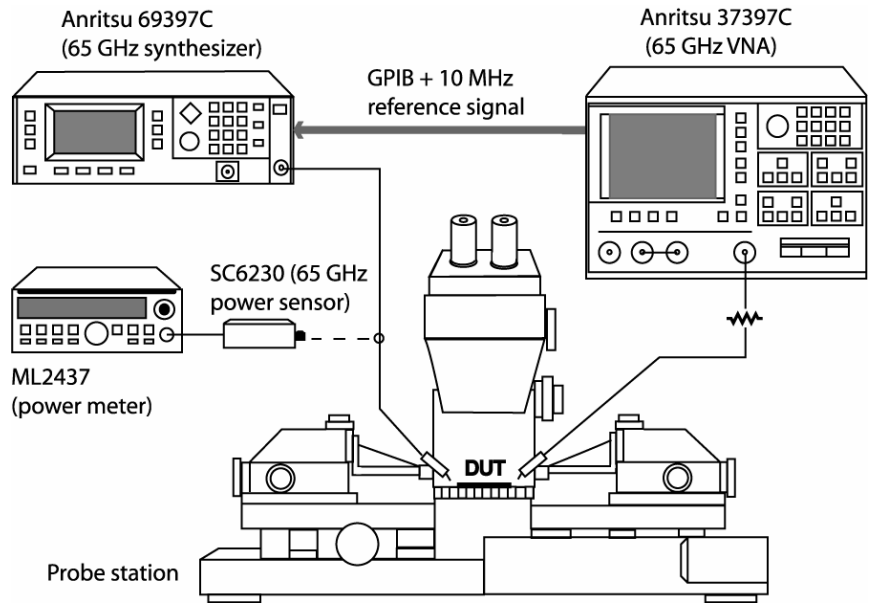
- Extensive on-wafer S-parameter measurement to 65 GHz over a wide bias range.
- Parasitic component values extracted using a hybrid optimization algorithm in Agilent IC-CAP.
- The broadband accuracy of the model verifies that using lumped parasitics is suitable well into the mm-wave region.



Large-Signal Verification







- Harmonics power measurement
  - Class AB operation
  - Large-Signal amplification at 60 GHz

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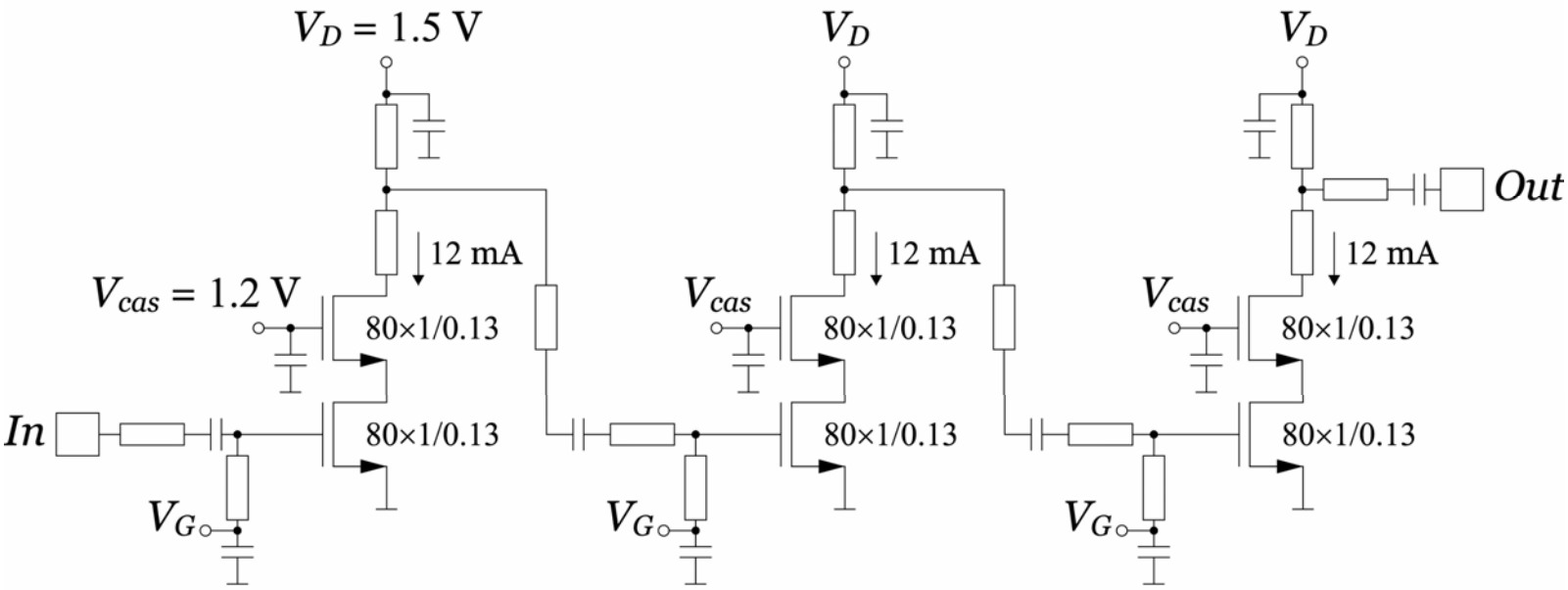
Challenges for 60-GHz Amplifiers

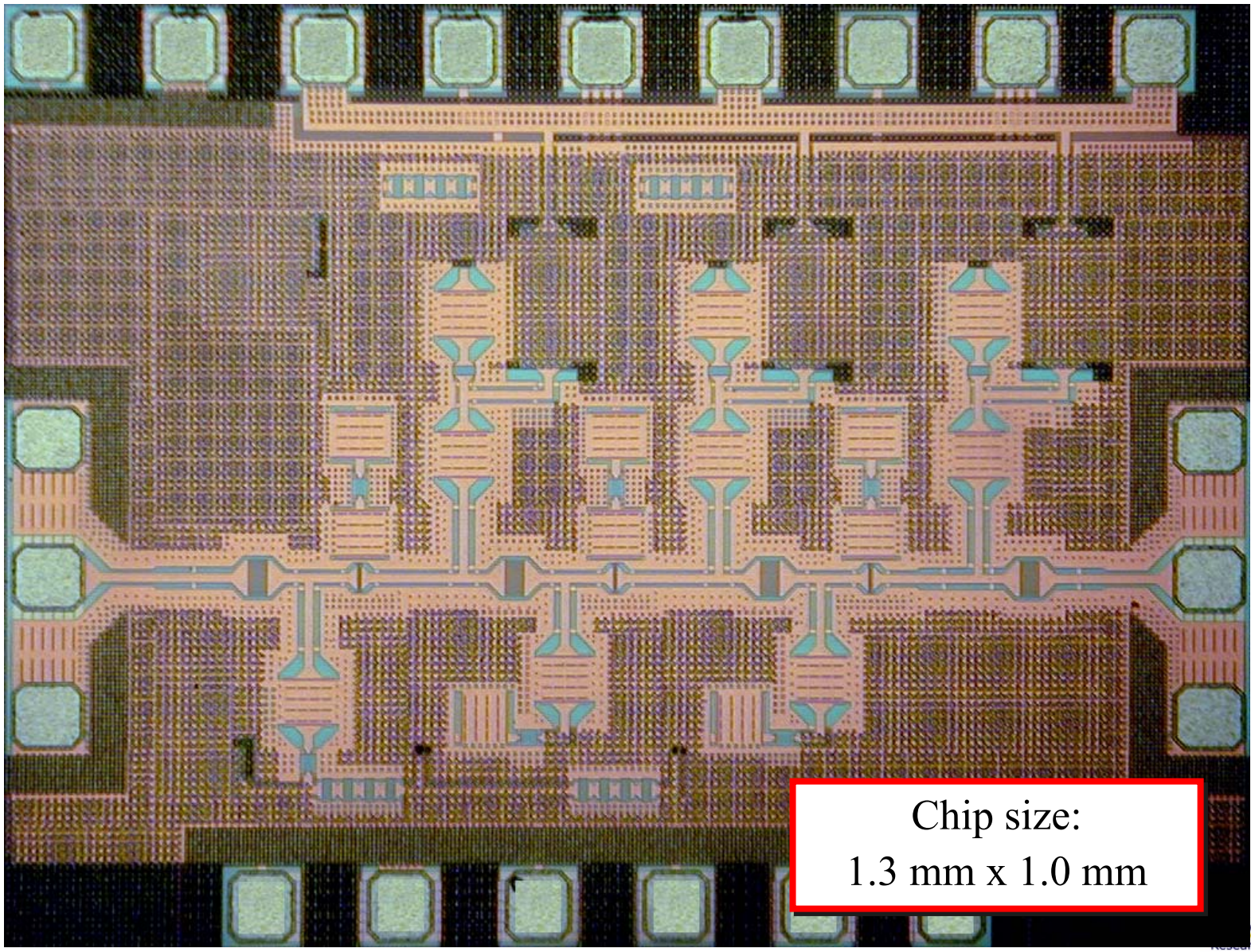
- Low transistor gain at 60 GHz
  - Optimized transistor layout
  - Require accurate device models
- Impedance matching networks
  - Need low-loss passives
  - Scalable models to design complex networks
- Broadband stability
  - Miller capacitance
  - Bias oscillations
- High output power or low noise

60-GHz Amplifier Schematic

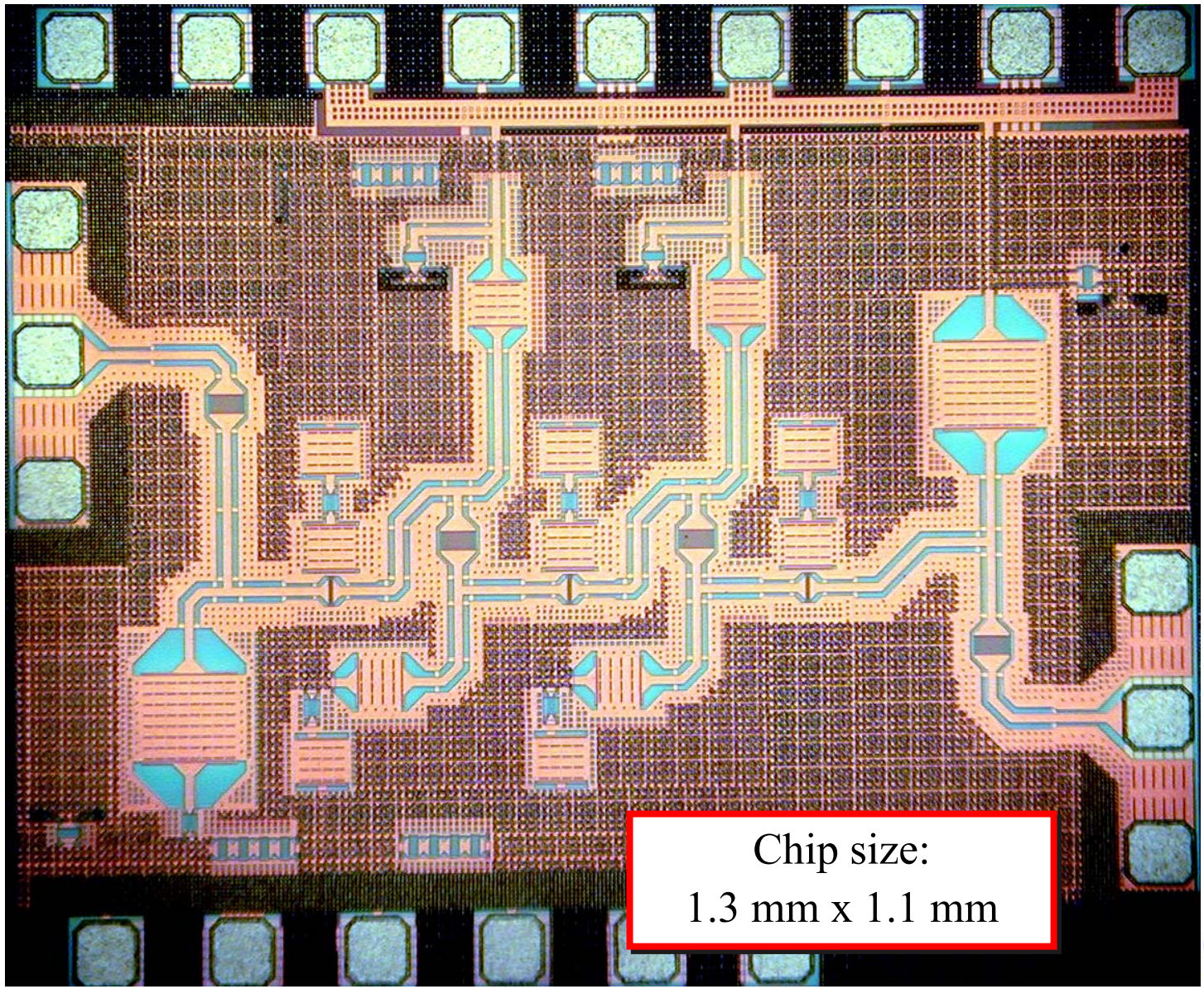


- 3-stage cascode amplifier design
- Cascode transistors improve isolation, stability
- Input/output matching networks designed to match 50 Ω
- Pads are included as part of amplifier
- Designed using only measured components

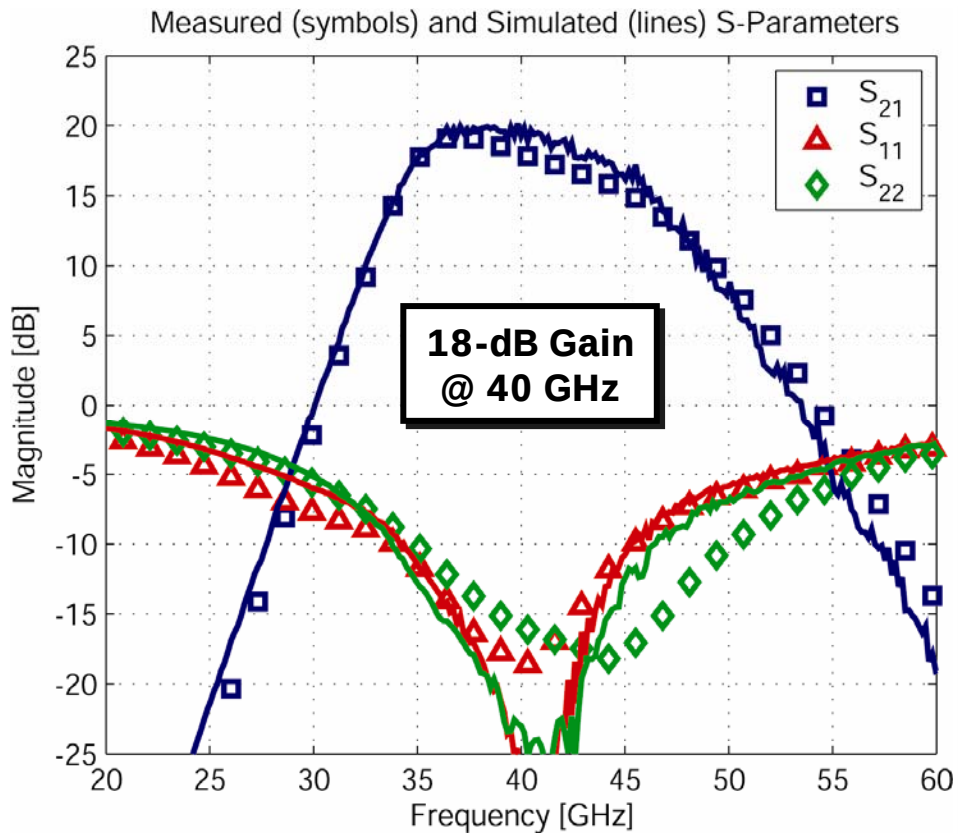
60-GHz Amplifier Layout

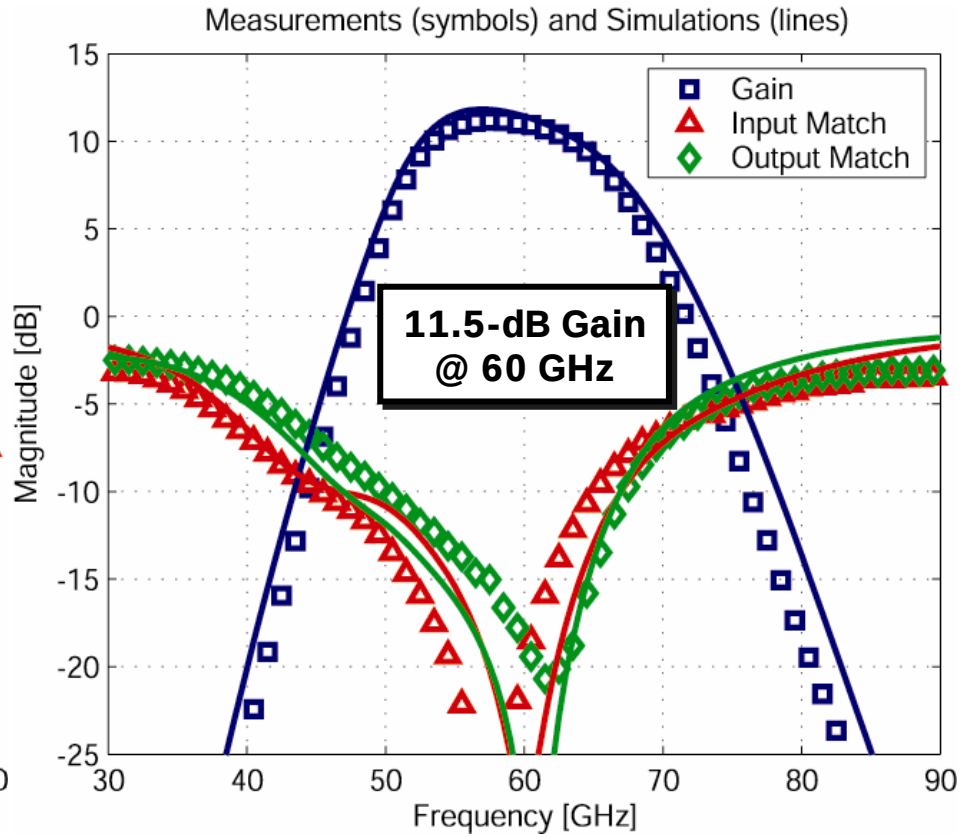


40-GHz Amplifier Layout



40-GHz and 60-GHz CMOS Amplifiers





- We have developed a design methodology that gives repeatable results for microwave CMOS design
- Power consumption: **36 mW** (40 GHz), **54 mW** (60 GHz)

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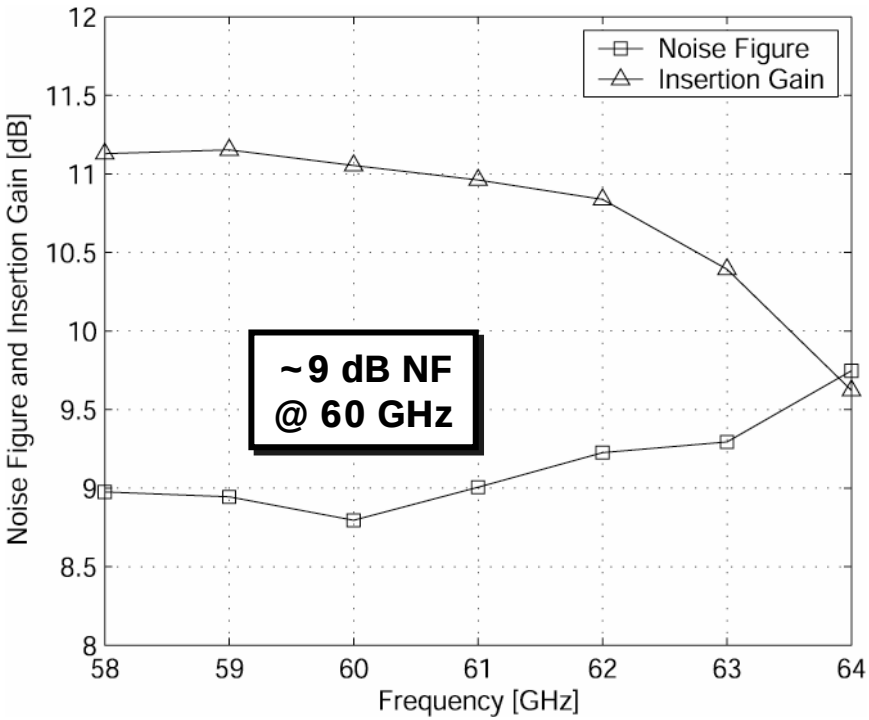
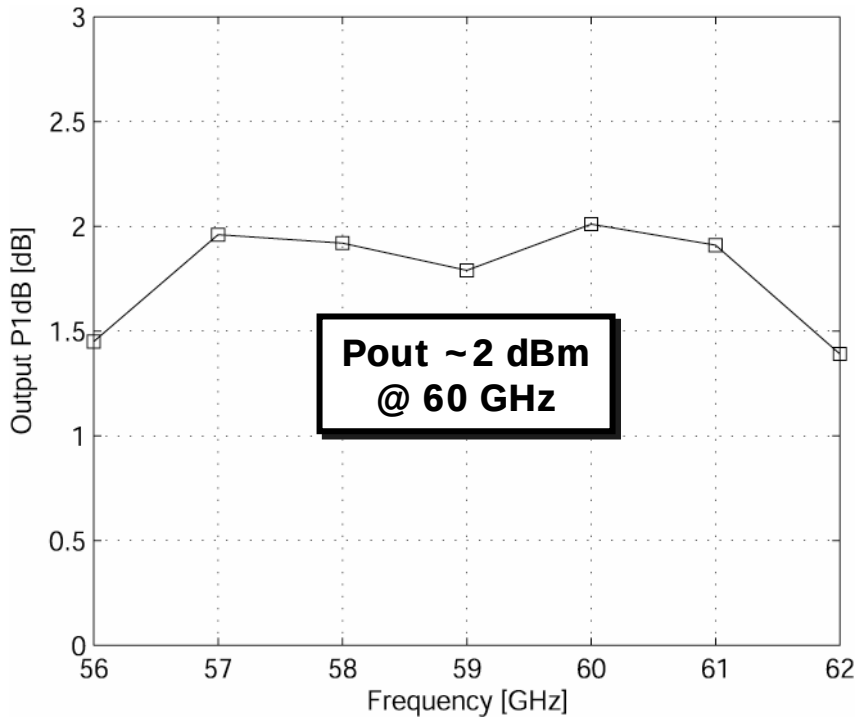
60-GHz Noise Figure and Compression





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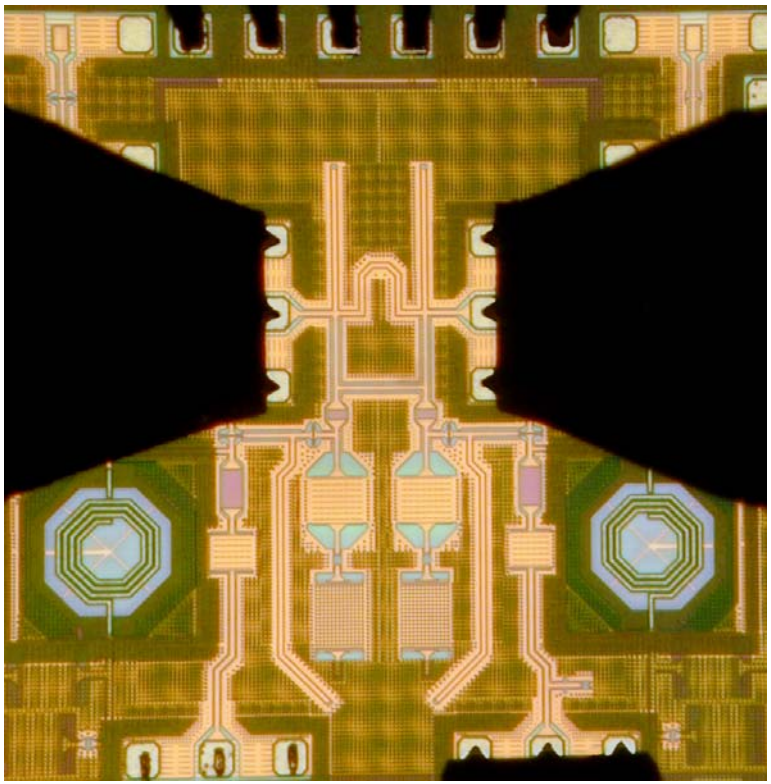
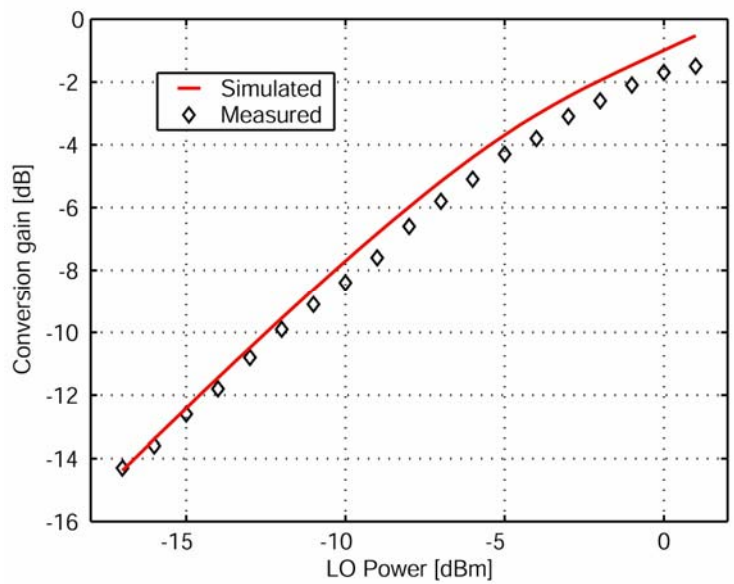
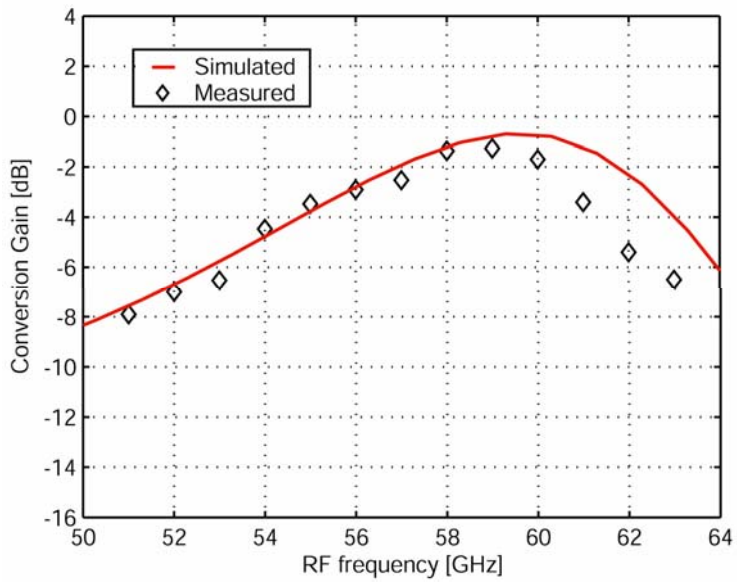
A 60 GHz CMOS Mixer



- Conversion loss is better than 2 dB for P_{LO}=0 dBm
- IF=2 GHz
- 6 GHz of bandwidth

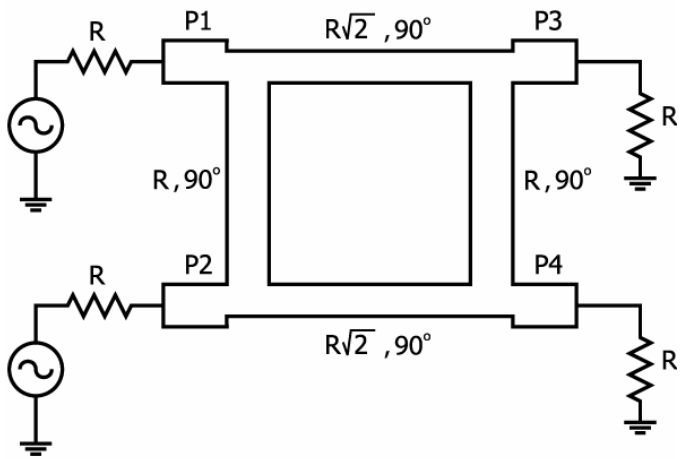




Research Center

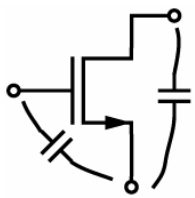
Combining LO and RF Signals

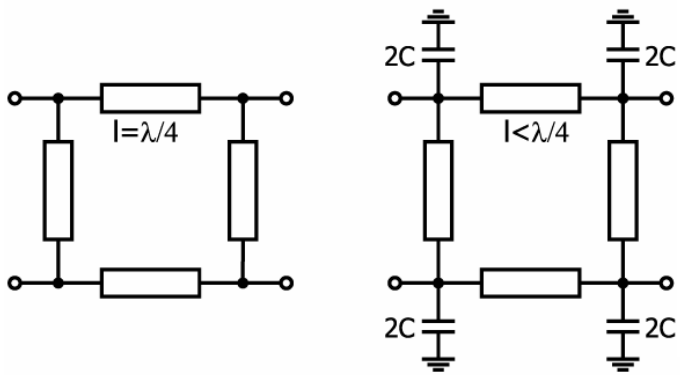
- Branch line 90º coupler
  - Long lines for phase shift
  - Hi insertion loss
  - Area



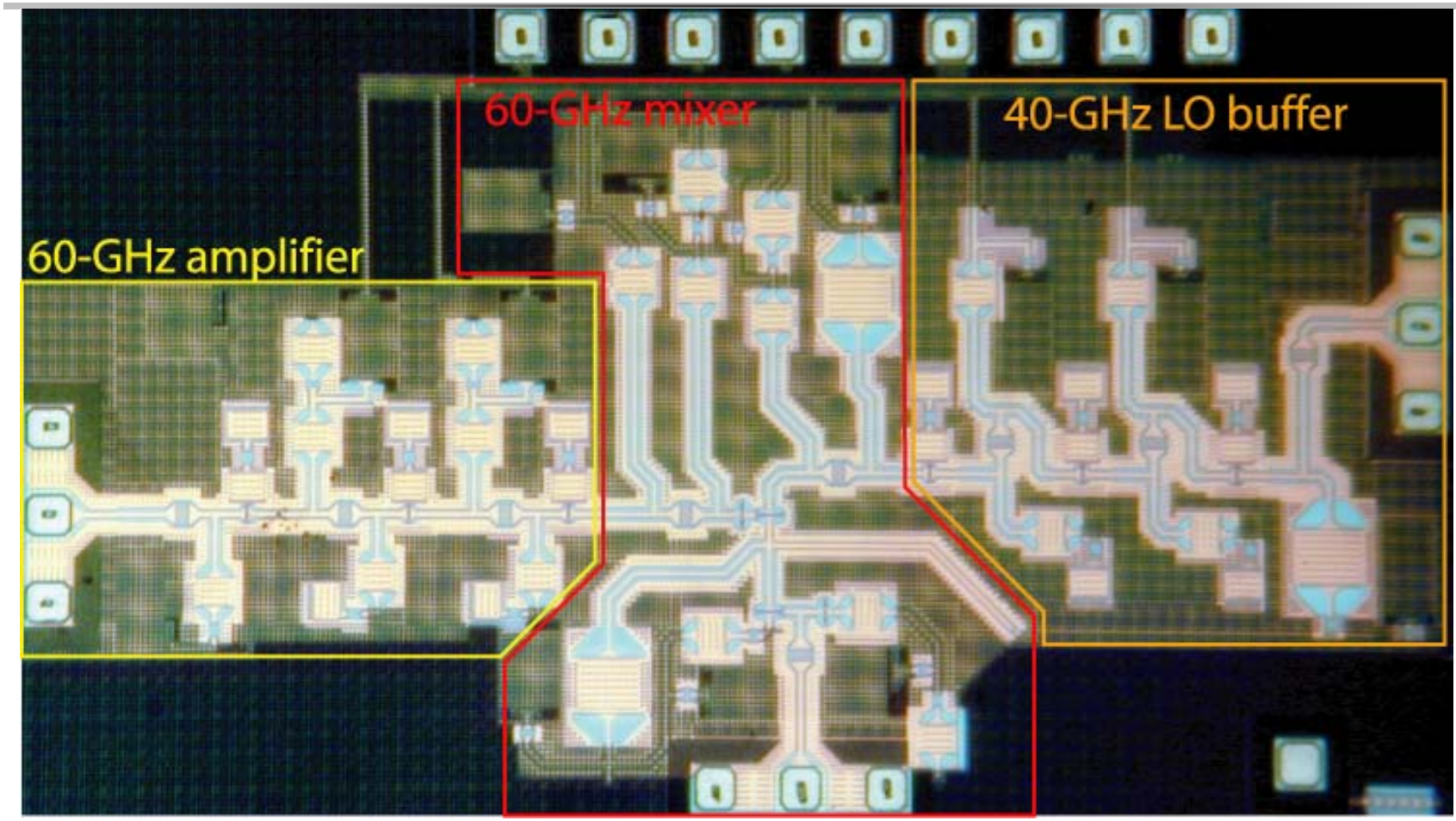
- Reducing t-line length

- Transistors provide some free caps!



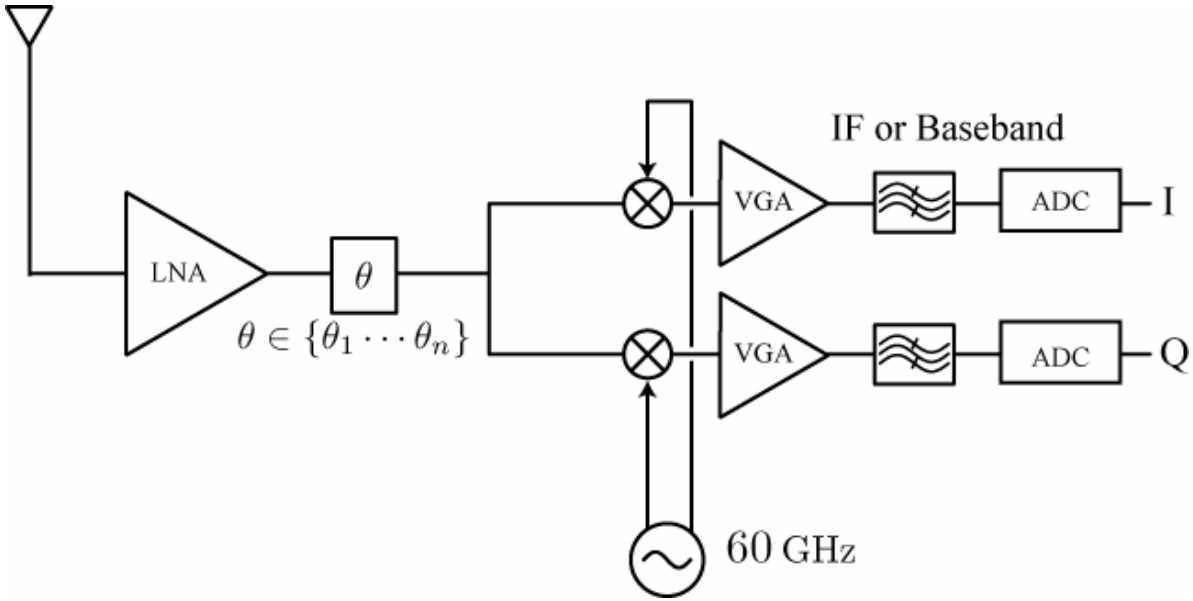


Integration: 60-GHz front-end



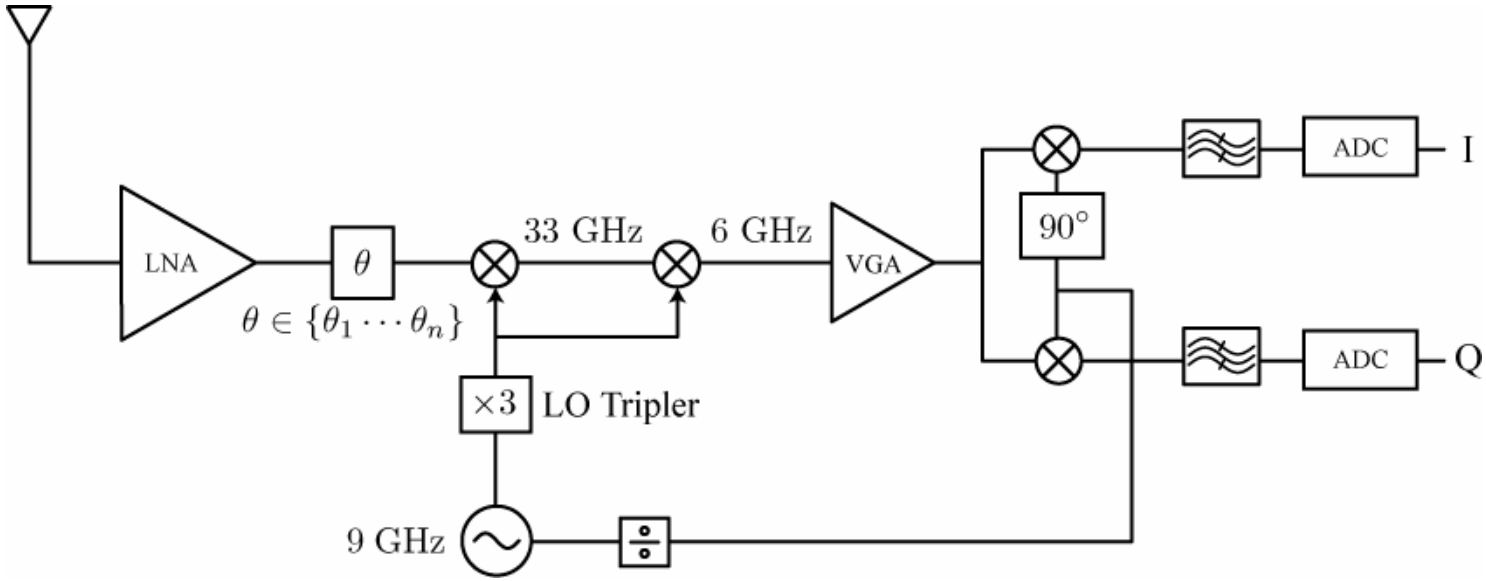
- 60-GHz front-end designed for a double-conversion architecture
- 7-dB measured conversion gain

Direct Conversion Radio



- Direct conversion or "low-IF" is simple but requires a 60 GHz VCO.
- While oscillation at 60 GHz is not too difficult, generating a synthesized LO signal requires a 60 GHz frequency divider (power hungry) and a 60 GHz LO buffer. Varactors also have a relatively low Q at 60 GHz.
- One way to relax the power requirements on the divider is to generate a 20 GHz LO with a frequency tripler to drive the mixer.
- Most of the gain must come from a broadband IF (~1 GHz of bandwidth) since the LNA/mixer may have a moderate gain of 10-20 dB.

Multi-Stage Conversion



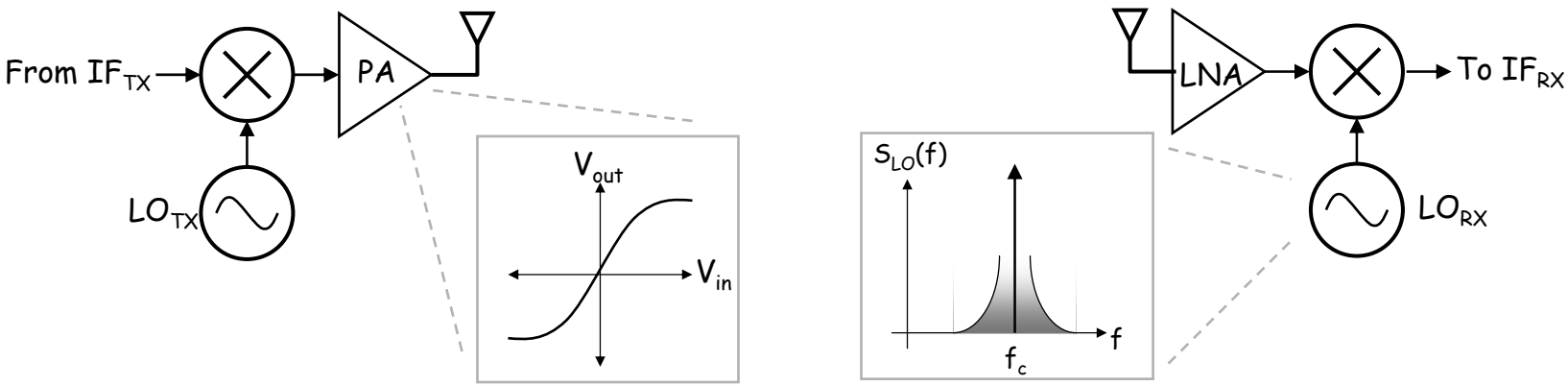
- 9 GHz VCO is locked to reference. Power consumption of frequency dividers is greatly reduced.
- A frequency tripler generates a 27 GHz LO.
- Gain comes from RF at 60 GHz, at IF of 33 GHz, and through a passband VGA at 6 GHz (easier than a broadband DC solution).

Link Budget for 10m, 1000Mbps

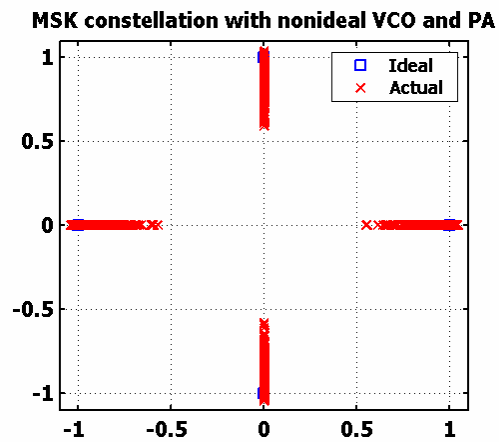
Component	Contribution	Running Total	Comment
Tx power	+2dBm signal power per PA	+11.5 dBm aggregate signal power	9 distinct PA's at +2dBm each
Tx Antenna Gain	+2.4dB (dipole) +9.5dB (array)	+23.4dBm effective radiated power	9-fold antenna array
Path loss	-87dB	-63.6dBm signal power	Path loss @ 10m in 60GHz band
Antenna nonidealities /Shadowing loss	-10dB	-73.6dBm signal power	
Rx Antenna Gain	+2.4dB (dipole) +9.5dB (array)	-61.7dBm received signal power	9-fold antenna array
Background noise	-174 dBm/Hz noise power	-174 dBm/Hz noise power	kT at room temp
Noise bandwidth	+90dB	-84 dBm/Hz noise power	1GHz noise BW
Noise figure	+10dB	-74 dBm/Hz noise power	Projected NF
SNR at input		12.3dB	Signal power /noise power
SNR required		7dB	Coherent MSK, BER=10^{-3}
System Margin		5.3dB	

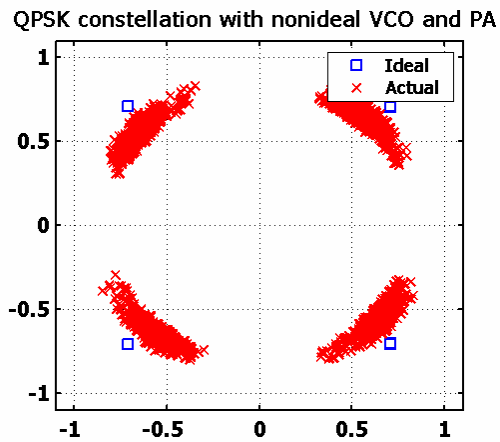
System Design Considerations

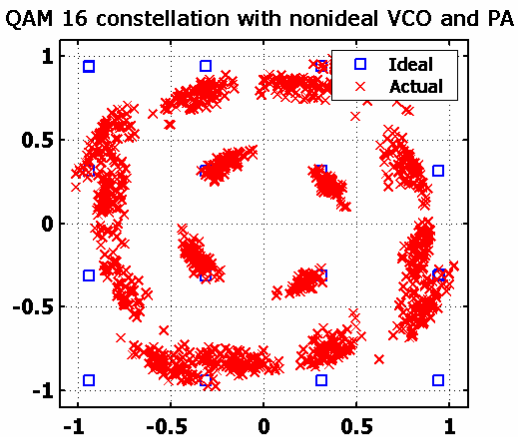
- 60 GHz CMOS PA will have limited P_{1dB} point
  - Tx power constraint while targeting 1Gbps
  - Must use low PAR signal for efficient PA utilization
- 60 GHz CMOS VCOs have poor phase noise
  - -85dBc/Hz @ 1MHz offset typical (ISSCC 2004)
  - Modulation must be insensitive to phase noise

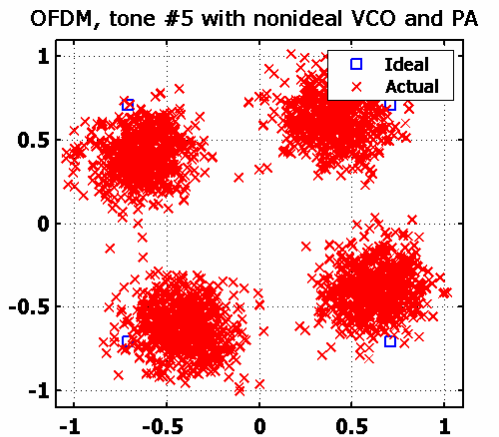


Example: PA and VCO nonidealities









Constellation observed at TX output

- No thermal noise

Simulation conditions:

- $P_{TX}=P_{1dB}$
- SSPA AM/AM, AM/PM model [1]
- Lorentzian PN spectrum
  - f_{3dB}=1MHz
  - -85dBc/Hz @ 1MHz

Simulation Results:

- MSK: SNR = 24dB
- SC-QPSK: SNR = 16dB
- OFDM: SNR = 9.5dB

[1] C. Rapp, "Effects of HPA-Nonlinearity…", Proc. 2nd European Conf. on Satellite Comm, 10/91.

60 GHz Channel Spatial Properties

- Specular, moderately reflective channel
  - Building materials poor reflectors at 60GHz
- "Typical" 60GHz indoor channel properties: [1]
  - Omni-antenna w/ LOS: $T_{RMS} \sim 25ns$, $K_{Rician} \sim 0\text{-}5dB$
  - 30° horn w/ LOS: $T_{RMS} \sim 5ns$, $K_{Rician} \sim 10\text{-}15dB$
  - $K_{Rician} = P_{LOS}/\Sigma P_{Multipath}$

Antenna directivity reduces **multipath fading** problem to **constrained ISI** problem

[1] M. Williamson, et al, "Investigating the effects of antenna directivity on wireless indoor communication at 60 GHz," PIMRC 1997

Modulation Scheme Comparison

Modulation	OFDM-QPSK	High-order modulation (16-QAM)	Single-carrier QPSK	Constant Envelope (MSK)
SNR_{req} ($BER=10^{-3}$)	7dB	12dB	7dB	7dB
PAR_{TX}	~10dB	~5.5dB	~3dB	0dB
PA linearity req't	High	High	Moderate	Low
Sensitivity to Phase Noise	High (ICI)	High (Symbol Jitter)	Moderate	Low
Complexity of Multipath Mitigation Techniques	Moderate (FFT)	High (Equalizer)	High (Equalizer)	High (Equalizer)

Beamforming to combat multipath.

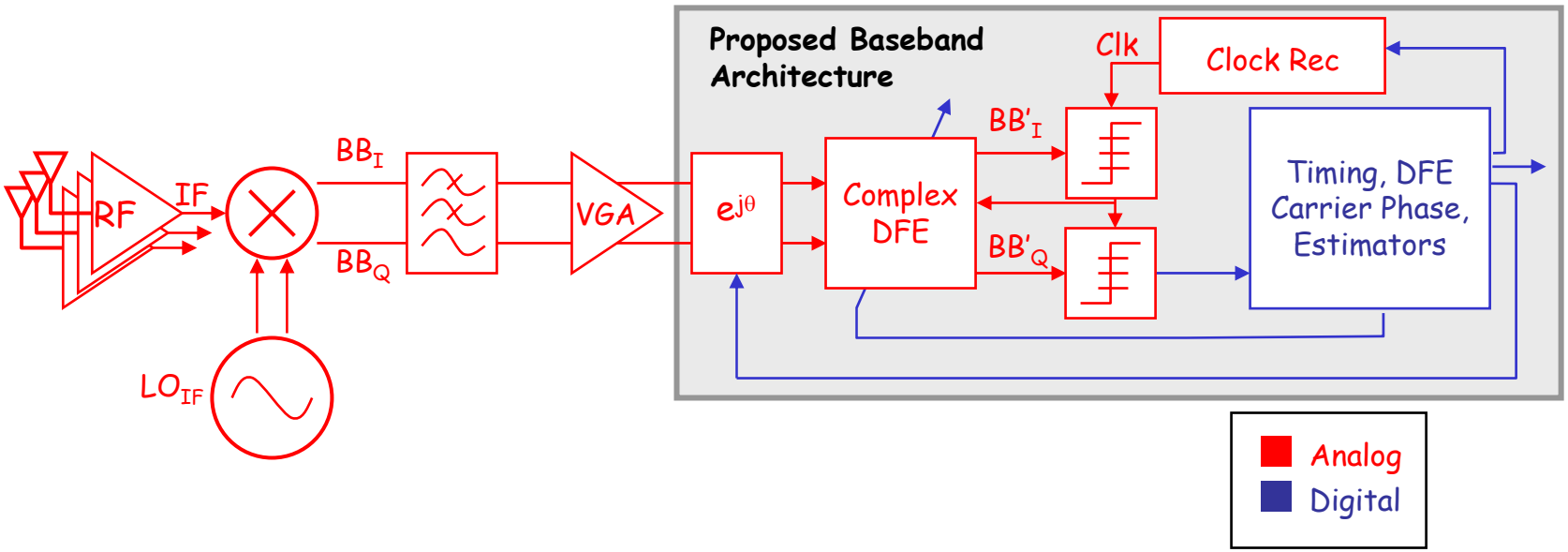
Simple modulation (MSK) for feasible CMOS RF circuits.

Baseband Architecture Considerations

- Targeting 1 Gbps with "simple" modulation scheme
  - Must use low-order constellation, high baud rate
- Fast baud rate (1Gsym/s) ➔ high-speed ADCs, VGAs
- Desire baseband architectures that:
  - Minimize ADC resolution
  - Minimize required ADC oversampling ratio
  - Incurs minimal SNR loss from above simplifications
  - Adaptable, robust to channel variations

Re-think "traditional" partitioning of analog and digital subsystems!

"Hybrid-Analog" Architecture



- Synchronization in "hybrid-analog" architecture
  - ESTIMATE parameter error in digital domain
  - CORRECT for parameter error in analog domain
- Greatly simplifies requirements on power-hungry interface ckts (i.e. ADC, VGA)
  - Additional analog hardware is relatively simple

Conclusions

- 60 GHz radio architecture involves a complexity and power tradeoff.
- At 130 nm, mainstream digital CMOS is able to exploit the unlicensed 60 GHz band. 90 nm should be even better.
- Accurate device modeling is possible by extending low-frequency methodologies.
- A transmission line-based circuit strategy provides predictable low-loss impedance matching and filtering.
- The antenna array plays a key role in maximizing link distance and minimizing baseband complexity.
- Simple modulation schemes relax PA and VCO requirements.
- A hybrid-analog baseband architecture simplifies ADC specification.

Acknowledgments

- DARPA TEAM Project
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