Teaching CMOS to Surf mm-Waves

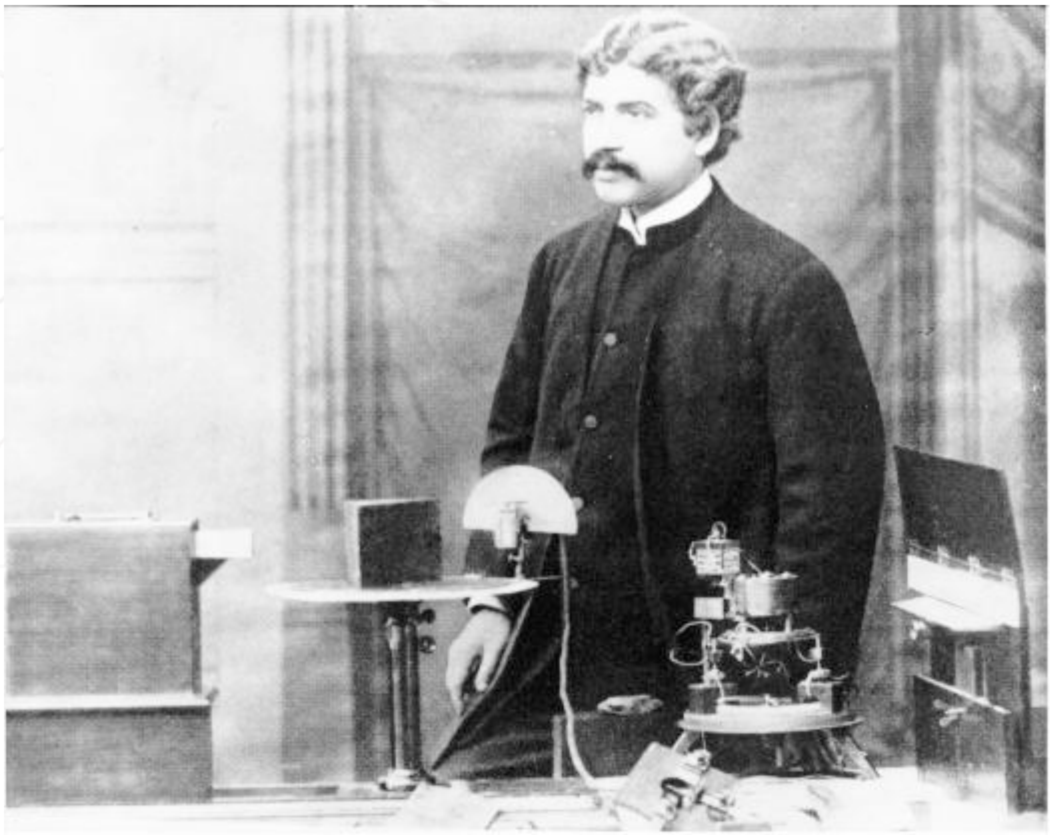
Thursday July 17, 2007

Berkeley Wireless Research Center

Ali M. Niknejad

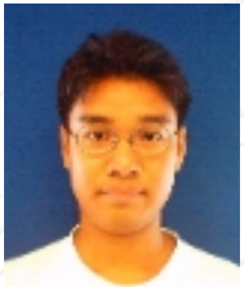
Berkeley Wireless Research Center

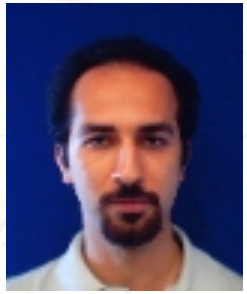
The Big Kahuna: Jagadis Chandra Bose

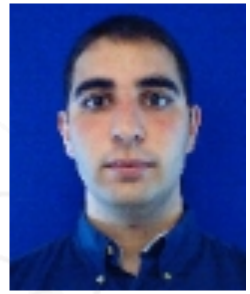


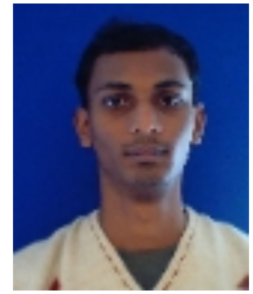
- “Just one hundred years ago, J.C. Bose described to the Royal Institution in London his research carried out in Calcutta at millimeter wavelengths. He used waveguides, horn antennas, dielectric lenses, various polarizers and even semiconductors at frequencies as high as 60 GHz…” (http://www.tuc.nrao.edu/~demerson/bose/bose.html)

The Young Surfers

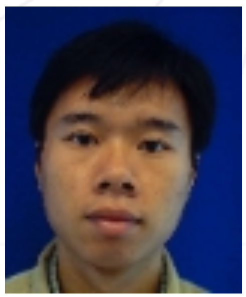

Nuntachai P.

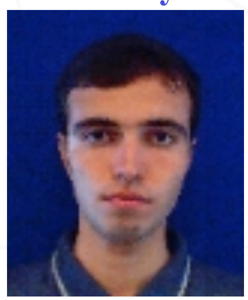

Babak Heydari

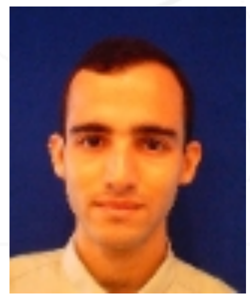

Mounir Bohsali

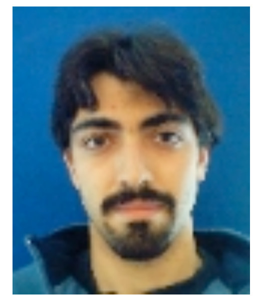

Mohan Dunga


Wei-Hung Chen


Zhiming Deng


Ehsan Adabi


Bagher Afshar


Amin Arbabian


Cristian Marcu


Debo Chowdhury


Omar Bakr


JiaShu Chen

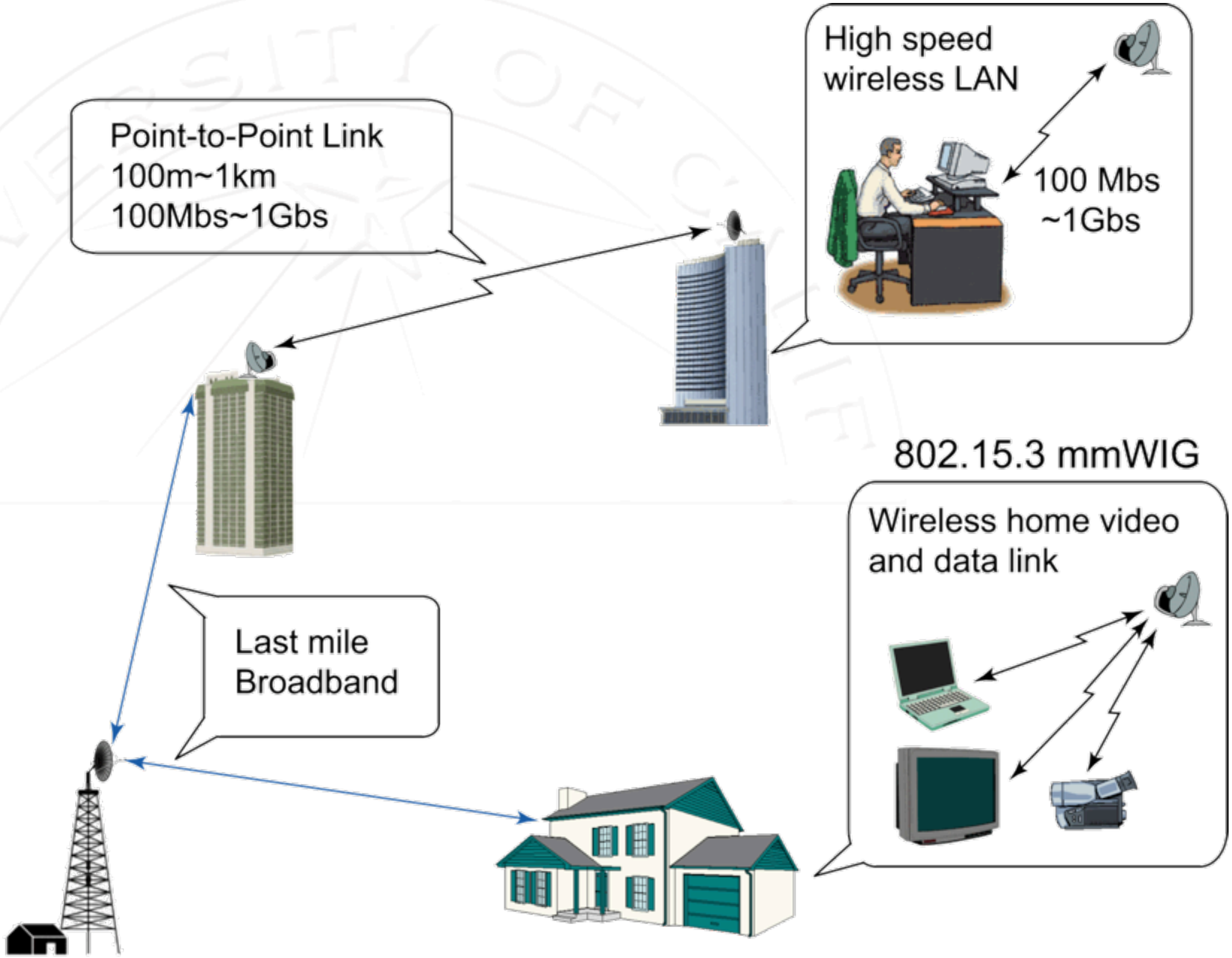

Sahar Tabesh


Jung Dong Park


Reza Zamani

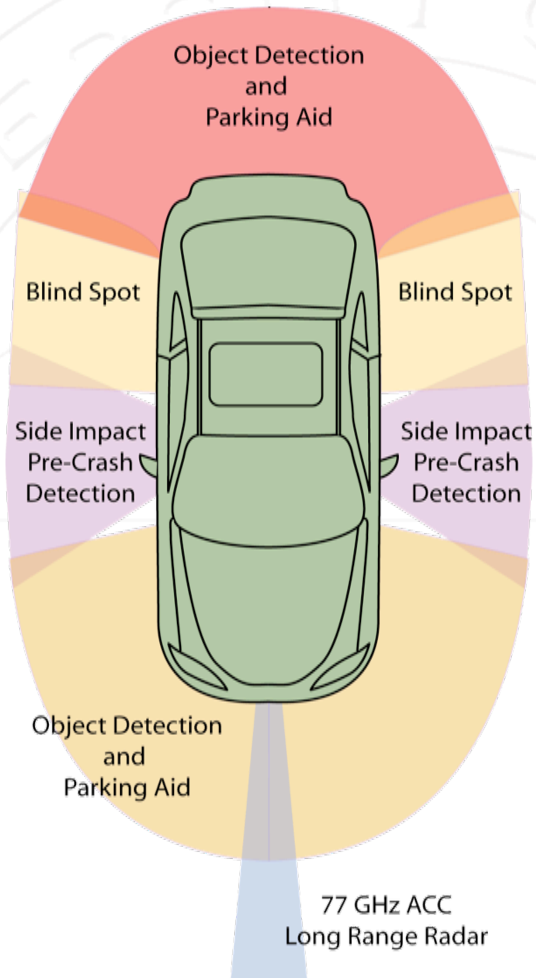
APPLICATION DRIVERS

The "Last Inch"



Universal Mobility

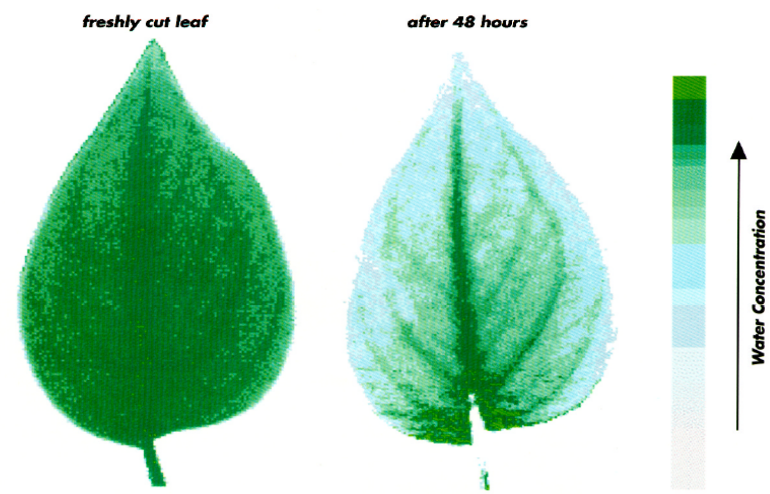
Automotive Radar



- Short range radar for parking assist, object detection
- Long range radars for automatic cruise control, low visibility (fog) object detection, impact warning
- Long range vision: automatic driver

mm-Wave Imaging … THZ?

- Use of microwave scattering from objects to predict image
- A low-cost, noninvasive solution (meV versus keV)
- Active and Passive Microwave Imaging
- Ultrawideband imaging
- THz detection … ?

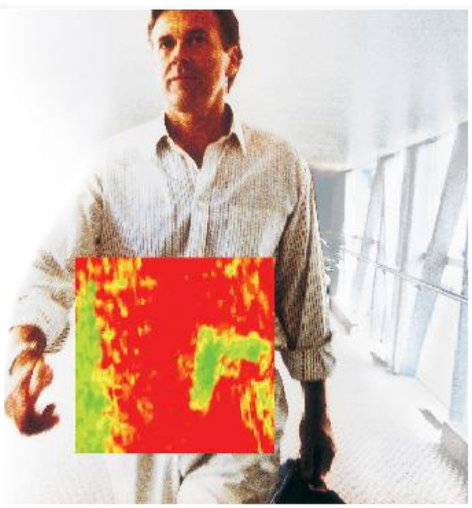


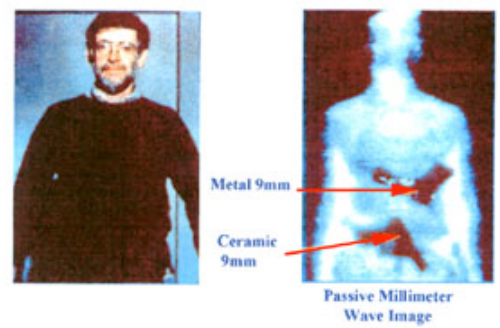
TeraView Ltd

Concealed Weapons Detection

Passive “Camera”
contains many receivers

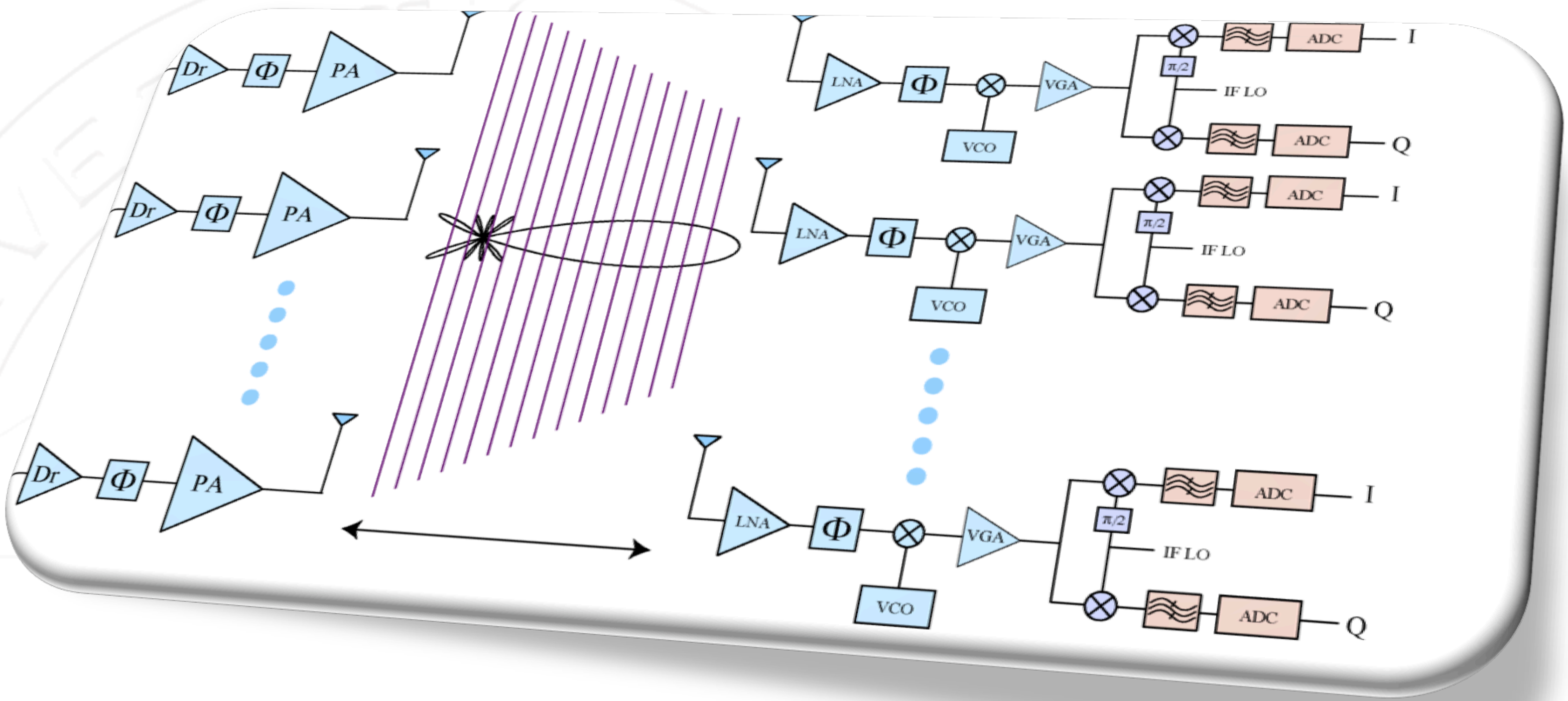
QinetiQ Passive Array





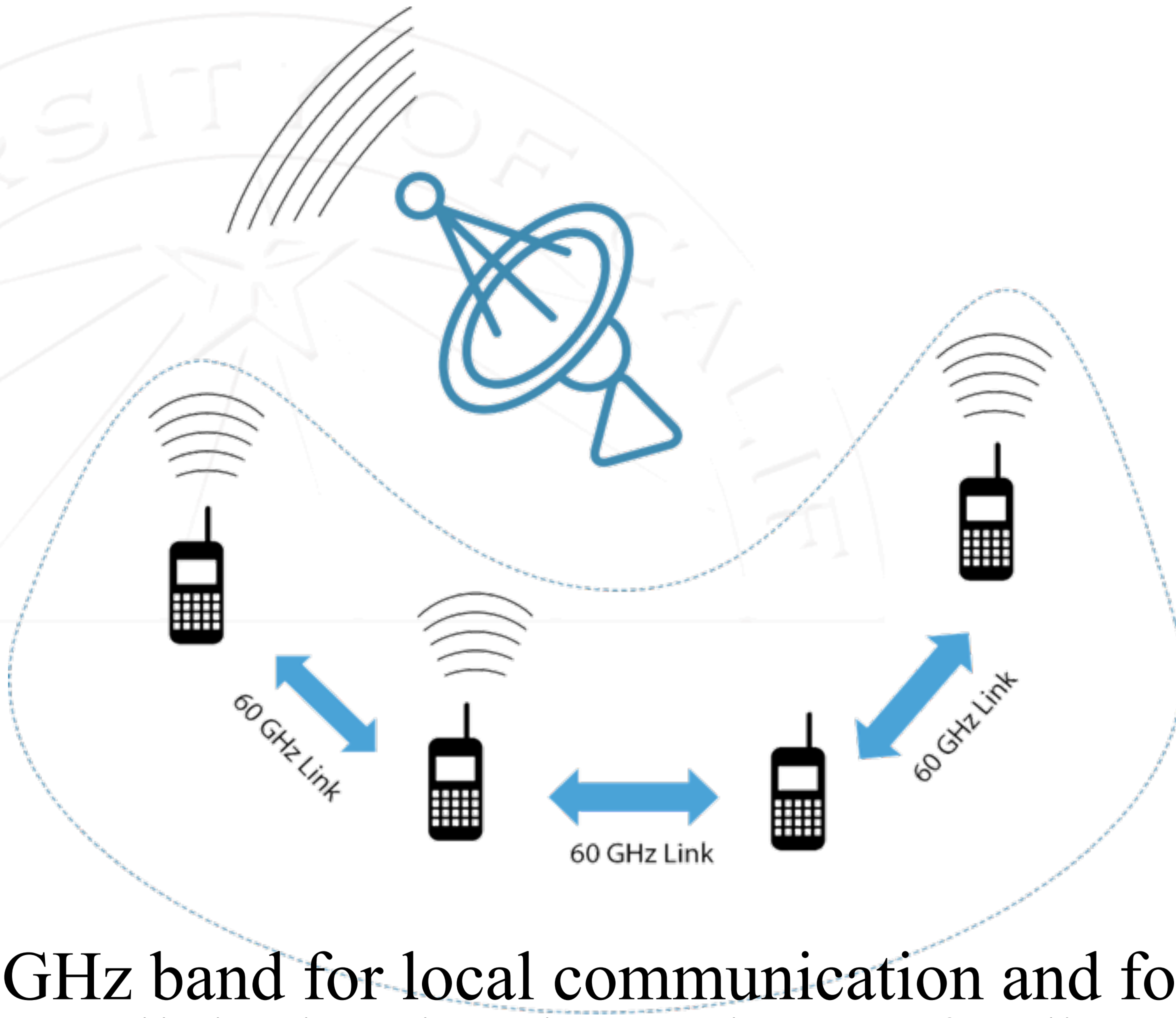
TeraView Ltd

Low Power Phased Array



- A fully integrated low-cost Gb/s data communication using 60 GHz band.
- 10 Gb/s at 100mW per channel should be possible! (10pJ/bit) at 10's of meters

Distributed MIMO

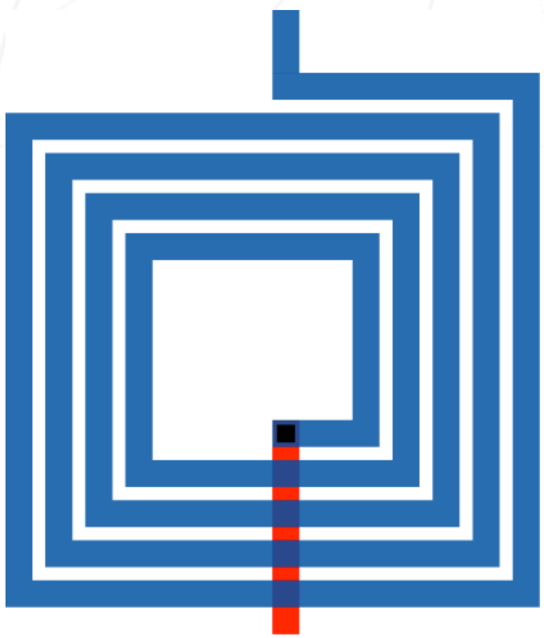


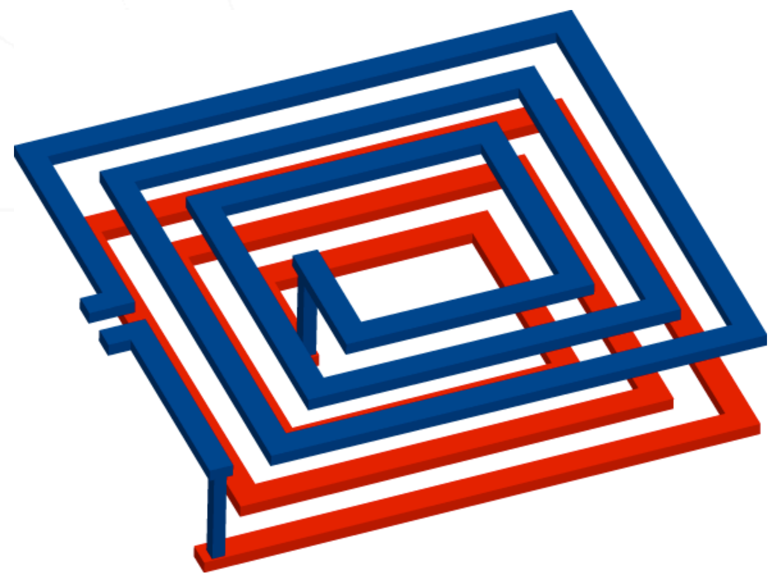
- Use 60 GHz band for local communication and form a MIMO at cellular bands using a cluster of radios.

THE FATE OF PASSIVE ELEMENTS

Passive Devices Don't Scale

- For fixed frequency, area of inductors roughly constant
- Multiple metal layers allow more compact inductors but high Q inductor still single layer (top thick layer)

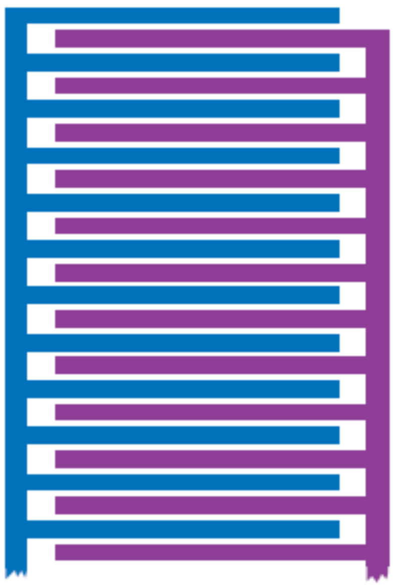


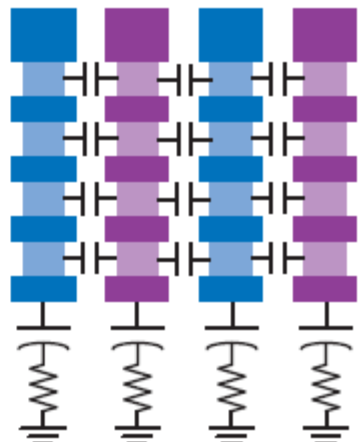


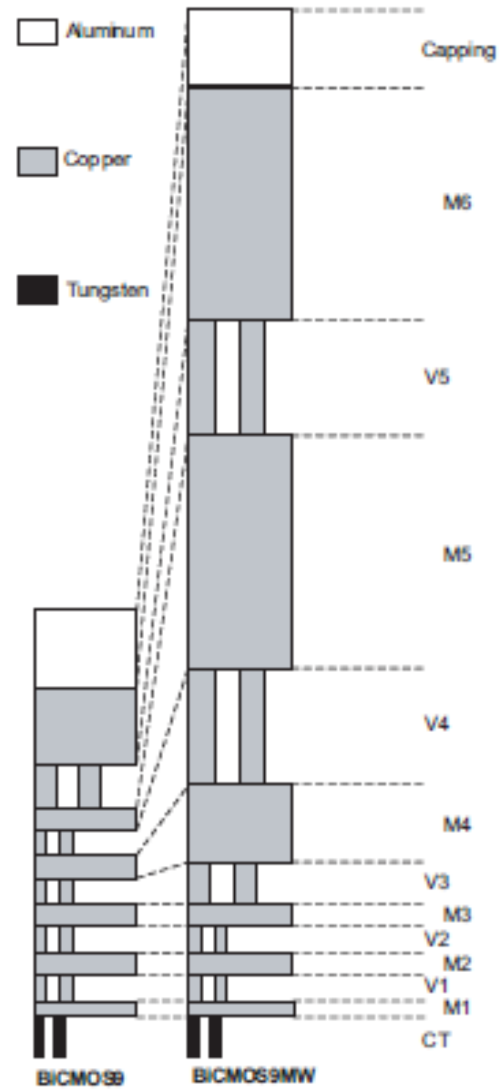
Microprocessor or Inductor?

- It is widely appreciated that the area of an inductor in today's CMOS is equivalent to a powerful CPU
- Low frequencies: **Get rid of them**
  - Use broadband circuit techniques
  - Analog design = RF design … use feedback
  - Use linearity enhancement schemes for out of band blockers
- High frequencies:
  - Area is still reasonable
  - T-line versus lumped?
- What to do with all that metal?
  - Slow wave structures

Scaling Helps and Hurts

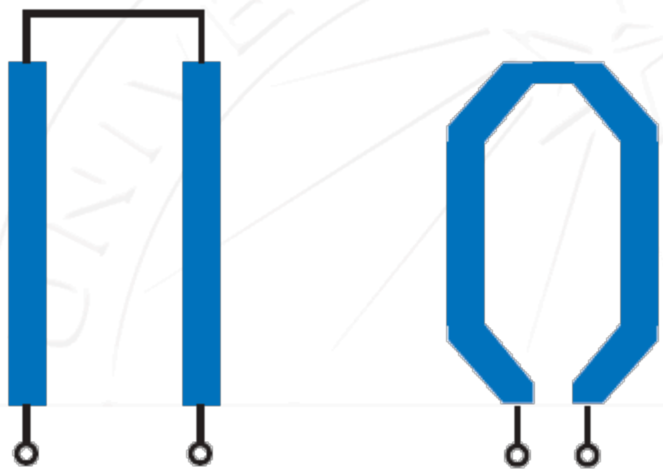


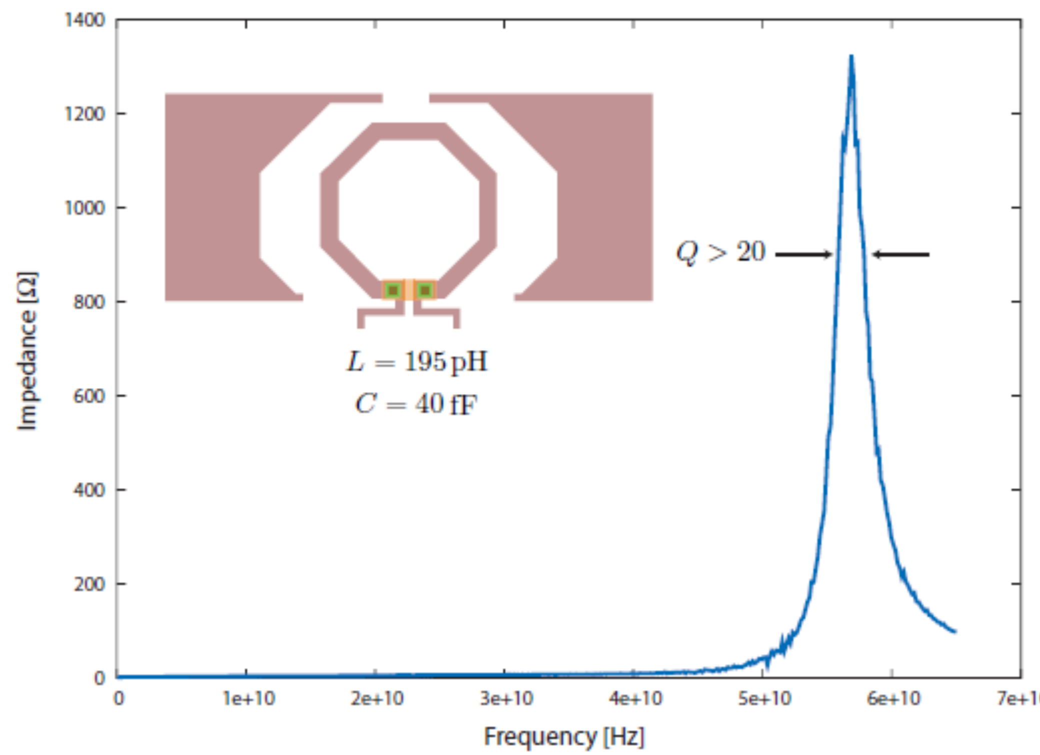




- Can build very high density caps
- Cu and thick metal stacks were very exciting (130nm, 90nm)
- Metals are getting thinner (low K)
- Inductors and T-lines are getting worse

Inductor or T-Line?

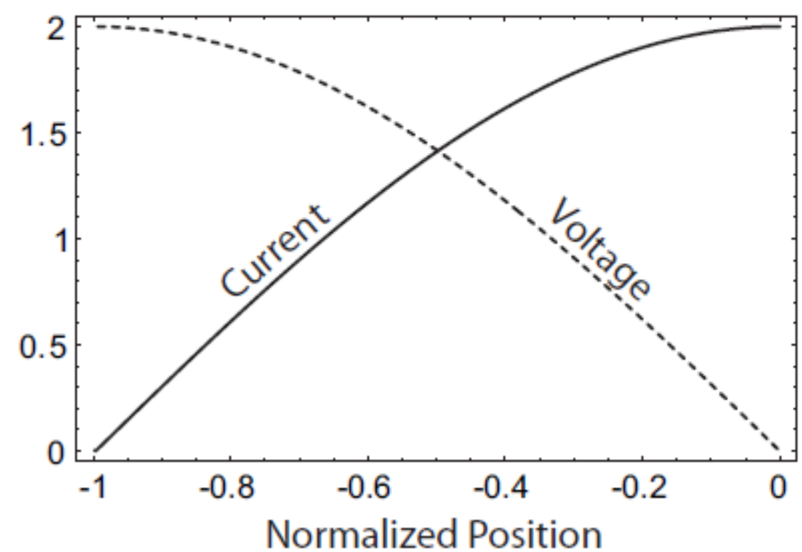


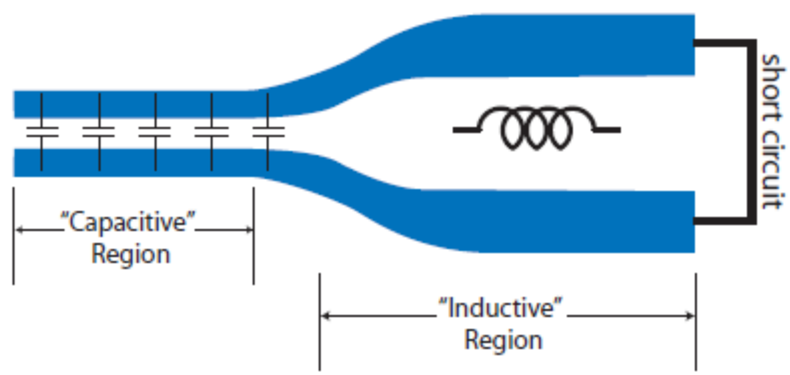


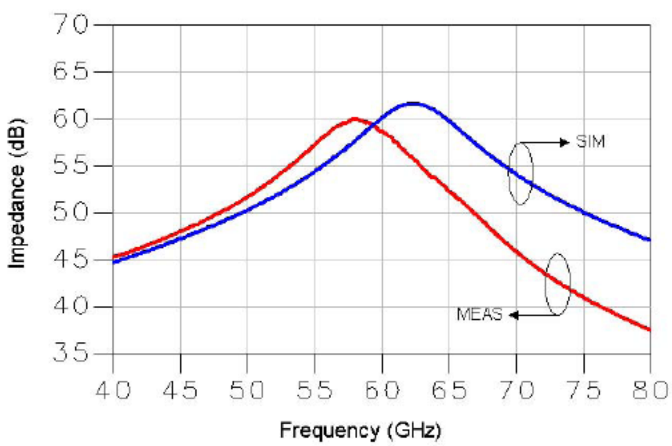
- LC resonators have good Q factor … varactors are problematic above 40GHz
- High Z0 quarter wave resonators → loop inductors

Optimal Taper Profile

- Andress and Ham [JSSC 2005] showed that a tapered resonator has improved Q
- Assumed a constant Z0 line. What if you remove this constraint?
- Result looks like an LC tank!



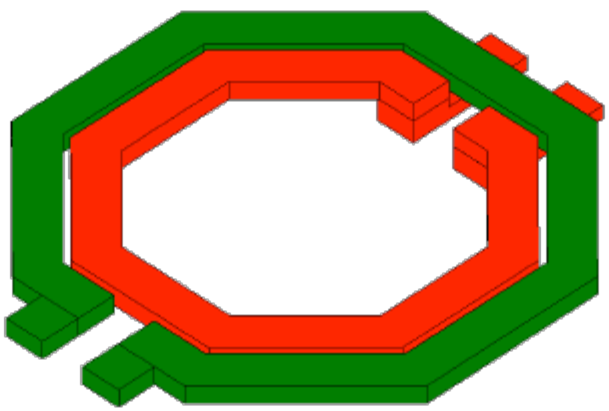


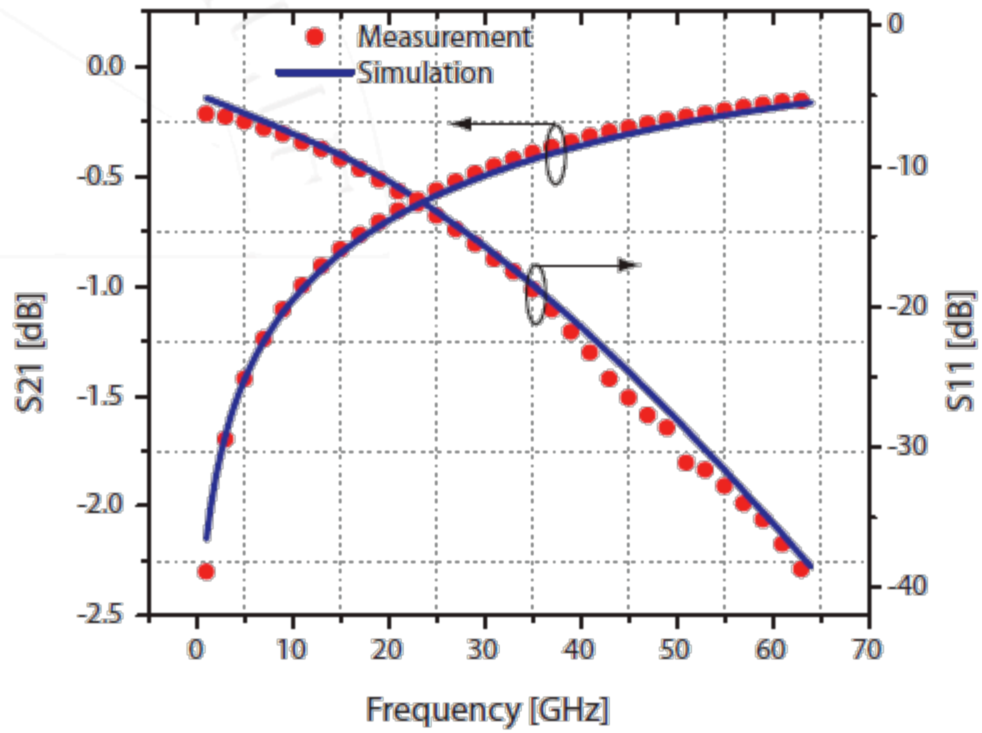


Resonator Type	f_0 (GHz)	Q	ΔQ
Uniform (ref.)	57.9	8.8	–
Tapered	54.4	15	70.4%
Cap-Loaded Half-Taper	55.4	15.1	71.6%

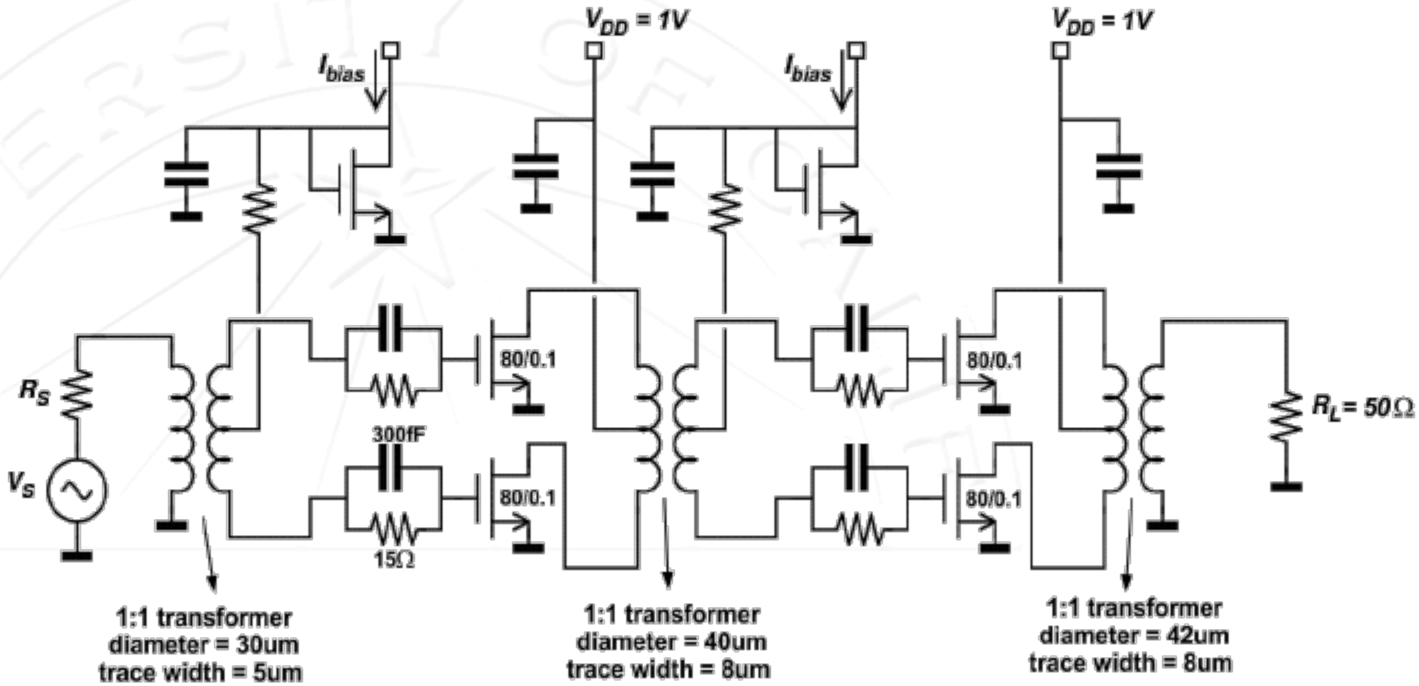
Transformers Scale to mm-Waves

- Isolation, impedance matching, biasing …
- Good insertion loss
- Compact layout compared to T-lines



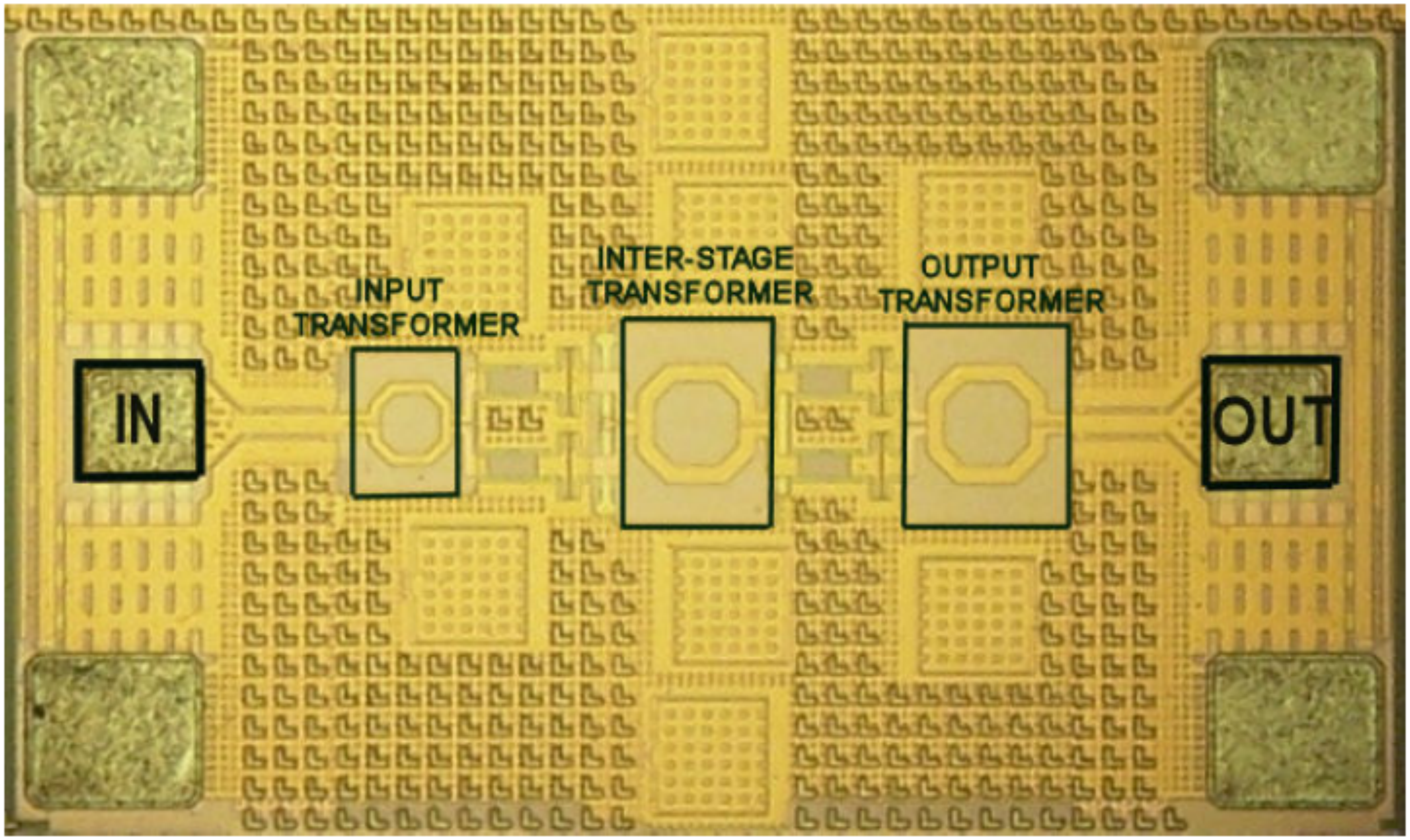


Broadband mm-Wave PA



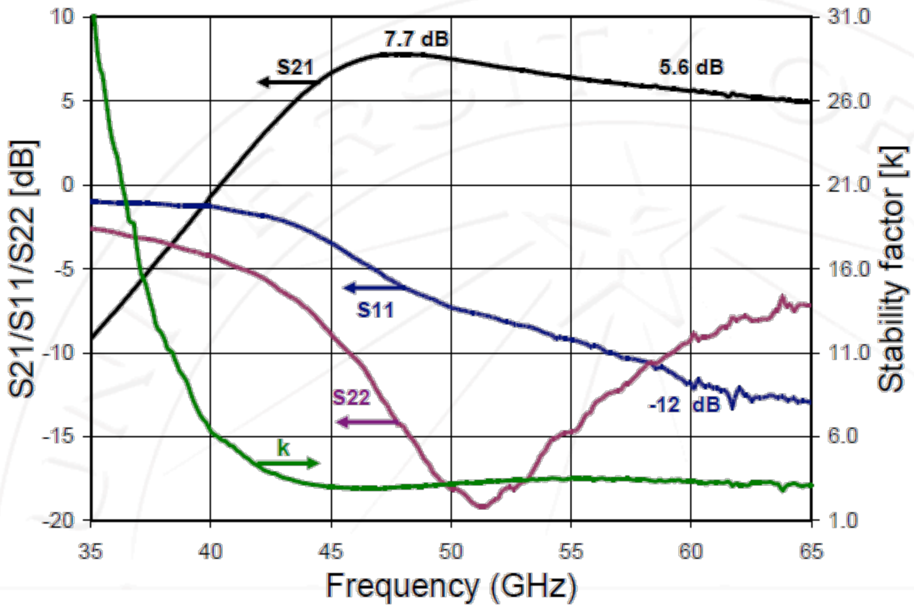
- Two stage transformer coupled PA
- Pseudo-differential design
- Transformer used for tuning, AC coupling, and biasing

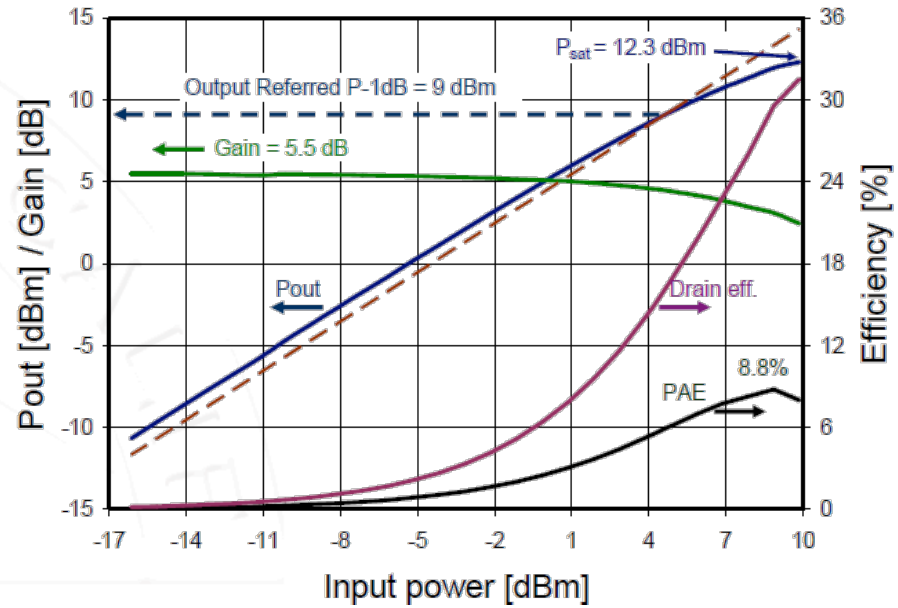
PA Die Photo



- Area: 0.25 mm^2
- Small area due to transformers

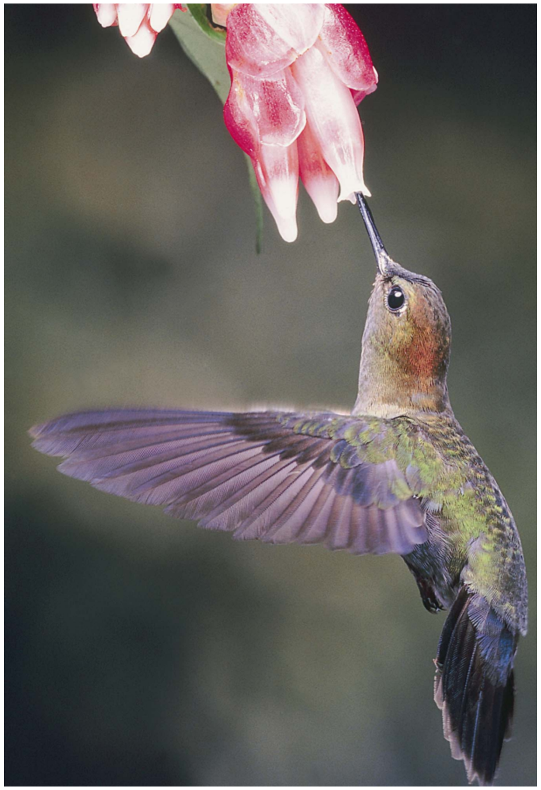
Measured Performance





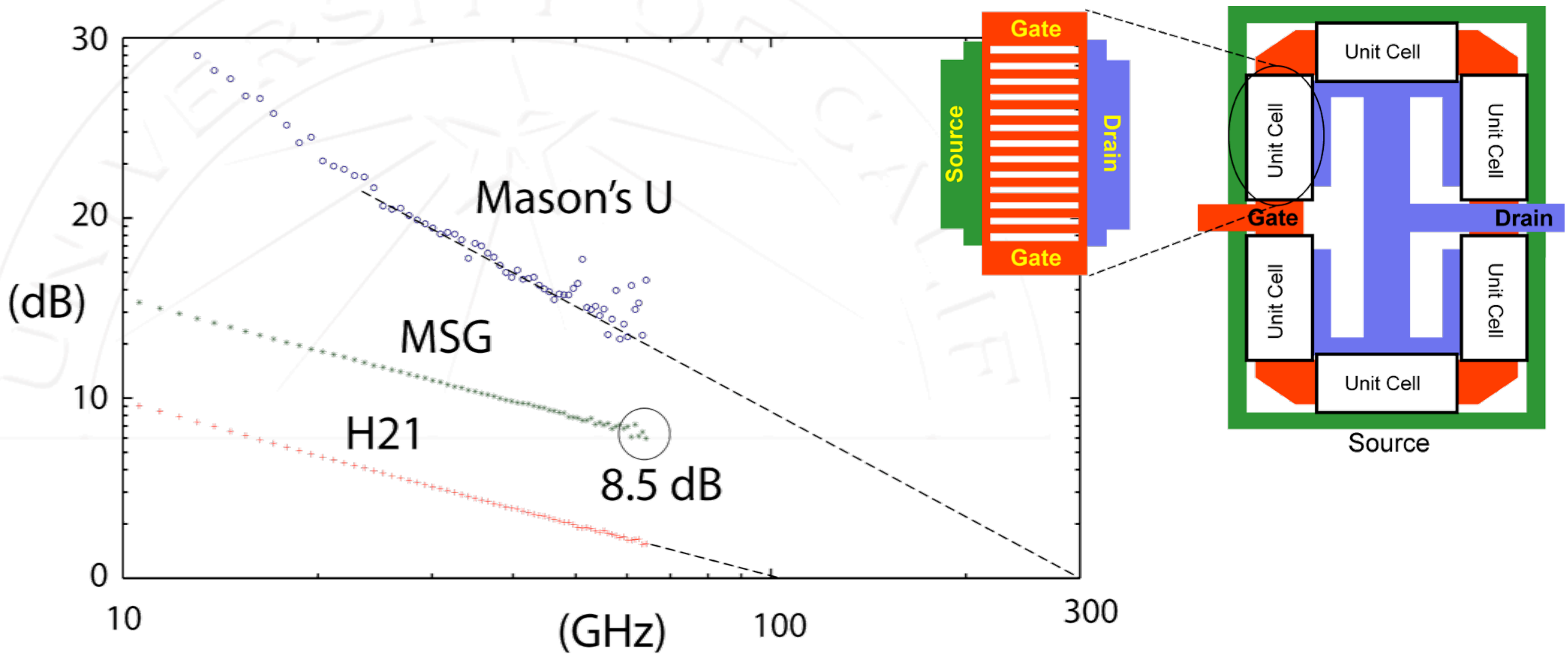
- Broadband gain (45 - 65 GHz)
- Good matching (55 - 65 GHz)
- Stable (K > 1)
- P_{-1dB} > 9dBm
- P_{sat} = 12.3 dBm

Debopriyo Chowdhury and Patrick Reynaert



TEENY TINY BUT VERY FAST

“Roundtable” 90nm Layout

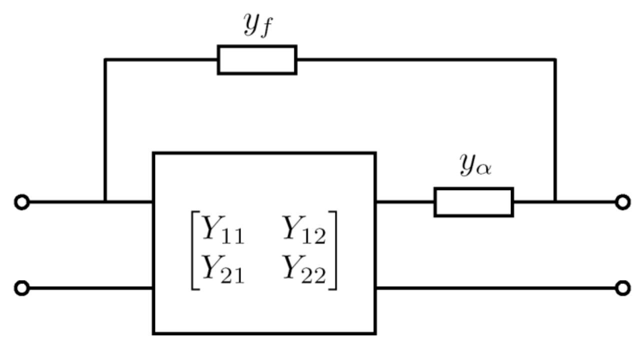


- MSG 60GHz = 8.5 dB, NFmin ~ 3-4 dB
- f_{max}= 300 GHz (*extrapolated*), f_T= 100 GHz
- Highest reported f_{max}/f_T=3 ratio for CMOS!

Babak Heydari, Mounir Bohsali, Ehsan Adabi

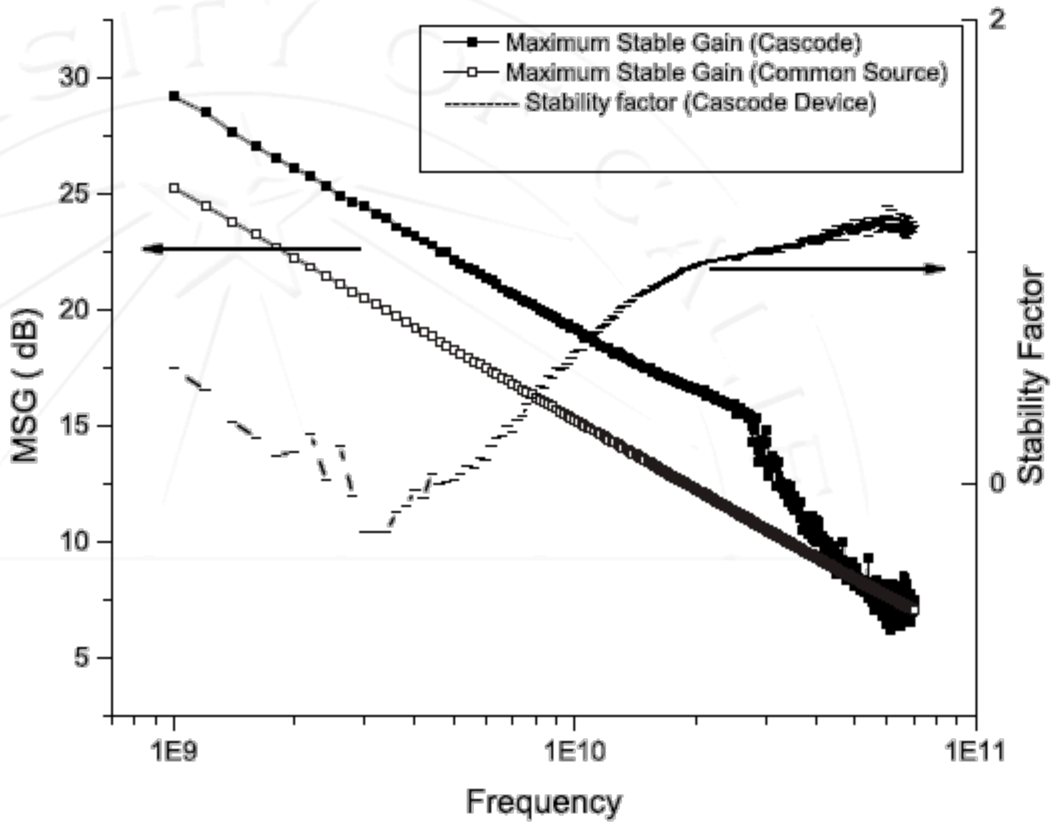
Mason's Unilateral Gain

$$U = \frac{|k_{21} - k_{12}|^2}{4(\Re(k_{11})\Re(k_{22}) - \Re(k_{12})\Re(k_{21}))}$$



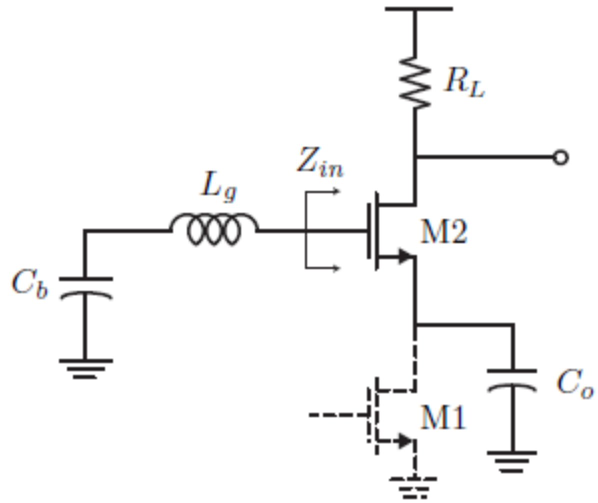
- Apply lossless feedback to unilateralize the 2-port
- Properties of U:
  - If U > 1, the two-port is active. Otherwise, if U 1, the two-port is passive.
  - U is the maximum unilateral power gain of a device under a lossless reciprocal embedding.
  - U is the maximum gain of a three-terminal device regardless of the common terminal.
- U is very sensitive to any loss in the 2-port. Good way to test accuracy of model *and* measurements.

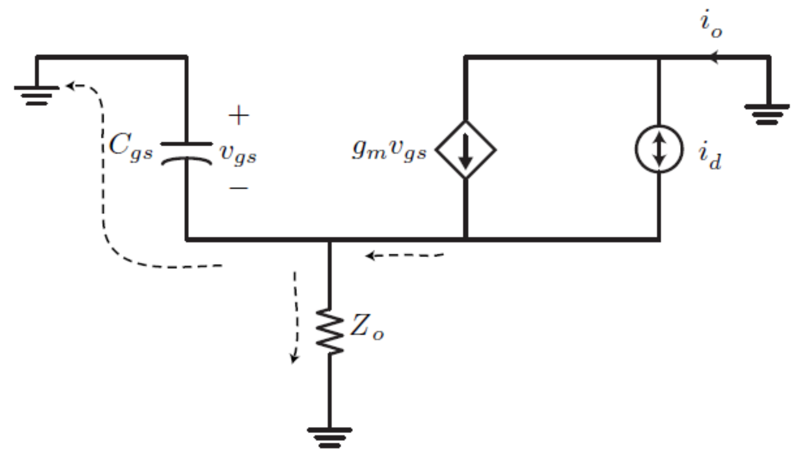
Cascode HF Bilateralization



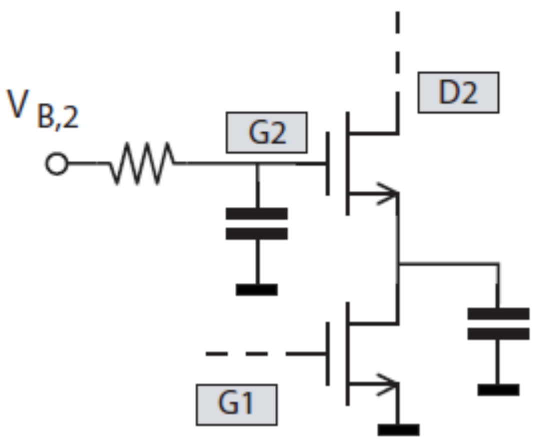
- MSG of cascode close to U of common-source device below 30 GHz
- At 60 GHz MSG of cascode same as common-source … device is no longer unilateral

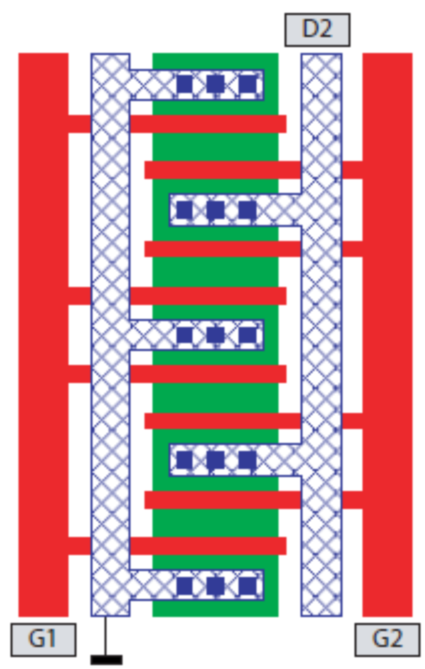
mm-Wave Cascode Device



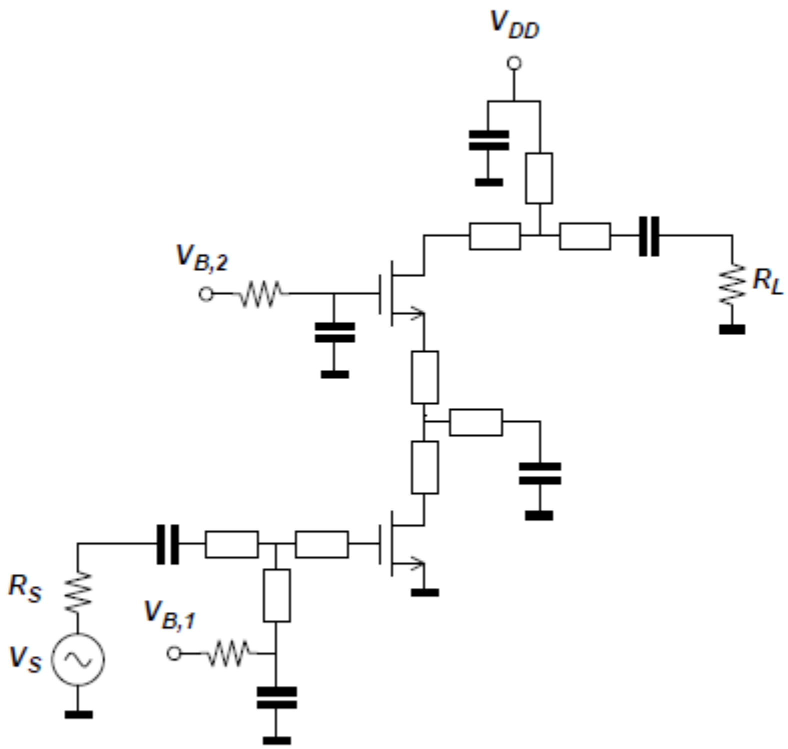


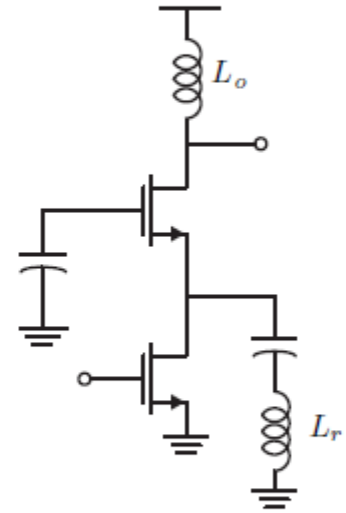
$$\overline{i_o^2} = \overline{i_d^2}\left|\frac{1/g_m}{1/g_m + Z_o}\right|^2 = \overline{i_d^2}\left|\frac{1}{1+g_m Z_o}\right|^2$$

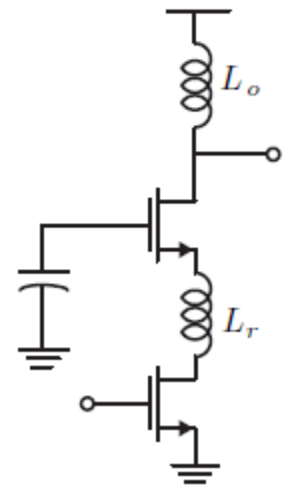




Cascode Gain Enhancement







- Tune out parasitics or design as a two-stage amplifier.
- Cannot use shared junction layout.

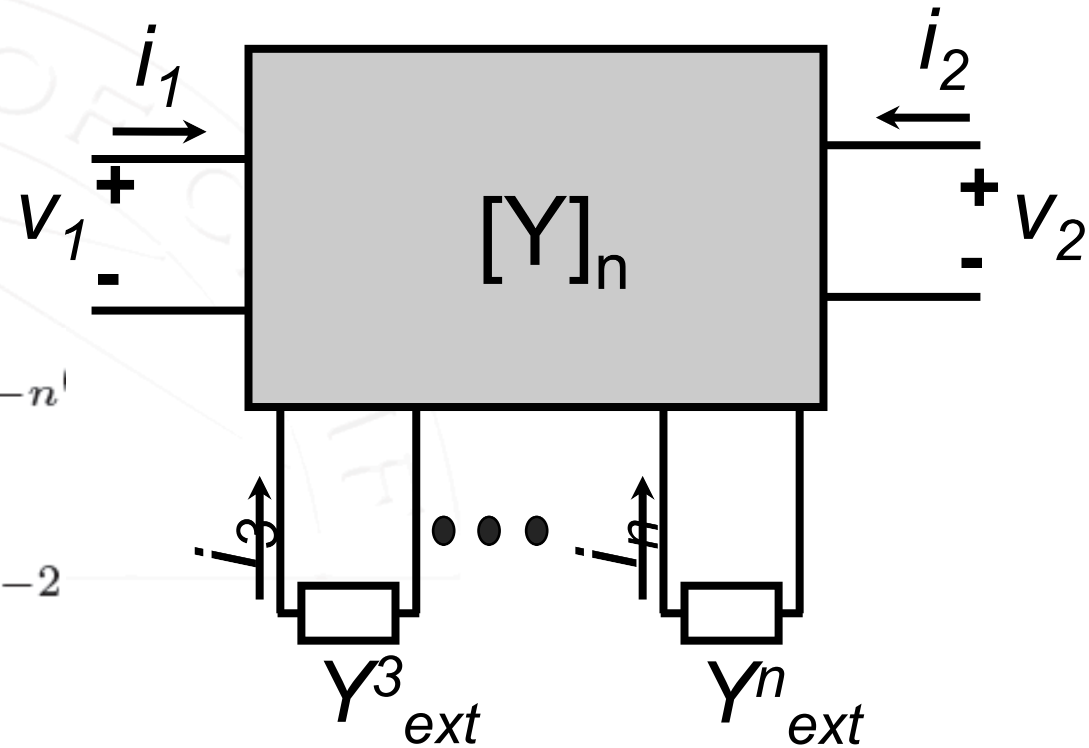
N-port Unilateralization

$$I_n = Y^{1-n}_{1-n} V_n$$

$$I_{1-2} = Y^{1-2}_{1-2} V_{1-2} + Y^{3-n}_{1-2} V_{3-n}$$

$$I_{3-n} = Y^{3-n}_{3-n} V_{3-n} + Y^{1-2}_{3-n} V_{1-2}$$

$$\vdots$$



$$\overline{Y^{1-2}_{1-2}} = Y^{1-2}_{1-2} - Y^{3-n}_{1-2}(Y_{ext} + Y^{3-n}_{3-n})^{-1} Y^{1-2}_{3-n}$$

Solve for $\overline{y}_{12}=0$ to get Y_{ext}

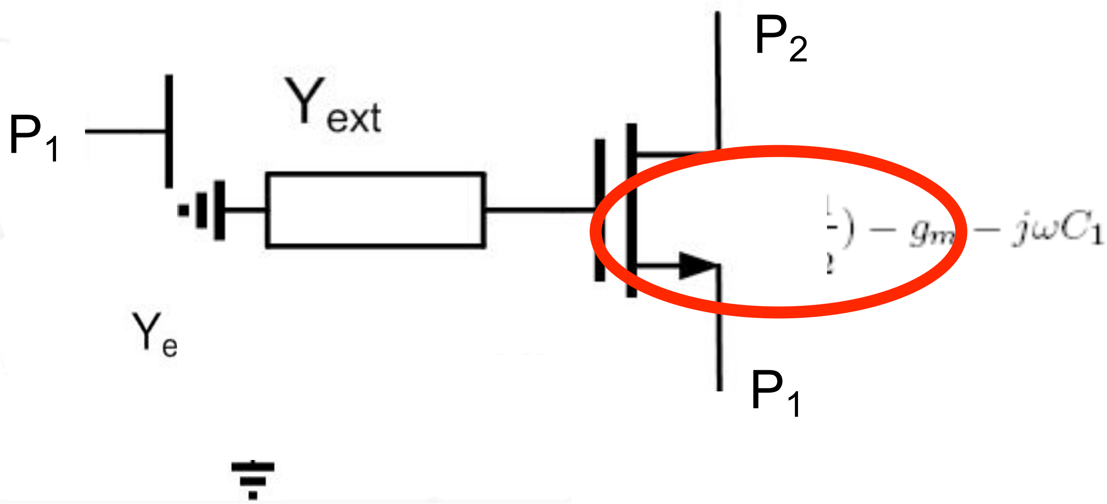
- ✓ **Passivity**
- ✓ **Stability**

Single Transistor Scheme

$$Y_{ext} = \frac{Y_{13}Y_{32}}{Y_{12}} - Y_{33}$$

$$\Re(Y_{11}) \geq \Re(\frac{Y_{31}Y_{12}}{Y_{32}})$$

$$\Re(Y_{22}) \geq \Re(\frac{Y_{23}Y_{12}}{Y_{13}})$$



$$\Re(Y_{ext}) = \frac{\omega^2 C_1 C_2}{g_{ds}}$$

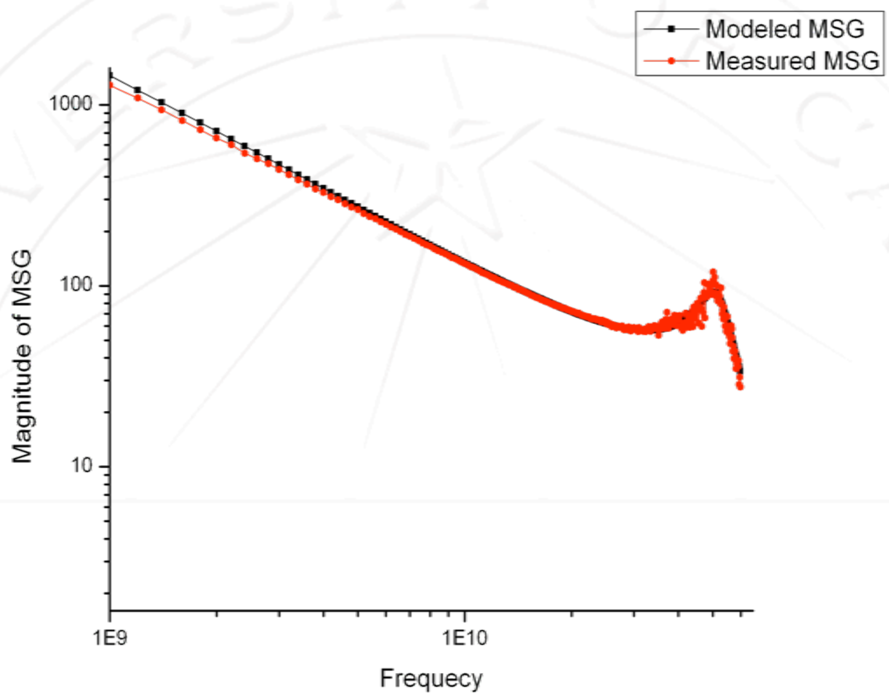
$$\Im(Y_{ext}) = -\omega(C_1 + C_2) - \frac{g_m C_2}{g_{ds}}$$

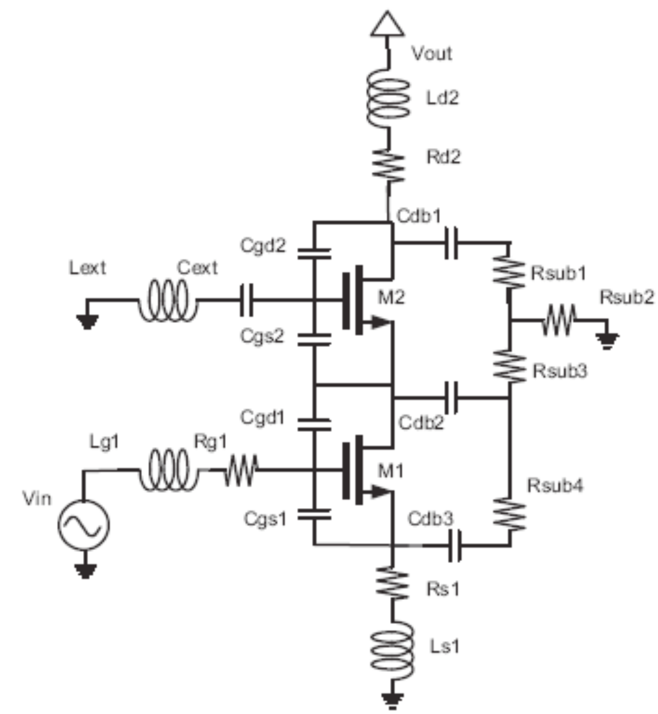
$$\Re(\overline{Y_{11}}) = g_m + g_{ds}(1 + \frac{C_1}{C_2}) \geq 0$$

$$\Re(\overline{Y_{22}}) = \frac{\omega^2 (C_1 - C_2) C_1}{g_m^2 + \omega^2 C_1^2} g_{ds} \geq 0$$

Stable if $C_{gs} > C_{gd}$

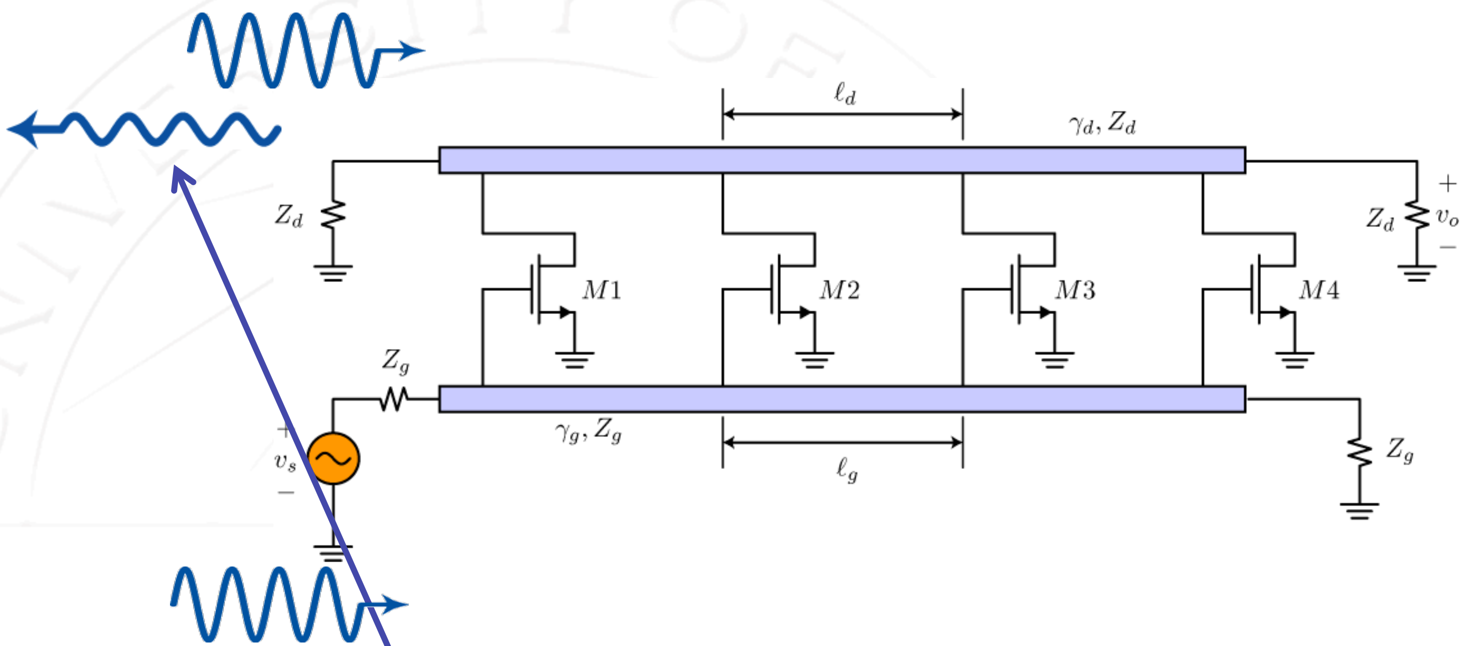
Unilateralization of Cascode Device





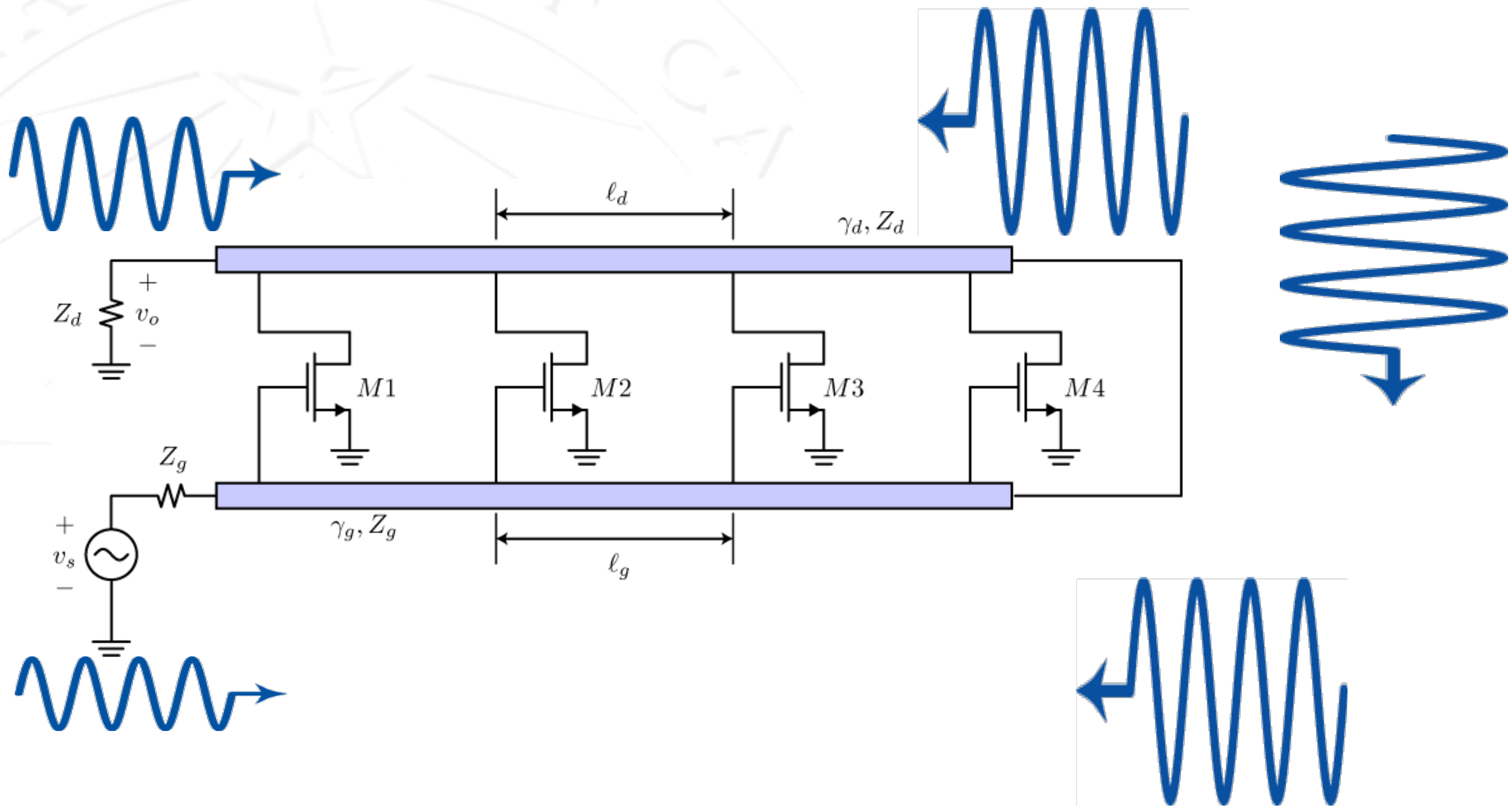
- Possible to simultaneously cancel the real and imaginary of Y_{12} using a gate inductance on cascode device.
- Substantial gain enhancement possible (MSG 8 dB → 20 dB).

Classic Distributed Amplifier



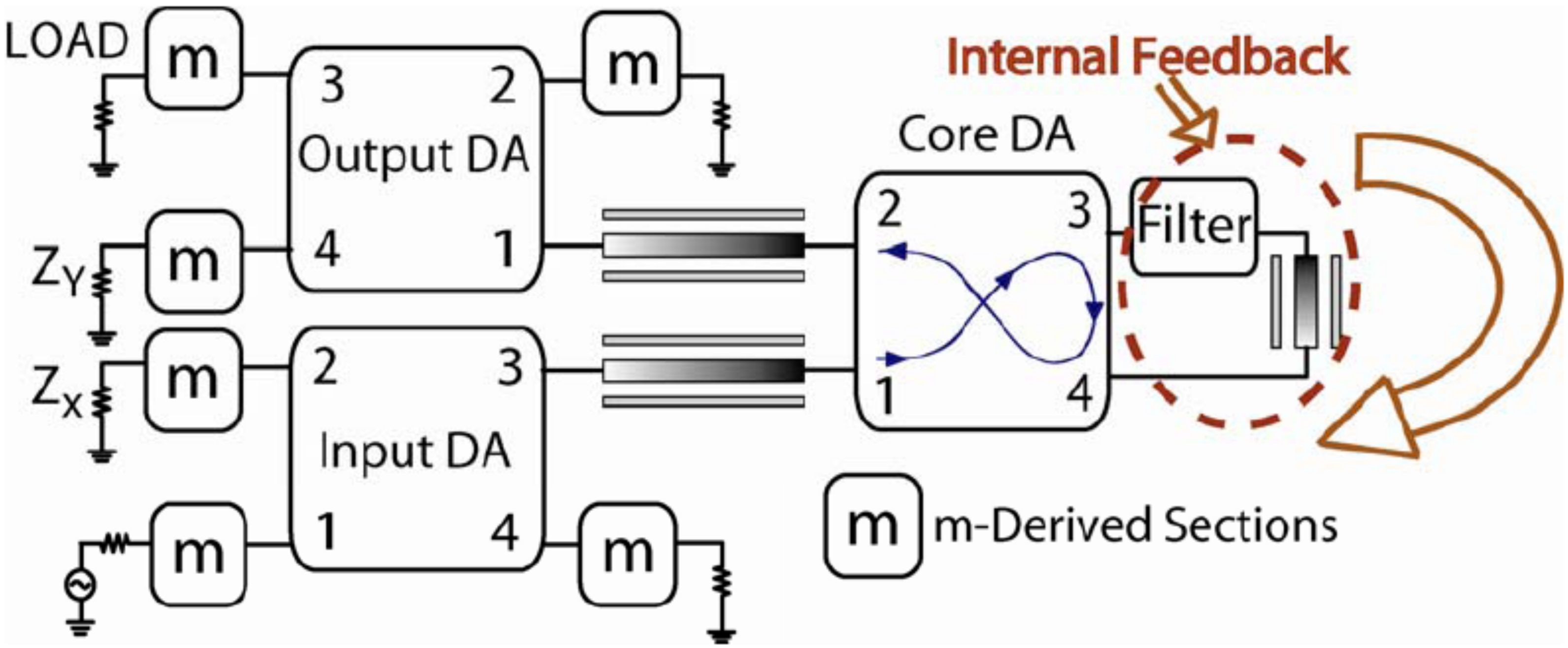
Power traveling to this side cancels out due to phase imbalance.

DA with Internal Feedback



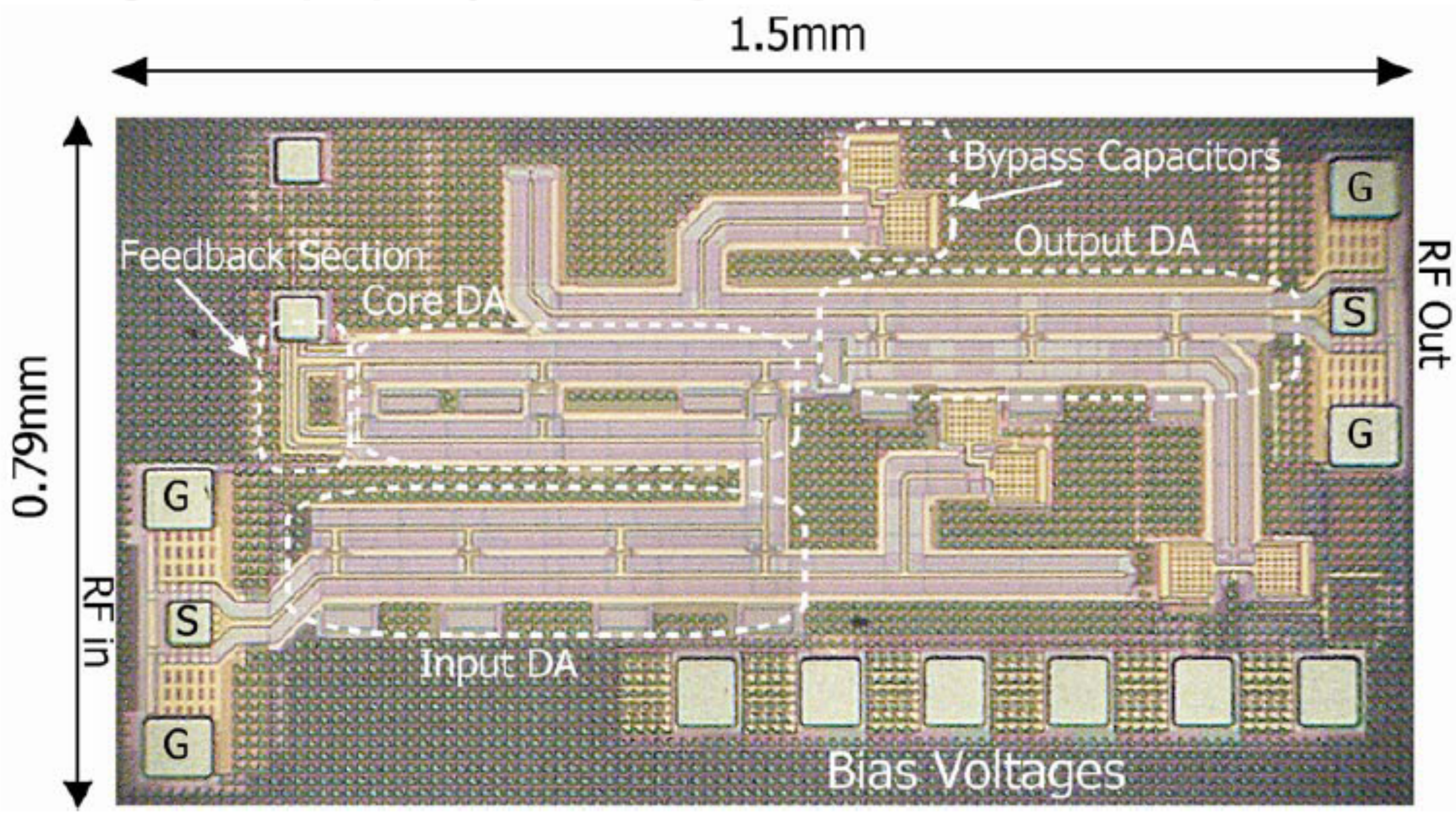
Multiplicative Gain Boosting From Feedback

Proposed Cascade DA



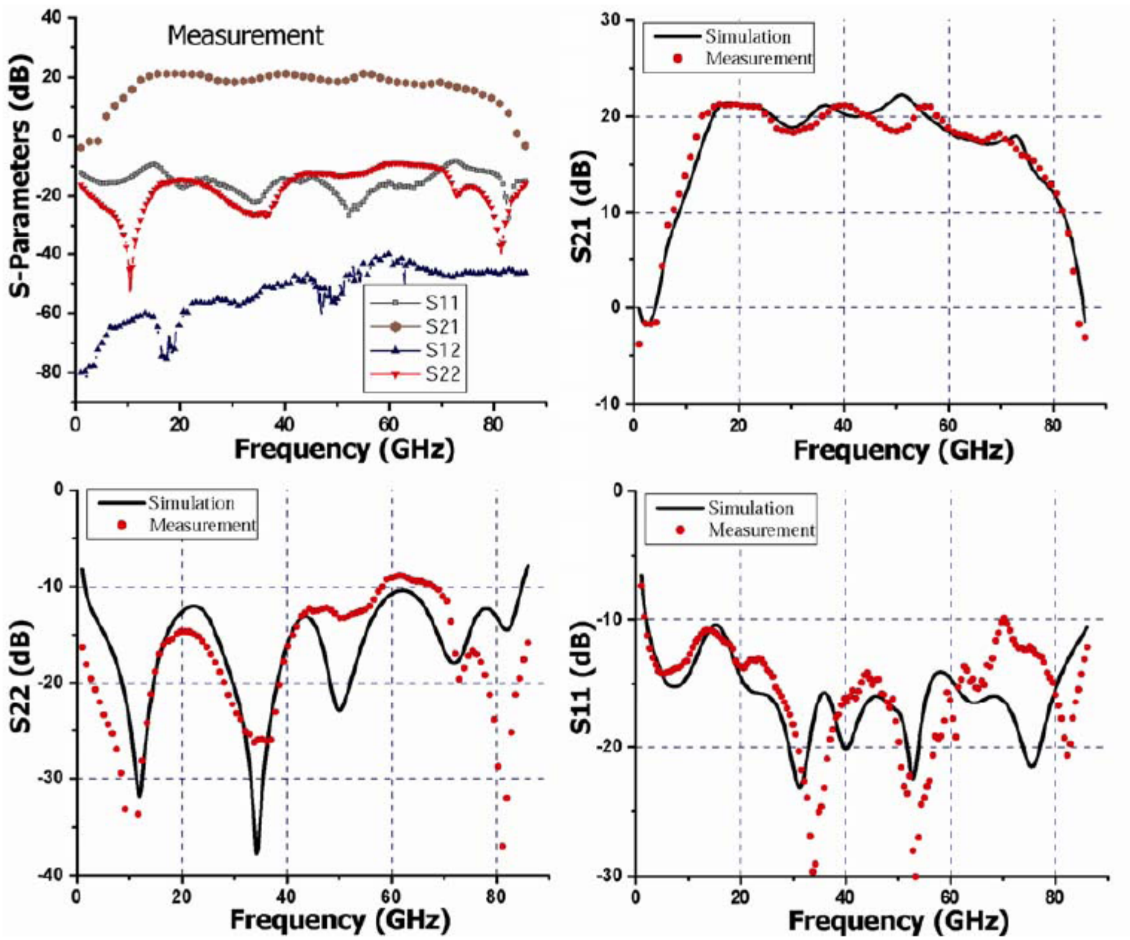
- Conventional DA's at input and output with *m*-derived sections
- Gain boosting internal feedback DA at core

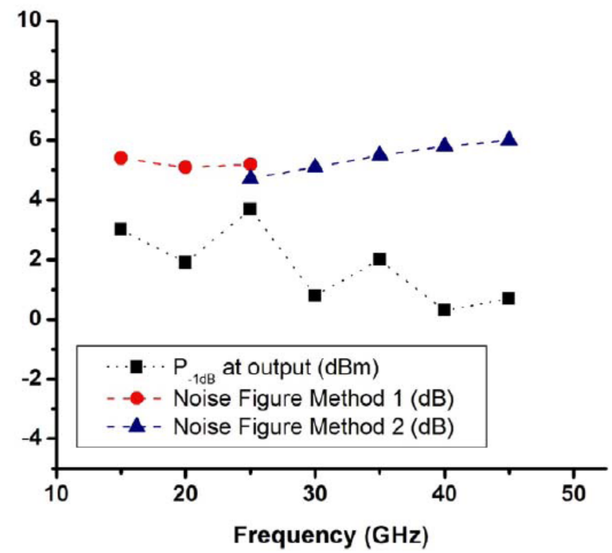
Die Photo



1.5mm
0.79mm
Bypass Capacitors
Output DA
Feedback Section
Core DA
Input DA
Bias Voltages
RF in
RF Out
G
S
G
G
S
G

Measured Response





60 GHz Front-End Receiver

Bagher Afshar, Yanjie Wang
Ali M. Niknejad

60GHz Link Margin

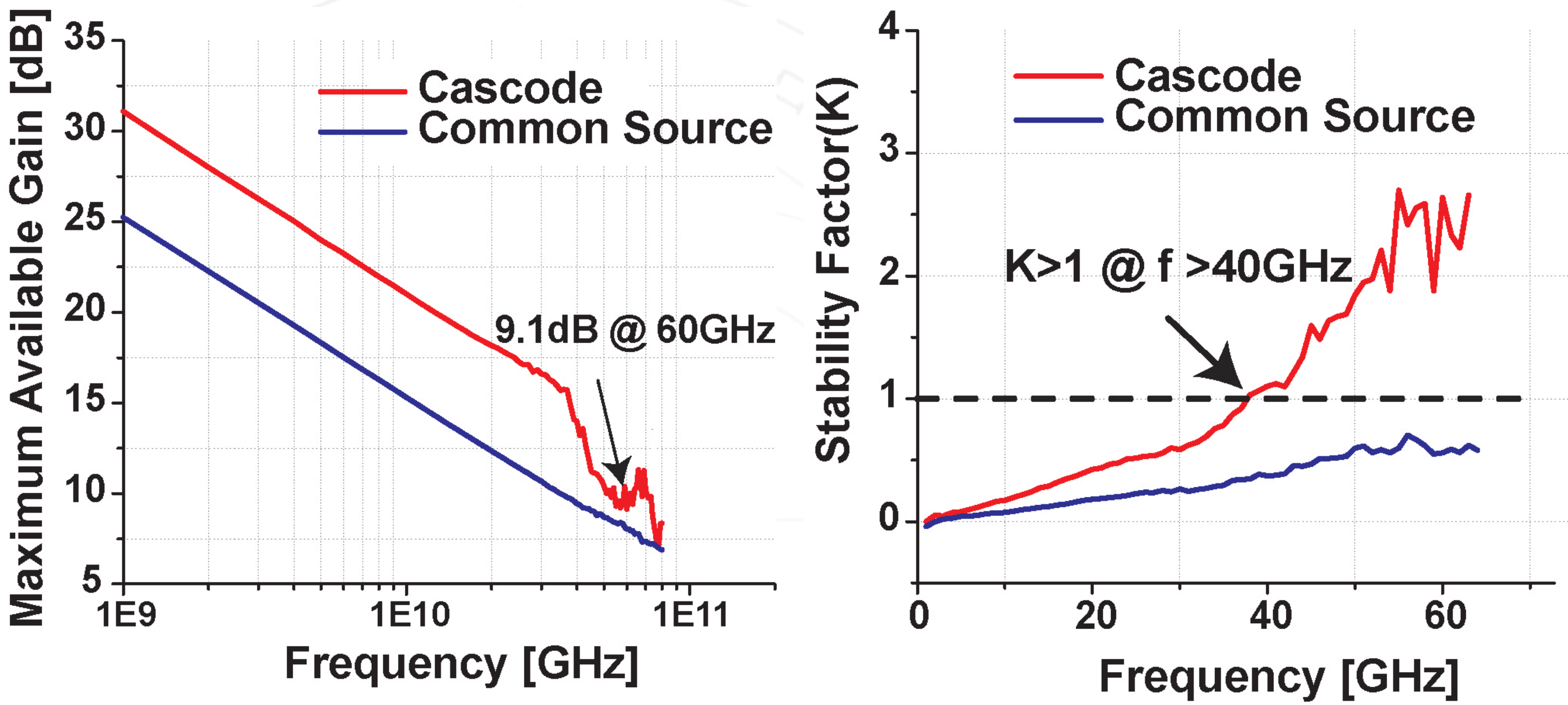
Link budget for a 1Gb/s 60GHz wireless system at ~1m communication distance

Tx Power	+10dBm	PA at P_{-1}dB
Tx Antenna Gain	+2dB	
Path Loss	-68dB	Path loss at 1m
Shadowing/ Fading Loss	-10dB	
Rx Antenna Gain	+2dB	
Net Signal Power	-64dBm	

Background Noise	-174dBm	KT at room temp
Noise BW	+90dB	1GHz noise BW
Noise Figure	+10dB	NF of receiver
Net Noise Power	-74dBm	

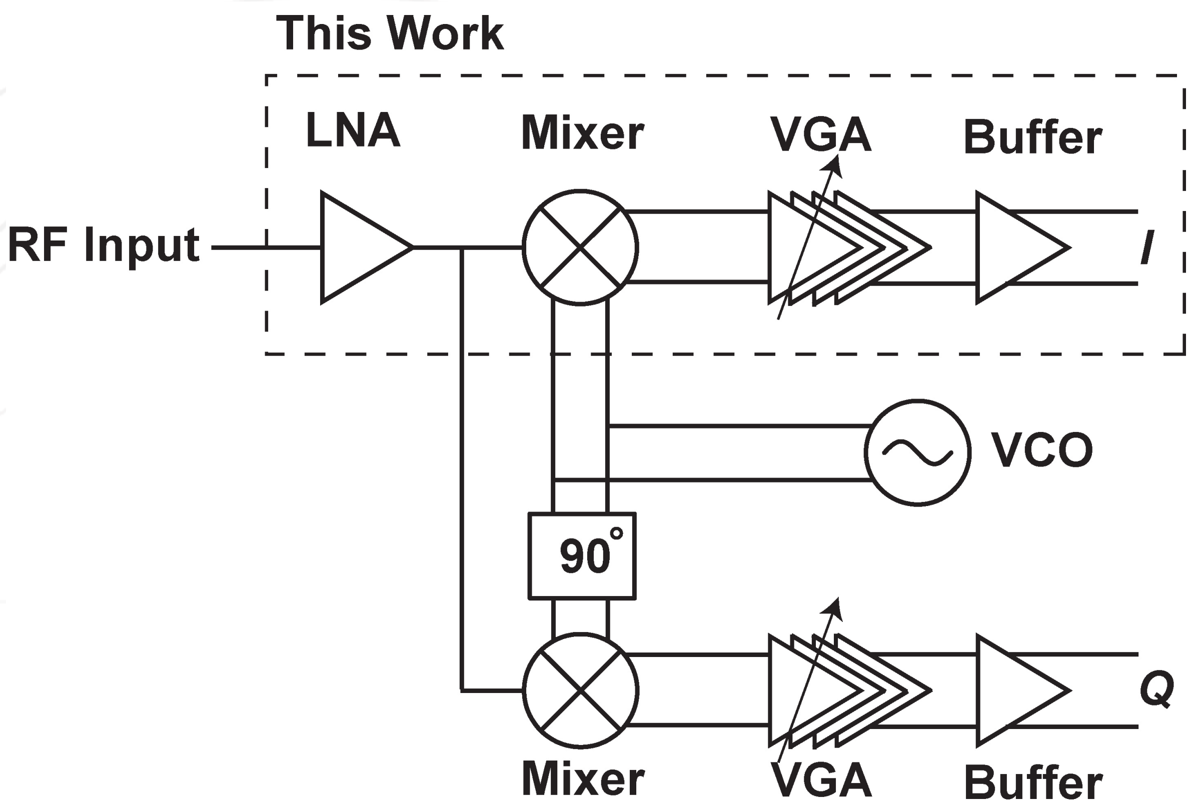
SNR at input =**10dB** adequate for many modulation schemes

Process Performance



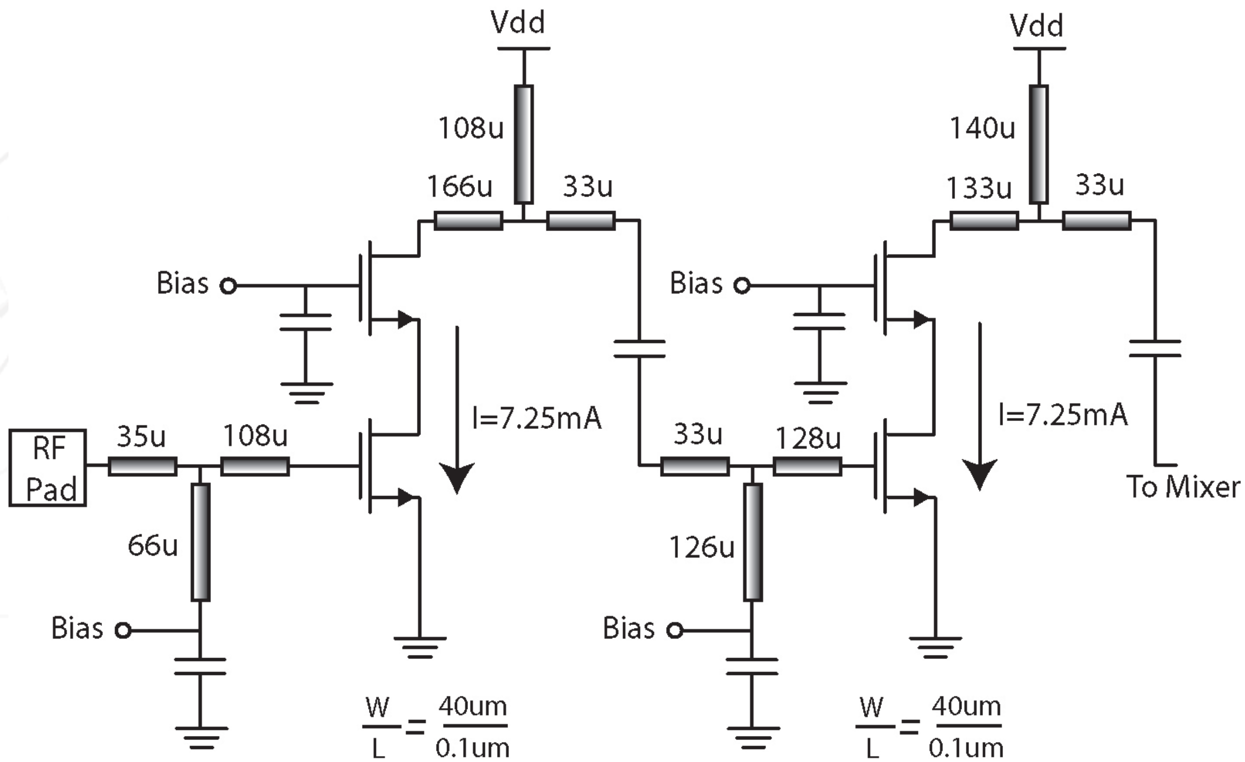
- 90nm digital process with f_T=100GHz
- Cascode device unconditionally stable for *f* >40GHz
- Maximum stable gain is 9.1dB for cascode and 8.2dB for a common source device

60GHz Front-End Receiver



- Includes LNA, Mixer, VGA, DC off-set cancellation loop, and output buffer
- Output buffer included for measurement purposes

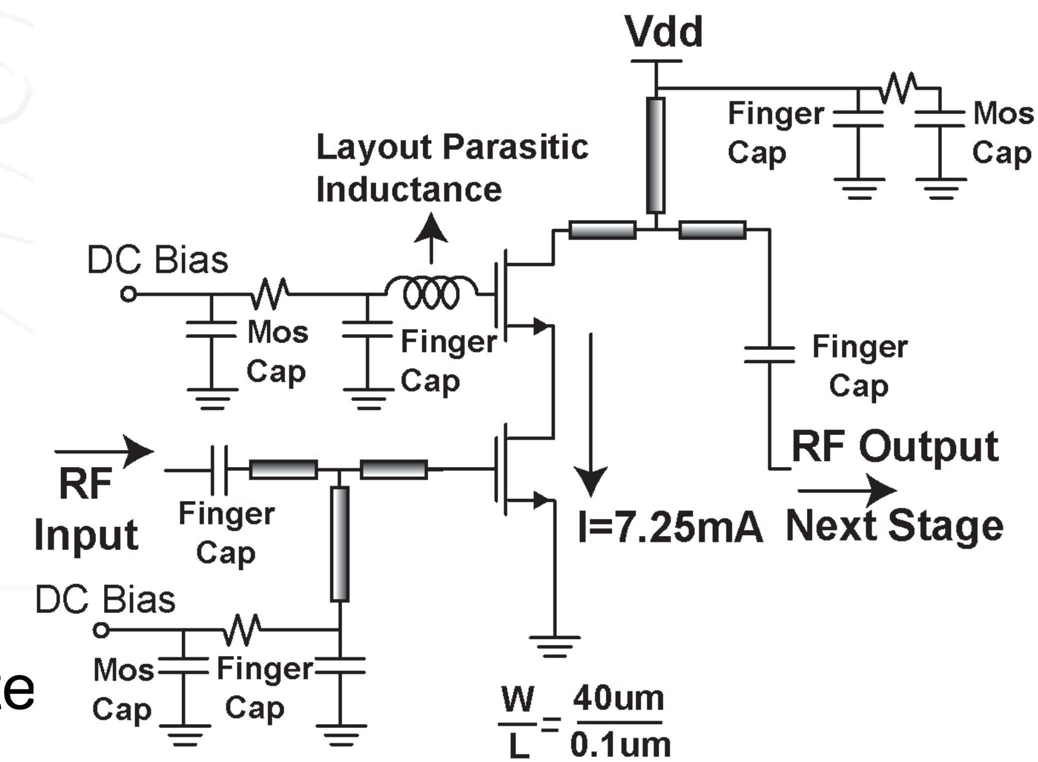
LNA Schematic



- Two stage cascode LNA
- CPW Transmission line with Z_0 =50.8Ω
- Consumes 14.5mW from a 1V supply
- LNA output matched to 50Ω

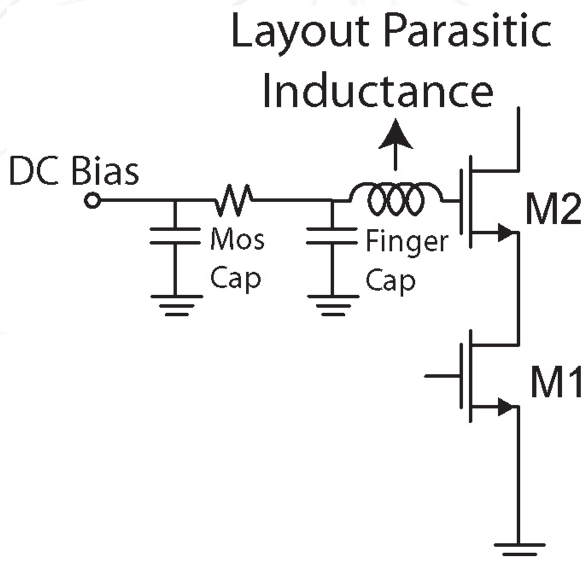
Cascode Design Issues

- Shared junction devices
- Unconditionally stable at f =60GHz
- High maximum available gain of 9.1dB at 1V
- High isolation (S_{12})
- Modeling required for gate of the cascode transistor
- Bias circuit uses C-R-C network to prevent low frequency oscillation

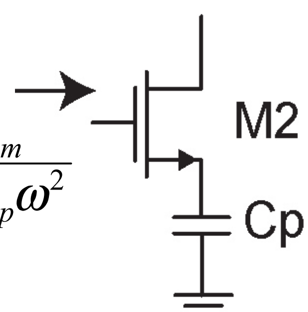


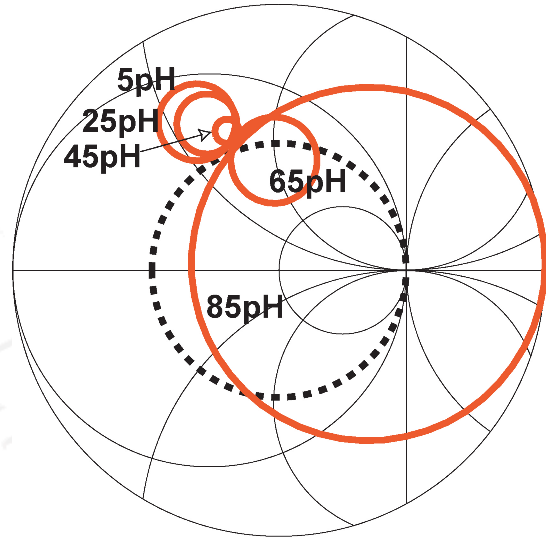
Cascode Gate Inductance

- Modeled cascode gate inductance ~ 25pH

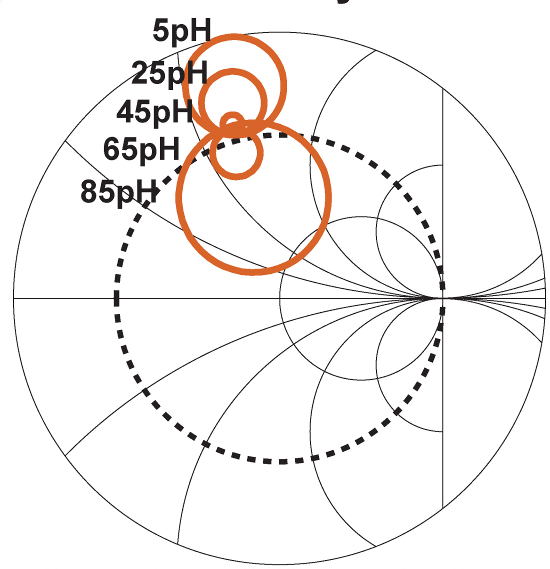


$$\mathrm{Re}(Zin) \approx \frac{-g_m}{C_{gs} C_p \omega^2}$$





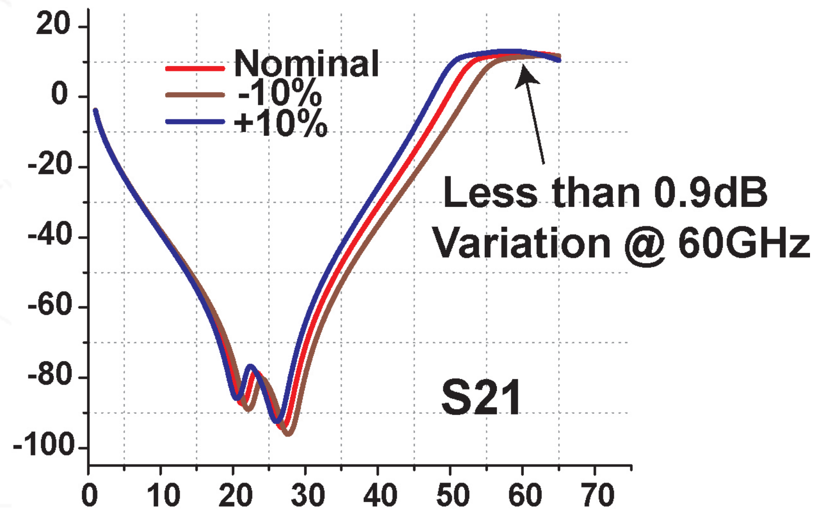
Source stability circles

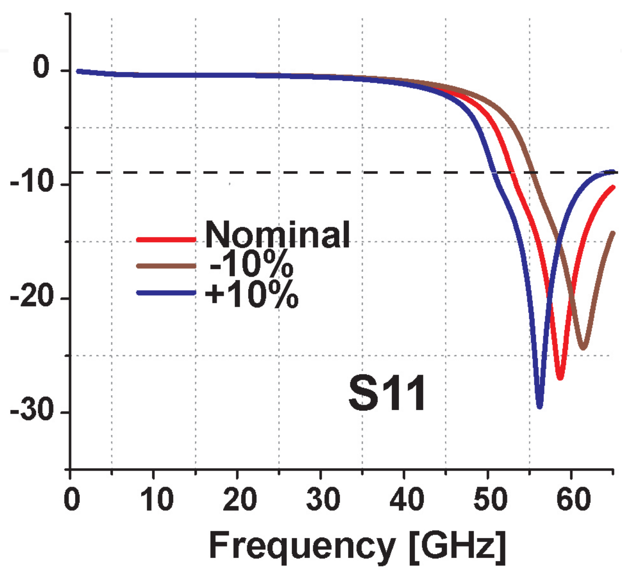


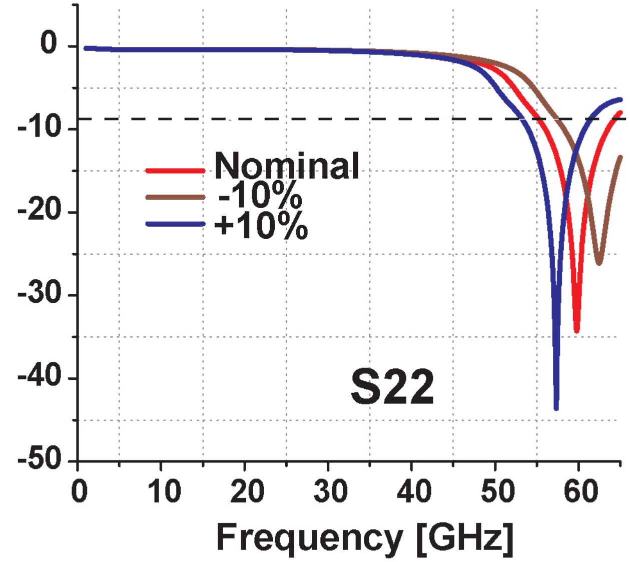
Load stability circles

LNA Simulated Process Variation

- Vary T-line lengths to emulate process variations
- Electrical length variation due to layout dependent performance

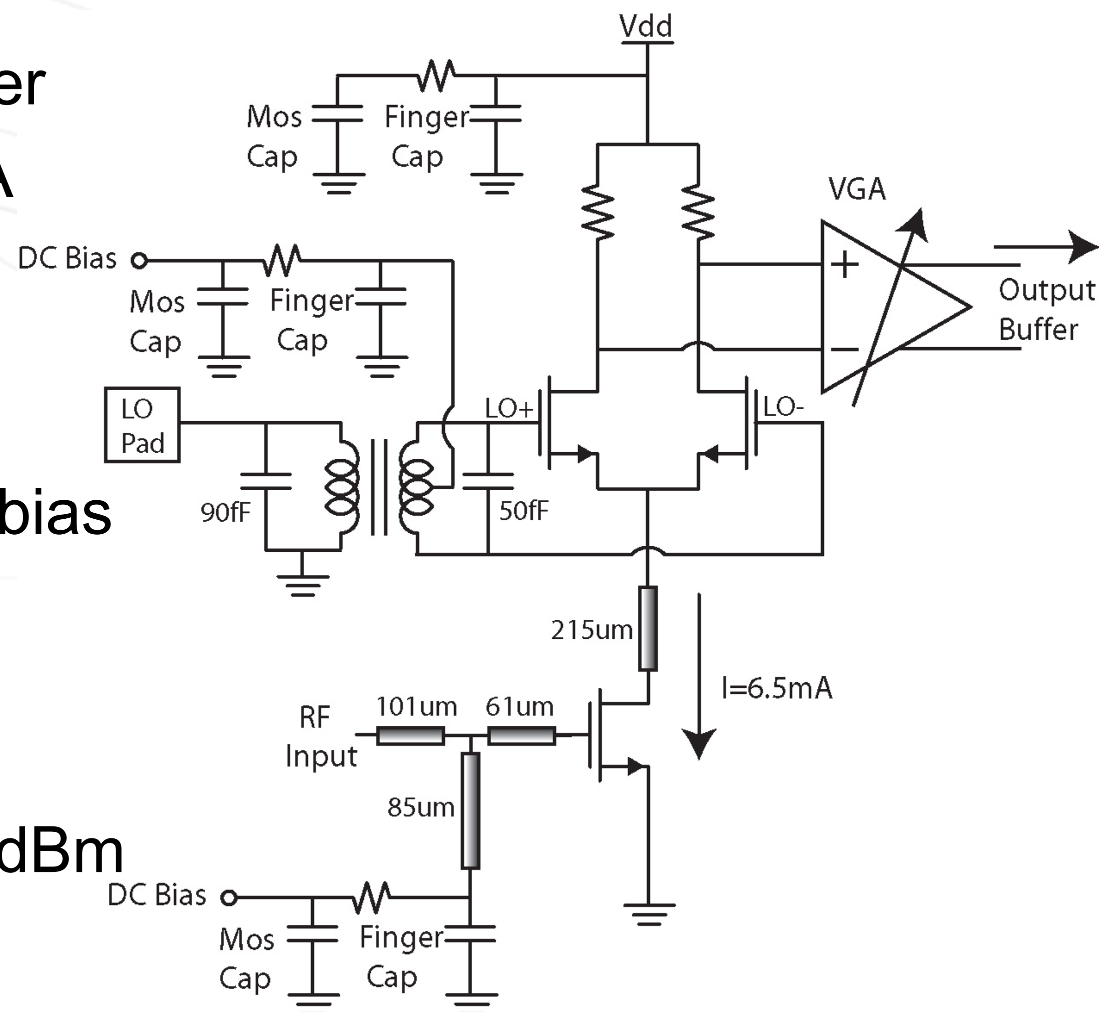






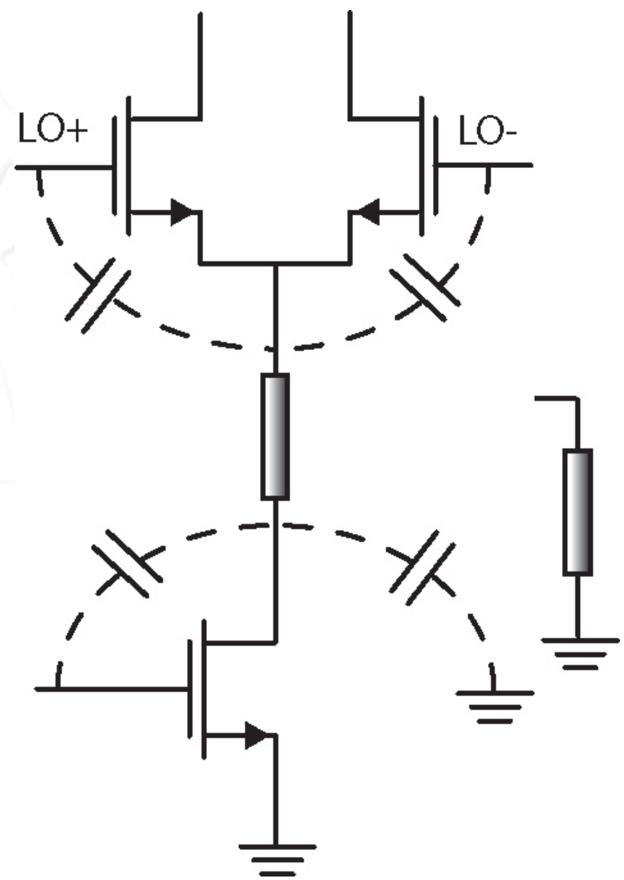
Mixer Schematic

- Single Balanced Mixer
- Mixer drives the VGA differentially
- On-chip tuned balun
- Balun center tap provides convenient bias point
- Gain enhancement tuning network
- Low LO Power= -2.5dBm
- Power consumption =6.5mW

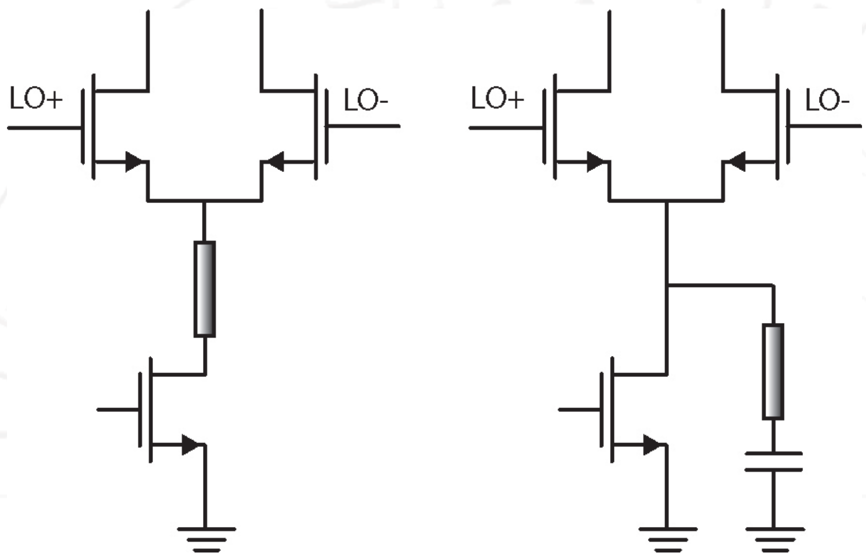


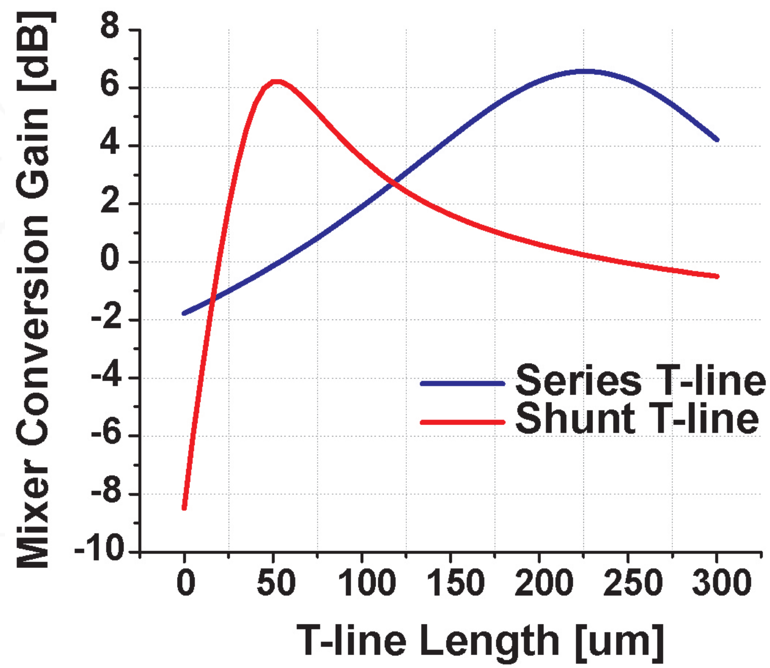
High Frequency Loss Mechanism

- High frequency signal loss through the intersection parasitic capacitances
- Conversion gain could be improved more than 7dB by tuning this node



Gain Enhancement Tuning Network



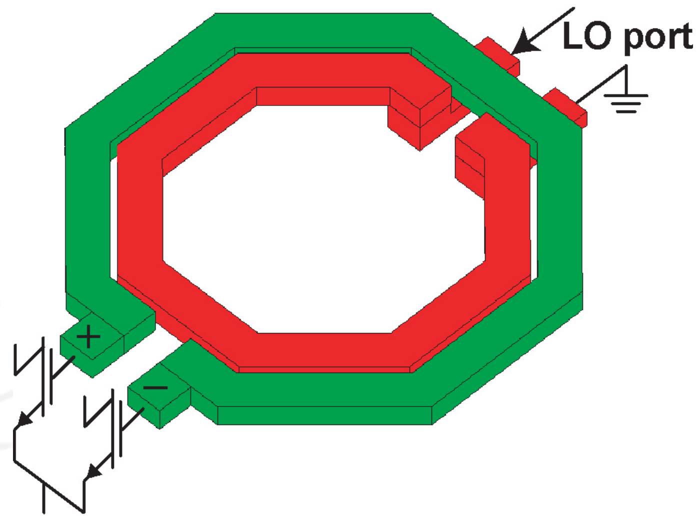


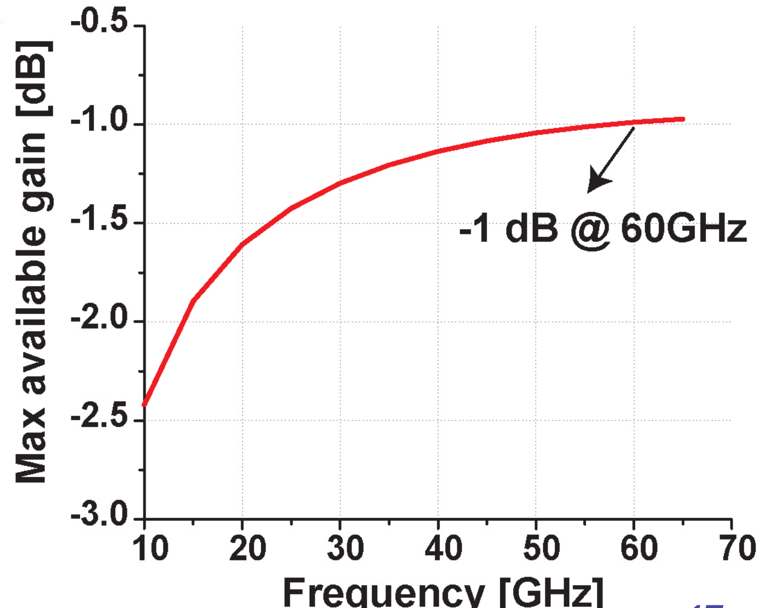
- Series tuning transmission line is less sensitive to variations in electrical length
  - It's longer and more natural to layout
  - Mainly concerned about modeling errors rather than actual length variation

Balun Design

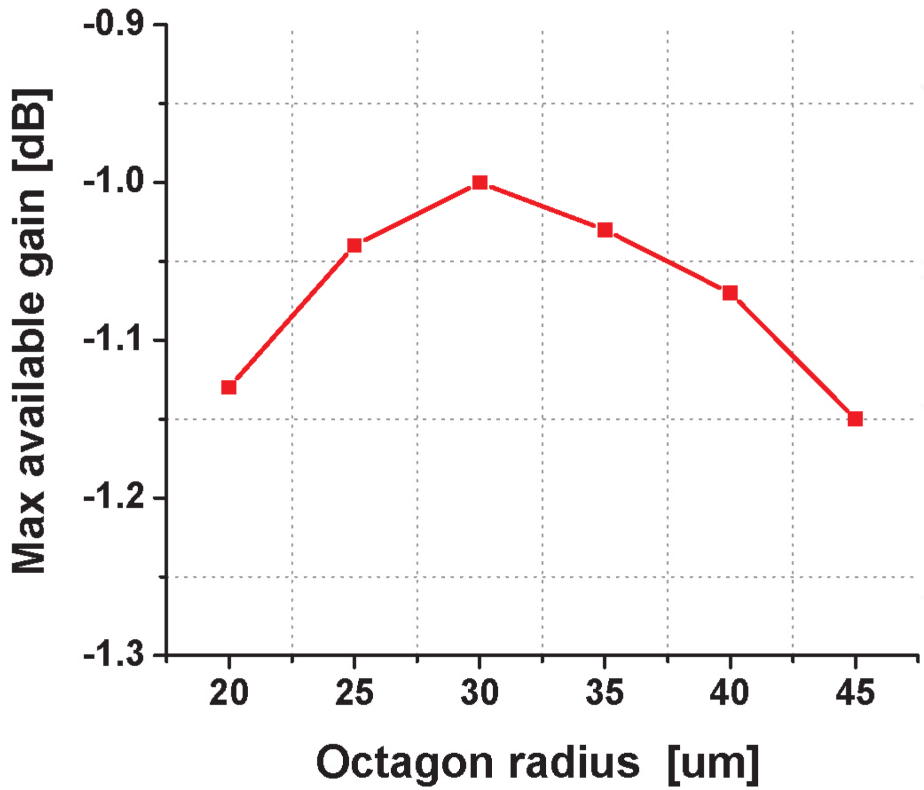
- Single-turn lateral balun
- Converts the single-ended LO

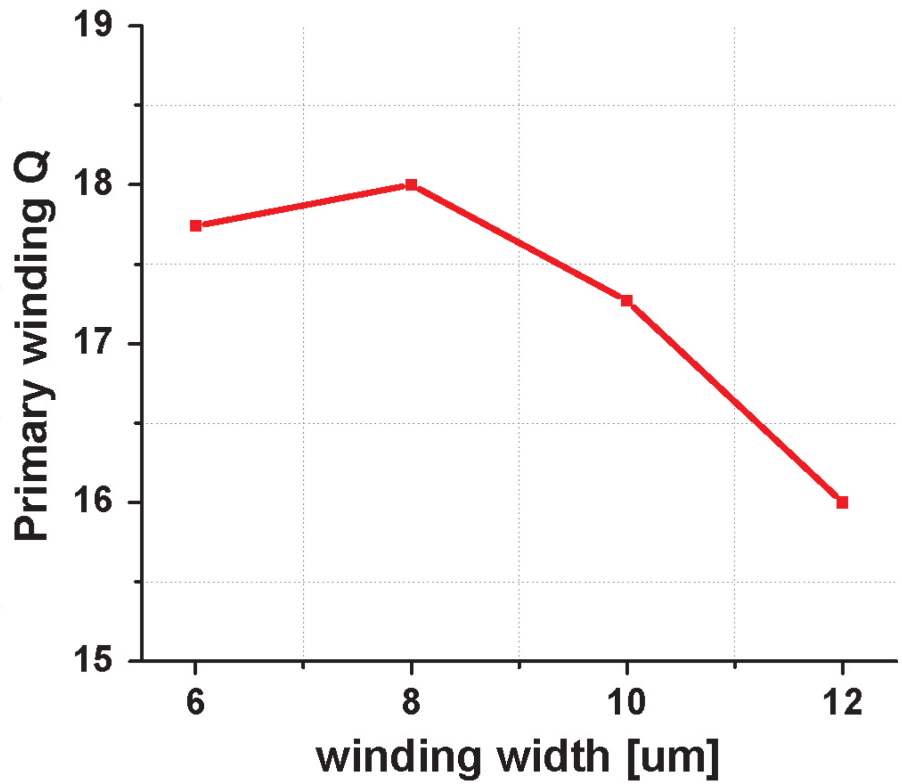
  signal to differential
- Matches the LO port directly to 50Ω
  - Removes the need to add additional matching networks
  - Decreases the LO power loss





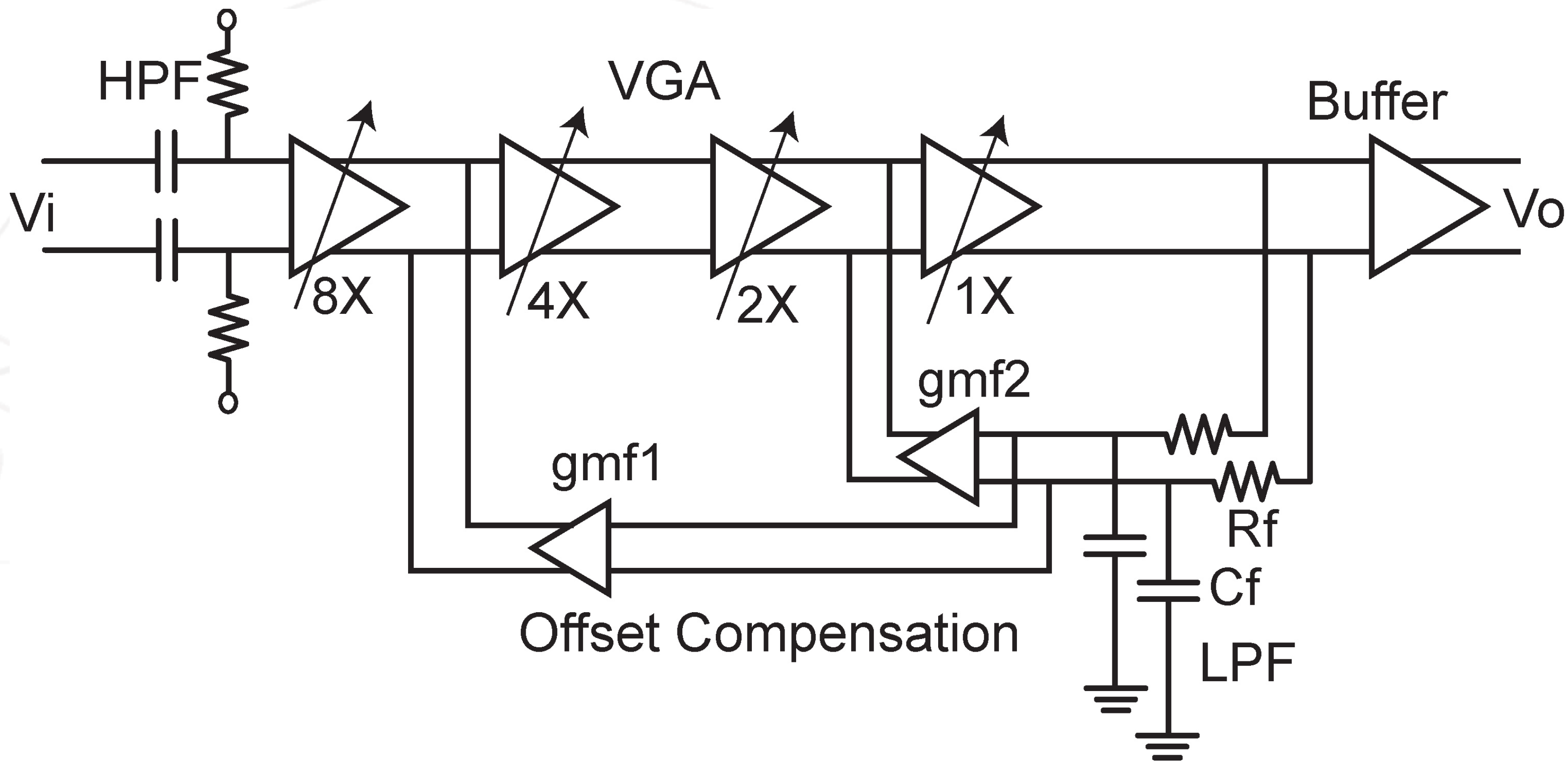
Simulated Balun Performance





- Optimum width and spacing to minimize the loss
- Design depends on transformer coupling (*K*) and winding Q factor

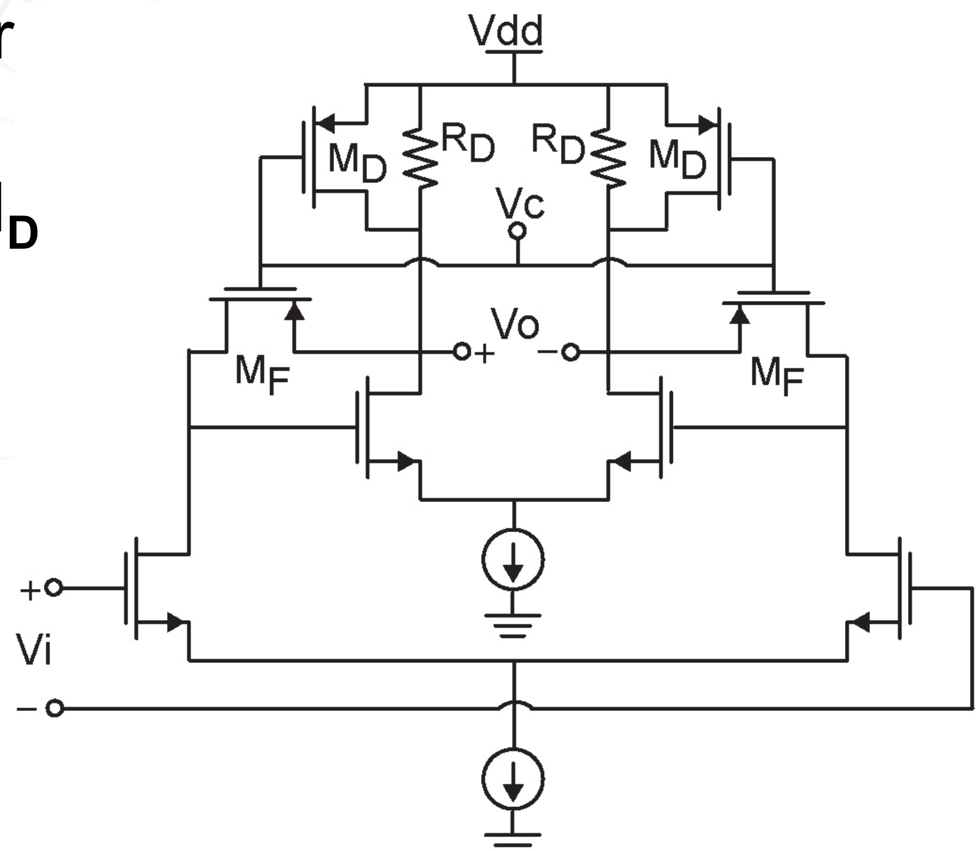
VGA Schematic



- VGA: variable gain, wide bandwidth, wide tuning range
- DC Offsets Correction: input & inter-stage offset correction
- Inverse Scaling: bandwidth extension, reducing power

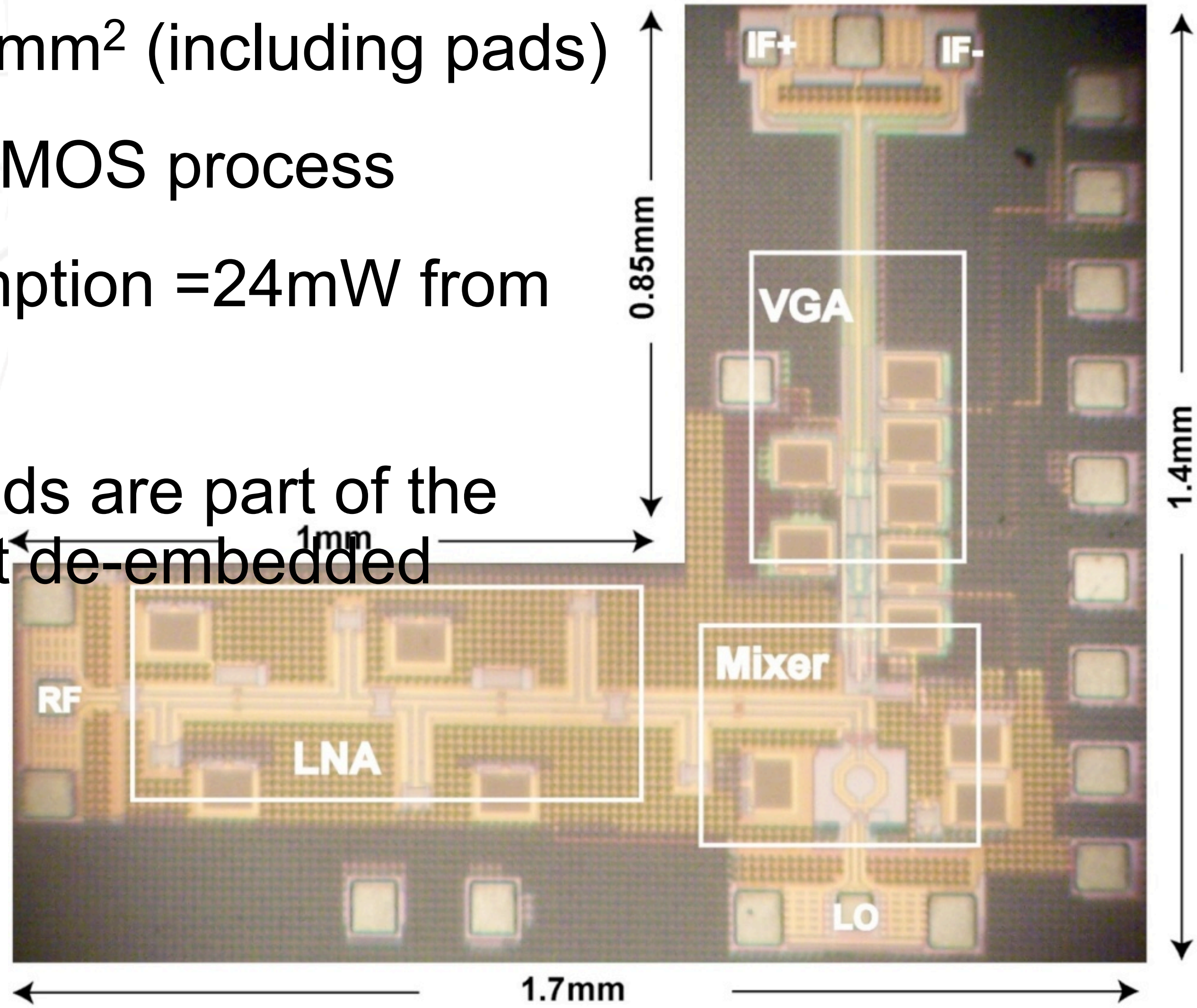
VGA Cell Schematic

- Modified Cherry-Hooper amplifier
- Wide tuning range by M_D and M_F
- Vc is analog control voltage
- Vdd=1V

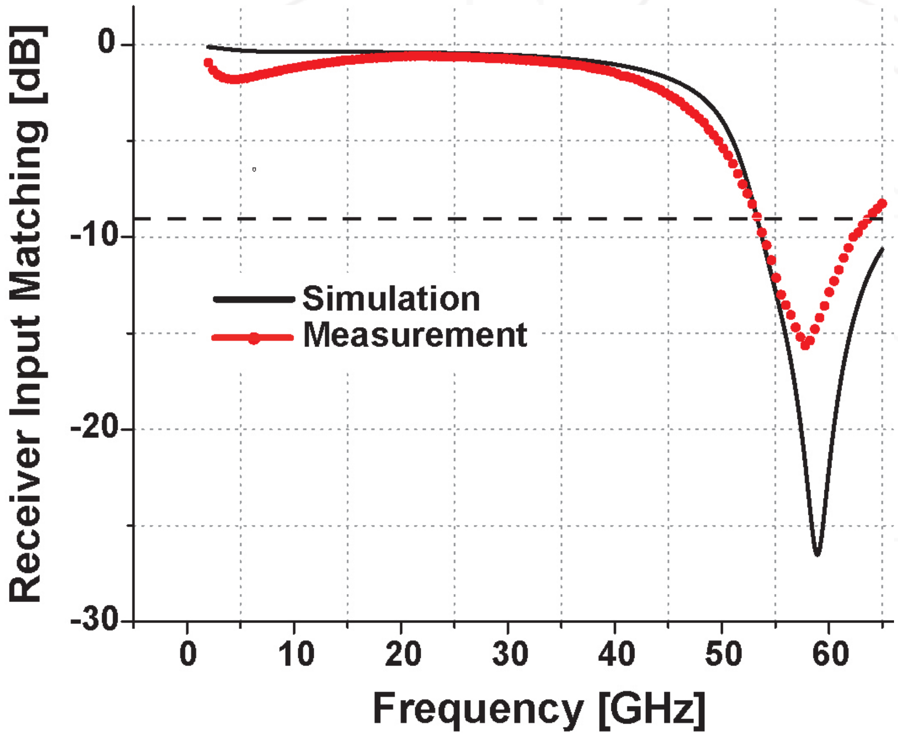


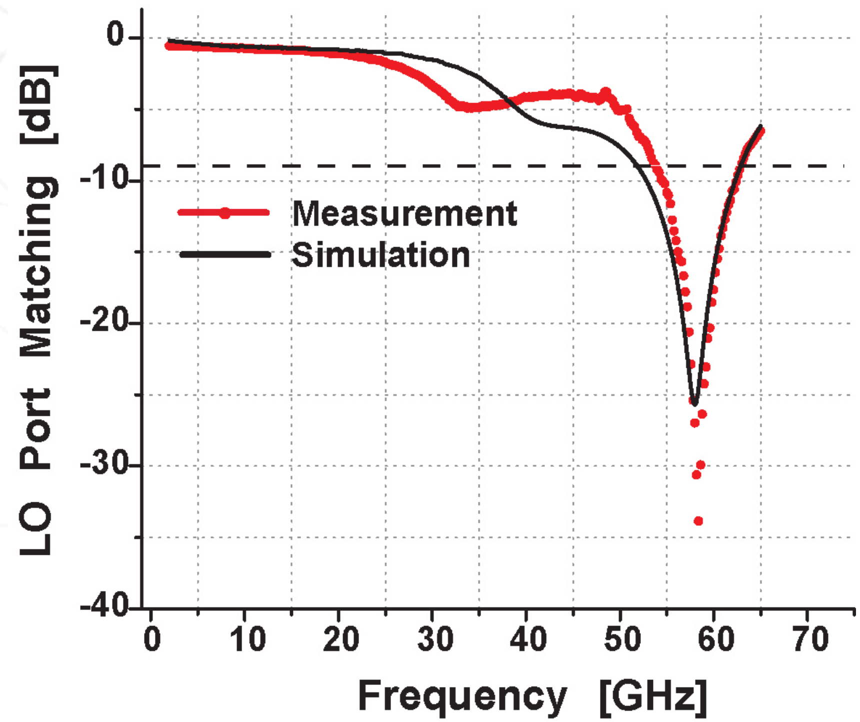
Die Photo of the FE RX

- Die area=1.55mm² (including pads)
- 90nm digital CMOS process
- Power consumption =24mW from 1V Supply
- The RF/DC pads are part of the design and not de-embedded



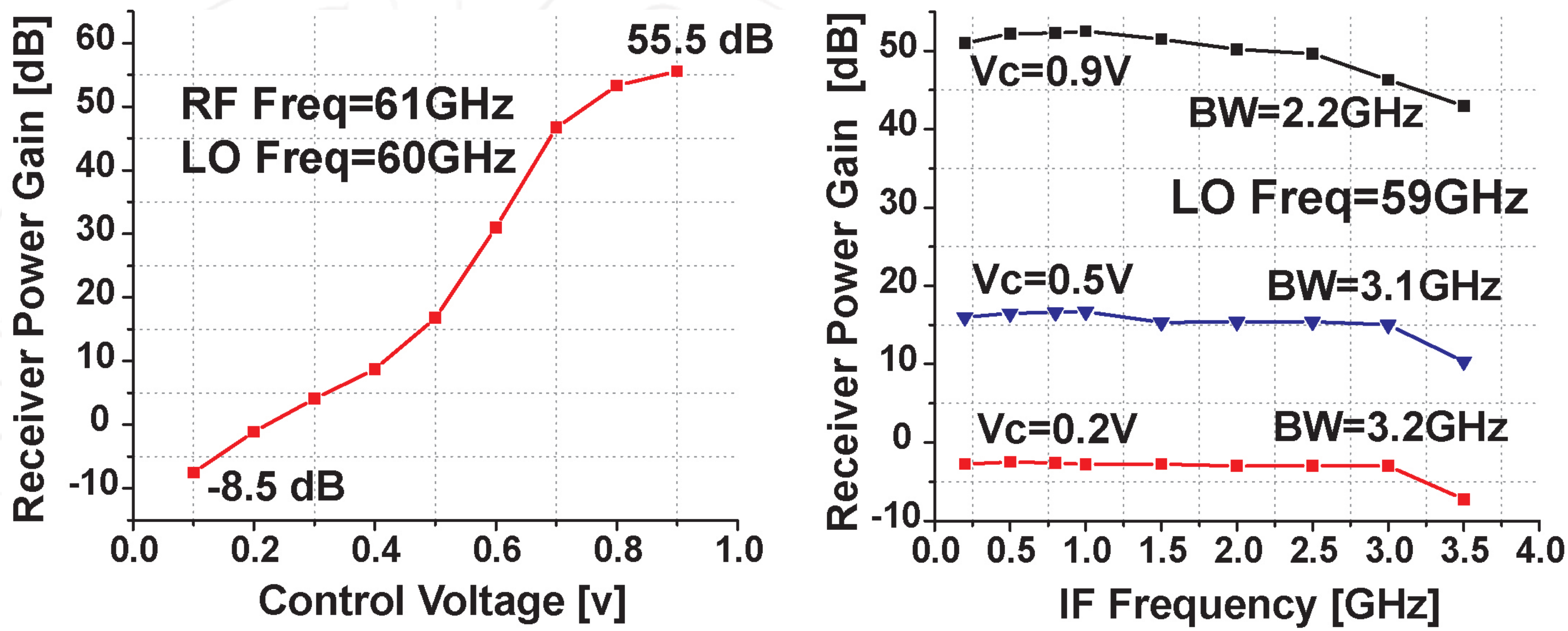
RF and LO Port Matching





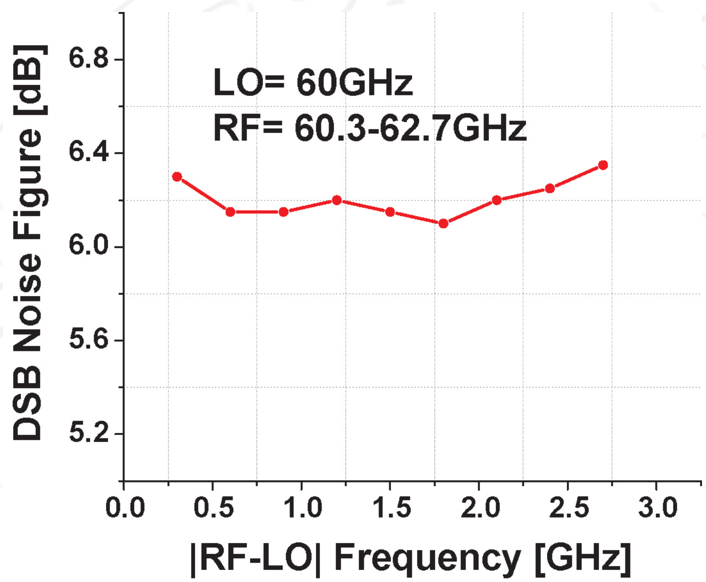
- Input match <-15dB (center) and <-9dB for the 60GHz band (57GHZ-63GHz)
- Small signal LO port match < -25dB (center) and <-9dB for the 60GHz band

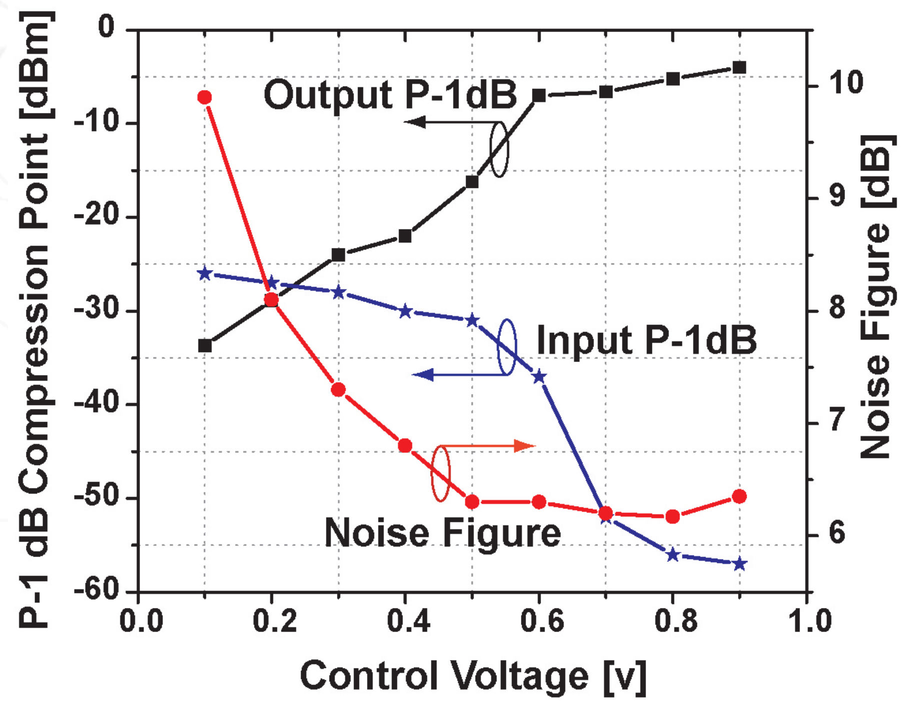
Receiver Power Gain and BW



- Peak receiver gain 55.5dB
- Gain tuning range from -8.5dB to 55.5dB
- Receiver IF bandwidth > 2.2 GHz
- IF bandwidth varies from 2.2GHz to 3.2GHz (high gain to low gain mode)

Noise and Linearity





- Noise figure measurement using 50-75GHz noise source
- DSB NF < 6.35dB at high gain mode (V_c=0.8V)
- P-1dB= -26dBm at low gain mode (V_c=0.1V)

Performance Summary

Technology	90nm digital CMOS	f_T=100GHz
Power Gain	-8.5 to +55.5dB	>60dB gain tuning range
Noise Figure	6.1-6.35dB	High gain mode
Input P_{-1dB}	-26dBm	Low gain mode
Input return loss	>-15dB (center)	>-9dB across the band
LO port return loss	>-25dB (center)	>-9dB across the band
Upper f_{-3dB}	2.2GHz-3.2GHz	High gain-Low gain
Power Dissipation	24mW	1V Supply

Conclusion

- CMOS technology offers
  - Fast transistors (low noise)
  - Low supply voltage and poor linearity
- Circuit techniques can overcome many limitations in linearity and power
- Technology scaling mostly beneficial for mm-wave
  - High f_{max} transistors, reduced power consumption
  - Circuit techniques to realize broadband and near f_T designs

Acknowledgements

- DARPA TEAM Program, C2S2
- STMicroelectronics
  - chip fabrication and support
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- UC Micro Program
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