One Day-Short Course on RF MEMS
Switches, Varactors and their Applications

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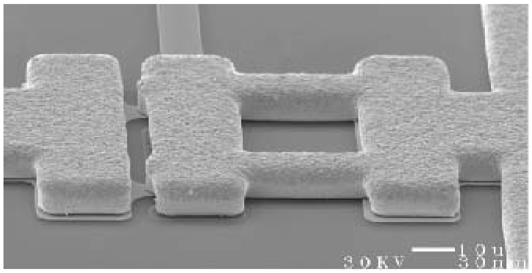
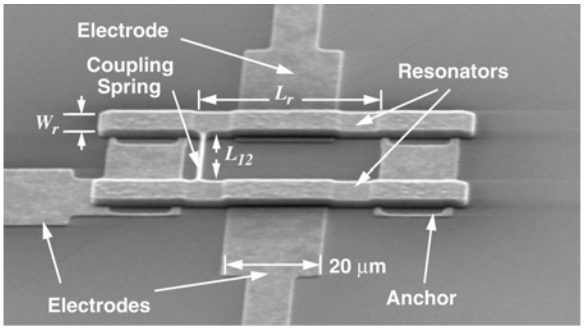
RF Micro-Electro-Mechanical Systems

RF : $\sigma = 2\text{-}4 \cdot 10^7$ S/m



- **Metals dominate fabrication process**
- **Substrates are glass, Si, GaAs**
- **Dimensions and lithography: Easy**
- **Post CMOS compatible**

Polysilicon : $\sigma = 0.5\text{-}5 \cdot 10^5$ S/m



- **Polysilicon dominates fab. process**
- **Substrate is silicon**
- **Dimensions and lithography: hard**
- **Post CMOS compatible**
- ***We will not cover this type of MEMS***

Why RF MEMS Switches and Varactors ?

- ***Amazingly linear device (IIP2 and IIP3 > 70 dBm).***
- ***Excellent for tuning (high Q)***
- ***Very low loss (0.1 dB DC-120 GHz).***
- Does not require MBE or MOCVD, GaAs or InP wafers. No 0.1-0.15 um E-beam lithography. Does not require ohmic and Schottky contact. Requires 3 um lithography.
- Can be built on glass or low-cost silicon substrates. Low cost processes. Can be built above silicon IC.
- Many academic/government labs and companies in USA and Europe have arrived to 10-100 Billion cycles (easily).
- *It is possible to build multifunctional devices using RF MEMS.*

Active Companies in RF MEMS

THE GREAT (> 10 B Cycles)

- Raytheon (Capacitive)
- Lincoln Labs (Capacitive)
- Radant MEMS (Metal Contact)
- *Motorola* (Metal Contact)
- Rockwell (Metal Contact)
- Terravicta (Metal Contact)
- Wispry (Metal Contact)
- Thales (Capacitive Contact)
- NMRD (Capacitive Contact)

THE LITTLE KNOWN

- Northrop Grumman (Capacitive)
- TRW (Metal-Contact)
- Mitsubishi (Capacitive)
- *Bosch* (Capacitive)
- Samsung (Metal Contact)
- Intel (Metal Contact)

THE GOOD (0.1-1B Cycles)

- IBM (Metal Contact)
- Omron, Japan (Metal Contact)
- *HRL/Raytheon* (Metal Contact)
- Univ. of Michigan (Capacitive, Metal Contact)
- *Univ. of Illinois* (Metal Contact)
- Magfusion (Magnetic, Metal Contact)
- *Cronos/JDS Uniphase* (Therm., Metal Contact)
- Microassembly (Metal Contact)
- IMEC (Capacitive)
- Philips (Capacitive)
- Univ. of Limoges (Capacitive, Metal Contact)
- Seoul National Univ. (Capacitive, Metal Contact)
- Univ. of Waterloo (Capacitive, Metal Contact)
- AFRL (Dayton and Hanscom, Capacitive)
- Sandia National Labs (Capacitive, Metal Contact)
- ST Microelectronics
- CEA LETI* (Metal Contact)

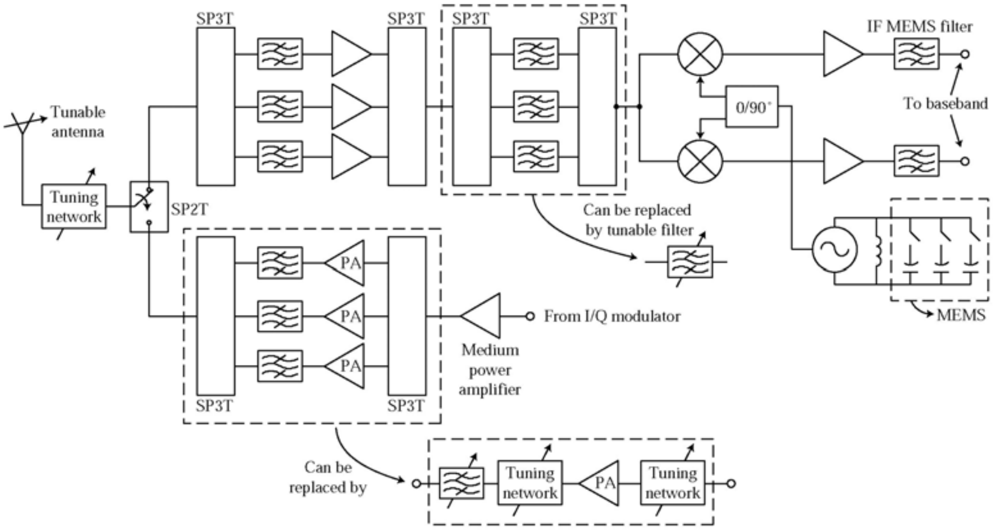
THE SILENT COMPANIES

- XCOM Wireless

Common Misperceptions in RF MEMS

- ***RF MEMS is unreliable?***
  - *This was true until 2004. Now, we can take them to > 100 Billion cycles at 100 mW of RF power.*
- ***RF MEMS is expensive?***
  - *Not with the new in-situ packaging techniques. The cost of packaging can be <2 cents per device.*
- ***RF MEMS requires non-standard CMOS fabrication?***
  - *Not with the new processes. Look at IBM, WiSpry, etc. with a complete CMOS compatible process.*
- ***RF MEMS is slow?***
  - *Our newest generation switches at 100 ns!*
- ***RF MEMS cannot handle a lot of RF power?***
  - *This is partly true. Watts are possible, but not 10-50 W. However, most applications are < 1 W of RF power.*

RF MEMS in Communication Systems: Example



- Many components possible using RF MEMS
- Can you handle the power in the transmit mode?
- Where do you want to be competitive?

Cost Targets:
Switch: <$0.5
Tunable Filter: <$1
Tunable Matching Network: <$1
Multi-Frequency Antenna: <$1

Motivation

Parameter	RF MEMS	PIN	FET
Voltage of Operation [V]	15-80	3-5	2-5
Current [mA]	0	3-20	0
Power Consumption [mW]	0.03	5-100	0.05-0.2
Switching Time	1-30 µs	2-60 ns	2-60 ns
Isolation (1-10 GHz)	Very High	High	Medium
Isolation (10-40 GHz)	Very High	Medium	Low
Isolation (60-100 GHz)	High	Medium	Low
Loss [dB]	0.05-0.2	0.4-1.2	0.4-1.6
Power Handling [W]	0.1-2	0.1-10	0.1-3
3rd Order Intercept [dBm]	+66-80	+27-45	+27-45

Advantages of MEMS

- Low loss and High isolation
- Low power consumption
- Very high frequency operation
  ($f_T=1/(2\pi R_s C_u)$ = 10-90 THz)
- Very low intermodulation products
- Low-cost fabrication
- High level of integration

Disadvantages

- Slow switching speeds
- Power handling capabilities
- Reliability
- Packaging

The University of Michigan

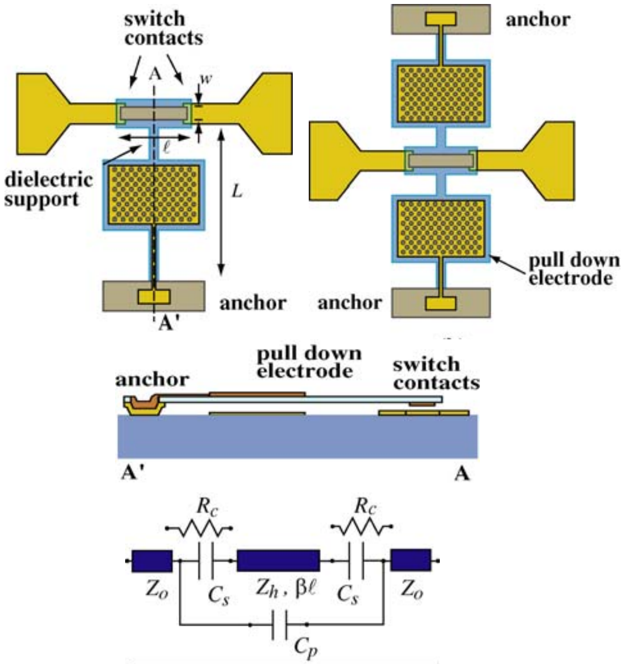
Different Types of MEMS Switches

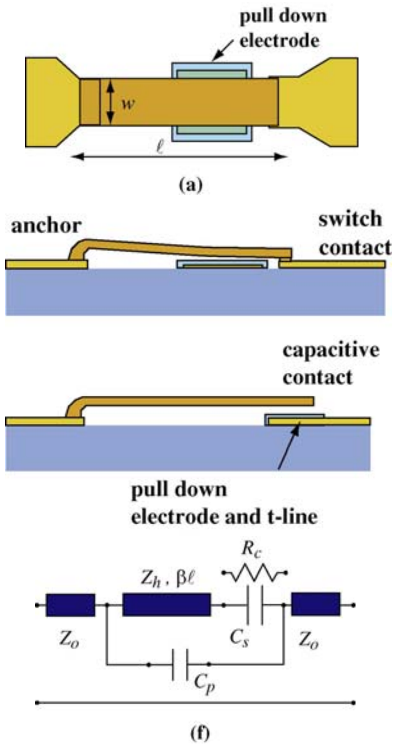
- Actuation:
  - Electrostatic
  - Thermal*/Piezoelectric/Magnetic*
- Contact Type:
  - Metal-to-Metal Contact
  - Capacitive Contact (metal-to-dielectric) – Not good at low frequencies

- Electrostatic Actuation: Dominant (20-90 V)
- Capacitive and Metal Contact switches are both prevalent
- Series and shunt designs are both prevalent (depending on the circuit)
- Magnetic and thermal actuation with electrostatic hold are being developed

* Consumes current, even if temporary with electrostatic or magnetic latch

Series Switches: Broadside and InLine Designs





MEMS DC-Contact Series Switches (Similar to a PIN Diode Switch)

UP-STATE:

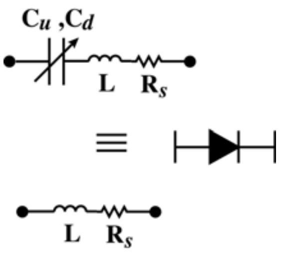
$$|S_{21}|^2 = 4\omega^2 C_u^2 Z_o^2$$

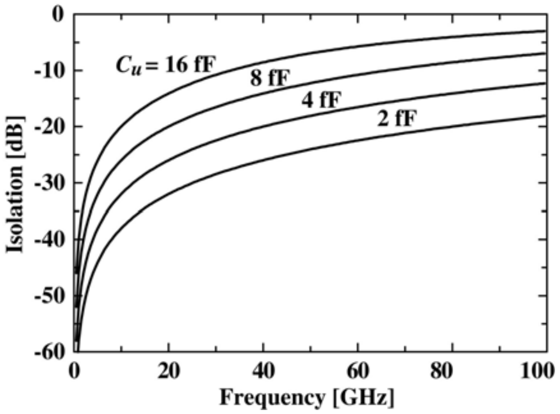
DOWN-STATE:

$$|S_{21}|^2 = 1 - \frac{R_s}{Z_o}$$

$$R_s = 1 - 2\ \Omega$$

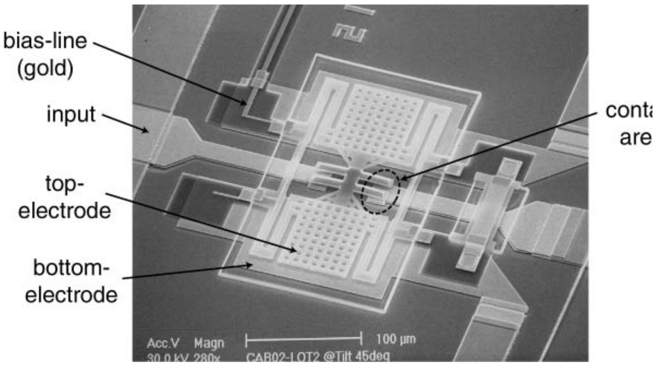
$$|S_{21}|^2 = -0.1 \text{ to } -0.2 \text{ dB}$$

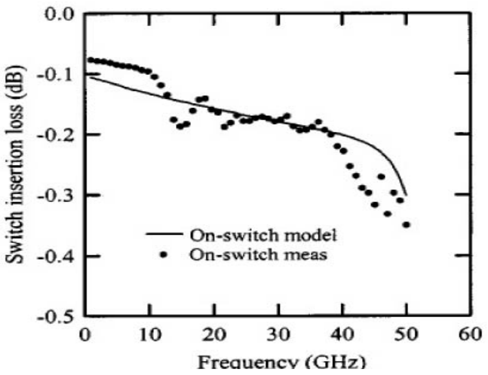


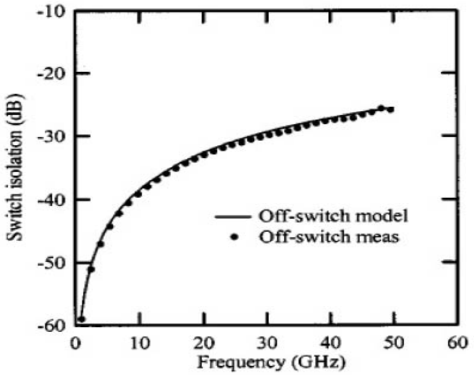


Rebeiz/Muldavin/Rizk

Rockwell DC-Contact Series Switch







- **Biasing circuits decoupled from RF Circuits.**
- **Dimples for improved contact.**
- **Actuation voltage = 70 V, t= 8-10 μs**
- **R_s=1-2 Ω, C_u=1.75 fF**

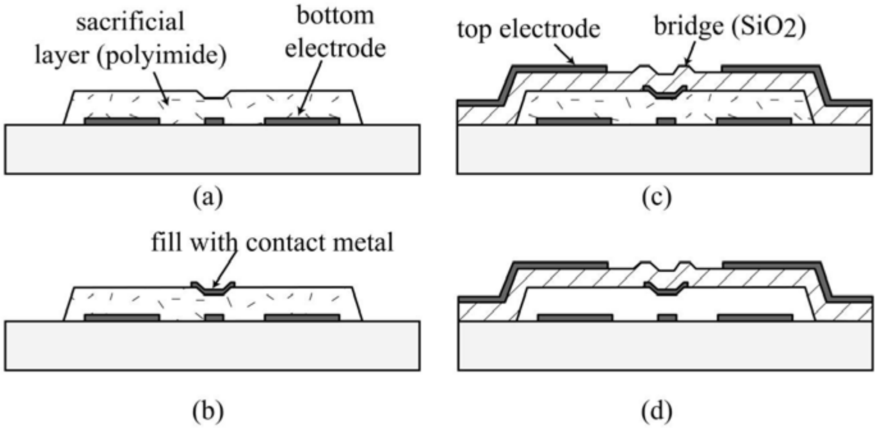
  $f_T = 1/(2\pi R_s C_u)$ = 90 THz
- **RF Performance:**

  Loss = -0.12 dB at 10 GHz

  Isolation = -40 dB at 10 GHz

Rockwell
Science Center

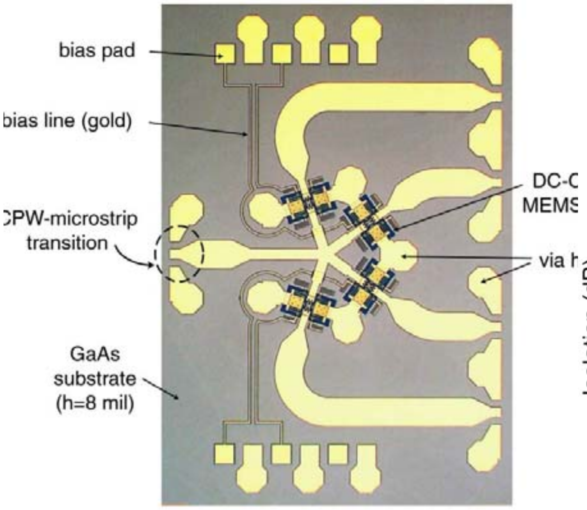
RSC MEMS RF Switch



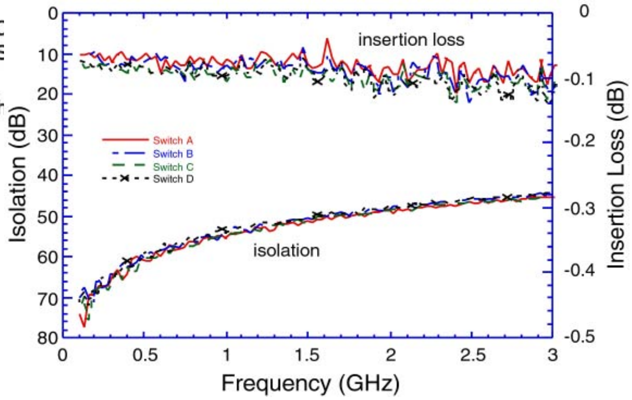
- **Crab-Leg flexure makes it insensitive to residual stress in membrane and much less sensitive to temperature (+/- 10 V over 0-80 C).**
- **Excellent design with very low capacitance, suitable for high-frequency operation.**
- **Planarity is very important. Deposition parameters of 2 μm SiO2 bridge is crucial.**

Rockwell
Science Center

SP4T MEMS Switch Measurements (DC-20 GHz)



- Measured data from 0.1-3 GHz
- IL = 0.1 dB, isolation <-44 dB
- Excellent performance up to 20 GHz
- Switch Networks, Switched Filters, etc..



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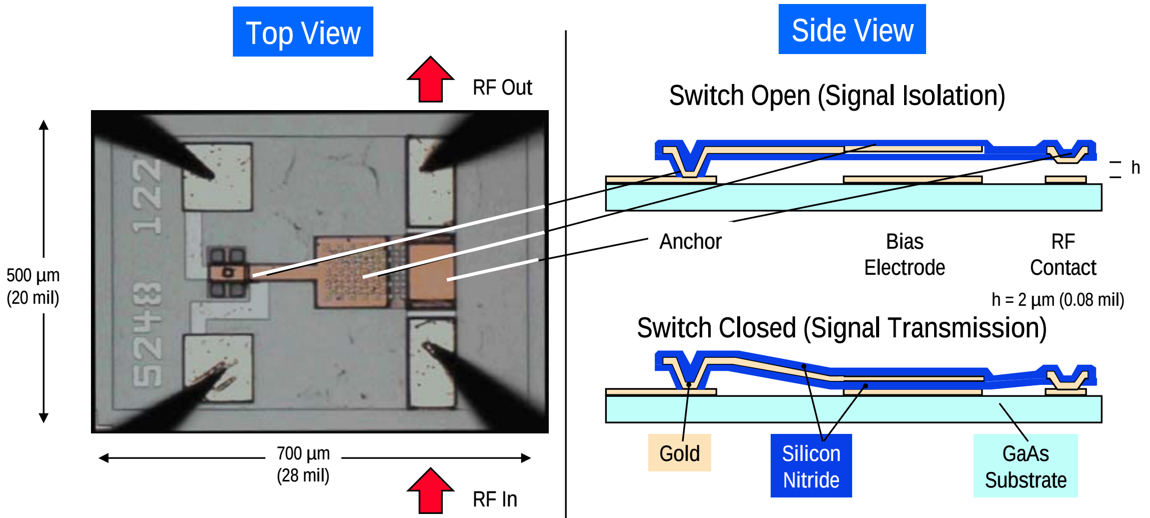
ROCKWELL SCIENTIFIC

HRL LABORATORIES

HRL RF MEMS
Metal-Metal Contact Series Switch

Raytheon

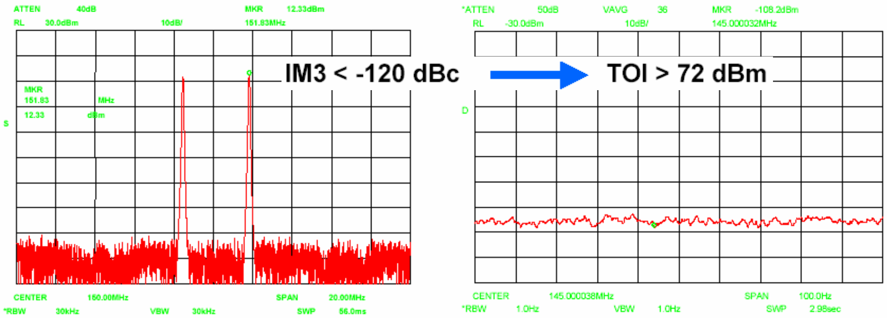


- Electrostatic actuation: 40 V
- Switching time: 20–30 µsec

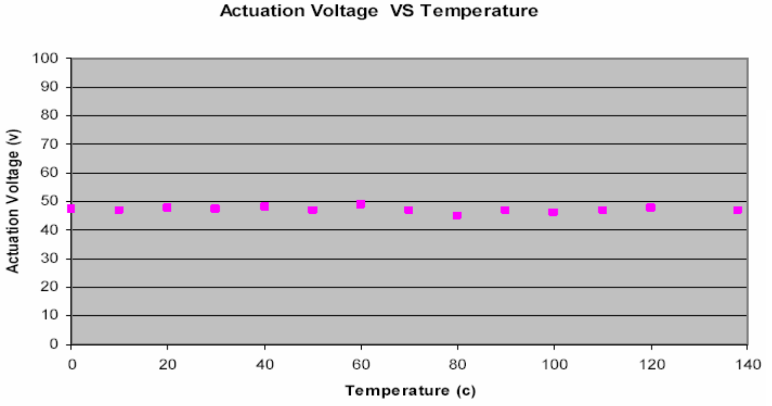
- Nitride/gold/nitride tri-layer prevents creep
- Contact is gold alloy
- Effort has nearly stopped at HRL

HRL Intermodulation and Temperature Effects

Two-tone test: 148.2 MHz and 151.8 MHz

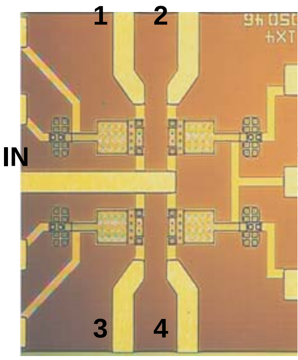


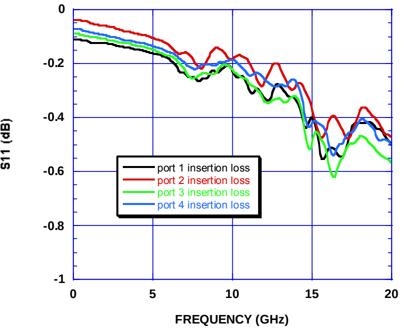
IM3 < -120 dBc → TOI > 72 dBm

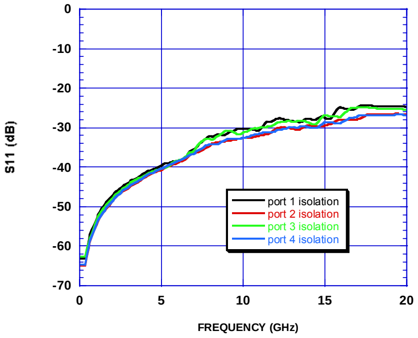


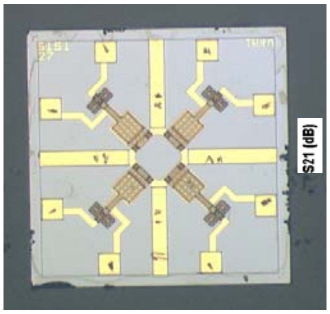
Cantilever design is excellent for thermal stability.

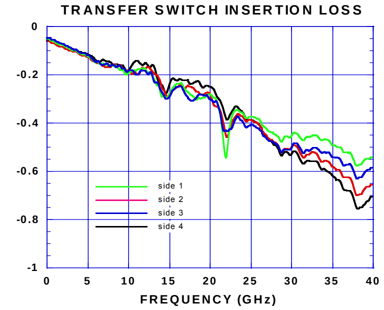
Examples of Switch Networks at DC-20 GHz

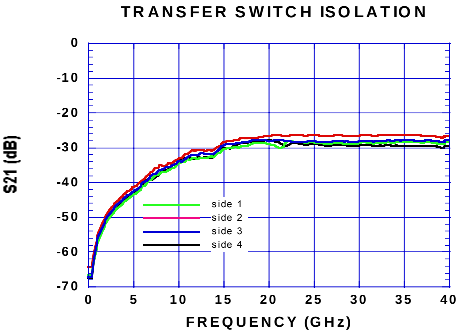










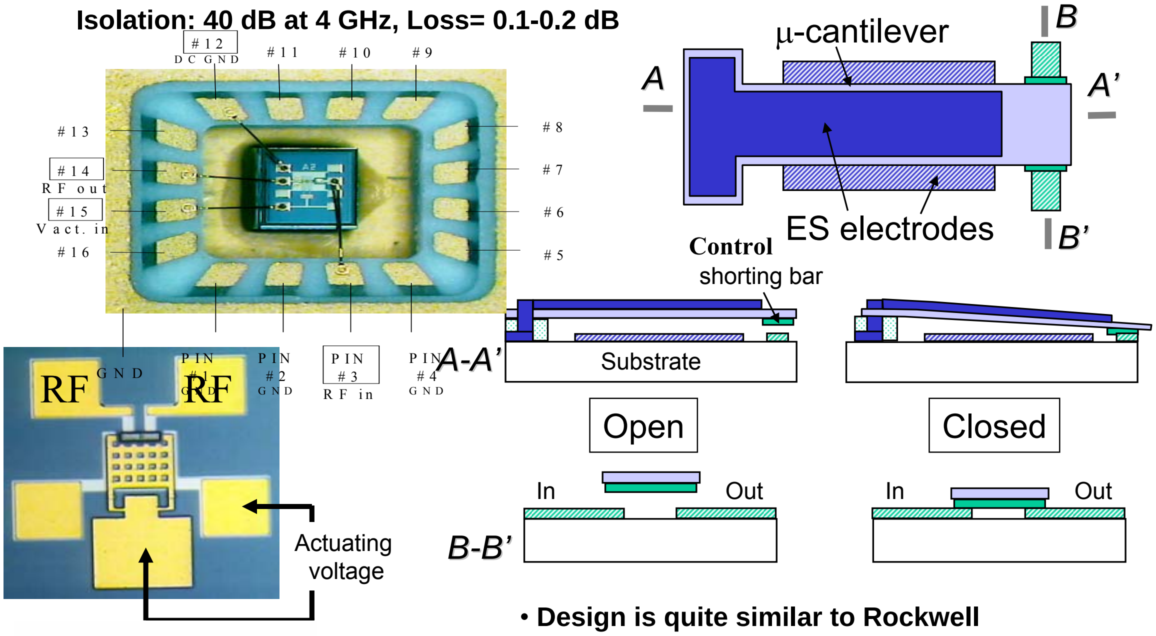


Motorola DC-Contact MEMS Series Switches

Vp = 40-60 V, t = 8 μs

Cu = 3-4 fF, Rs = 1-2 Ω

Isolation: 40 dB at 4 GHz, Loss= 0.1-0.2 dB



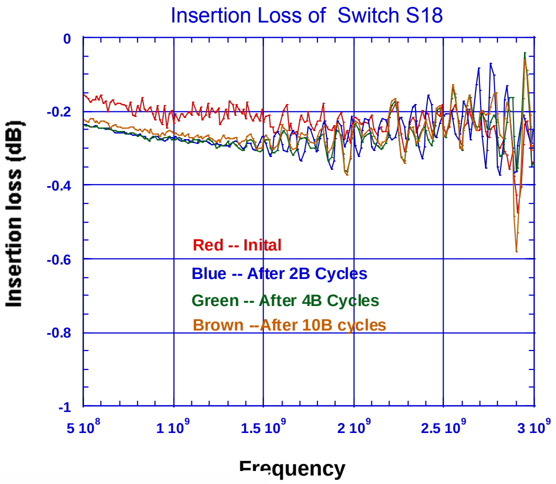
- **Design is quite similar to Rockwell**
- **Effort stopped by Motorola.**

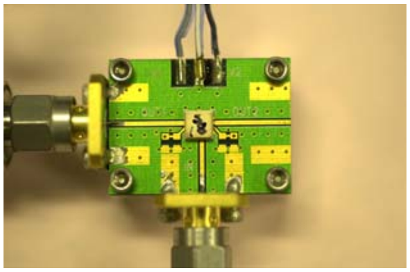
MOTOROLA
Semiconductor Products Sector

Motorola Life Test: > 30 Billion in 2002

- Contact metal is gold alloy
- Tested on 8 switches – Same results
- Package is standard ceramic
- 10-100 mW cold-switching

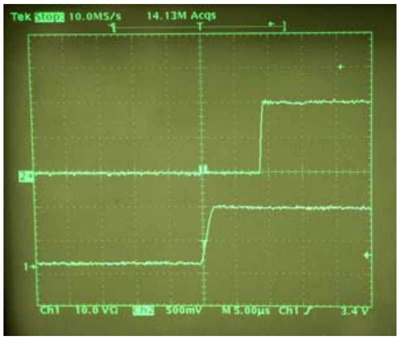
Switch Package on Test Board





Test Fixture

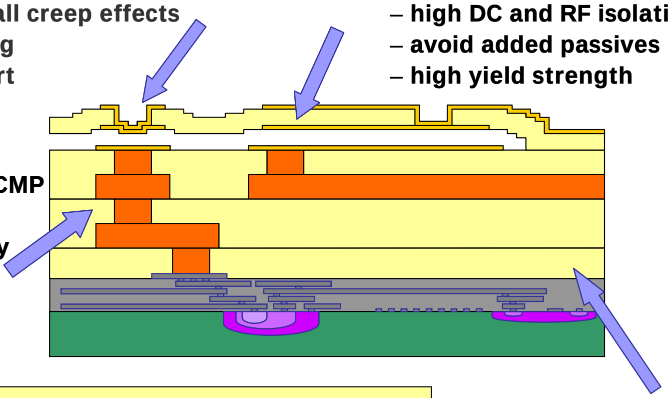
Switching Waveform

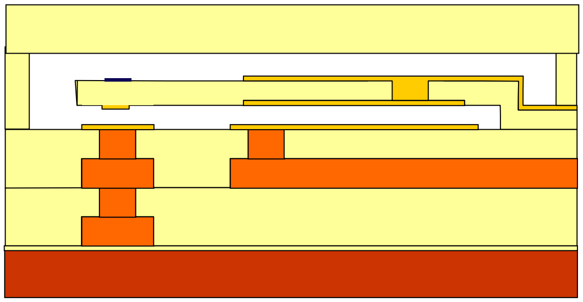


MOTOROLA
Semiconductor Products Sector

WiSpry/Coventor Metal Contact Switch

- Gold-based electrodes and contacts
  - stress balanced, small creep effects
  - no dielectric charging
  - chemically fairly inert
- Silica mechanical material
  - high DC and RF isolation
  - avoid added passives
  - high yield strength
- Thick copper conductors
  - fast deposition and CMP
  - low resistance
  - high current capacity

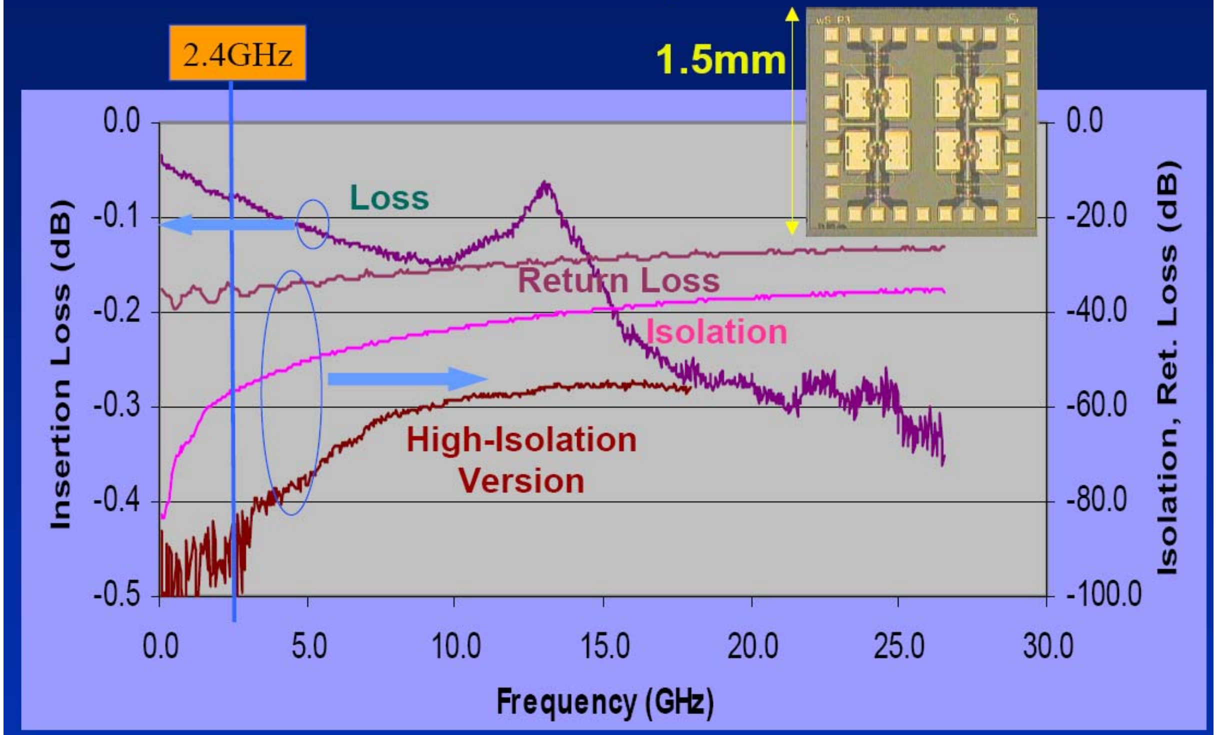




- Thick silica insulators
  - fast deposition and CMP
  - low loss tangent
  - low k -> high impedance
- No information on packaging
  - thin film sealing
  - add 25% to cost model

*wi*Spry

Switch Die S-parameters



Non-deembedded results!

*wi*Spry

17 June 2005

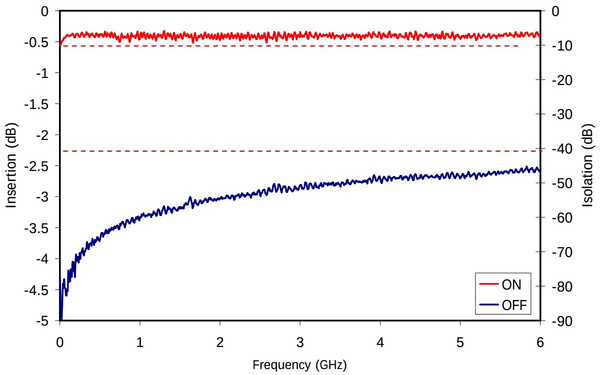
art.morris@wispry.com

Integrated Switch on FEOL Measurement Result

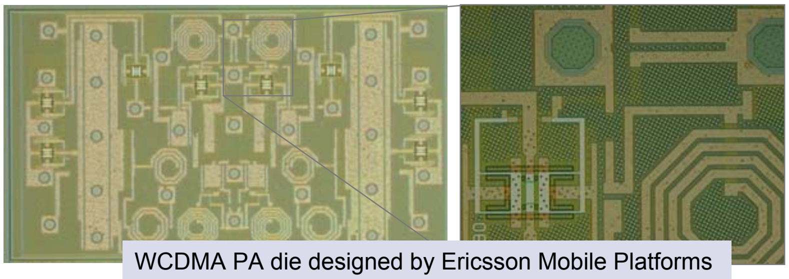
First demonstration of operational MEMS switches fabricated on top of SiGe wafer

A large gap & small contact area result in excellent isolation

Ultimate goal is to show MEMS switching PA output signal from underlying SiGe circuit



Fabricated SiGe Chip with MEMS switches



WCDMA PA die designed by Ericsson Mobile Platforms

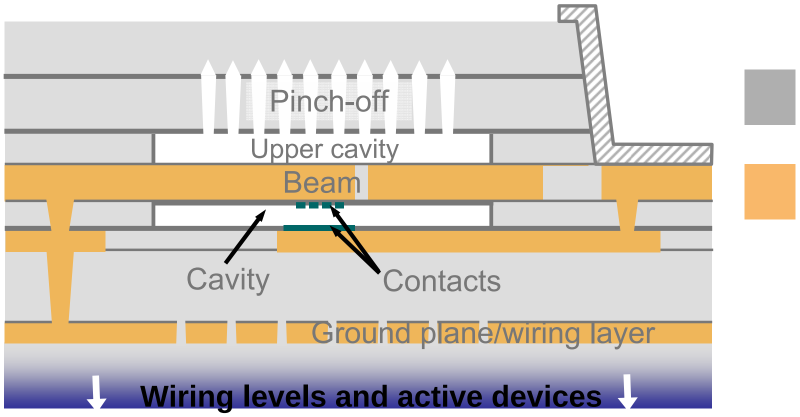
IBM-Integration Approach

MEMS switches and resonators which can be integrated within the wiring levels for SiGe or analog CMOS IC's
- Better performance, smaller size than separate components
- Potential for lower assembled cost as technology matures
- Could enable novel radio architectures requiring many MEMS devices

Devices built in a CMOS manufacturing environment with no new tools

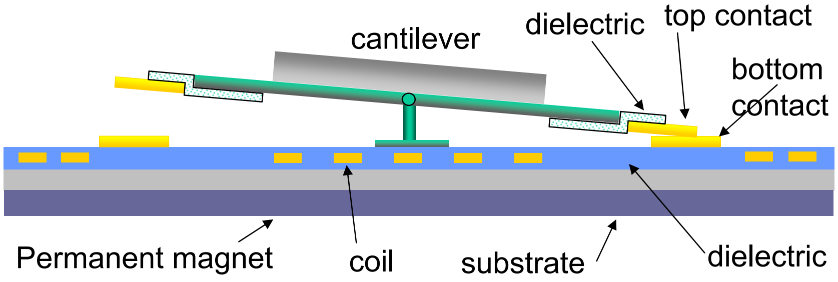
Process flow that allows fabrication of multiple types of devices

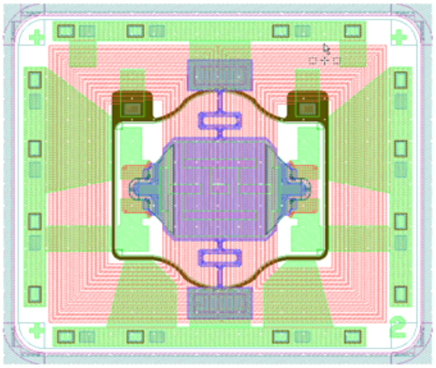
Fully encapsulated devices at wafer level

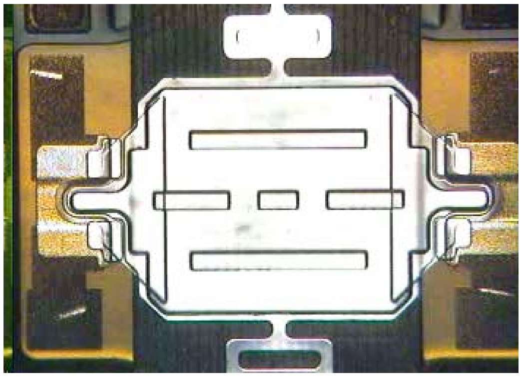


Technology Overview

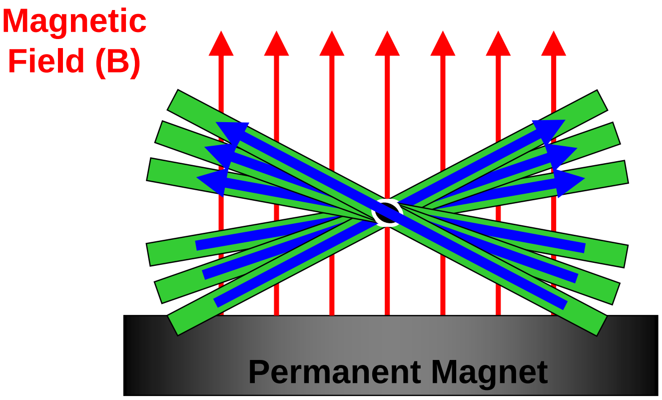
➔SPDT switch







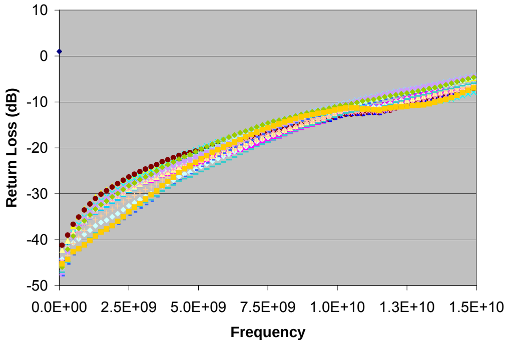
Microlab Magnetic Latching Switch Operation



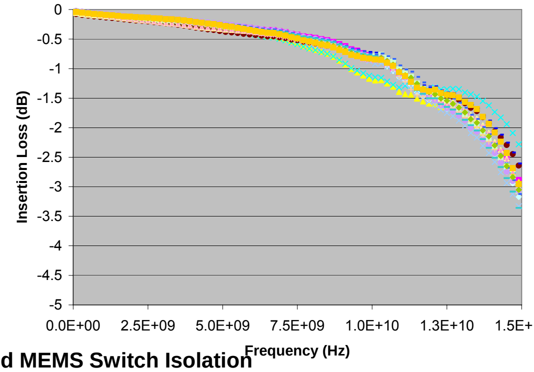
$\tau = m \times B$

- Apply current in loop with CW or CCW direction (100 mA for 100 μs at 3-5 V)
- Magnetic field generated by current changes equilibrium of the switch
- Switch toggles to opposite position
- Remove current. Permagnent magnet holds switch in new position.
- Contact force is dependent on permanent magnet (B). It is around 100-200 uN.
- The higher the permanent magnetic field, the higher the current needed for operation.
- Slow switch due to its weight (15 μm of Nickel is plated for m)
- *This is the only latching switch today available at microwave frequencies.*
- Packaging is done with a standard ceramic substrate with gold-gold eutectic solder.

Packaged MEMS Switch Return Loss
5 Parts, 10 contacts tested
Probed directly on 5mm package

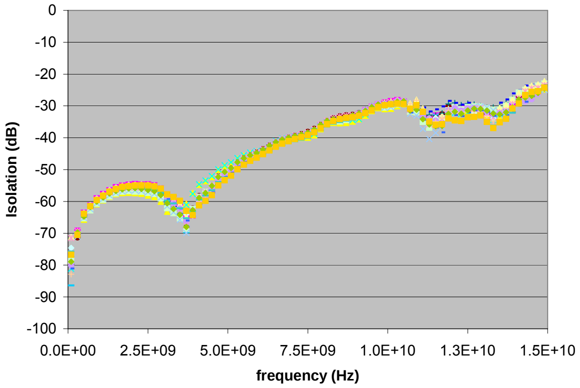


Packaged MEMS Switch Insertion Loss
5 Parts, 10 contacts tested
Probed directly on 5mm package



9/30/03
CBW/JBT

Packaged MEMS Switch Isolation
5 Parts, 10 contacts tested
Probed directly on 5mm package



9/30/03
CBW/JBT

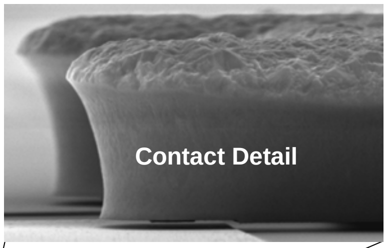
Reliability guaranteed to 10M cycles, hot or cold switched, at 10 mA, 10 V. Gold-based contacts.

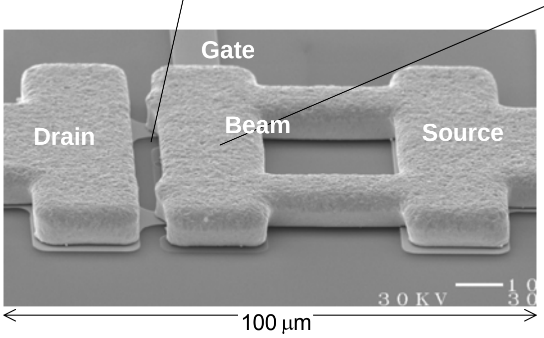
Available for purchase.

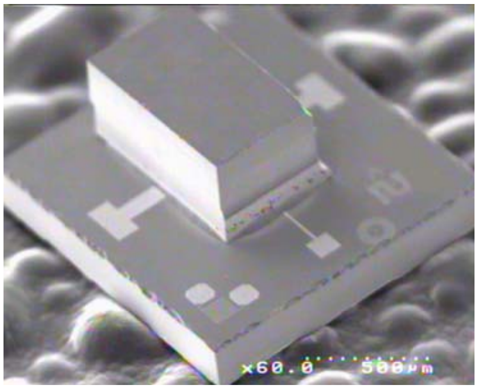
Magfusion

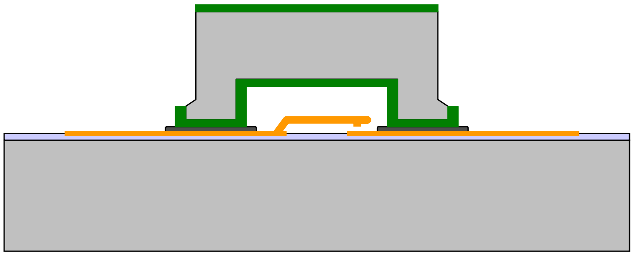
RMI MEMS RF Switch (Radant MEMS)

RADANT MEMS



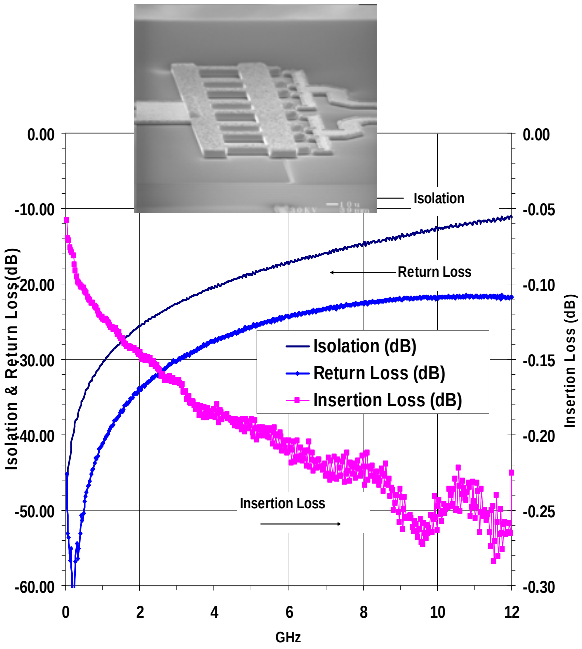


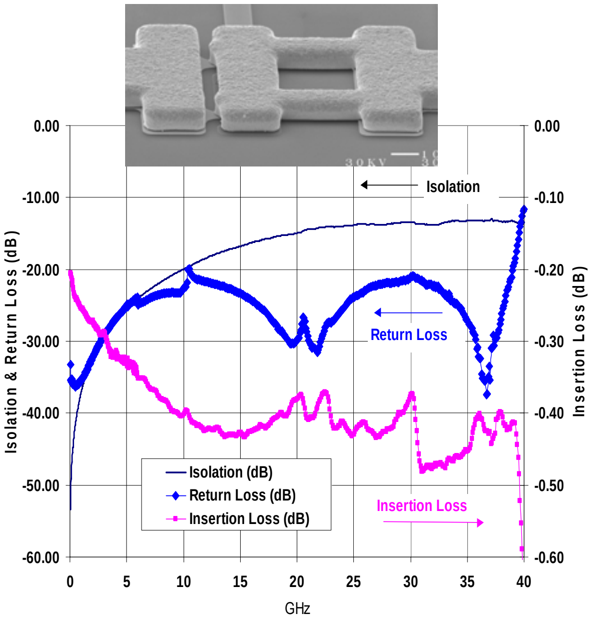




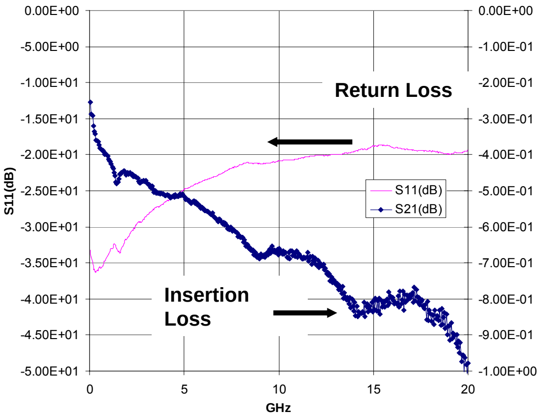
- Glass to glass hermetic sealing.
- Wafer scale on silicon, 400-450C.
- High yield.

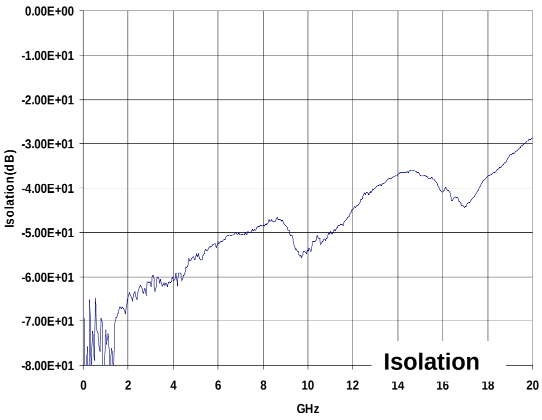
Measured RF Performance
2- and 8 Contact Switch - Wafer Capped



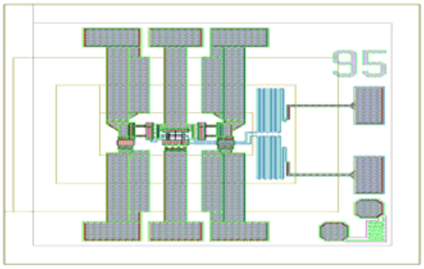


CPW Series-Shunt Switch based on the Radant MEMS



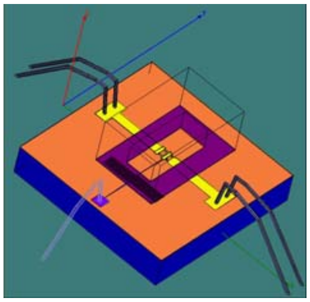


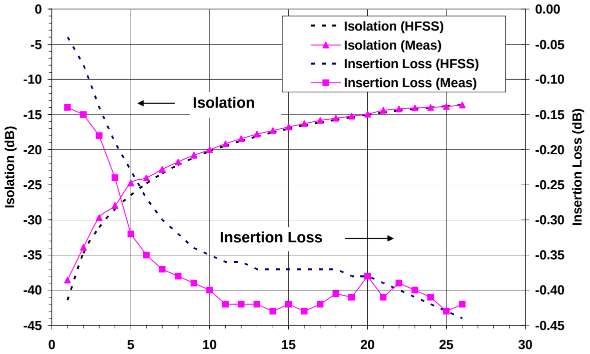
- Very Good Isolation: 50 dB at 10 GHz, 30 dB at 20 GHz.
- >100 mW power carrying capability



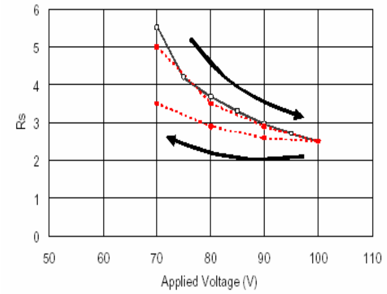
Modeling and Measured Switch Resistance

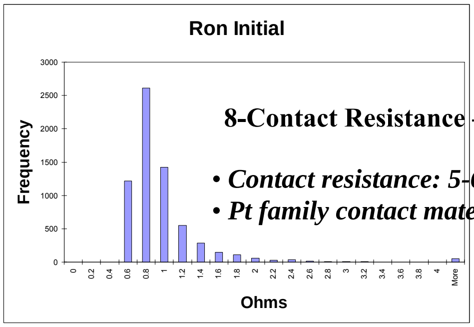
ANSOFT HFSS





4-Contact Resistance vs. Voltage

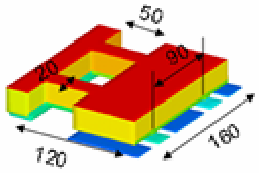




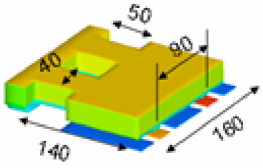
8-Contact Resistance – Wafer Scale

- *Contact resistance: 5-6 Ω per contact !*
- *Pt family contact material (not disclosed)*

Mechanical simulations done using Coventorware (UoM Switch)

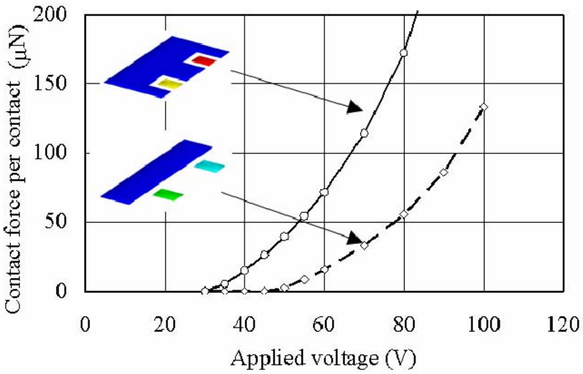


SW1



SW2

		SW1	SW2	
Pull-in Voltage	V	30-35	35-40	
Collapse Voltage	V	>100	>100	
Contact Force	uN	40-70	50-90	Vs=50-60 V per contact
Restoring Force	uN	60	70	Per switch
Switching Time	us	5-7	4-7	Vs=60 V
Release time	us	17	16	1/f0: f0 resonant freq

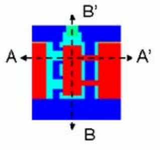


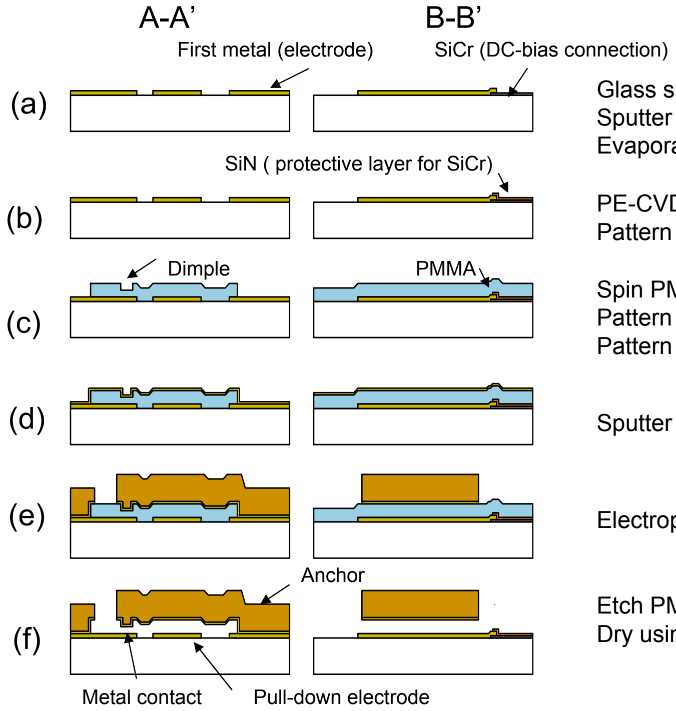
Electrostatic-mechanical coupled FEM analysis to investigate pull-down voltage and corresponding force.

Reduced voltage by 30 V for same force!

The University of Michigan

Fabrication process at UoM





(a) Glass substrate (pyrex® 7740)
Sputter SiCr layer ->Lift-off
Evaporate First metal layer (Ti/Au/Ti) ->Lift-off

(b) PE-CVD Si3N4
Pattern it using RIE

(c) Spin PMMA
Pattern cantilever gap using RIE
Pattern dimple using RIE

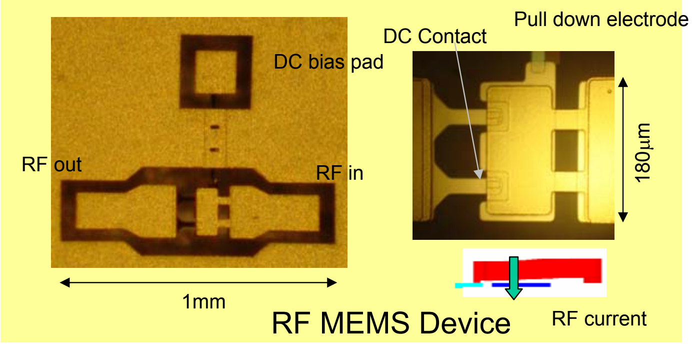
(d) Sputter seed layer for electroplating (Au/Ti)

(e) Electroplate the cantilever (Au)

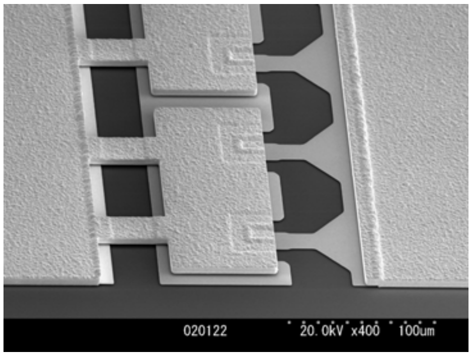
(f) Etch PMMA (release a cantilever)
Dry using a critical point drying

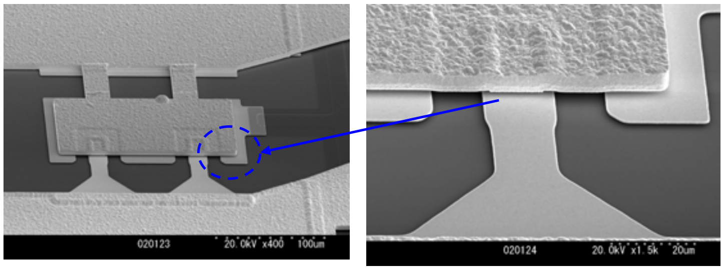
-Need 6 Masks
-SiCr can be replaced by any high resistivity metal, compatible with high volume manufacturing.

RF MEMS Series Switch for DC-40 GHz



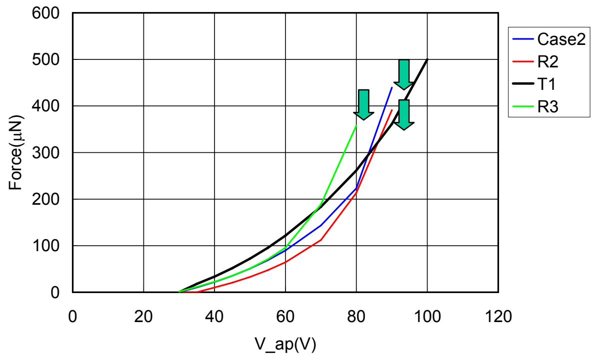
RF MEMS Device





SEM pictures of metal-contact switch

Contact Force vs Applied voltage



-Case R3 has a higher contact force than Case R2, but the switch collapse at lower voltage. This is because the length between the anchor and the contact dimples is long and the switch bends along this line.(please see fig.4)

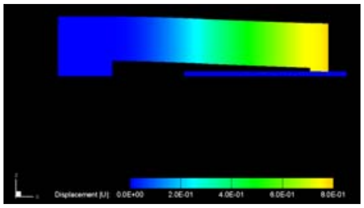


Fig.2 :Displacement at 60V for case R2

The gap is small, and strongly contributes to contact force.

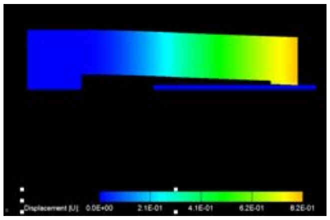


Fig.2 :Displacement at 60V for case 2 – THIS IS OUR SWITCH

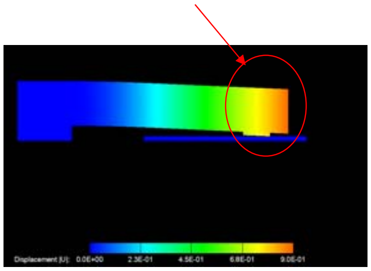


Fig.3 :Displacement at 60V for Case T1 (coloring are the same as case 2)

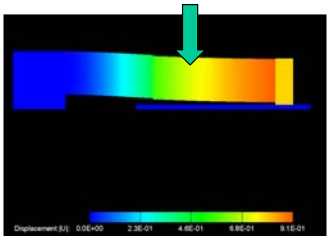
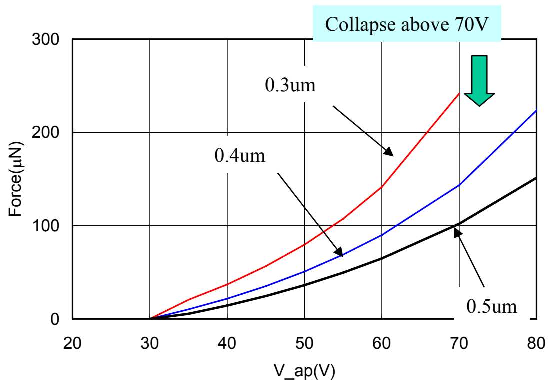
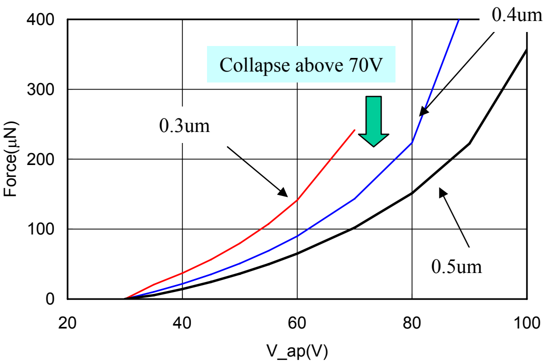


Fig.4 :Displacement at 80V for Case R3 (coloring are the same as case 2)

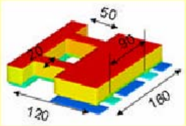


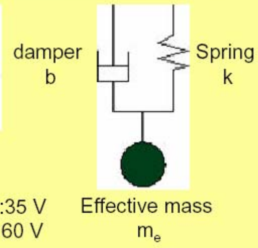


(Only plot ranges are different)

Case 2 contact force vs. dimple thickness

Modeling of Switching time





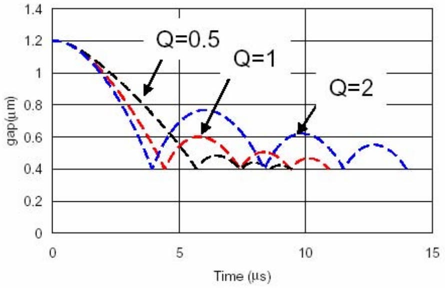
Gap:1.2 um
Dimple:0.4 um
Pull down voltage:35 V
Actuation voltage:60 V

Switch configuration and 1D model

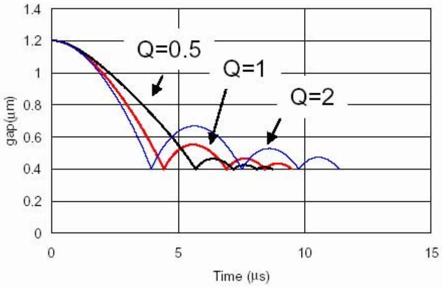
k_effective=131N/m (from mathematica model)
k=64N/m (coventorware)
m_e=4.79E-10 kg =38% of actual mass (coventorware)
$\omega_0=2\pi x 58x10^3$ rad/s (coventorware)

$$m_e \frac{d^2 x}{dt} + b\frac{dx}{dt} + k\left(g_0 - x\right) = \boxed{\frac{k}{k_{effective}}} F_e$$

Model equation



No energy dissipation at bouncing



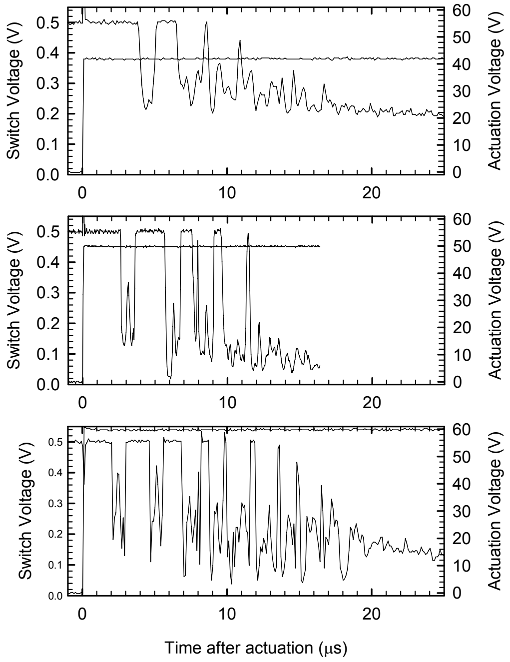
25% of kinetic energy dissipated at each bouncing

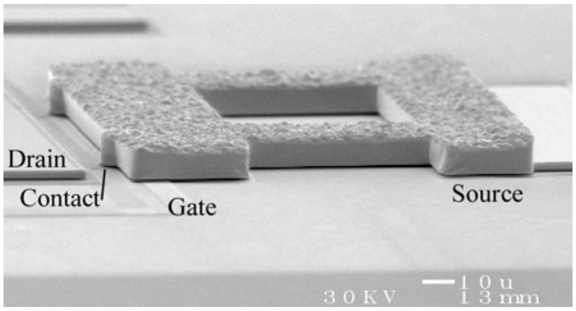
Simulation results

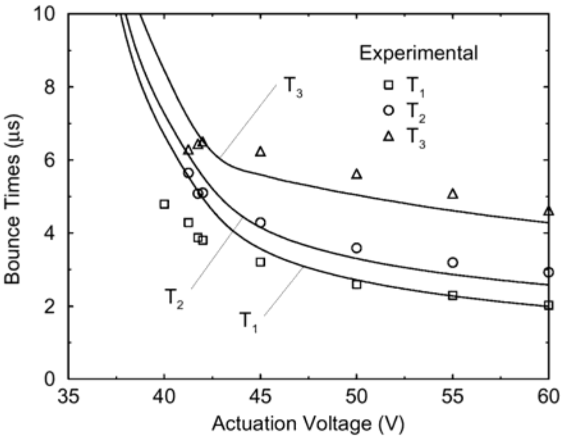
- -Switching time is calculated based on a non-linear 1D kinetic model.
- -Some modification was added to account for the cantilever deformation. (indicated by a blue circle)
- -Mechanical Q is assumed to be independent of gap displacement.
- -Lower Q results in small bouncing.

Mathematica Modeling

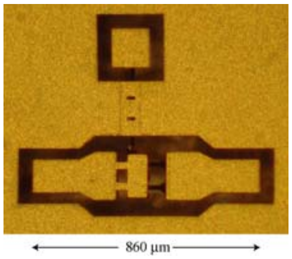
Bounce of Radant/ADI Switch (from Prof. McGruer, NEU)



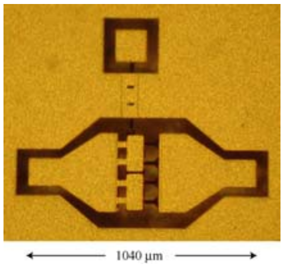




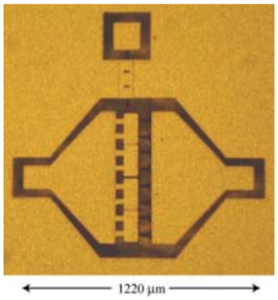
Measurements of DC-contact switches on Quartz (UoM)



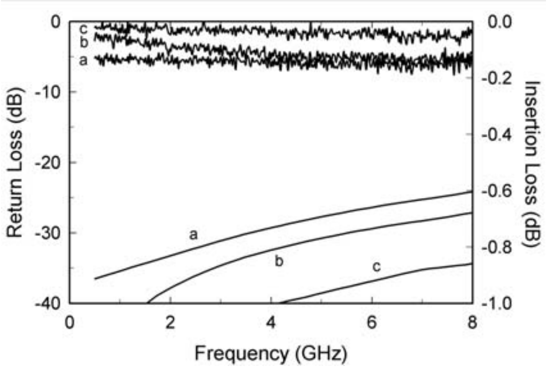
(a)

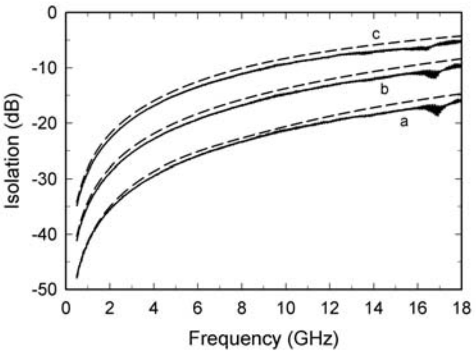


(b)



(c)





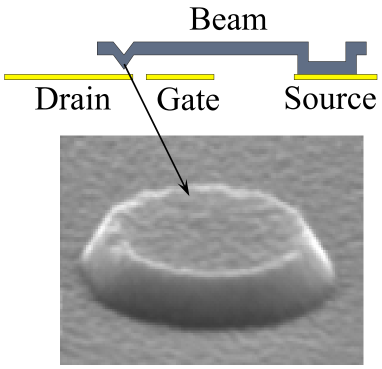
Simulations vs. measurements

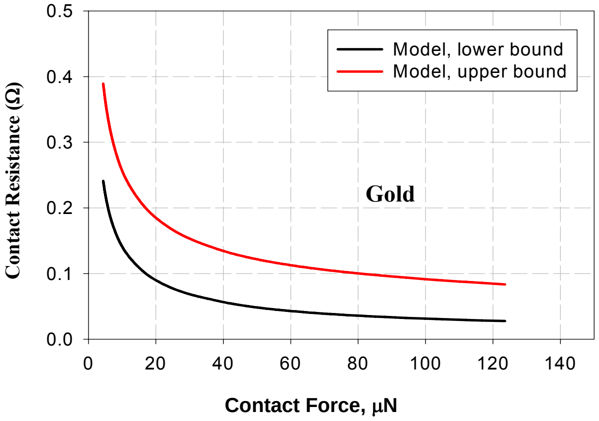
Case2 (Design#1) on Glass and Design 2 on Silicon

	Glass substrate ($\varepsilon_r = 4.6$)		Fitted/meas results on glass	Si substrate ($\varepsilon_r = 11.9$)		Fitted/meas results on Si
gap height *at contacts*	0.8 um designed	1.3 um achieved		0.8 um designed	1.3 um achieved	
2 contacts	17.6	14.6	13	27.5	23.5	18.5
4 contacts	38.2	32.1	28	60.7	52.6	44.4
8 contacts	76.7	64.7	65.6	125.1	109.4	93.3

Dimple size: 15x10 um^2. gap = 10 um

Reliability of Metal-Contact Switches: It is the contact!





- **For a single, circular contact spot:**

$$R = \frac{\rho}{2a}$$

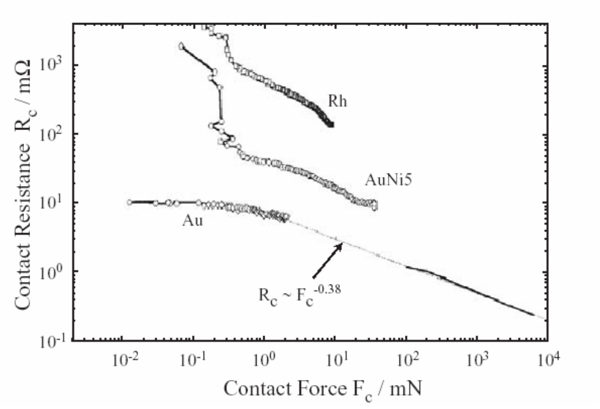
ρ: electrical resistivity
a: contact radius

F= H*A (hardness*contact area)

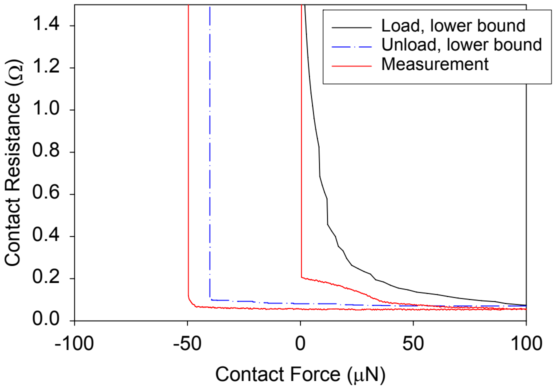
- **The contact surface is rough, which results in multiple (5~20) contact spots.**
  - **lower bound if contact spots are far apart, conduct independently**
  - **upper bound if spots are merged into a single large spot.**

From Prof. Nick McGruer, NEU

Contact Resistance vs. Contact Force



Adhesion force responsible for – 50 μN



$$F + 2\pi\gamma R = \pi r^2 H$$

- In general, the more the contact force, the more reliable is the switch.
- Electrostatic actuation does not result in high contact force (50-200 μN)
- Gold results in very low resistance, but is soft and sticks easily.
- Gold alloy is the most used material (except Radant MEMS).

Basic Thermal Properties of Contacts

Assumption:

The electrical and thermal currents flow in the same paths.

Wiedemann-Franz Law:

$$\rho\lambda = LT$$

T: Temperature, K
ρ: Electrical Resistivity, Ω m
λ: Thermal Conductivity, W/(m K)
L: 2.4*10^{-8} $(V/K)^2$

Voltage - Temperature Relation in metallic constriction:

$$T_\Theta^2 - T_0^2 = V^2/(4L)$$

T_Θ: Maximum temperature in constriction, K
T_0: Bulk temperature, 300K
V: Voltage across constriction, V
L: 2.4*10^{-8} $(V/K)^2$

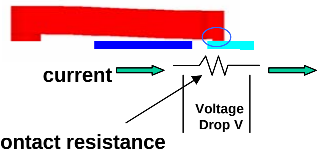
The maximum temperature in a metallic constriction is nearly independent of geometry and material.

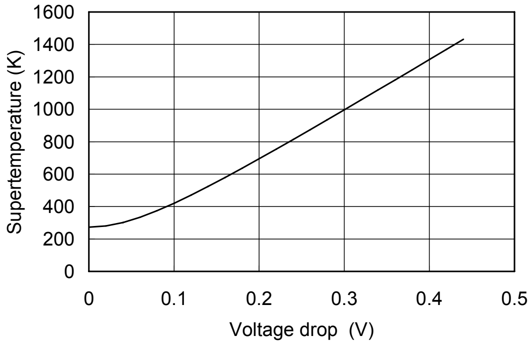
Nick McGruer, NEU

Simple calculation of Supertemperature

$$Ts = \sqrt{\frac{V^2}{4L} + T_0^2}$$

$$L: Lorenz\ number = 2.45 \times 10^{-8}\ (W \cdot \Omega / K^2)$$





Supertemperature in the contact: Independent of contact material

	Resistance per contact (Ohm)			
Current (A)	0.5	1	1.5	2
0.01	0.005	0.010	0.015	0.020
0.03	0.015	0.030	0.045	0.060
0.05	0.025	0.050	0.075	0.100
0.1	0.050	0.100	0.150	0.200
0.2	0.100	0.200	0.300	0.400
0.4	0.200	0.400	0.600	0.800

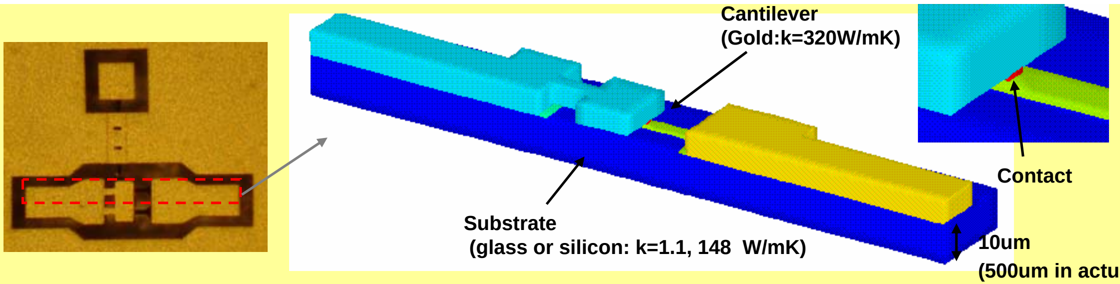
▨ **Ts (increase from ambient) < 100C**

Voltage drop as a function of contact resistance and current

-Supertemperature is the maximum temperature defined on the microscopic scale around contacts.
-Assume that the increase of Ts < 100 C is necessary for reliable contact, current should be limited to 0.03-0.1 A depending on the contact resistance.

Aug.20.2003

Thermal simulation using FEM – Model on Silicon substrates (Coventorware)

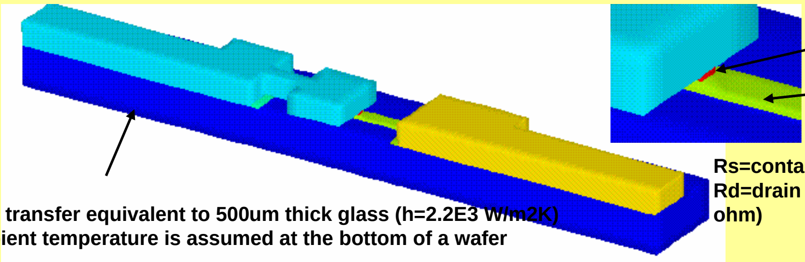

Cantilever
(Gold:k=320W/mK)

Contact

Substrate
(glass or silicon: k=1.1, 148 W/mK)

10um
(500um in actual)

Simulation model


Heat generation =I^2Rs W

Heat generation =I^2Rd W

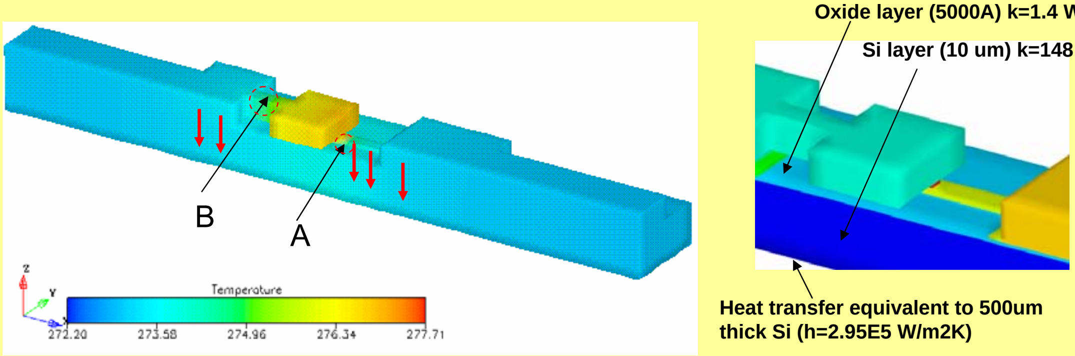
Rs=contact resistance
Rd=drain electrode resistance(=0.11 ohm)

Heat transfer equivalent to 500um thick glass (h=2.2E3 W/m2K)
Ambient temperature is assumed at the bottom of a wafer

Boundary condition

FEM simulation is performed to investigate the thermal dissipation path on the wafer level
Dimple is touched to drain electrode in advance, no mechanical deflection is simulated.
Joule heating is not directly simulated, but taken into account by placing heat generation around contacts
Thermal conductivity is assumed to be constant.

Thermal simulation using FEM – Silicon substrate (Coventorware)



Oxide layer (5000A) k=1.4 W/mK

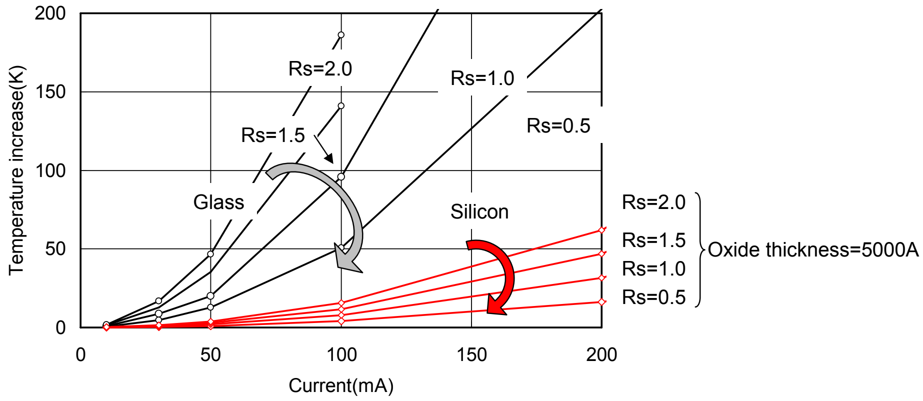
Si layer (10 um) k=148 W/mK

Heat transfer equivalent to 500um thick Si (h=2.95E5 W/m2K)

Temperature distribution (Rs=0.5ohm, I=0.1A,Total heat =6.6mW)

-The maximum temperature is obtained in a cantilever, but fairly low compared with that of glass substrate.
-There are two thermal resistance where temperature change occur, but there are quite small: A: Drain electrode near the contact, B: Cantilever beam
-Because thermal conductivity of silicon is >100 times larger than that of glass, heat is easily dissipated to the bottom of the substrate.

Thermal simulation using FEM – Maximum temp vs. current, contact resistance



Maximum temperature for various Rs and I

-In the case of silicon substrate, temperature increase on the wafer level is very small, however supertemperature which is defined on the microscopic scale around contacts is as high as in the case of glass.

-In the case of glass substrate, temperature increase is less than 50K, if we limit current within 50mA per a contact.

-**Because temperature is proportional to I^2 and Rs, Reducing current per each contact (increase the number of contact) is better than reducing Rs.**

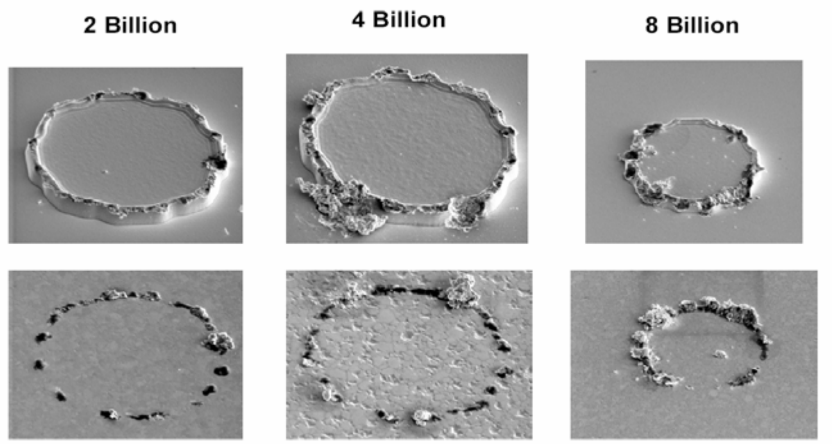
Which metal to use?

Au-Alloy

Material	Density (g/cm3)	Melting Range (C)	Resistivity at 20 (C) uohm cm	Temp coeff elec resistance	Thermal cond (W/mK)	Young's Modulus (Gpa)	Hardness (10^2 N/mm2)
Au	19.3	1063	2.19	4	297	80	2-7
AuAg(8)	18.1	1060	6.1			82	
AuAg(10)	17.8	1058	6.3	1.25	147	82	4-8.5
AuAg(20)	16.4	1036-1040	10	0.86	75	89	4-9.5
AuAg(30)	15.4	1025-1030	10.2	0.7			4.5-9.5
AuNi(5)	18.3	995-1010	13.3	0.71	52	83	11.5-16
AuCo(5)	18.2	1010	5.2-55.5	0.68		88	9.5-16
AuPt(10)	19.5	1150-1190	12.2	0.98	54	95	8-10
AuAg(25)Cu(5)	15.2	980	12.2	0.75			9-16
AuAg(20)Cu(10)	15.1	856-895	13.7	0.52	66	87	12-19
AuAg(26)Ni(3)	15.4	990-1020	11.4	0.88	59	114	9-14
AuAg(25)Pt(6)	16.1	1060	15.9	0.54	46	93	6-11
AuCu(14)Pt(9)Ag(4)	16	955	14.3-25				19-27

We are working on gold alloys since we only need billion cycle operation

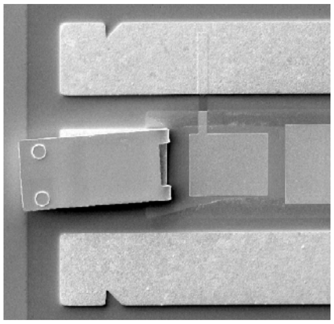
Switch Contact Pairs

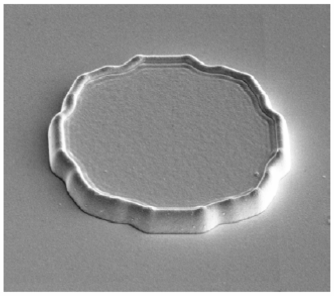


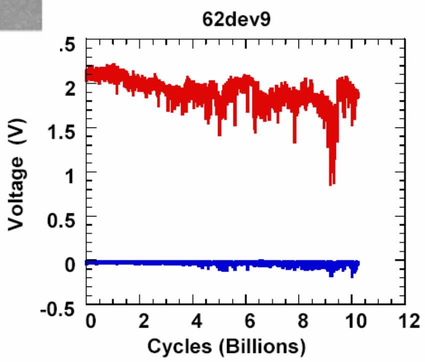
Switch is working even if it looks ugly.

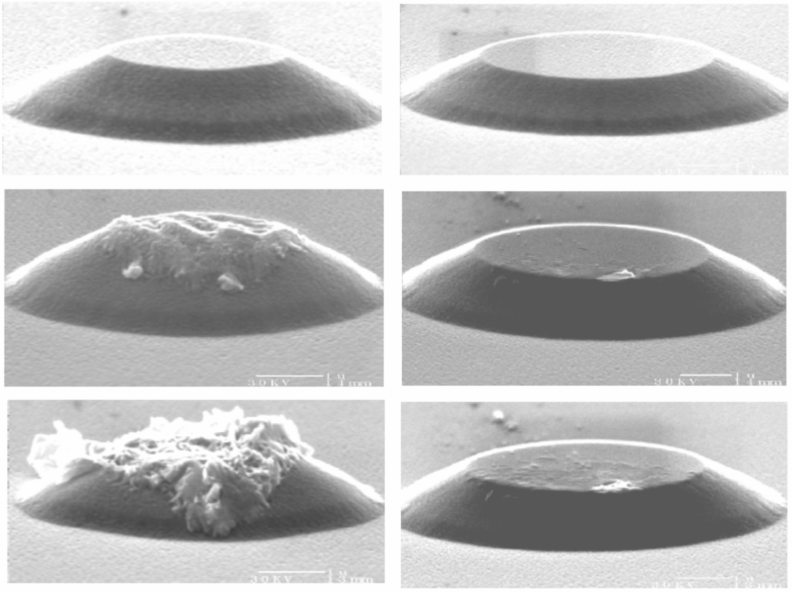
Ti/Au 3000 A on bottom. 1000 A suputtered Au, then 5 um plated Au on top.

AFRL/Dayton Work









No Cycles

10,000 Cycles

1,000,000 Cycles

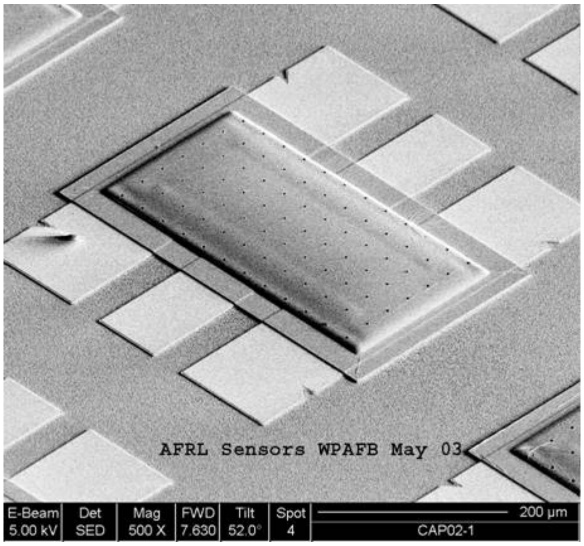
Au Contact, 200 µN, 2 µm Diameter, 1 µm thick, ~60 MPa.

Au Contact, 200 µN, 5 µm Diameter, 1 µm thick, ~10 MPa.

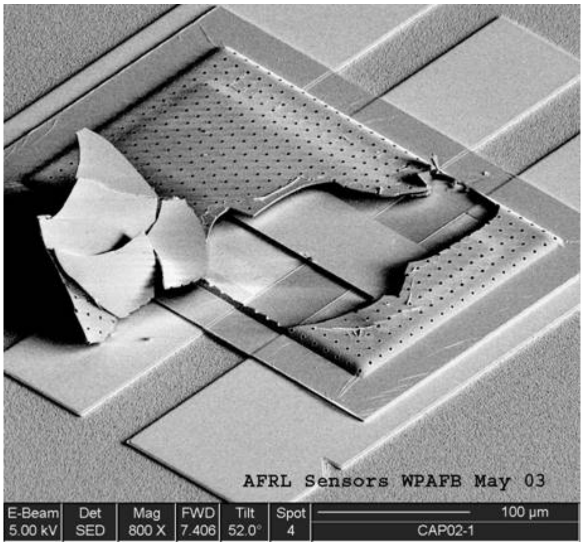
Conclusions on Reliability of Metal-Contacts

- Under ideal conditions (gold) microswitch contacts achieve predicted metal-metal contact resistance.
- Adhesion can be a large fraction of the actuation force.
- *Thermal effects* limit the maximum switch current.
- Switch can work even if the contacts look bad.
- More work is needed on models and verification, particularly on contaminant/protective films, material transfer and electromigration.
- This is an area of active research. I call it Voodoo science.
- The ADI/Radant switch can handle > 2 W at 10 GHz for > 2 Billion cycles.

Silicon Nitride Encapsulated Switches



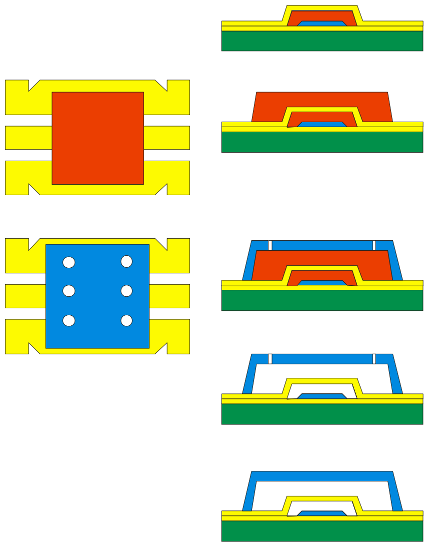
Released switch under nitride cap



Nitride cap partially removed showing released switch

Capping Layer Process Flow

Mask Layout **Side View** **Process Step**



Unreleased switch wafer

Deposit 2nd sacrificial layer
PMGI, 3.0 µm

Deposit dielectric capping layer
Sputtered Si_3N_4, 1.7 µm

Release switches through access holes
Wet release, Supercritical CO_2 dry

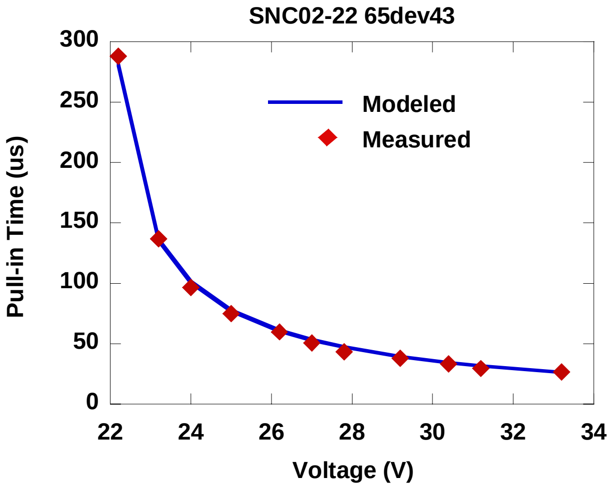
Seal access holes
PECVD SiO_2, 2.0 µm, 300°C

ITAR (2005)

1-D Dynamic Model

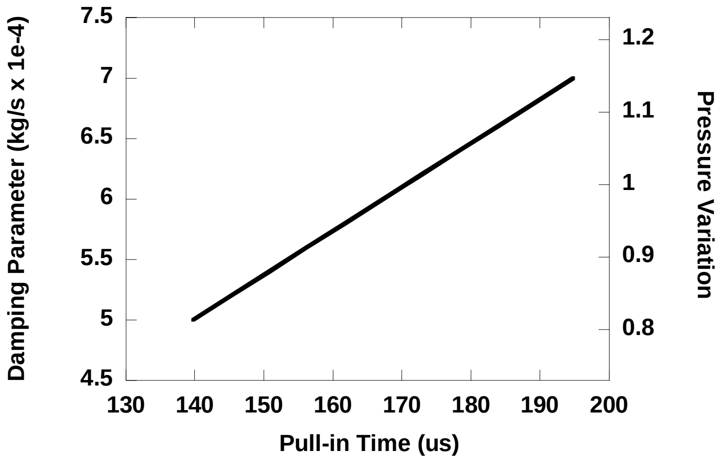
$$\frac{d^2x}{dt^2} = \left(\frac{k(x_0 - x)}{m}\right) - \left(\frac{\varepsilon_0 A V^2}{2mx^2}\right) - \left(\frac{b}{m}\frac{dx}{dt}\right)$$

Spring Force **Electrostatic Force** **Damping**



Model Parameters
b = 6.1e-4 Kg/s
k = 33.8 N/m
x_0 = 1.5 um
m = 1.5e-10 kg
A = 6.4e-9 m^2

Modeled Pull-in time Variation

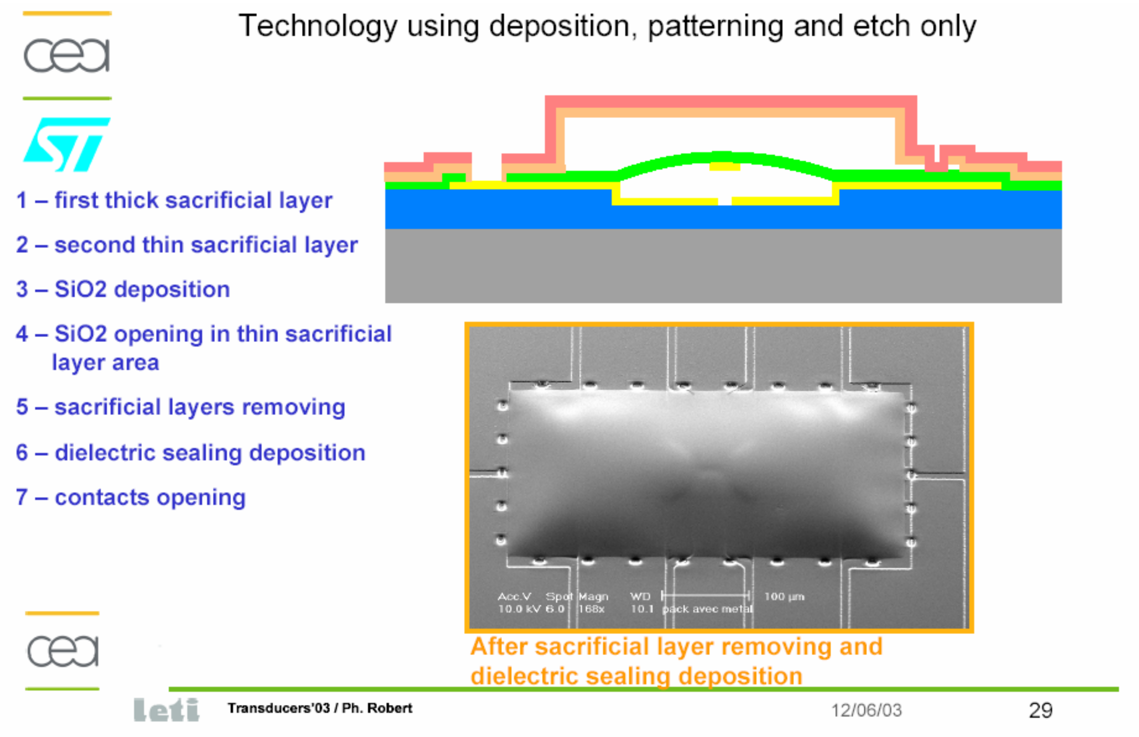


Damping coefficient , b, varied in model to establish pull-in time variation

b is linearly related to absolute pressure

Pull-in time measurement can easily detect < 3μs variation

Correlates to < 2% absolute pressure variation



Technology using deposition, patterning and etch only

1 – first thick sacrificial layer

2 – second thin sacrificial layer

3 – SiO2 deposition

4 – SiO2 opening in thin sacrificial layer area

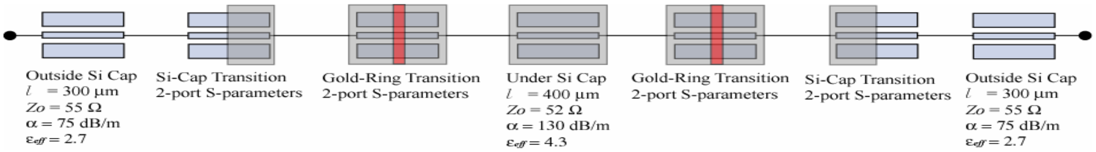
5 – sacrificial layers removing

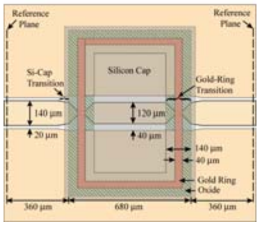
6 – dielectric sealing deposition

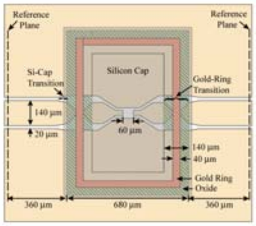
7 – contacts opening

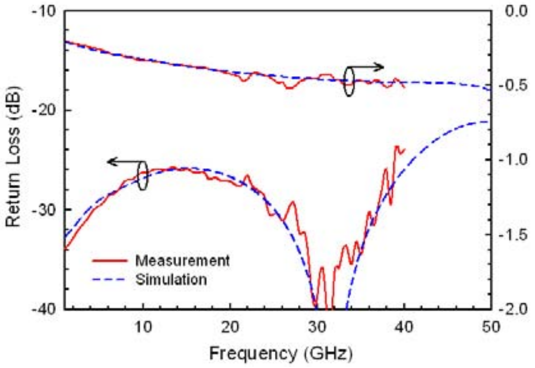
After sacrificial layer removing and dielectric sealing deposition

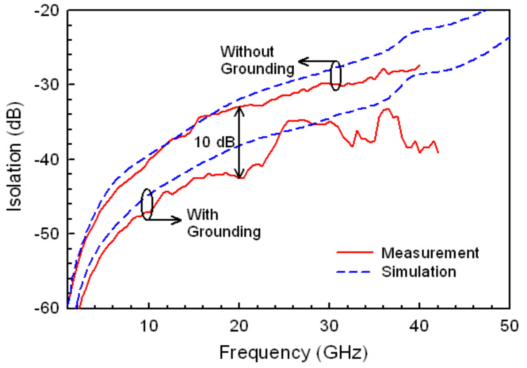
Packaged CPW Line



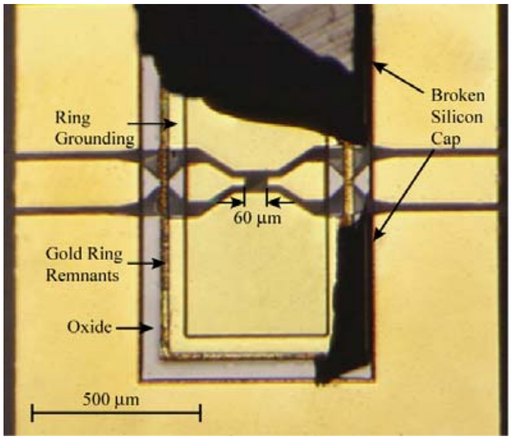


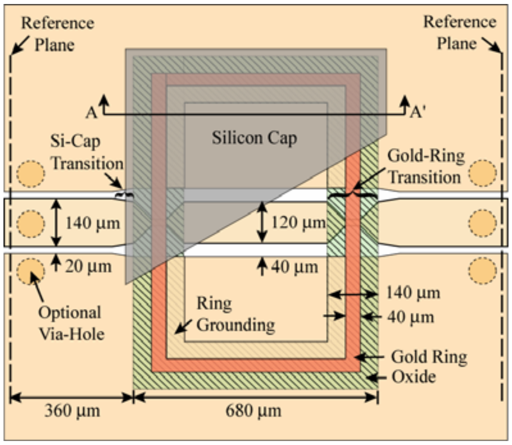




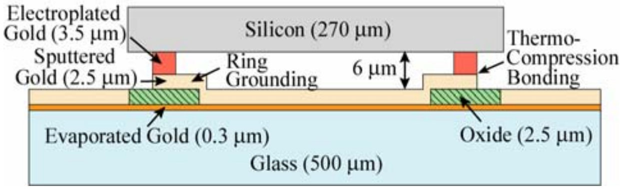


DC-50 GHz Wafer-Scale Package: UoM





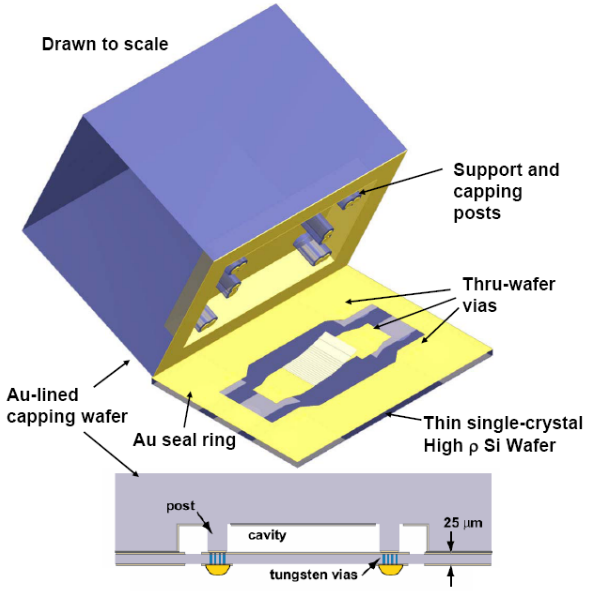
- CPW line on glass wafer.
- Silicon cap wafer (1000 Ω-cm).
- Oxide interlayer.
- Gold-to-gold thermo-compresssion
- Bonding (360°C, 200 N, 30 min)



Package Requirements

- Mechanical protection and hermetic environment
- Very low-loss and wide-band electrical interconnects
- Verification of package environment
- Wafer-scale and potentially low-cost manufacturing process
- Compact size and ease of integration to other technologies

Conceptual Illustration



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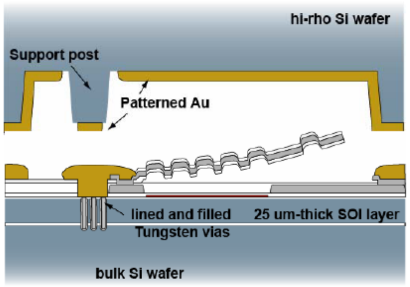
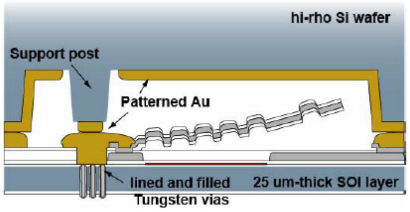
Fabrication Overview

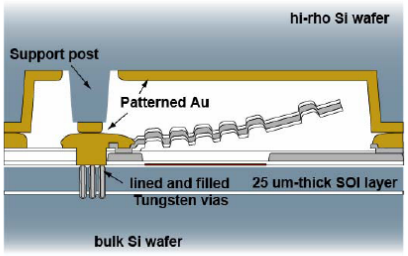
Device & Cavity Wafer Fabrication



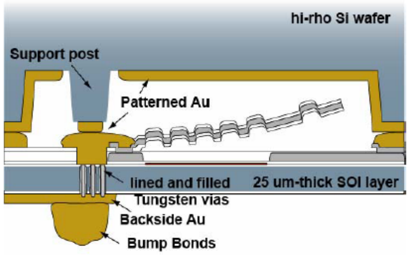
Wafer Lapping and Wet Thinning



Au Thermo-compression Bonding



Backside Metal and Bump Bonds



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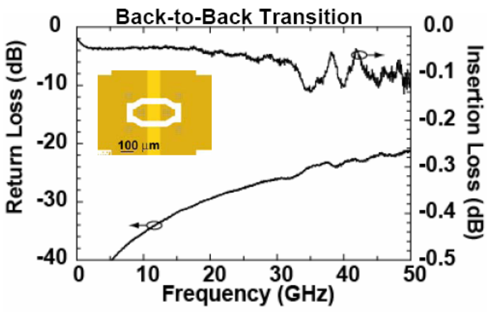
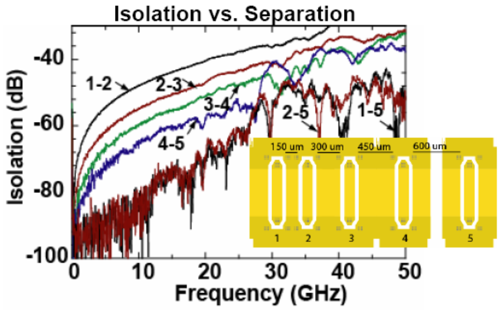
RF Package Measurement Results

- Package insertion loss < 0.06 dB @ 20 GHz, less than 0.025 dB per transition
- Package return loss less than –30 dB @ 20 GHz, well matched transitions
- Line attenuation is 0.92 dB/cm @ 40 GHz (with only 1 micron Au on transmission lines)
- Isolation below – 80 dB @ 10 GHz (near noise floor of the system) for >750 micron separation

100% Yield on First Die Tested





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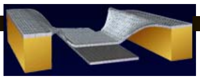
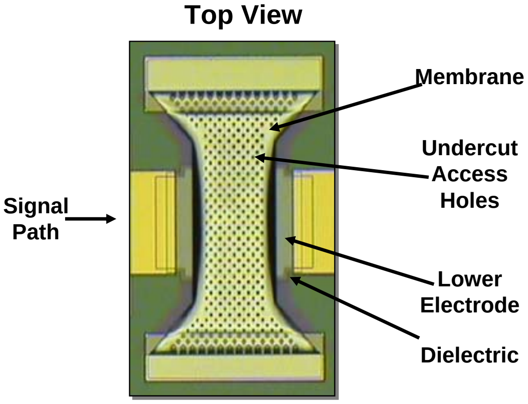
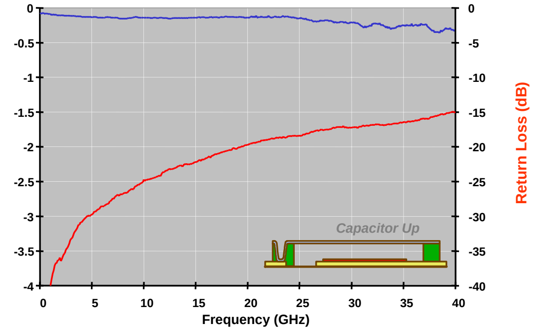
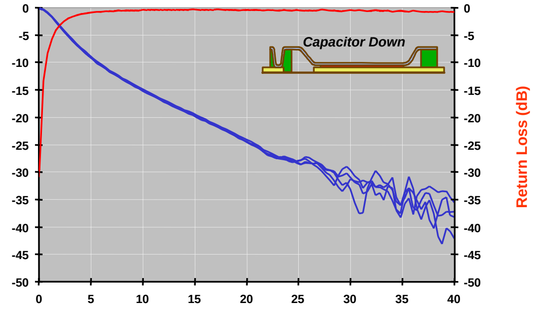


Capacitive Membrane Switches

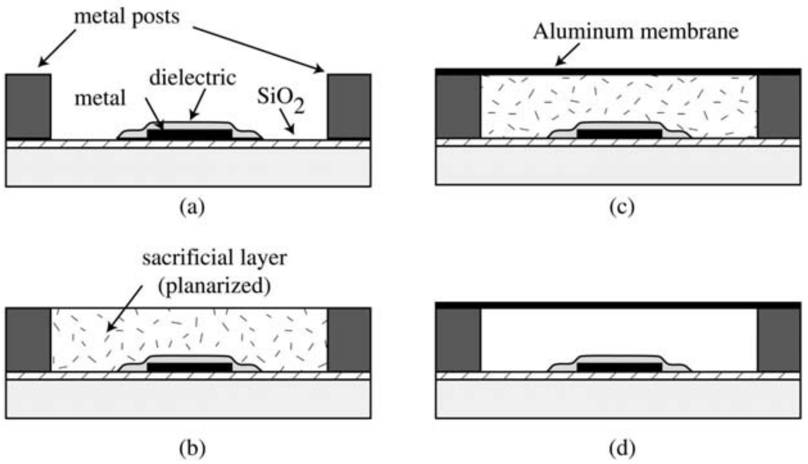


•Capacitance Ratio	70-110	
•Cu=35 fF, Cd=2.8-3.5 pF		
•Cutoff Frequency	18,000	GHz
•Switching Speed	< 10	µs
•Intercept Point	> +66	dBm
•Switching Voltage	30-40	volts
•Size	280 × 170	µm



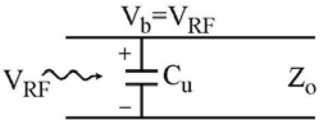


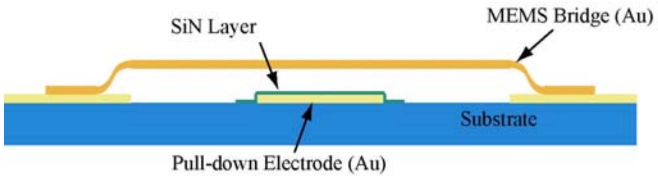
Fabrication of Capacitive Membrane Switches



- Very easy to fabricate. Has been the most used to-date at > 10 GHz.
- Many labs fabricate this switch with high yield
- Can be done in shunt or series designs
- Sensitive to temperature but corrugations in the membrane help to mitigate.

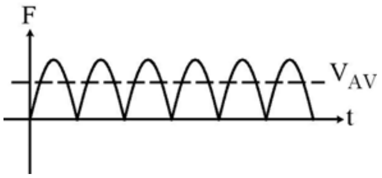
Power Handling: Shunt Capacitive Switch in Upstate-Position





$$V_b = V_{RF}$$

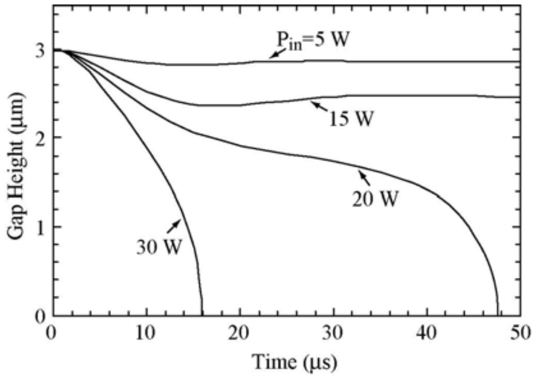
$$V_{AV} = \frac{V_b}{\sqrt{2}} = \sqrt{PZ_0}$$



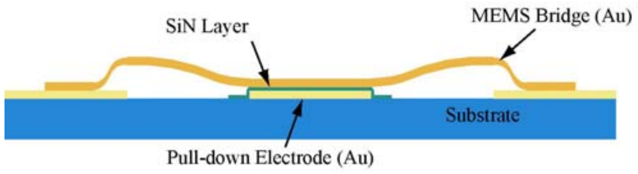
If V_{AV}>V_P; Self Actuation

V_P = 10V P = 2 W; (Z_0 = 50 Ω)

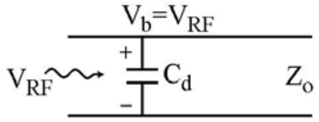
V_P = 20V P = 8 W;

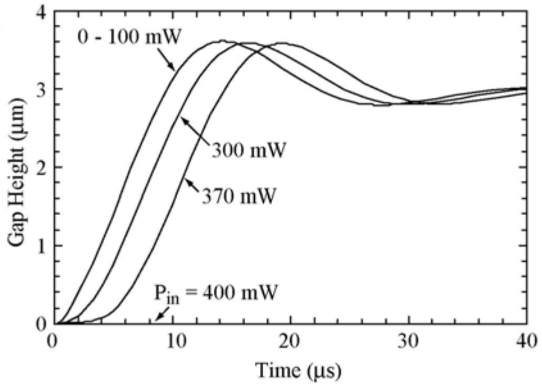


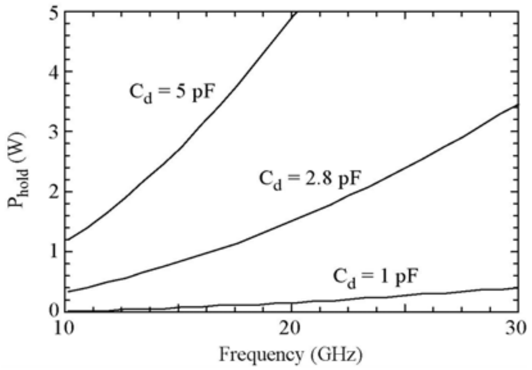
Power Handling: Shunt Capacitive Switch in Down-State Position



$$V_b \approx \frac{2\sqrt{2PZ_0}}{\omega C_d Z_0}$$







If $\frac{V_b}{\sqrt{2}} > V_{Hold}$; **Hold Down**

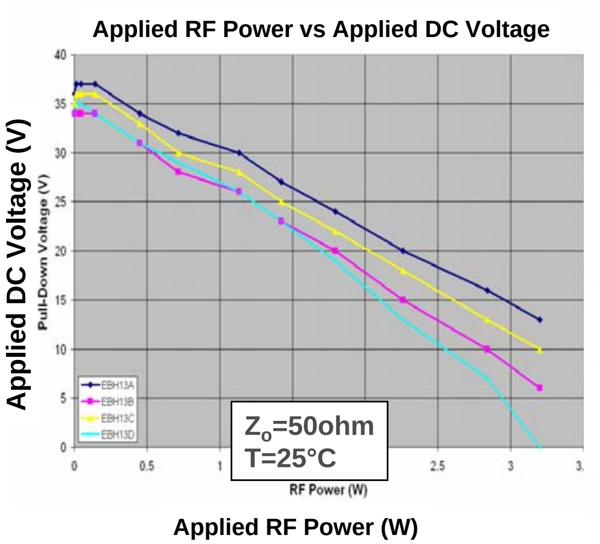
V_{Hold} = 1 V,

C_d = 2.8 pF,

f = 10 GHz;   P = 390 mW;

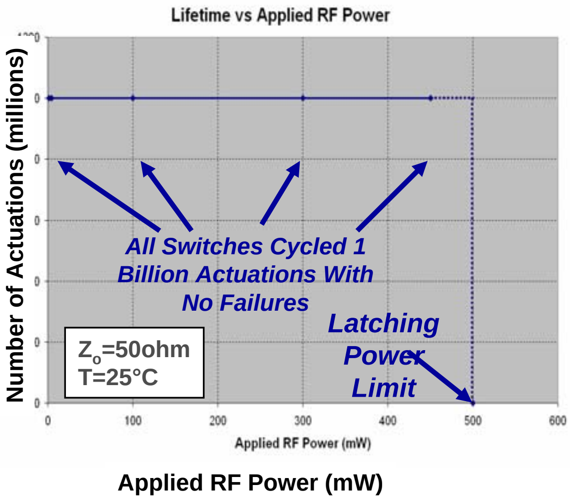
The University of Michigan

Self-Actuation Power Limits: Measurements



Z_o=50ohm
T=25°C

Actuations vs. Applied RF Power



All Switches Cycled 1 Billion Actuations With No Failures

Latching Power Limit

Z_o=50ohm
T=25°C

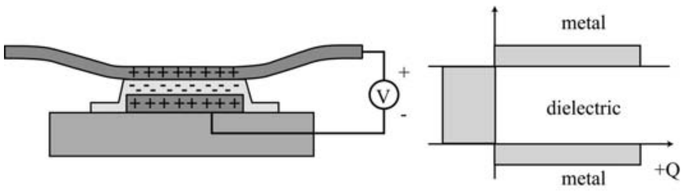
Applied RF Power (mW)

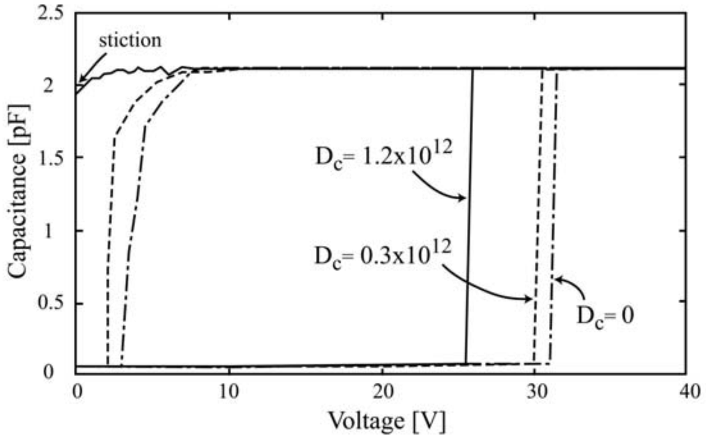
- Agrees quite well with models. Well understood phenomena.

Raytheon

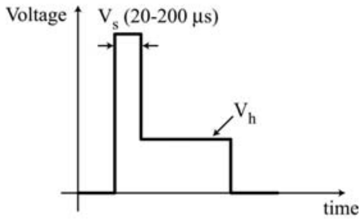
Reliability of Capacitive Switches

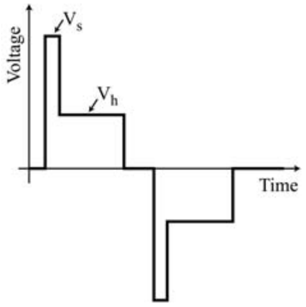
- Switch lifetime in Capacitive Switches is due to metal-to-dielectric stiction.
- In this case, there is a large contact area (80x100 um) and stiction occurs mostly due to *dielectric charging*.
- Possible Solution: Use bipolar voltage so as not to charge the dielectric. Price is a two level voltage which is not allowed in many portable applications.

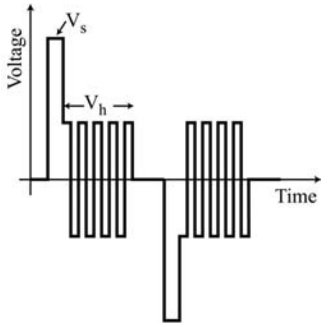




Bipolar Activation to Solve Dielectric Charging

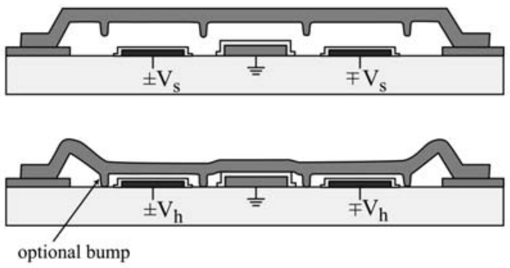






- Bipolar results in low frequency noise (may be acceptable in some applications)

Separation of pull-down electrodes



Raytheon

Dielectric Charging

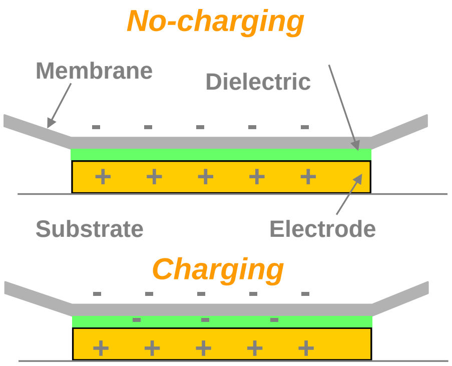
- Phenomena

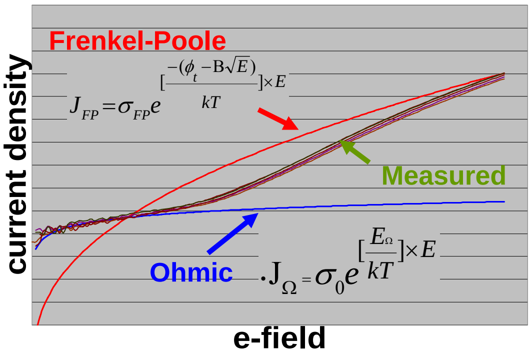
  Tunneling and trapping of electric charges on or in the switch dielectric layer. These charges are isolated by the high resistivity and long recombination times within the dielectric.

- Effect on MEMS switches

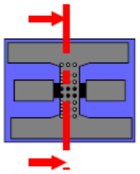
  Buried charges within the dielectric layer screen the electrostatic field and may cause the switch not to release (stick) or actuate when desired.

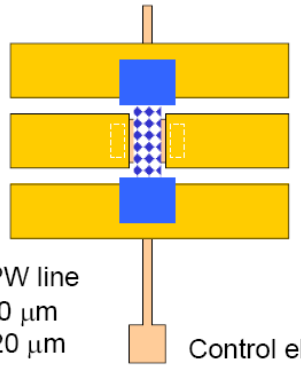
- Types of Charging
  - **Ohmic (Fowler-Nordheim)**
  - **Frenkel-Poole**
  - **Dielectric charging is a combination of both charging mechanisms**

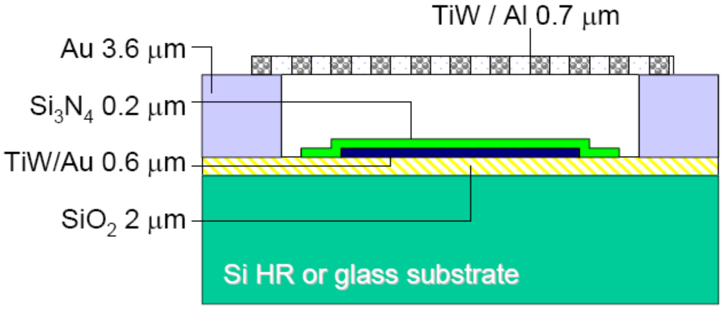




MEMS technology used : ‘ Surface micro-machining ’







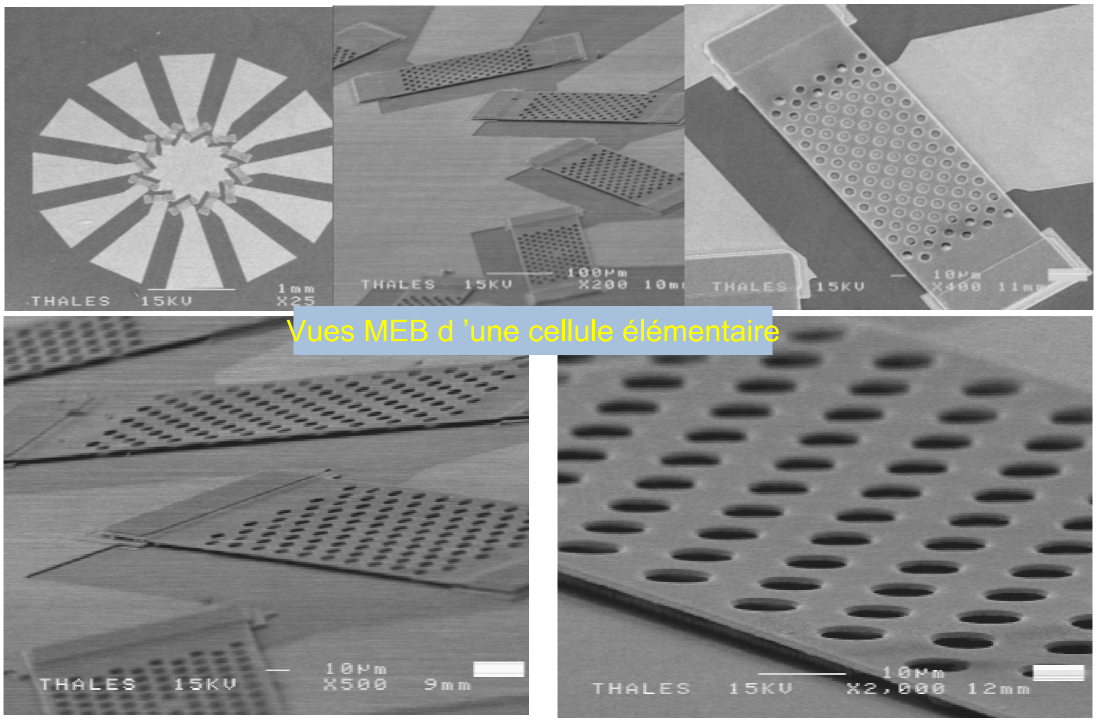
Schematic of cross section (Shunt Switch)

Holes are etched into the membrane in order to facilitate the membrane ‘ delivery ’

afshin.ziaei@thalesgroup.com

Reflectarray antenna for satellite : ARRESAT

Réalisation cellules actives



Vues MEB d 'une cellule élémentaire

Power Handling of RF MEMS Capacitive shunt switches

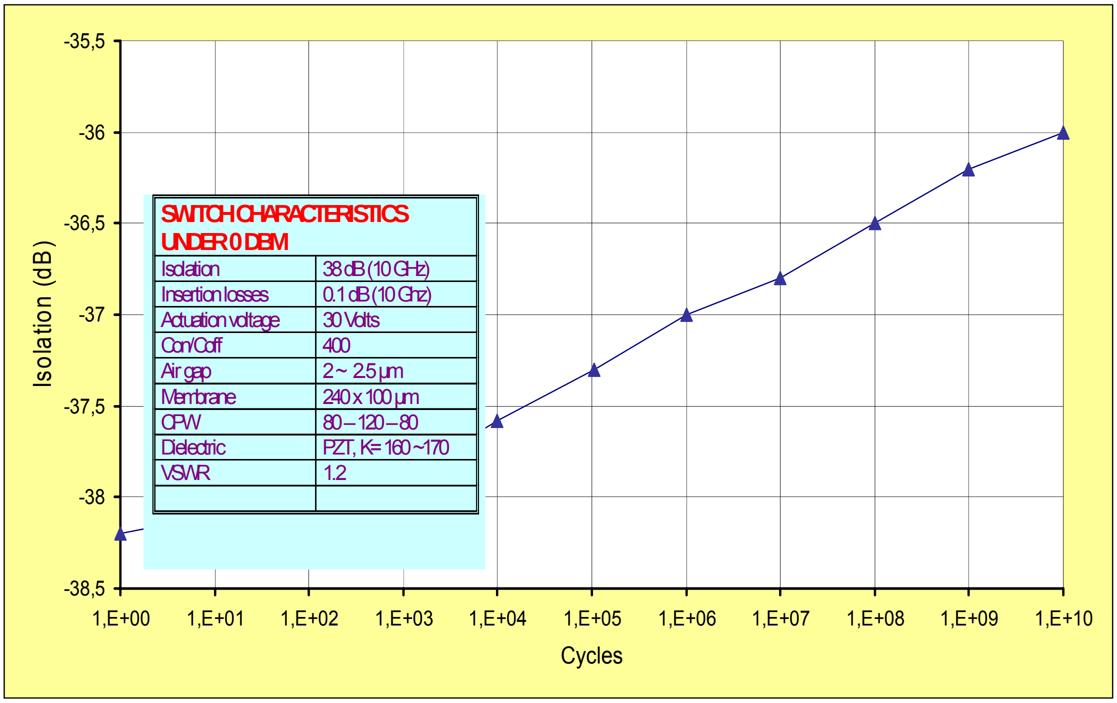
PZT parallel capacitive switch

ISOLATION	36dB (10GHz)
PERTES INSERTION	0.1dB (10GHz)
TENSION D'ACTIVATION	55 Volts
RAPPORT Con/Coff	400
GAP D'AIR (entre membrane et diélectrique)	2~2.5µm
MEMBRANE	240µm x 100µm
Cpw	80µm/120µm/80µm
METALLISATION DE LA MEMBRANE	0.5 µm Al, 0.2µm TiW
CONSTANTE DIELECTRIQUE UTILISEE (PZT)	160~170
VSWR	1.2
Switching time	5 µs

under 0dBm (10 GHz)

afshin.ziaei@thalesgroup.com

RF lifetime of switch at 10GHz with 30 dBm of input power, cold switching conditions



SWITCH CHARACTERISTICS UNDER 0 DBM	
Isolation	38 dB (10 GHz)
Insertion losses	0.1 dB (10 Ghz)
Actuation voltage	30 Volts
Con/Coff	400
Air gap	2 ~ 2.5 µm
Membrane	240 x 100 µm
CPW	80 – 120 – 80
Dielectric	PZT, K= 160 ~170
VSWR	1.2

RF lifetime of switch at 10GHz with 30 dBm of input power, cold switching conditions

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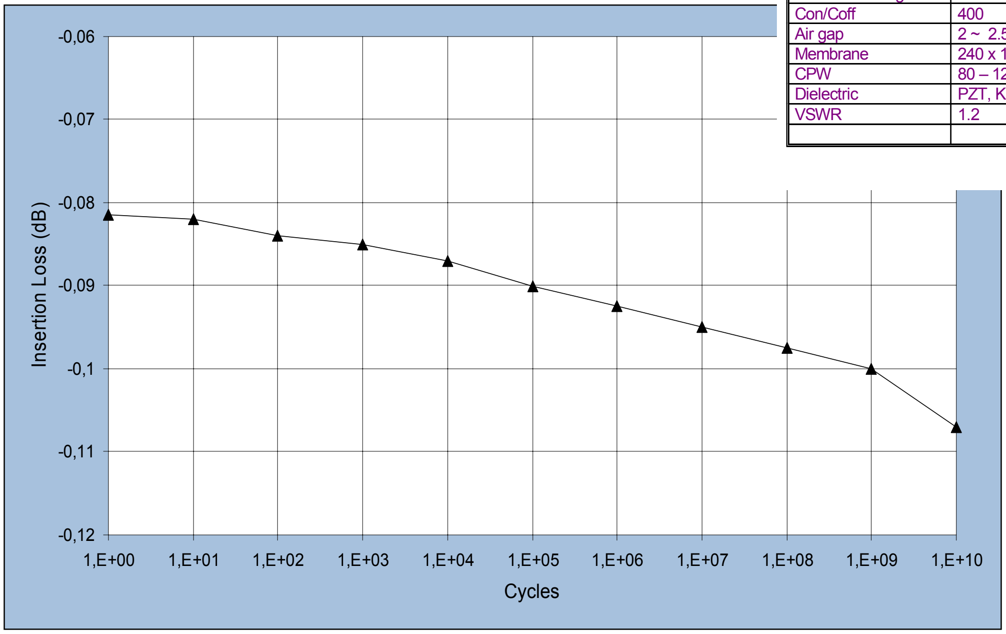
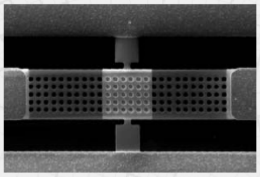
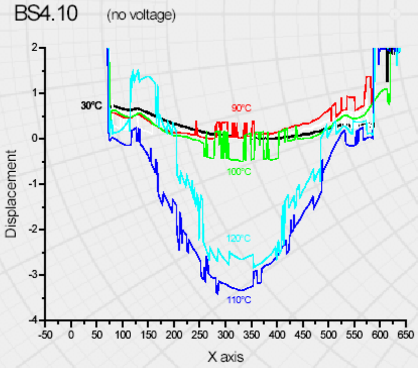
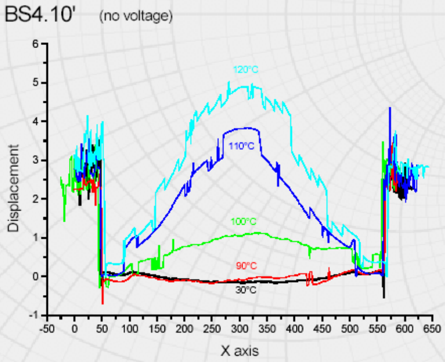


Thermomechanical Behaviour

	Al	Si
Young's modulus	71 GPa	
Thermal expansion	$22.7 \ 10^{-6} \ {}^\circ C^{-1}$	$2.3 \ 10^{-6} \ {}^\circ C^{-1}$





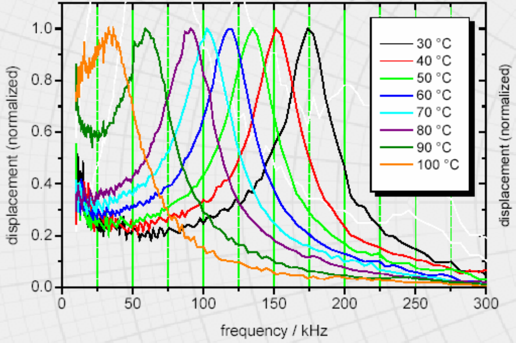


$$\sigma = \sigma_{res} - \alpha \Delta T E \left[1 - \frac{L_b - W}{3 L_b} \right]$$

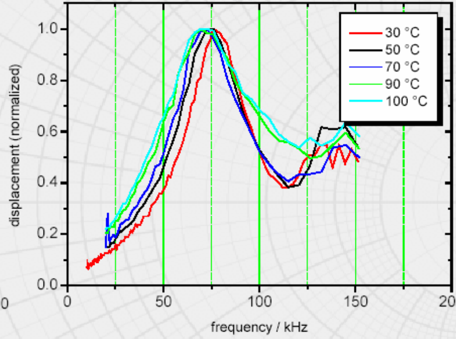
$$k = k1 + k2 = \frac{32\, E w_b t_b^3}{L_b^3 \left[2 - \left(2 - \frac{W}{L_b} \right) \left(\frac{W}{L_b} \right)^2 \right]} + \frac{8 \sigma (1 - \upsilon) w_b t_b}{L_b \left(2 - \frac{W}{L_b} \right)}$$

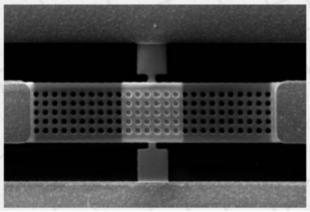
Temperature and resonance frequency

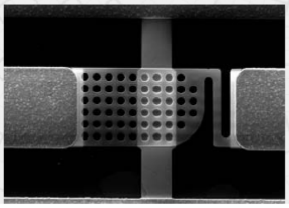
Standard bridge



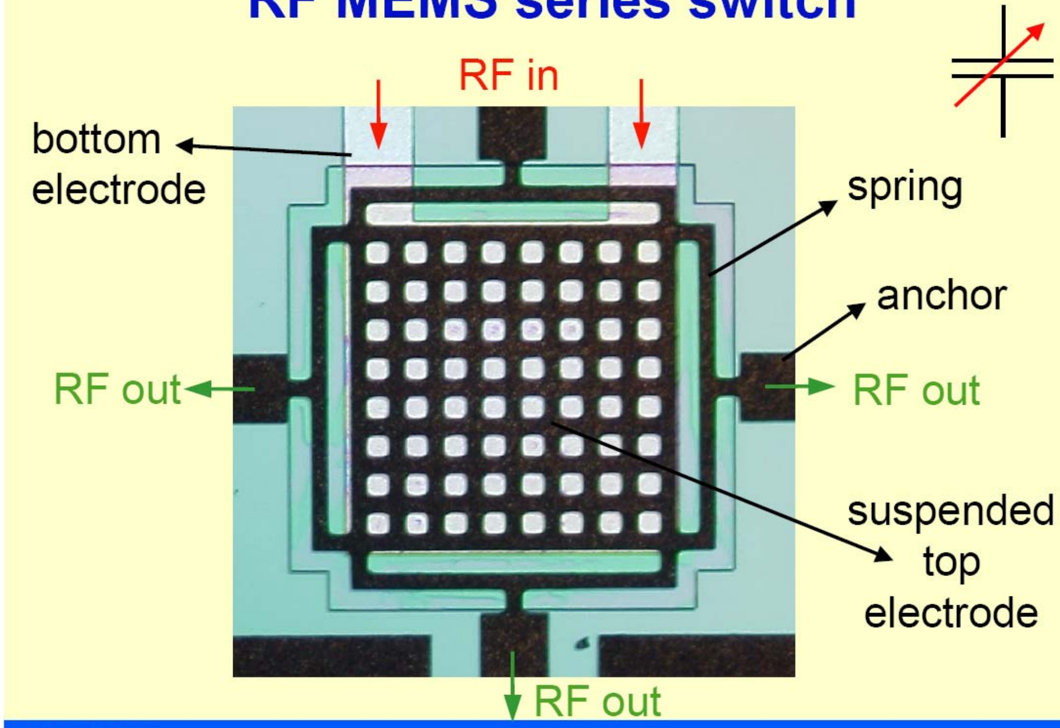
Bridge with S-type suspension







RF MEMS series switch



Current handling

Issues:

- RF losses → efficiency reduction
- Heating → deformations

1 A → ΔT_{max}=86 °C

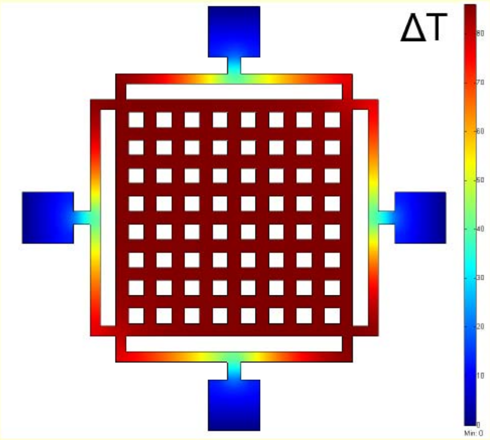
→ ~0.5 µm in-plane deformation

Solutions:

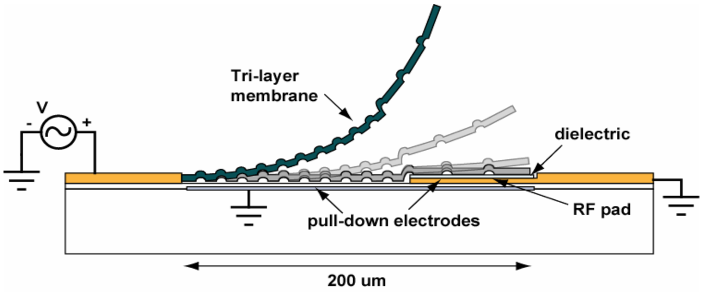
- Minimize ESR
  - Thick metal
  - Wide,short&many springs

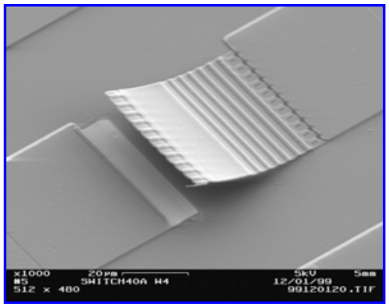
→ ESR <500 mΩ at 3 GHz, R_{dc}<100 mΩ

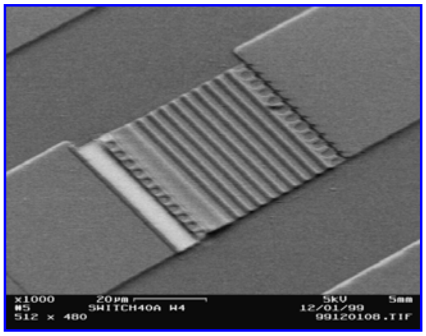
  - Multiple switches in parallel
- Reduce temperature sensitivity
  - Temperature stable design



Lincoln Labs Capacitive Switch Actuation







- Electrostatic Actuation
  - Moderate pull-down voltage (V_p = 35-40 V)
  - Low hold-down voltage (V_h = 8-10 V)
- Residual stress in tri-layer membrane provides restoring force
  - Tri-layer membrane is temperature stable from -70 to 170º C
  - Withstands 350º C processing steps
  - Peeling action helps reduce stiction and squeeze film damping

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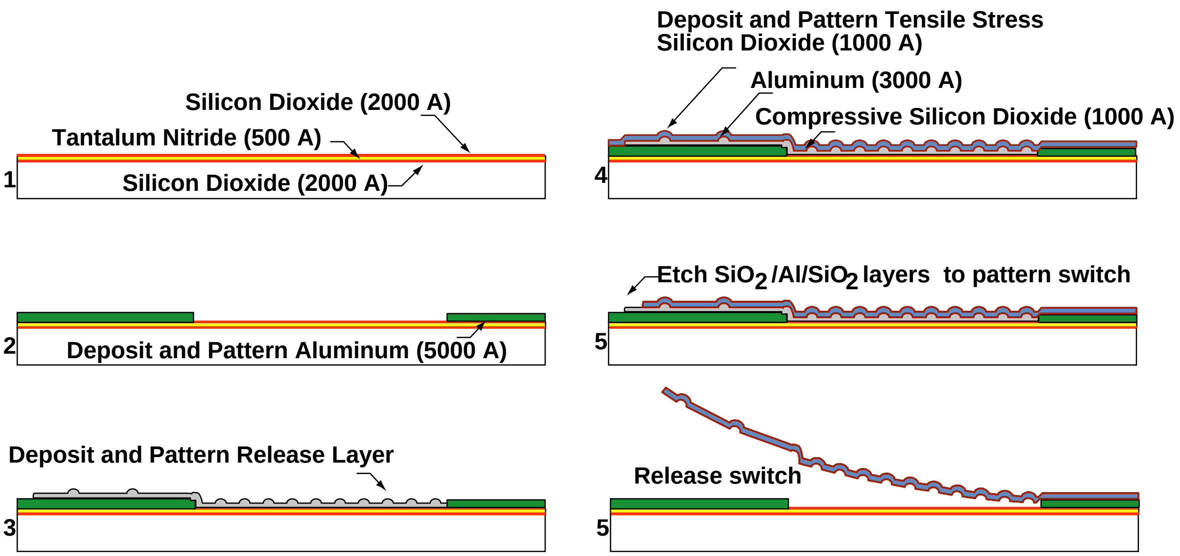
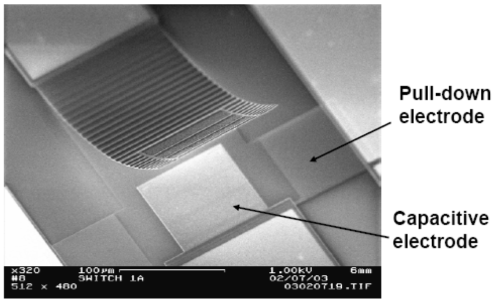
Lincoln Labs Capacitive Switch Fabrication Flow

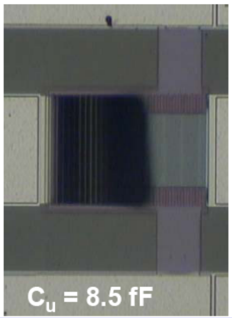


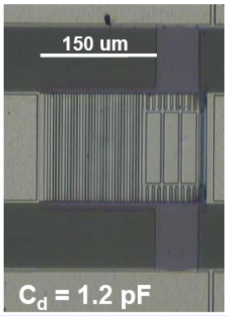
1. Silicon Dioxide (2000 A)
   Tantalum Nitride (500 A)
   Silicon Dioxide (2000 A)
2. Deposit and Pattern Aluminum (5000 A)
3. Deposit and Pattern Release Layer
4. Deposit and Pattern Tensile Stress Silicon Dioxide (1000 A)
   Aluminum (3000 A)
   Compressive Silicon Dioxide (1000 A)
5. Etch SiO_2 /Al/SiO_2 layers to pattern switch
5. Release switch

MIT-LL Capacitive Switch

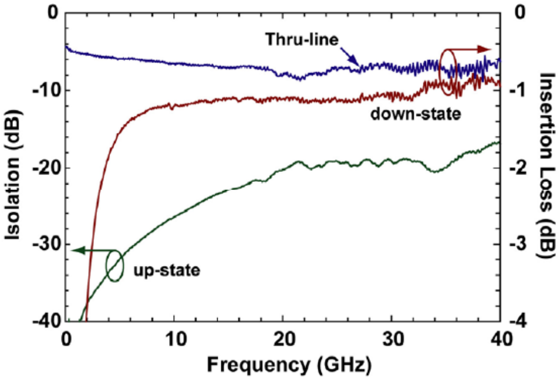
SEM of Series Switch







Measured S-Parameters



- Low insertion loss: <0.4 dB from 10-40 GHz
- High isolation: >20 dB from 0-40 GHz
- Power Handling: Successful hot/cold switching measured to 1.7/7 watts
- Unpackaged reliability: >100 B cycles
- Actuation voltage: 20-30V
- Low hold-voltage for high reliability

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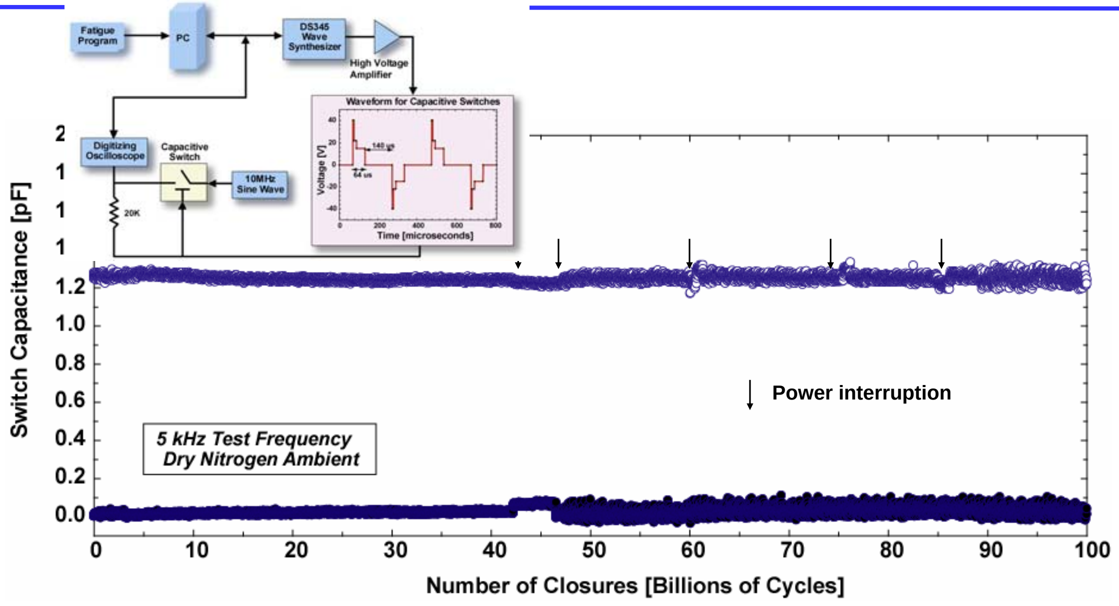
100 Billion Mechanical Cycles

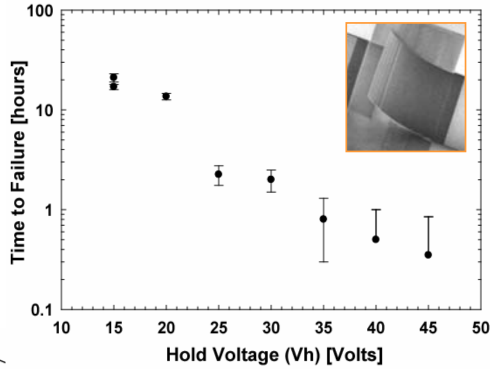


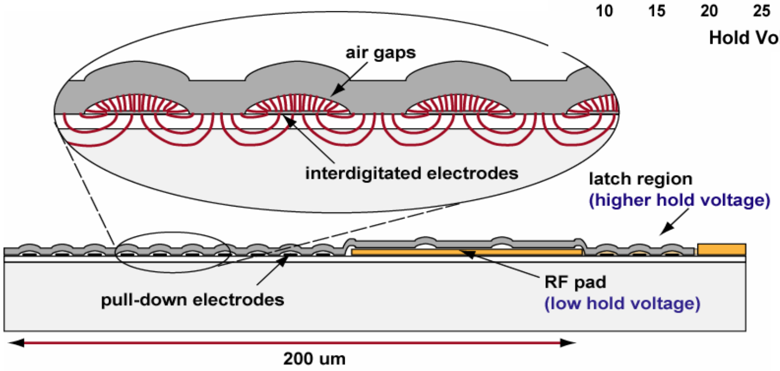
Test Notes: **- Open state capacitance floor is set by test set-up, actual open state capacitance is ~8.5 fF**
- Data re-calibrated from test circuit, average relative down-state value set to 1.25 pF.

Hold-Time vs. Hold-Voltage

- Hold-down times are important for re-configurable systems
  - Several switches have been held down for over a month with out failure
  - Integrated air gaps and thick dielectric layers can extend the hold-down time

Classic dielectric charging problem





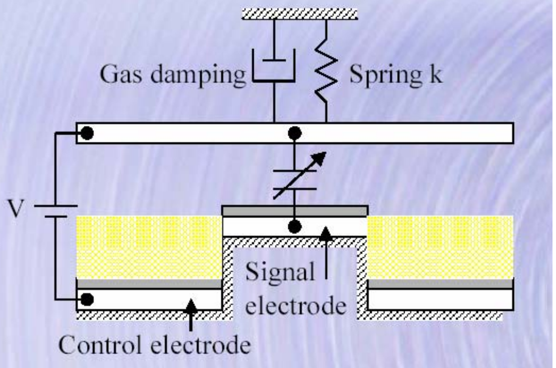
Quasi dual-gap

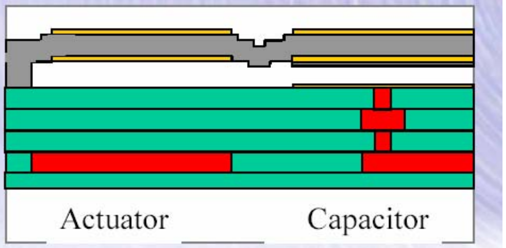
Musalem et al. Coventor

- If signal voltage << control voltage, a dual-gap approach can be used:

  Actuator air-gap should be > 3 times the capacitor air-gap

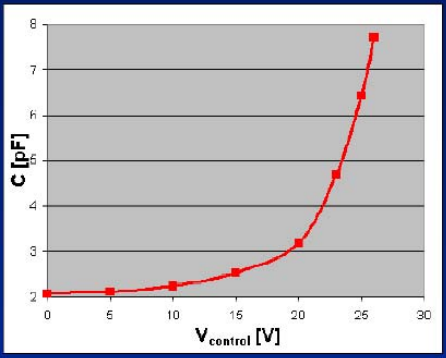
- Quasi- dual approach is equivalent, with a thick dielectric in the actuator gap

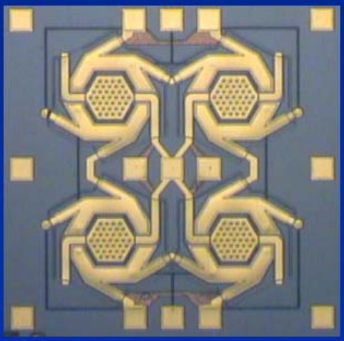


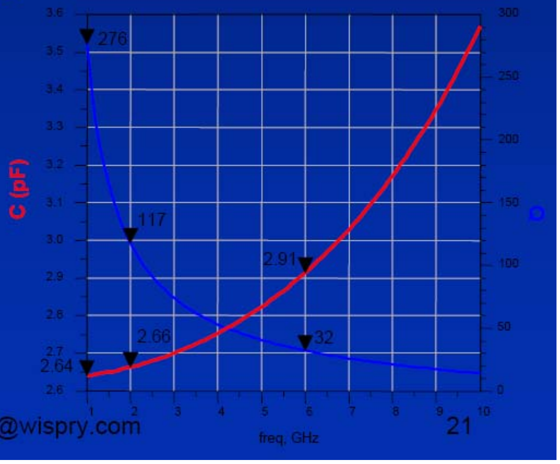


Varactor

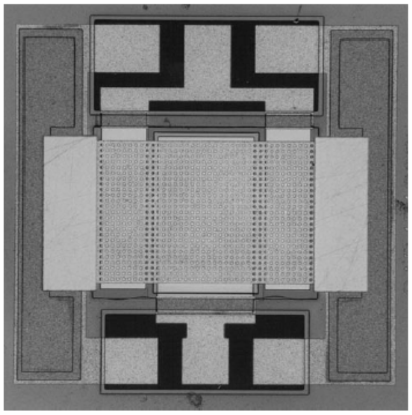
- Full controllable travel
  - No pull-in
  - Maximum capacitance at 25V
- Capacitance 0.5 – 2.0 pF
  - Ratio ~ 4
- Q at 2 GHz > 70
- Mechanical resonance > 20 kHz

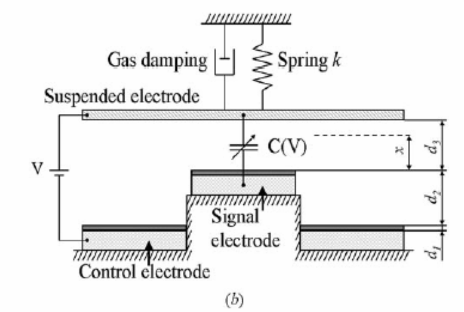


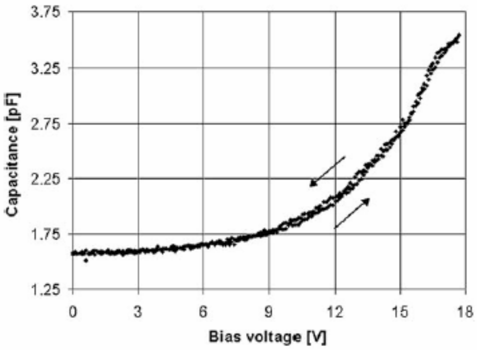


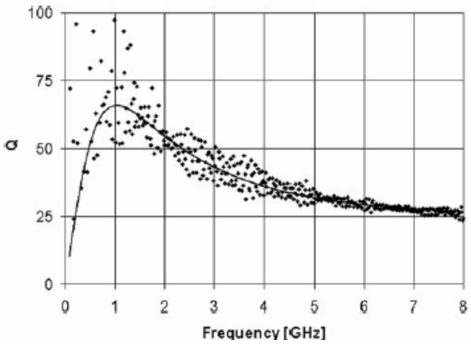


Analog Two-Gap Varactor from Nokia Research Labs



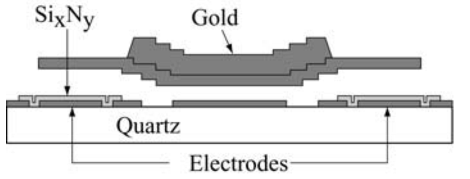


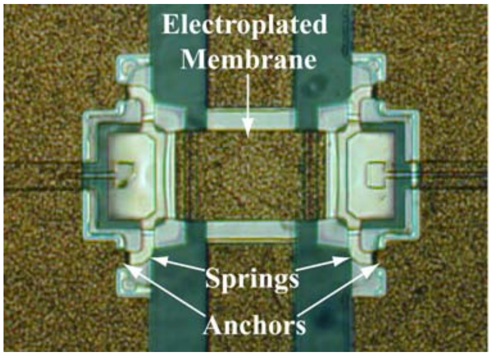


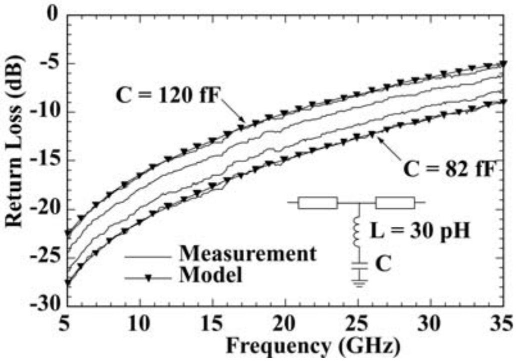


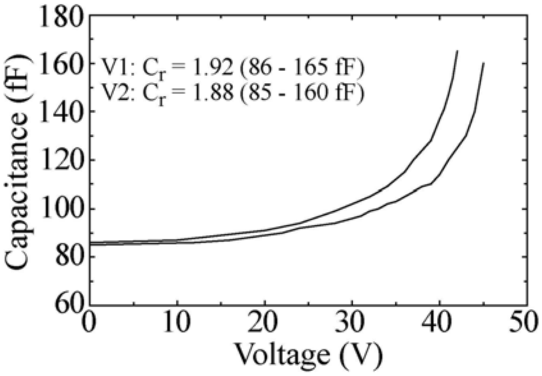
2 um gold membrane, Cr=1.7 with parasitics, Cr=2.7 without parasitics
Nieminen et al.; J. Micromachining 2002.

Extended-Range MEMS Varactors (UoM)



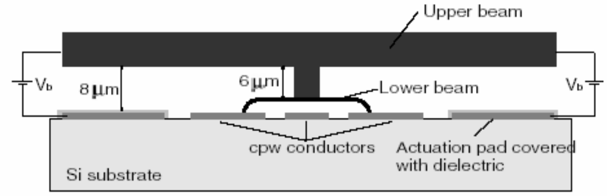




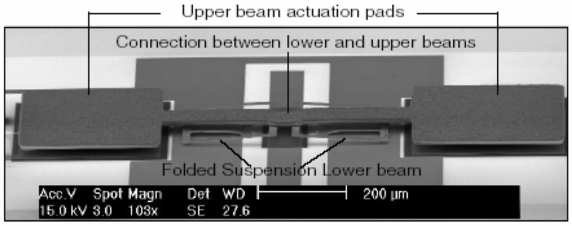


- **Q= 120-150 at 30 GHz (measured)**

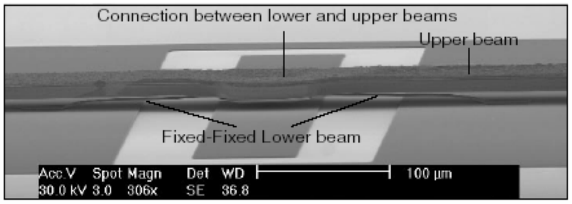
Extended Tuning Range with Two Metal Levels



(a)

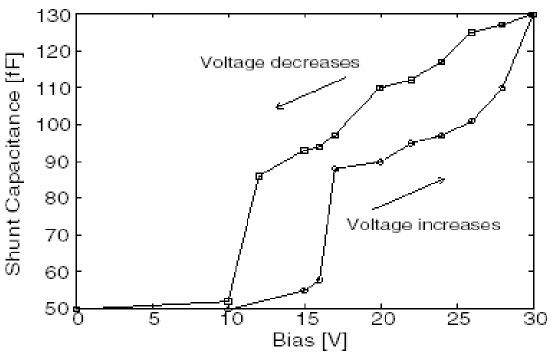


(b)



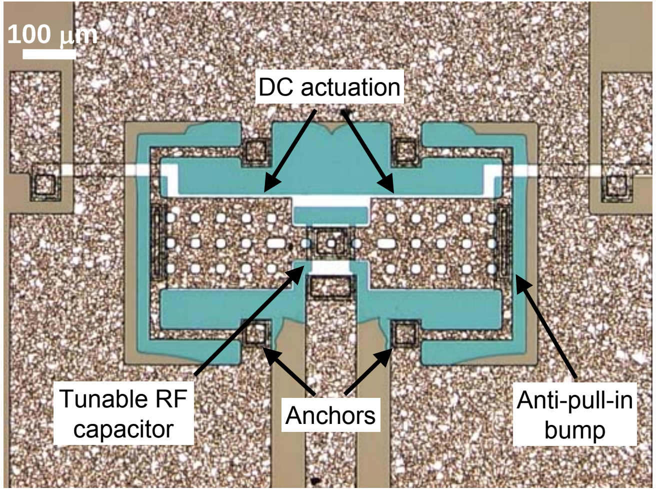
(c)

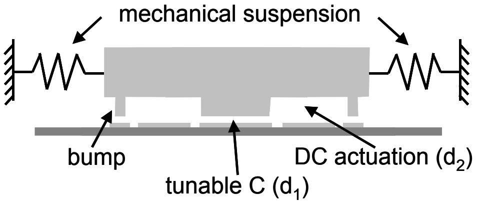
Varactor	A	B	C	D
Min. measured cap. value (fF)	50	51	42	40
Max. measured cap. value (fF)	130	140	130	125
Pull-in voltage (V) (± 1 V)	31	33	34	34
Pull-in capacitance (fF)	270	265	230	240
Measured tuning range (%)	160	175	210	213

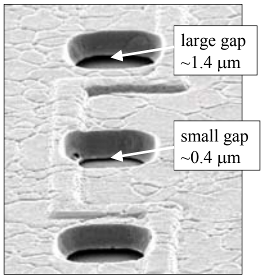


Peroulis, Katehi; MTT-S 2003.

Dual-gap tunable capacitor

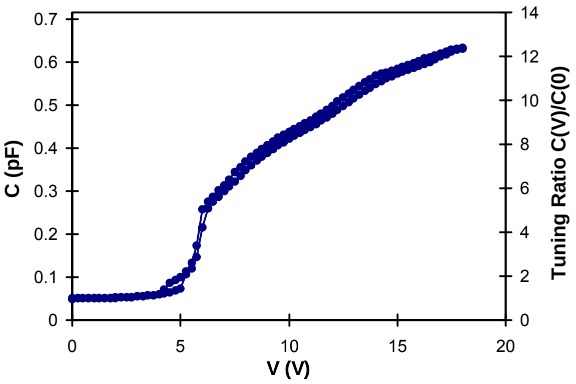


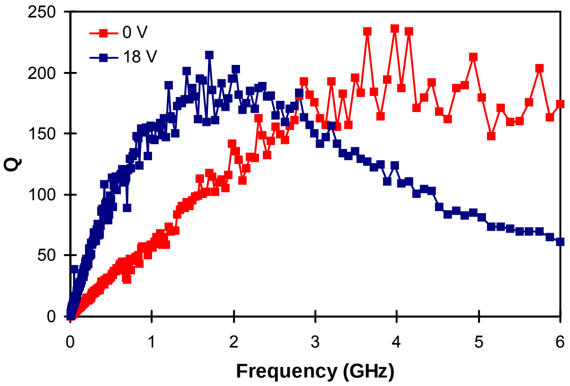




- Dual-gap design and bumps prevent ‘pull-in’ effect
- Mechanical suspension limits deformation due to thermal expansion
- Shunt capacitor in a 50 Ohm coplanar wave guide (CPW)

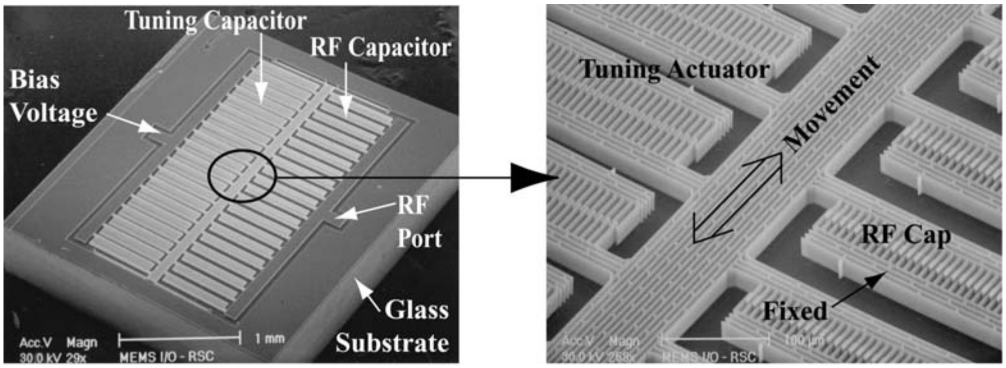
Capacitance versus bias voltage

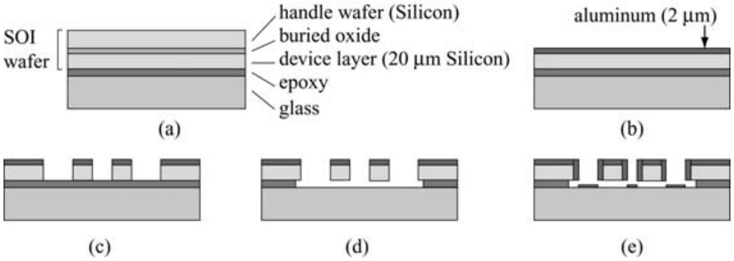


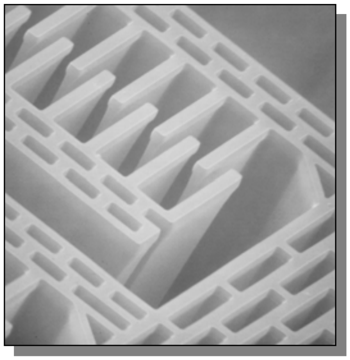


- Continuous and reversible tuning (no hysteresis)
- Tuning ratios up to 17 measured at 20 V actuation

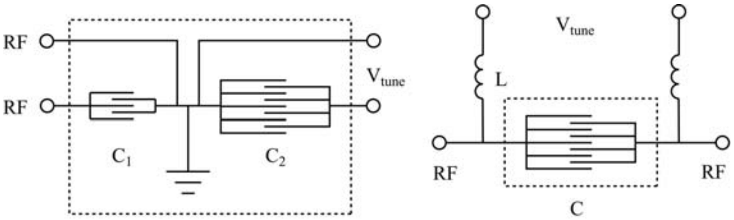
Rockwell Interdigital Varactor: Separate Actuation Electrode

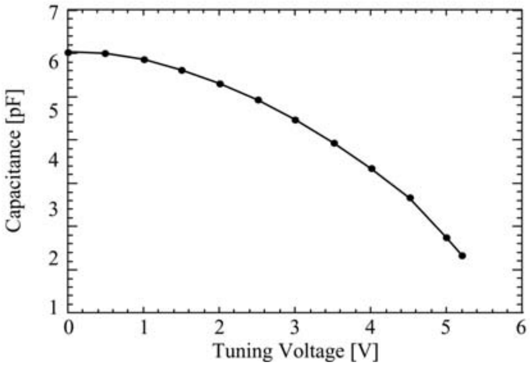


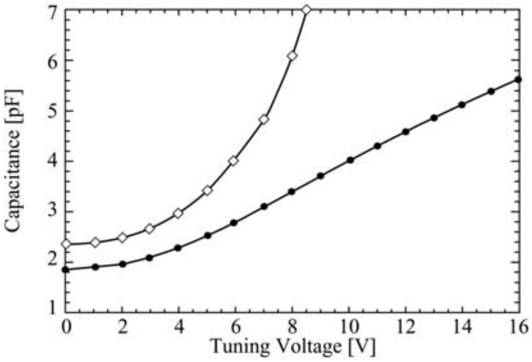




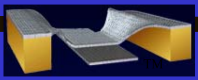
Rockwell Interdigital Varactor: Actuation Mechanisms





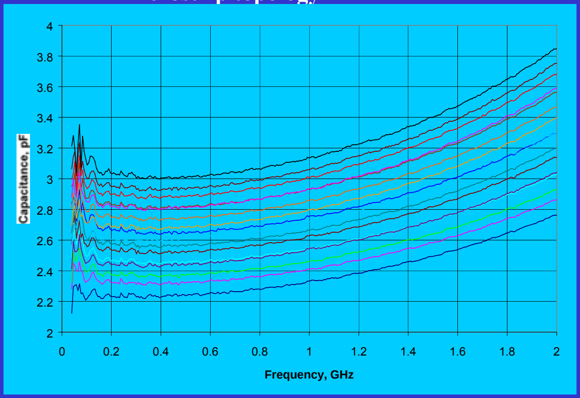


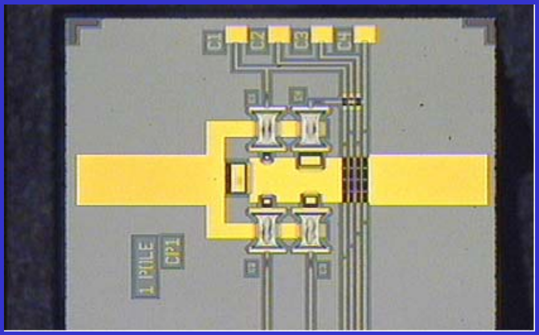
- Capacitance can be made to increase or decrease with voltage depending on the finger orientation. This results in 1:1 insertion with deployed filters.

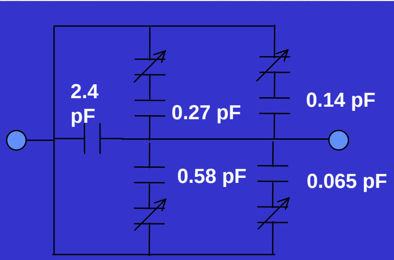


RF MEMS Variable Capacitor

- Five fixed capacitors
- Four MEMS switches
- Sixteen states
- Range 2.3-3.1 pF typ.
- Microstrip topology



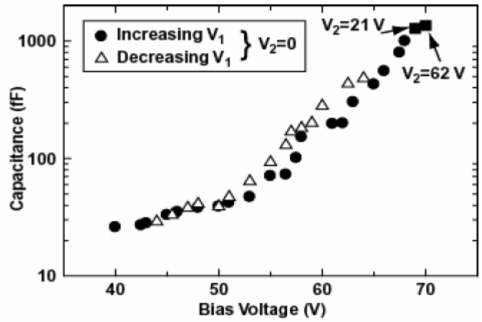


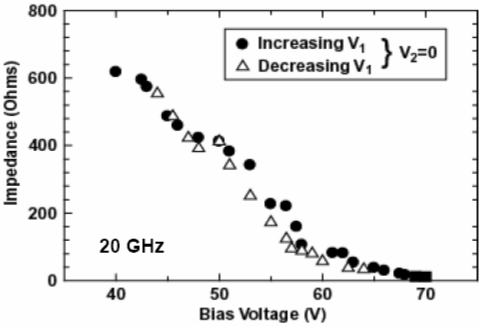


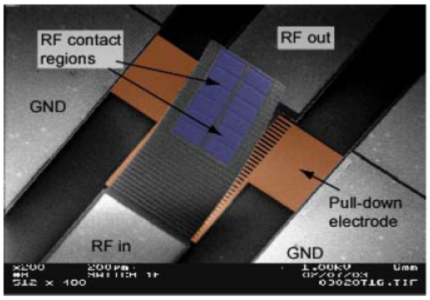
Raytheon

Variable Capacitor

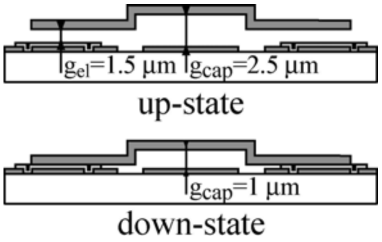
- Performance
  - 1.5 decade capacitance variation (30 fF-1.3 pF)
  - Low hysteresis
  - Nearly linear impedance vs voltage

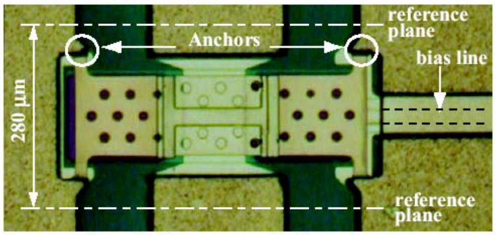


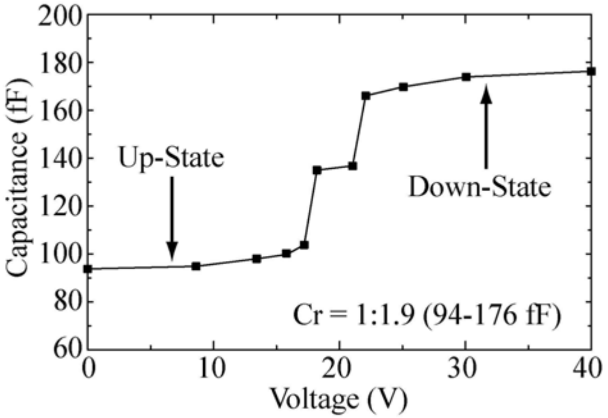


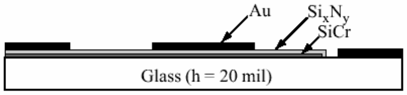


Switched Two-State M-A-M MEMS Capacitors

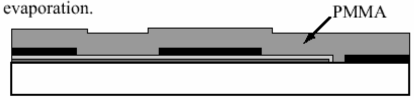




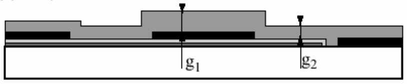




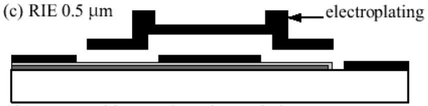
(a) 120 nm SiCr, 200 nm Si_xN_y PECVD, 0.5 µm gold evaporation.



(b) 1.5 µm PMMA



(c) RIE 0.5 µm



(d) 0.8 µm gold sputtering, electroplating, PMMA sacrificial layer etching and critical point drying

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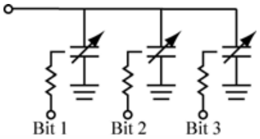
Discrete-Position Varactor Bank

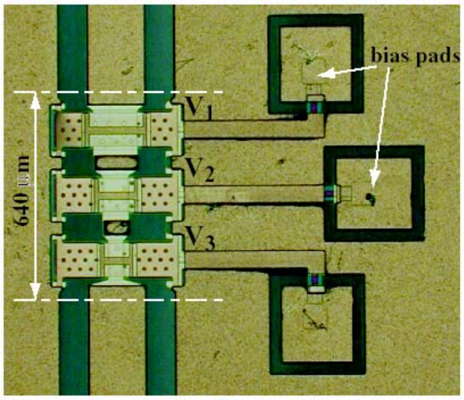
A varactor bank including 3 different discrete-position varactors in parallel results in 8 capacitance values. Bias electrodes are on the side.

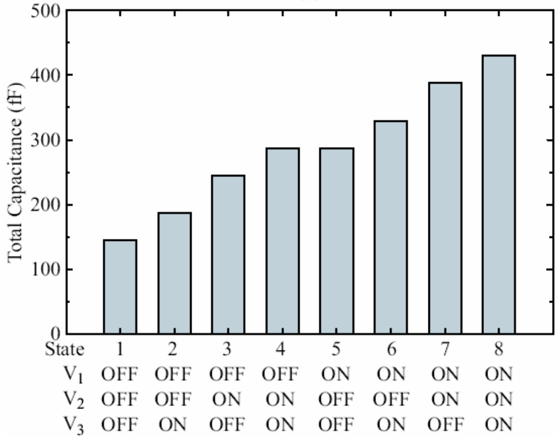
	C_1	C_2	C_3
C_u (fF)	63	45	38
C_d (fF)	205	145	80
Cap. Ratio C_d/C_u	3.25	3.22	2.1
C_{MIM} (fF)*	580	340	200

3-Bit Design

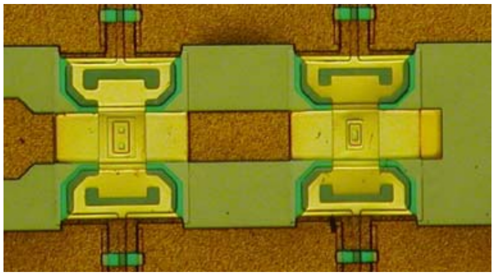


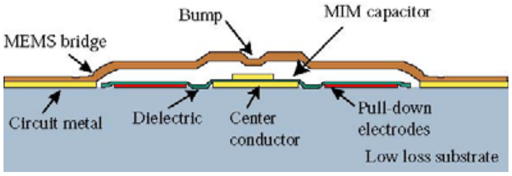
W_{Bridge} = 60 µm
W_{CPW} = 100, 70, 40 µm

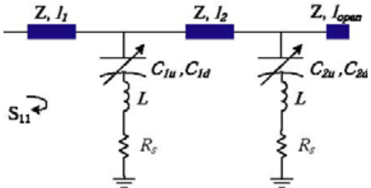


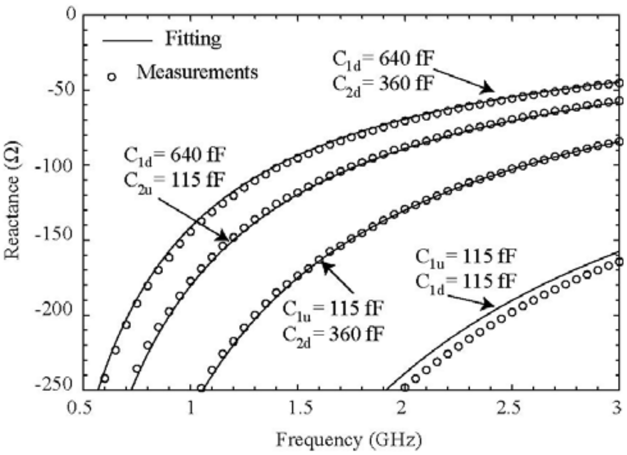


Two-Bit Switched Capacitor Array (metal contact is needed)





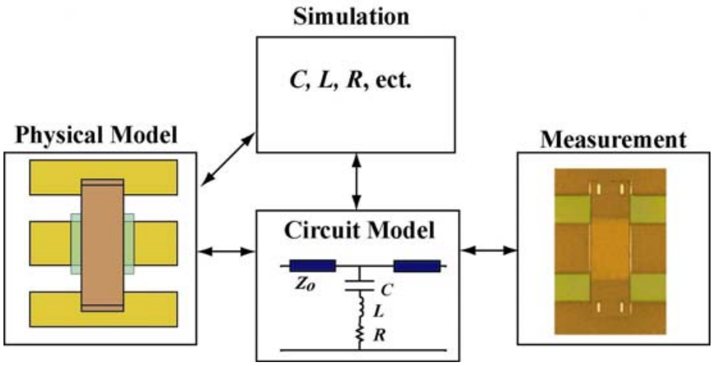




State	X @ 2 GHz	Ratio
C_{1u} & C_{2u}	-*j*250 Ω	1
C_{1u} & C_{2d}	-*j*130 Ω	1.9:1
C_{1d} & C_{2u}	-*j*90 Ω	2.8:1
C_{1d} & C_{2d}	-*j*70 Ω	3.6:1

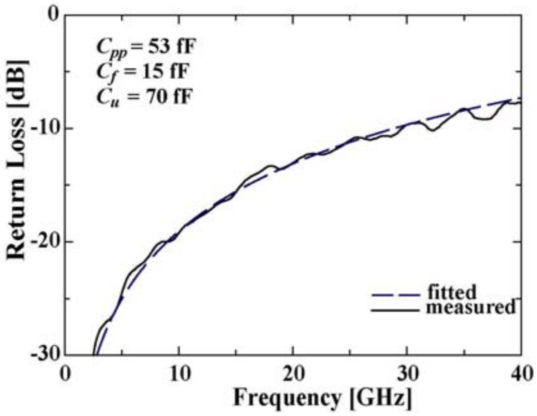
Electromagnetic Modeling of Capacitive Switches

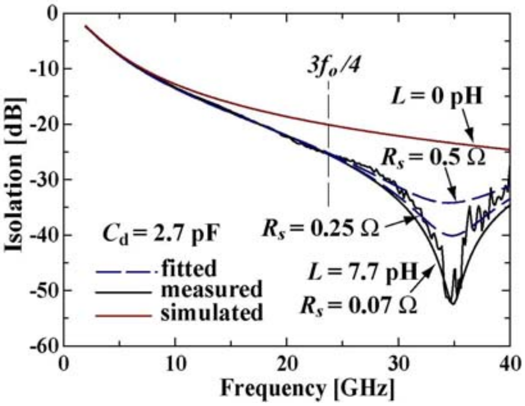
- **Develop simple equivalent circuit models to describe RF electrical behavior.**
  - **Isolation, Return Loss, Insertion Loss**

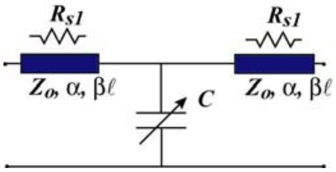


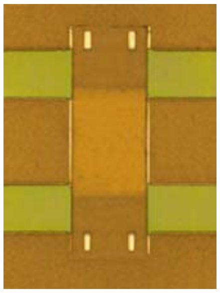
$$Z_s = \frac{1}{j\omega C} + j\omega L + R_s \qquad f_o = \frac{1}{2\pi\sqrt{LC}}$$

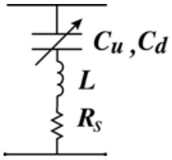
Fitting CLR to Switch Measurements







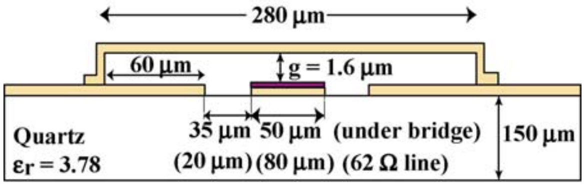


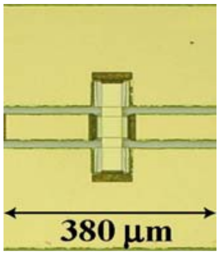


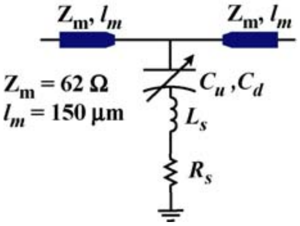
$W = 100$ μm, $w = 80$ μm, $L = 300$ μm,

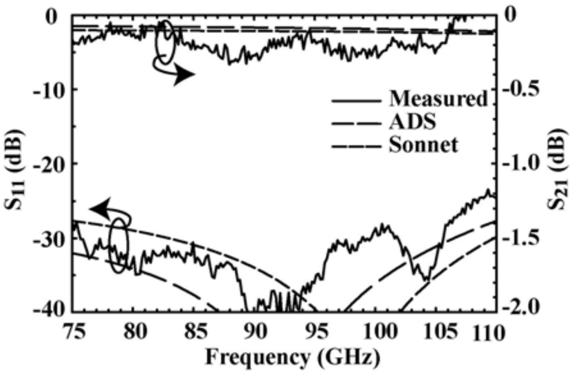
$t = 2$ μm, $t_d = 0.15$ μm

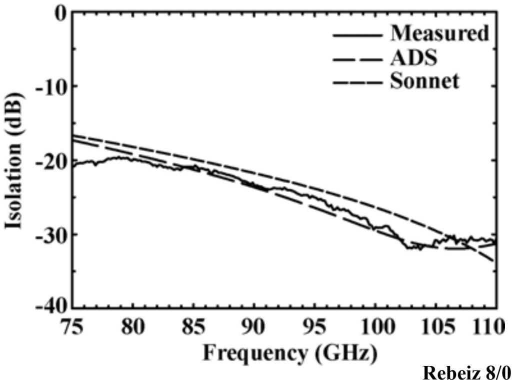
W-band CPW MEMS Switches on Quartz









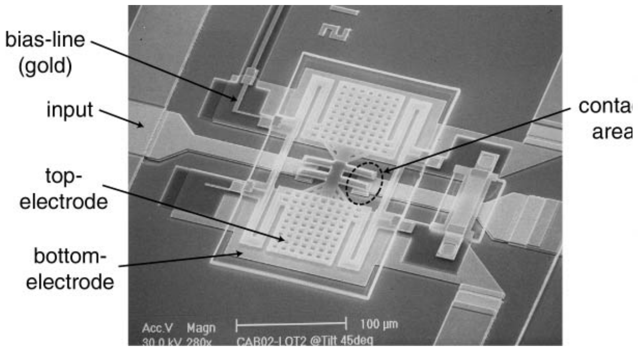


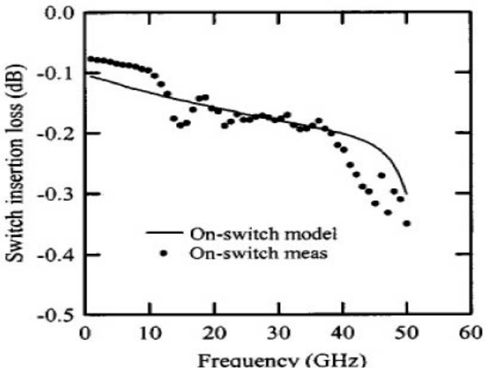
Measured Performance:

0.2 dB loss from 75-110 GHz
> 20 dB Isolation from 75-110 GHz

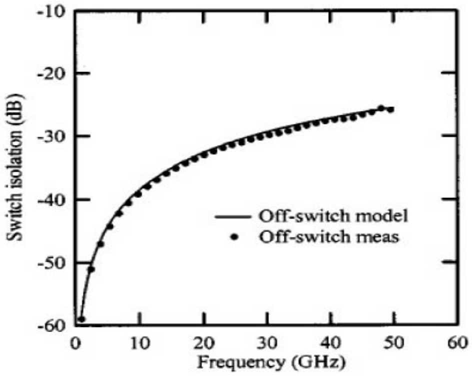
$C_u = 14$ +/- 1 fF, $C_d = 280 – 320$ fF
$L_s = 8\text{-}10$ pH, $R_s = 0.8 – 1\ \Omega$

Rockwell DC-Contact Series Switch





- Biasing circuits decoupled from RF Circuits.
- Dimples for improved contact.
- Actuation voltage = 70V
- R_s=1-2 Ω, C_u=1.75 fF
  $f_T = 1/(2\pi R_s C_u) = 90$ THz
- RF Performance:
  Loss = -0.12 dB at 10 GHz
  Isolation = -40 dB at 10 GHz



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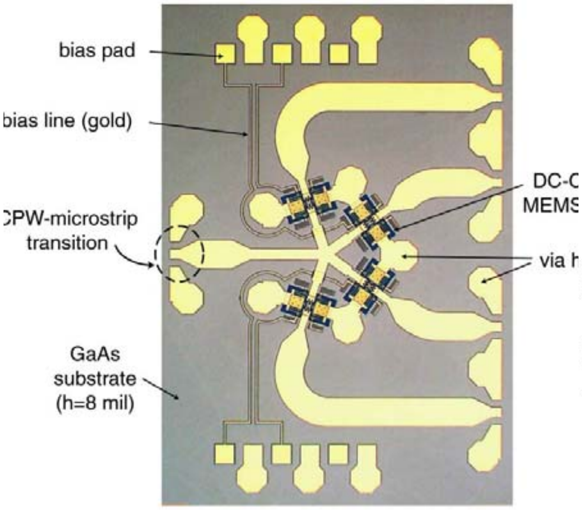
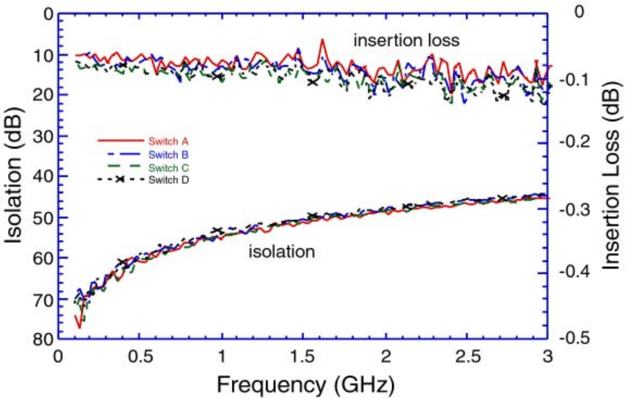
SP4T MEMS Switch Measurements (DC-20 GHz)



- Measured data from 0.1-3 GHz
- IL = 0.1 dB, isolation <-44 dB
- Excellent performance up to 20 GHz
- Switch Networks, Switched Filters, etc..



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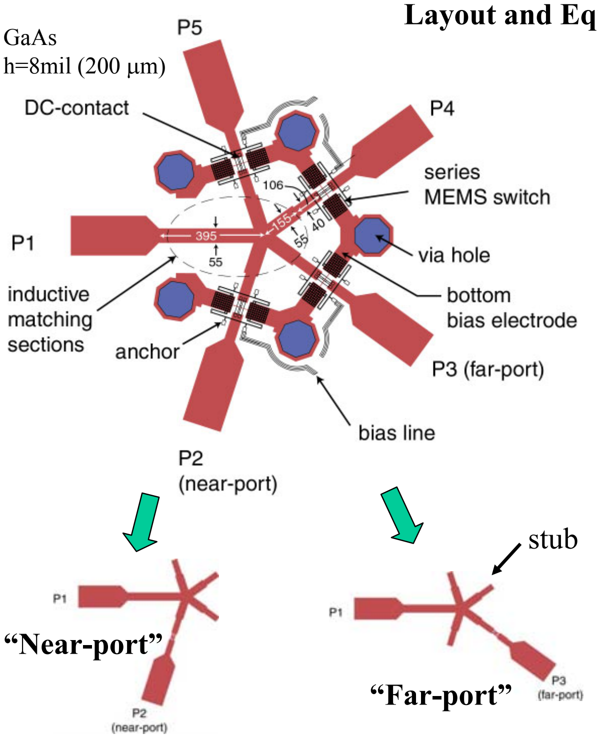
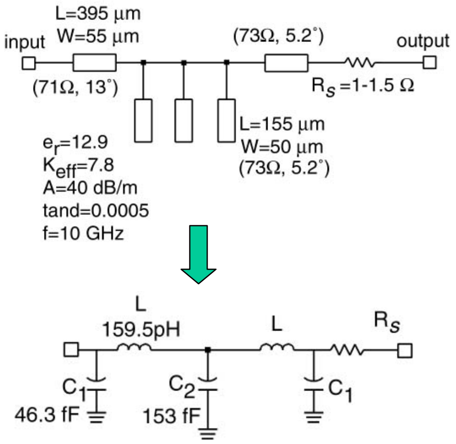
Design of SP4T Switch

Layout and Equivalent Circuit



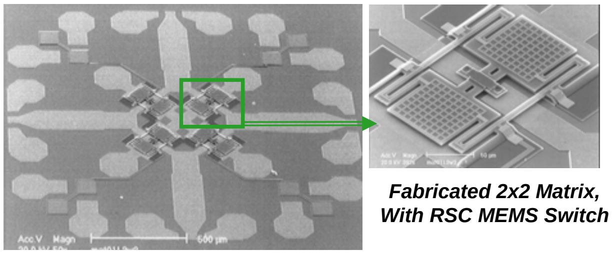
- **Determines the bandwidth of switched-line phase shifter**
- **Minimum stub length required for maximum bandwidth**



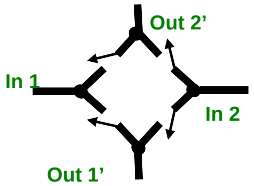
SPDT Building Block using MEMS Switch

Reconfigurable 2x2 Building-Block Circuit designed using (SPST) RSC MEMS Switch, whereby circuit functionality provided by 4 switches

MEMS 2x2 Circuit and Schematic

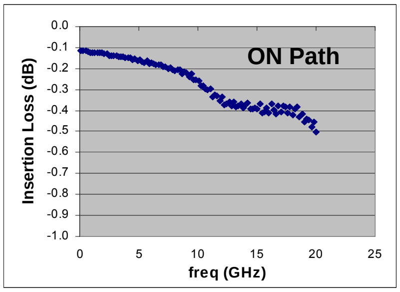


Fabricated 2x2 Matrix, With RSC MEMS Switch



Electrical Schematic of MEMS2x2 Switch Matrix utilizing UofM design elements

Circuit Performance



Measured ON State Loss

MEMS-Based circuit shows desired functionality with excellent electrical performance, suggesting minimal cost to host circuit.

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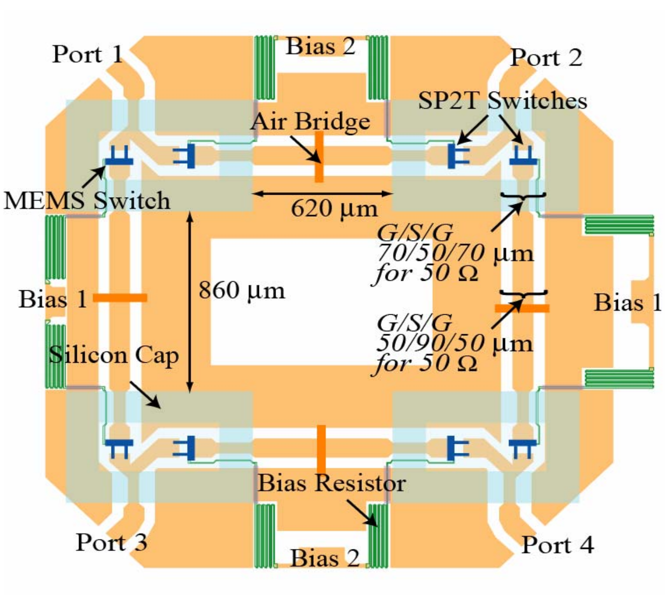
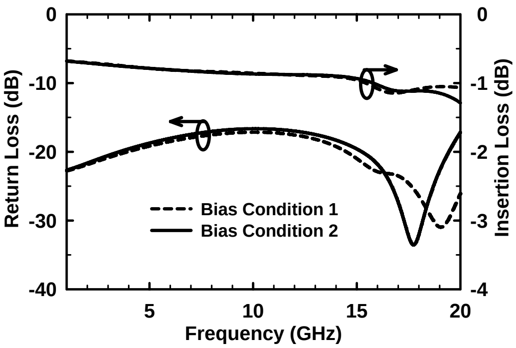
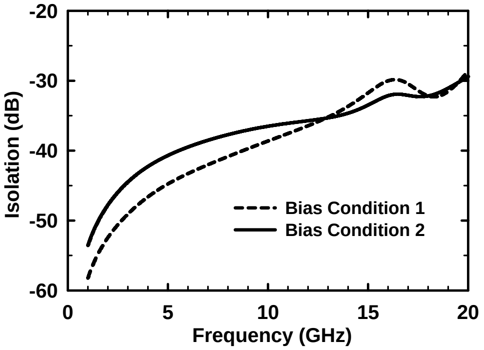
CPW DPDT Design Using Radant Switches



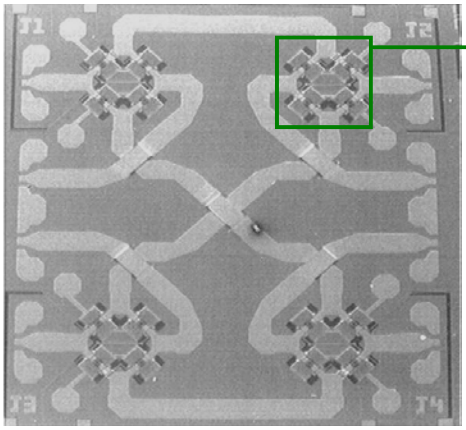




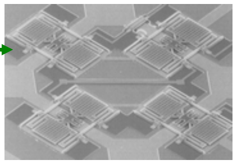
Scalability to 4x4 Switch Matrix

Reconfigurable 4x4 Circuit designed designed using 50-ohm T-Line connections of four 2x2 Circuits and micromachined airbridges

MEMS 4x4 Circuit

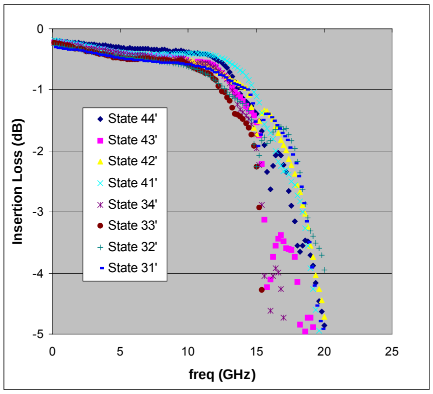


Fabricated 4x4 MEMS Switch Matrix



2x2 MEMS Subcircuit

Circuit Performance



Measured ON State Loss for 8 States

Architecture Scalability demonstrated, with large matrices also showing good electrical performance

State of the Art in RF MEMS Phase Shifters

- **Switches: 0.1 dB intrinsic loss up to 40-50 GHz (capacitive and metal-contact)**
- **State-of-the-art in MEMS Phase Shifters:**

  0.25 dB/bit at X-band (demonstrated: U.S., *Japan*)
  0.35 dB/bit at Ku-Band (demonstrated:U.S., *Japan*)
  0.50 dB/bit at K-Band
  0.70 dB/bit at Ka-Band (demonstrated: U.S., *Japan, Korea, Europe*)
  0.80 dB/bit at V-Band (demonstrated: *Korea* !)
  1.0-1.2 dB/bit at W-Band (demonstrated: U.S.)

- **Infinite shelf life. NO AGING. Low sensitivity to radiation damage**
- **Ideally suited for radars (always switching)**
- **On-wafer reliability demonstrated to 50-100 Billion cycles in the U.S. and Billions in Japan, Korea and Europe (at mW power levels). Excellent for missile systems.**

RF MEMS will be an enabling technology for phased array systems

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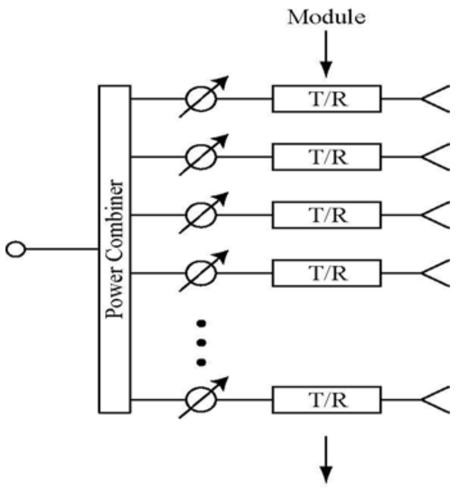
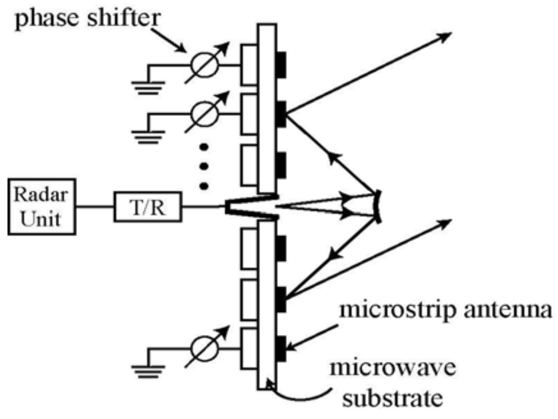
Phased Array Topologies





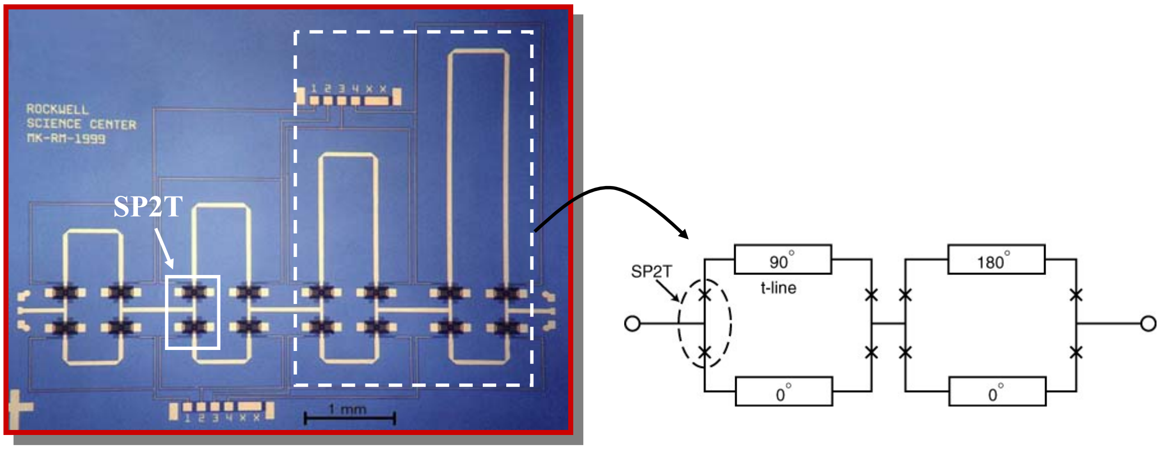
Standard Design:

- **Used in all systems today**
- **NF: 2-5 dB (17-35 GHz)**
- **Requires a T/R module per element**

Reflect Array Design:

- **Limited by phase shifter loss**
- **Requires one T/R module**
- **Not practical with GaAs MMICs (NF: 10-17 dB at 17-35 GHz)**

4-bit Rockwell Phase Shifter: Standard Design



- Based on SP2T switches
- Excellent Response: DC-40 GHz (linear phase shift)
- Insertion loss at 10 GHz: -1.0 dB (2-bit), -2.5 dB (4 bit)
- Signal passes by 4 MEMS switches in any phase state (2-bit)
- Long “reference” sections (increased loss)

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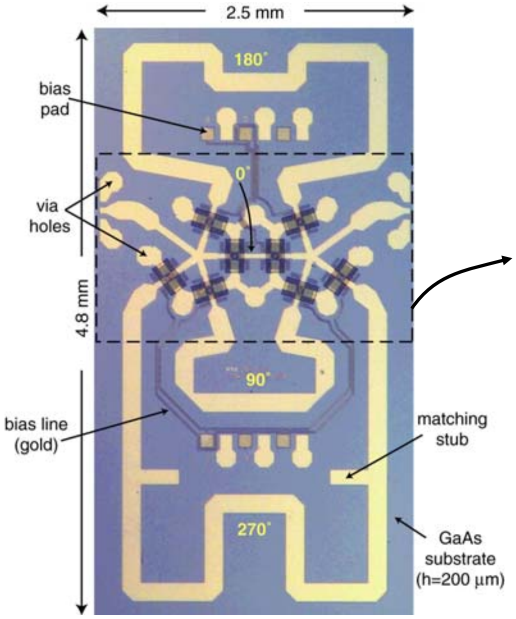
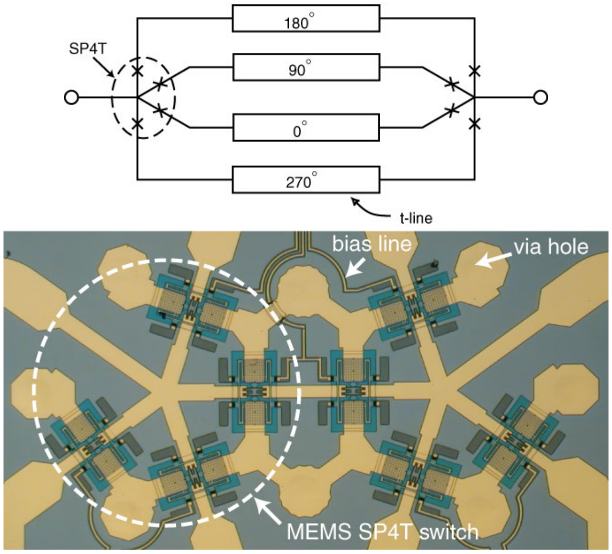
SP4T-Based Phase Shifters: UoM/Rockwell

- Circuit design by UoM, fabrication/test by Rockwell Scientific





- Pass by 2 switches and not 4 switches (2-bit)
- Very short reference line possible
- More compact circuit

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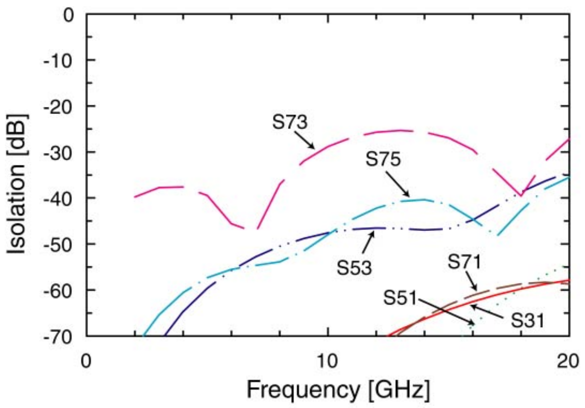
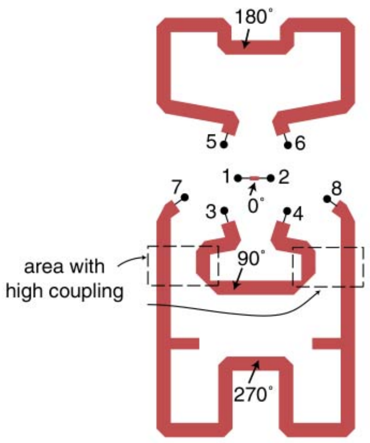
Rockwell Scientific

Design of 2-bit Phase Shifter

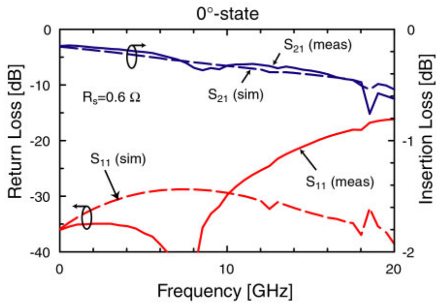
- **Coupling kept to < -25 dB to minimize influence on phase and matching of neighboring lines.**

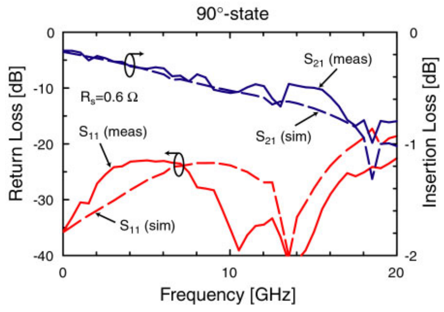


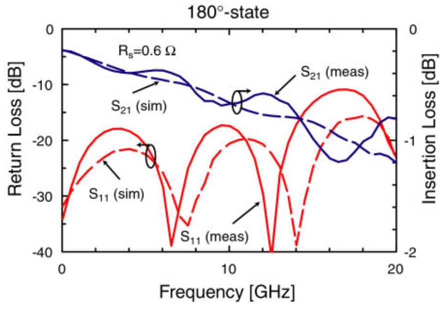


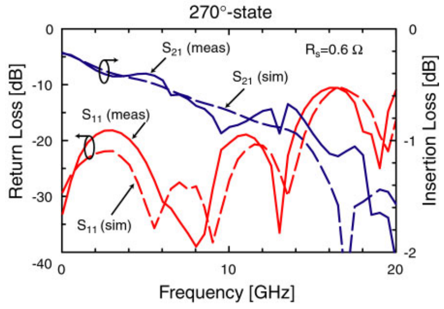
2-bit Phase Shifter Measurements

- **Curve-fitted R_s=0.6 W**
- **Insertion Loss = 0.6±0.3 dB (8-12 GHz), Return Loss < -17 dB**





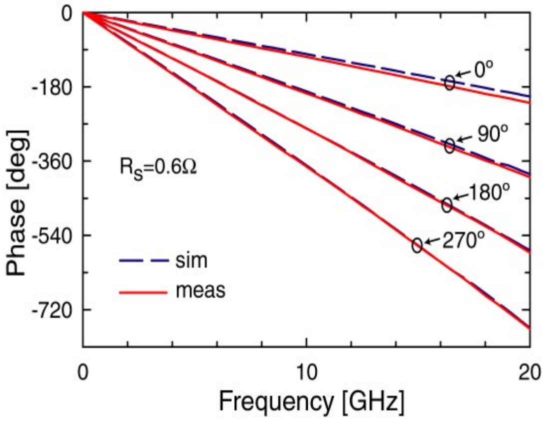




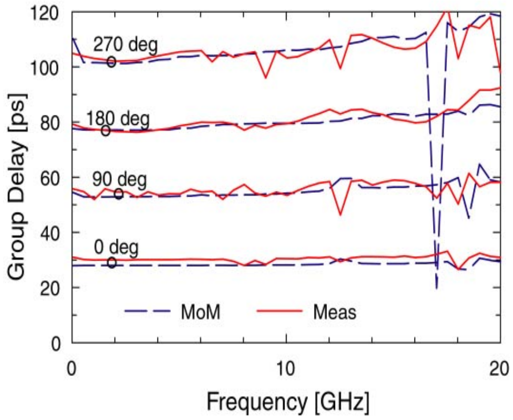
2-bit Phase Shifter Measurements: Phase

- 0 ° / 90.1 ° / 177.8 ° / 272° at 10.25 GHz
- Average Insertion Loss: -0.55 dB at 10 GHz
- Phase Accuracy = ± 2 deg (10 GHz)
- Substrate=GaAs, h=200 um
- Area = 9.6 mm2 (4.80x2.5mm)

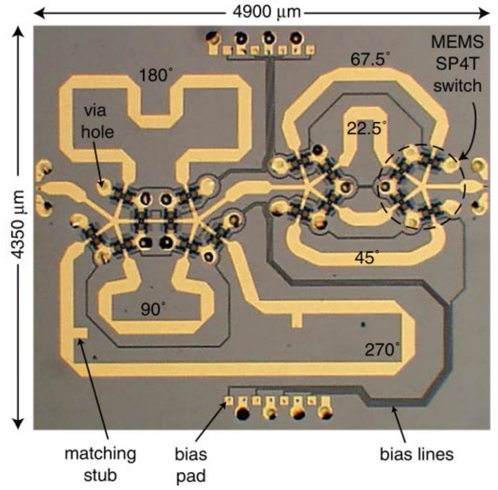
Phase

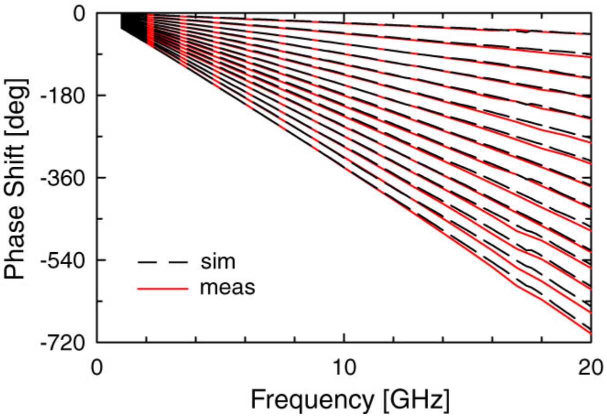


Group Delay



Extension to 4-bit Designs: UoM/Rockwell





- Phase Accuracy = ± 2 deg (10 GHz)
- Average Insertion Loss = -1.1 dB (10 GHz)
- Return loss < -14 dB DC-14 GHz

- Substrate=GaAs, h=200 μm
- Area = 21 mm^2 (4.90x4.35mm)

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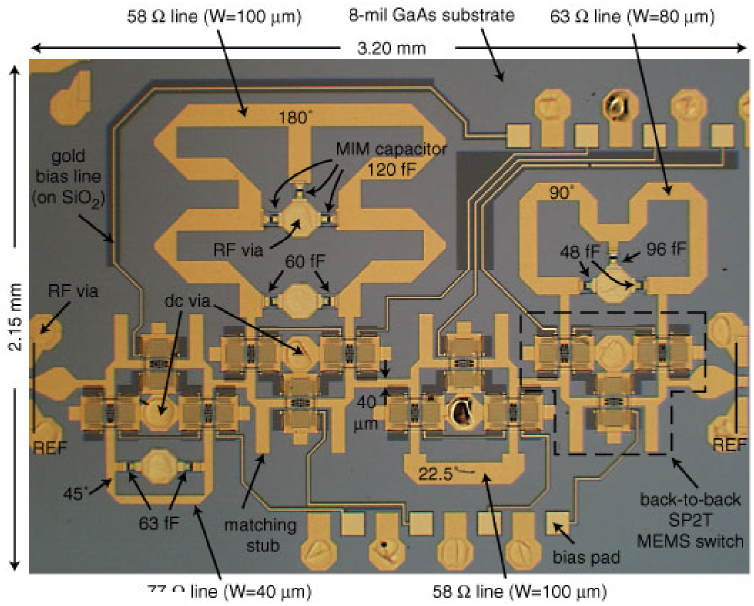
4-bit Miniature X-band MEMS Phase Shifter

- 8-mil (200 um) GaAs or high-rho Silicon substrate
- 7 mm^2 area (smallest MEMS phase shifter to date)
- We can make it 4.5 mm^2 in the next generation



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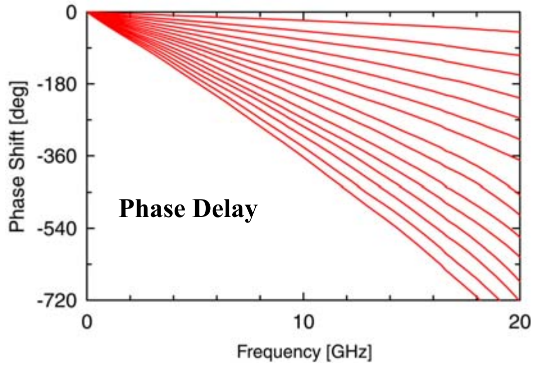
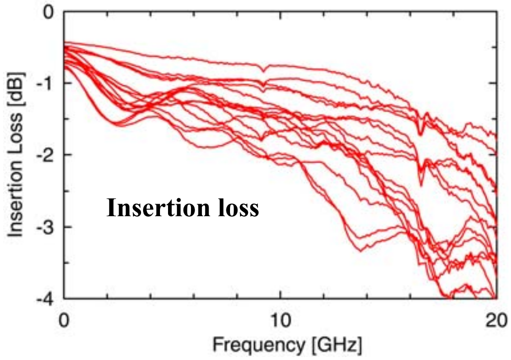
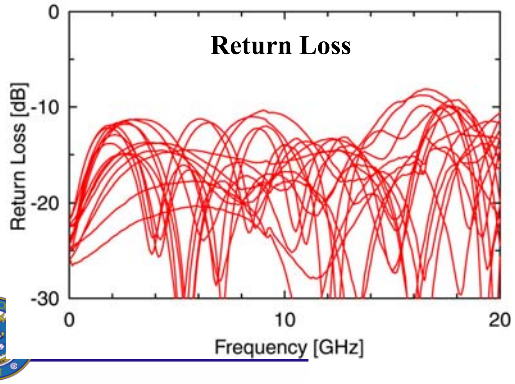
4-bit Mini-MEMS Phase Shifter Measurements







- Substrate=GaAs, h=200 μm
- Area = 7 mm^2 (1.95x2.49mm)

Average loss (16 states):
8.00 GHz = -1.33 dB
9.42 GHz = -1.47 dB
12.0 GHz = -1.64 dB

f_o = 9.42 GHz
Peak phase error = +2.7, -3.3deg,
RMS phase error = 2.05 deg

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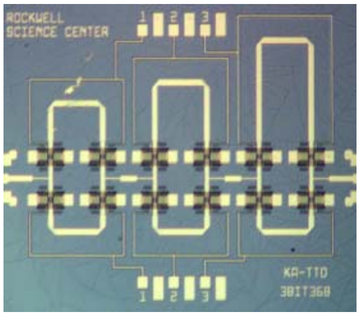
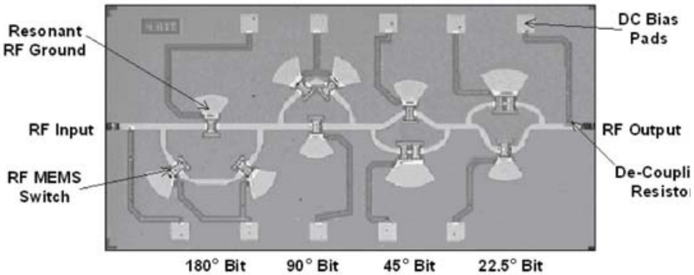
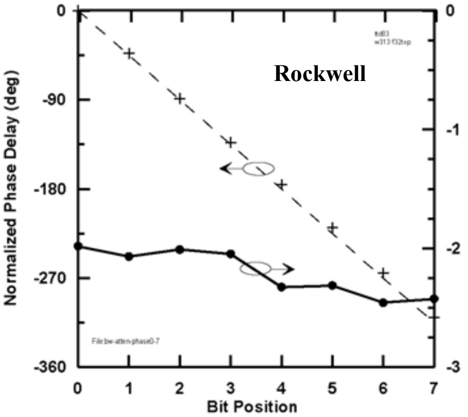
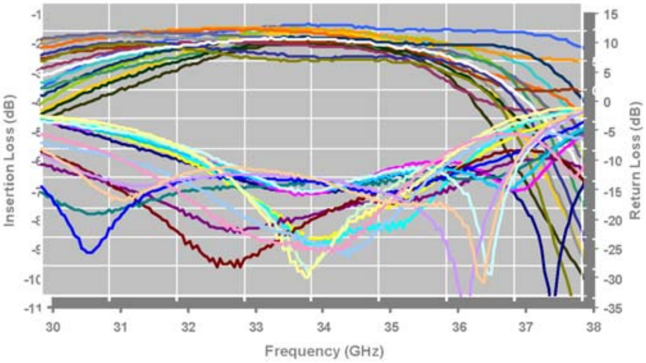
Ka-Band Phase Shifters: Rockwell and Raytheon





Raytheon





- **Loss is 0.65-0.75 dB/bit for both designs**
- **RSC is much more wideband than Raytheon**

Conclusions on RF MEMS Switches and Phase Shifters

- We basically can design any switch or phase shifter up to 200 GHz using RF MEMS.
- At X to Ka-Band, switched T-lines (and switched networks) are best.
- At mm-wave frequencies (60-140 GHz), distributed phase shifters are very good since they are easy to analyze and build. Also, they require a capacitance ratio of 2-3, so high reliability devices can be used.
- As usual, packaging and the package resonance are key in the design. In situ packaging will help a lot.

Review of Tunable Filter Technologies

1) Mechanically Tunable Filters:

- Advantages: Low insertion loss, large power handling
- Disadvantages: Large Size, very slow tuning, heavy

2) Magnetically-Based Tunable Filters (YIG):

- Advantages: Very large tuning range, low insertion loss
- Disadvantages: Medium size, considerable DC power consumption, slow tuning (ms)

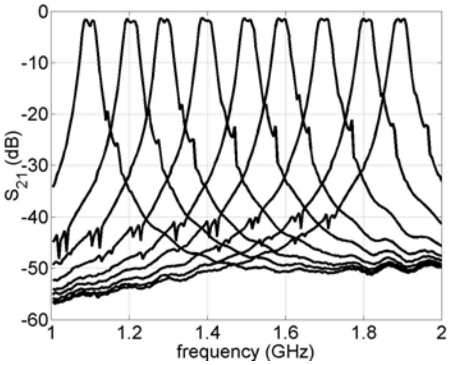
3) Electrically Tunable Filters (Semiconductors, RF MEMS, Ferroelectrics):

- Advantages: Small size, low power consumption, fast tuning (μs)
- Disadvantages: Low Q, high insertion loss, low power handling
- *Research topic: Higher Q, less loss, more tuning, higher linearity*

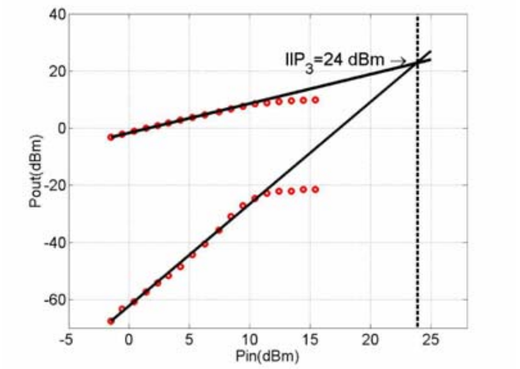
YIG Filters

Two Stage (2-pole), 1-Octave tuning range

BW : 30 MHz, Q_u : 500, IL < 2dB



Filter center frequency: 1.5 GHz



The OMNI-YIG filter

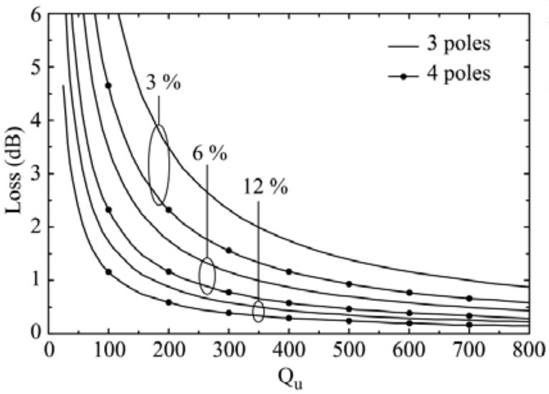
Disadvantages:

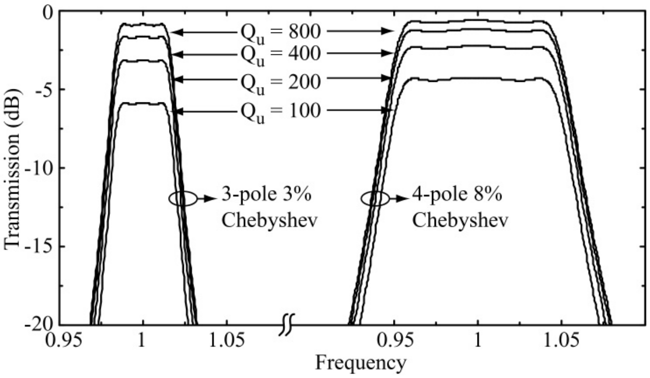
- DC Power Consumption : 1 – 3 W
- Weight (2-pole): 500 gr
- Size (2- pole): 35mm * 35mm * 35mm
- Acceptable linearity

Advantages:

- High Q , Narrow bandwidth
- High tunability (octave)

Filter Performance vs. Resonator Q

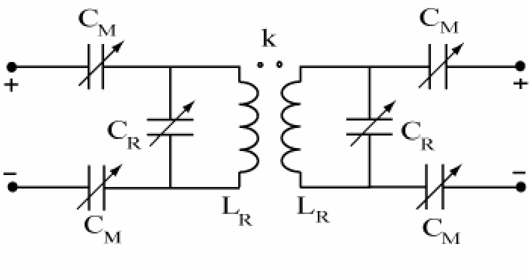




$$\Delta L_A(\text{dB}) \cong 8.686 \frac{c_n}{\varpi Q_u}$$

Tunable Filter Design

Topology: 2-pole band pass filter

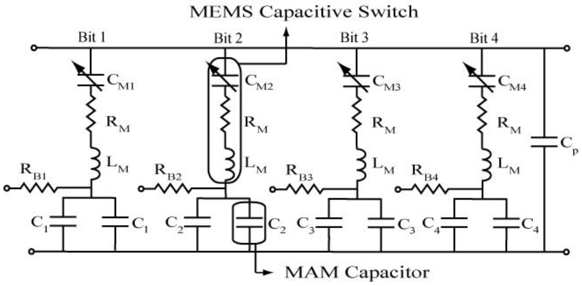


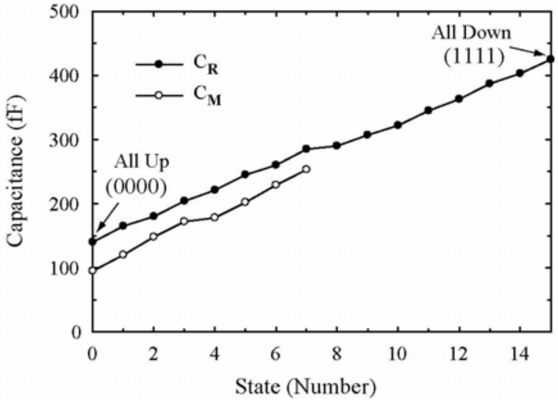
Filter Specs:
- N = 2 (Chebyshev)
- $(\Delta f / f_0) = 0.05$ (5%)
- Freq. range: 6 -10 GHz ,
- Number of states: 16
- Differential (100 Ω)

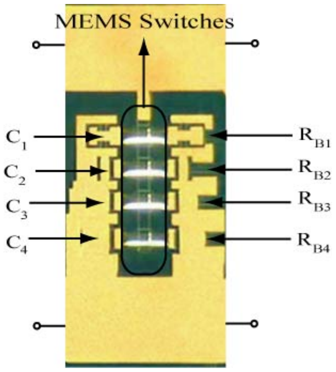
k	0.072
L_R (nH)	1.4
$C_{R(max)}$ (pF)	0.42
$C_{R(min)}$ (pF)	0.14
$C_{M(max)}$ (pF)	0.21
$C_{M(min)}$ (pF)	0.09

Substrate (Glass):
- $\varepsilon_r = 4.6$
- h = 500 μm
- tan (δ) = 0.01

Switched Capacitor Bank Design and Simulations







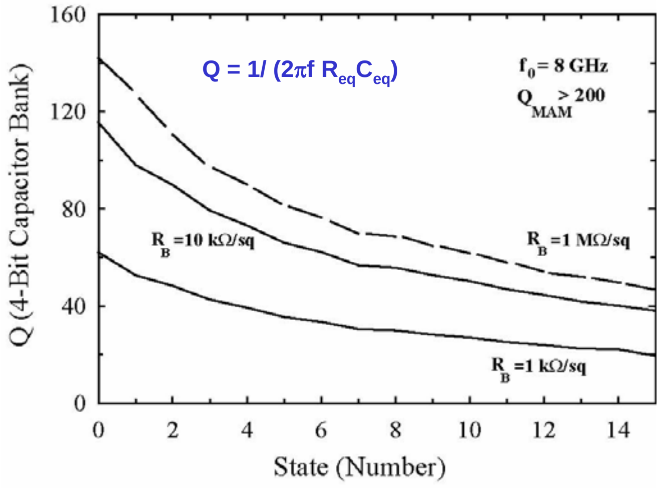
MAM capacitor element values

$C_{1(R)}$ (fF)	**24**
$C_{2(R)}$ (fF)	**35**
$C_{3(R)}$ (fF)	**65**
$C_{4(R)}$ (fF)	**120**
$C_{P(R)}$ (fF)	**35**

MEMS switch element values

$C_{MEMS\text{-}up}$ (fF)	**38**
$C_{MEMS\text{-}down}$ (fF)	**720**
L_M (pH)	**15**
R_M (Ω)	**0.7**

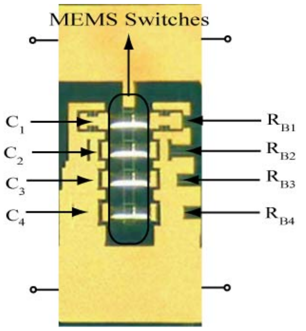
The Effect of Bias Resistance on Capacitor Q


$Q = 1/ (2\pi f\ R_{eq}C_{eq})$

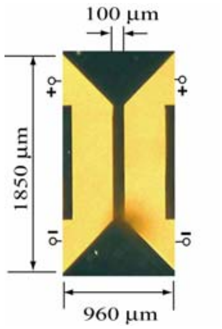
- The bias line resistor has a strong loading effect on the Q of C_R.
- The C_R quality factor doubles for bias line resistance change from 1 kΩ/sq to 10 kΩ/sq.

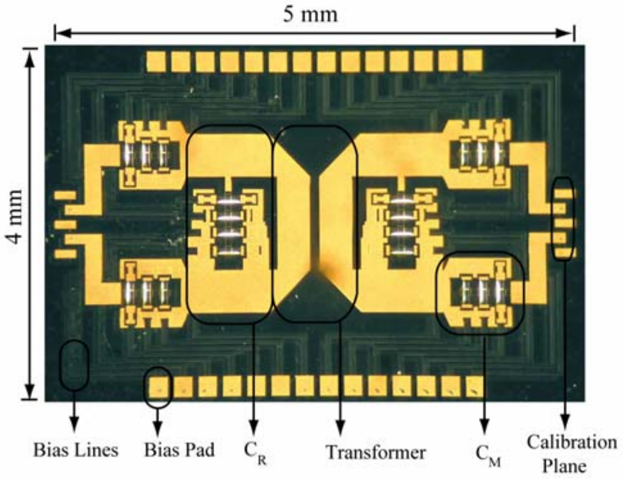
Layouts for capacitor bank, transformer and tunable filter

C_R (4-Bit)



Q_u = 78





- The coupling factor between two resonators is not exactly the same as lumped model, because the coupling is not only from the transformer.

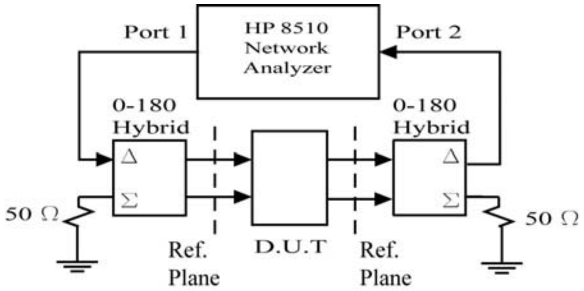
- The amount of desired coupling can be adjusted by the distance between two inductors when the whole resonator is simulated using the MOM.

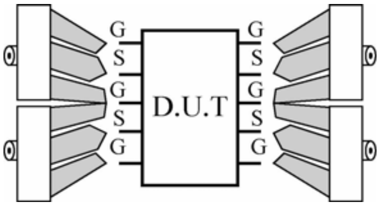
Differential Measurement Setup

Testing Procedure :

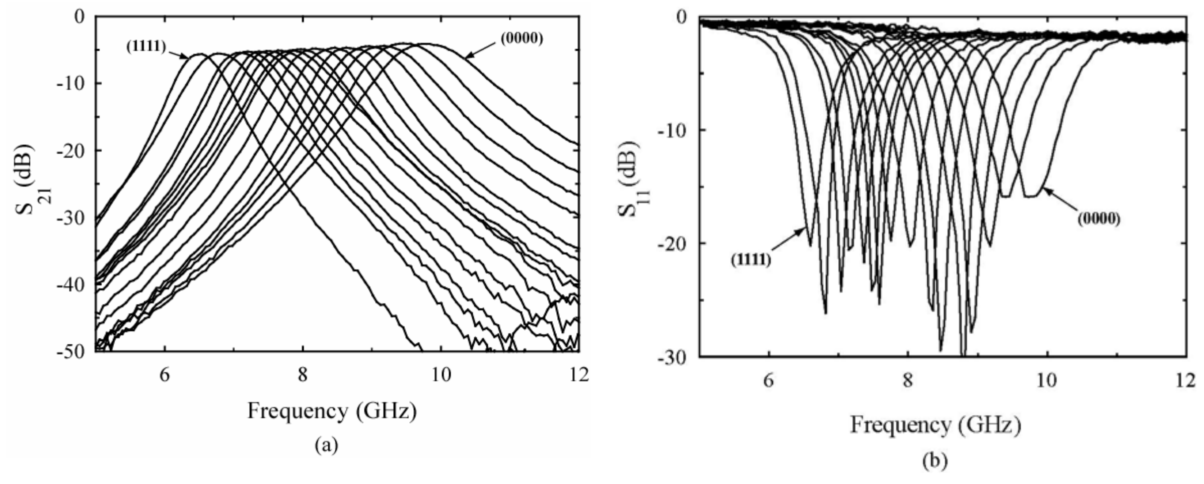
- Fully differential excitation using two hybrid couplers
- Using differential RF probes (GSGSG) for measurement
- Acceptable imbalance for the hybrid couplers:
  - \- Phase imbalance < 10 Degree
  - \- Amplitude imbalance < 2 dB

- A calibration software is used to achieve LRRM differential calibration.





Measured S-parameters for 6-10 GHz Filter

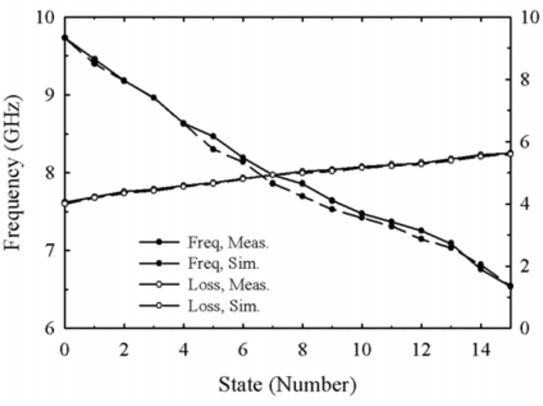


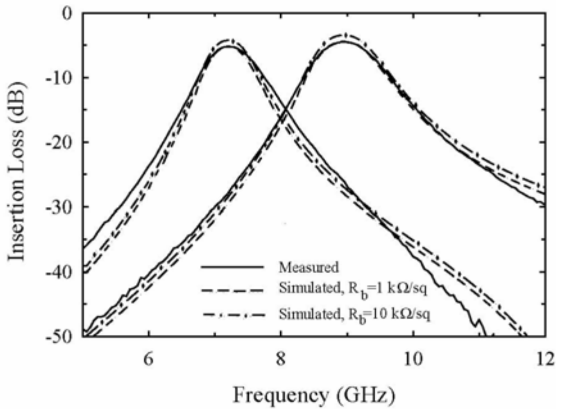
(a)

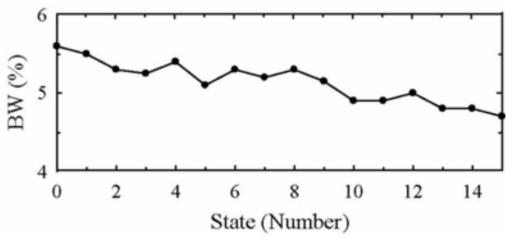
(b)

f (GHz)	(Δf)/f	Q_u	I.L (dB)	R.L (dB)
6.5 (Min)	4.5%	50	5.6	> 18
9.8 (Max)	5.0%	60	4.1	> 15

Comparison Between Simulation and Measurement







- **Insertion loss for two arbitrary states:**
  - **- State 13 (7.1 GHz)**
  - **- State 4 (8.6 GHz)**

RF MEMS Mechanical Model

- **Static model of a MEMS switch/varactor**

- **Capacitance**: $C = \varepsilon_0 \varepsilon_r \frac{wW}{x} + C_f$

- **Electrostatic Force**: $F = \frac{CV^2}{2x}$

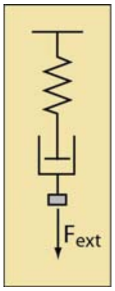
- **Displacement**: $\Delta x = \frac{F}{k}$

- **Pull-down voltage**: $V_P = \sqrt{\frac{8kg_0^2}{27C_0}}$

- **Dynamic model of a MEMS switch/varactor**

- **Dynamic Mechanical Response**:

$$m\frac{d^2x}{dt^2} + b\frac{dx}{dt} + kx = f_{ext}$$

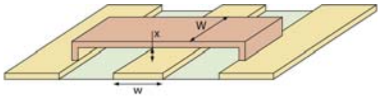


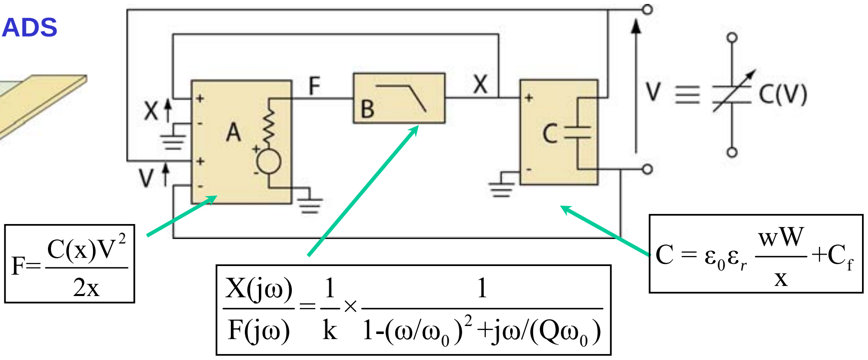
- **Frequency domain**:

$$\frac{X(j\omega)}{F(j\omega)} = \frac{1}{k} \times \frac{1}{1-(\omega/\omega_0)^2 + j\omega/(Q\omega_0)}$$

$$\text{with } \omega_0 = \sqrt{\frac{k}{m}} \text{ and } Q = \frac{k}{b\omega_0}$$

- **Nonlinear Model in ADS**



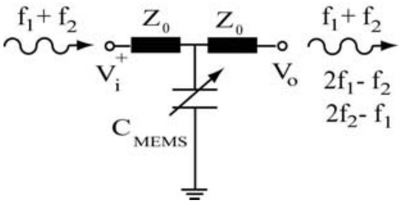


$$F = \frac{C(x)V^2}{2x}$$

$$\frac{X(j\omega)}{F(j\omega)} = \frac{1}{k} \times \frac{1}{1-(\omega/\omega_0)^2 + j\omega/(Q\omega_0)}$$

$$C = \varepsilon_0 \varepsilon_r \frac{wW}{x} + C_f$$

RF MEMS Switch Nonlinear Analysis



$C(t) = C_0(1- \Delta x(t)/x)$, $\phi(t) = \phi_0 (1- \Delta x(t)/x)$

$\Delta x(t) = F / k = C_0 V_i^{+2} /2x$

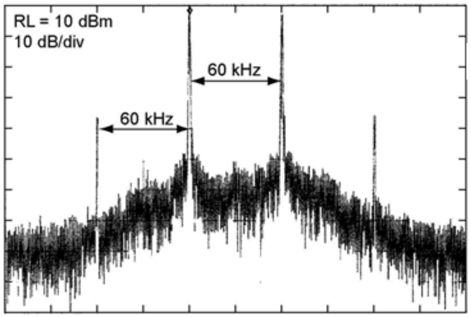
$V_i^+ = V(\sin(\omega_1 t) + \sin(\omega_2 t))$

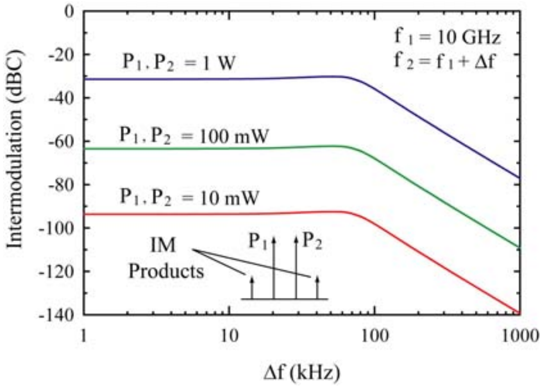
$V_0 = V_i^+ S_{21} = V_i^+ e^{j\phi(t)}$

$\phi(t) = - (1/2)\omega_0 Z_0 C(t)$

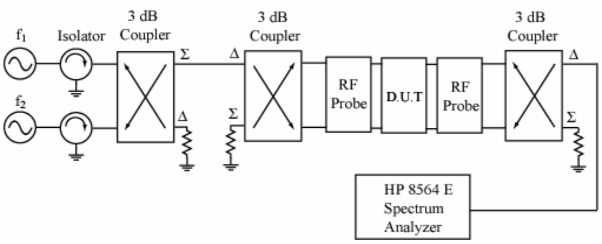
$V_o \sim V(\sin(\omega_1 t) + \phi_0)$, $V(\sin(\omega_2 t) + \phi_0)$,
$V^3(\cos(2\omega_1 - \omega_2)t + \phi_0)$, $V^3(\cos(2\omega_2 - \omega_1)t + \phi_0)$

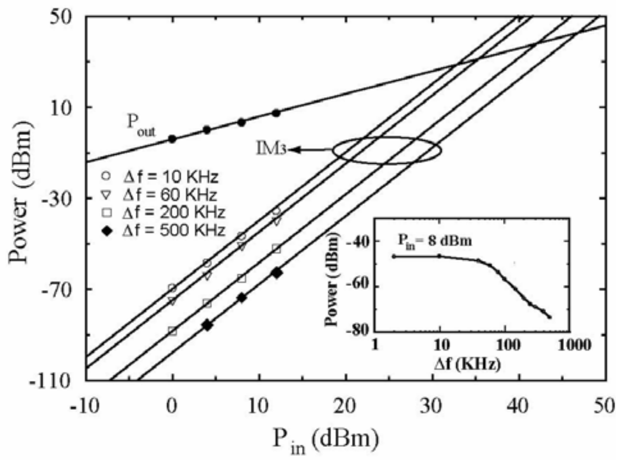
- **Intermodulation test (f = 10 GHz)**





Nonlinear Measurement, Power Handling

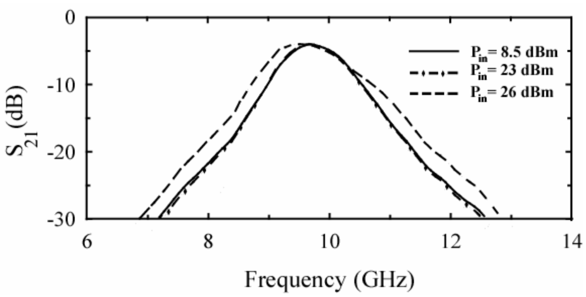


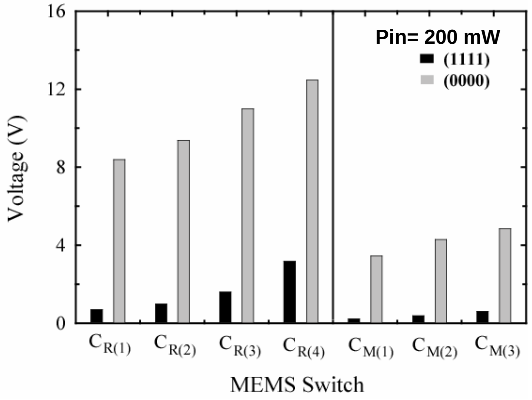


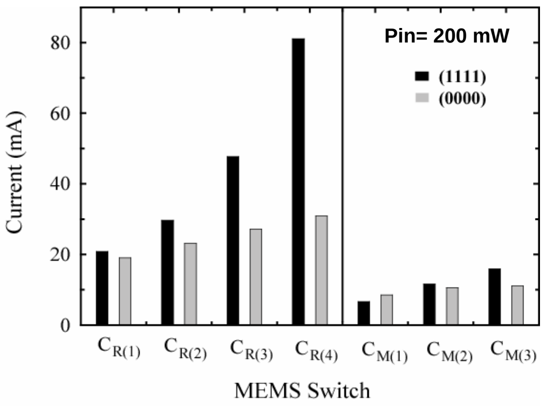
- Amazing Linearity: IIP3> 45 dBm for Δf > 500 KHz measurement in the up-state
- IIP3 > 60 dBm for Δf > 2 MHz
- This filter can handle an input power up to 24 dBm (250 mW).
- for Pin > 24 dBm (250 mW) self-biasing occurs.

High Power Analysis and Measurement

Filter is limited by voltage level on switches and not by current. Voltage self-biases the MEMS capacitors and changes the filter response.

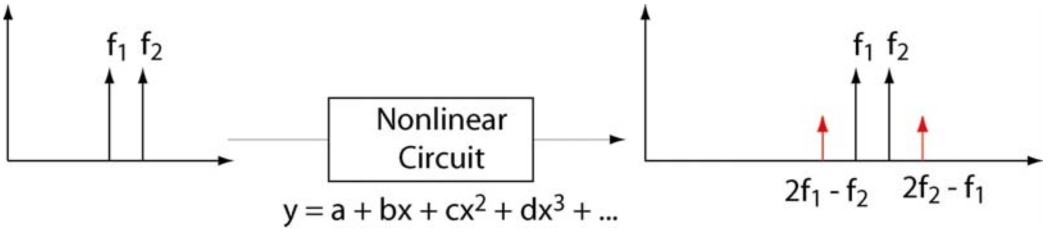






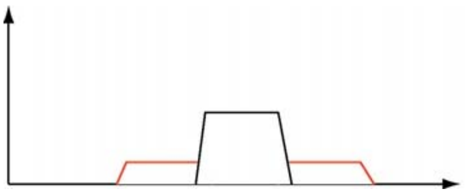
The Impact of RF MEMS on the system-level performance

- Two-tone intermodulation products generation:

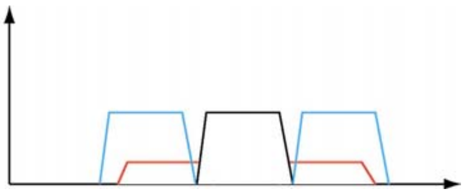


- Consequences**:**

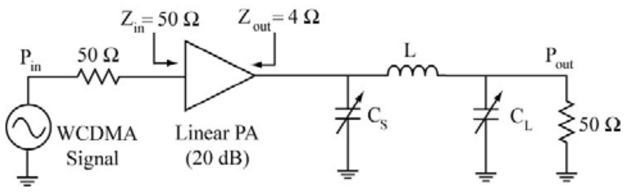
- Spectrum regrowth



- Inter-channel interference

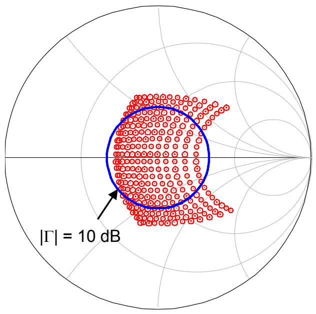


Impedance Tuner Implementation

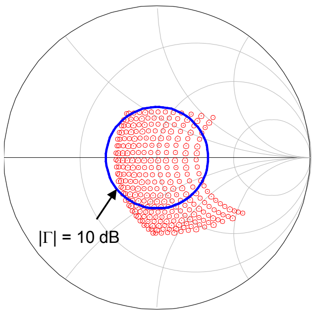


Center frequency: 1.95 GHz
Chip Rate : 3.84 Mcps
Z_{Load}= 50 Ω, Z_{out} = 4 Ω
C_S = C_L = 5.7 pF
L= 1.15 nH

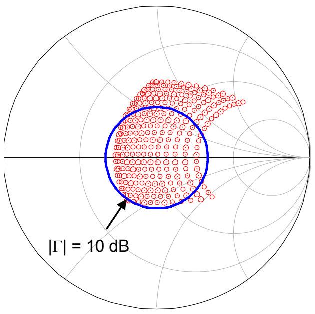
- **PA output impedance variation : between 2 +/- j4 Ω and 6 +/- j4 Ω**
- **The PA output impedance is matched to 50 Ω load better than 10 dB by changing CL and CS between 5.2 and 6.4 pF.**



C_s = C_L = 5.7 pF

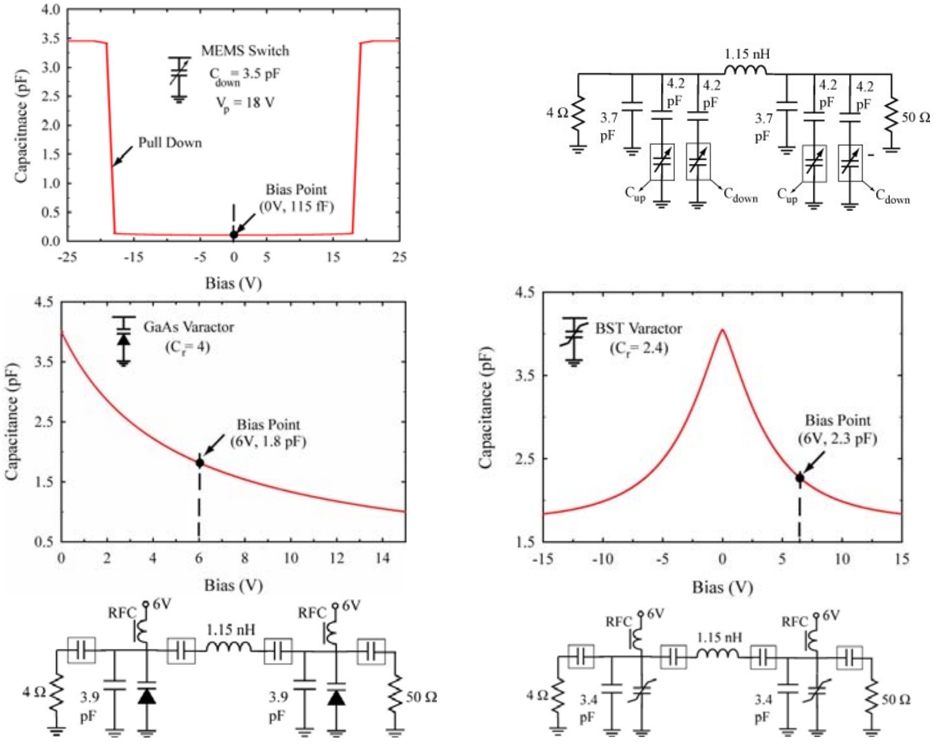


C_s = C_L = 5.2 pF



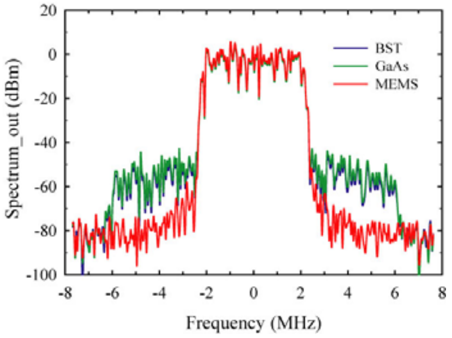
C_s = C_L = 6.4 pF

GaAs, BST and RF MEMS Impedance Tuners

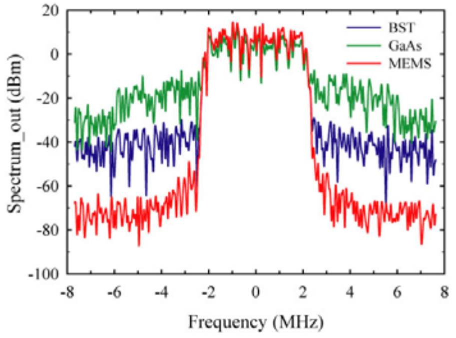


WCDMA Spectral Distortion by Impedance Tuners

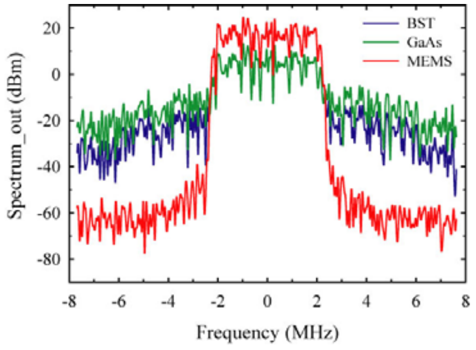
P_{in} = -10 dBm, P_{Load} = 10 dBm



P_{in} = 0 dBm, P_{Load} = 20 dBm



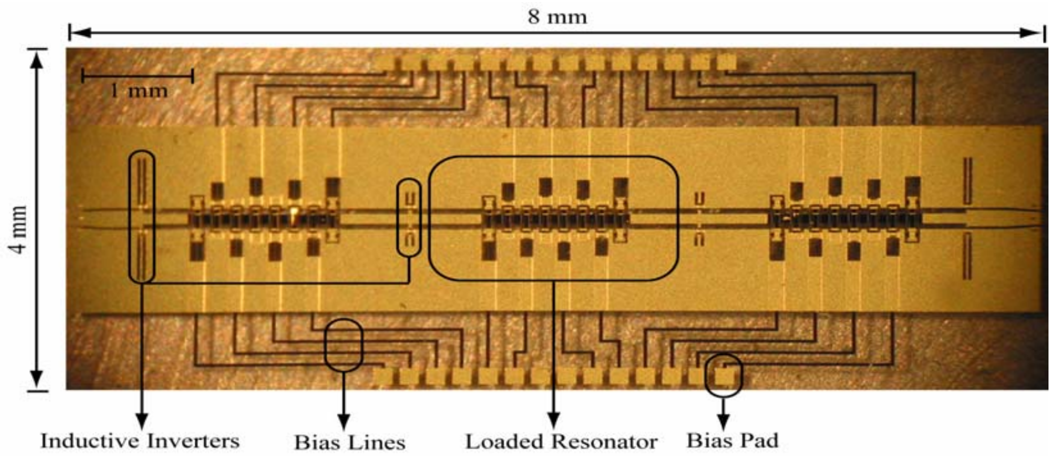
P_{in} =10 dBm, P_{Load} (GaAs)= 20 dBm, P_{Load}(BST,MEMS) = 30 dBm



- **Increasing the input power results in a strong spectral re-growth for BST and GaAs impedance tuners due to their non-linear behavior.**

- **The output power of the GaAs tuner is compressed for 10 dBm input power.**

Fabricated 12-18 GHz Tunable Filter

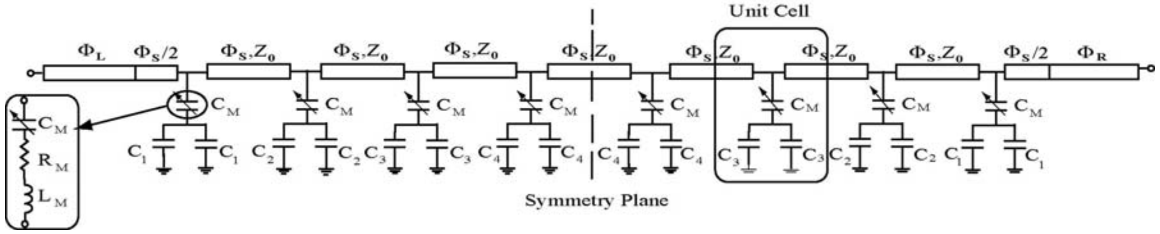


Substrate (Glass):
- $\varepsilon_r = 4.6$
- h = 500 µm
- tan (δ) = 0.01

CPW Line:
- $Z_C = 77\ \Omega$
- G / W / G : $(70^{\mu} / 120^{\mu} / 70^{\mu})$
- $\varepsilon_{r\text{-eff}} = 2.8$
- $\alpha = 42$ dB/m (f = 18 GHz)
- $Q_u = 65$
- $Z_A = 50\ \Omega$

Filter Specs:
- N = 3 (Chebyshev)
- $(\Delta f / f_0) = 0.06$ (6%)
- Freq. range : 12-18 GHz
- Number of states : 16
- Single ended (50 Ω)

Single Loaded Resonator Design

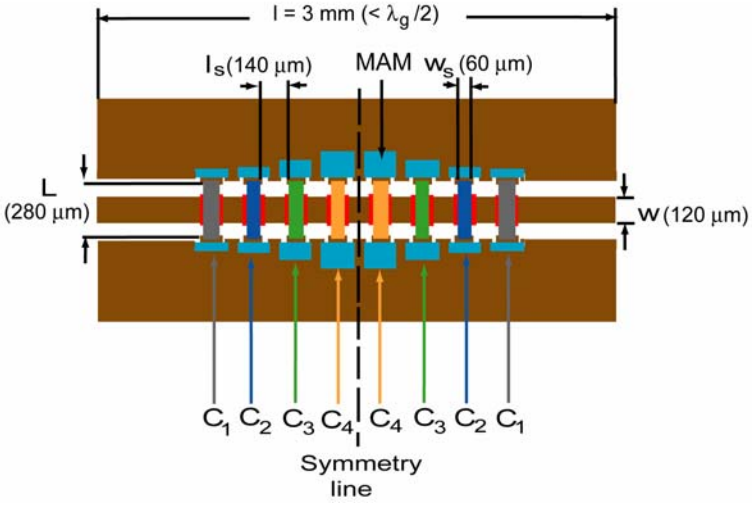


MAM capacitor element values

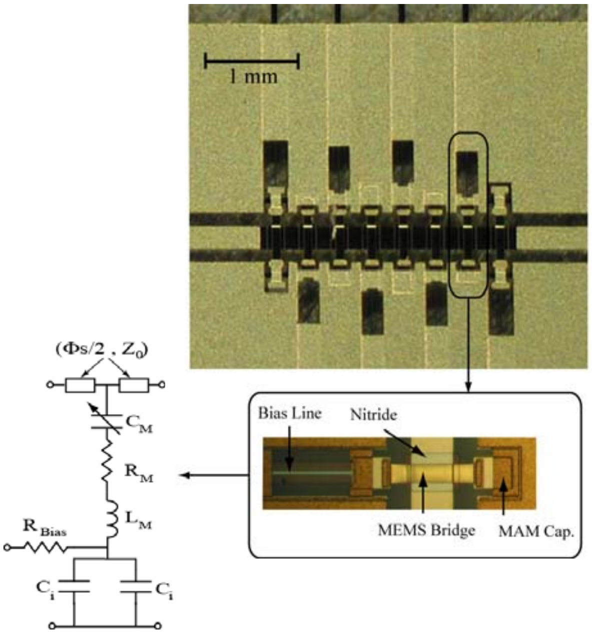
C_1 (fF)	26
C_2 (fF)	31
C_3 (fF)	43
C_4 (fF)	59

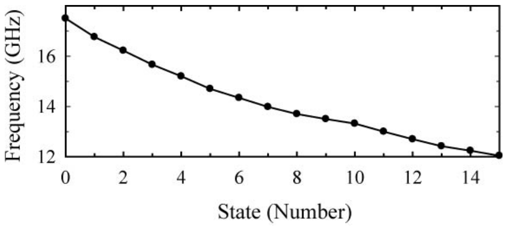
MEMS switch element values

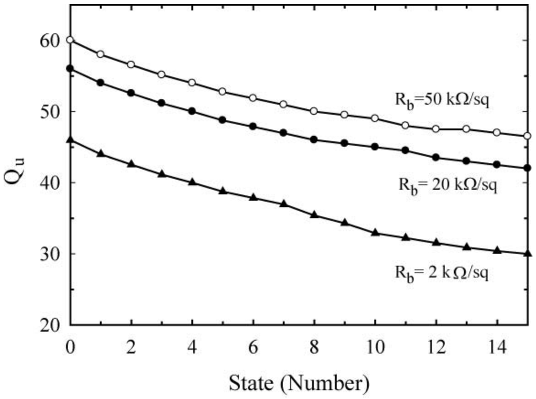
$C_{MEMS\text{-}up}$ (fF)	50
$C_{MEMS\text{-}down}$ (fF)	1350
L_M (pH)	15
R_M (Ω)	0.7



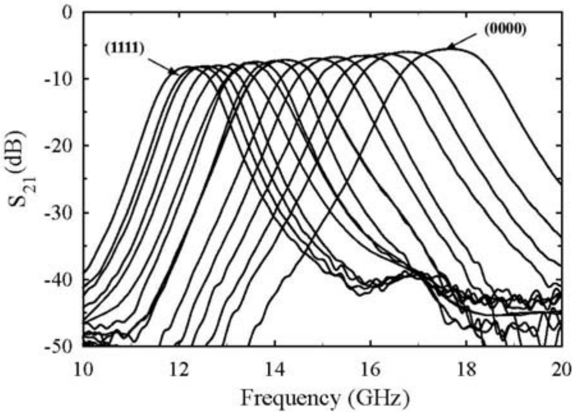
Resonator Characterization

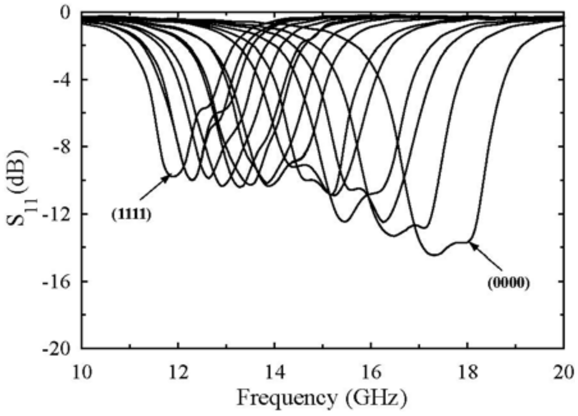




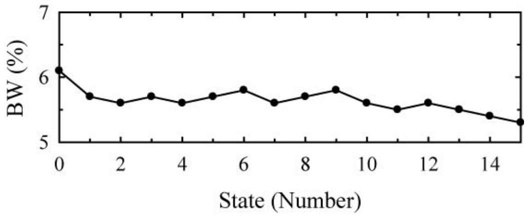


Measured S-Parameters for 12-18 GHz Filter



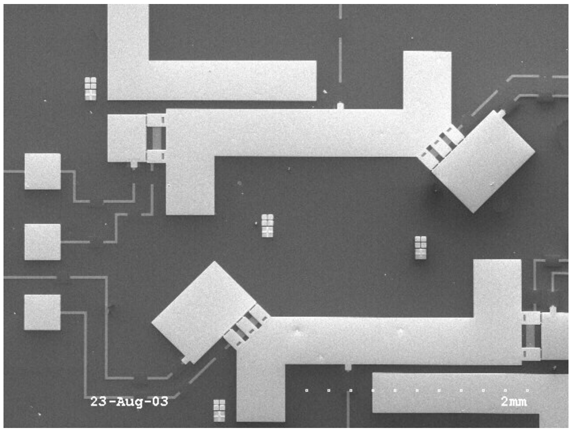


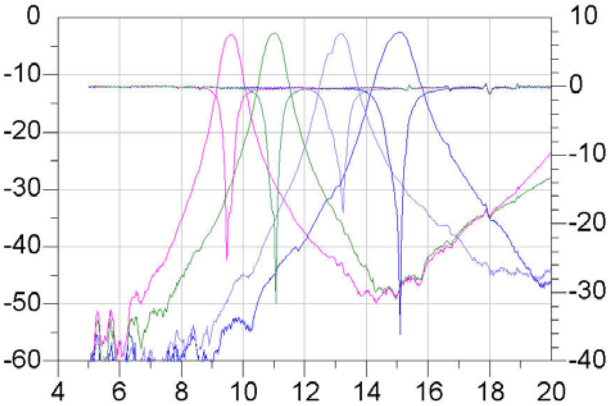
f (GHz)	(Δf)/f	I.L (dB)	R.L (dB)
17.8 (max)	6.1%	5.5	> 14
12.2 (min)	5.3%	8.2	> 10



2-Bit Metal Contact Tunable Filter

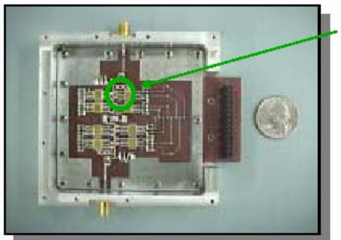
Limoges Group in France



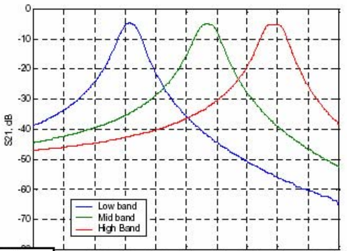


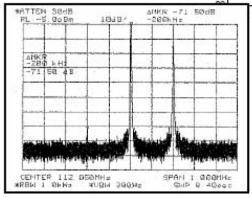
Switched-Capacitor Tracking Filter

MNT-A1-4/14/00-11

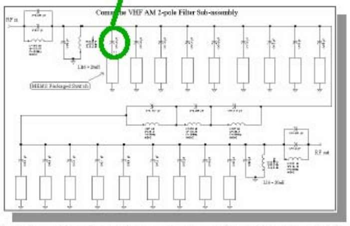


16 MEMS switches in 8 packages





Measured S-parameter (above) and Filter intermodulation (left) for 2-Pole Filter with MEMS Switch



Schematic of switched-capacitor tracking filter

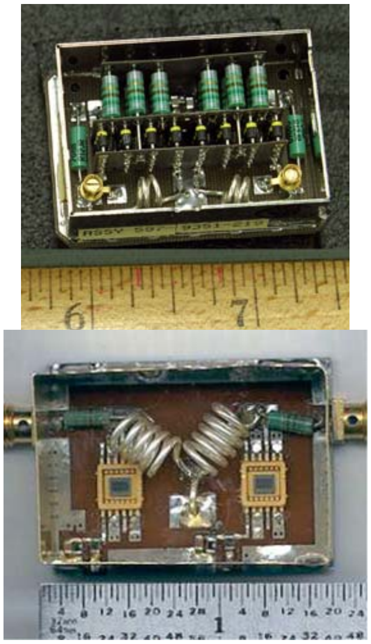
Demonstrated system benefits:

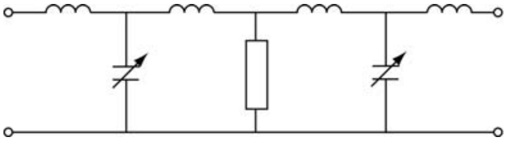
- 500x improvement in linearity
- 42% parts count reduction
- static power reduced from 1.5W to near-zero

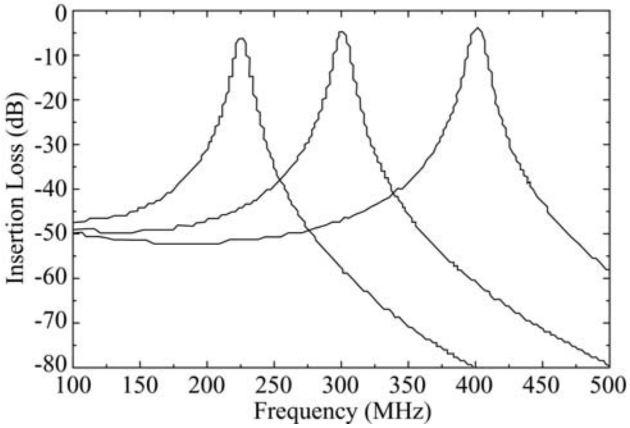
Rockwell
Collins

Rockwell
Science Center

Rockwell 2-pole 240-360 MHz Tunable Filter



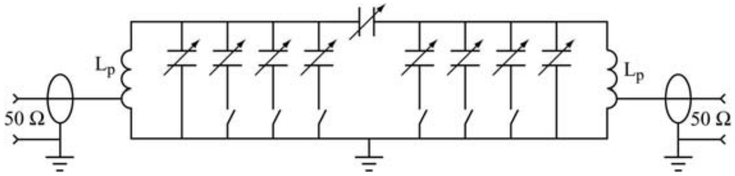




- Dramatic (90%) parts count reduction validated for MEMS circuit
- Higher loss at low frequency due to reduced capacitor Q

ROCKWELL SCIENTIFIC

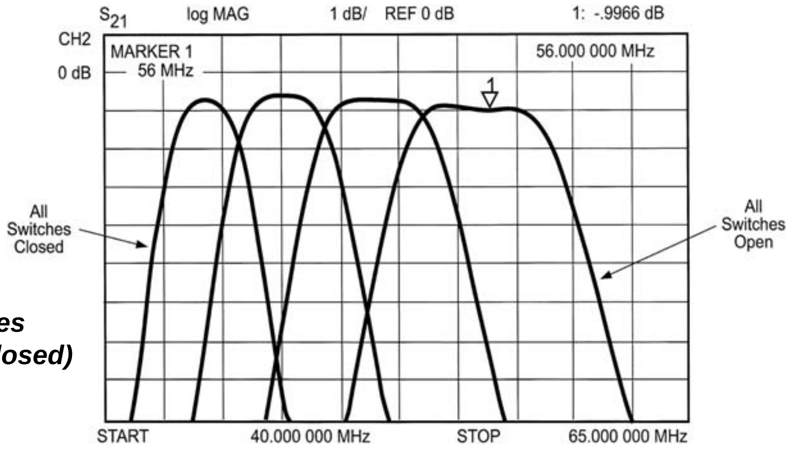
Raytheon 2-pole 44-56 MHz High-Power Filter



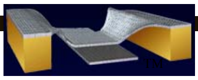
Work done at Raytheon-Illinois

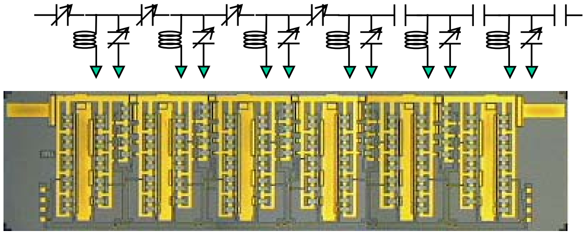
- **Cronos thermal switches**
- **Filter bandwidth: 10-11%**
- **High Q Cap and Ind. used**
- **As usual, loss is limited by switch Rs and Cap/Ind. Q**

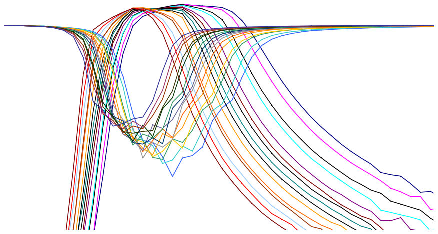
- ***Tested at 25 W for 53 M cycles***
- ***150 Vrf (open) and 0.2 Arf (closed)***
- ***Hot switched !***



Raytheon

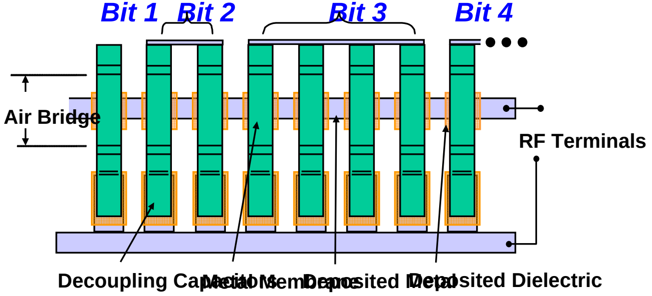


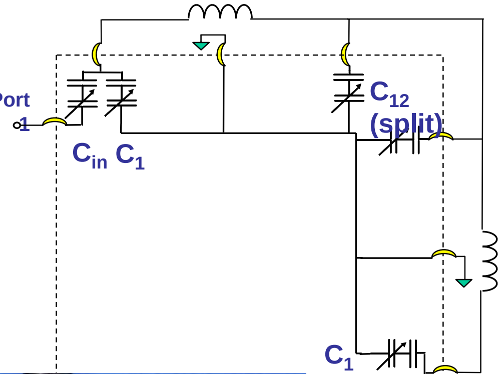


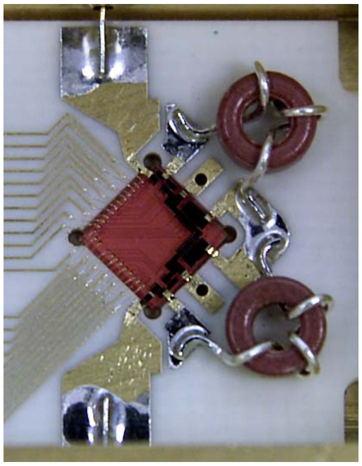


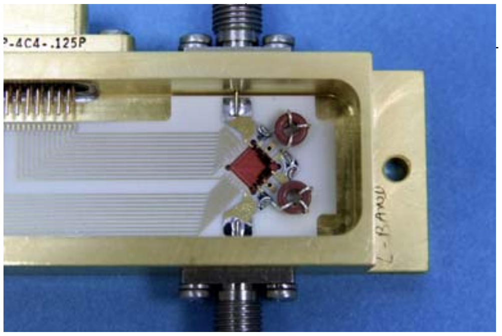
Raytheon

N-G L-Band Filter topology MEMS Tunable Filter



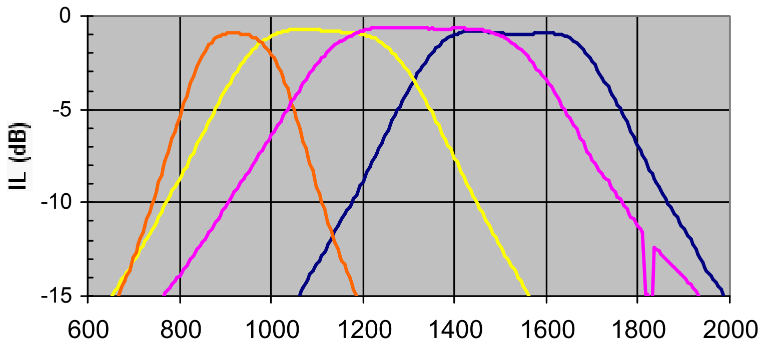




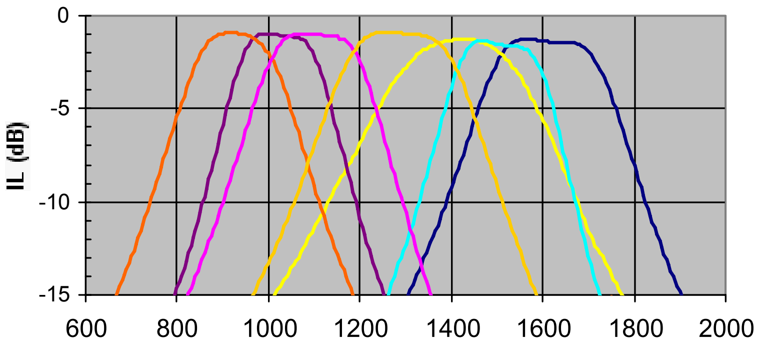


NORTHROP GRUMMAN

L-Band MEMS Tunable Filter
Variable Center Frequency



- One Octave Tuning
  - 812 to 1750 MHz
- Low Insertion Loss
  - -0.6 to -0.9 dB
- Good Return Loss
  - -15 dB typ.
- Bandwidth (3dB) 7 to 40%

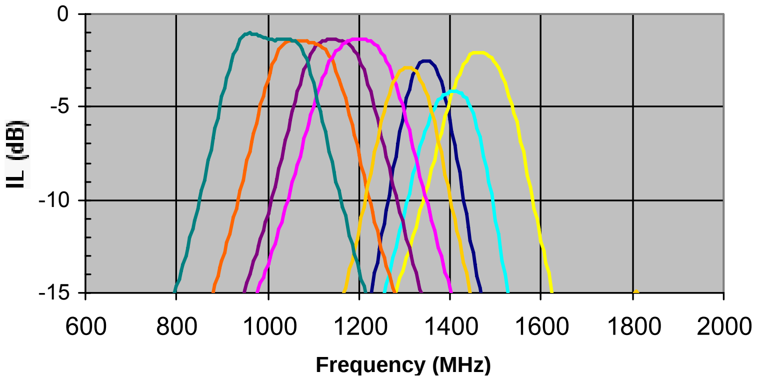


- One Octave
- -1dB Insertion Loss typical
- Medium Bandwidth

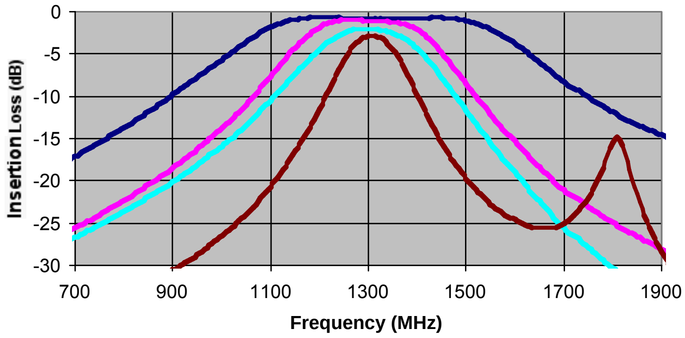
NORTHROP GRUMMAN

Variable Center Frequency (Narrow) and Bandwidth Control

- 4-bit tuning
  - More bits would close gaps in coverage
- -1 to -4 dB I.L.

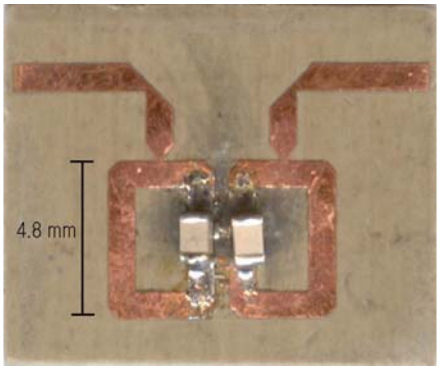


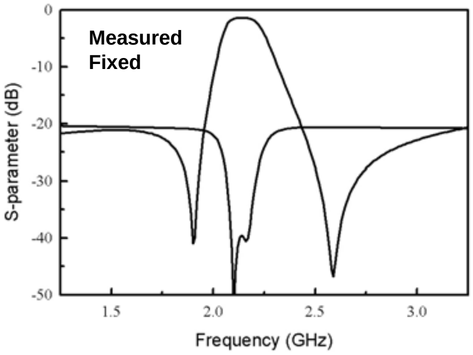
- Bandwidths 9 to 42%
- 2nd peak for narrowest band
- Insert. Loss -0.6 dB to -2.9 dB
- Ret. Loss shows large dissipation for narrowest band
  - Metal thickness & skin depth

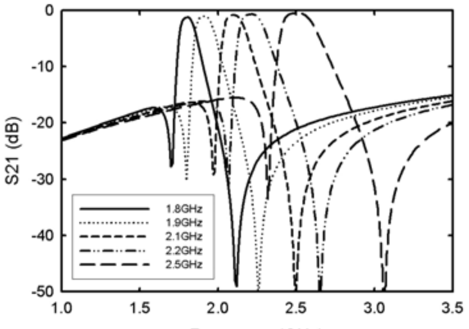


NORTHROP GRUMMAN

1.6-2.5 GHz Tunable Filter (Ring Tapped Input)





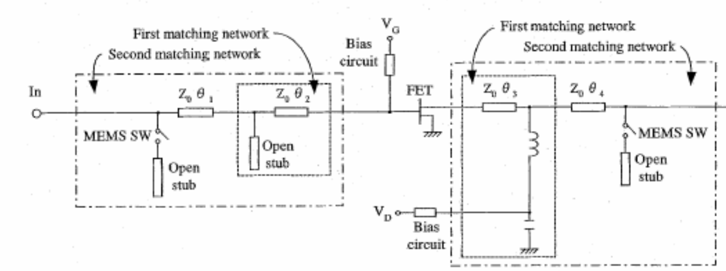


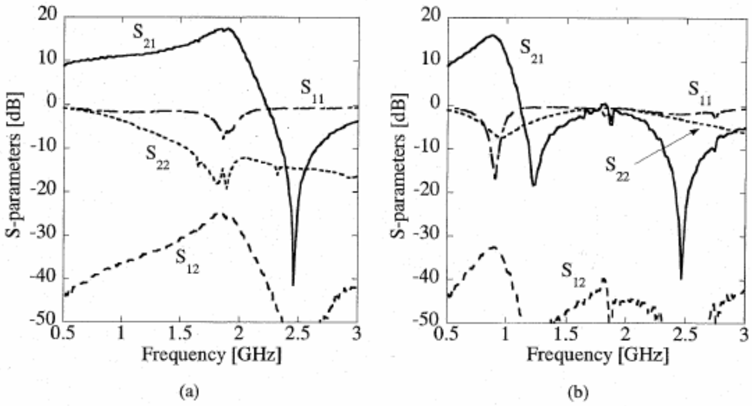
- **Fabricated on Duroid substrate (ε_r=10)**
- **Overall size 4.8 mm x 5 mm**
- **Chip capacitors are used**
- **Insertion loss -1.4 dB (Q=160)**
- **Measured bandwidth 4% (single filter)**

- ***Tunable filter graphs are simulations***
- ***Cr=3 (only!) for a 1.7-2.5 GHz tuning***

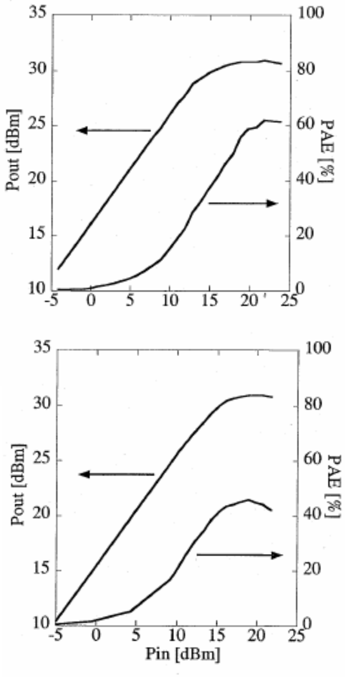
Dual Band (900/1900 MHz) Power Amplifier by NTT

Equivalent circuit





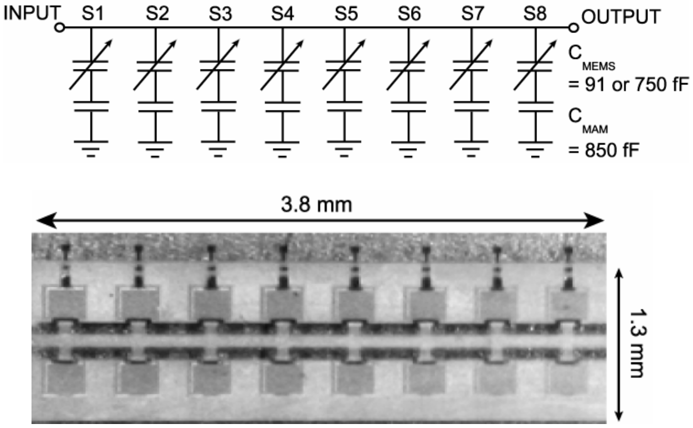
(a) (b)



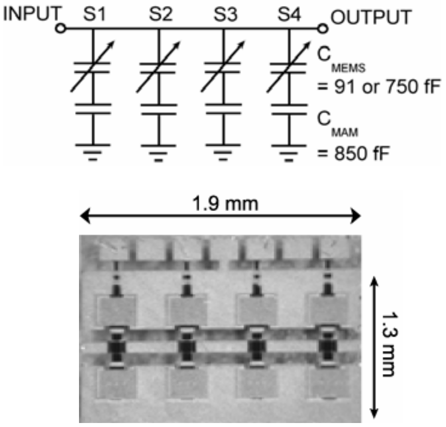
(b)

Matching Networks for 4-20 Power Amplifier Applications

8-element network

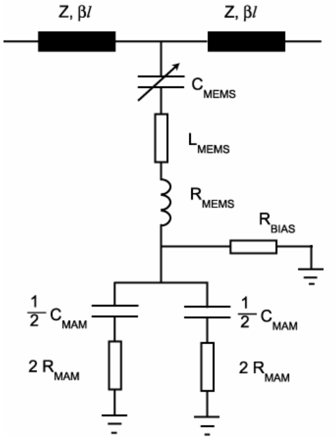


4-element network



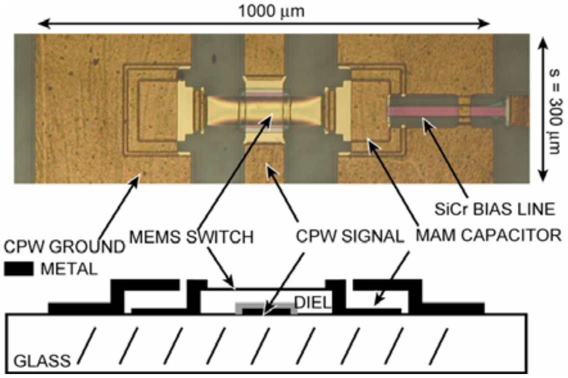
Switched Capacitor: MEMS Switch and MAM Capacitor

Equivalent circuit



C_{MEMS}: C_{UP} (fF)	91
C_{MEMS}: C_{DOWN} (fF)	750
R_{BIAS} (kΩ)	> 3
L_{MEMS} (pH)	9.5
R_{MEMS}+ R_{MAM} (Ω)	0.6
C_{MAM} (fF)	850

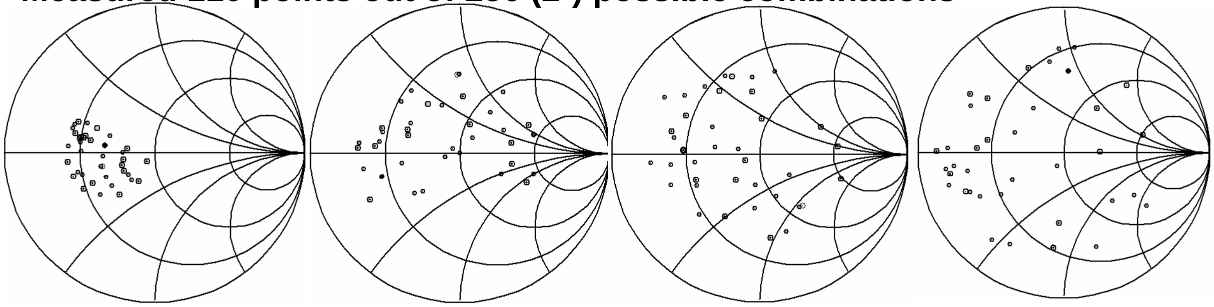
Fabricated Switched Capacitor



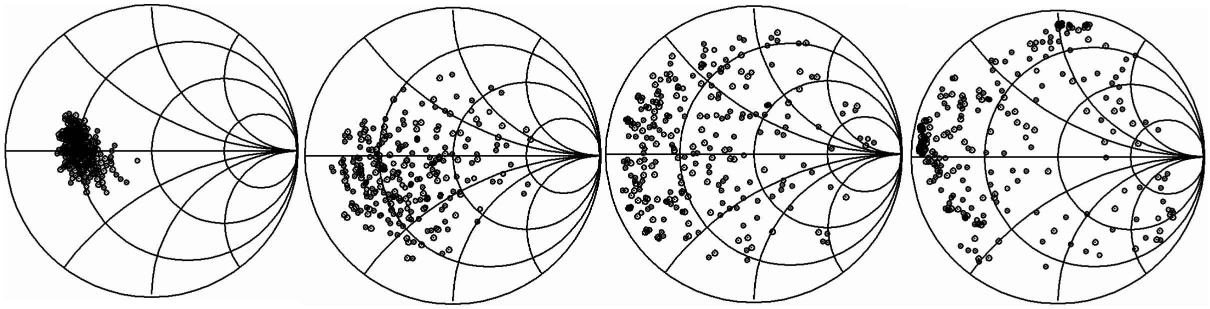
ε_r	4.6
Z_0 (Ω)	86.2
ε_{reff}	2.72
α(dB/cm),10/20 GHz	0.35/0.52
s (µm)	480
Z_U (Ω),ε_{reff_U}	45, 10
Z_D (Ω),ε_{reff_D}	23, 38

8-Element Network: Impedance Coverage

Measured 110 points out of 256 (2^8) possible combinations



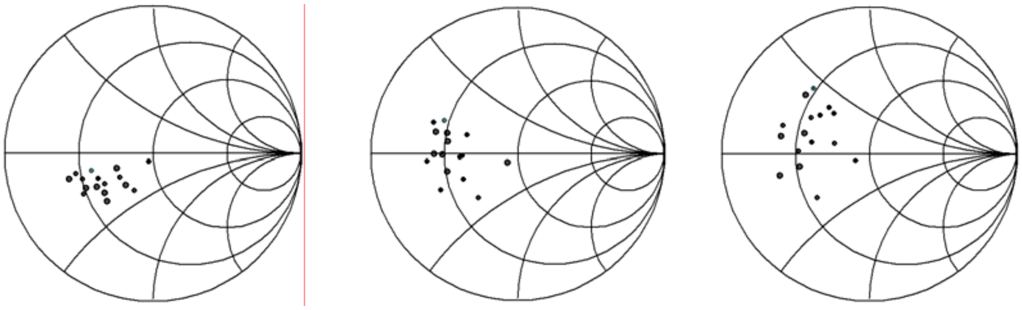
Meas. 4.1 GHz Meas. 10 GHz Meas. 17.8 GHz Meas. 26.2 GHz



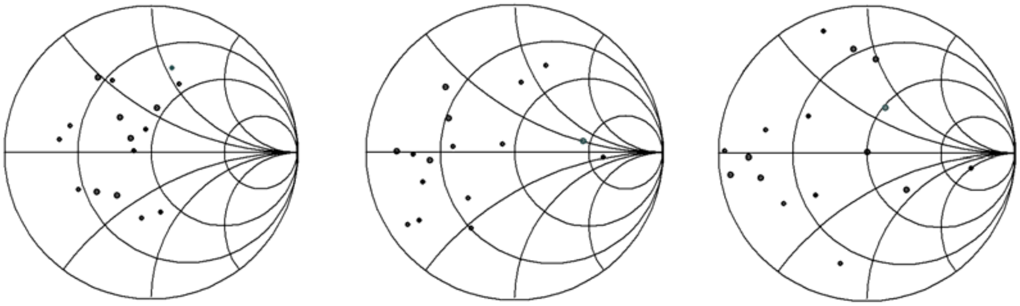
Sim. 4.1 GHz Sim. 10 GHz Sim. 17.8 GHz Sim. 26.2 GHz

4-Element Network: Impedance Coverage

Measured 16 points



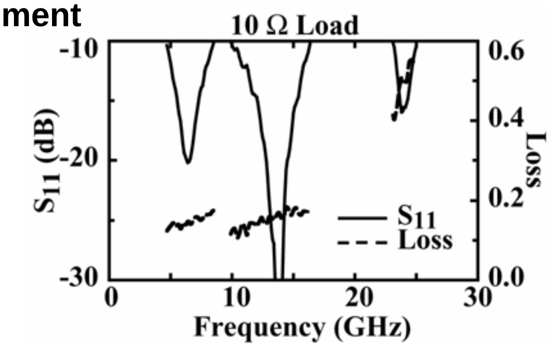
4.1 GHz 8.1 GHz 10.1

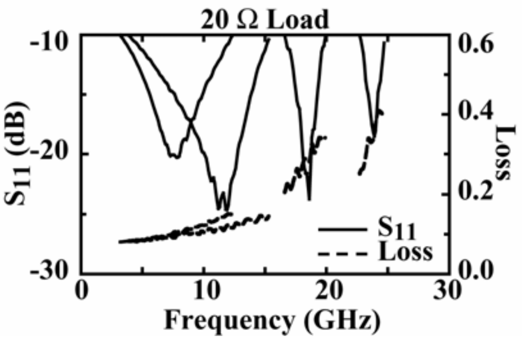


14.1 GHz 18 GHz 24.2 GHz

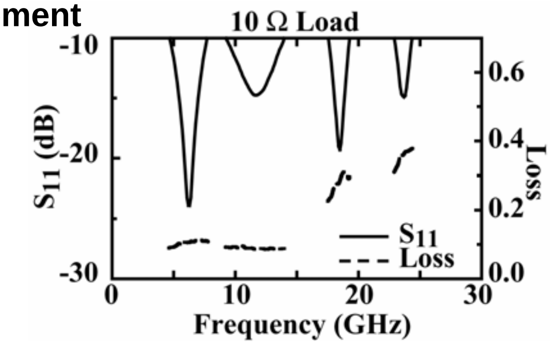
Case Study: Matching of 10 and 20 Ω Loads to 50 Ω

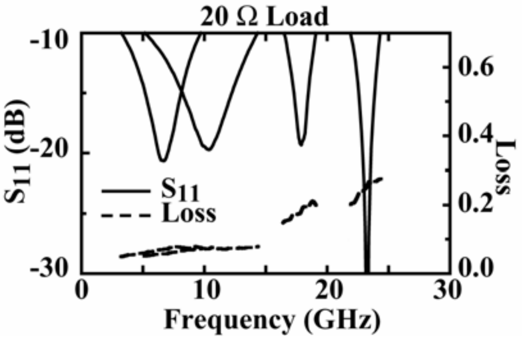
8-Element





4-Element

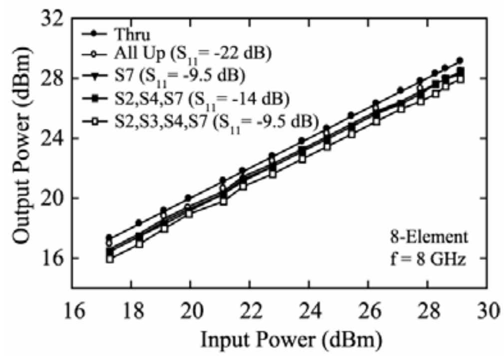


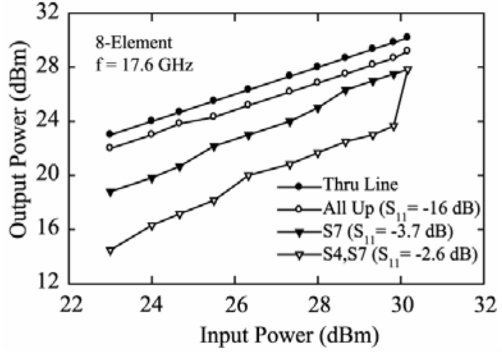


RF Power Handling Measurements: 8 and 17.6 GHz

Output power as a function of input power

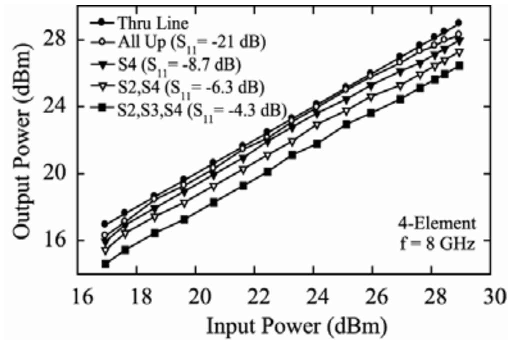
8-Element

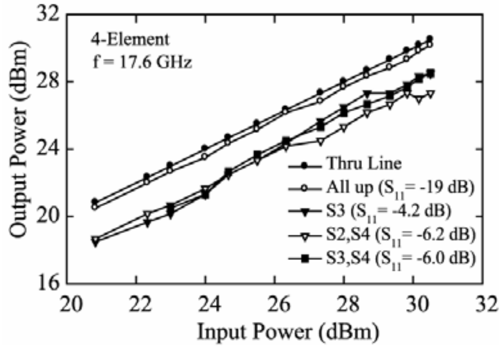




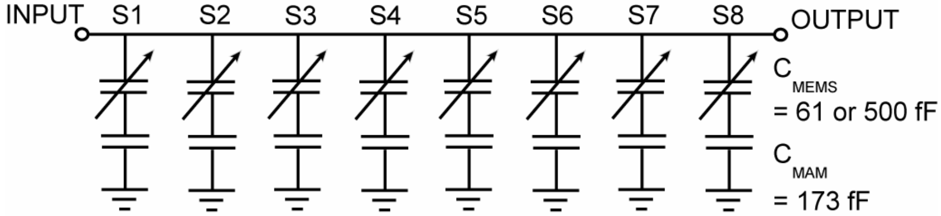
4-Element

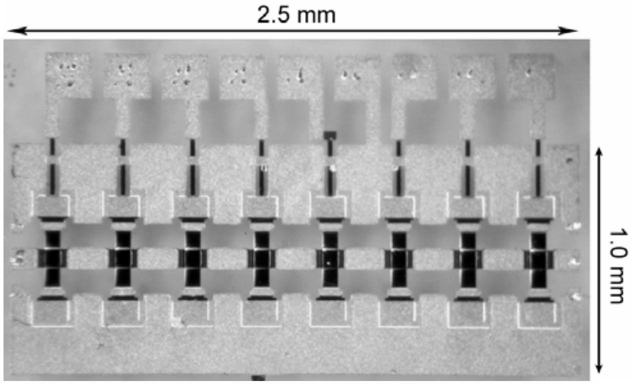
>1 W power handling





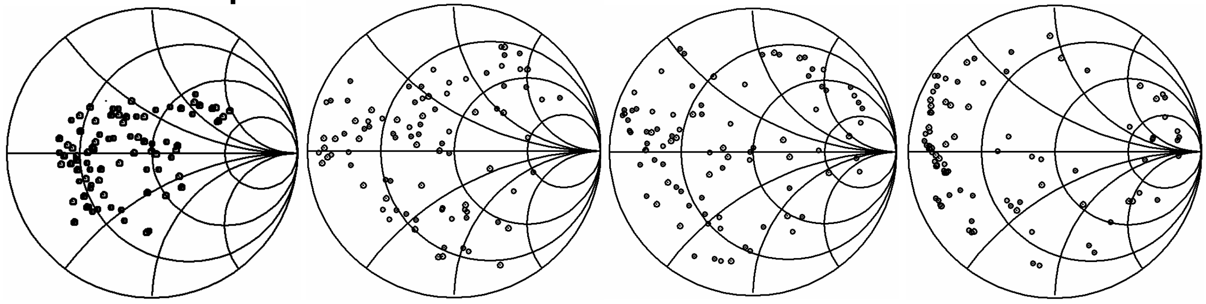
Ka-Band Reconfigurable Network with 8 Switched Capacitors



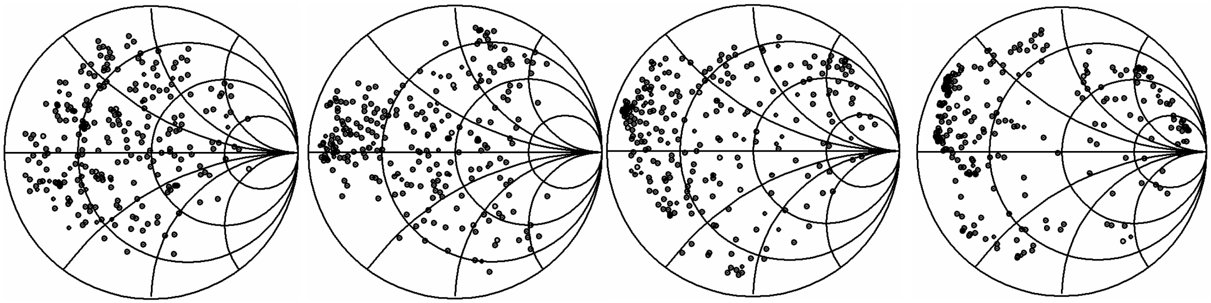


Impedance Coverage (2)

Measured 90 points out of 256 (2^8) possible combinations

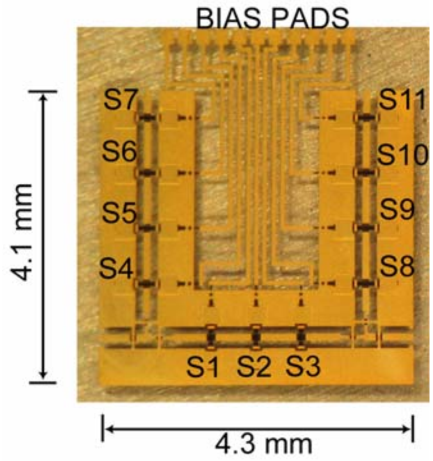


Meas. 40.3 GHz **Meas. 50 GHz** **Meas. 54.9 GHz** **Meas. 60.1GHz**



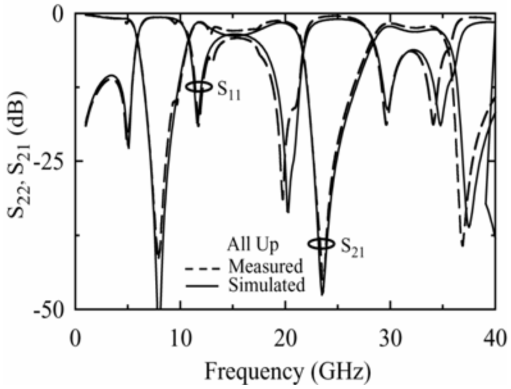
Sim. 40.3 GHz **Sim. 50 GHz** **Sim. 54.9 GHz** **Sim. 60.1GHz**

Double-Stub Tuner with 11 Switched Capacitors for 6-20 GHz Applications

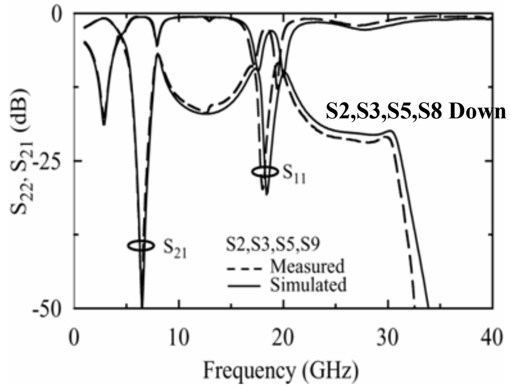


2048 (2^{11}) different impedances can be generated

All switches up

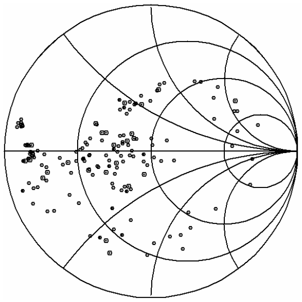


S2,S3,S5,S8 Down

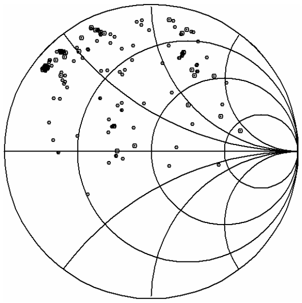


Impedance Coverage of the Double-Stub Tuner

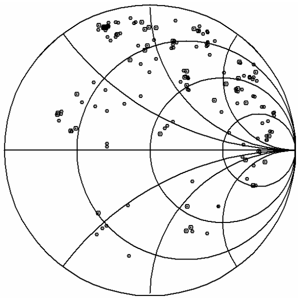
Measured 160 points out of 2048 (2^{11}) possible combinations



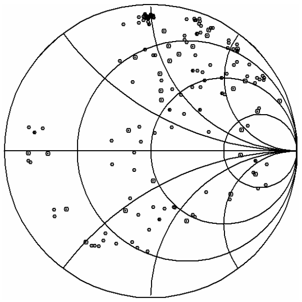
Meas. 4.1 GHz



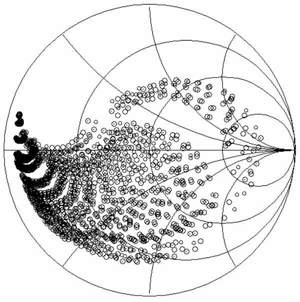
Meas. 8.1 GHz



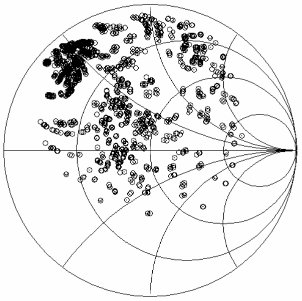
Meas. 16.2 GHz



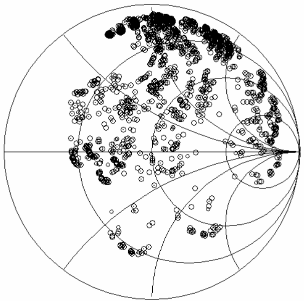
Meas. 20.2 GHz



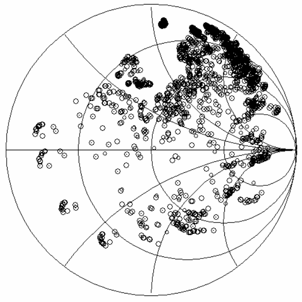
Sim. 4.1 GHz



Sim. 8.1 GHz

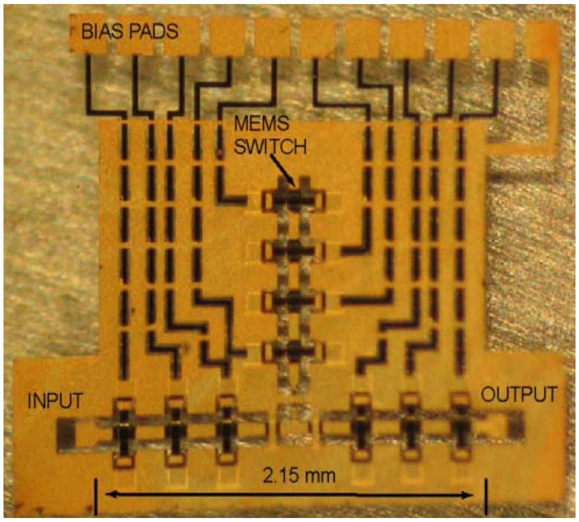


Sim. 16.2 GHz



Sim. 20.2 GHz

Single-Stub Tuner with 11 Switched Capacitors for 50-80 GHz Applications

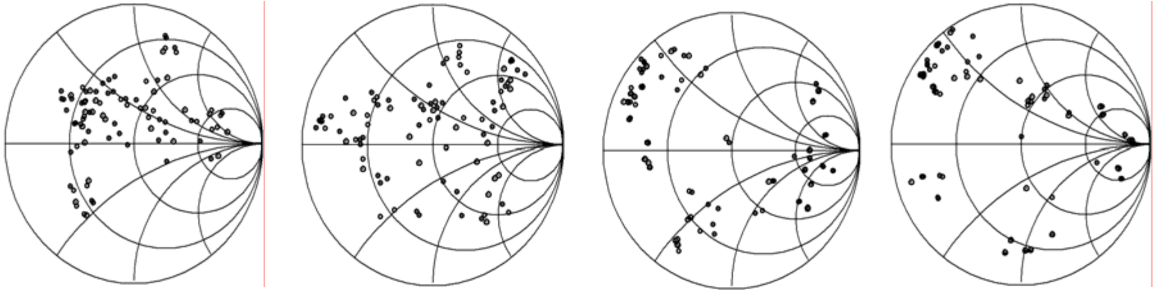


$|\Gamma_{MAX}|$ from 90 measured impedances out of 1024 (2^{10}) possible ones

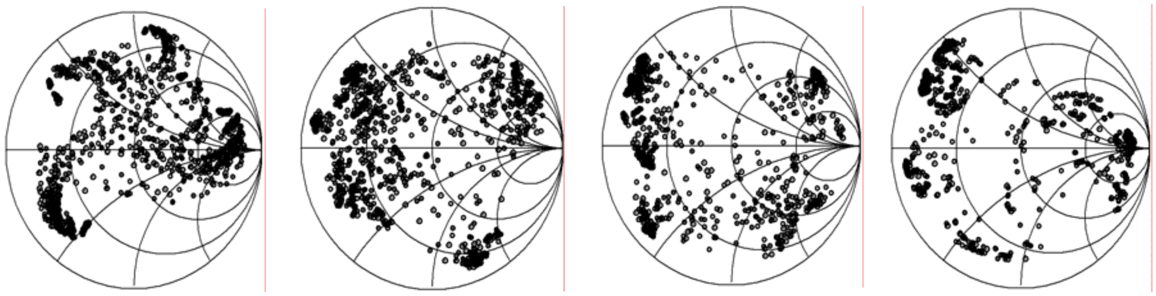
f (GHz)	$\lvert\Gamma_{MAX}\rvert$
50	0.81
55	0.80
60	0.90
65	0.94
70	0.97
75	0.97
78	0.99

Impedance Coverage with 50 Ω Terminations

Measured 90 points out of 1024 (2^{10}) possible combinations



Meas. 50 GHz **Meas. 60 GHz** **Meas. 70 GHz** **Meas. 75 GHz**



Sim. 50 GHz **Sim. 60 GHz** **Sim. 70 GHz** **Sim. 75 GHz**

Conclusions on Reconfigurable Networks

- Easy compared to tunable filters.
- Pay attention to the voltage across the switches/varactors, and for hot actuation. This is important in power amplifiers.
- We have done them all the way to 120 GHz. No more work in this area (unless there is some serious power to handle).
- Distributed designs have much less loss than stub-based designs.