Microwave Electronics Laboratory

Department of Microtechnology and Nanoscience, Chalmers University

Herbert Zirath, head of laboratory

~>35 people, 18 seniors, 16 PhD-students, 3 adjuct professors

Research at the Microwave Electronics Laboratory:

MEL hosts

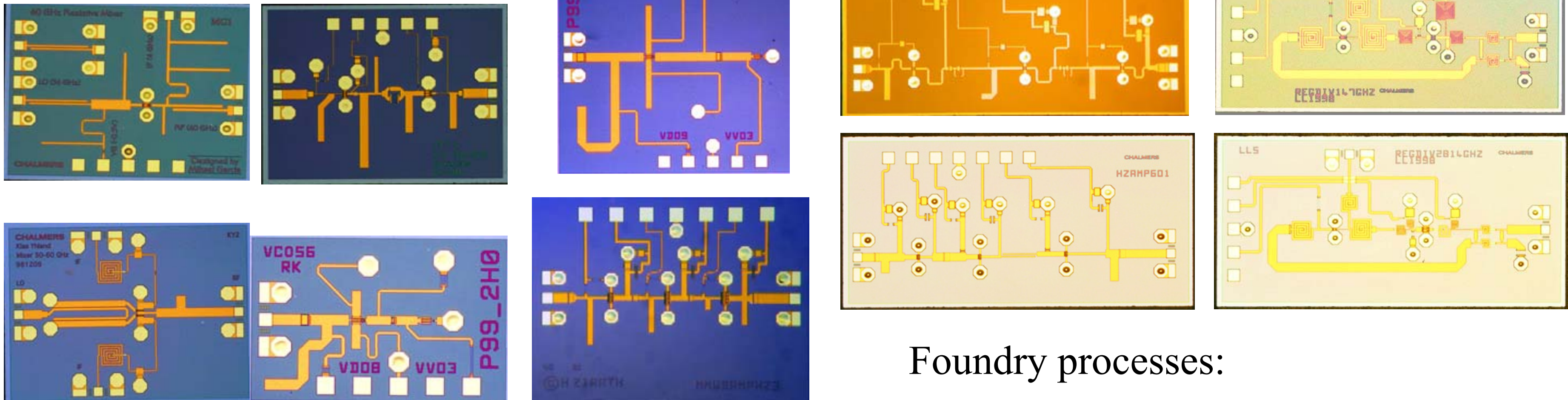
-HSEP: SSF Strategic Research Center in High Speed Electronics and Photonics
-GHz Center funded by VINNOVA

MEL is a member of European Networks of Excellent (NoE): TARGET

Participate in European widebandgap initiative Korregan

Groups	groupleader
1. Widebandgap devices and circuits	N Rorsman
2. SiC MOSFET	E Sveinbjörnsson
3. InP HEMT MMIC	J Grahn
4. MMIC design group	H Zirath
5. MBE group	T Andersson
High-Speed LSI Circuit Design (CIT)	T Swahn

Analog MMIC design group at Chalmers



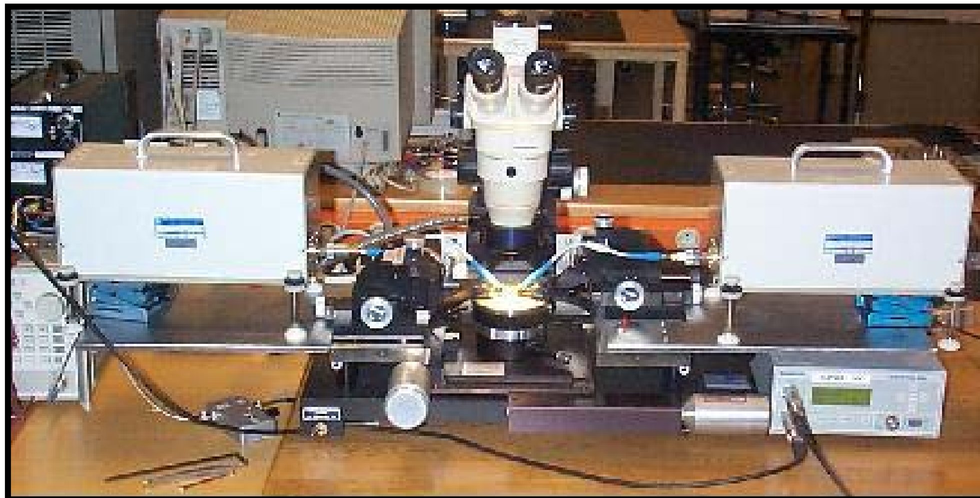
Foundry processes:

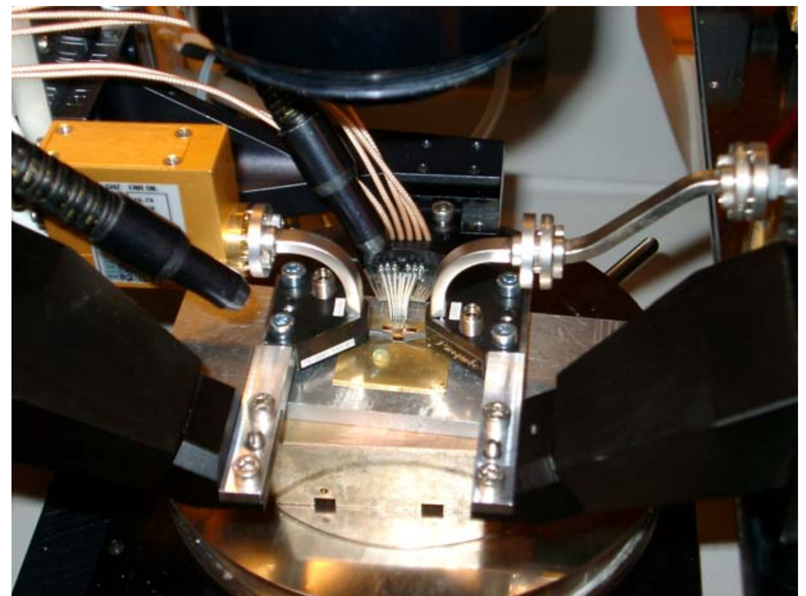
Process	Foundry
•AlGaAs-InGaAs HEMT	OMMIC
•AlGaAs-InGaAs HEMT	WIN
•InGaP-GaAs HBT	K*ON
•90 nm CMOS	IMEC
•45 nm CMOS	IMEC
•MHEMT fmax 250 GHz	OMMIC
•MHEMT MP15-01	WIN
•MHEMT 50/100 nm	IAF

- Research on new circuit topologies
- Searching for new system applications
- Advancing MMICs to state-of-the-art performance
- Multifunctional MMICs for system demonstrators
- Silicon based MMICs for low cost applications at frequencies 10-60 GHz
- Packaging of MMICs i e flip chip etc

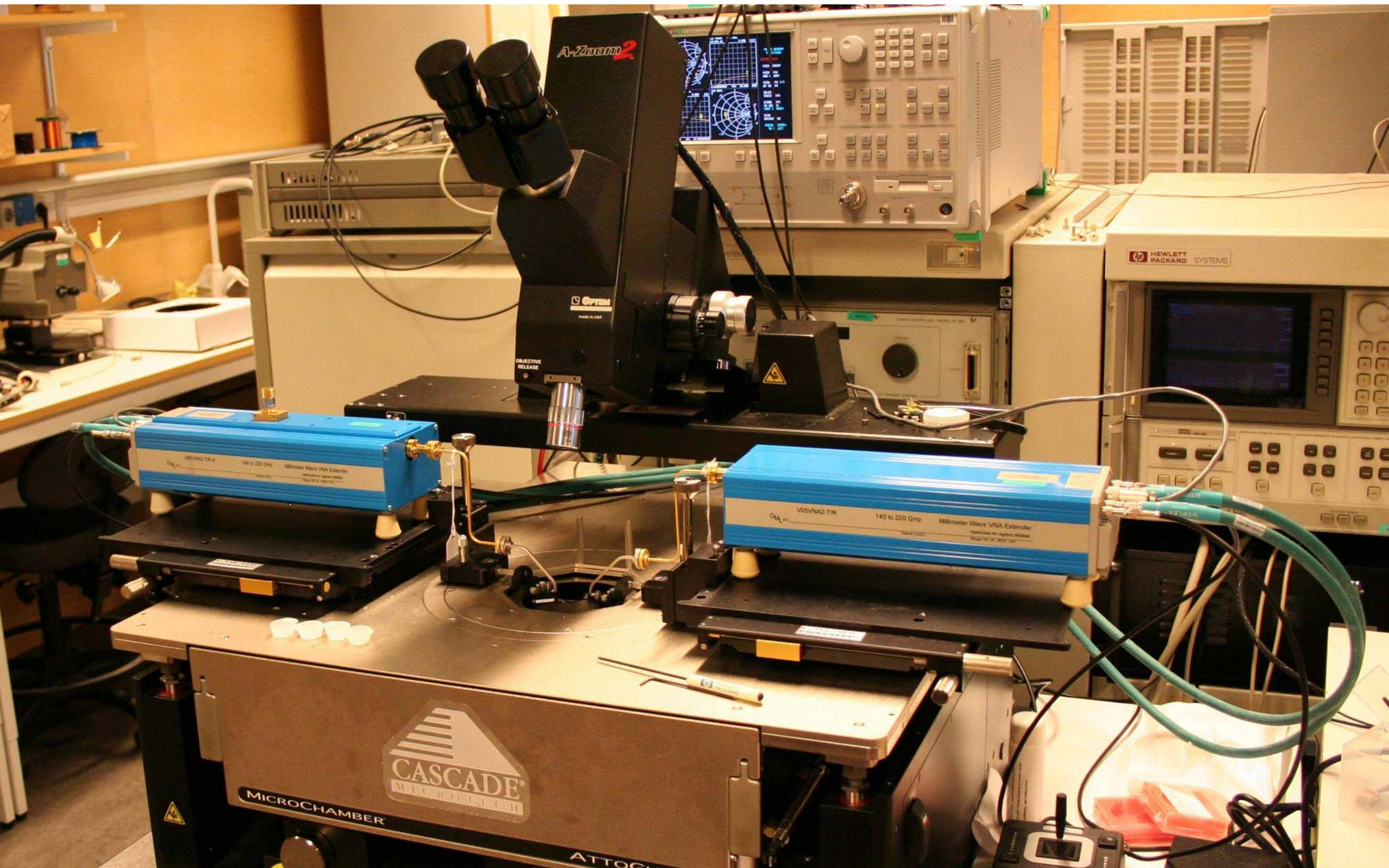
4 characterization labs: THz-lab, Cryo-lab, load-pull lab, general lab

Network analyzers covering kHz up to 350 GHz
Pulsed S-parameters, Spectrum analyzers up to 75 GHz
Noise figure from 2 to 115 GHz
Load pull and noise parameter system for from 0.8 to 110 GHz
THz-lab with FTS to 8 THz, FIR laser sources up to 3.5 THz
Cryogenic lab: 4 cryo-stations down to 15 K, including CPW-probing
DC-parameters





First test of OML 140-220 GHz modules



Outline MMIC-design seminar

1. Introduction		10
2. Devices and models for III-V	60	60
3. Circuit design:		
4. Amplifiers	30	30
5. Frequency multipliers	26	30
6. Mixers	25	45
7. Multifunction MMIC: 60 GHz WLAN	10	10
8. Oscillators	35	45
9. Models again	30	15
10.Si-MMICs, SiC MMIC ?	35	30
11.The GHzCentre, a new VINNOVA centre	9	15

Introduction

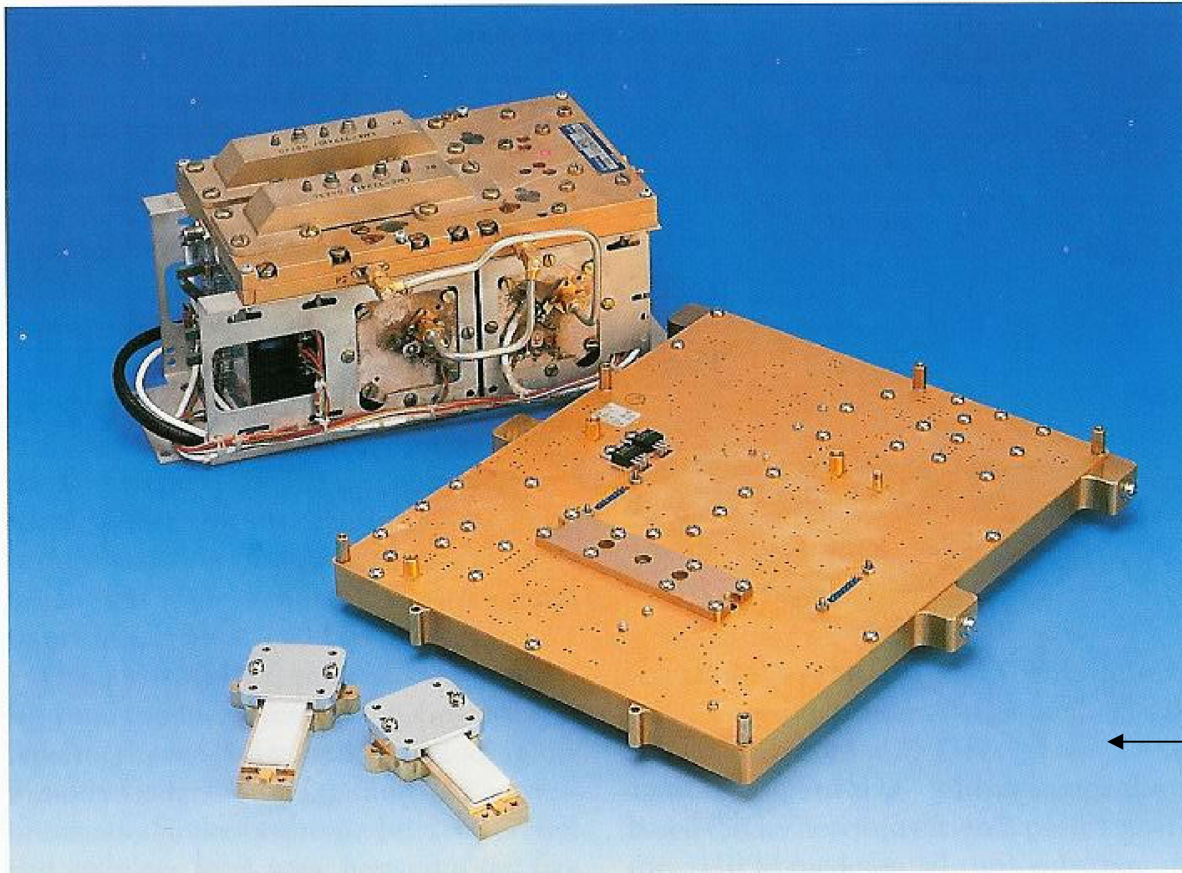
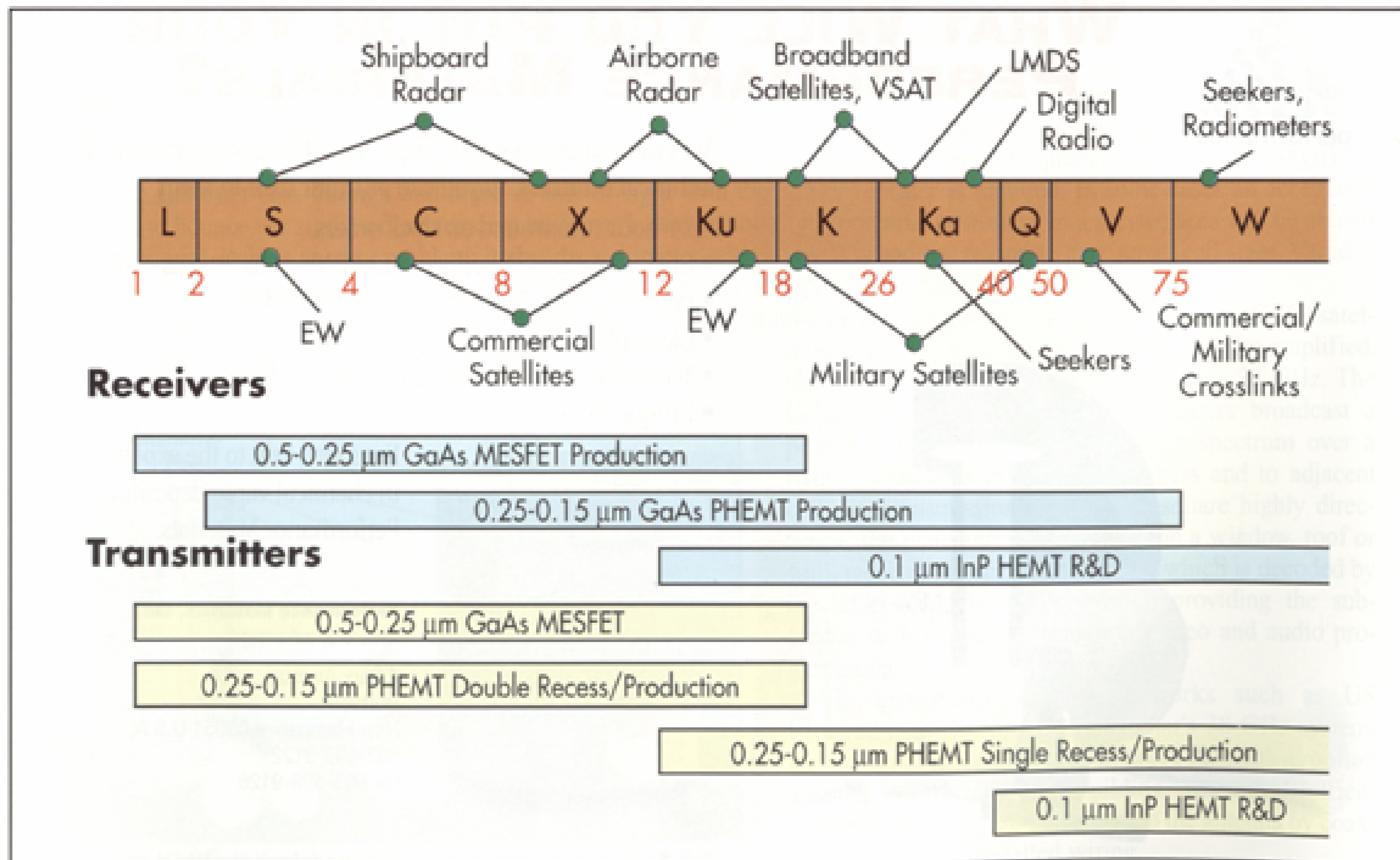


Figure 2
Three generations of the microwave block: back, waveguide technology (first generation, 1985); middle, microstrip technology (current generation, 1992); front, MMIC technology (next generation).

R. Pucel,'Design considerations for Monolithic Microwave Circuits', MTT 1981

microwave millimeterwave frequency bands and applications and available technologies



Applications for high frequency MMICs, and Sanders' MMIC processes.

GaAs Opportunities from 5 - 100 GHz

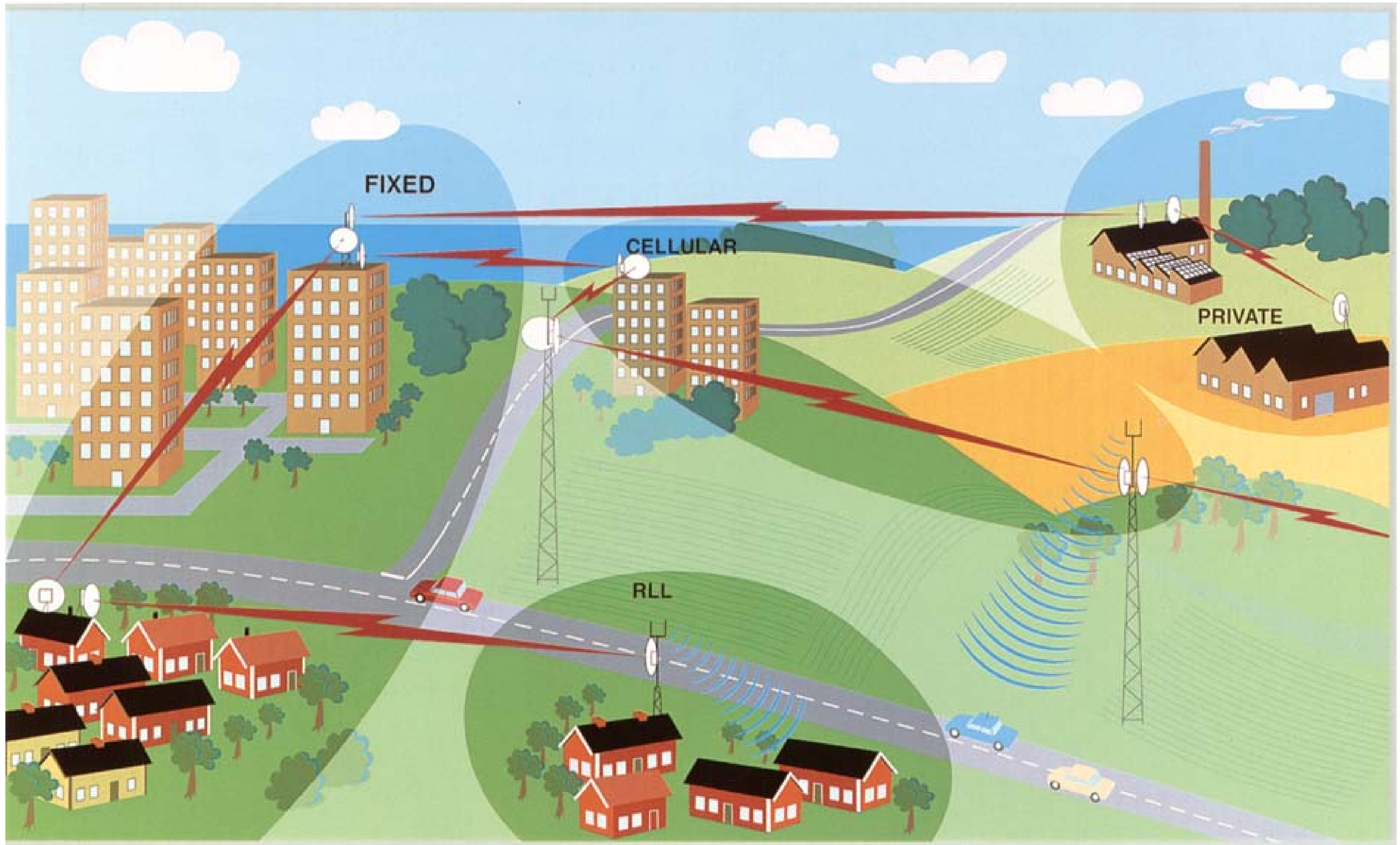
System Type or Application	Operating Frequency	GaAs Chips Required	Status & Comments
WLAN	5.2 GHz	T/R MMICs	Emerging now, used for data communication
Short Distance Communications	5.8 GHz	Transceiver MMICs	Emerging, potentially large market for remote ID
DBS (Direct Broadcast Satellite)	10.5 - 11.5 GHz	LN converter MMICs & discrete HEMTs	Existing/mature; requires large volumes & lowest cost
Point-to-Point Communications	13 - 60 GHz	T/R MMICs	Emerging, fast growth, 1st volume application for MMICs >12 GHz
Video Distribution Systems	28 GHz* & 42 GHz**	LN converter & transceiver MMICs	LMDS started in 1997, MVDS will start in 2000. Consumer driven, requires low cost
Optical links	up to 60 GHz	digital drivers, MUX/DMUX	Existing, rapidly growing, today limited to commercial systems
Satellite Networks	12 - 40 GHz	T/R MMICs	Emerging, will serve commercial and consumer markets
Automotive Radar	76 GHz	Transceiver MMICs	Emerging in '98 but slow growth until after 2004

*LMDS = Local Multipoint Distribution System = North America
**MVDS = Microwave Video Distribution System = Europe

100Gbps..

System type or application	Operating frequency	GaAs chips required	Status & comments
Millimeterwave Point to point communication 10 Gbps wireless	57-64 GHz WLAN/PAN 71-76 GHz 81-86 GHz 92-95 GHz 120 GHz and above	Receivers and transmitters	Emerging, frequencies have been allocated Research by NTT
Radiometers for Remote sensing Security & safety	60, 119, 183 GHz 220 GHz	Receivers transmitters&rec	Environmental study Ozone, oxygene, water weapon detection
radar	24 GHz	Receive&transmit	Level measurements in oil-tanks etc

Radiolinks for mobile and fixed communication



Exampel radiolink, Minilink E from Ericsson AB

Mini-link is manufactured for 7, 8, 15, 18, 23, 26 och 38 GHz. Capacity from 2 Mbps to 36 Mbps.

Used for

*fixed and mobile telecomnetwork
*private networks
*links for radiobase-stations
*Highcapacity mobile city networks
*approx 200 000 shipped units/year
*manufactured in Borås

IEEE 802.15 TG3c

60 GHz WPAN

The millimeter-wave WPAN will allow very high data rate applications, such as high speed internet access, streaming content download (video on demand, HDTV, home theater, etc.), real time streaming and wireless data bus for cable replacement. Optional data rates in excess of 2 Gbps will be provided.

Participants:

- **Motorola, IBM, Siemens, NEC**
- **OKI, NICT, NewLAN, Millisys, TiaLinx, BridgeWave**
- **CRL, Tohoku U, U Massachusetts**
- **……**

(more than 40 companies)

Wireless HDTV interconnects

NEC – 60 GHz wireless TRX

Characteristics

- 60 GHz band
- 1 Gbps data rate
- 1080lines HDTV
- ASK modulation
- Ceramic module with FC
- 70x50x15 mm^3
- Path diversity scheme (dual receivers)

NEC

60 GHz's Unique "Feature"

- 60 GHz is the resonant frequency of O_2 molecules

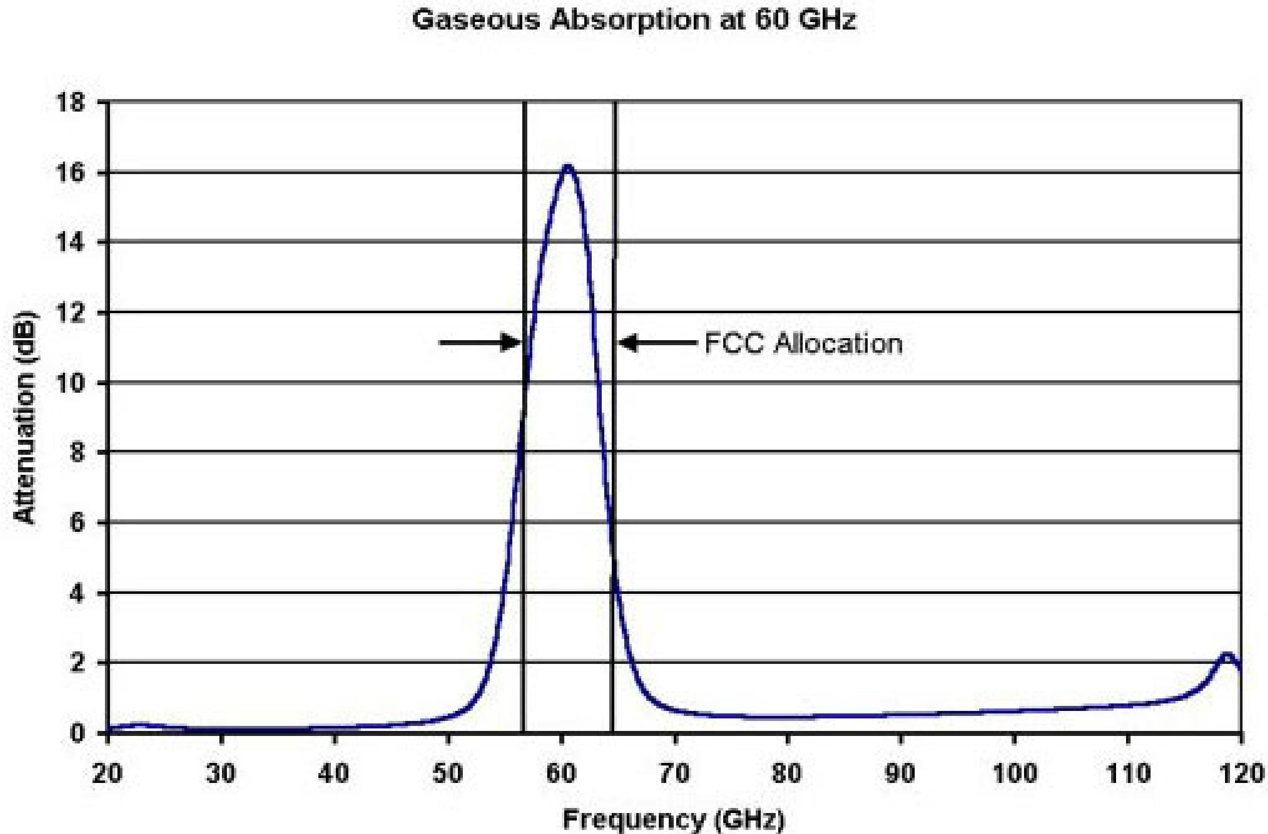


Figure 2 – O_2 attenuation versus frequency

The Effect of O_2 Absorption

- A 60 GHz signal is essentially extinguished at 2 km from the source at sea level
- Used as an intra-satellite communication frequency
- Frequency can be reused even when in line with another source

The Limits of 60 GHz Transmission

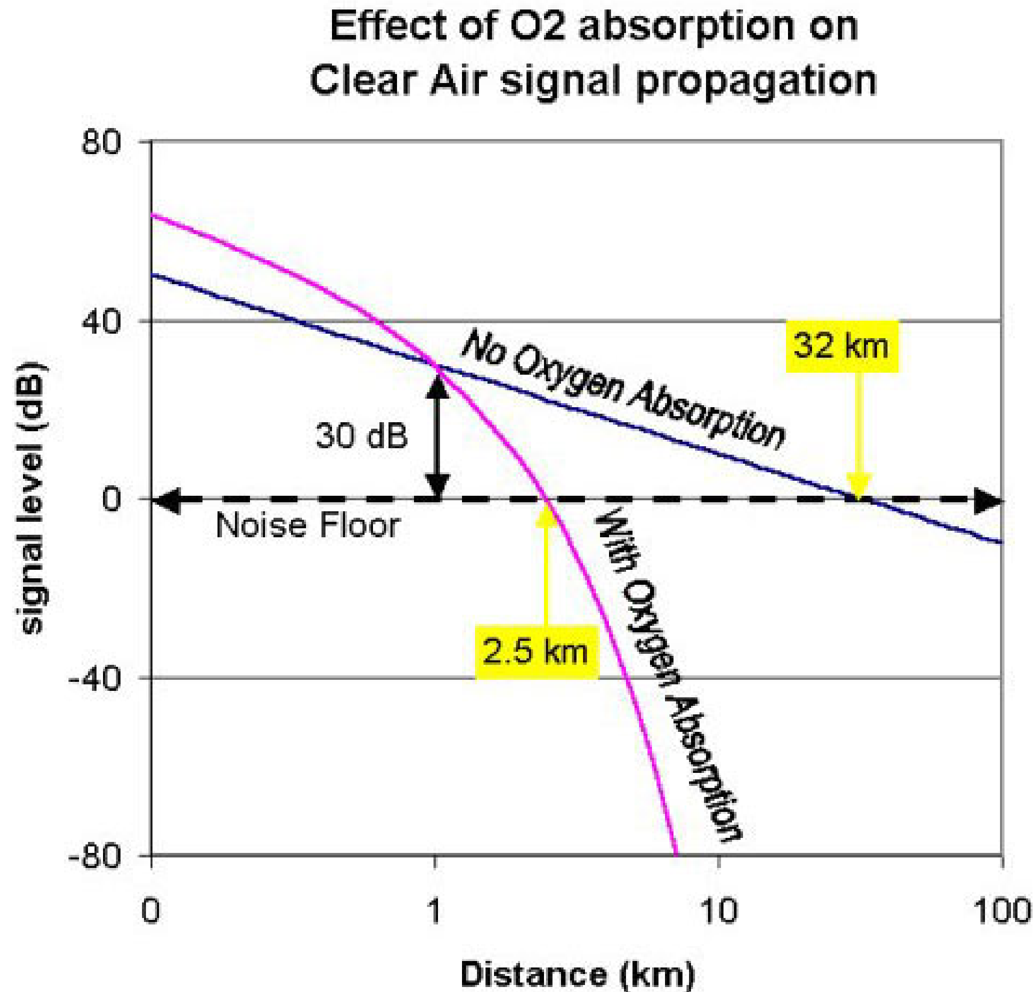


Figure 3 – Radiation Limiting by O_2 Absorption

MMIC: Monolithic Microwave Integrated Circuit

The MMIC concept combine active and passive components at the surface of an insulating semiconductor leading to:

Advantages:

1. Lower cost per circuit in volume production
2. Improved reliability and reproducibility
3. Small size and weight
4. Larger bandwidth due to less interconnects (wire inductance)

Disadvantages:

1. passive components often take up large area (expensive)
2. difficult to trim
3. hard to search and find errors
4. almost impossible to fix errors
5. crosstalk might be a problem
6. difficult to combine different semiconductors
7. initially expensive, development expensive
8. Foundry turn-around time

Wish list of components

Inductors
Resistors
Capacitors
Transformers
Shortcircuits / viaholes to ground
Crossing conductors
Several metal layers

Transmission line components such as:
Stubs
Impedance transformers ($\lambda/4$) etc
Couplers: Lange, Marchand etc
Different types of transmission lines e g MS, CPWG, SL etc
Transitions between different transmission lines

Semiconductors

Transistors of FET type
Transistors of BJT type

Diodes:
Varactor diodes for frequency multipliers, VCO-tuning etc
Switch diodes for mixers, detectors, frequency multipliers etc

Silicon technologies can combine different semiconductor components like FET+BJT in BiCMOS, rarely found in GaAs or other III-V technology. New process from WIN underway..

We have freedom to choose the size of the devices, normally the width of the device. The transconductance etc can now be tailored since gm scales linearily with the width !

MMIC processes and components

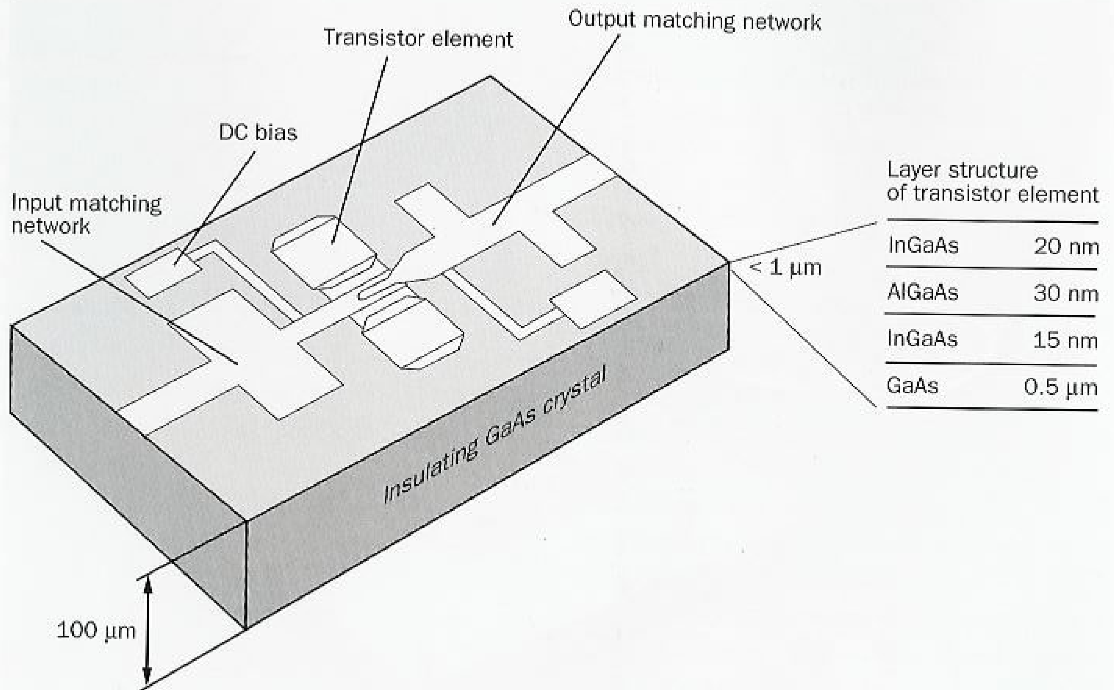


Figure 3
Schematic view of an MMIC. The semiconductor layer structure for high-frequency transistors are combined with "semi-insulating" GaAs which acts as a good dielectric. All active and passive components are built on the top of the GaAs crystal. The ground plane is at the bottom of the wafer.

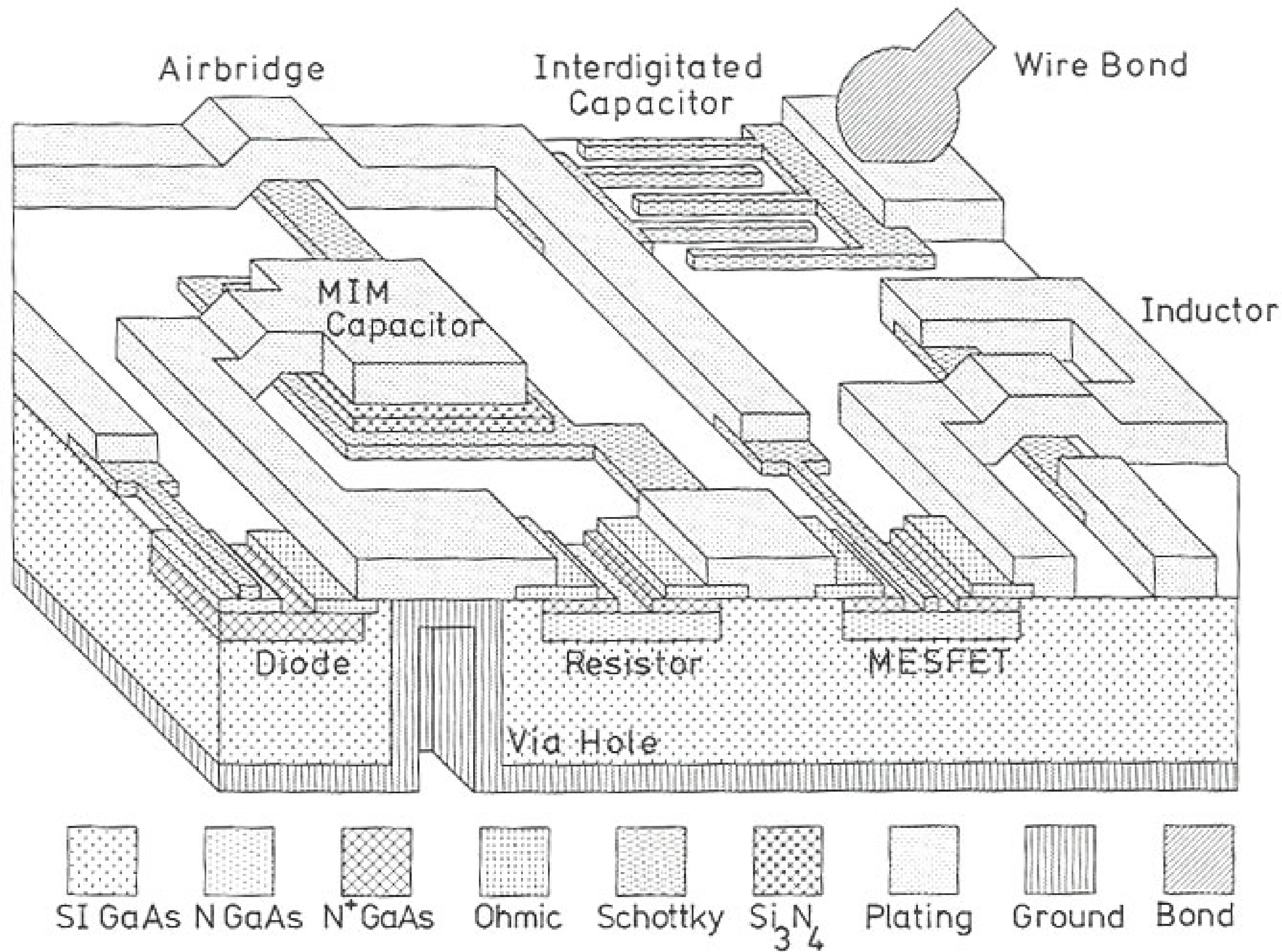


Fig. 3.1 Three-dimensional schematic of basic MMIC construction.

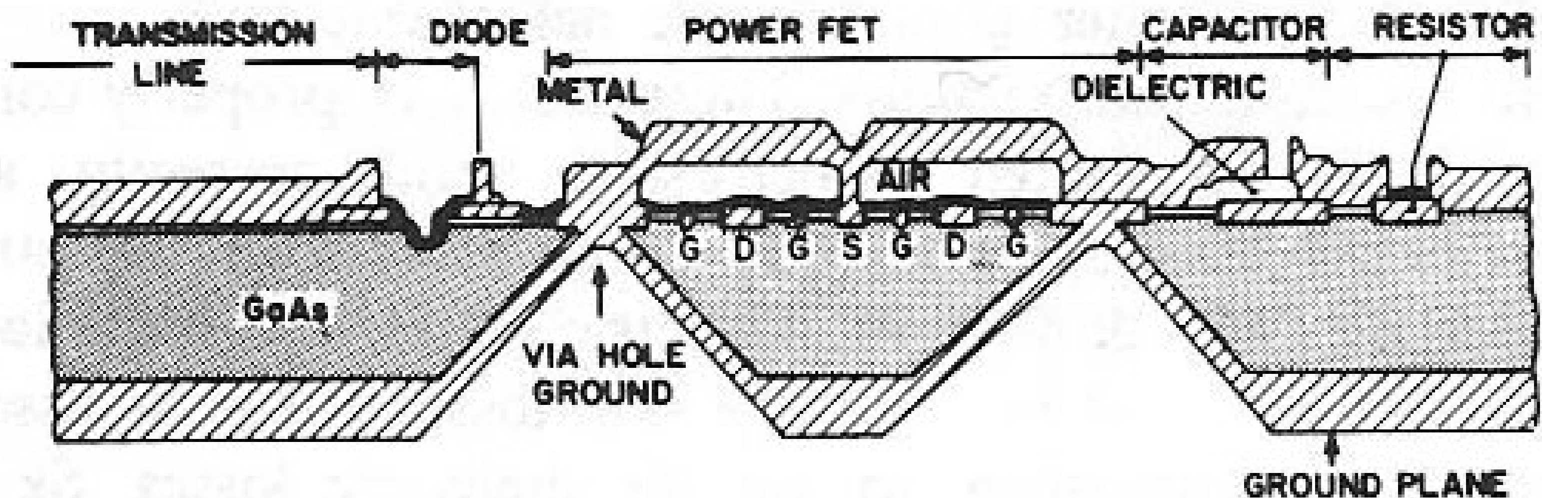
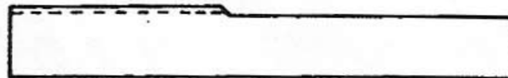


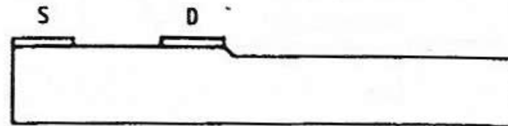
Fig. 22. Composite sketch illustrating technologies used in monolithic circuits.

MMIC-process sequence

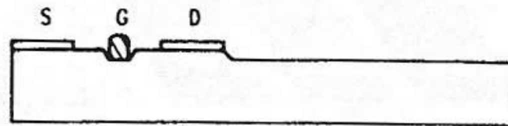
1. Mesa Etch



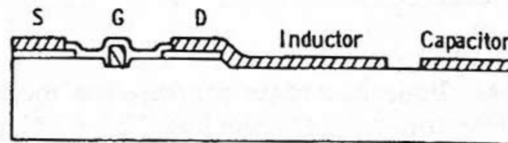
2. Ohmic Contact Metallization



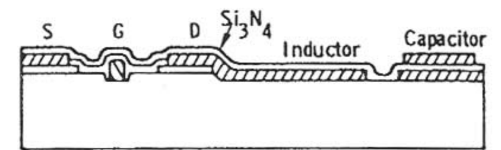
3. Schottky Gate Metallization



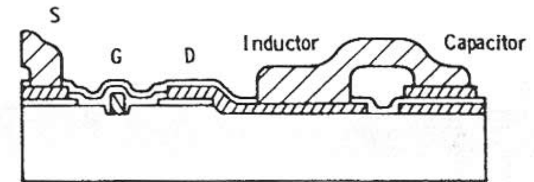
4. First Level Metal (Inductors, Capacitors, S-D Overlay)



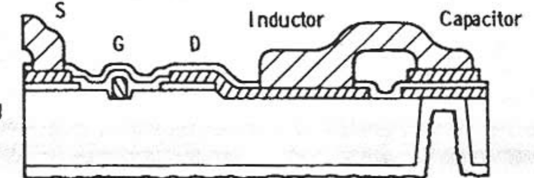
5. Capacitor Top Plates



6. Air Bridge Interconnects



7. Via Grounding, Backside Plating



Different transmission lines and their properties

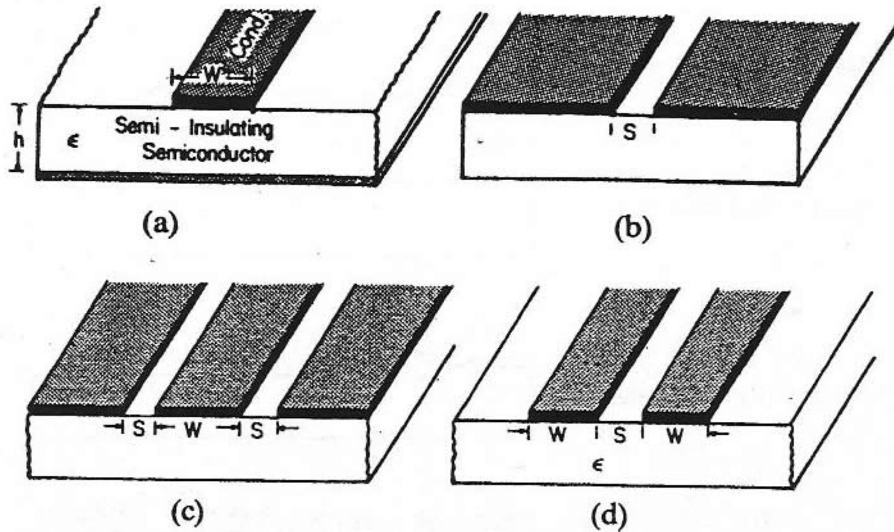


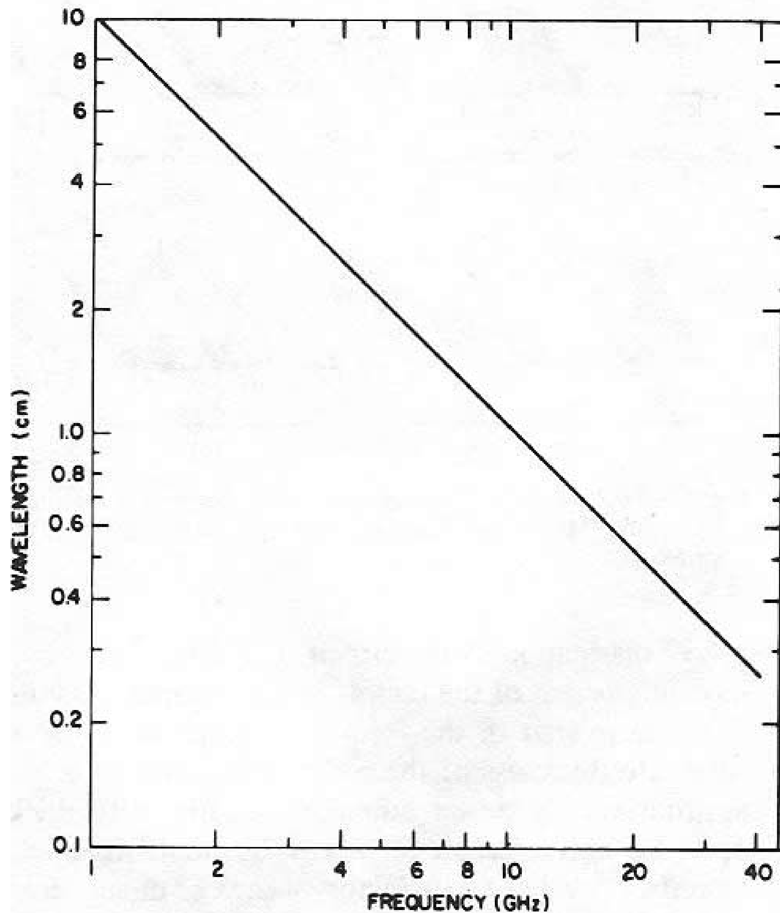
Fig. 4. Four candidate propagation modes for monolithic circuits. (a) Microstrip (MS). (b) Slot line (SL). (c) Coplanar waveguide. (d) Coplanar strips (CS).

TABLE II
QUALITATIVE COMPARISON OF PROPAGATION MODES

	MICROSTRIP	COPLANAR WAVEGUIDE	COPLANAR STRIPS	SLOT LINE
Attenuation Loss	low	medium	medium	high
Dispersion	low	medium	medium	high
Impedance Range (ohms)	10-100	25-125*	40-250*	high
Connect Shunt Elements	diff.	easy	easy	easy
Connect Series Elements	easy	easy	easy	diff.

*Infinitely thick substrate

Wavelength and loss GaAs microstrip, h=0.1mm



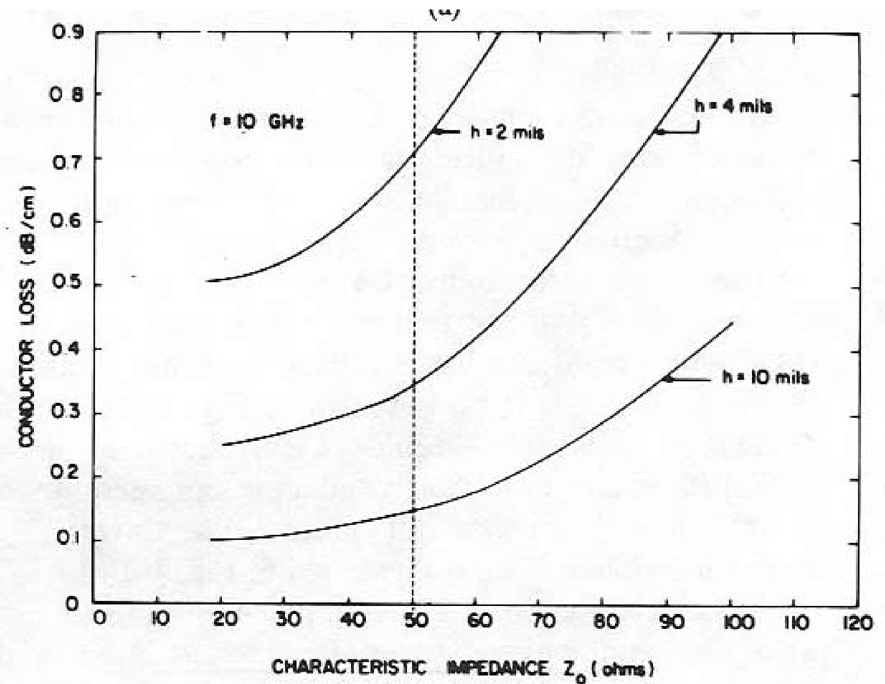
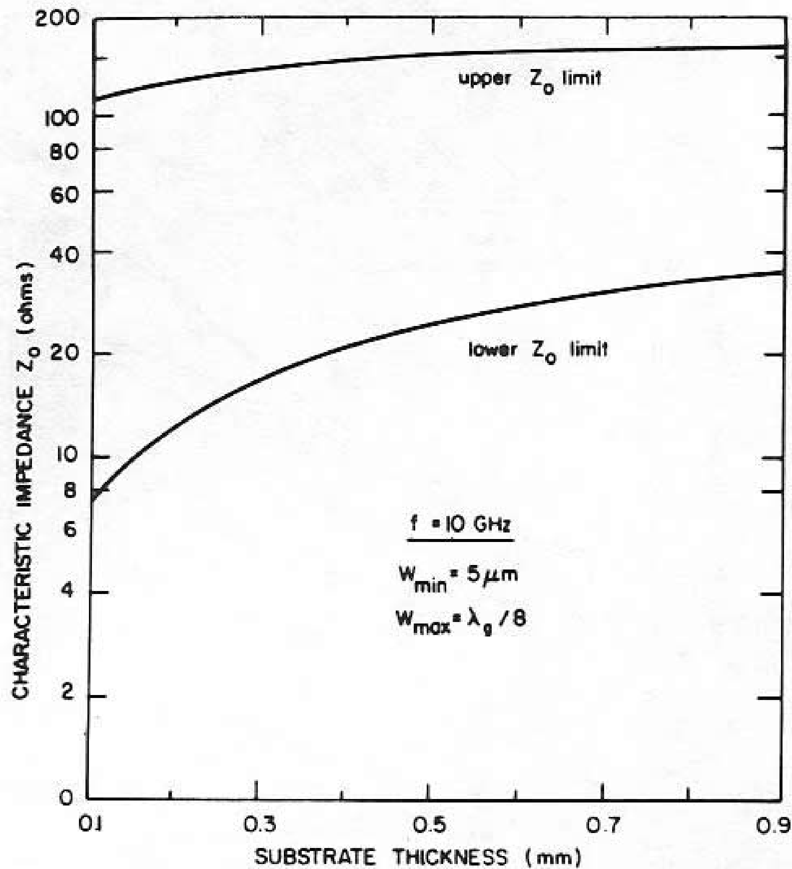
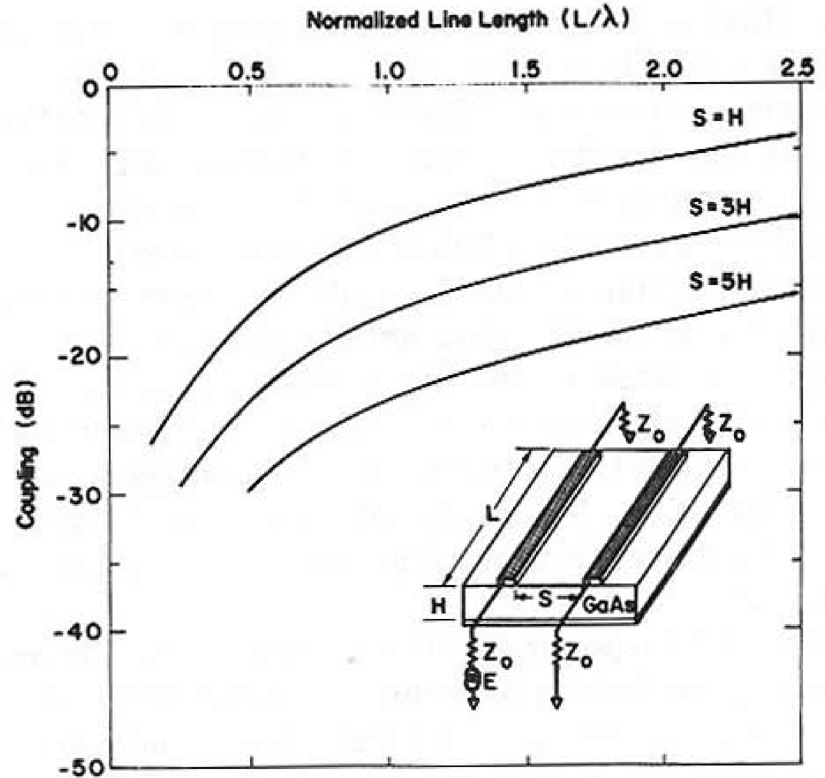


Fig. 7. (a) Wavelength as a function of frequency for microstrip on a GaAs substrate for $h=0.1$ mm. (b) Conductor loss of microstrip on a GaAs substrate as a function of substrate thickness and characteristic impedance for $f=10$ GHz.

Characteristic impedance and coupling



Range of characteristic impedance of microstrip on GaAs substrate as a function of substrate thickness.



Calculated coupling between adjacent parallel microstrip lines as a function of spacing and frequency.

Via-hole for grounding

40-60 pH/mm

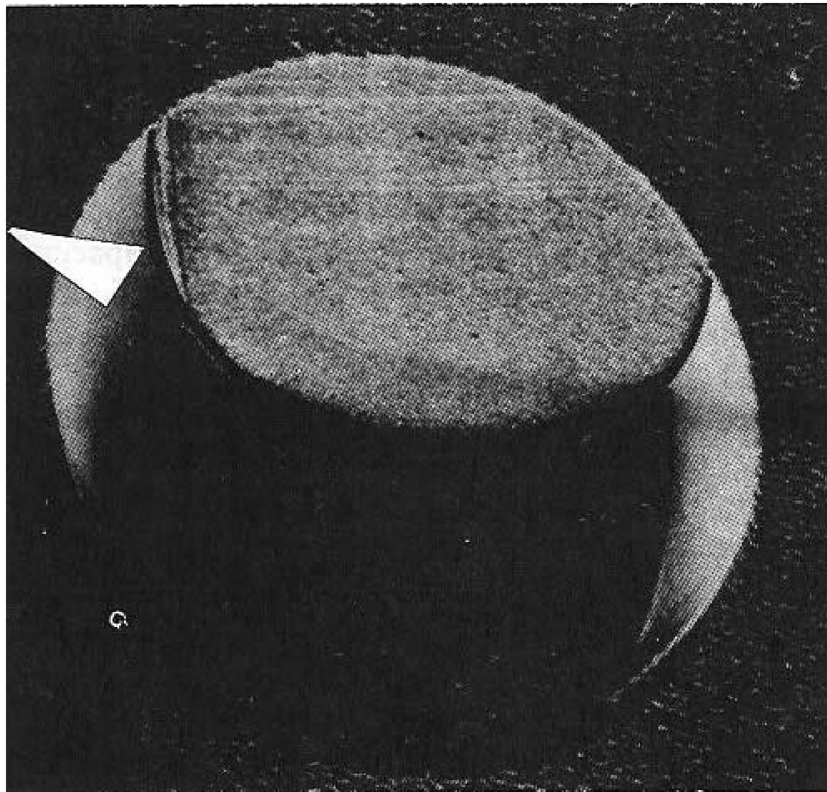


Fig. 8. 50-μm diameter "via" hole etched in a GaAs wafer.

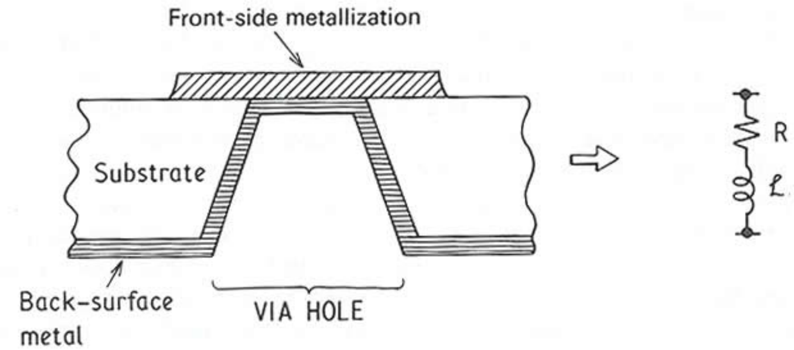
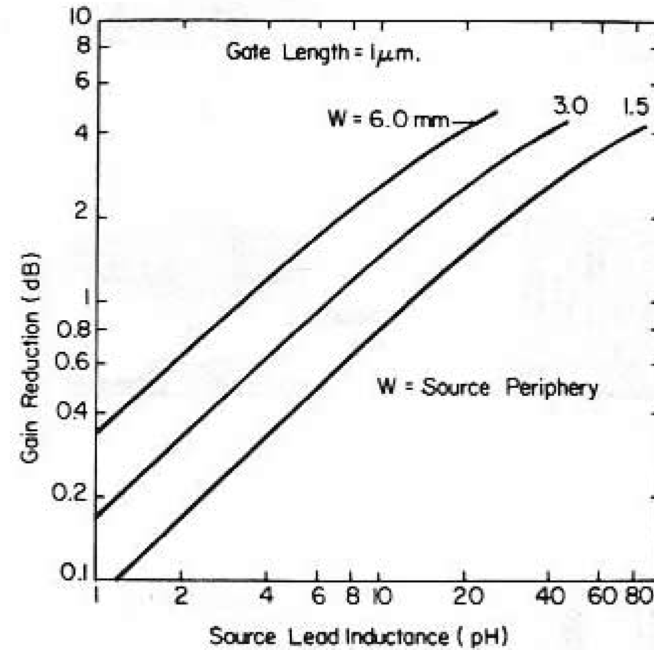


Fig. 6.50 A via ground, with equivalent circuit.



Calculated gain reduction of a GaAs power FET as a function of source lead inductance.

Discontinuities

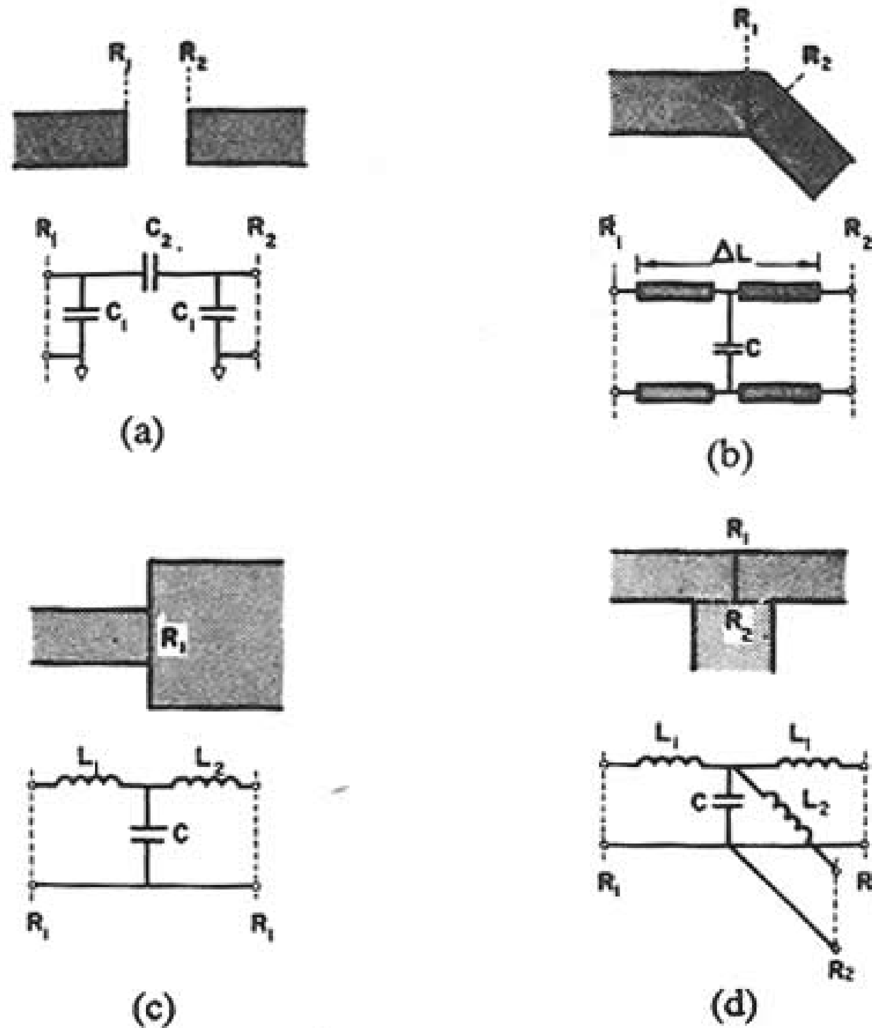


Fig. 23. Some microstrip discontinuities and their equivalent circuits. (a) Gap. (b) Bend. (c) Width discontinuity. (d) Tee junction.

Planar inductors

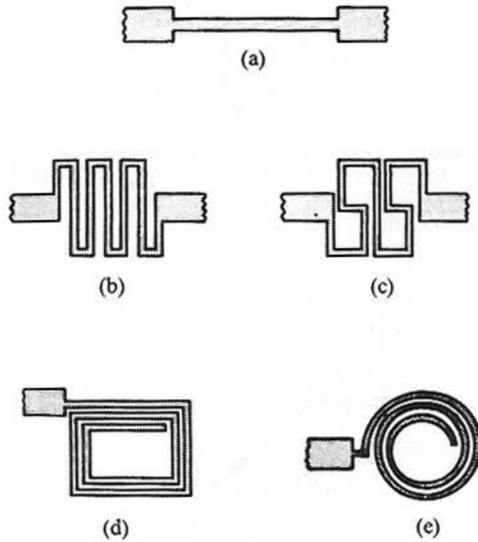
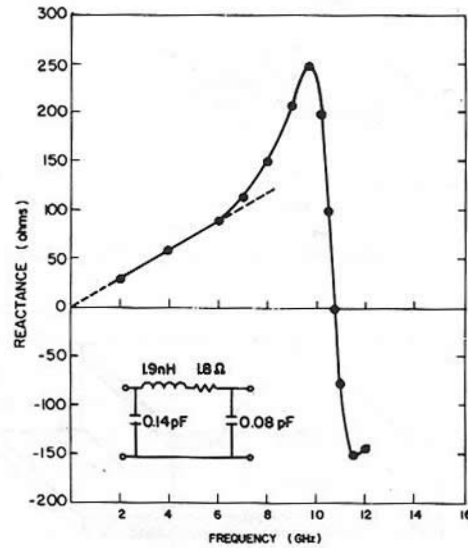
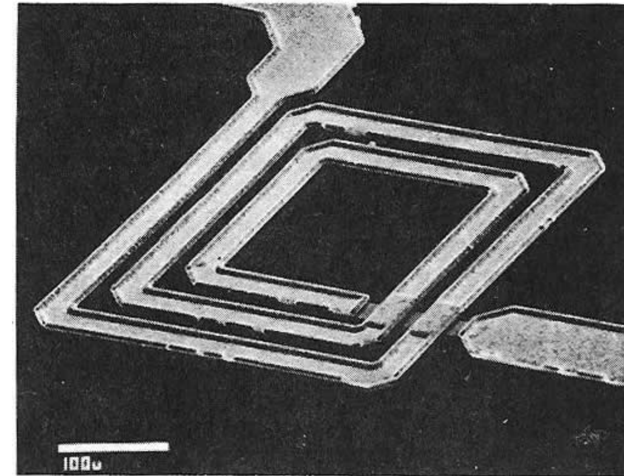


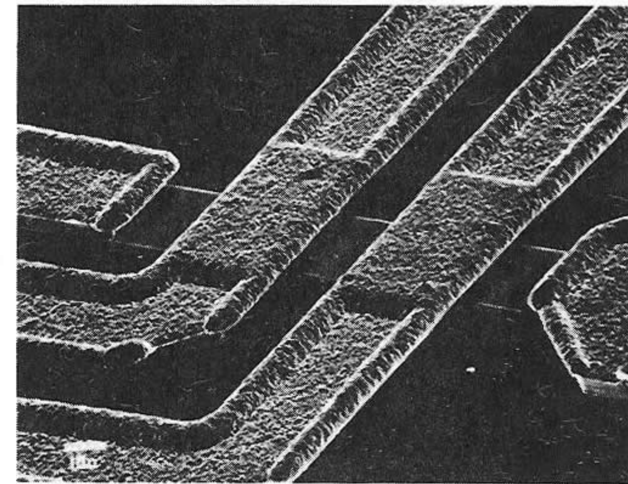
Fig. 16. Some planar inductor configurations. (a) High-impedance lir section. (b) Meander line. (c) *S*-line. (d) Square spiral. (e) Circul spiral.



MEASURED REACTANCE OF A TEN-SEGMENT SQUARE-SPIRAL GROUNDED INDUCTOR ON A 0.1 MM THICK SI-GAAS SUBSTRATE



(a)



(b)

Resistors

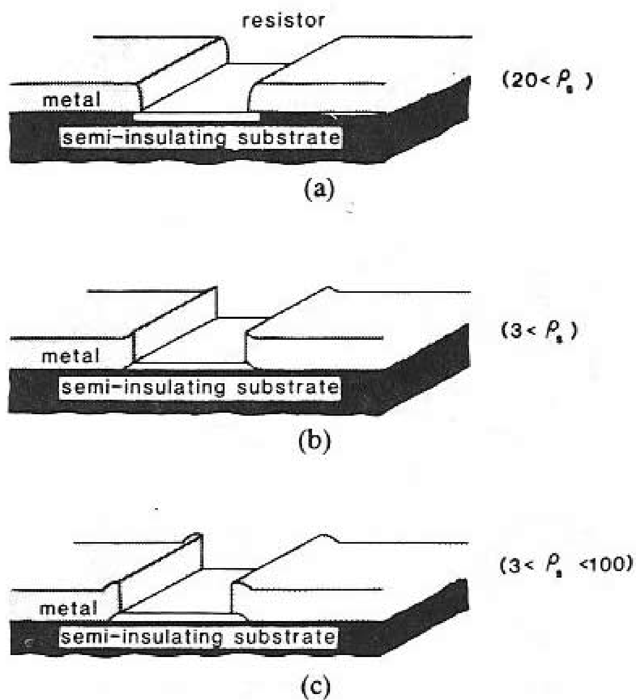


Fig. 20. Examples of planar resistor designs. (a) Implanted resistor. (b) Mesa resistor. (c) Deposited resistor.

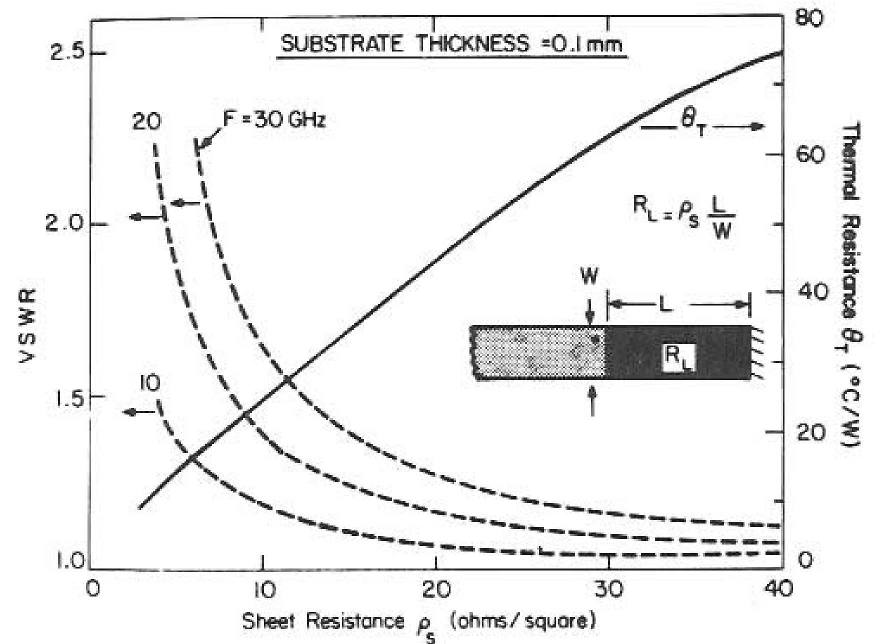


Fig. 21. Thermal resistance and VSWR of a planar resistor as a function of sheet resistance and frequency.

<u>Tradeoff between thermal resistance and VSWR</u>

For low thermal resistance, the area should be as large as possible i e the sheet resistance should be minimized. At some point however, the resistive film behaves like a transmission line and VSWR increases

TABLE IV
PROPERTIES OF SOME RESISTIVE FILMS

MATERIAL	RESISTIVITY (μΩ-cm)	TCR (ppm/°C)	METHOD OF DEPOSITION	STABILITY	COMMENTS
Cr	13 (BULK)	+3000 (BULK)	EVAPORATED SPUTTERED	G-E	EXCELLENT ADHERENCE TO GaAs
Ti	55-135	+2500	EVAPORATED SPUTTERED	G-E	EXCELLENT ADHERENCE TO GaAs
Ta	180-220	-100 TO +500	SPUTTERED	E	CAN BE ANODIZED
→ Ni Cr	60-600	200	EVAP. (300°C) SPUTTERED	G-E	STABILIZED BY SLOW ANNEAL AT 300°C
TaN	280	-180 TO -300	REACTIVELY SPUTTERED	G	CANNOT BE ANODIZED
→ Ta_2N	300	-50 TO -110	REACTIVELY SPUTTERED	E	CAN BE ANODIZED
→ BULK GaAs	3-100 ohms/sq.	+3000	EPITAXY OR IMPLANTATION	E	NONLINEAR AT HIGH CURRENT DENSITIES

Capacitors

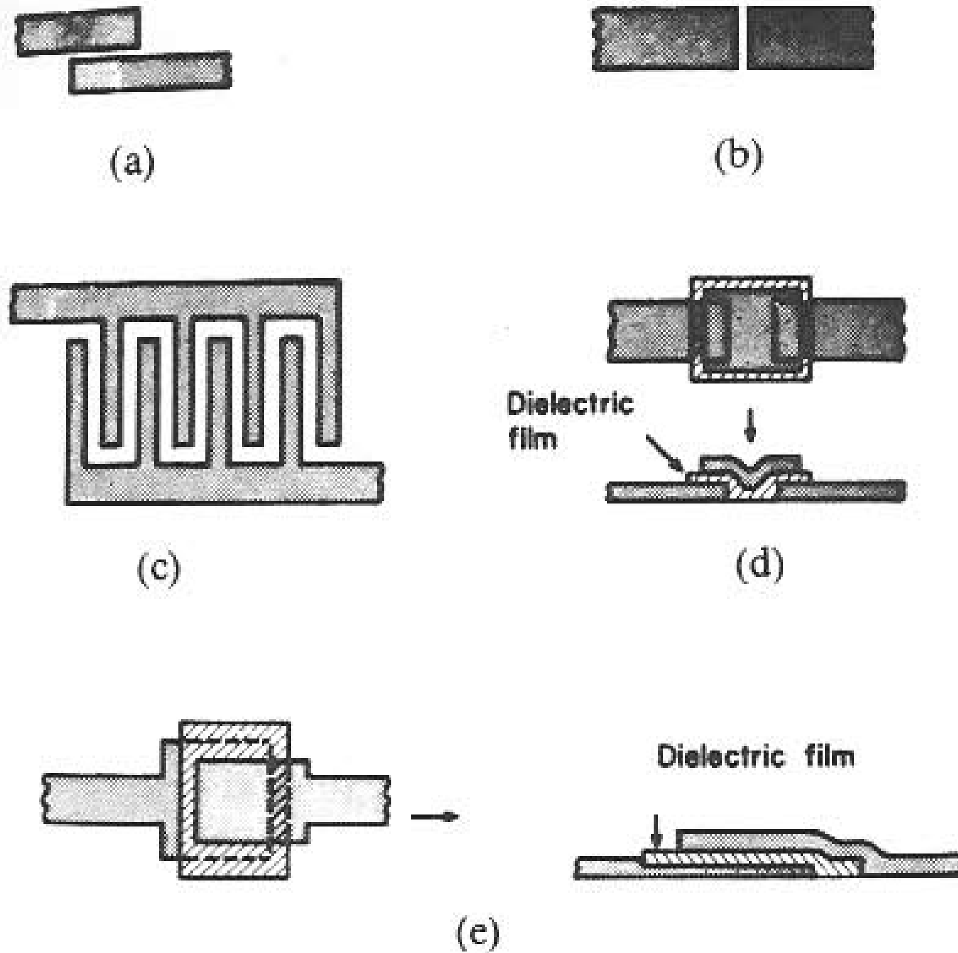


Fig. 11. Some planar capacitor designs. (a) Broadside coupled. (b) End coupled. (c) Interdigitated. (d) End-coupled overlay. (e) Overlay.

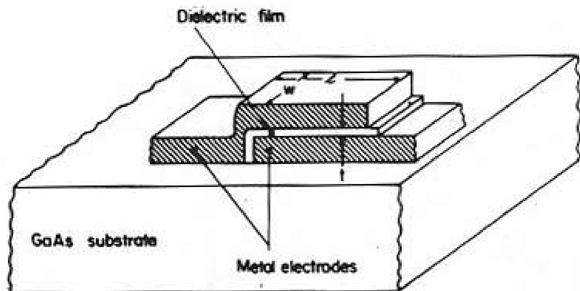
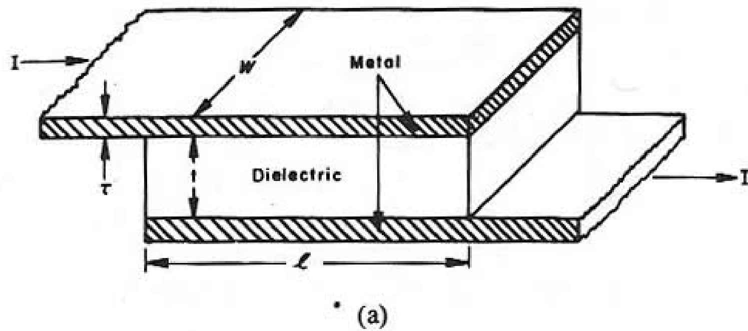
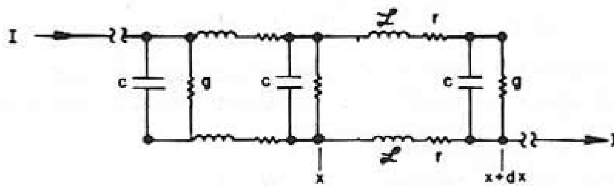


Fig. 12. Perspective of an overlay thin-film capacitor.



(a)



(b)

Fig. 13. Diagrams relevant to analysis of impedance of a thin-film capacitor. (a) Thin-film capacitor. (b) Circuit model.

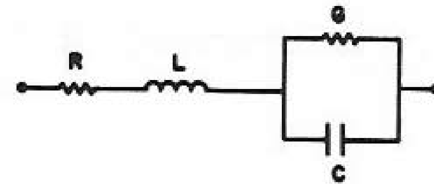
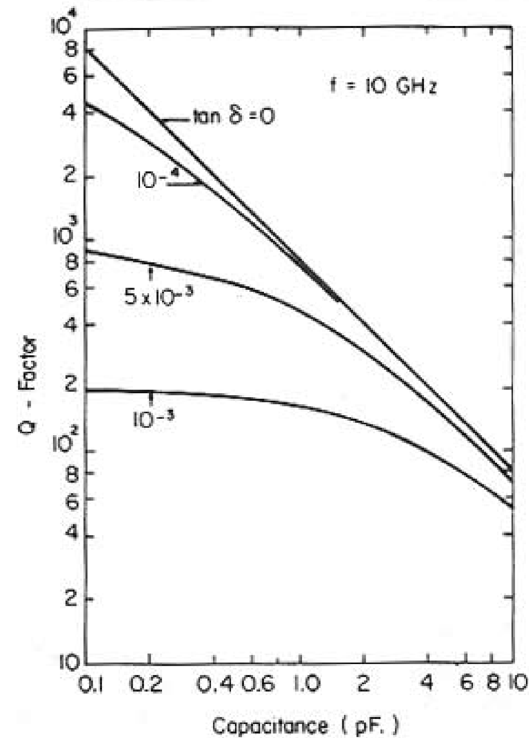


Fig. 14. Equivalent circuit of a thin-film capacitor. $R=2/3\ rl$. $C=cl$. $G=\omega c \tan\delta$. $L=\mathfrak{L}l$. r = resistance/length (electrodes). c = capacitance/length. $\mathfrak{L}$ = inductance/length (electrodes). $\tan\delta$ = loss tangent of dielectric film.



Quality factor of a square thin-film capacitor as a function of capacitance and dielectric loss tangent for $f=10$ GHz.

Transistors: the basis for the MMIC

Transistors on GaAs originate from the GaAs MESFET

Several different GaAs technologies are available on foundry for various applications:

AlGaAs-GaAs 'HEMT'
AlGaAs-InGaAs-GaAs HEMT: 'PHEMT'
AlGaAs-InGaAs-GaAs HEMT with enhancement/depletion transistors 'E/D'
AlInAs-GaInAs-AlGaInAs-GaAs 'mHEMT'
AlInAs-GaInAs-InP 'InP HEMT'

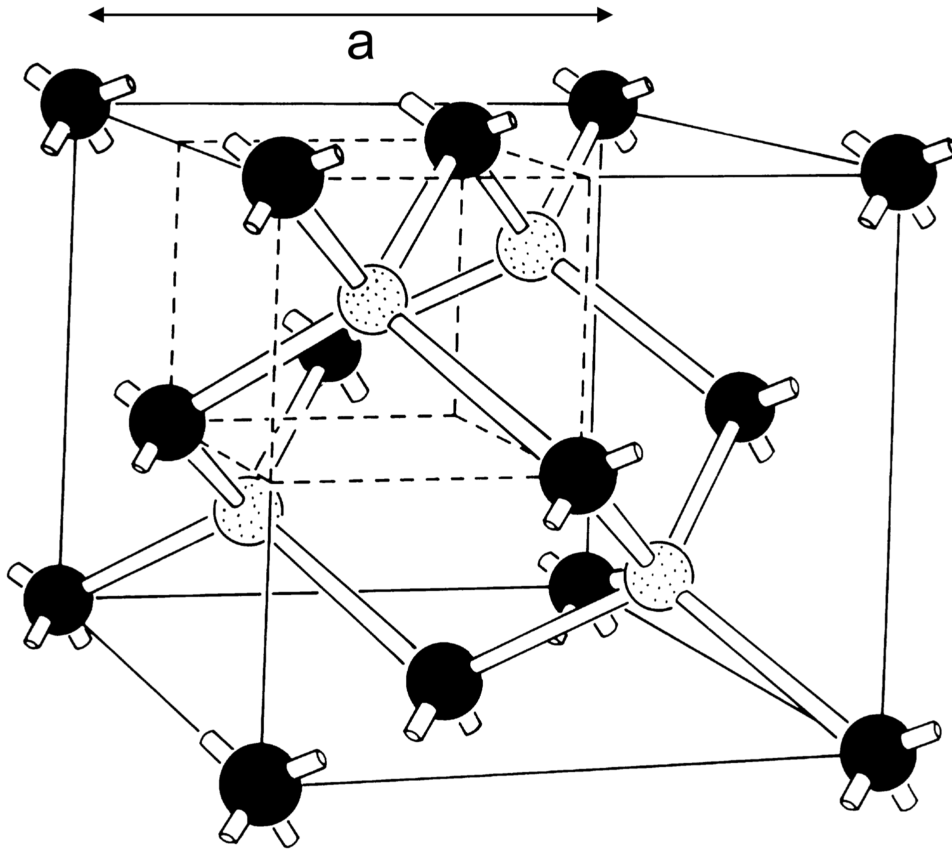
Also bipolar transistors are available: Heterojunction Bipolar transistor: HBT

AlGaAs-GaAs HBT
InGaP-GaAs HBT
AlInAs-GaInAs-InP HBT

Bandgap engineering, HEMT

- Modulation doping
- The heterojunction
- Heterojunction designs
- The principle for the HEMT
- Different HEMT types

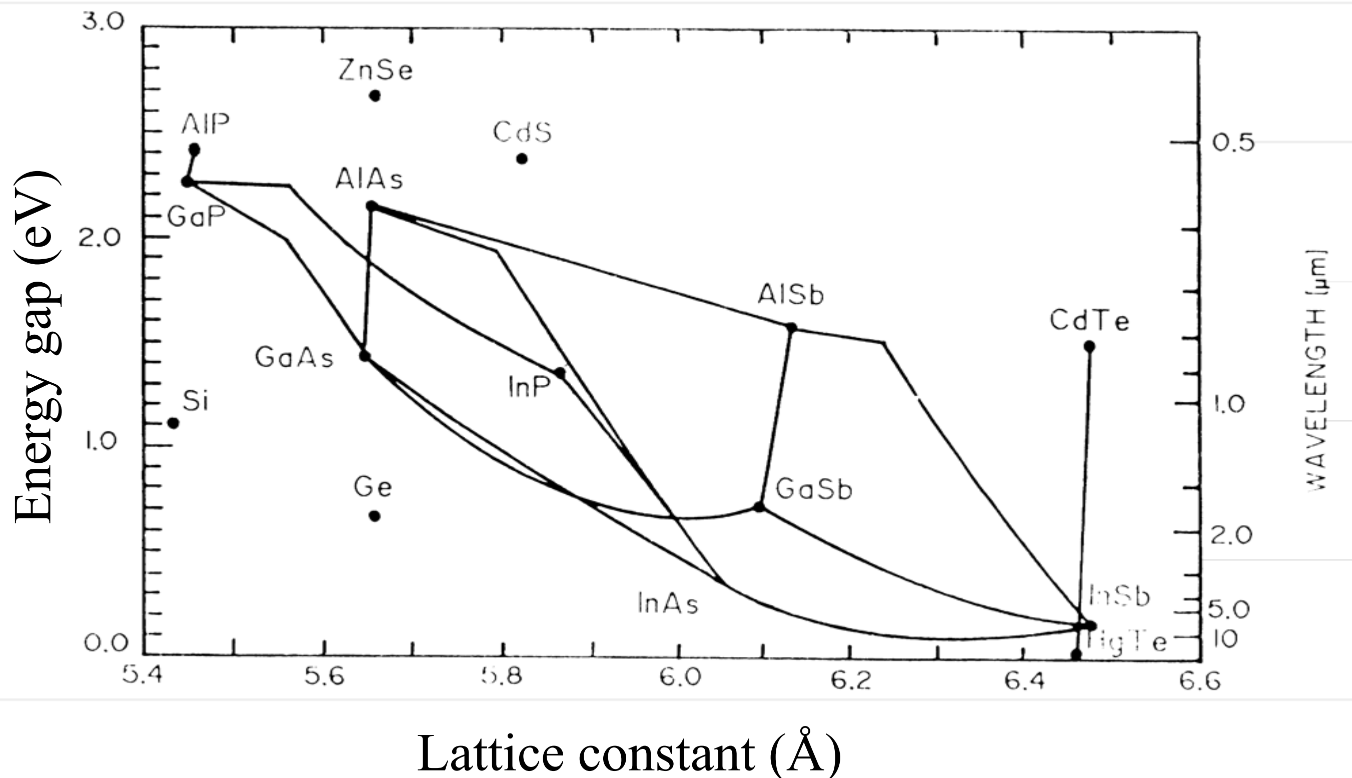
Bandgap engineering



We will study semiconductors with a crystal structure called ‘zinkblende’. The lattice constant ‘a’ is an important parameter for the crystal

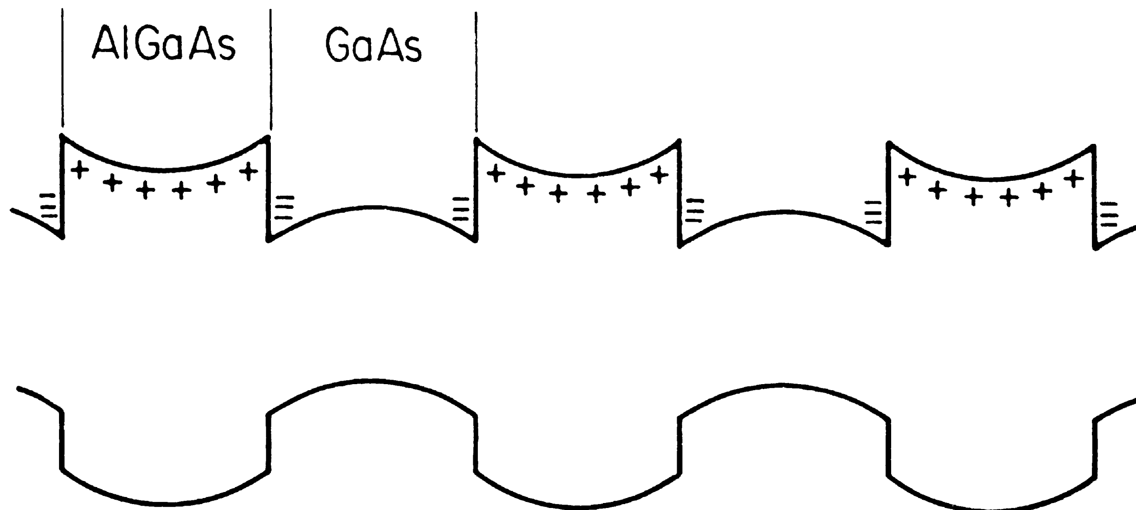
Band gap –lattice constant

The diagram below shows the energy gap versus lattice constant for certain semiconductors. Some semiconductors have similar lattice constant, those can be combined i e ’sandwiched’.

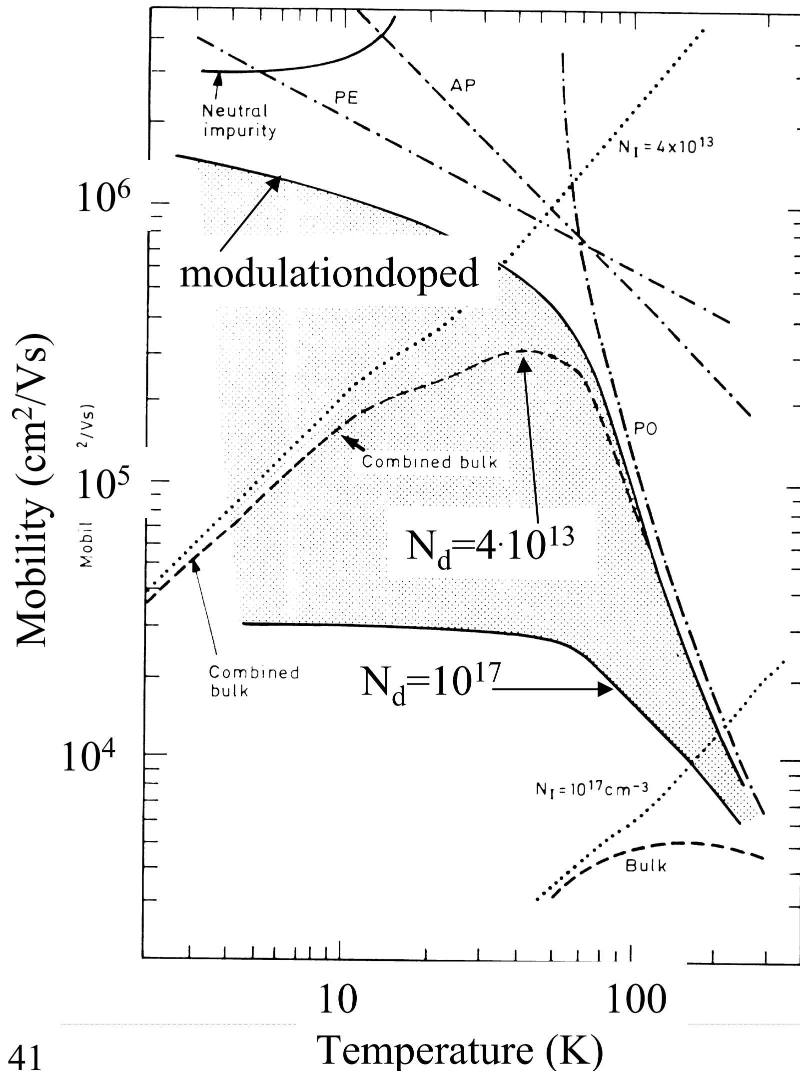


The two dimensional electrongas

The stucture below was the ’breakthrough’ for the ‘bandgap-engineering’. A sandwich-structure with two different semiconductors are grown on a GaAs substrate, see figure below. AlGaAs layer is n-type doped, GaAs layers are undopade. The donors in the AlGaAs layers are normally ionized and their electrons have moved to the GaAs-layers because of lower energy. The electrons are attracted to the positive (immobile) donor charge and the probability of finding electrons is maximum close to the AlGaAs-GaAs junction. The electrons are confined in a thin layer, called a ’two dimensional electrongas’.



Two-dimensional electrongas (2)

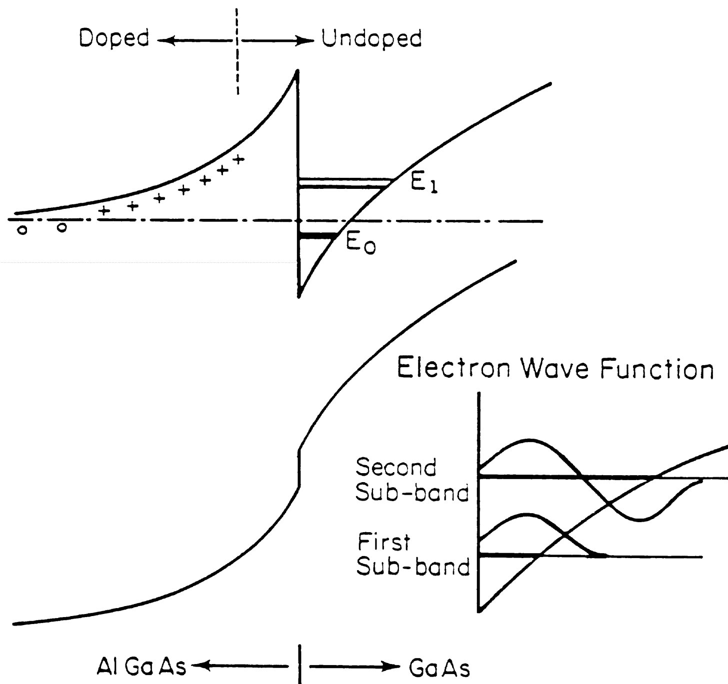


The result of the modulationdoping can be seen in this figure. It shows the mobility of the electrons as a function of temperature for an ordinary GaAs semiconductor with $4*10^{13}$ resp 10^{17} dopants cm^{-3} and the modulation doped material.

The modulationdoped material has a very high mobility especially for low temperatures which is due to the lack of impurity scattering i e electrons do not collide with the doping atoms because they are separated !!!

How can we make practical use of this ?

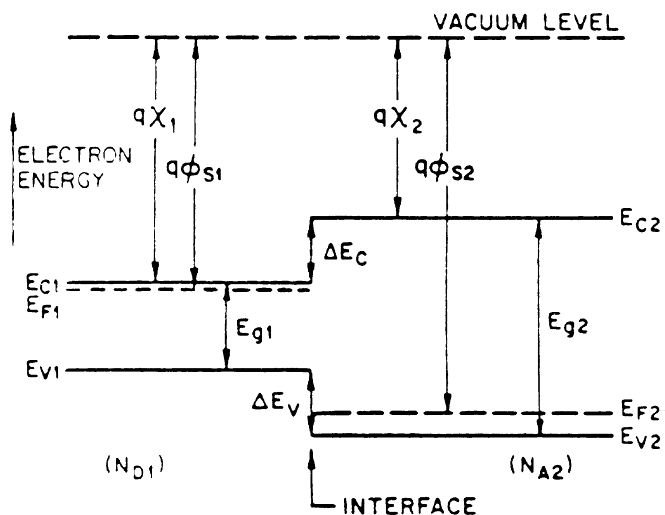
A single heterojunction



The figure shows a single heterojunction between n-AlGaAs och undoped GaAs.
Since the wavelength of the electrons is similar to the dimension of the potential well, the electrons will be quantized i e their energy have certain discrete values determined by the ges av Schrödinger-equation.
The barrier is approximatively triangular, note that the wavefunction has a non-zero value in the AlGaAs

The discontinuity in valence and conductionband

A model describing the value of the discontinuity in the valence and conduction band is the s c 'Anderson electron-affinity-model'. According to this model, the conductionband discontinuity is determined by the difference in electron affinity ΔEc, between the two semiconductors.



$\Delta Ec = q\,X_1 - q\,X_2$

$\Delta Eg = \Delta Eg2 - \Delta Eg1$

$\Delta Ev = \Delta Eg - \Delta Ec$

for AlGaAs-GaAs

$\Delta Ec \approx 0.6\,\Delta Eg$

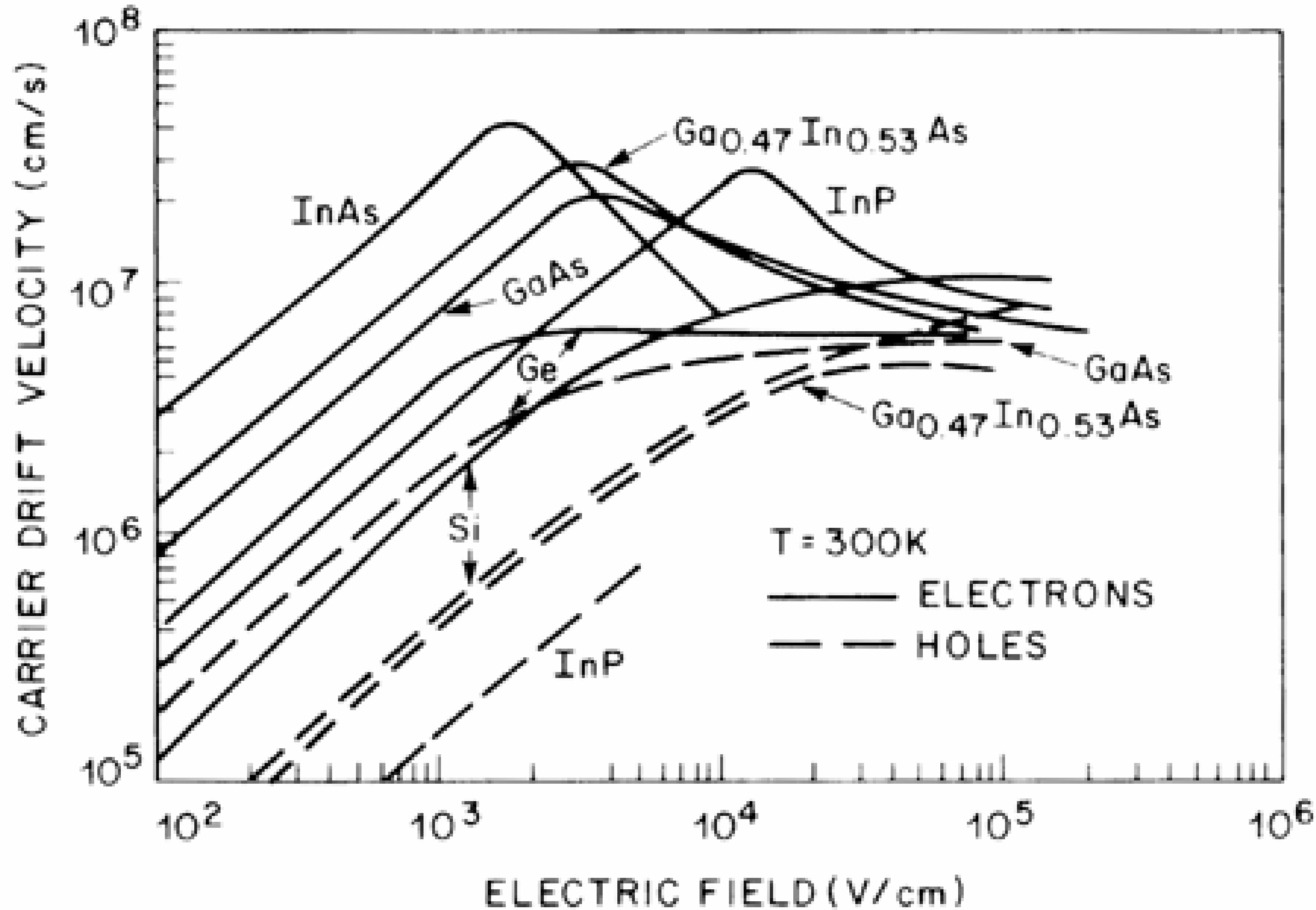
$\Delta Ev \approx 0.4\,\Delta Eg$

Bandgap for different III-V semiconductors

Semiconductor		bandgap eV at 300K	mobility (electron)	effective e-mass
AlP	i	2.45		
AlAs	i	2.163		
AlSb	i	1.58	200	0.12
GaN	i	3.36	380	0.19
GaP	i	2.261	110	0.82
GaAs		1.424	8500	0.067
GaSb		0.726	5000	0.042
InP		1.351	4600	0.077
InAs		0.360	33000	0.023
InSb		0.172	80000	0.0145

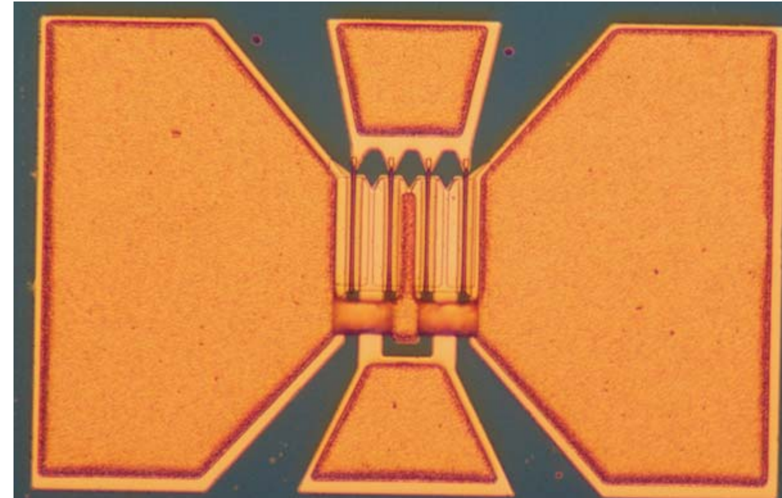
i: indirect bandgap, otherwise direkt

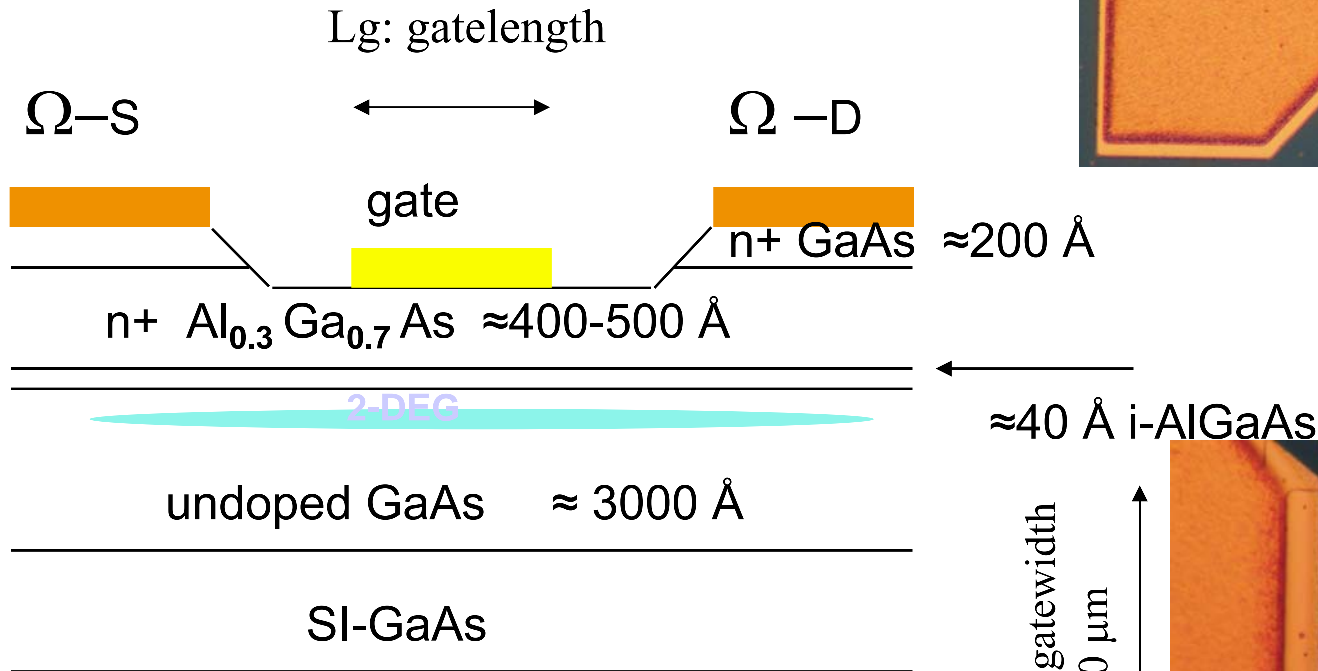
Electron velocity versus electric field for different semiconductors
Important parameter cut-off frequency

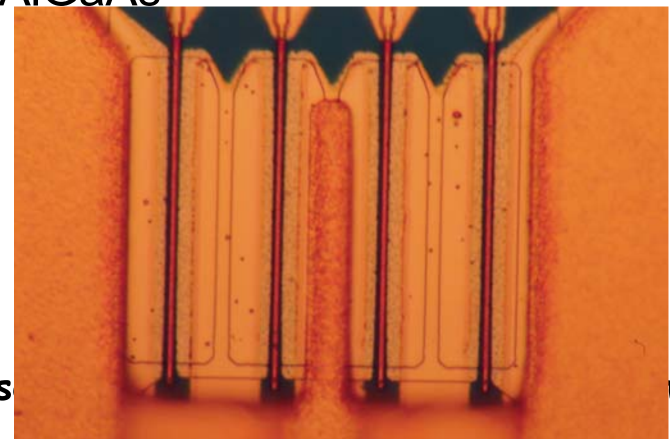


High Electron Mobility Transistor

The High Electron Mobility Transistor was first described by researchers at Fujitsu 1980
The figure shows a cut through a HEMT







Lw: gatewidth of unit cell x number of gatefingers

IEEE MMIC s

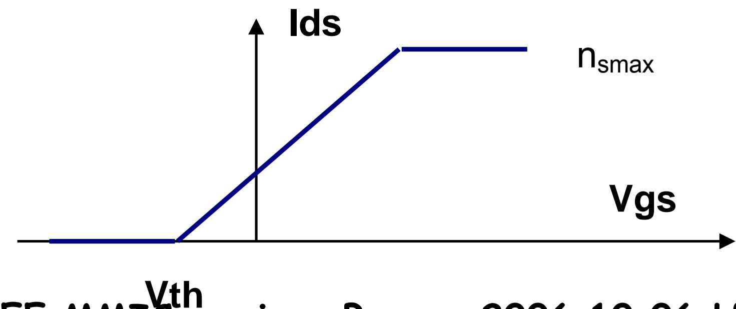
Current transport in a HEMT

The current through the HEMT can be described by following simplified expression

$I_{ds}=L_w \cdot q \cdot n_s \cdot v$ L_w is the gatewidth, q the electron charge
v the average velocity for the electrons

n_s is the charge concentration (cm^{-2}) of the 2-dimensional electrongas.

n_s (Vgs) can be calculated with Schrödinger +Poissons equation
n_s is approximatively:
$n_s = \varepsilon /(q\ (d_d+d_i+\Delta d)) \cdot (Vgs-Vth)$
d_d is the thickness of the n^+AlGaAs layer
d_i is the thickness of the i-AlGaAs layer
Δd is the thickness of the 2-DEG



Current transport (2)

For $V_{gs}=V_{th}$, the transistor is pinched-off i e Ids=0

$V_{th}=\phi_b-\Delta Ec- q N_d d_d^2/2\varepsilon +\Delta E_{f0}$

ϕ_b =barrier height of the gate Schottky

The threshold voltage is quadratically dependent on d_d !!!!

Other useful expressions:

$f_T=v_{sat} / 2\pi Lg$

$g_m=\varepsilon\ v_{sat}\ Lw/ (d_d+d_i+\Delta d)$

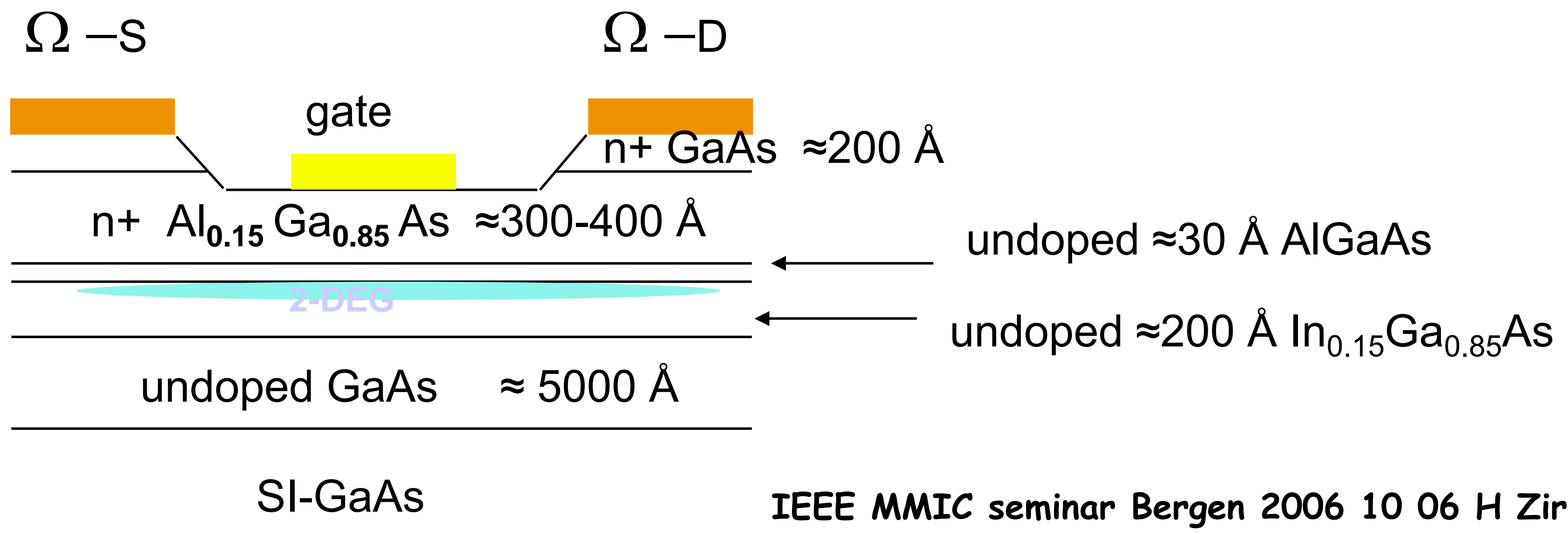
g_m is the transconductance of the HEMT and is typically 300-1500 mS/mm depending on the type of transistor

ε is the dielectric constant for the semiconductor

HEMT with InGaAs-channel: pHEMT

The most popular HEMT today has a InGaAs channel with 15-20% indium. InGaAs has a different lattice constant compared to GaAs, and the channel-layer has to be thin ≈200Å in order to avoid dislocations.

Advantag: higher electron velocity, and higher n_s>gives a higher maximum current per unit width

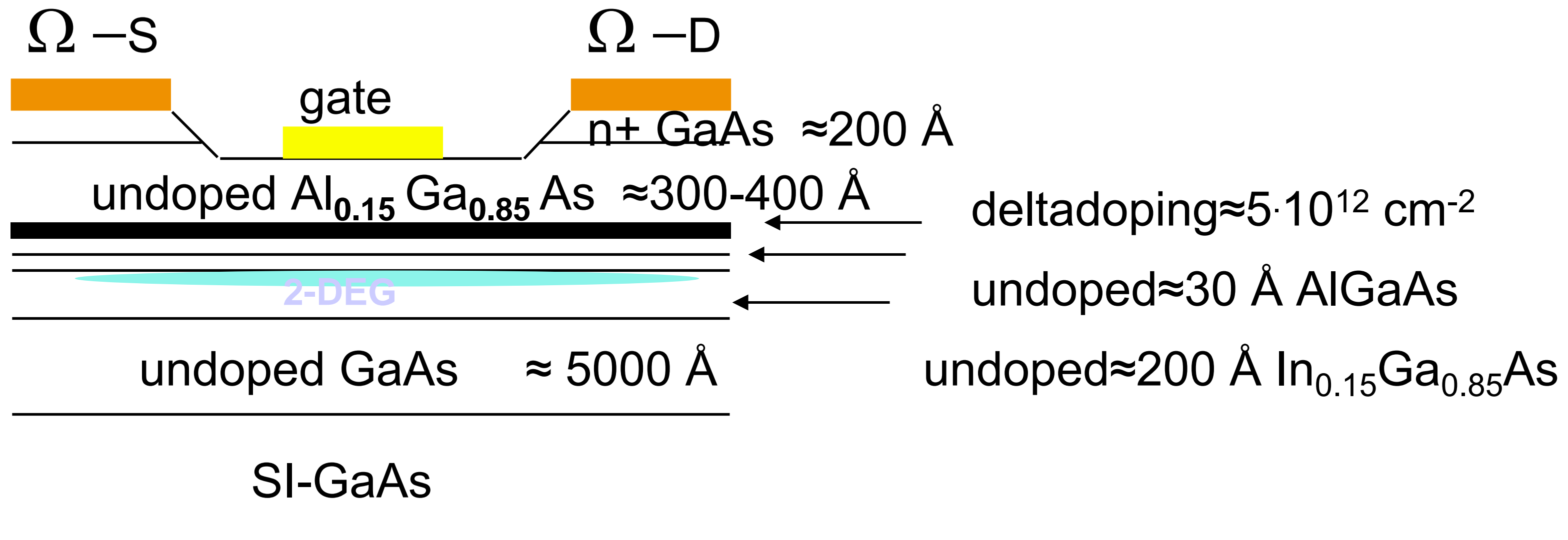


deltadoped HEMT with InGaAs-channel

Next improvement is the deltadoping i e the doping atoms are all confined very close to the channel but in the AlGaAs layer which is *undoped*

Advantage: as the InGaAs channel, but V_{th} is proportional to d_d (better control of the threshold voltage)

Common for low noise circuits up to millimeterwave frequencies

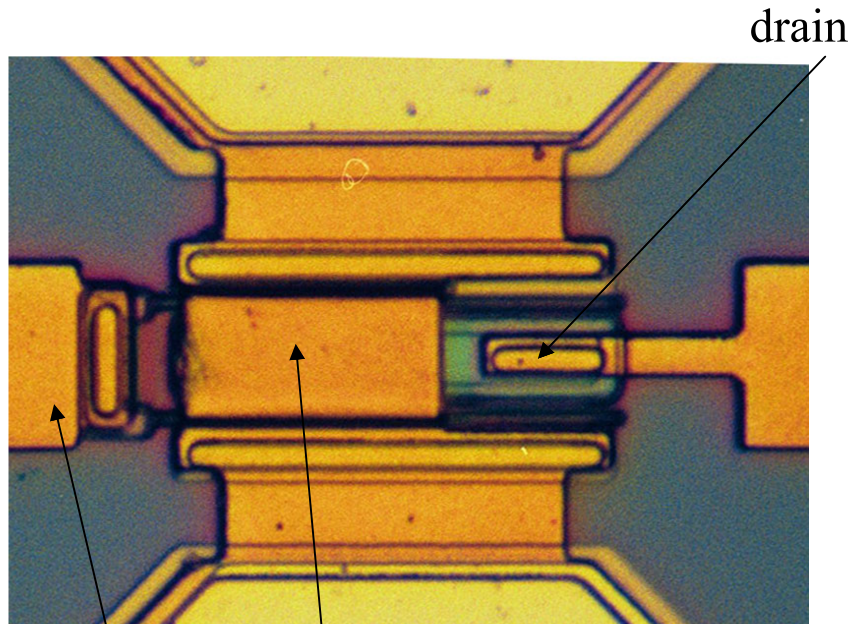


Double deltadoped HEMT with InGaAs-channel

'Industry standard' combine high power with low noise
Offered by many foundries such as WIN, Triquint, OMMIC

Example: D01PH process from OMMIC: f_{T}/f_{MAX}=100 /180 GHz

photo of 2 · 50 µm L_w HEMT

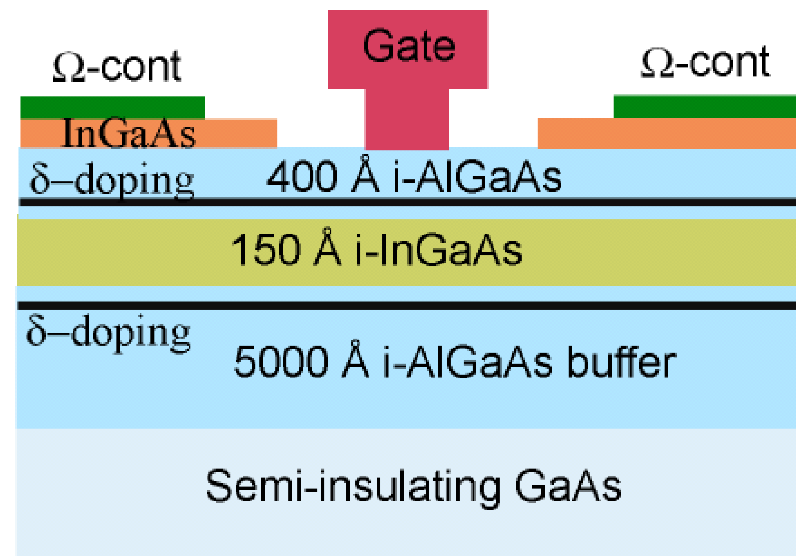


drain

Gate pad

Airbridge connecting the sources

Mushroom gate, 0.14 µm gate length



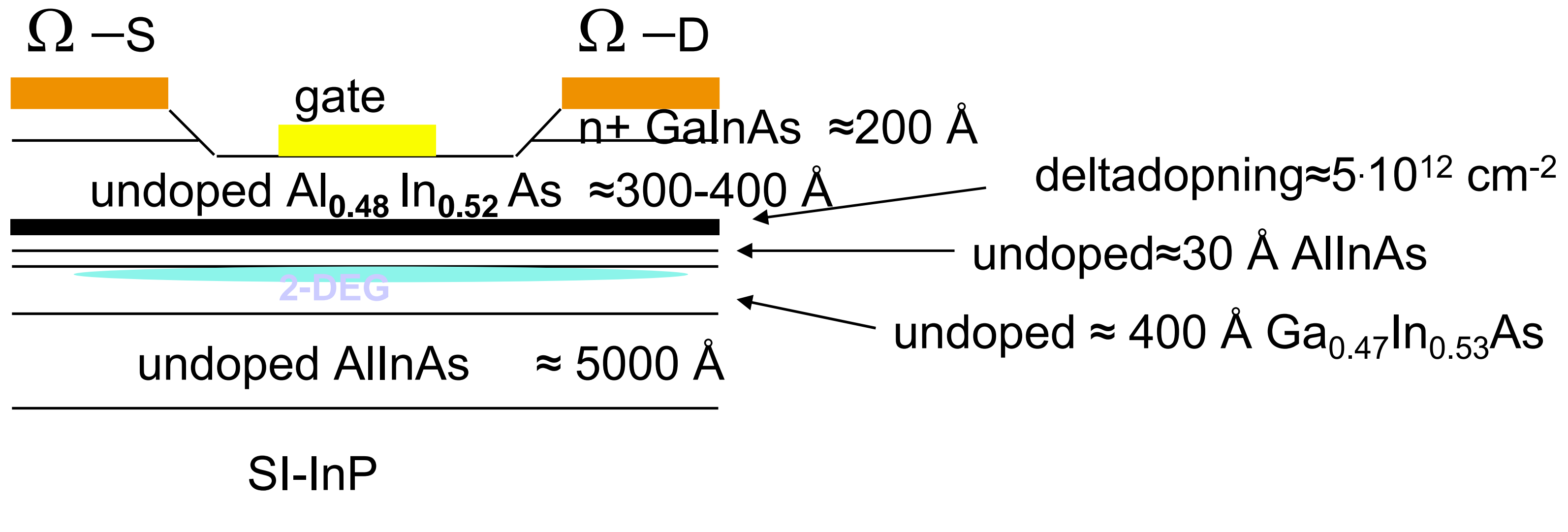
InP-based HEMT with $In_{0.53}Ga_{0.47}As$-channel

State of the art results for HEMT is demonstrated on InP !

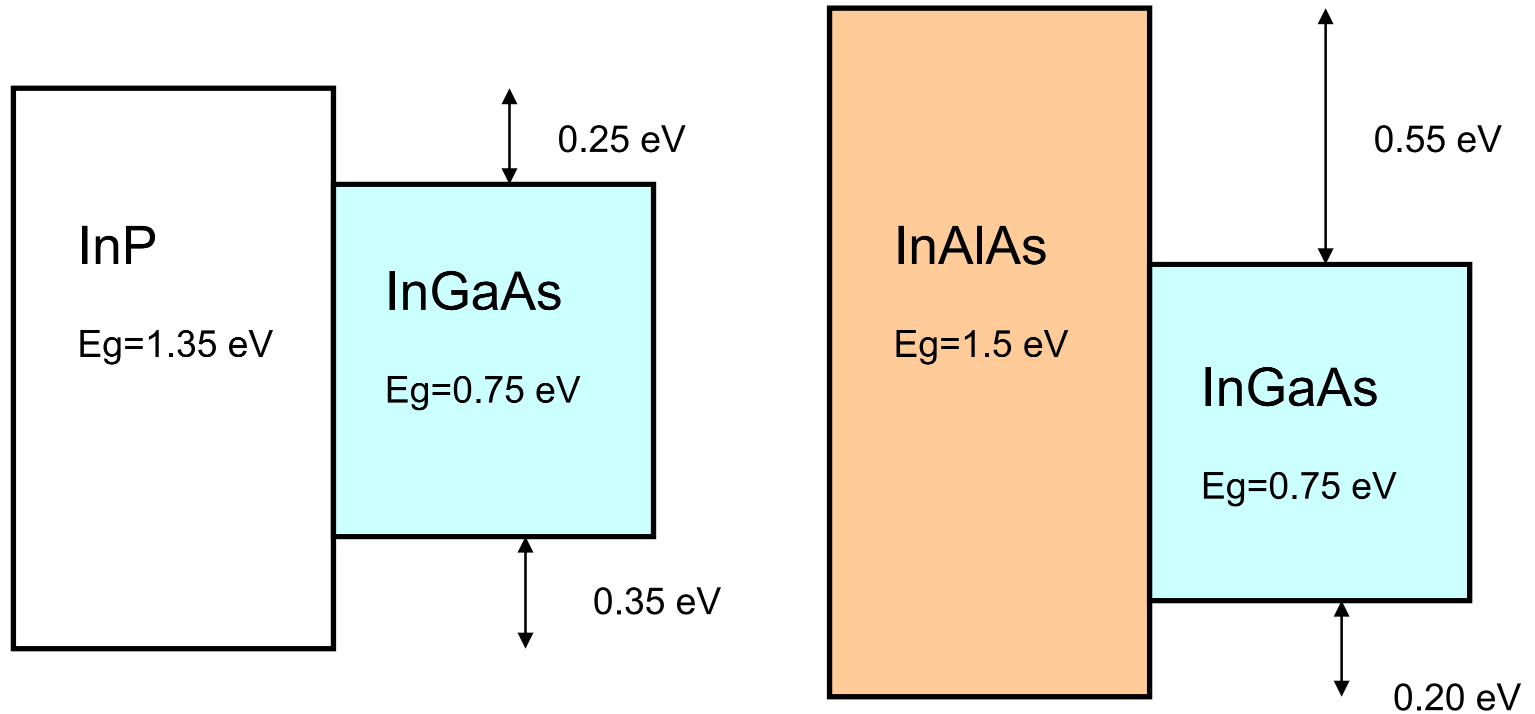
In-content can be increased >50% electron velocity and mobility are increasing.

ΔEc=0.55 eV -> better confinement of 2-deg electrons

$f_{MAX}\approx$400 GHz, f_T > 300 GHz, Fmin≈1.3 dB at 100 GHz



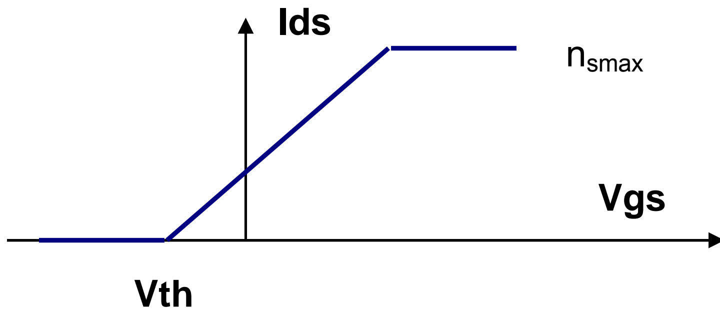
Band line-up for InP-matched materials



The semiconductor foundry provide models and tools for layout generation in a ’design kit’ for various CAD-software like ADS and Microwave office….

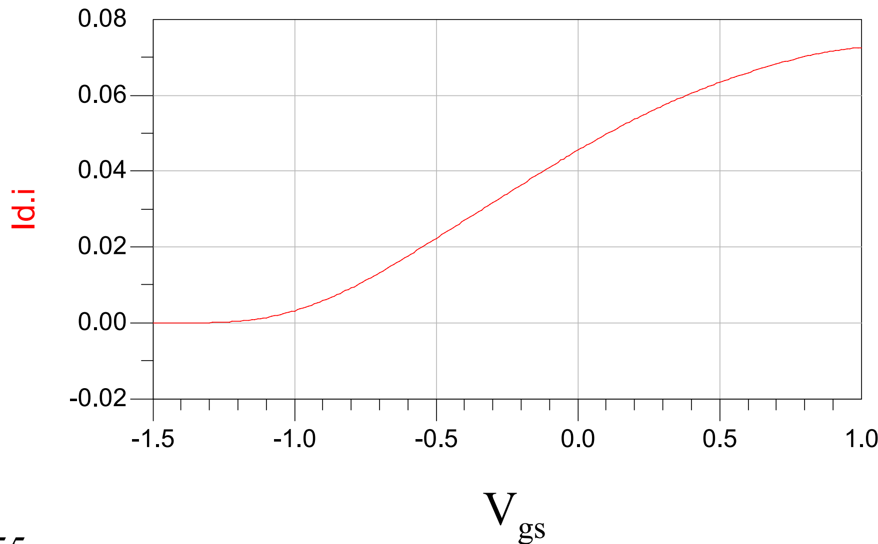
Let’s take a look at a pHEMT transistor based on the models provided by the foundry WIN. The process is called PP-15 and is a 0.15 μm gatelength pHEMT.

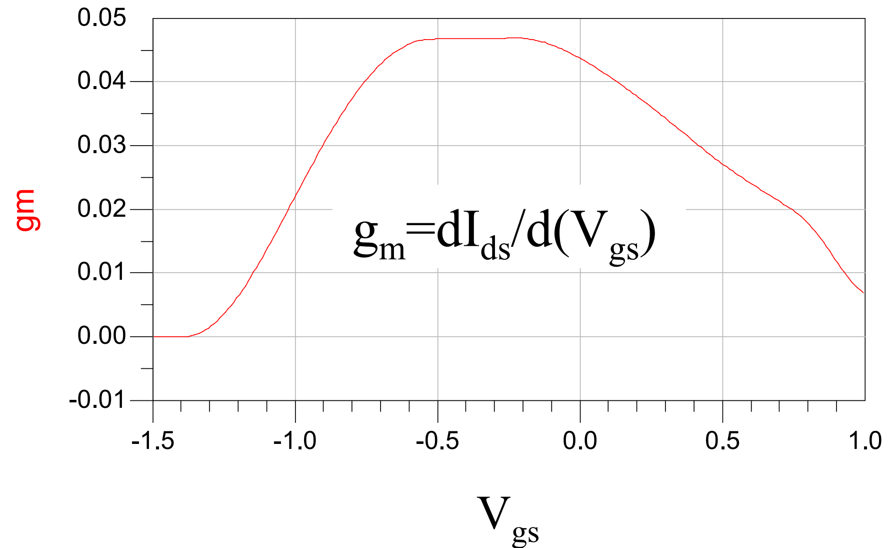
this was our simple analythical model, remember ?



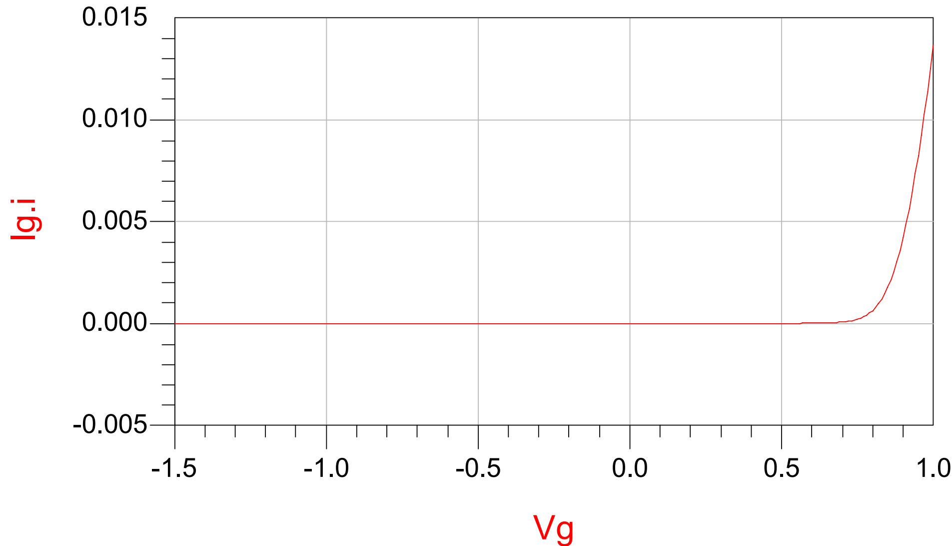
advantage: gives some insight to the physics
However, too simple for circuit design:
V_{ds} dependence lacking
discontinous derivatives, g_m either zero or constant

This result is obtained by using the foundry-model (EEHEMT): V_{ds}=2V in the simulation
Be careful using gate voltage above 0V, the Schottky diode will conduct at 0.7V !!

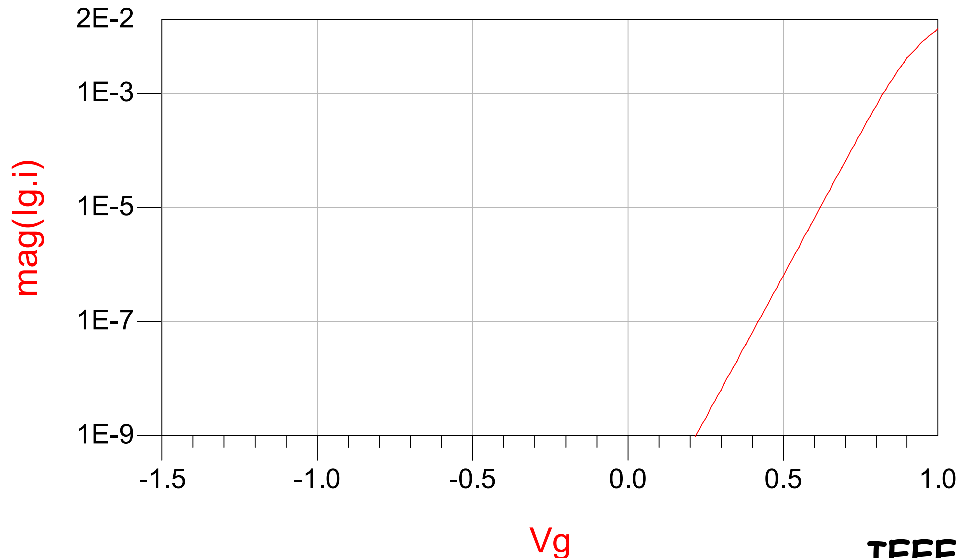




Linear scale:



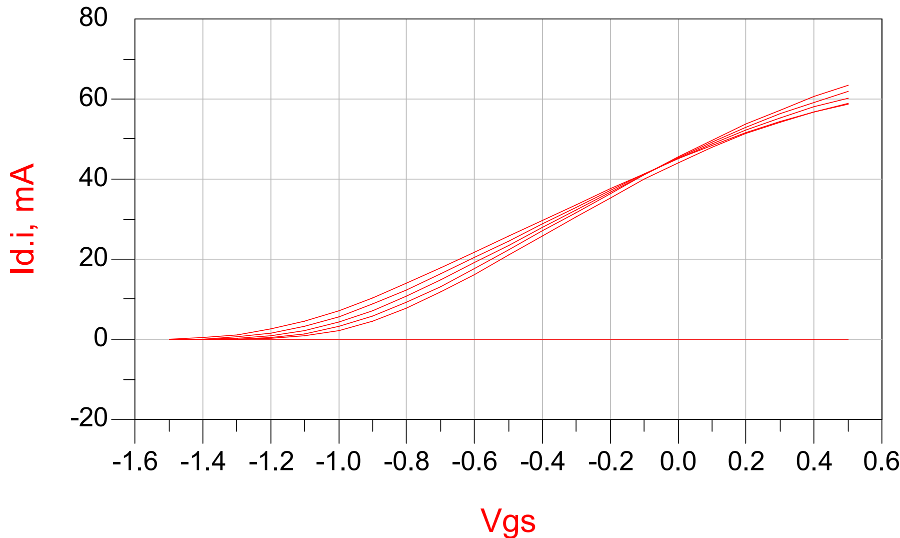
Logaritmic scale:



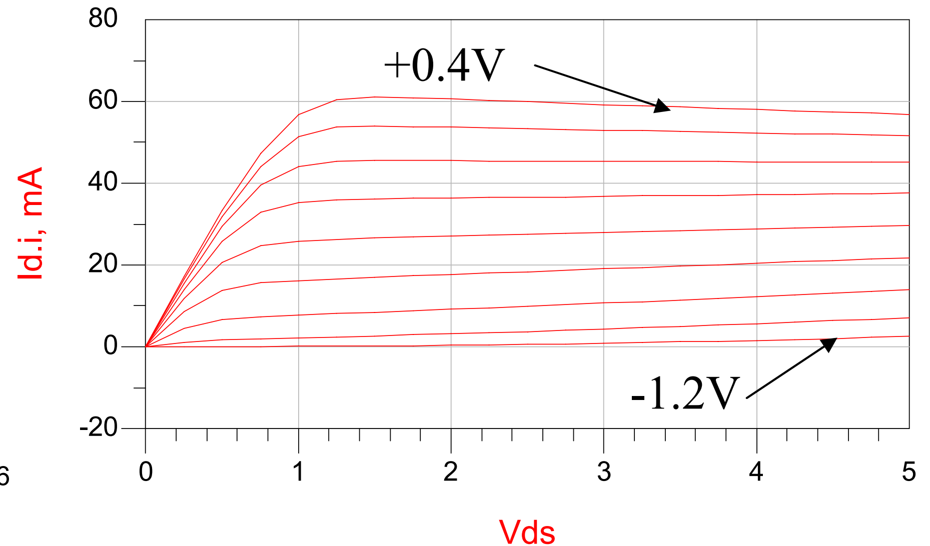
Gate current add noise in a circuit and should be avoided. At levels above a few 100 μA/mm the reliability might be jeopardized. Always remember to check the gatecurrent in your circuit.

More I-V characteristics…

Vds=0, 1, 2, 3, 4, 5 V



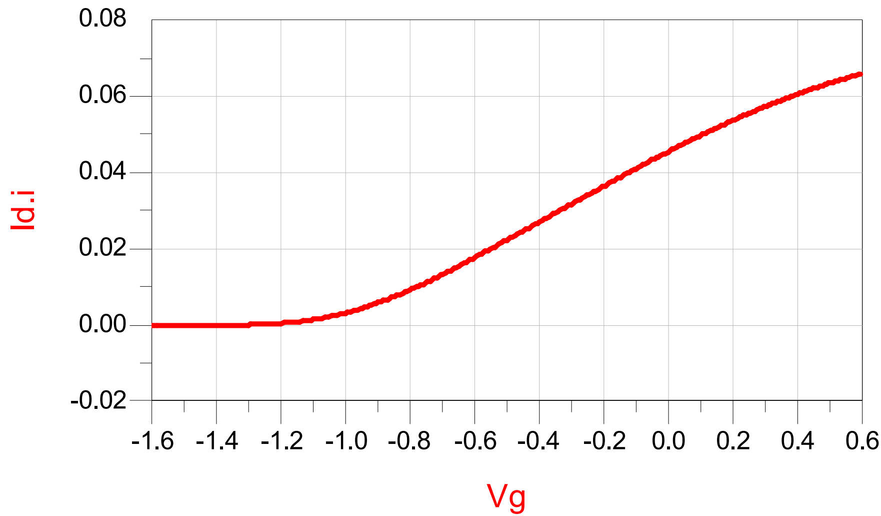
Vgs=-1.2, -1.0……+0.4V

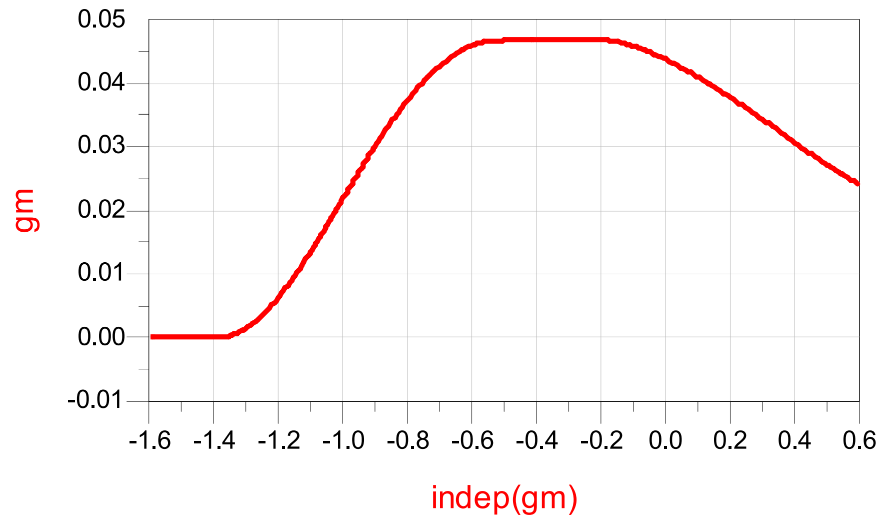


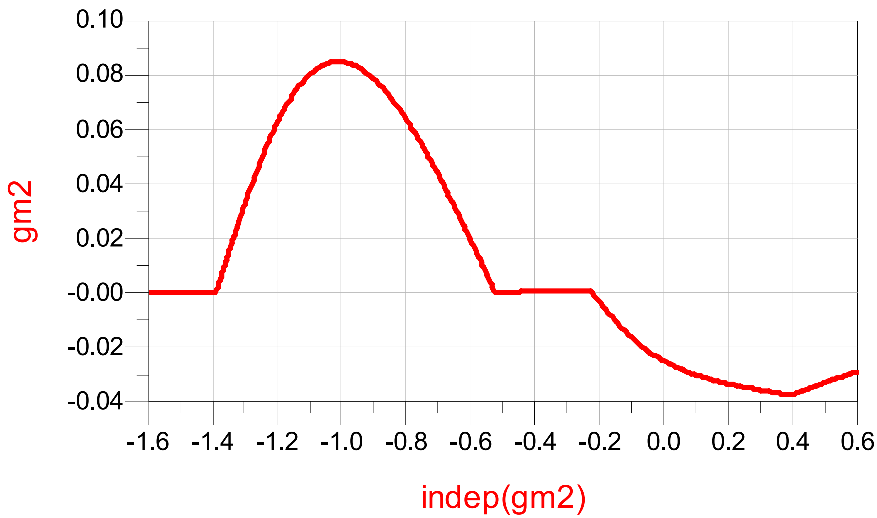
Always check a model before designing, by investigating the dc-characteristics, S-parameters, noise-parameters etc. Don't expect **ANY** model to perfectly describe the characteristics of the component.

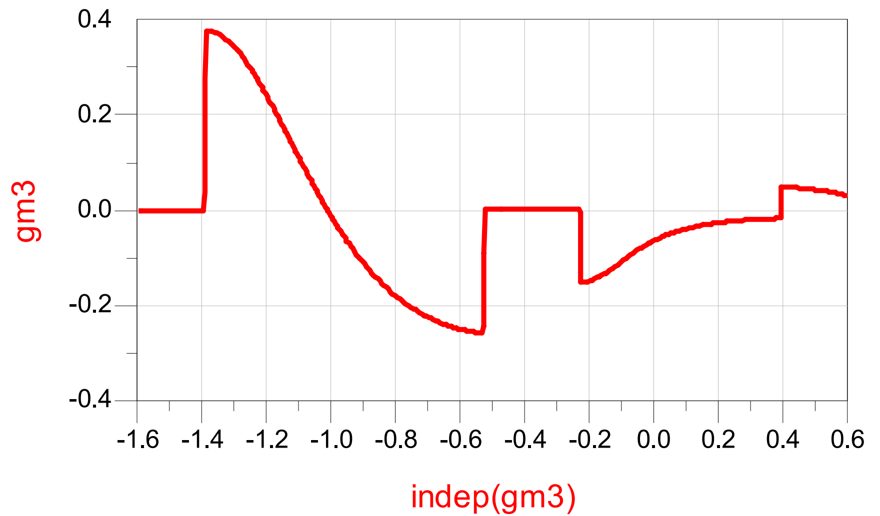
Just an example……

The Ids/Vgs characteristics and its derivatives are plotted below
2nd and third derivatives look strange….

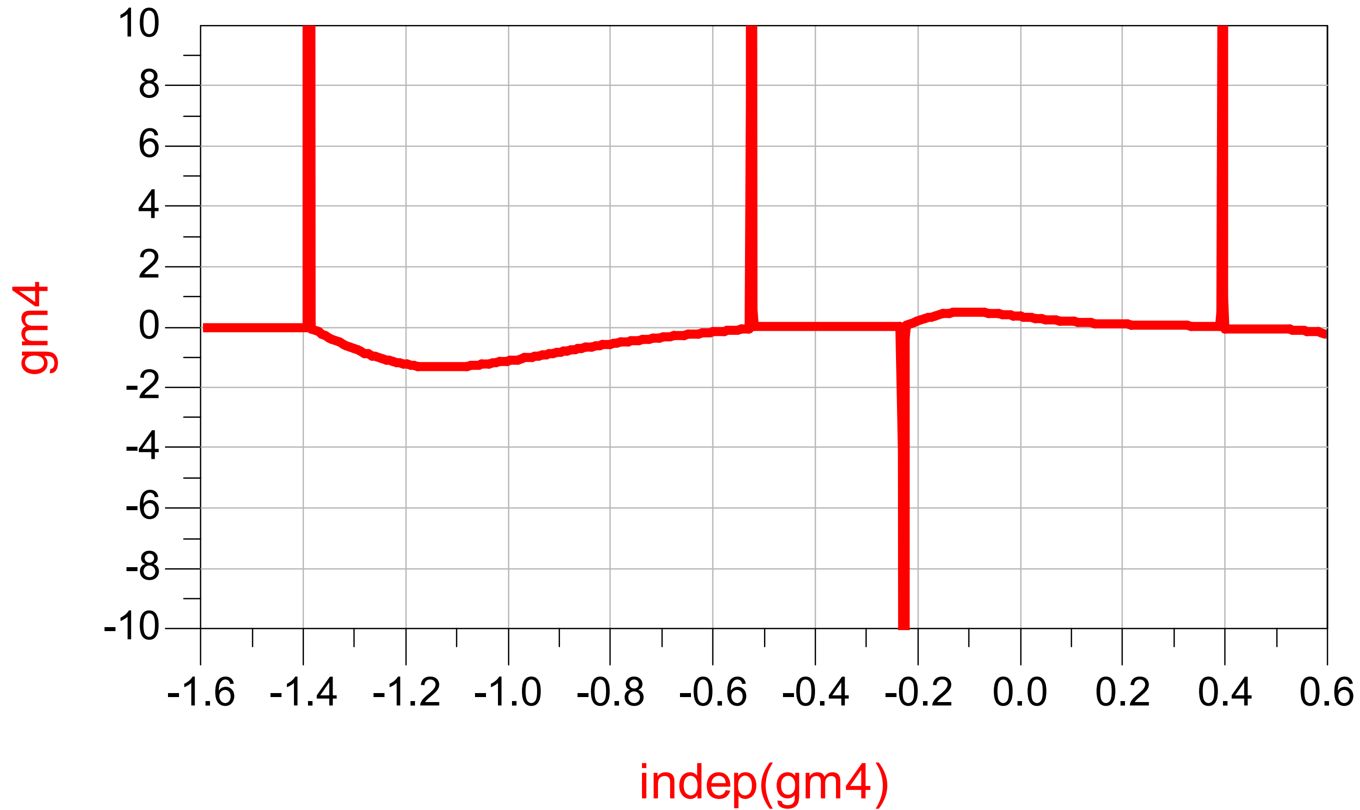




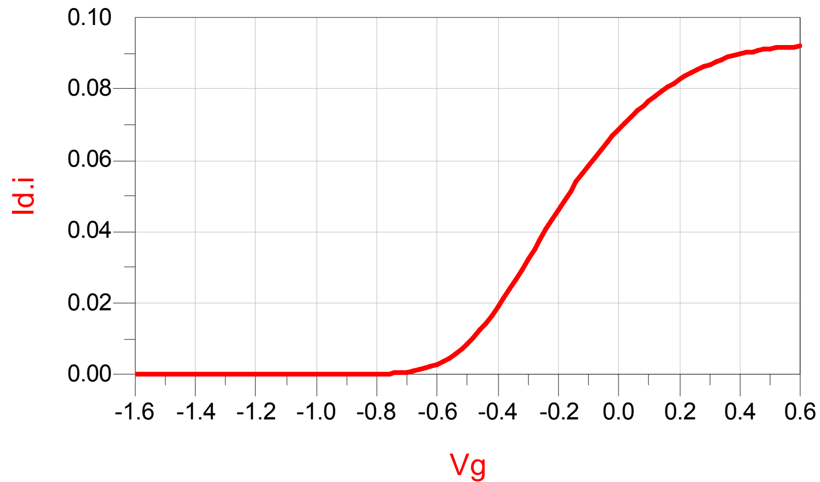


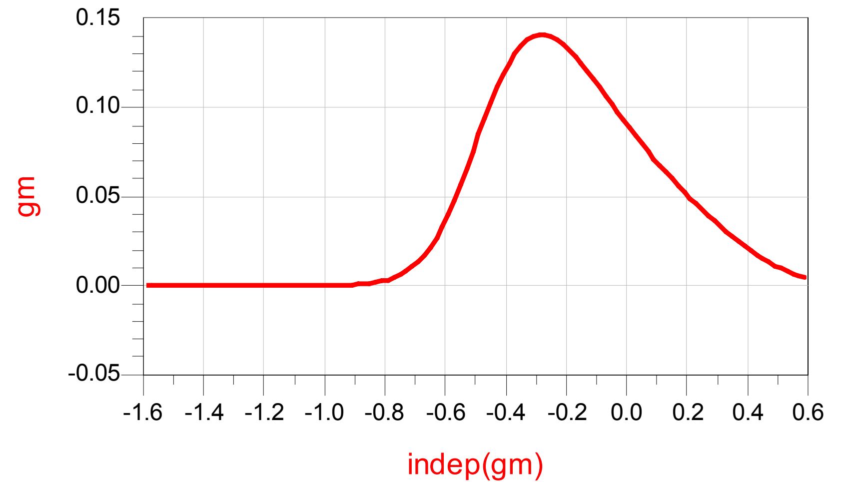


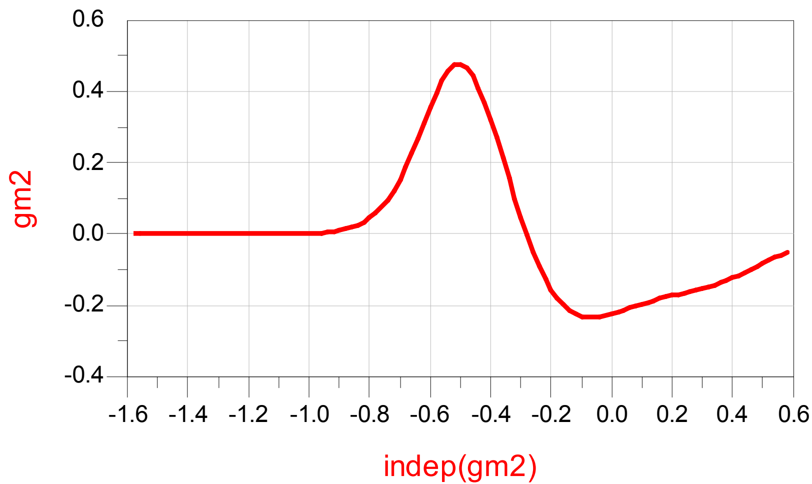
Fourth derivative gives deltafunctions….

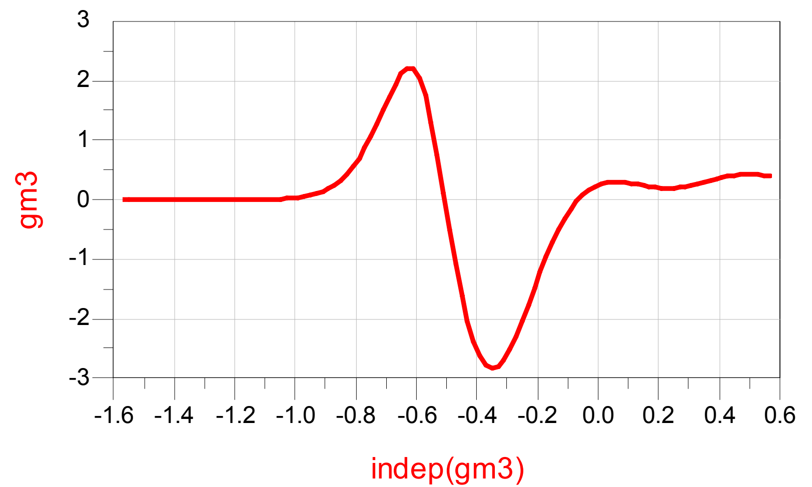


’Chalmers model’: 2x75 µm mHEMT device :





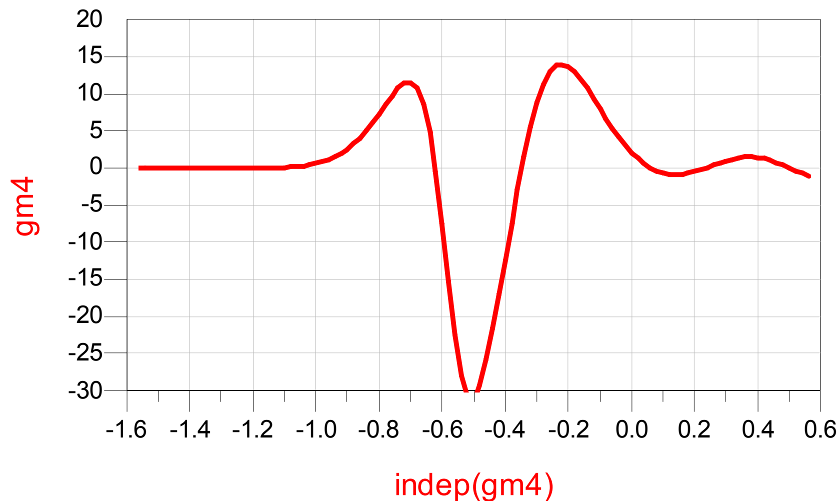


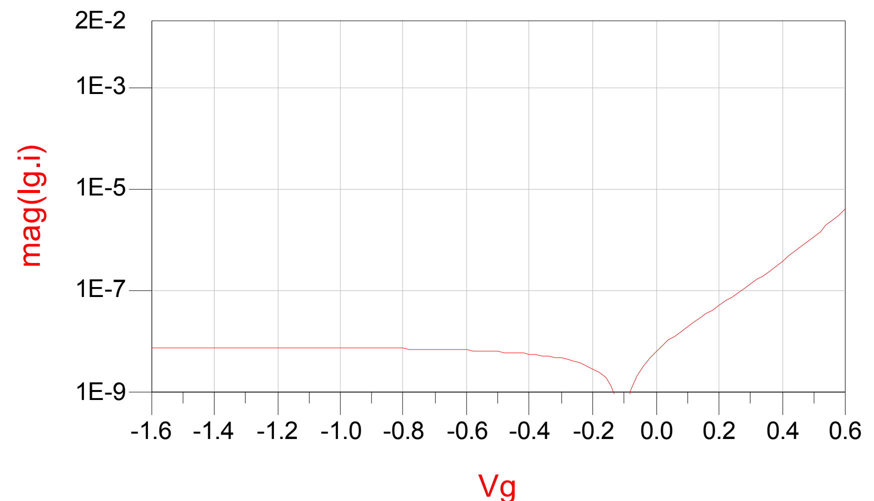


Now the fourth derivative is continous, in addition reverse gatecurrent exists…

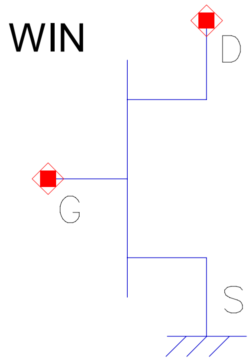
In most cases, the EEHEMT model is ok….

Just be careful with using models, try to judge how well the model can predict reality !
A model should also be **scalable** i e the transistor geometry, for example L_w can be a model parameter.



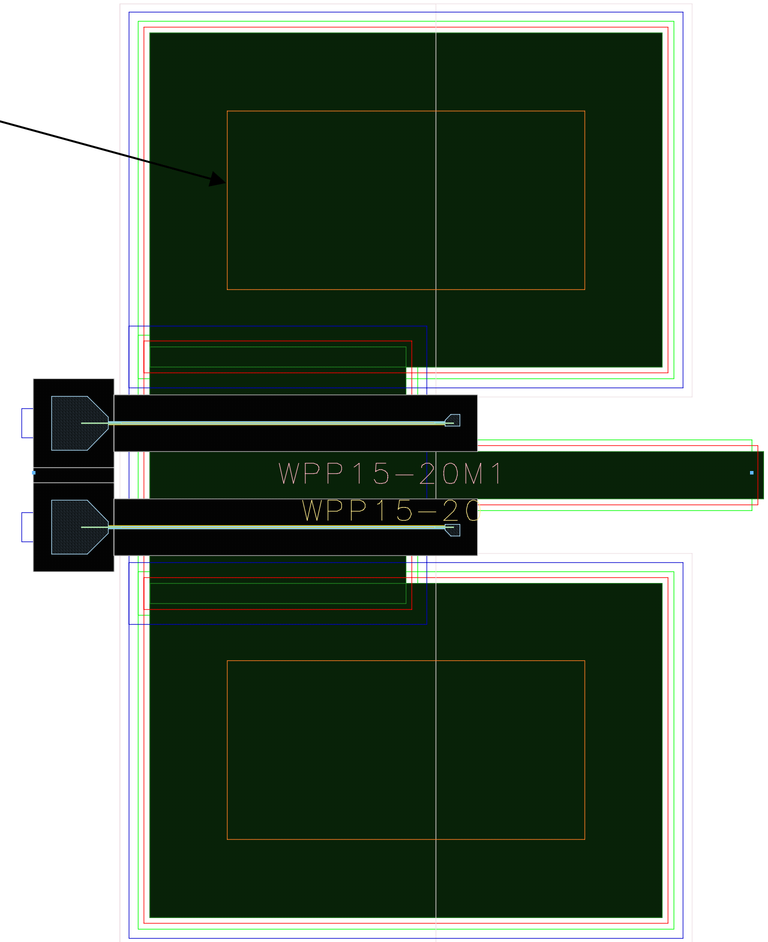


Transistor layout 2x50 μm gatewidth
Slot via for grounding

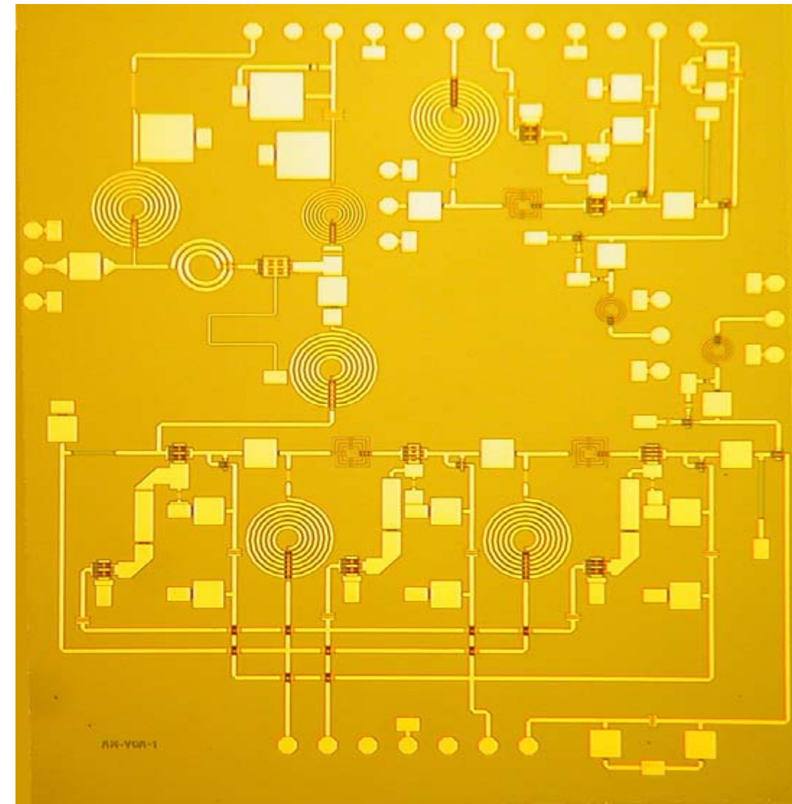


WPP15-20
WPP15-20M2
NOF=2 ← Number of gatefingers
Ugw=50 um ← Unit gatewidth

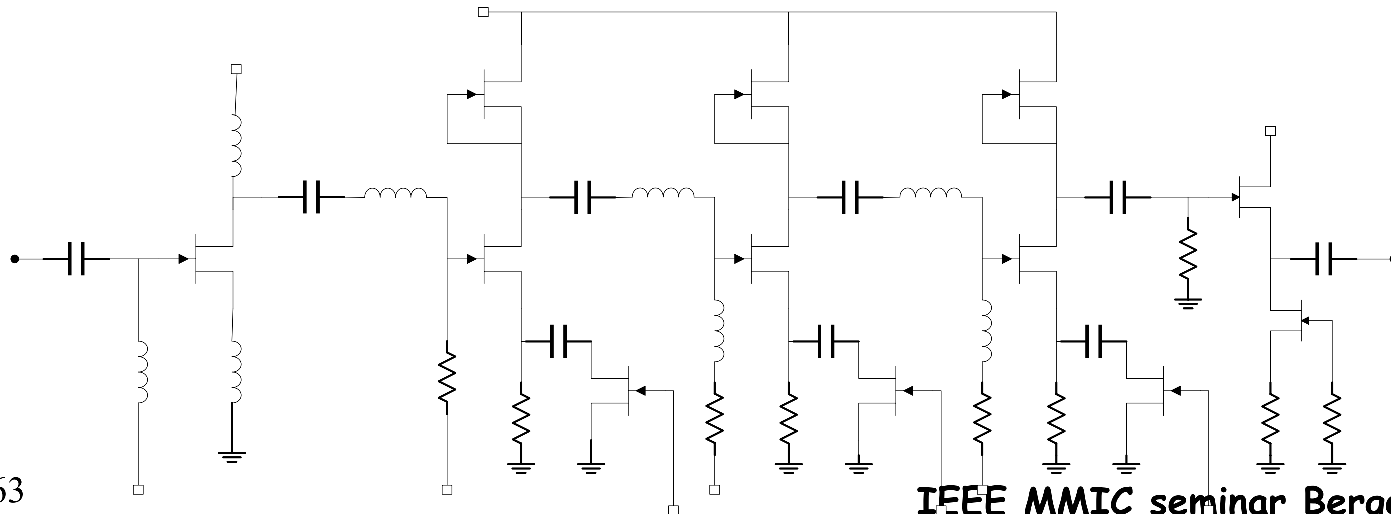
Slot-via



RC-design technique



Design example: Variable Gain Amplifier, VGA
2.5 GHz 45 dB gain, 45 dB gain variation



Summary RC design technique

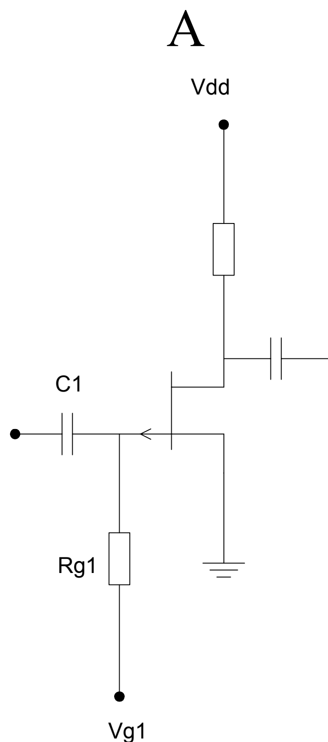
Can be used at low frequencies compared to f_T and f_{MAX}
Cost effective since circuit area is small
CS-stage as amplifying stage
CG -stage as input matching
CD -stage as output matching
Differential stage popular for many circuits functions
Suitable for both FETs and BJTs

Bias circuits

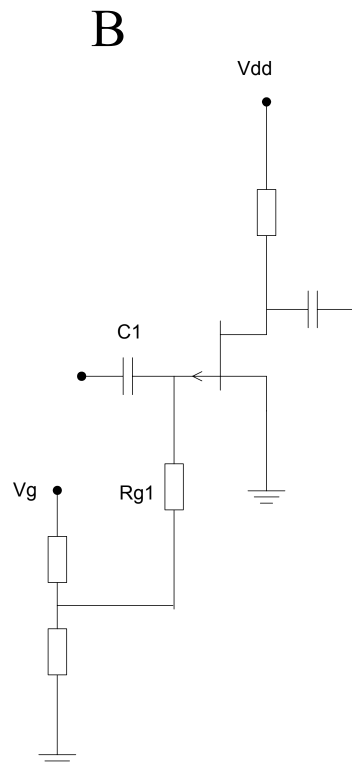
Necessary to set the operating point, I_{DS} ,of the transistor

A: direct gate bias. optimum bias set for each transistor, complicated bias supply ?
B: one bias voltage for many stages, simplified biassupply, no individual bias
C: selfbias. Good solution if low freq. RF-response not important
D: bias utilizing biasing diodes, 0.5-0.7 V per diode, attenuation of bias noise

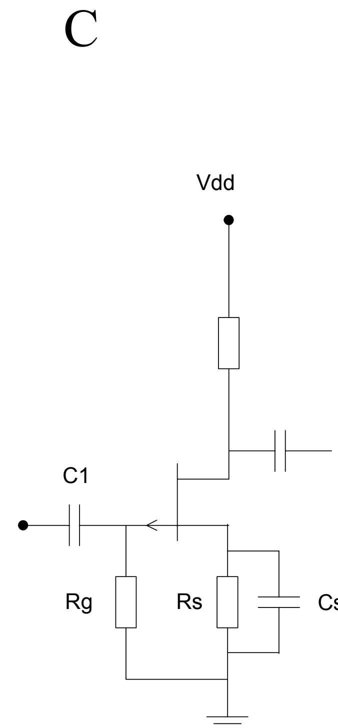
A



B



C



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