Analog MMICs for microwave and millimeterwave applications based on HEMTs

Herbert Zirath

Microwave Electronics Laboratory
Department of Microtechnology and nanoscience
Chalmers University of Technology
Göteborg, Sweden

Outline

-PHEMT MMIC-technology

Amplifiers

- -Feedback amplifiers
- -low noise millimeterwave high gain amplifiers

Frequency Multipliers

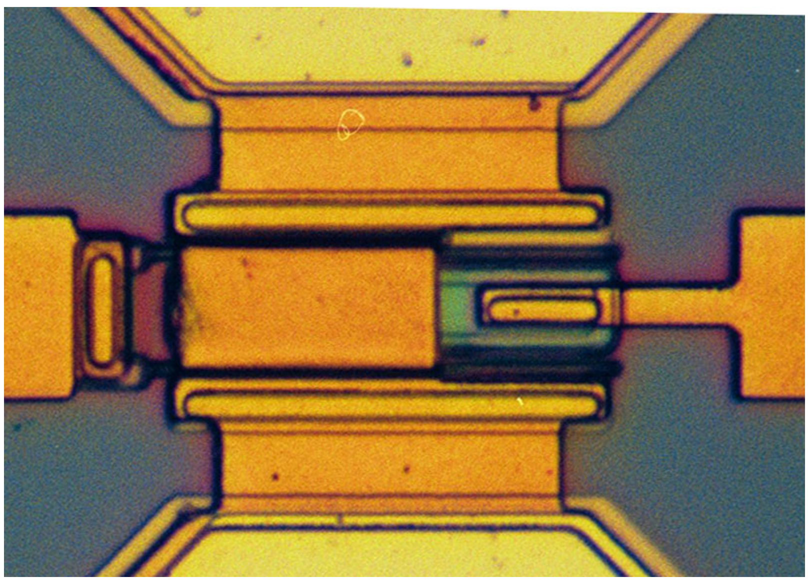
Oscillators

Frequency mixers

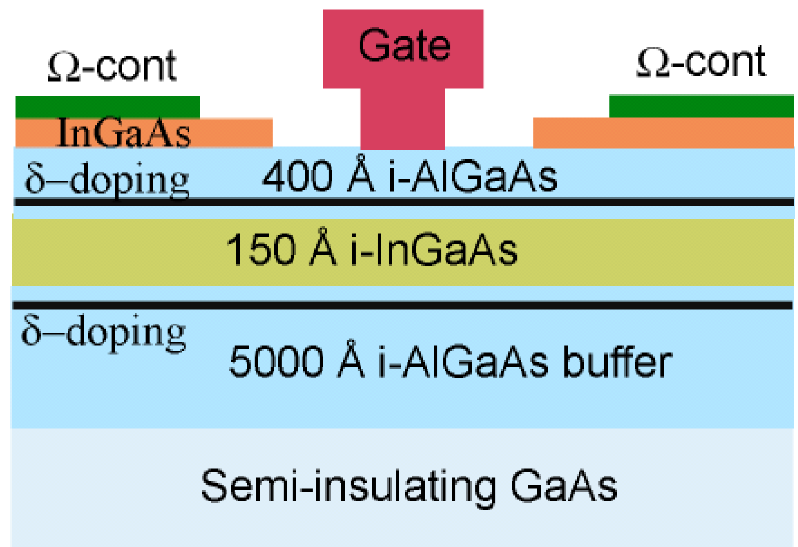
The MMIC-technology

The D01PH process:
Ft=100 GHz, fmax=180 GHz

Top view of 2 · 50 μm L_w HEMT



Mushroom gate, 0.14 μm gatelength



D01PH MMICs designed & fabricated for 60 GHz WLAN

Amplifiers:	M=Measured, S=Simulated
3 stage 60 GHz amplifier Lw=2*15 um	M/ f=57-60.8GHz, G=17dB, P_{DC}=27mW
3 stage 60 GHz amplifier Lw=4*15 um	M/ f=54.3-60GHz, G=17.6dB Pout=15mW P_{DC}=60mW
1 stage 60 GHz amplifier Lw=4*25 um	M/ f=35-65.0GHz, G>6dB, Pout=40mW
3 stage 60 GHz amplifier Lw=8*40 um	M/ f=40-65.0GHz, G>14dB, Pout=200mW
2-18 GHz feedback-amplifier, 2-stage	M/G=22 dB, NF=2.7 dB, P_{DC}=100mW
1-20 GHz feedback-amplifier, 1-stage	M/G=12 dB, NF=2-3 dB. Pout=19dBm
1-10 GHz feedback-amplifier, 1-stage	M/G=14 dB, NF=2-3 dB. Pout=21dBm
2-27 GHz feedback-amplifier, 1-stage	M/G=9-11 dB, NF=2-3 dB. Pout=16dBm
1-8 GHz VGA	M/G=12 dB Gain control=12 dB

Frequency multipliers:	
Active 7.3-8.6 GHz doubler+doubler (29.2-34.4)	M/G=-4 dB@0dBm, P_{DC}=27 mW
Active 7.0-8.5 GHz quadrupler (28-34)	M/G=-13dB@0dBm, P_{DC}=30 mW
Resistive doubler 24 to 31 GHz	M/G=-10 dB@5dBm, P_{DC}=0 mW
Active doubler 25 to 30 GHz (CF)	M/G=2 dB@5dBm, P_{DC}=275 mW
Active doubler 27 GHz (HZ)	M/G=4dB@0dBm, P_{DC}=66 mW
Active doubler 14-17 GHz (HZ)ED02AH	M/G=4.7 dB@0dBm, P_{DC}=60 mW
Active tripler 8-24 GHz D01PH	
Balanced doublers D01PH	

Mixers:

50-65 GHz single resistive HEMT-mixer	M/Lc=8dB@PLO=4dBm, P_{DC}=0
30-60 GHz balanced wideband resistive HEMT-mixer	M/Lc=8dB @ PLO=9dBm, P_{DC} =0
15-30 GHz balanced wideband resistive HEMT-mixer	M/Lc=7dB @ PLO=10dBm, P_{DC} =0
55-65 GHz image reject resistive HEMT-mixer	S/Lc=8dB @ PLO=10dBm, P_{DC} =0

Oscillators:

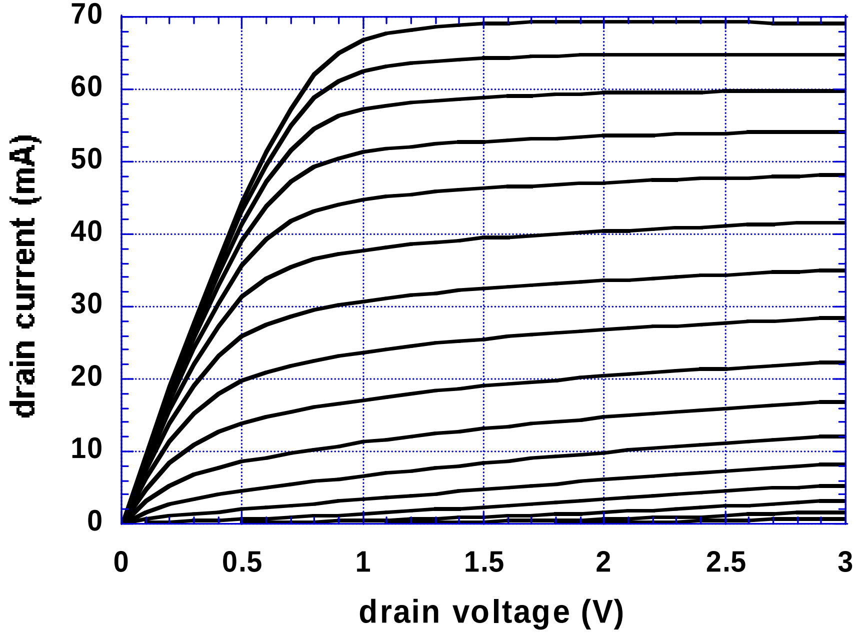
VCO 7.5 GHz	L=-74dBc @100kHz, Pout=6-7dBm, P_{DC}=160 mW
VCO 14.5-15.2 GHz	L=-59dBc @100kHz, Pout=8 dBm , P_{DC}=160 mW
VCO 29-30 GHz	L=-53dBc @100kHz, Pout=11 dBm, P_{DC}=160 mW
VCO 52.4-53.2 GHz	L=-45dBc @100kHz , Pout=-1 dBm, P_{DC}=160 mW
SiGe HBT balanced Colpitt	L <-108dBc @100kHz at 5 GHz, Pout -5dBm, P_{DC}=50 mW
Balanced Colpitt oscillators	7-7.5, 14-15 GHz
Negative gm-oscillators	7-7.5. 14-15 GHz

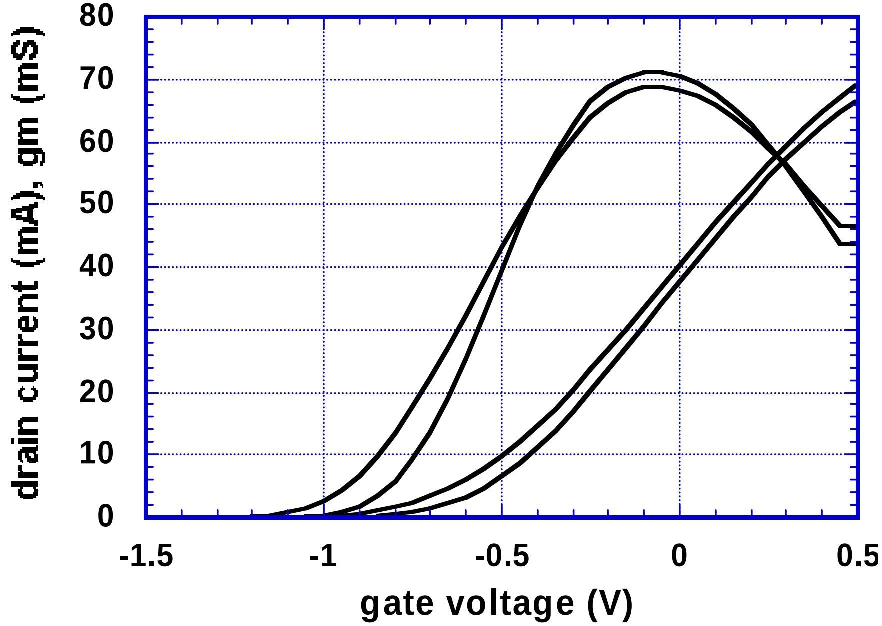
Frequency dividers:

Regenerative freq div 14 to 7 (6.3-7.5) GHz	Pin=5dBm, Put=5dBm, P_{DC}=100mW
Regenerative freq div 28 to 14 (13.8-15) GHz	Pin=5dBm, P_{DC}= 100mW

Device characteristics I-V D01PH

size: 2 · 50 μm





I_{dsmax}>700mA/mm g_{mmax}>700mS/mm

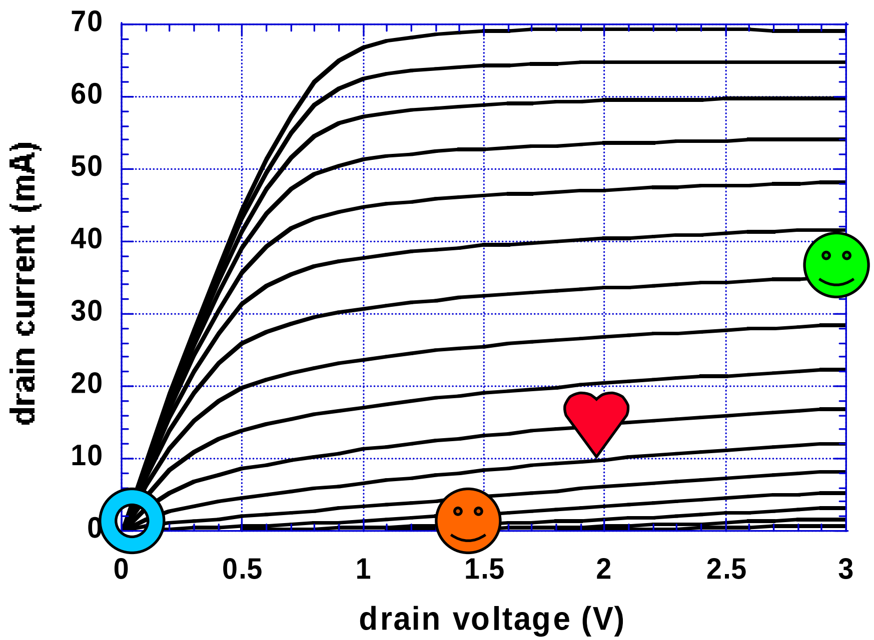
Typical bias points for different circuits:

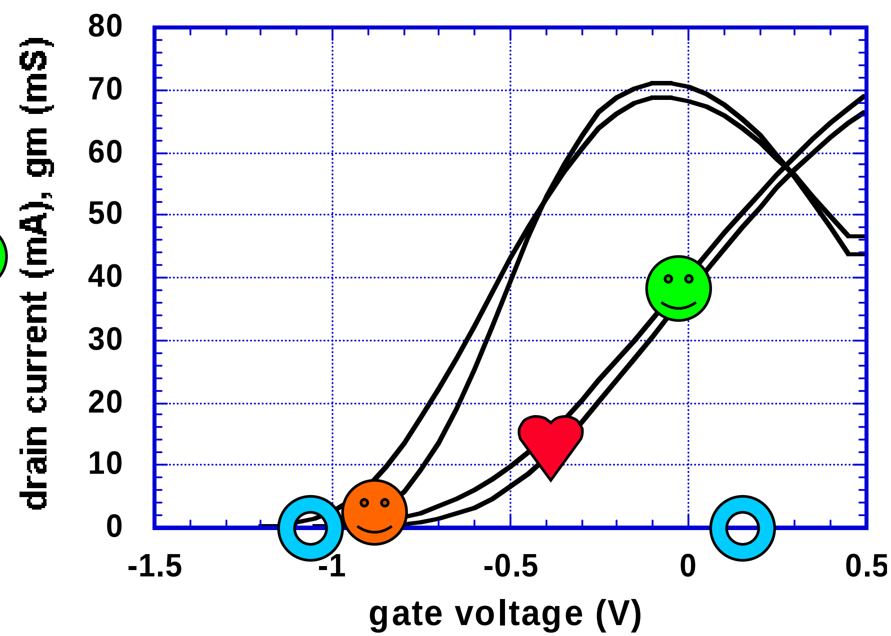
:Frequency multiplier

:Low noise amplifier

:Power amplifier

:switch, resistive mixer



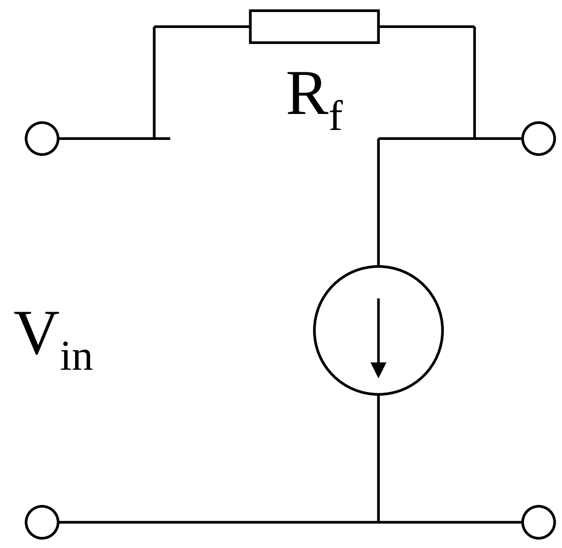


Amplifiers:
A Low Noise 2-20 GHz Feedback MMIC-Amplifier

1. Introduction

It is well known that resistive feedback can simultaneously give flat gain and good input and output match. The relation between transconductance g_m, feedback resistance R_f, and characteristic impedance Z_0 for the condition that S11=S22=0 is

$$R_f = g_m \cdot Z_0^2$$



The gain S_{21} of such an amplifier is then

$$S_{21} = \frac{Z_0 - R_f}{Z_0}$$

Ex: gm=100 mS
Z0=50->Rf=250
S21=-4

For a high gain, g_m should be high !

RFIC symposium, Boston 2000

Circuit diagram of the amplifier

Device width=200 μm

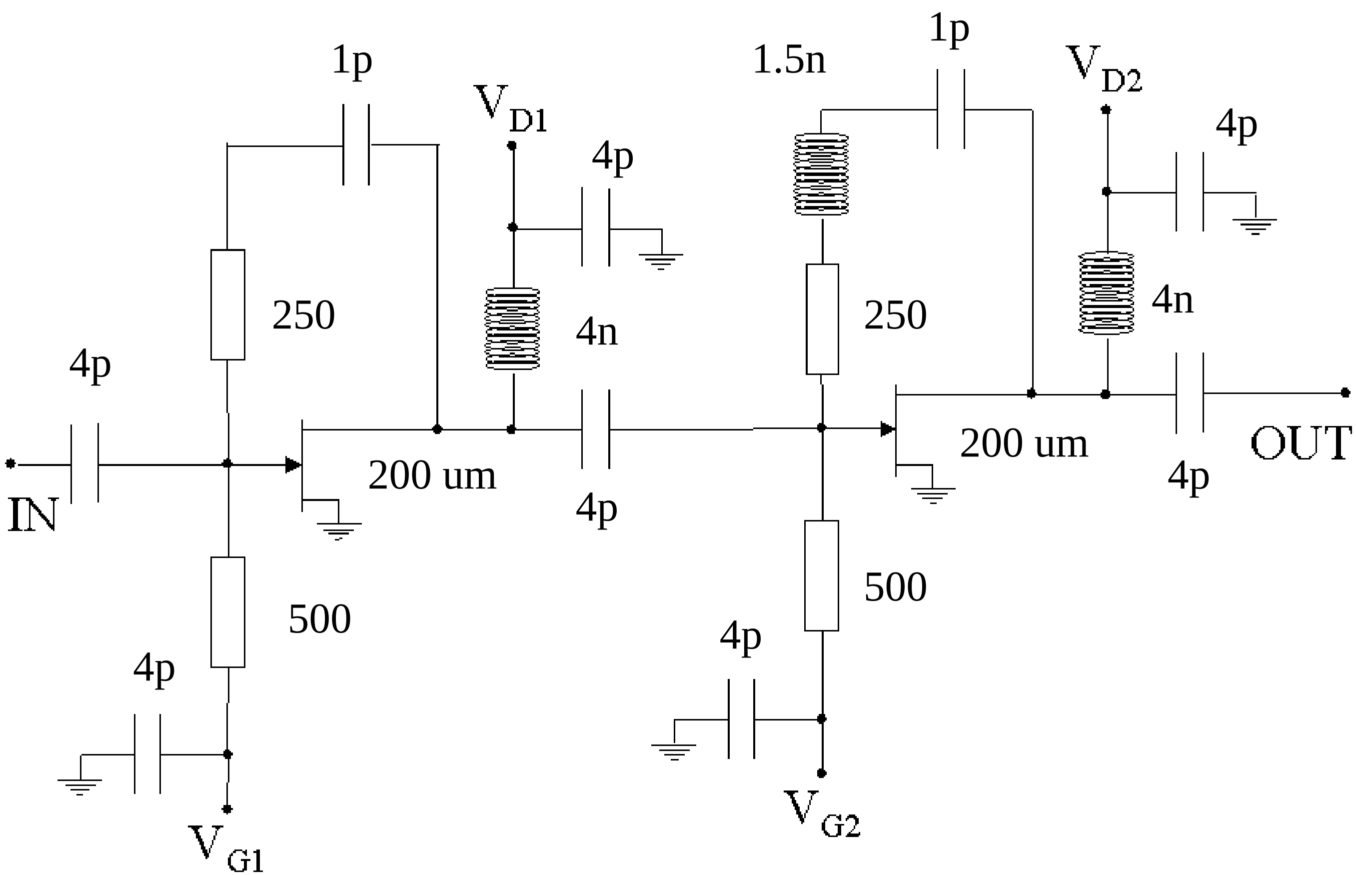
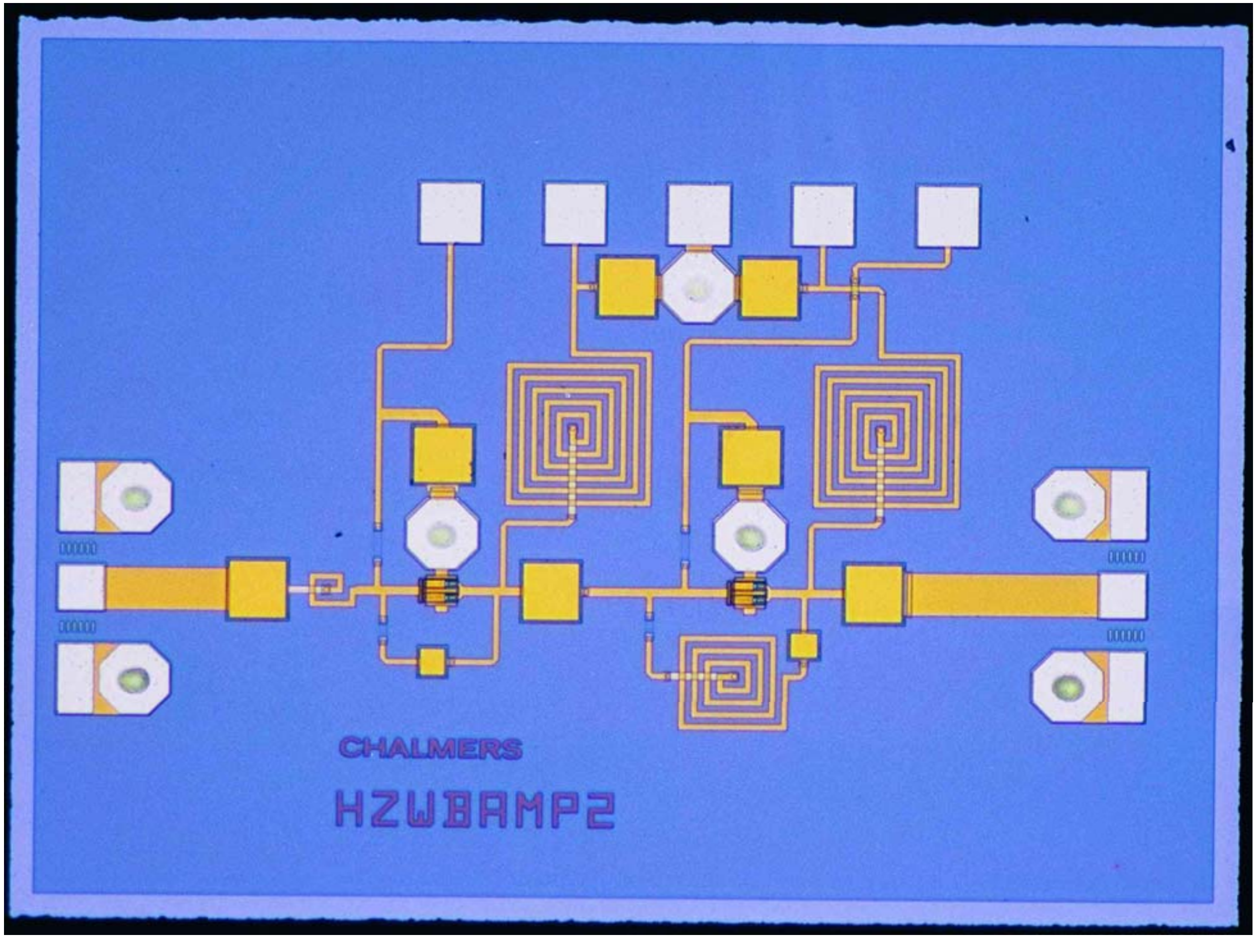
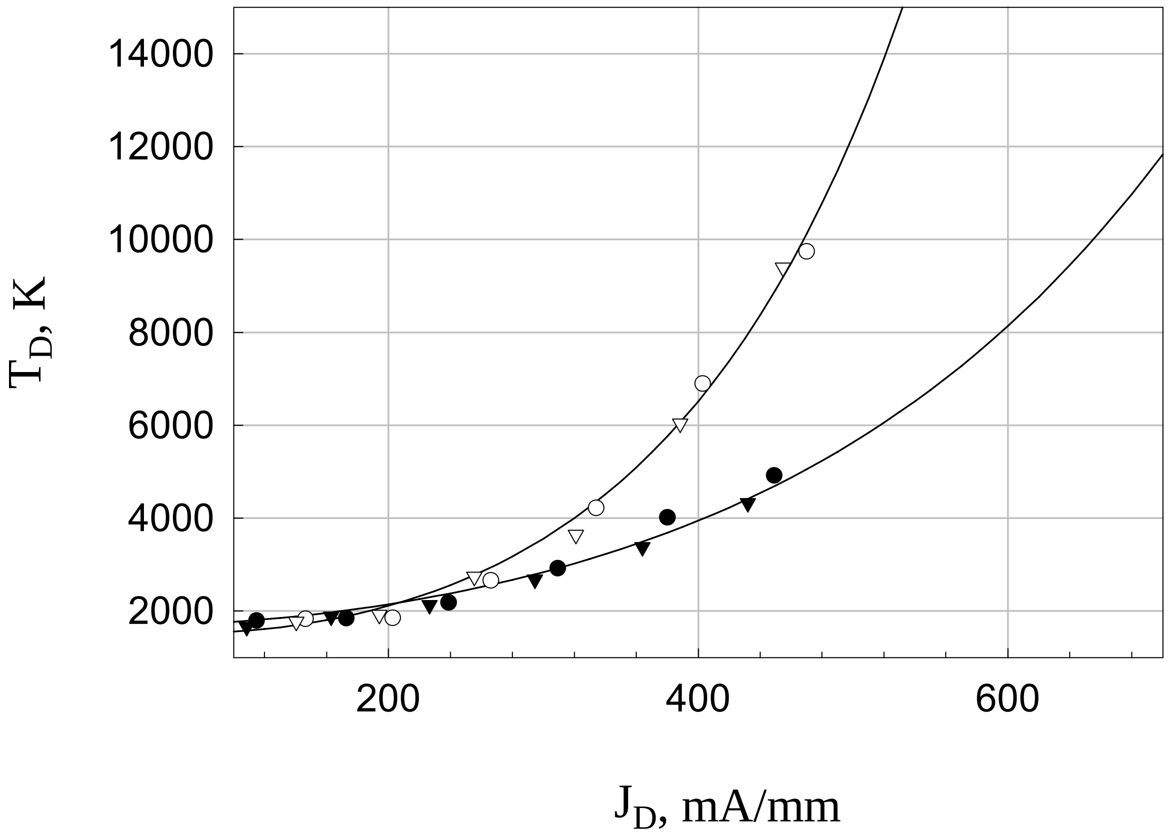


Photo of the feedback amplifier
chip size 2*1.5 mm, effective area 1mm^2



The noise parameters of different HEMT devices were measured and the results were fitted to a 2-temperature noise model which was used in the simulation of the amplifier

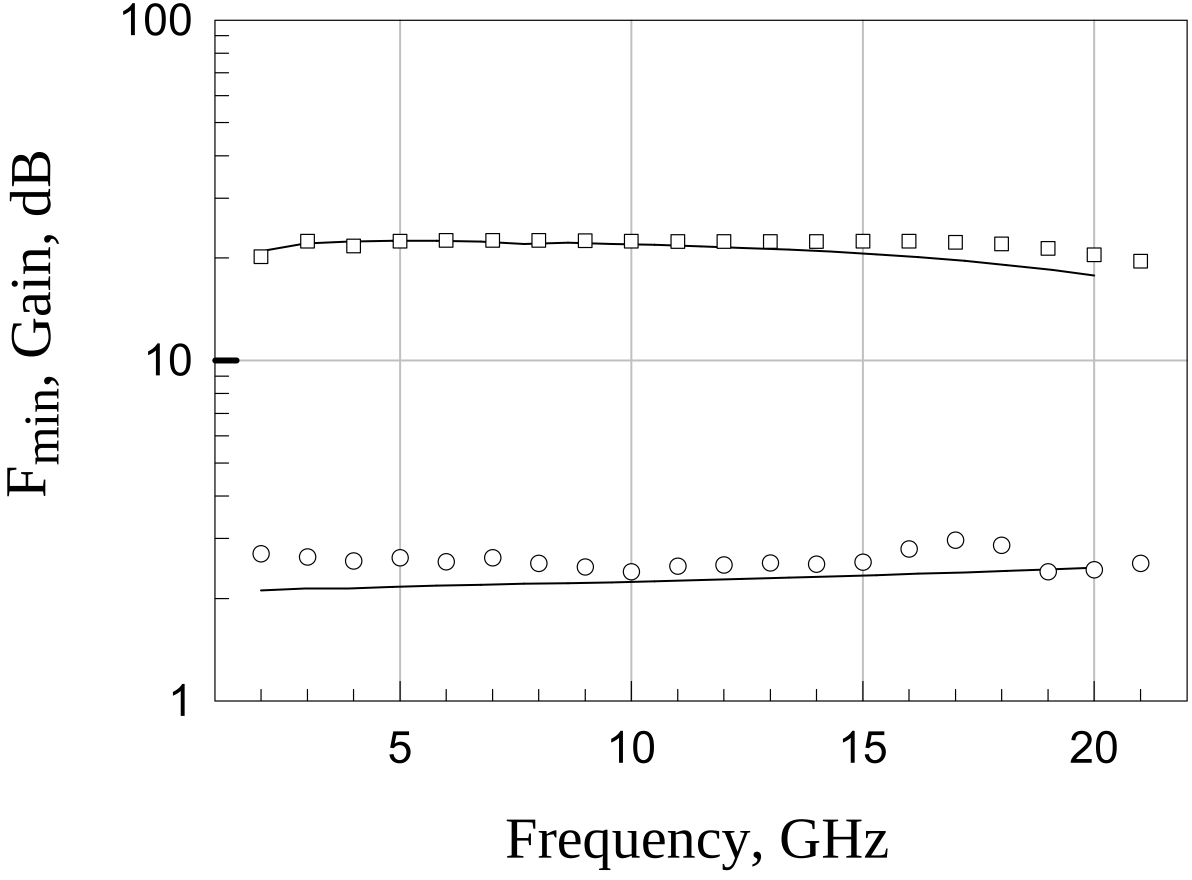


Data was fitted to

$$T_D = T_{D0} \cosh \frac{J_D - J_0}{J_1}$$

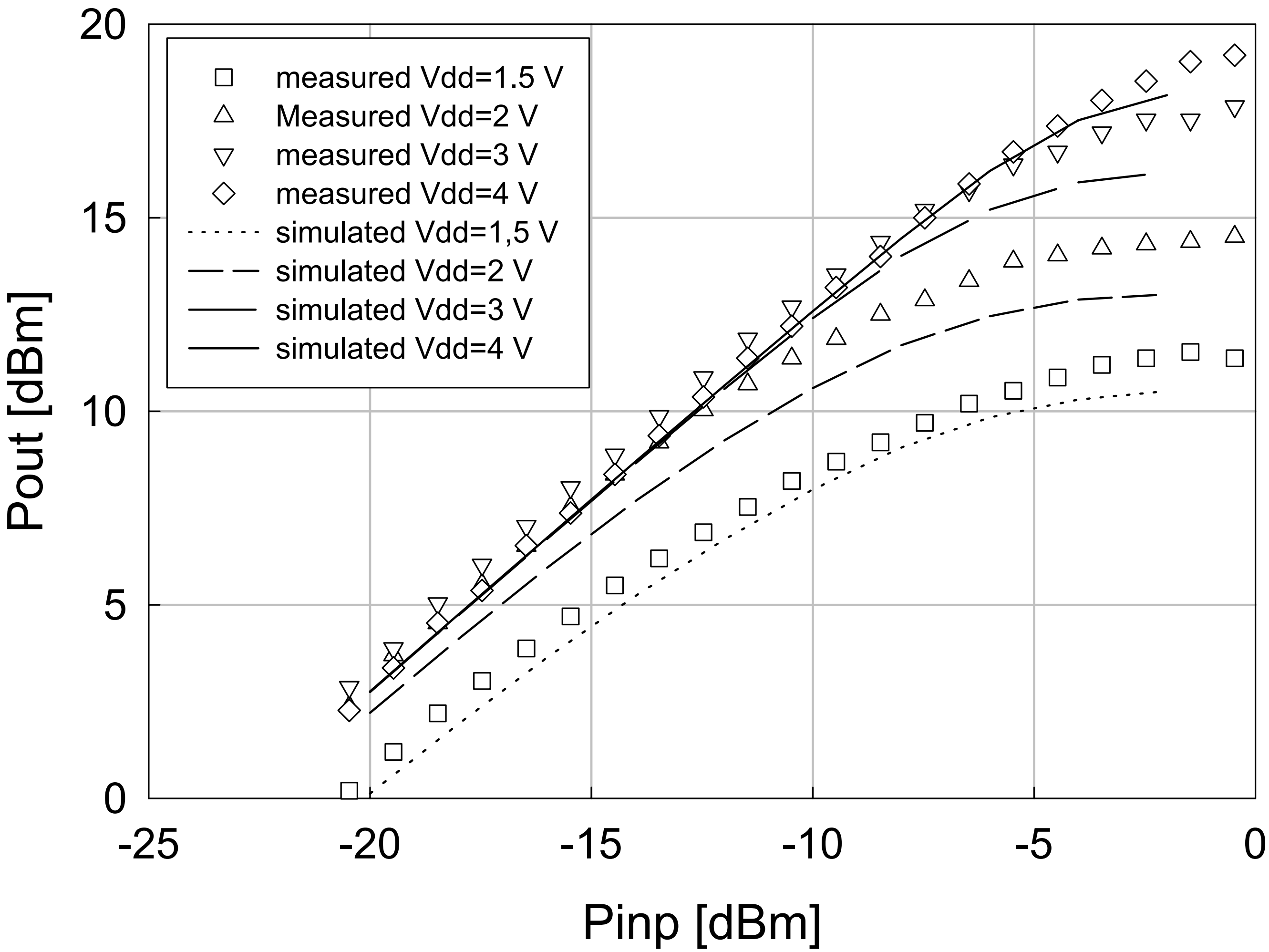
Open symbols Vd=2V
solid symbols Vd=1V
circles= 100 μm
triangles=200 μm

Measured gain and noise figure of the amplifier

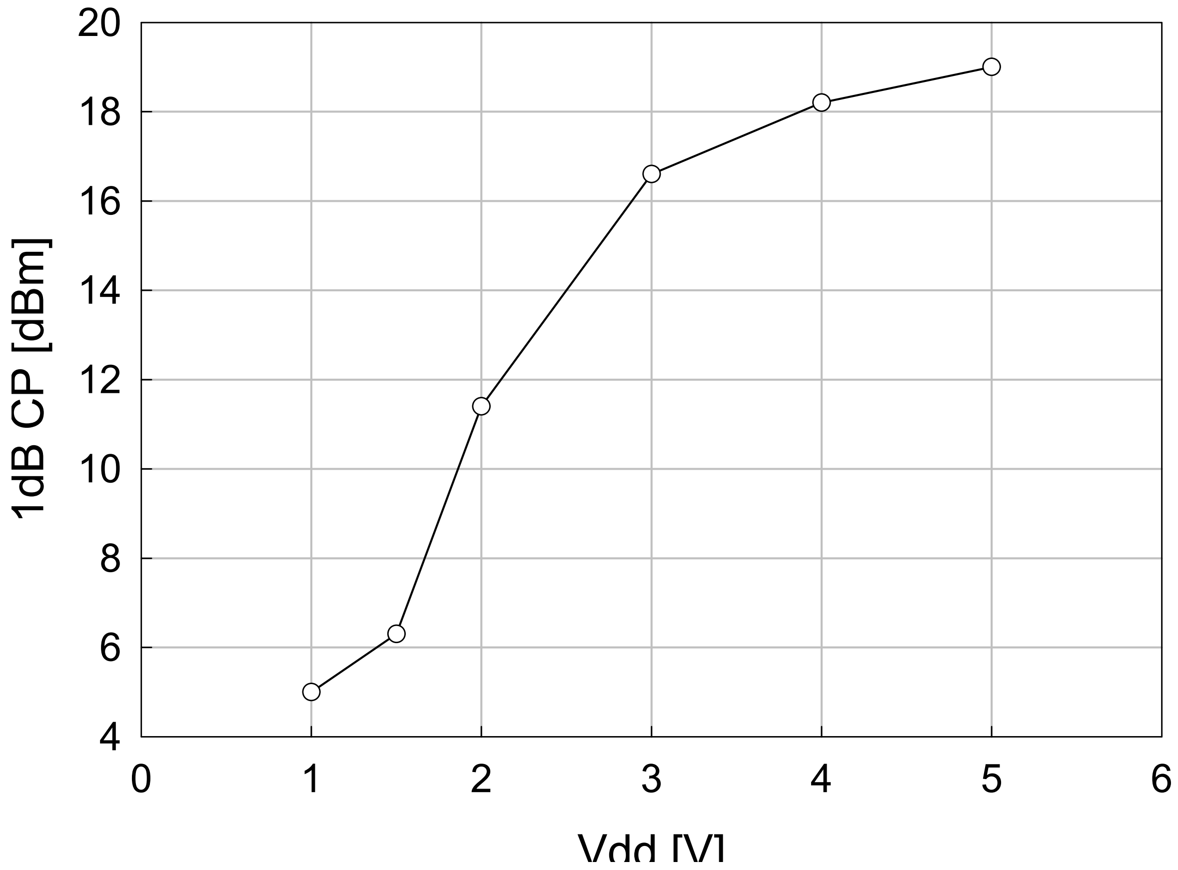


Bias:
Vd1=Vd2=1.5V
Vg1=Vg2=0V

Output power versus input power at 10 GHz versus drain bias



1 dB compression point versus drain bias at 10 GHz



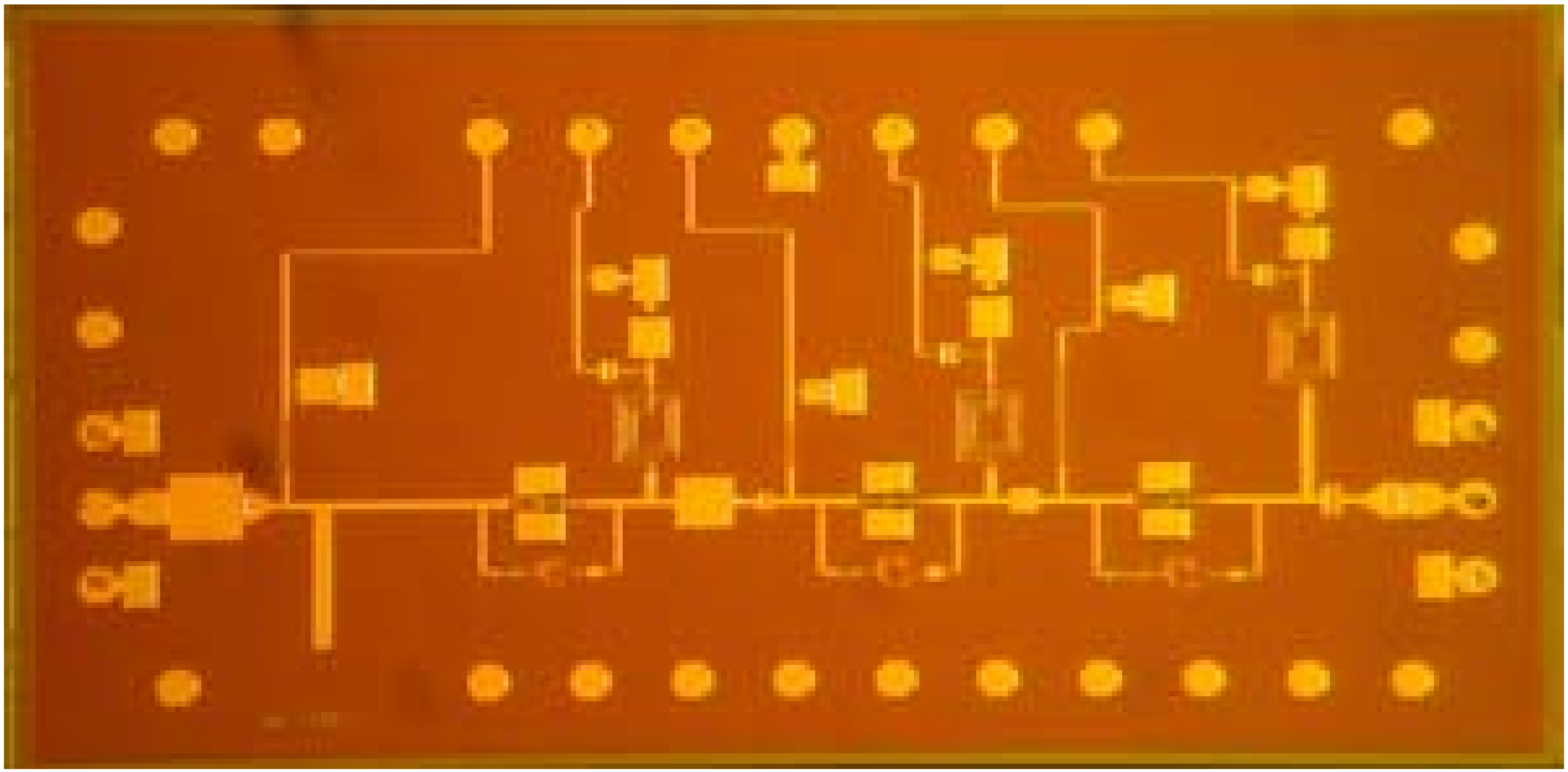
Conclusions

A 2-20 GHz PHEMT feedback amplifier was designed, analyzed (noise, S-parameters, output power), fabricated and characterized

The amplifier show excellent results:

-Noise figure below 3dB
-Gain of 11dB per stage i e 22 dB
-Output power of 100 mW (max)
-effective circuit area only 1mm^2
-DC-power consumption 125mW (70-180 mW)
-Resistive Feedback in addition stabilizes the transistor

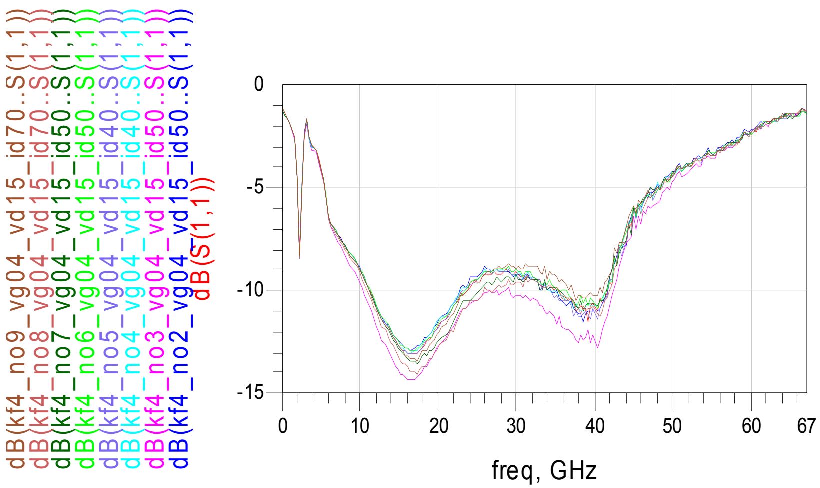
3-stage wideband amplifier with resistive feedback WIN mhemt MP-15 process

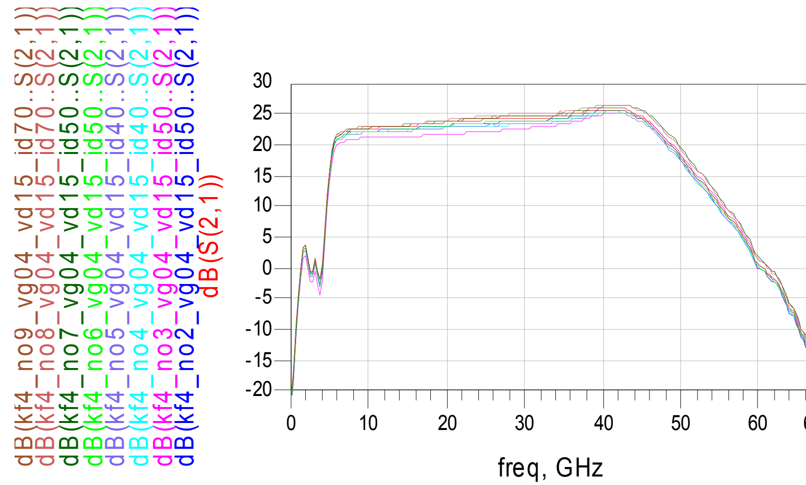


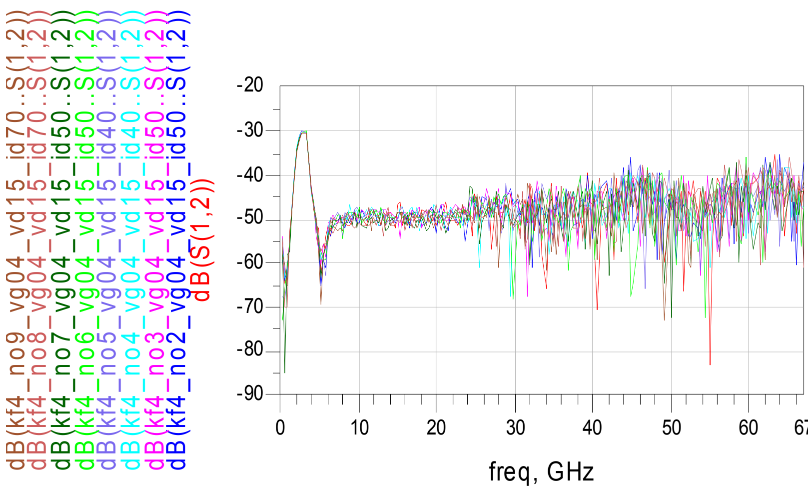
⇨ Gain >20 dB (5.7 to 48 GHz)

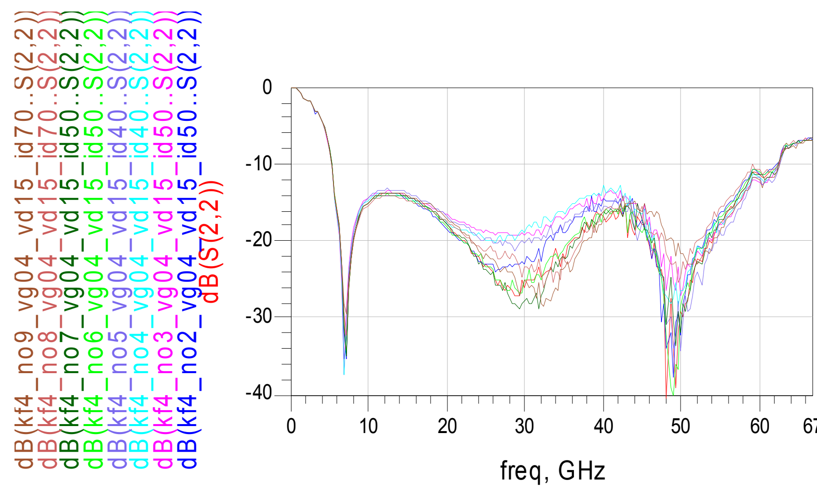
⇨ S11 < -5 dB and S22 < -10 dB

⇨ Measurement on 9 MMICs

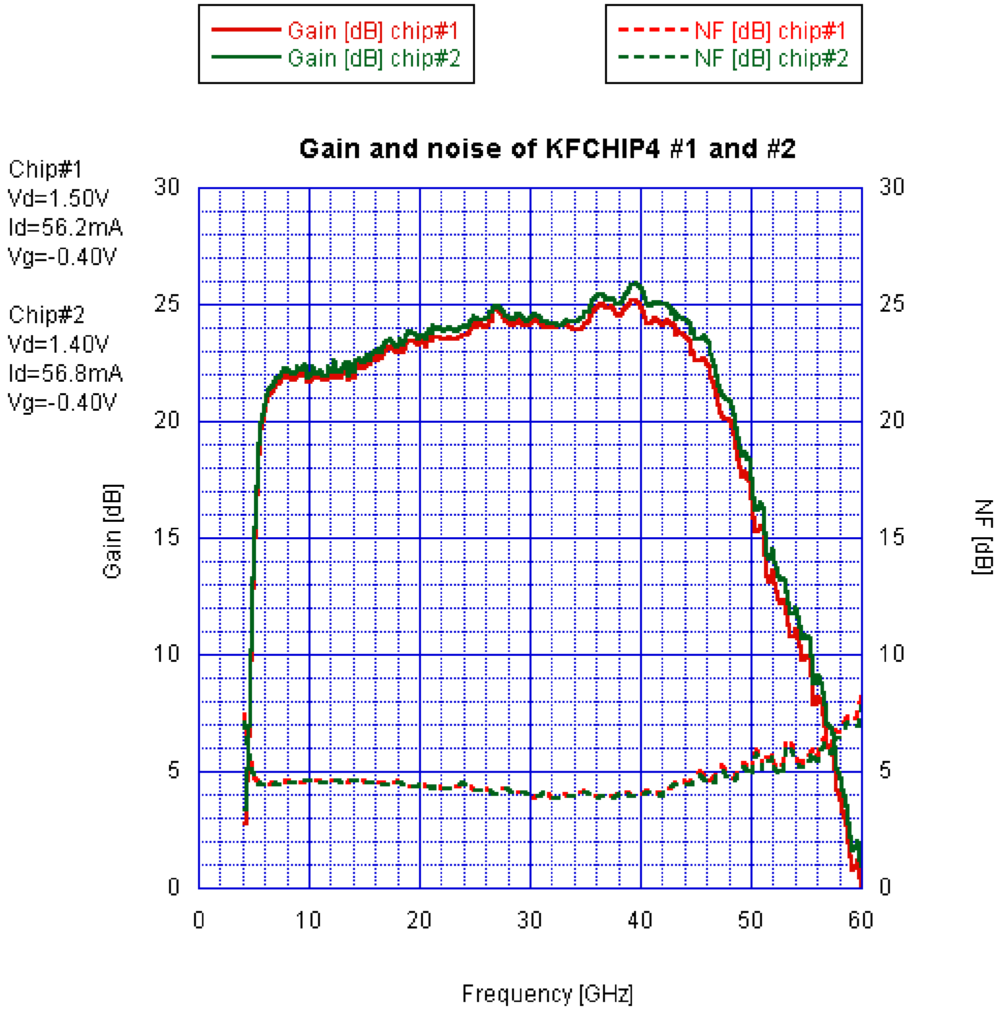








Noise figure



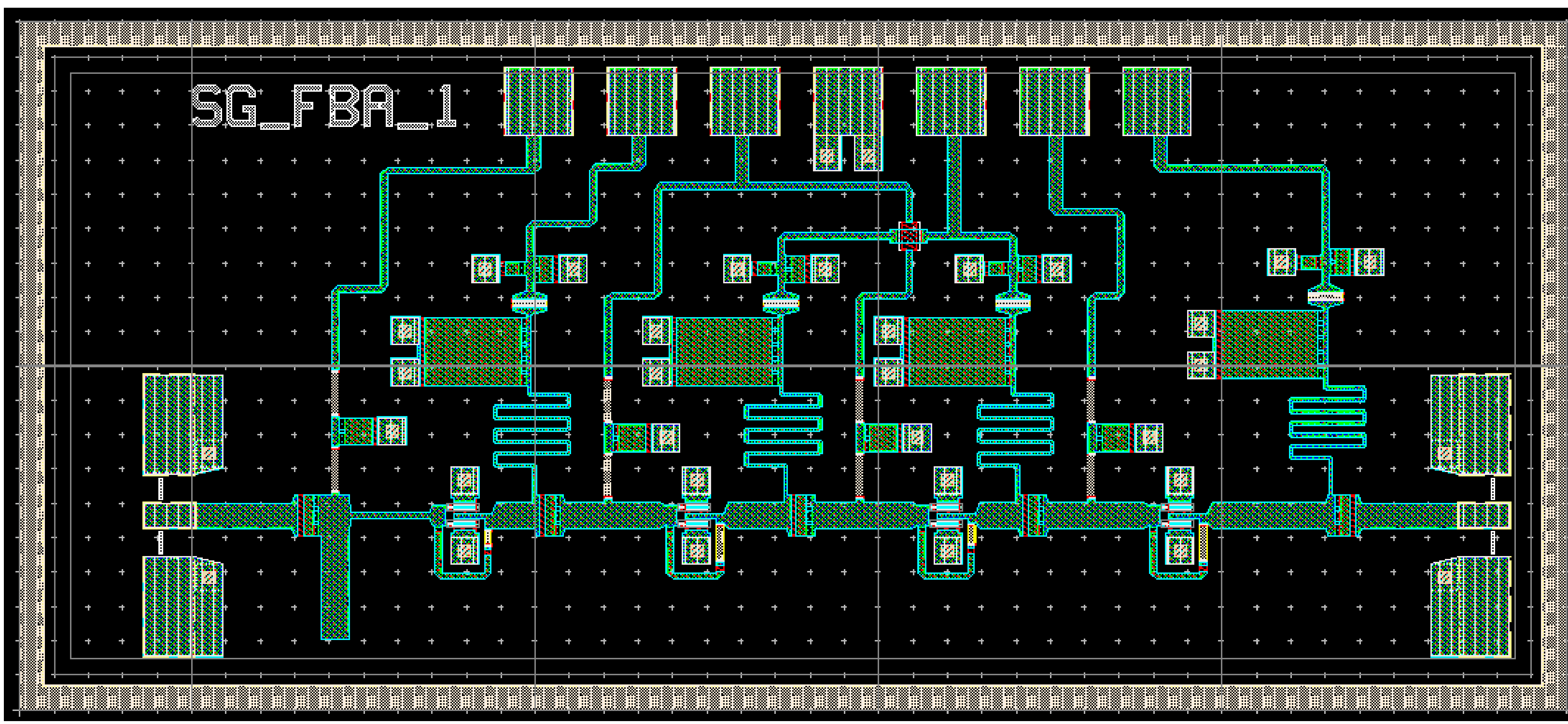
NF_{min}= 4 dB

$NF_{@48GHz}$= 5 dB

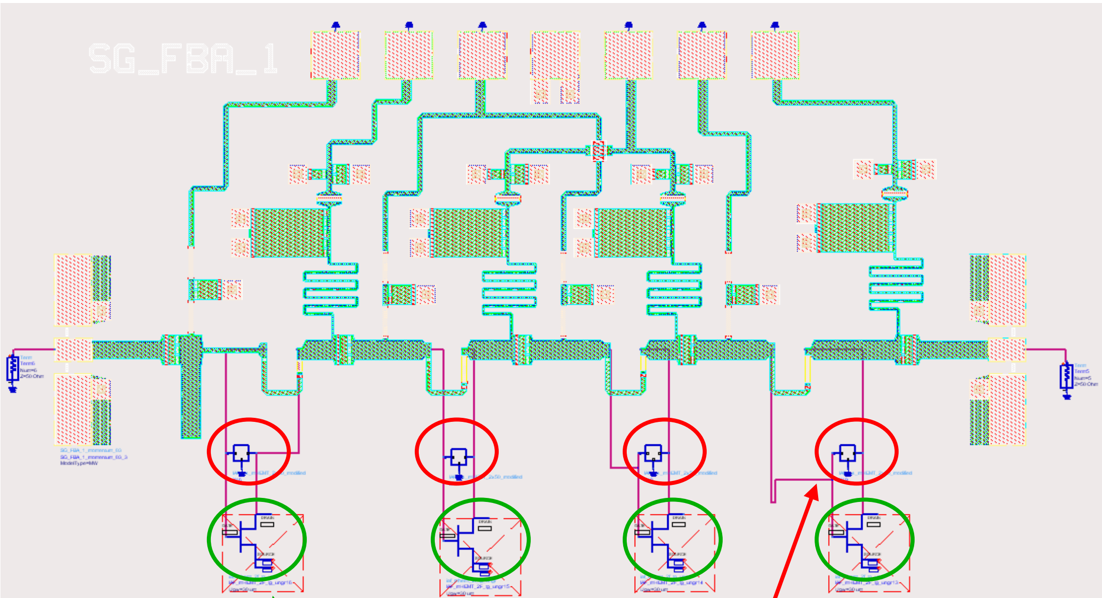
SG_FBA_1

- Feedback amplifier, 4 stage, 2×30µm (IAF device layout) , 2.0 × 0.9 mm^2

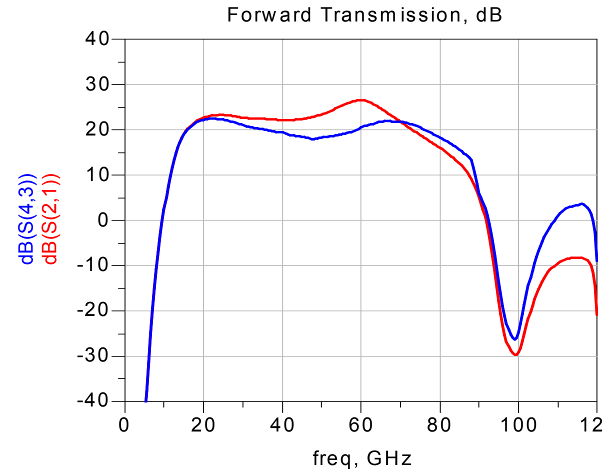
Process: IAF mhemt 100nm gatelength



Simulation results

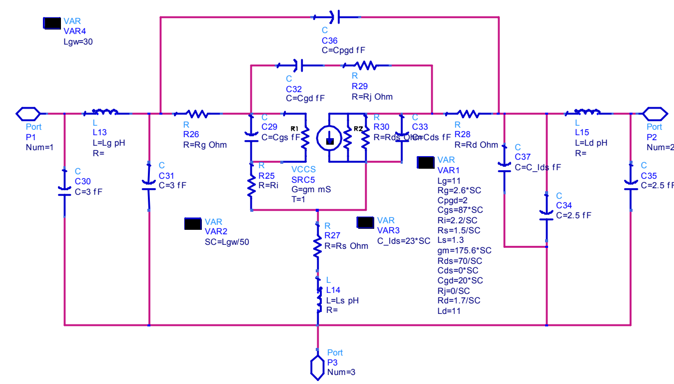


Blue = IAF meas. Red = CTH SS-model



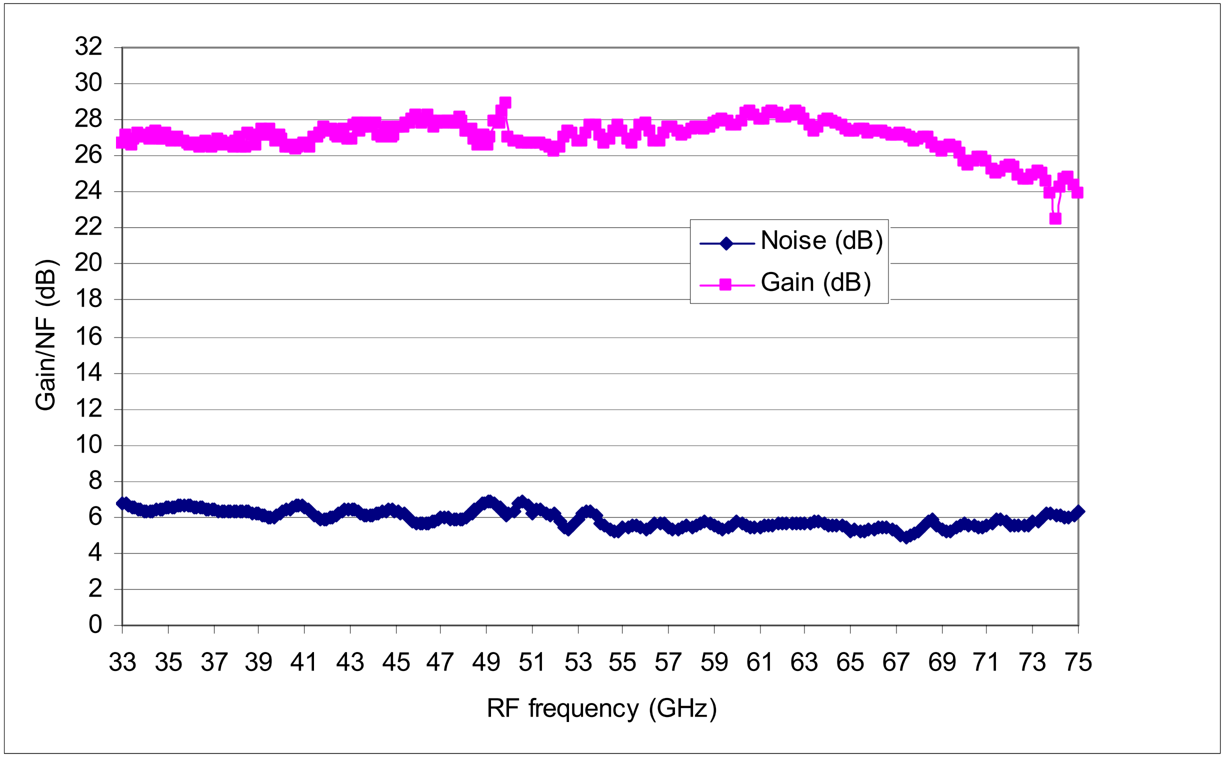
Gain
(blue = IAF meas.,
red = CTH SS-model)

- Full EM simulation of the FBA in Momentum
- Data from IAF measurements and CTH SS-model used in simualtions



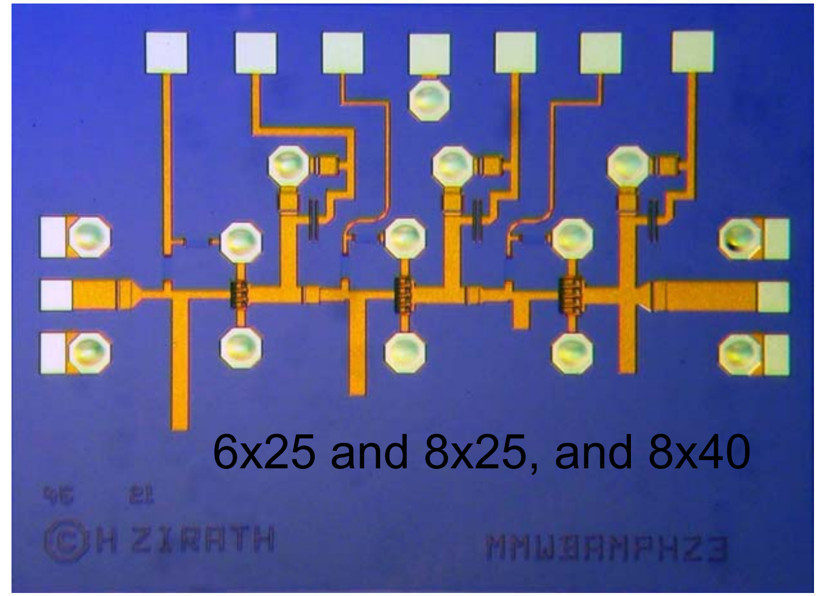
CTH SS-model

Noise measurements with gain

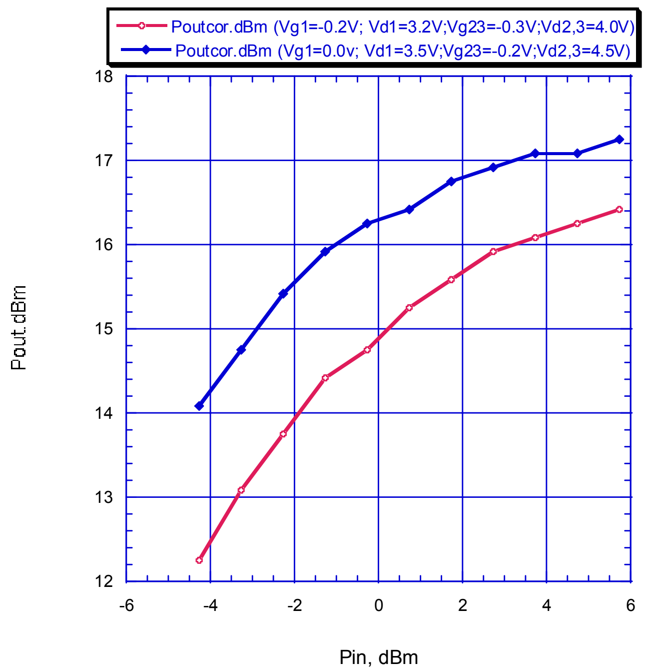


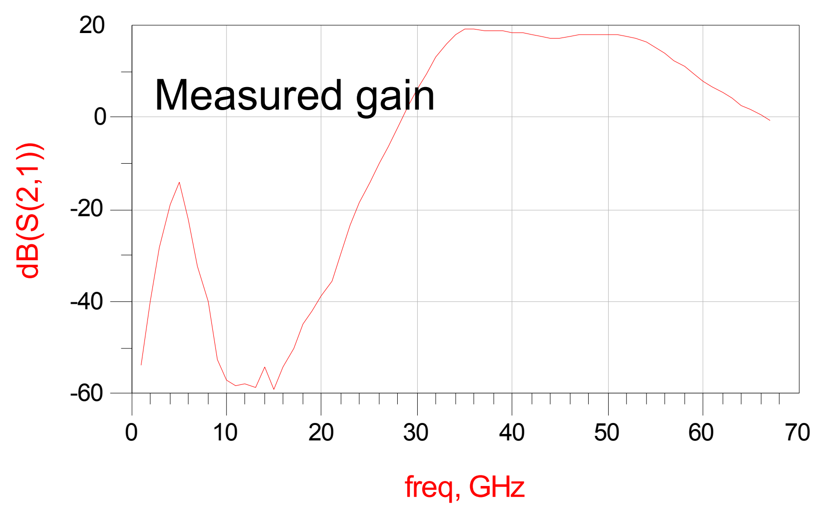
Q-band (33-50) GHz medium power amplifiers, optimized interstage matching topology for increased bandwidth

- 3-dB bandwidth typ 50%
- 20dB Gain
- Output power >50 mW
- 3 dB noise figure
- Shorted stubs in drain bias line <λ/4



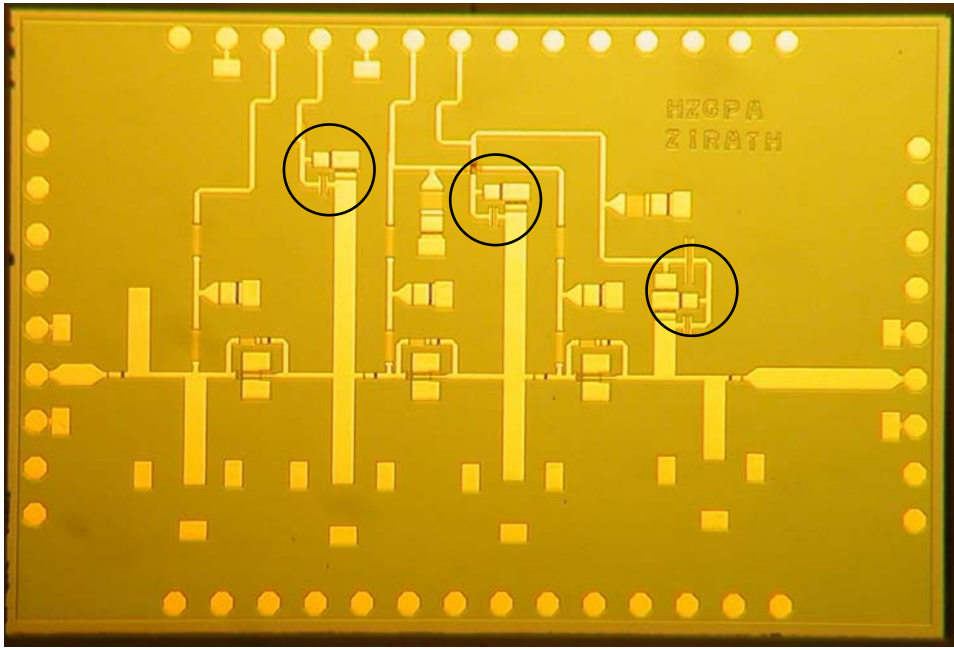
Output power



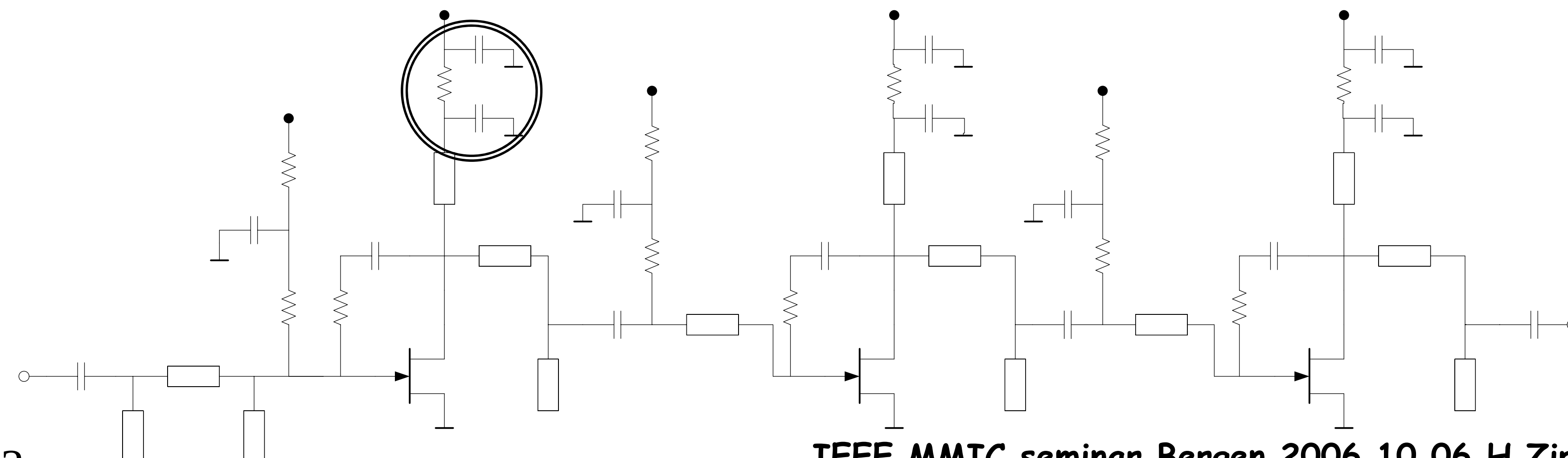


Wideband amplifier in WIN PP-15 process

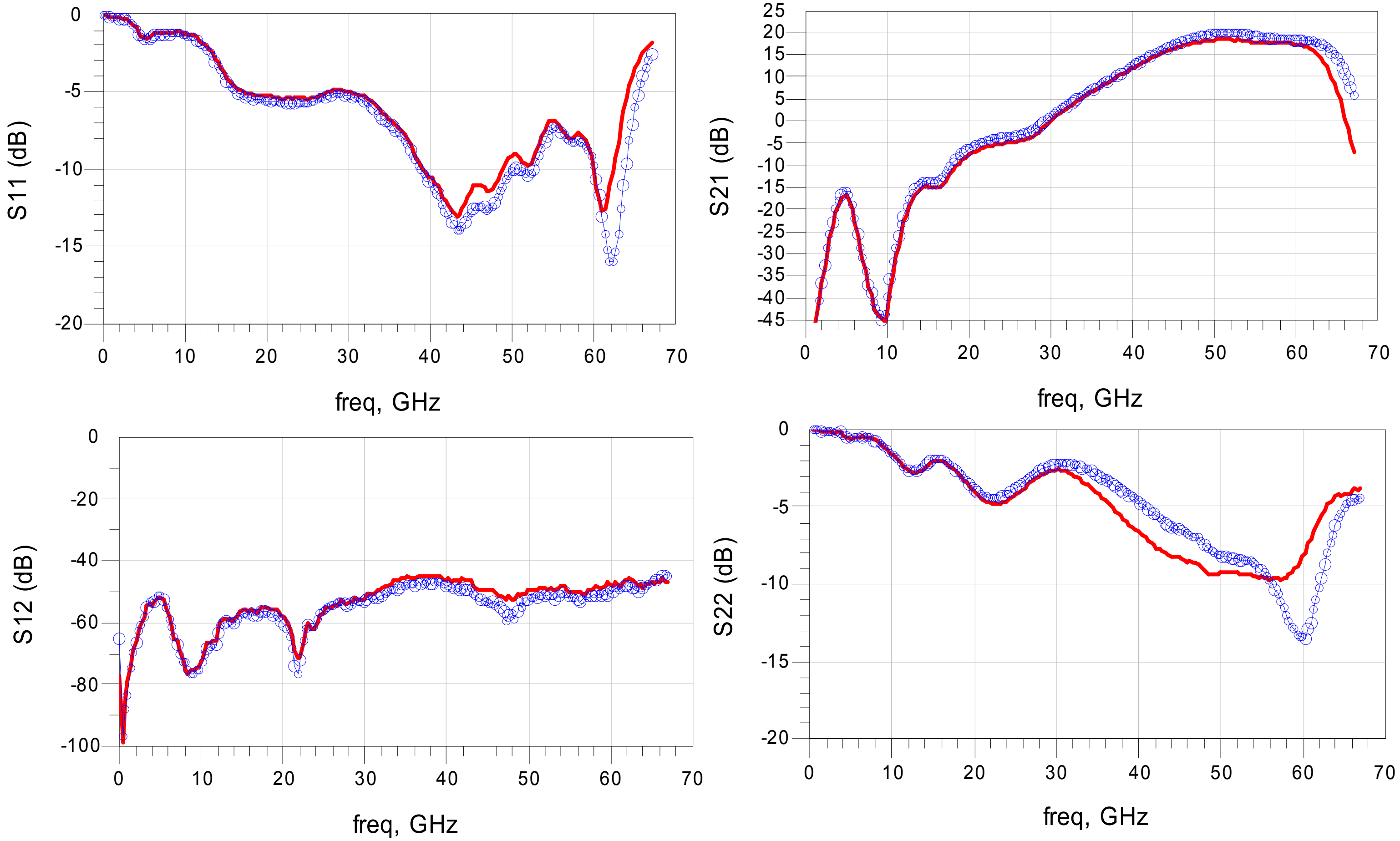
Each amplifier stage has a gate-drain parallel feedback stabilization network consisting of an RC network with R=166 Ω and C=210 fF. Each transistor has two gate fingers with a unit width of 50 μm. The drain DC supply resistance is 10 Ω. The simulated small signal gain ($S21$) is 17 dB ±1 dB, between 45 and 70 GHz, for VD=3 V and VG=-0,2 V. Simulated noise figure is 4,9 dB.



3x2 mm

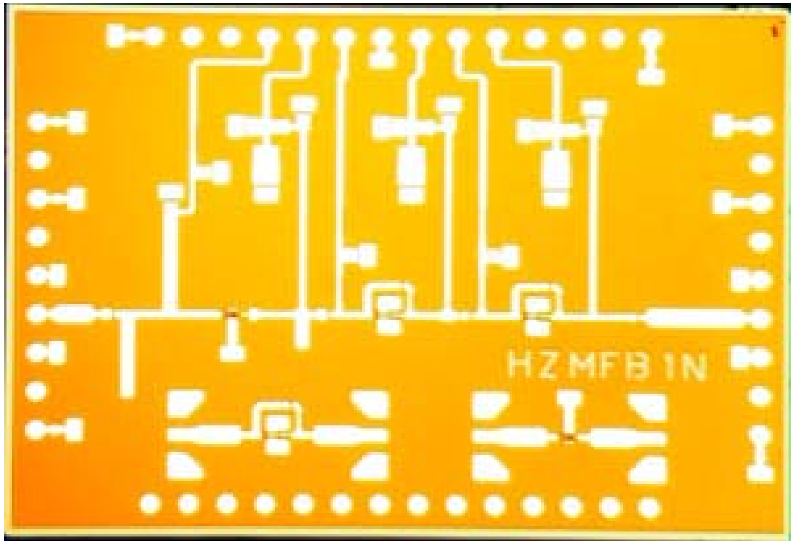


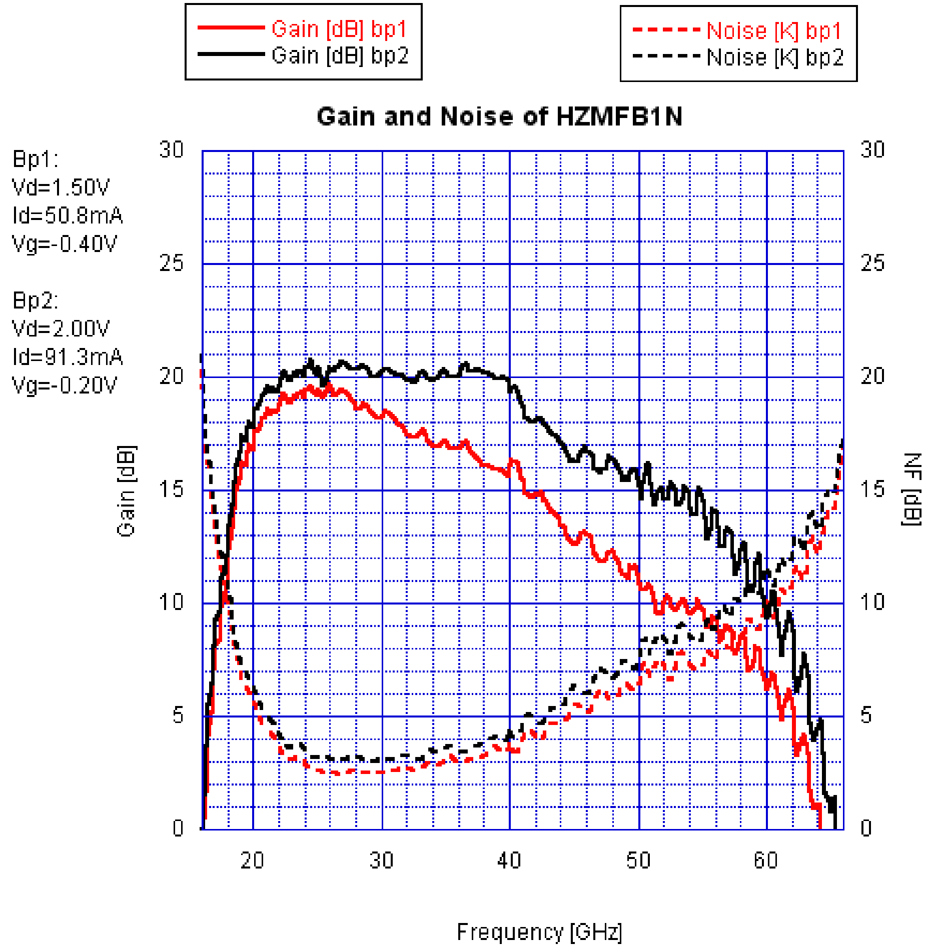
Measured results, S-parameters
Red curve is with extra passivation (BCB)



HZMFB1N

1st stage reflection match
stage 2-3 resistive FB

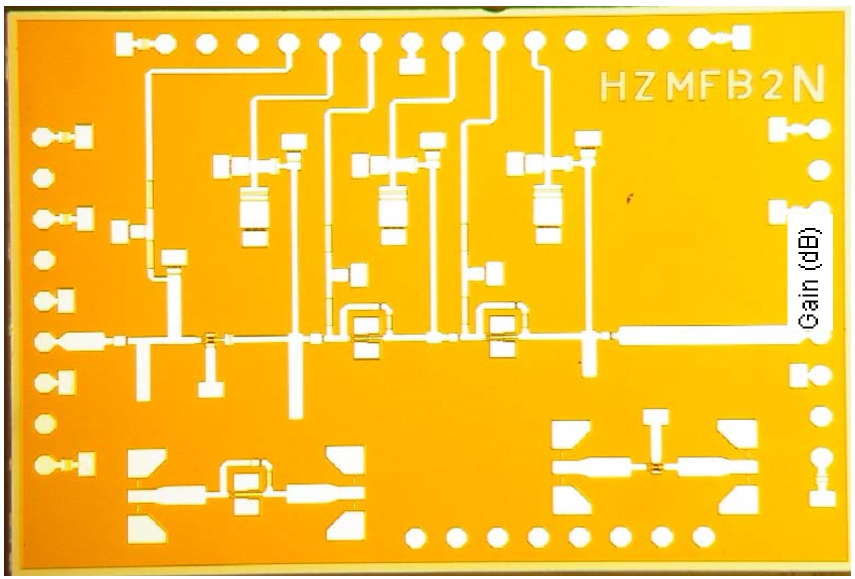




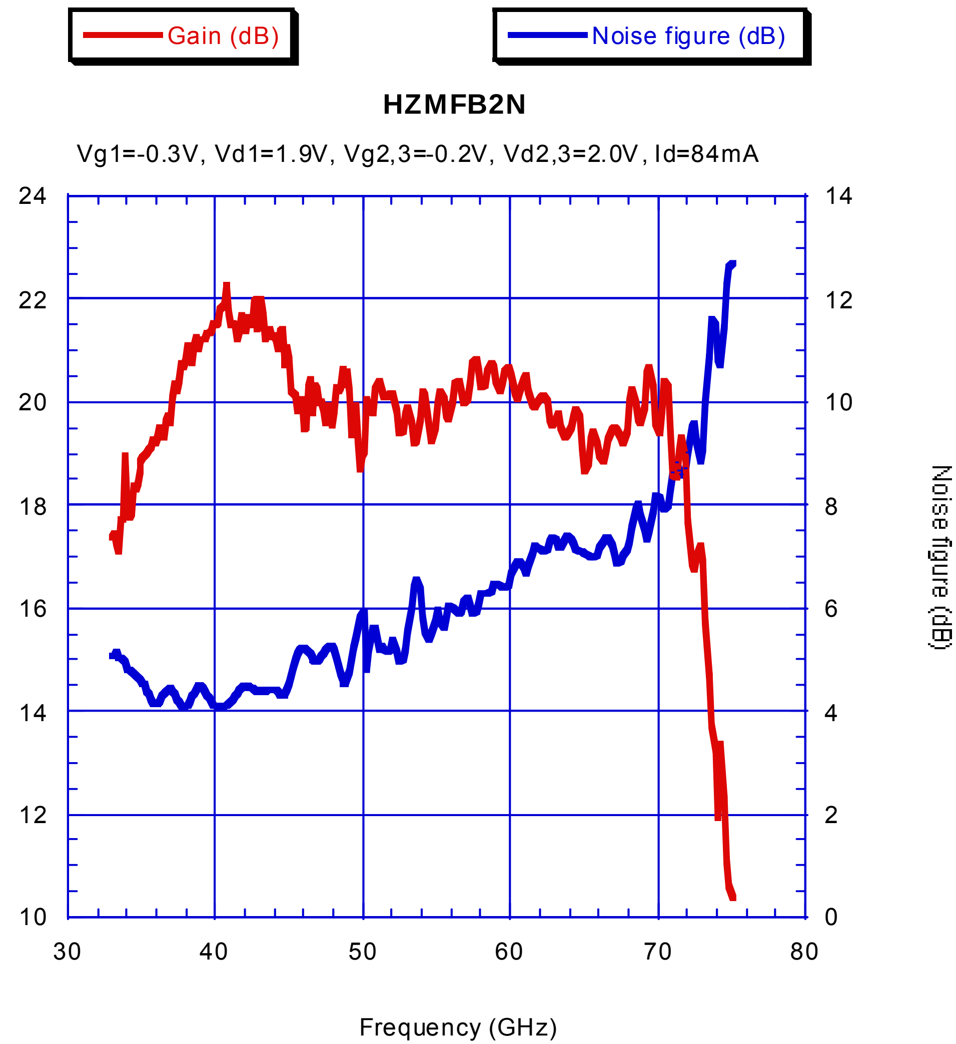
NF_{minBp2}= 3 dB

HZMFB2N

1st stage reflection match
stage 2-3 resistive FB



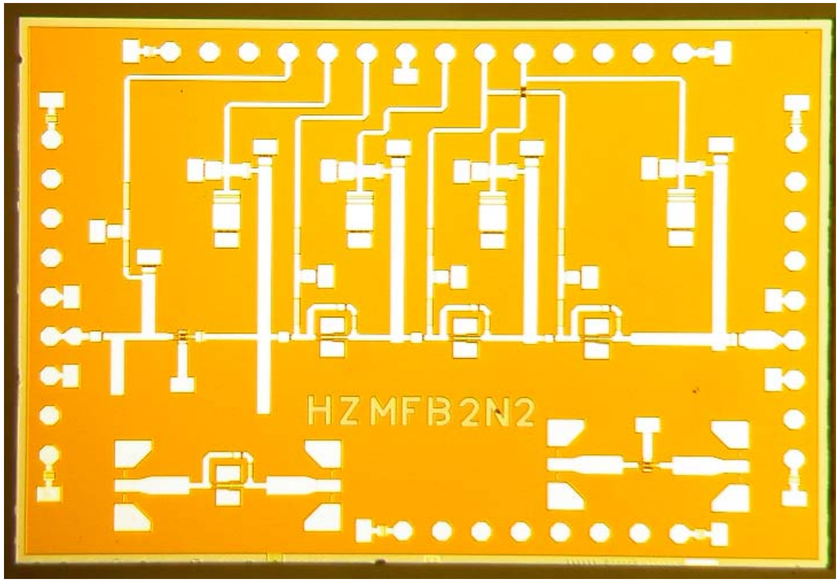
NF_{min}= 4.5 dB

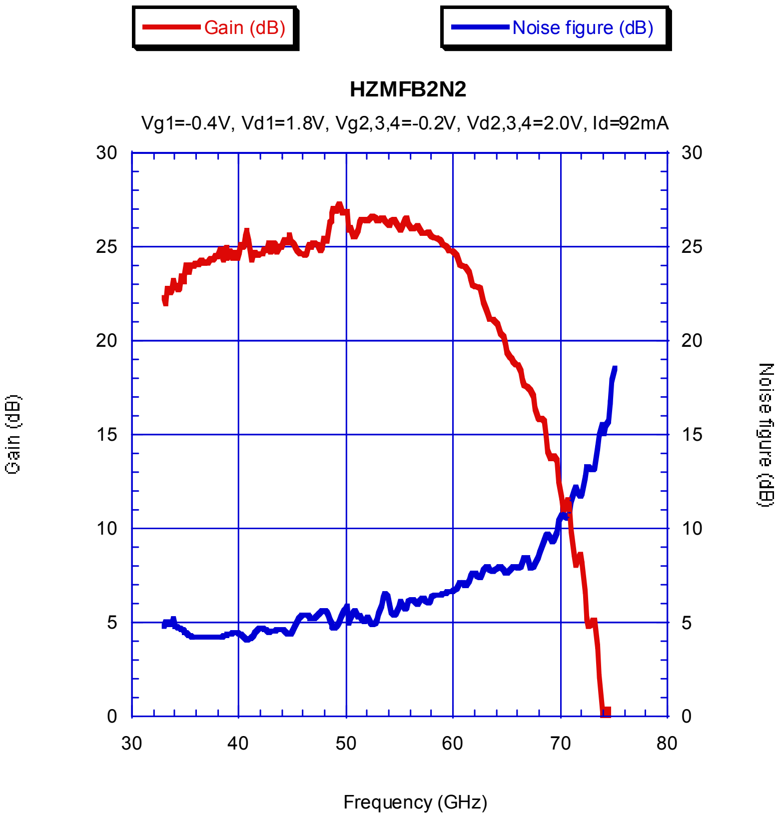


HZMFB2N2

1st stage reflection match

2-4 stage resistive FB



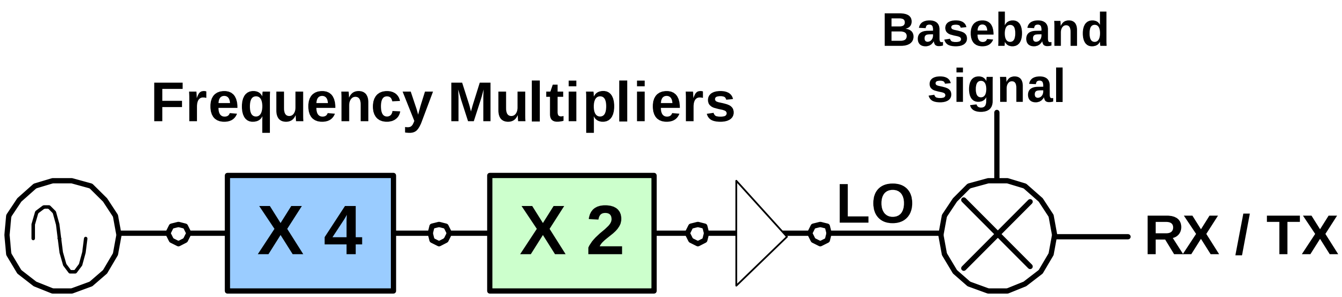


$NF_{min} = 4$ dB

Frequency multipliers

Motivation

- Low-cost LO-chain for 60-GHz WLAN

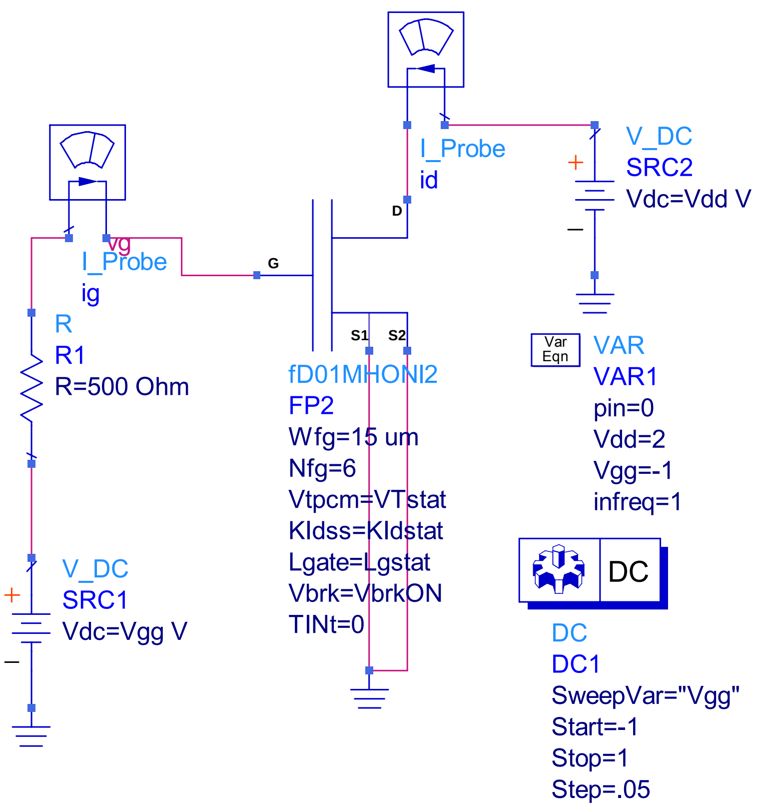


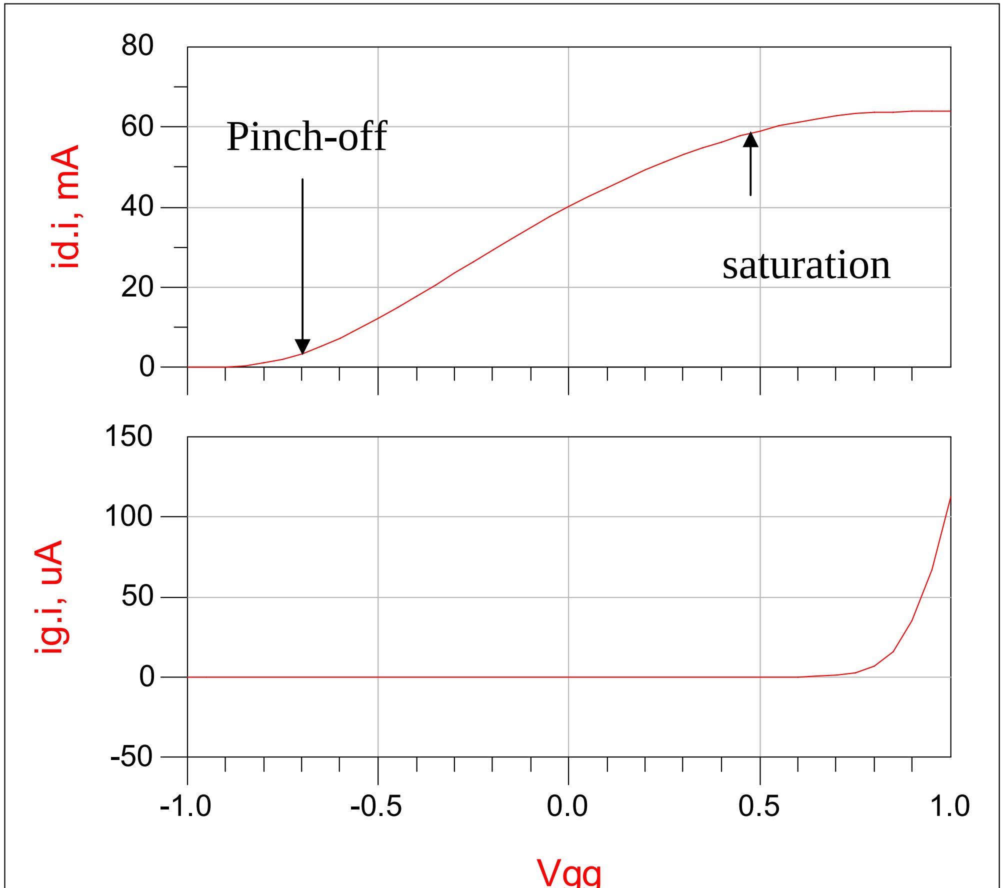
- High conversion efficiency
  - ⇨ Doubler + Doubler
- Wideband operation, Small chip area
  - ⇨ Active input matching circuit + Quadrupler
- Low power consumption
  - ⇨ Single-ended Doubler with Buffer Amplifier

How can we get a frequency multiplication ?

We investigate an MHEMT, Lw=90 um

DC-characteristic id versus vg at Vdd=2V

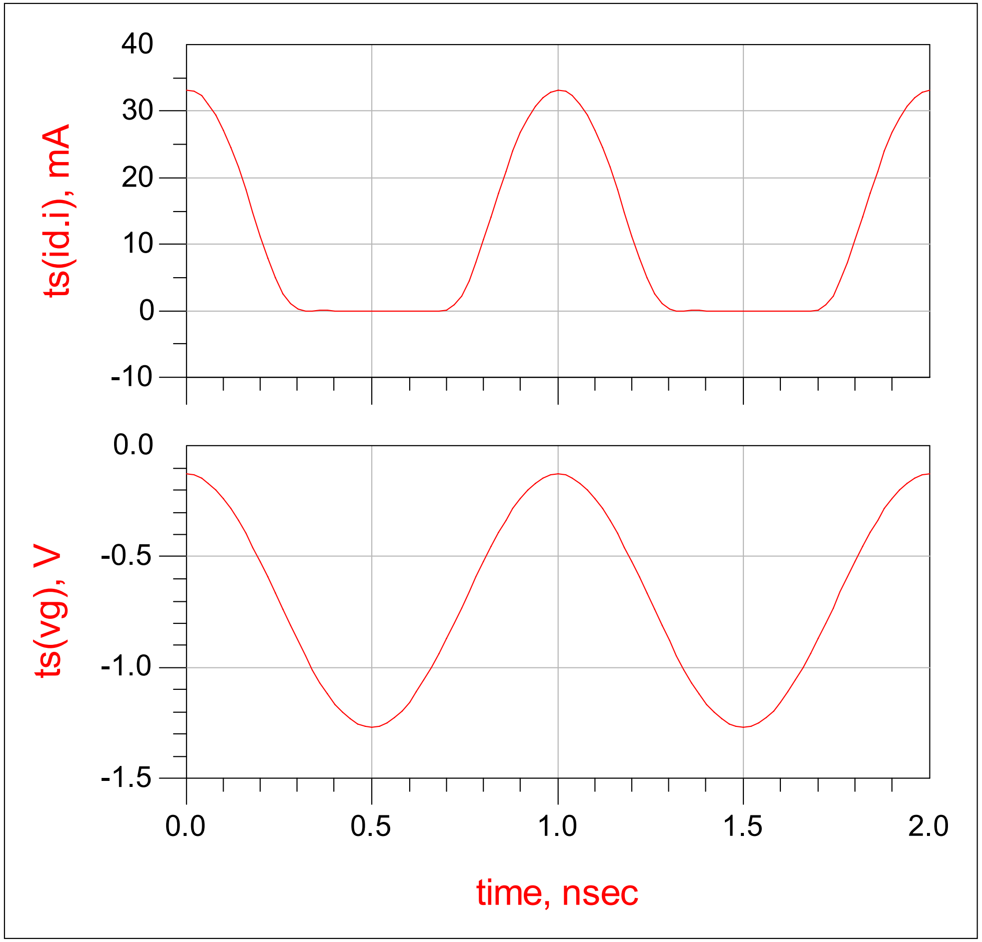


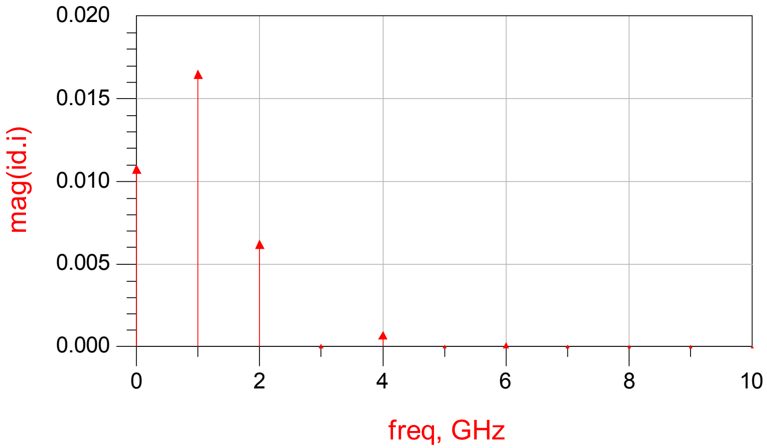


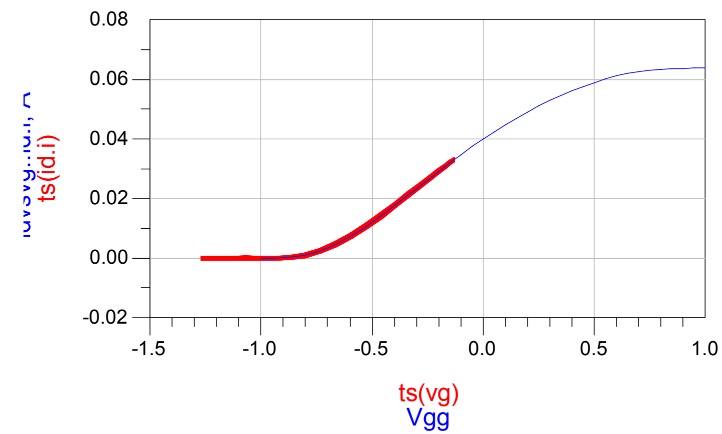
Bias for *even harmonics*, close to pinchoff –0.7 V

Pin=0dBm, substantial 2nd harmonic !

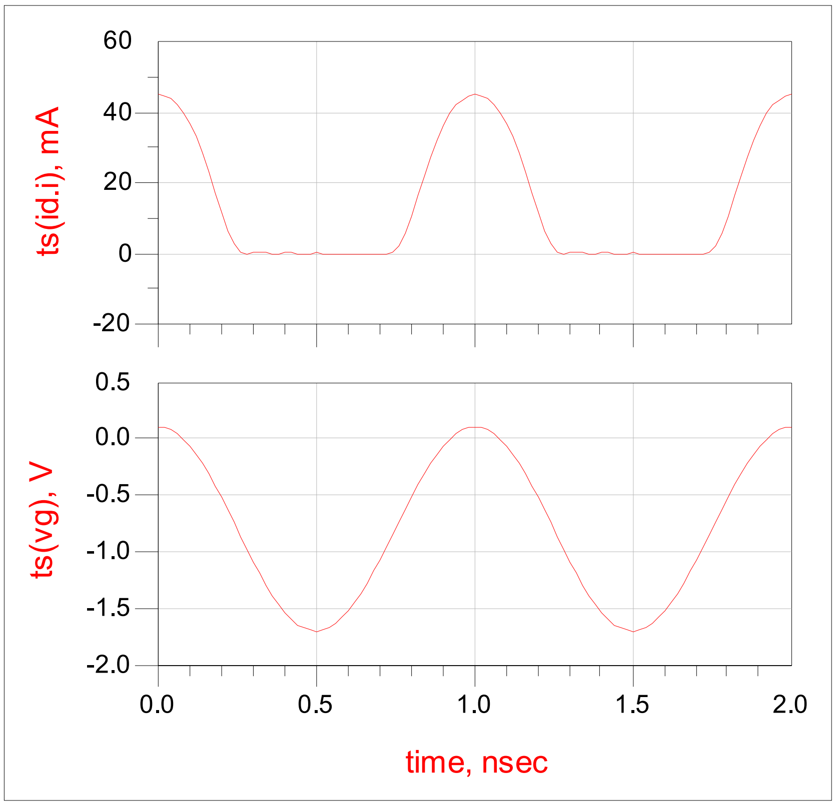
’Sine-pulse’

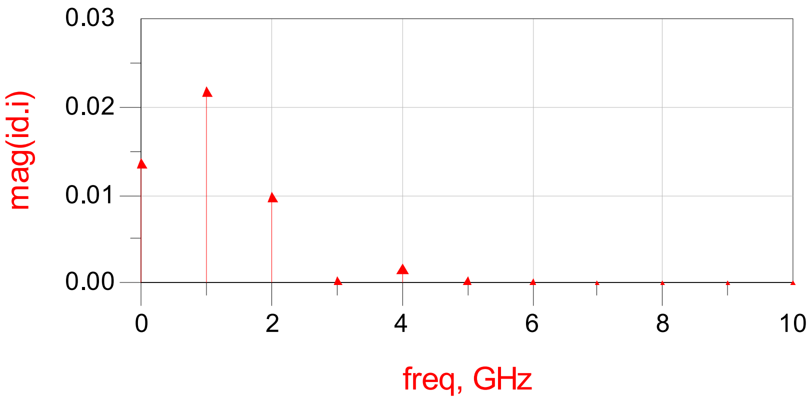


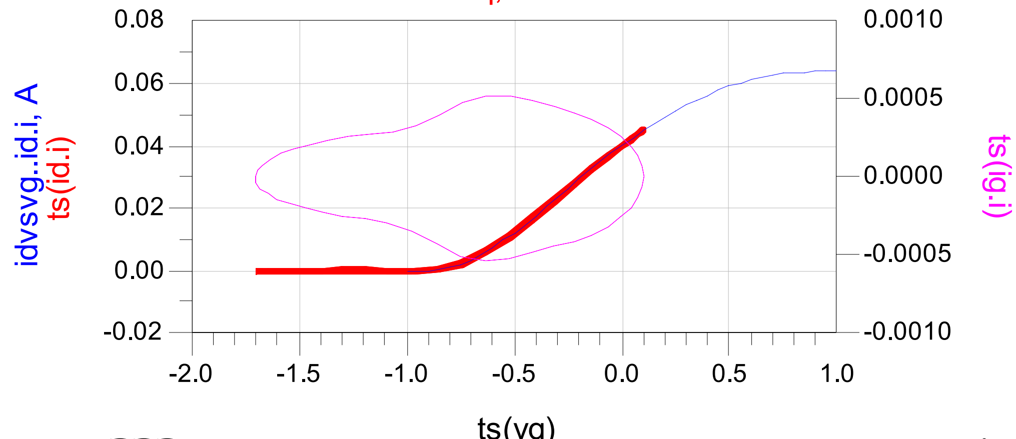




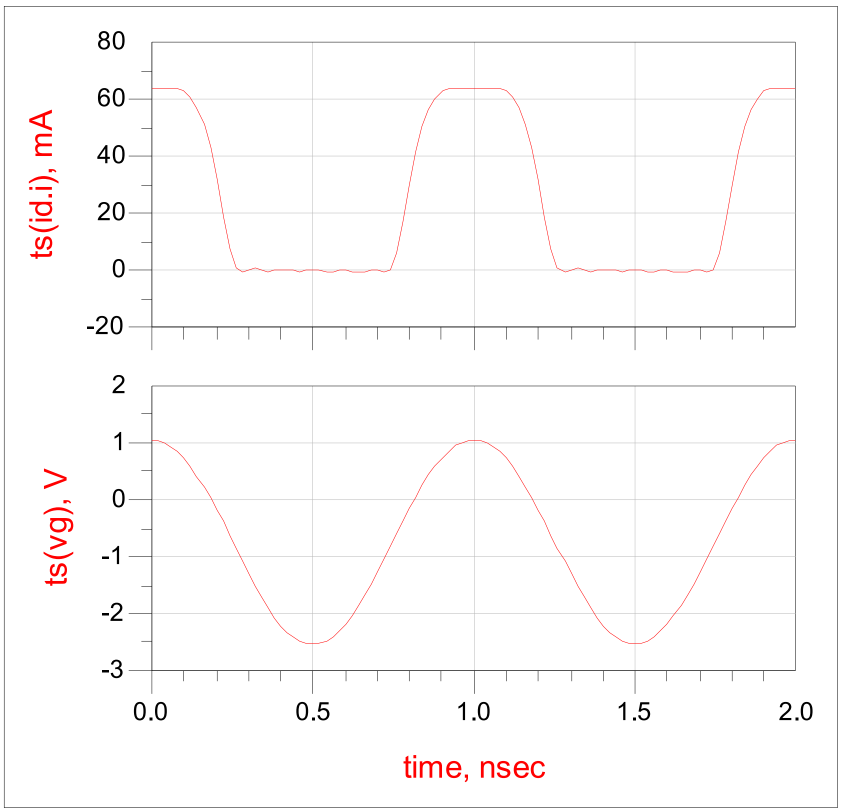
Bias for *even harmonics*, close to pinchoff –0.8 V
Pin=4 dBm
’Half-sine’ waveform

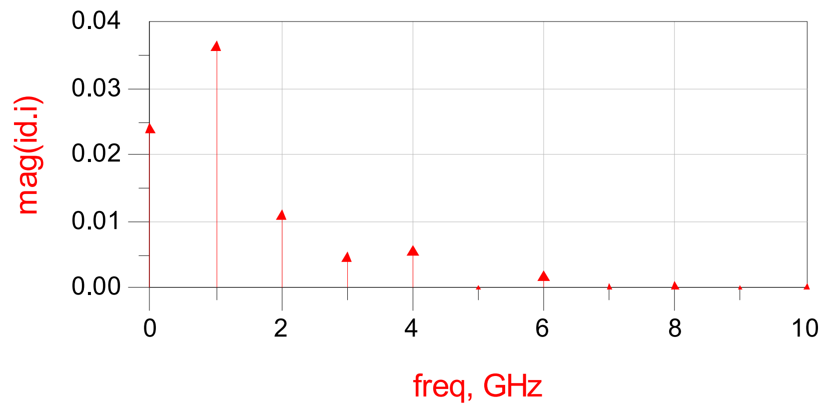


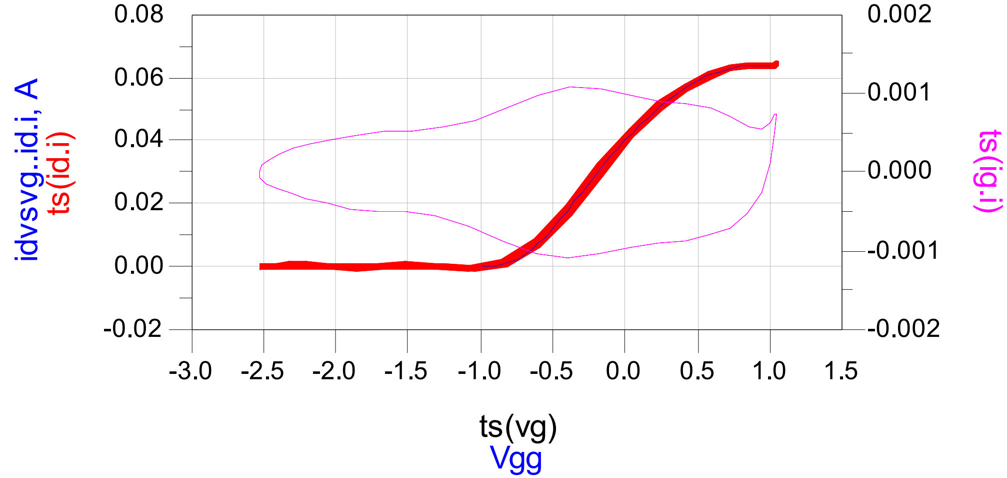




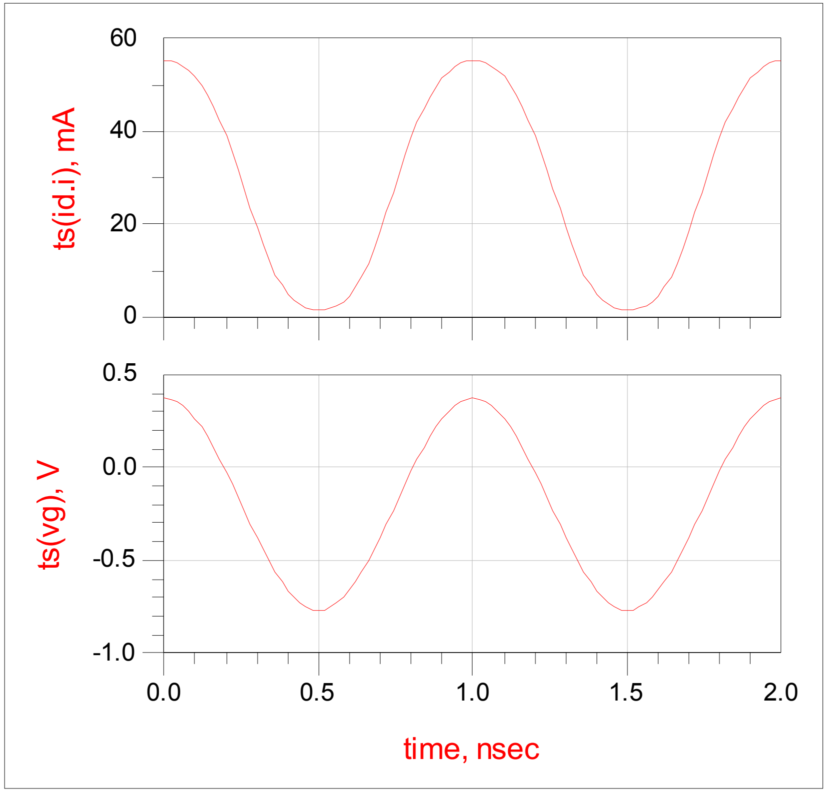
Bias for *even harmonics*, close to pinchoff –0.7 V
Pin=10 dBm, onset of gate conduction current
Rectangular waveform !

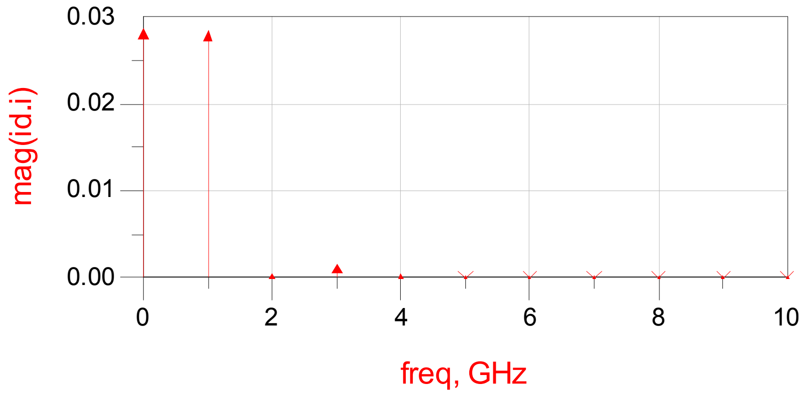


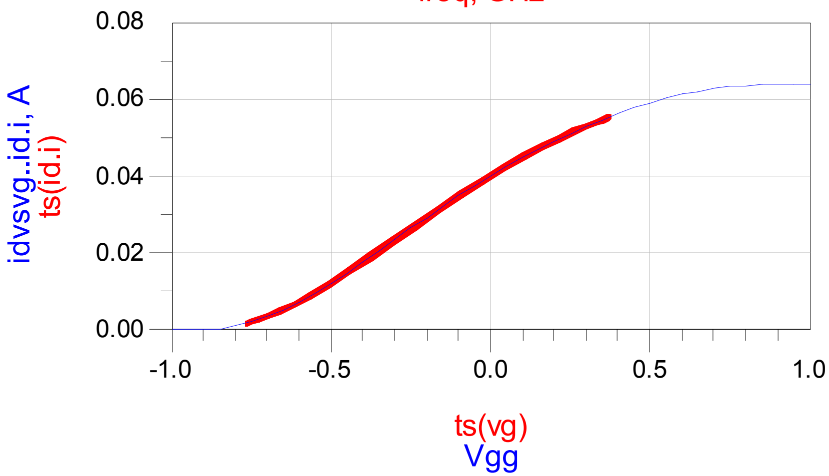




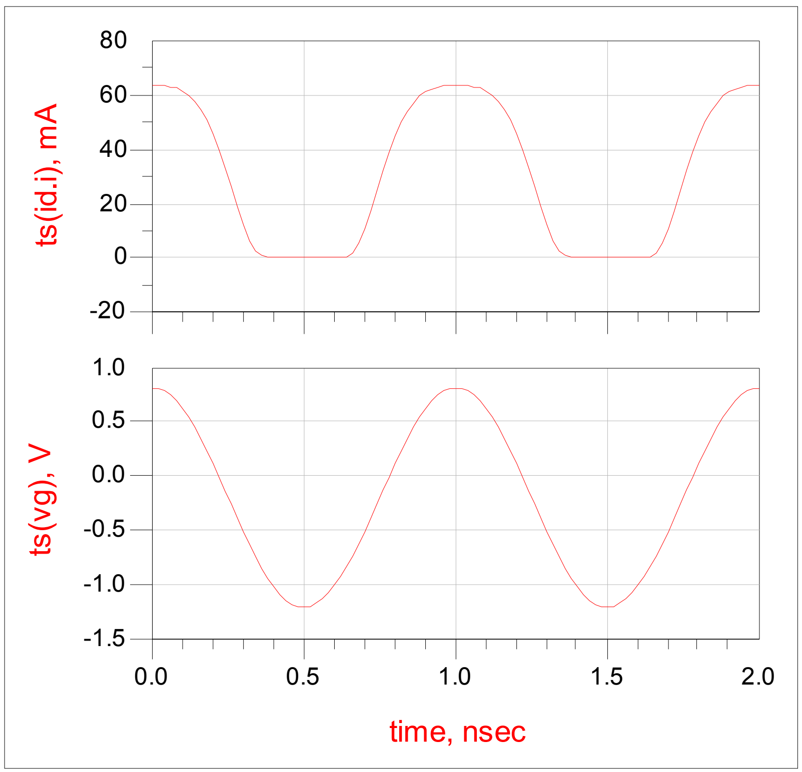
Bias for odd harmonics, max gm-point
not-so-large signal 0 dBm input power
Not much of 3rd harmonic

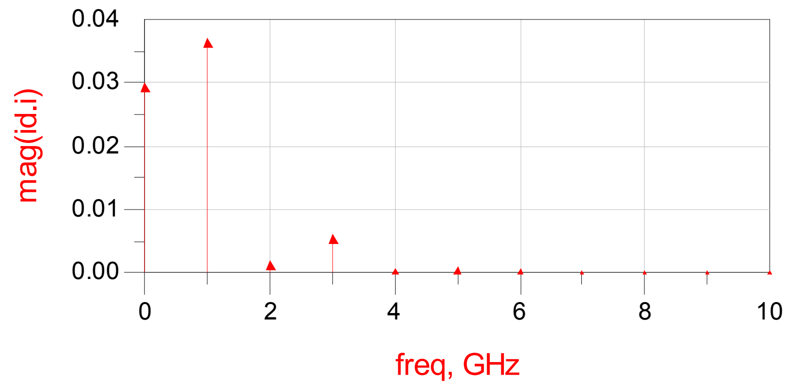


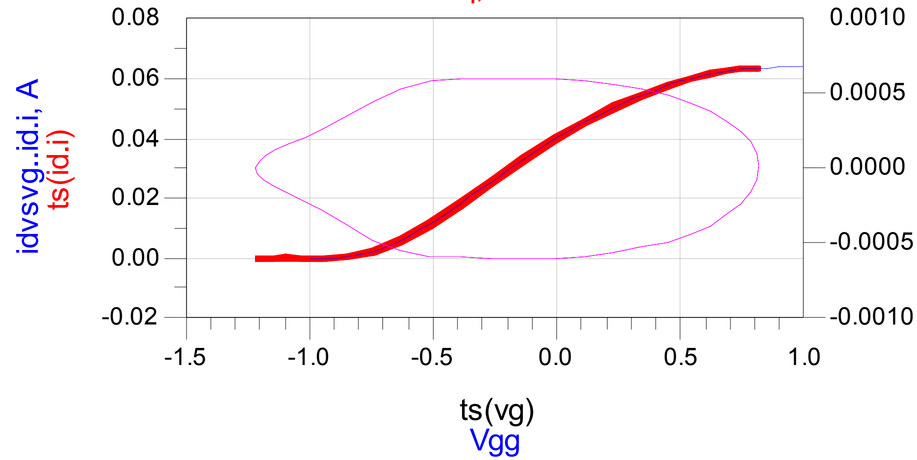




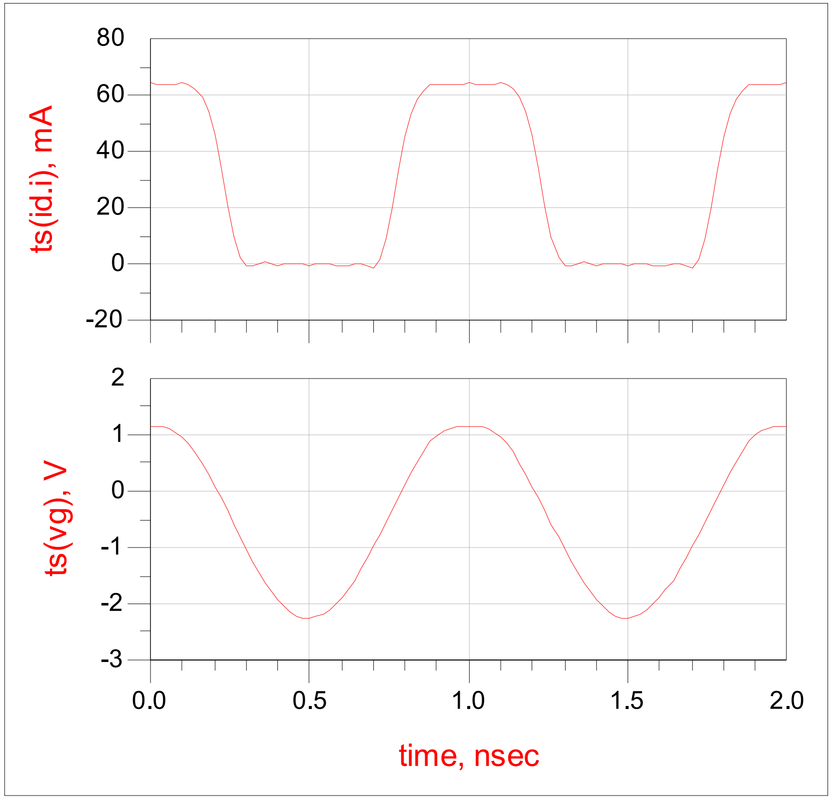
Bias for odd harmonics, max gm-point larger signal: 5 dBm input power

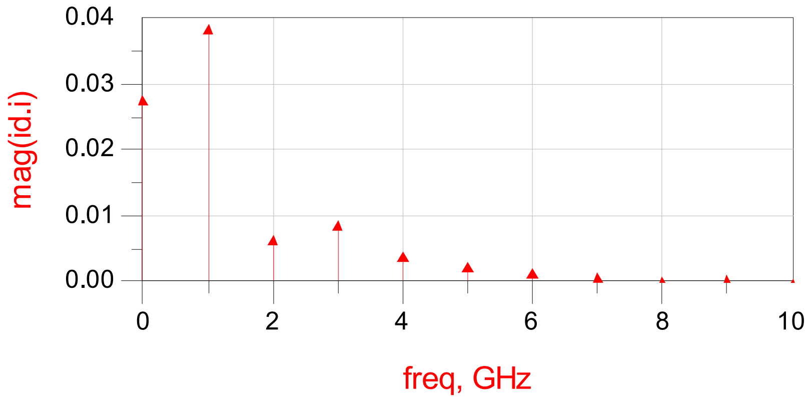


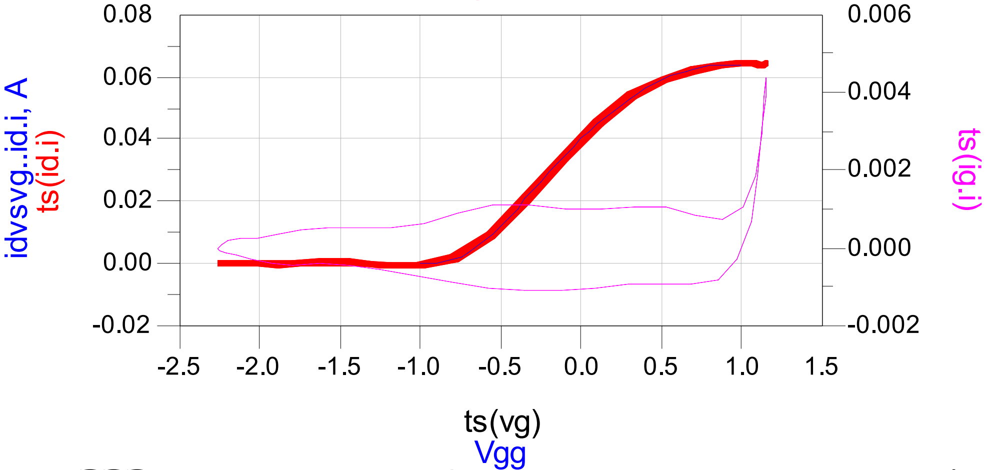




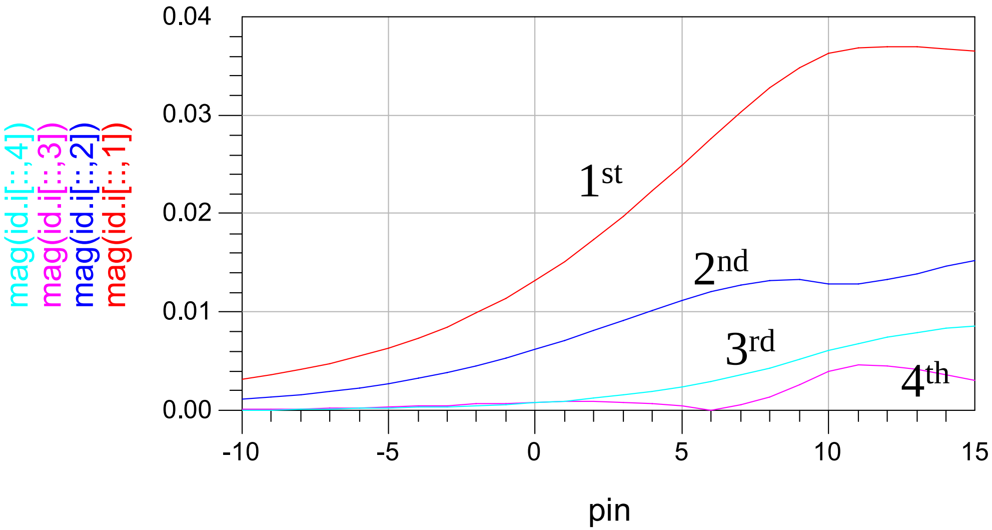
Bias for odd harmonics, max gm-point
even larger signal: 10 dBm input power
Clear gate conduction, 4 mA peak current, be careful !



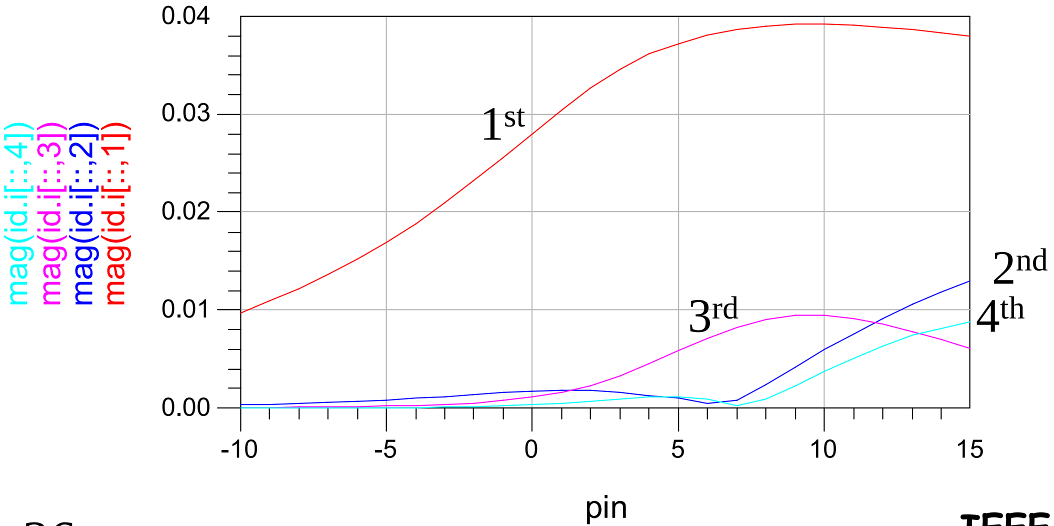




drain-current harmonics, **input power sweep**:

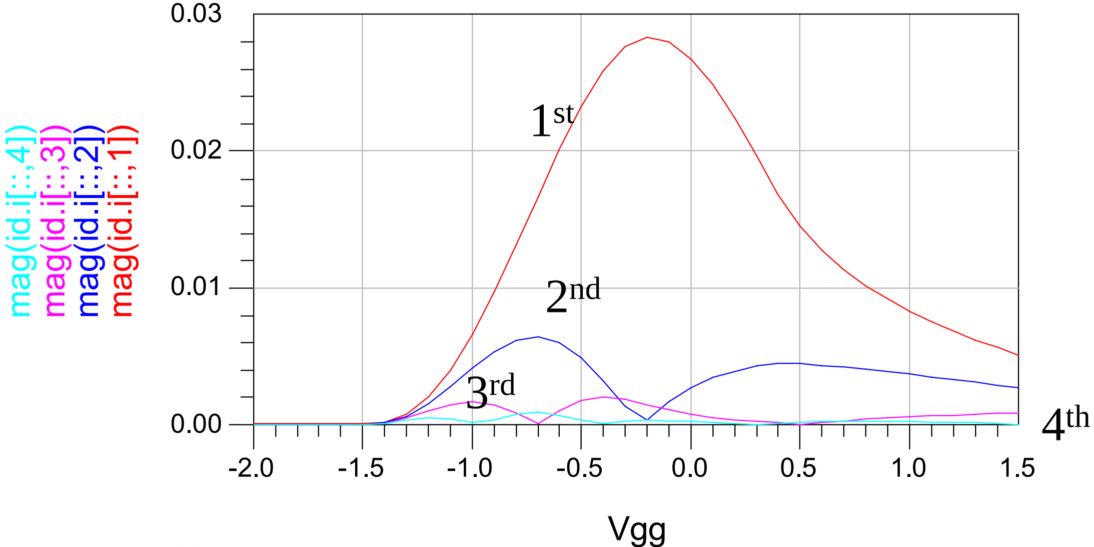


Even harmonic optimum
Vgg=-0.8V

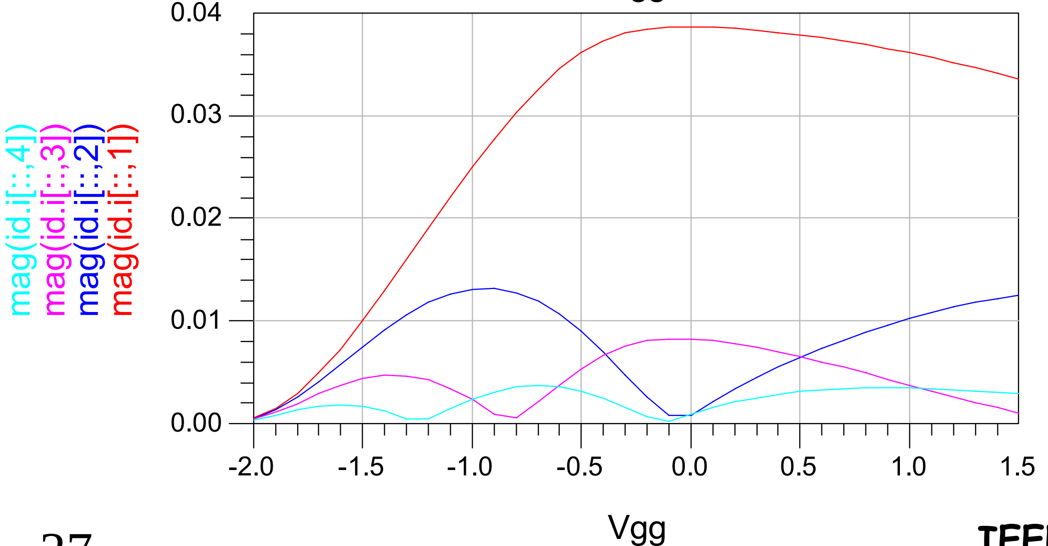


Odd harmonic optimum
Vgg=-0.1V

drain-current harmonics, **gate bias sweep**:



Pin=0dBm



Pin=7dBm

Fabrication

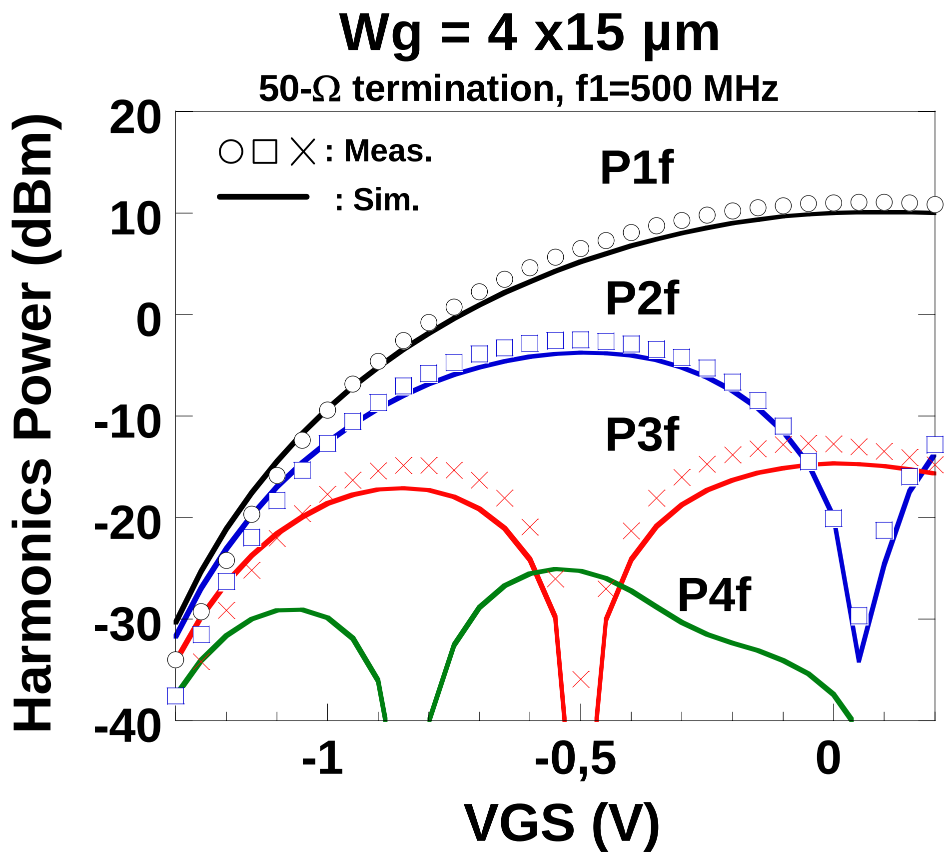
OMMIC D01PH process

pHEMT

- Lg = 0.14 µm
- f_T = 95 GHz
- f_{max} = 180 GHz
- g_{m_max} = 700 mS/mm
- Ids_{max} = 700 mA/mm

Spiral Inductor

- Q = 29
- L = 1 nH
- @ 28 GHz

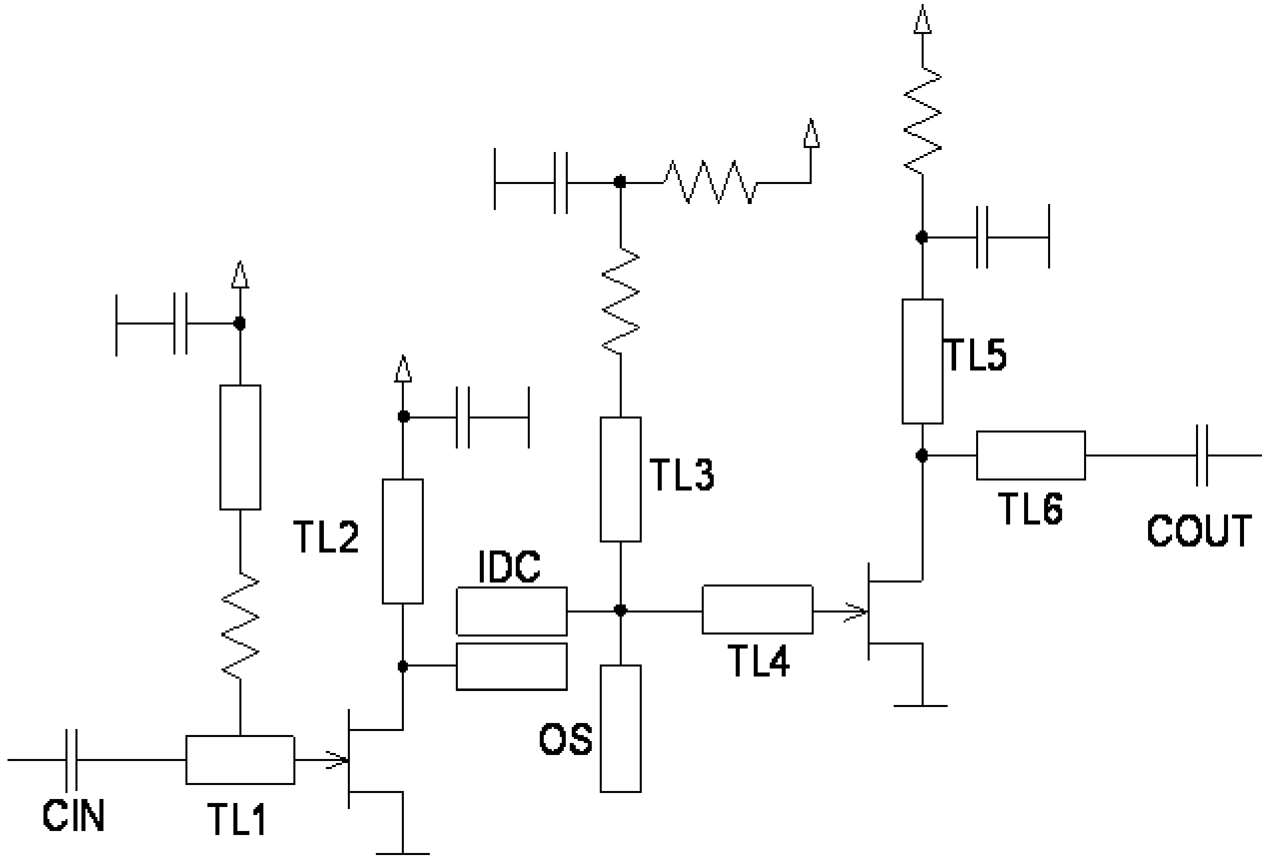


A 16-32 GHz Frequency Multiplier

Design Goals

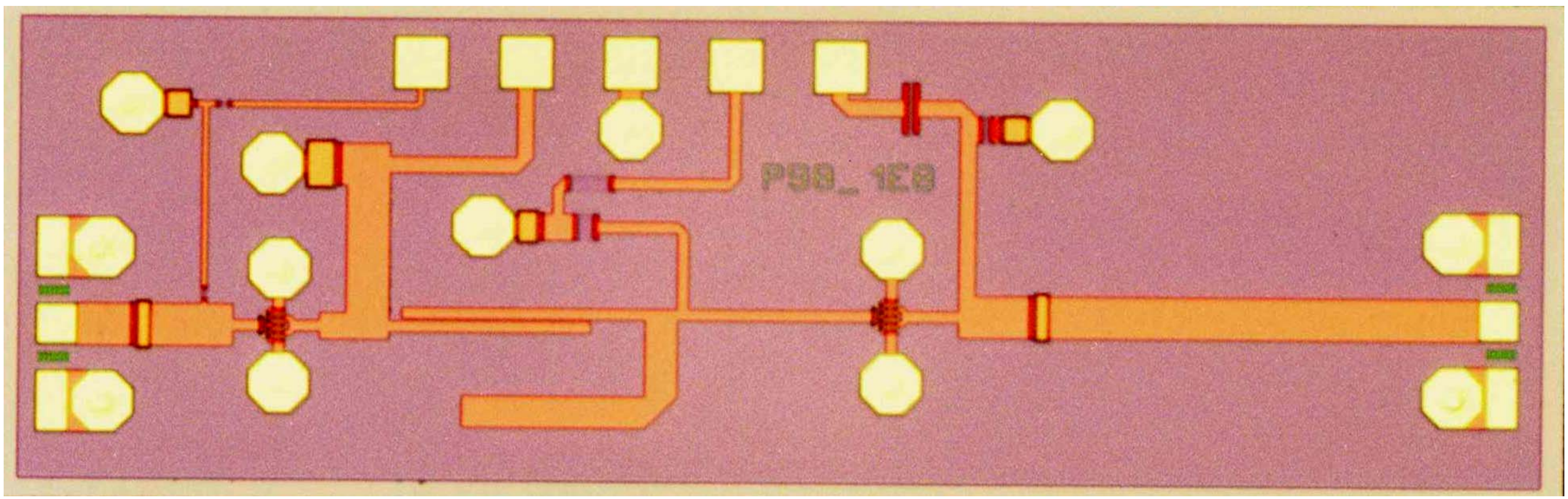
- Input frequency, f_{in} = 16 GHz
- High rejection of unwanted harmonics
- Low power consumption

Circuit Topology



Layout

- Chip size 3×1 mm^2



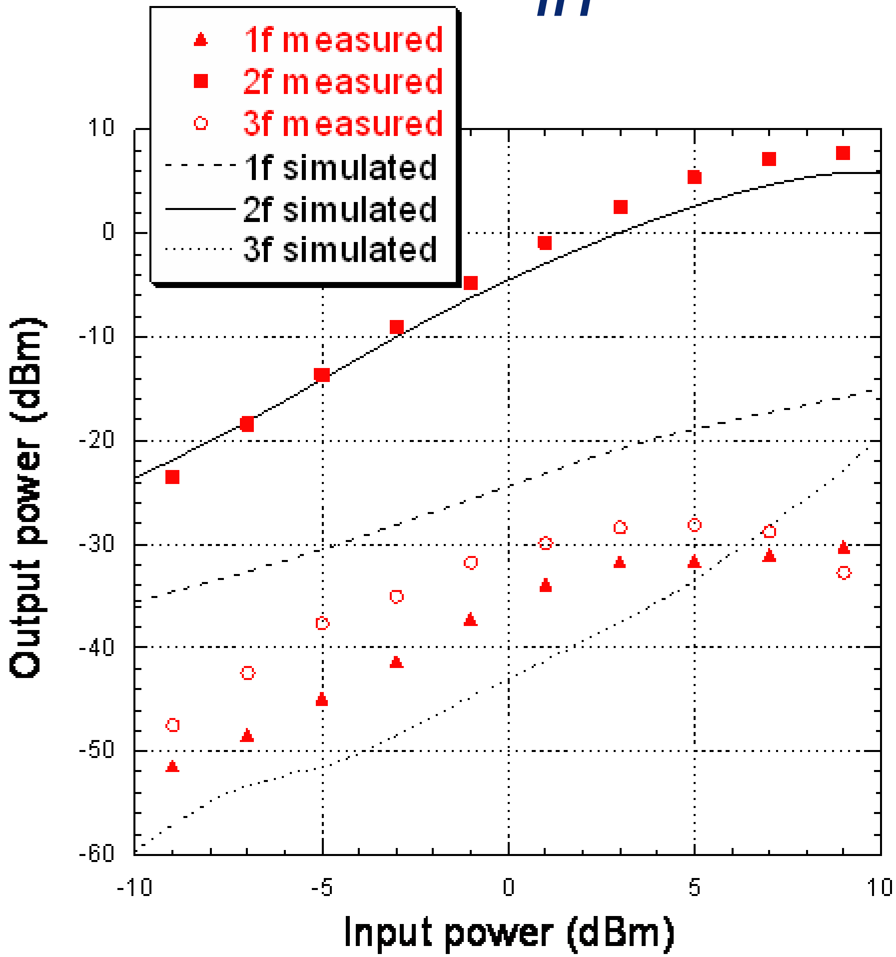
Simulated Results

- Conversion gain ≈ 0 dB
- Output power ≈ 0 dBm
- Rejection of unwanted harmonics > 20 dB
- P_{DC} ≈ 40 mW
- 3-dB bandwidth > 30 %

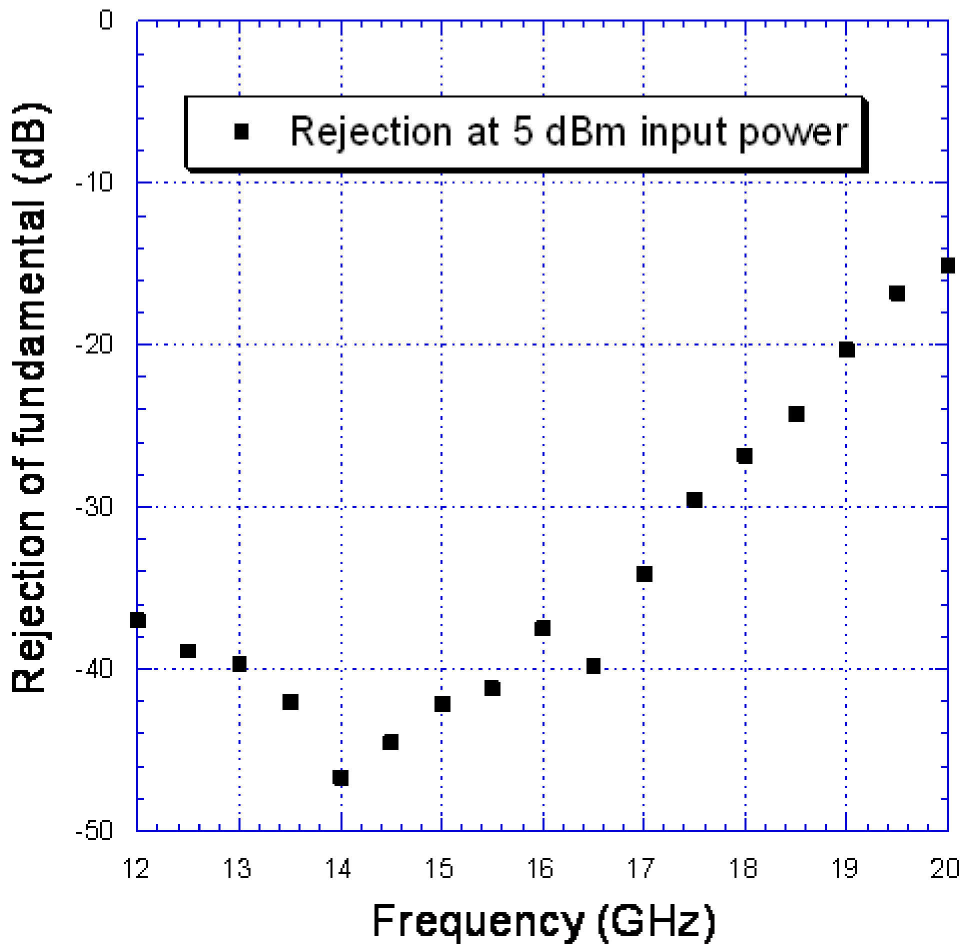
Measurements

- On-chip measurements using coplanar probing
- Rejection of unwanted harmonics > 25 dB
- P_{DC} = 40 mW
- 3-dB bandwidth ≈ 25 %

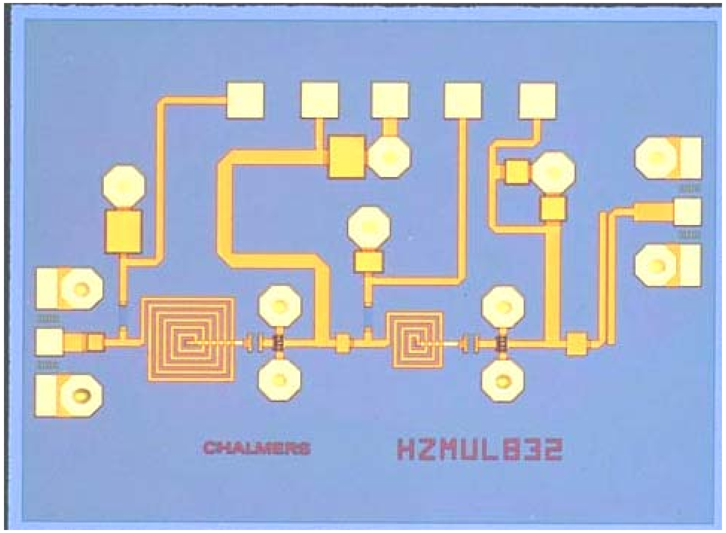
Output Power Versus Input Power at f_{in} = 16 GHz



Rejection of Fundamental Frequency @ 5 dBm Input Power

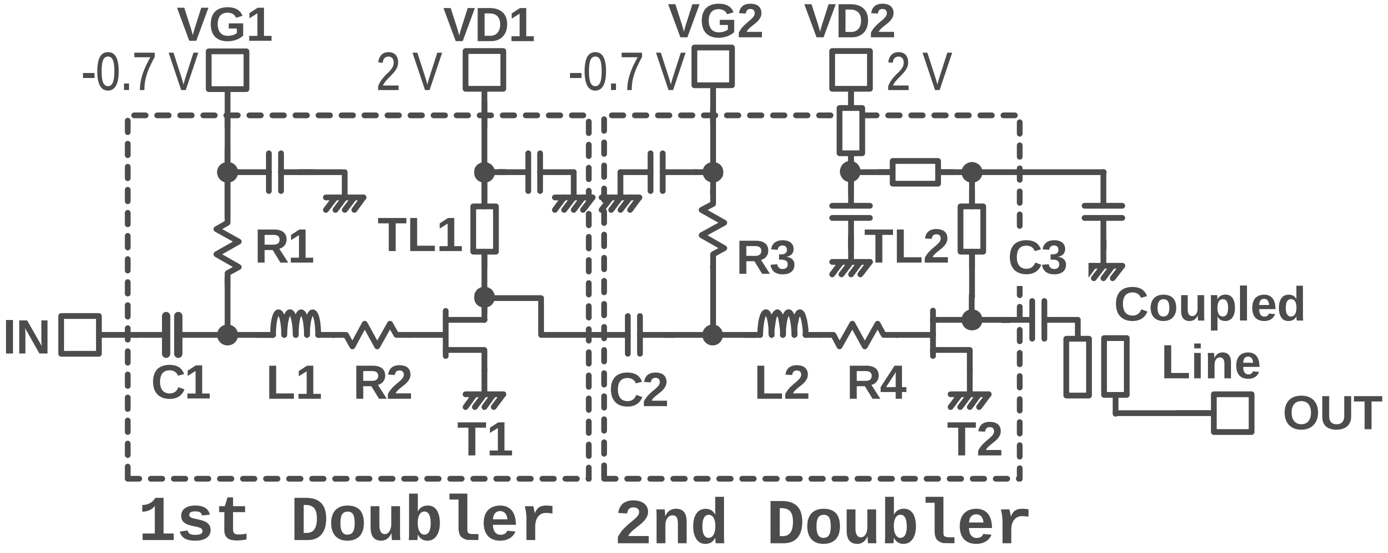


32GHz Quadrupler(I) - Schematic



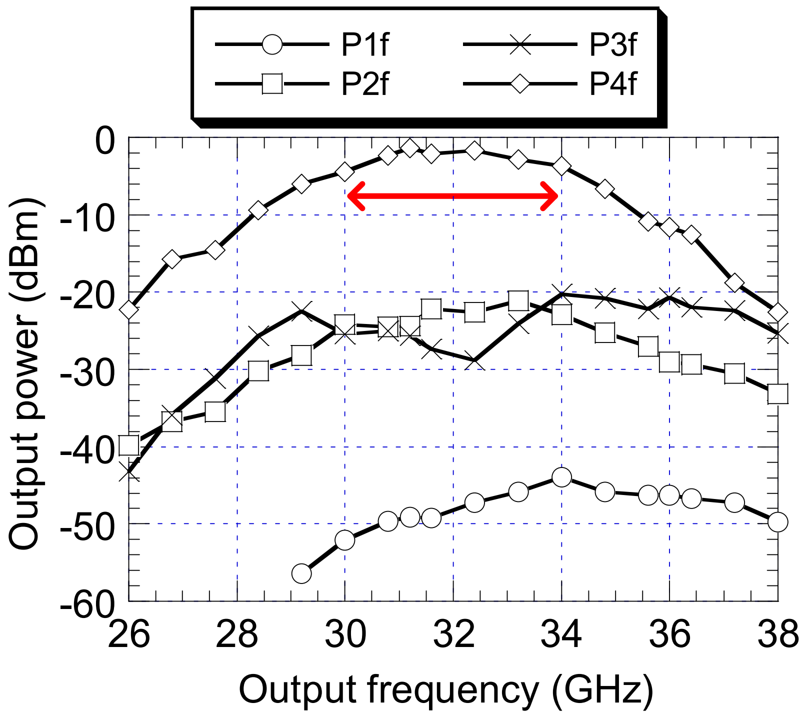
- Doubler + Doubler
- High Conversion Efficiency
- Large-area components (L1, TL1)
- 2 x 1.5 mm^2 chip

Design:
Herbert Zirath



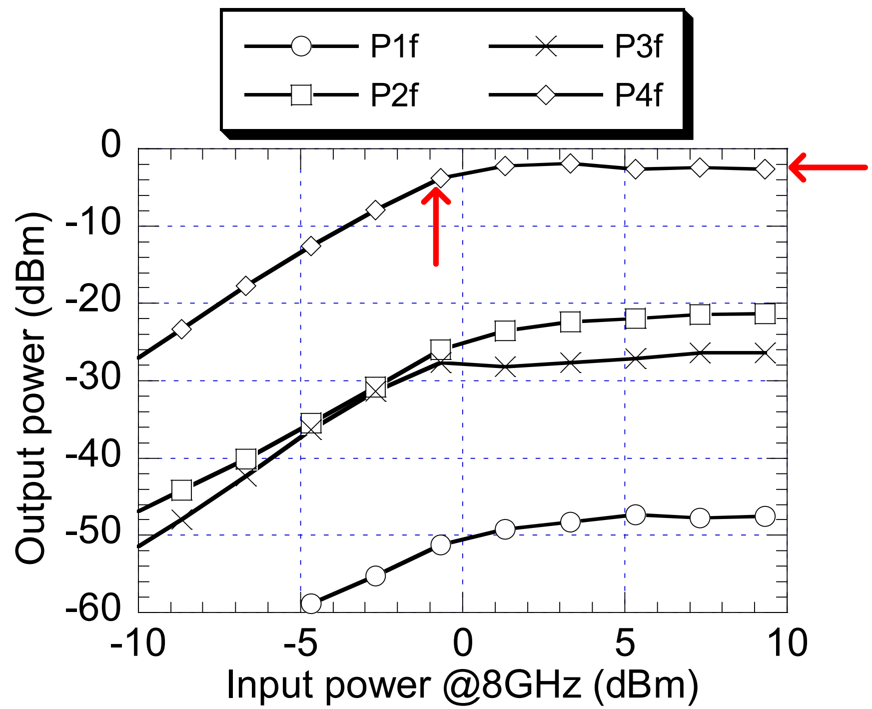
32GHz Quadrupler(I) - Measured Results

- **Pdc = 16 mW (@Pin = 0 dBm)**



Pin = +3.3 dBm

Output -3dB Bandwidth = 4 GHz



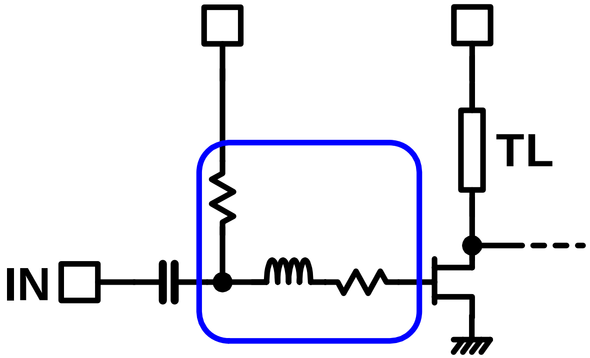
Fout = 32 GHz

$Conv.Gain_{max}$ = -3 dB

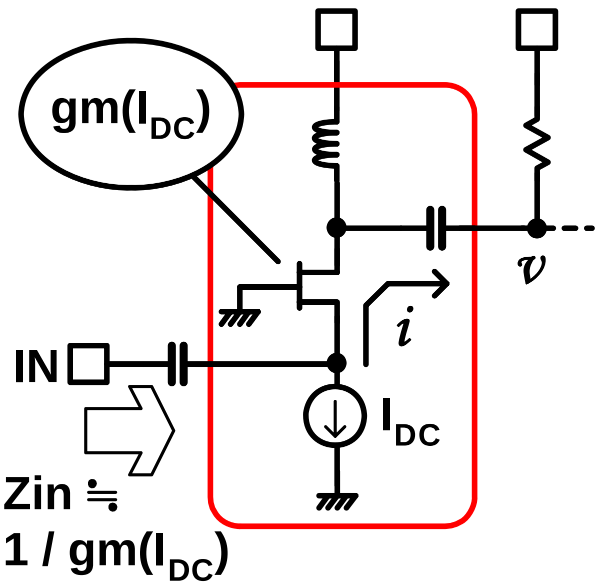
$P4f_{sat}$ = -2 dBm

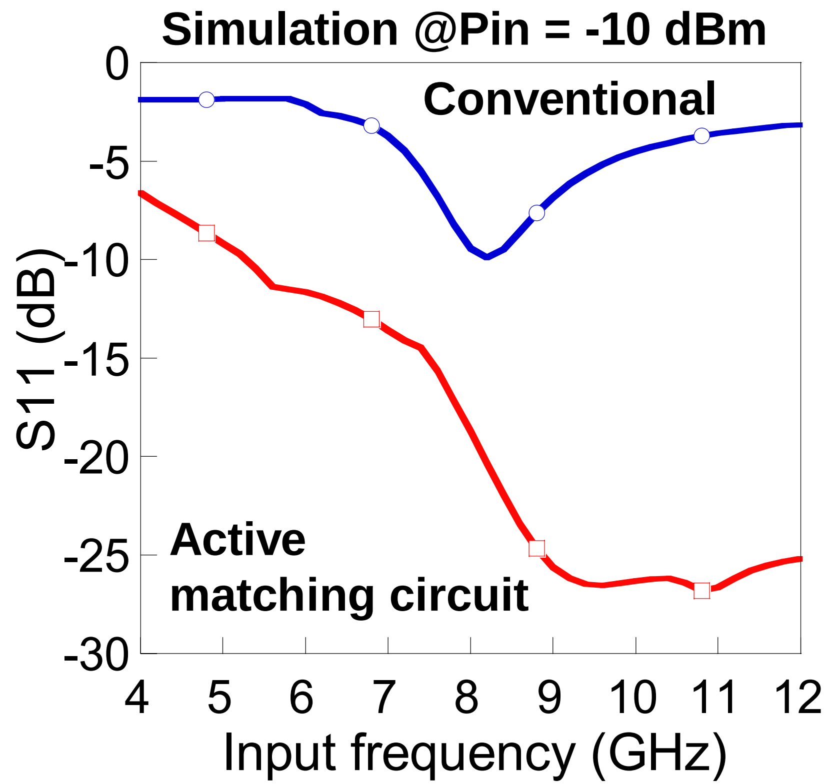
32GHz Quadrupler(II) - Concept

- **Conventional**

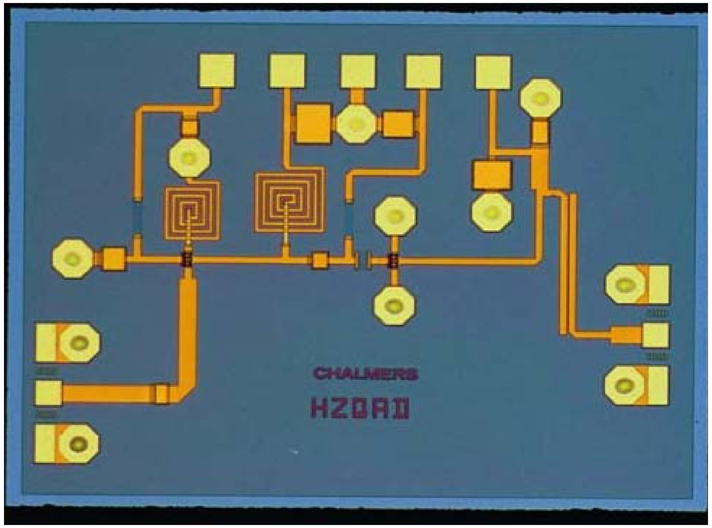


- **Active Matching Circuit**

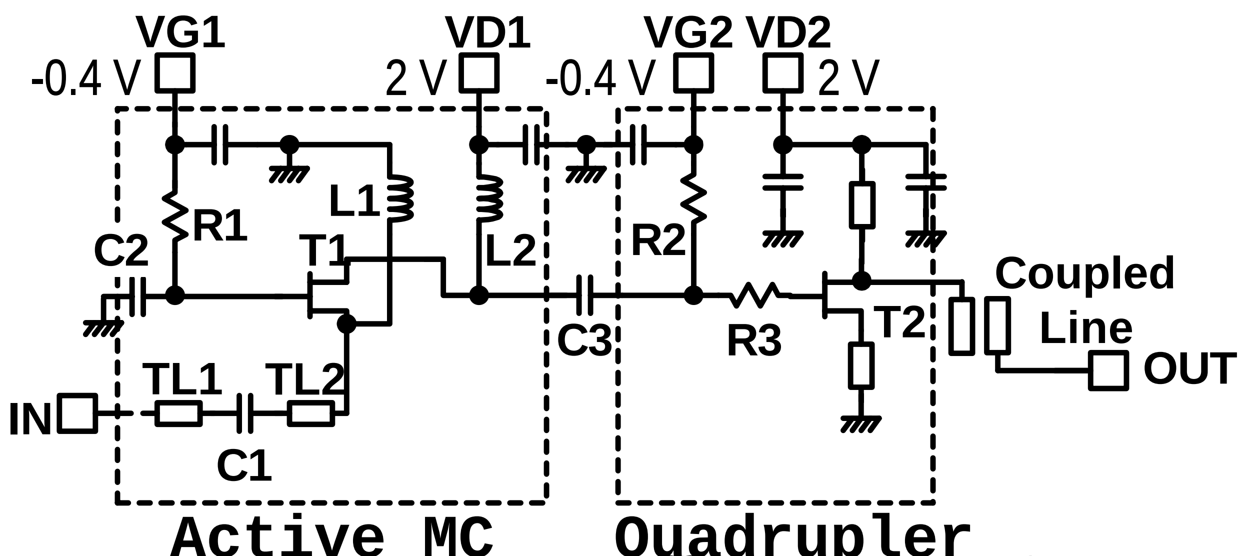




32GHz Quadrupler(II) - Schematic

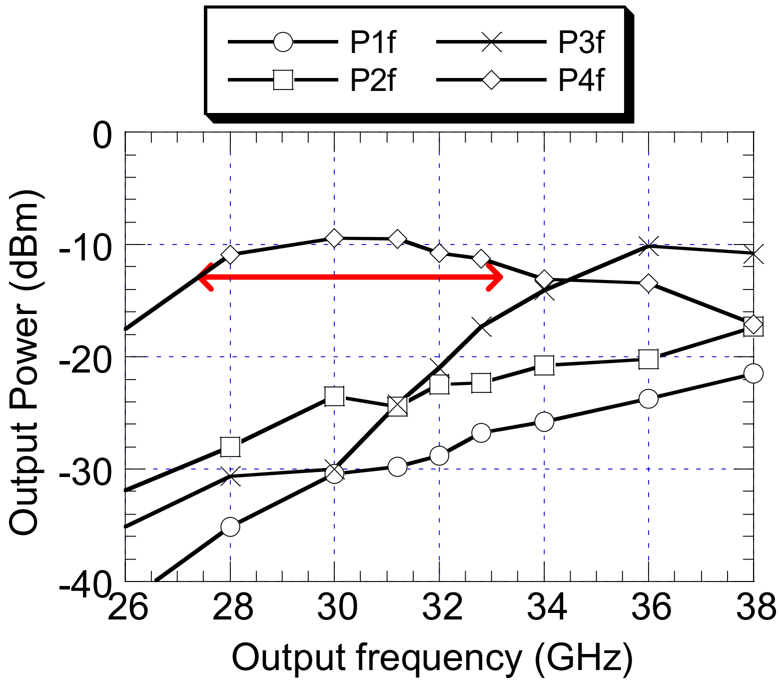


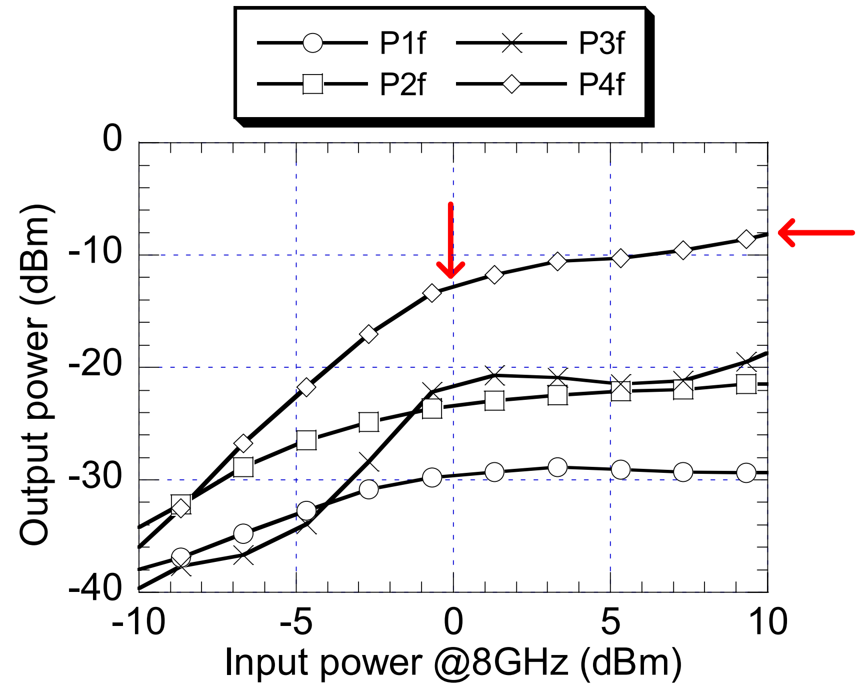
- Common-gate stage + Quadrupler
- Active Matching Circuit (MC)
  - ✓ Wideband matching
  - ✓ Small chip-area
- 2 x 1.5 mm^2 chip



32GHz Quadrupler(II) - Measured Results

- **Pdc = 28 mW (@Pin = 0 dBm)**





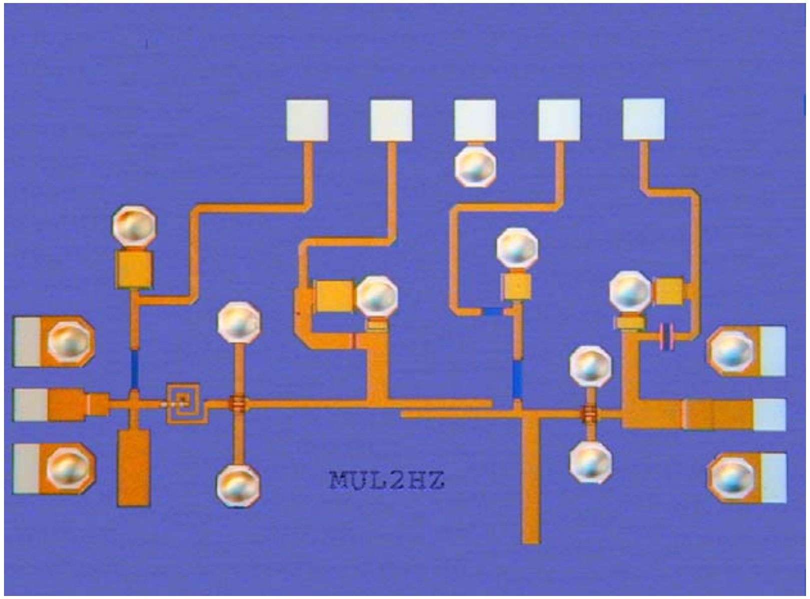
Pin = +3.3 dBm

Output -3dB B.W. = 6 GHz

Fout = 32 GHz

Conv.Gain$_{max}$ = -13 dB

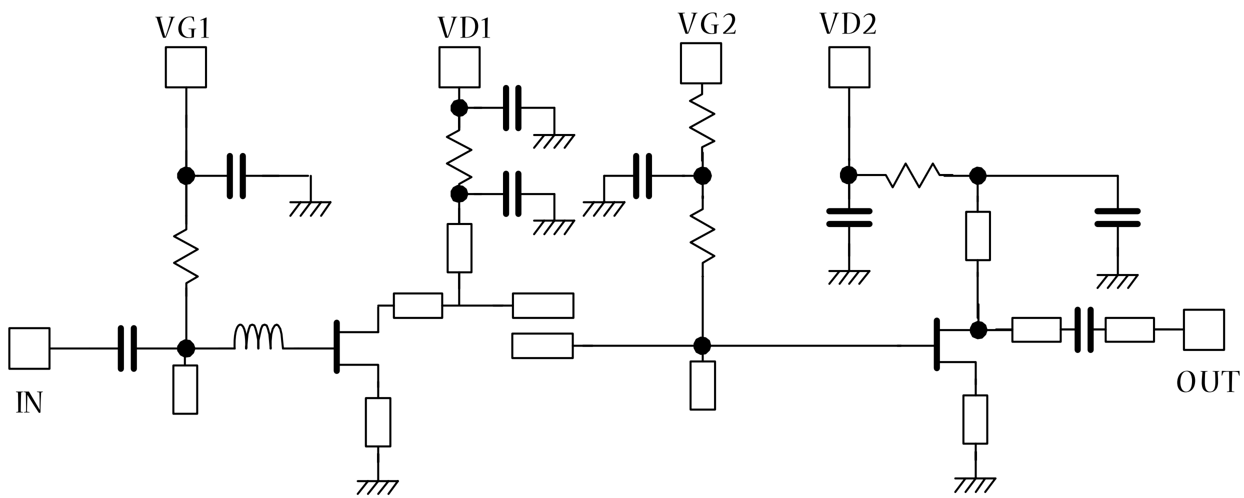
P4f$_{sat}$ = -8 dBm



56 GHz doubler design

Doubler+ buffer amplifier
DC-power minimized
Each device is 4x25 um

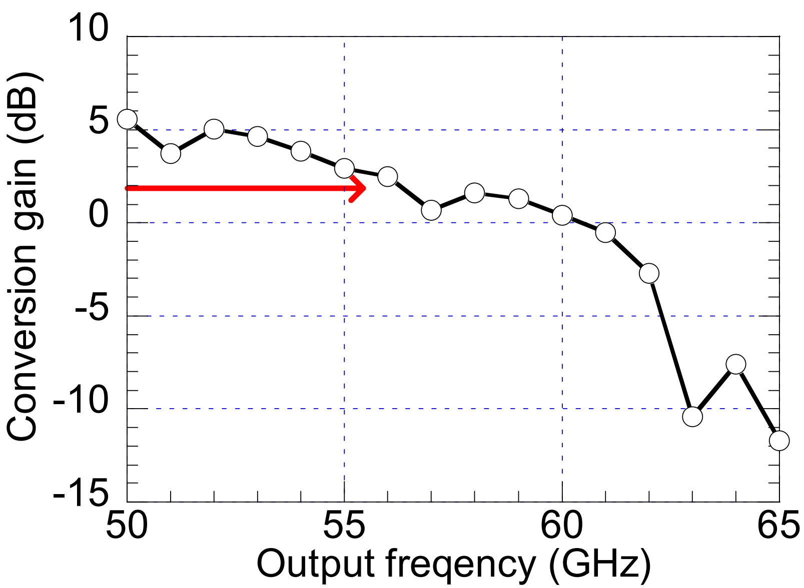
Design:
Herbert Zirath

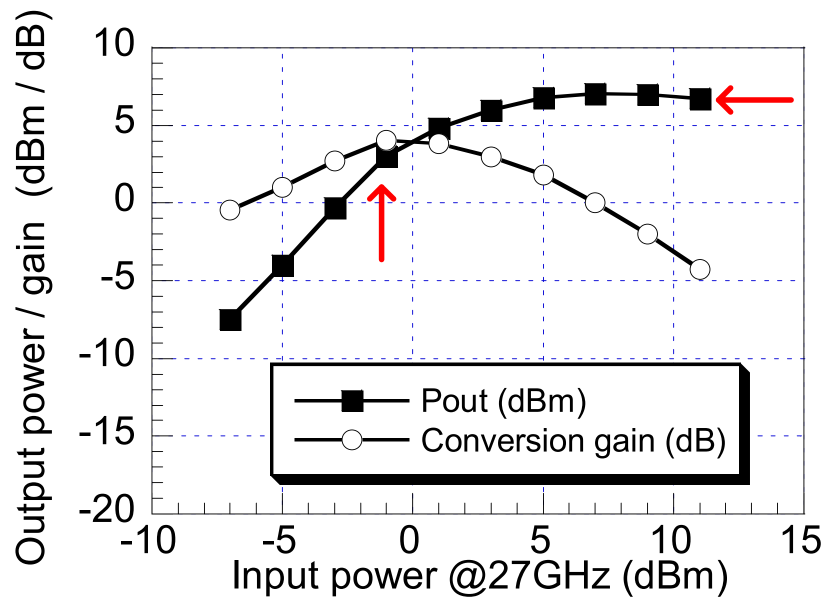


(a) Acitive frequency doubler with an amplifier stage.

56GHz Doubler - Measured Results

- **Pdc = 66 mW (@Pin = 0 dBm)**





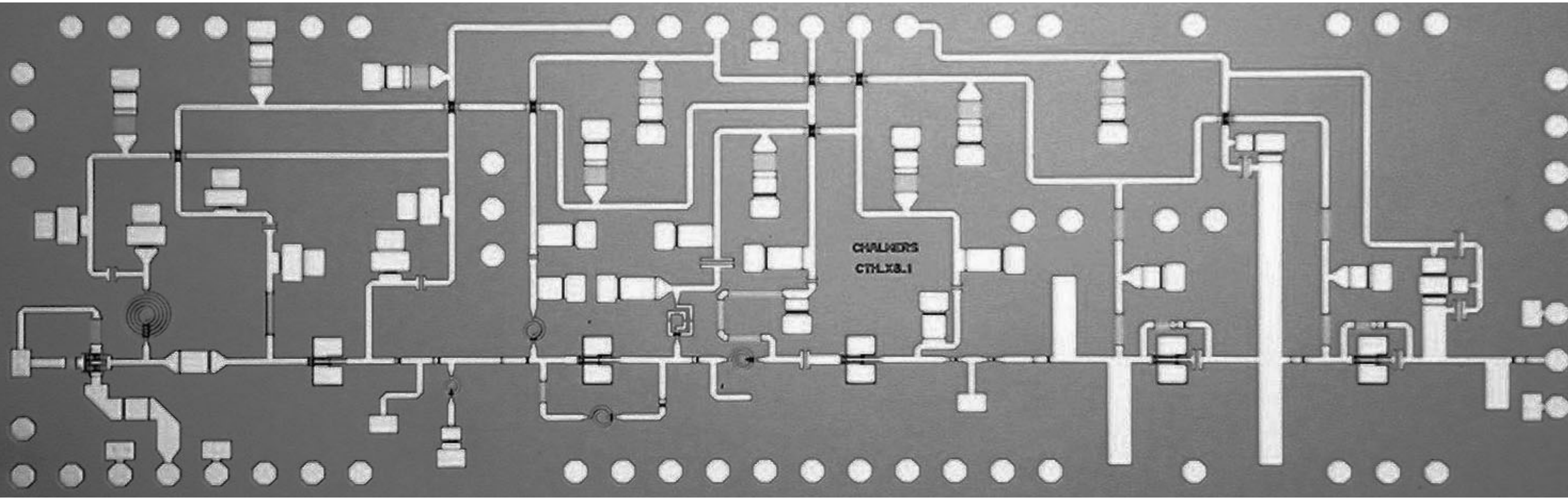
Pin = +1 dBm

Fout = 54 GHz

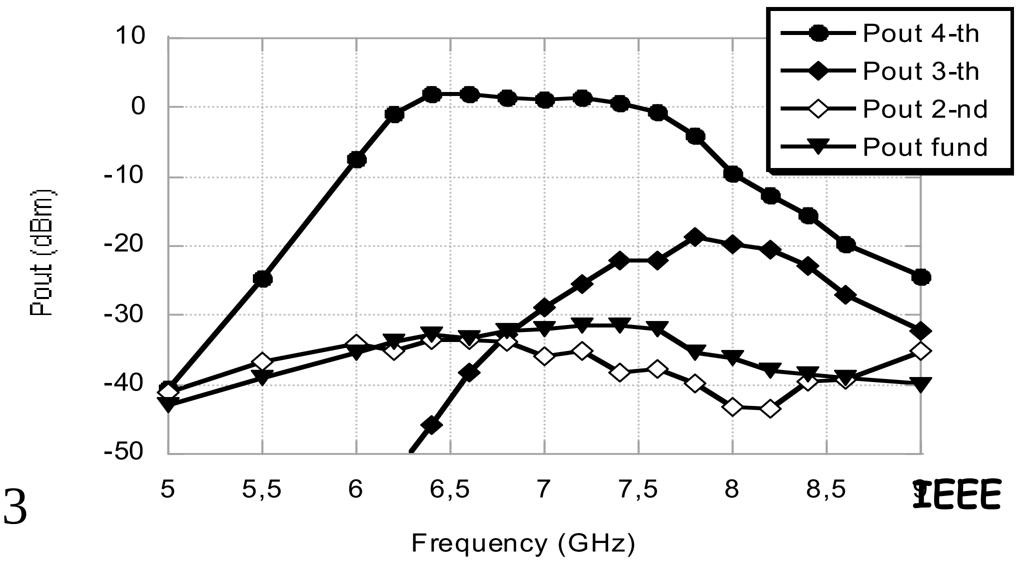
Conv.Gain$_{max}$ = 4 dB

P2f$_{sat}$ = 7 dBm

X8 multiplier on WIN pHEMT PP-15 process



Result x4 breakout:



Measured output power of the 4th, 3rd, 2nd harmonic and fundamental frequency versus frequency at 0 dBm input power.