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für Höchstfrequenztechnik

Flip-Chip for MM-Wave and Broadband Packaging

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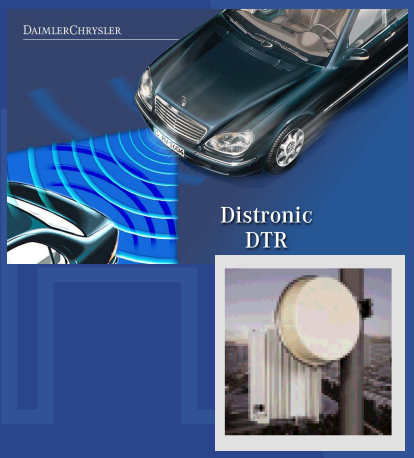
Motivation

Growing markets for mm-wave systems, e.g.

- 77 GHz automotive radar
- 60 GHz wireless communications
- 40 GHz radio links
- high bit-rate electronics (40 Gbps and beyond)

ICs are available: GaAs, SiGe, (CMOS)

What about packaging (low cost !)



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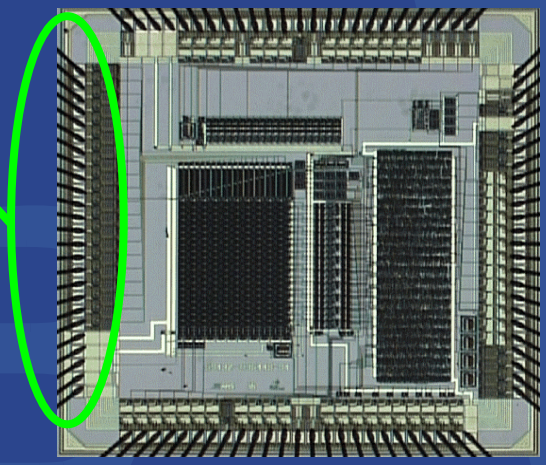
Packaging a mm-wave IC (I)

As conventional
- same as for VLSI chips ?

High frequency
-> increased parasitics
at interconnects



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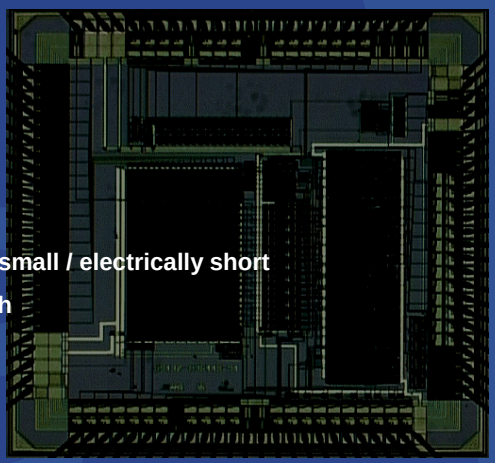
Packaging a mm-wave IC (II)

As conventional
- same as for VLSI chips ?

High frequency
-> increased parasitics
at interconnects

General rule: keep dimensions small / electrically short

- compact mounting approach
- miniaturized interconnects



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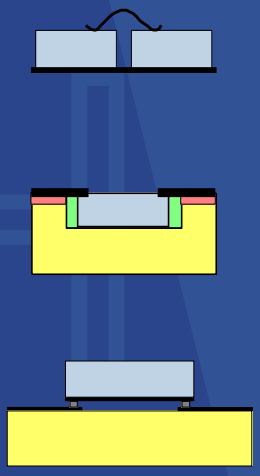
Techniques available

Wire bonding (up to 40 GHz and beyond)
- tight tolerances
- narrow-band (compensation)

Embedded chips
- interconnect smaller than for wire bonding
- impedance mismatch due to gap (tolerances!)

Flip-chip
- smallest interconnect
- well-controlled geometry



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Packaging is more than just the interconnect

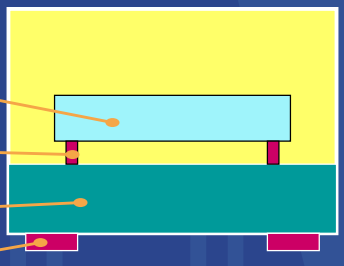
The generic structure

Chips: GaAs, SiGe
- microstrip, coplanar, TFMSL

0-level interconnect
(e.g. flip-chip)

Carrier substrate

1-level interconnect
(flip-chip, ball grids)



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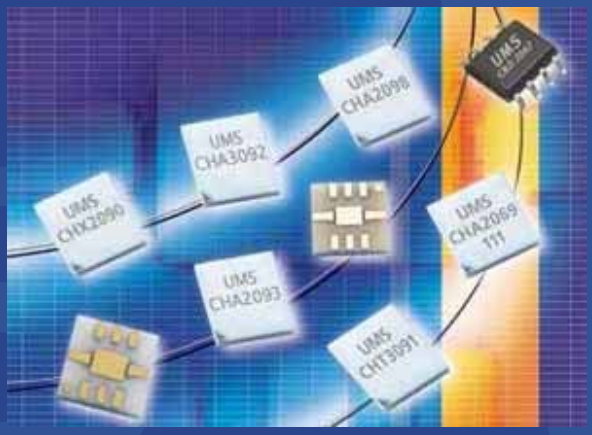
Example: SMD chips at mm waves

United monolithic Semiconductors (UMS)

- Very attractive, but general approach for mm-waves ?



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This talk

Flip-chip for mm-wave and broadband packaging

- identify key issues from electrical / em design point of view
- provide understanding of mechanisms

Needs comprehensive view

- flip-chip interconnect
- carrier substrate & housing

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Contents

The flip-chip interconnect
- overview on processes
- mm-wave & broad-band characteristics
- parasitic moding
- hot-via interconnect

The package
- thin-film & flip chip
- LTCC as carrier substrate

Conclusions

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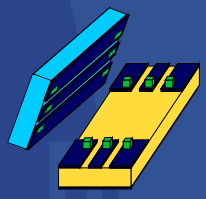
Flip-chip processes for mm-waves



Chip interconnect by means of bumps

Two technologies:

(i) Thermocompression
- Au bumps (using electroplating or stud bumps)
- bonding by thermocompression

(ii) Soldering
- e.g., AuSn bumps
- chip bonding & soldering in reflow oven

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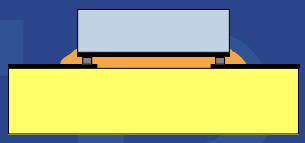
Which issues need to be considered?

Electrical characteristics

Thermal behavior

- heat-sinking (incl. additional thermal bumps)
- CTE mismatch (materials, chip size, underfiller?)



Manufacturability / cost

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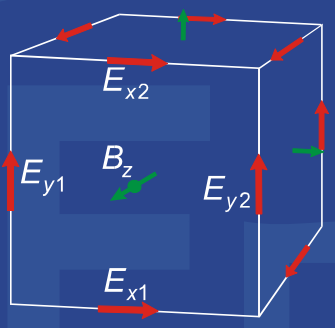
A remark on 3D electromagnetic simulation



Tools used

- Based on finite-difference / finite-integration method
- F3D: FBH in-house code
  - frequency domain (FDFD)
- Microwave Studio (CST)
  - time domain (FDTD)

CST GMBH

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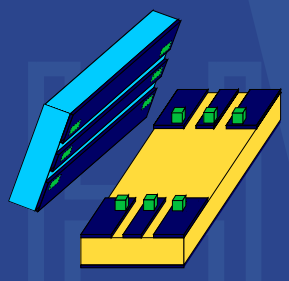
The flip-chip interconnect: mm-wave characteristics

Flip-chip approach

- well-known for lower frequencies
- suitable also for mm-waves because of small dimensions

Two main RF effects

- detuning of on-chip circuit
- reflections at bump transition



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Detuning

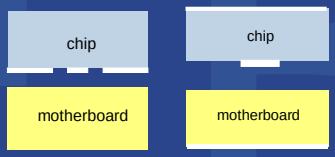
Changes of circuit behavior due to flip-chip mounting

Most critical elements: passives

- **transmission lines**
- **spiral inductors**

Underfiller has a particular influence

Transmission lines can be used as a benchmark



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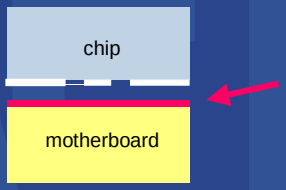
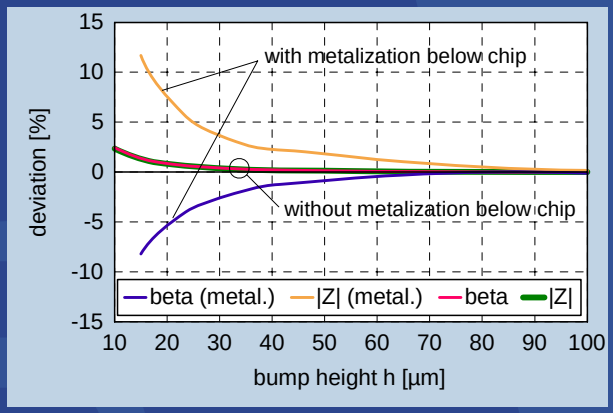
CPW : deviation β/β_0 and Z vs. bump height h

Chip: 50 µm wide CPW

With/without metalization on motherboard below chip

f = 50 GHz





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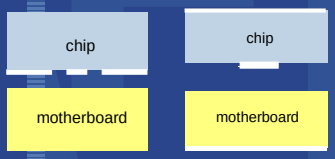
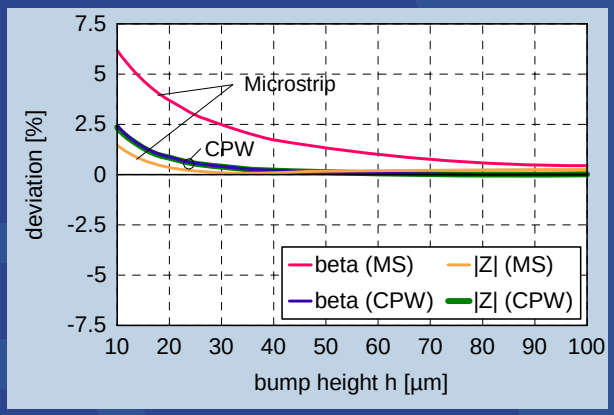
Detuning: comparison CPW & microstrip on GaAs

Deviation β/β_0 and Z vs. bump height h

- 50 µm wide CPW
- microstrip (MS): 72 µm strip on 100 µm substrate
- f = 50 GHz





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Chip detuning: design rules

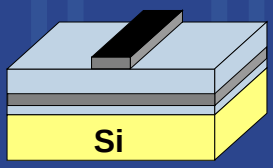
Avoid metalization on carrier substrate below chip

Minimum bump height h_{min} ($\Delta\beta < 1.5\%$) :

- CPW (50 µm wide): 15 µm -> 0.3 ground-to-ground spacing
- MS (100 µm-GaAs): 50 µm -> half the substrate thickness

Relaxed constraints for chips

- with small line cross-sections or
- without critical elements (transmission-line / spiral inductors)
- e.g. Si designs, digital circuits



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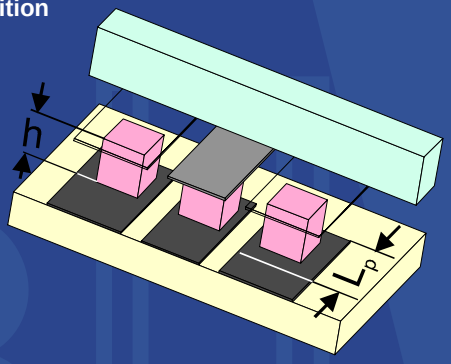
Reflections at the interconnect

Basic structure: CPW-to-CPW transition

Bump geometry

- **height h**
- **diameter l**
  and related quantities
  - **pad size l_p**
  - **total width of transition**



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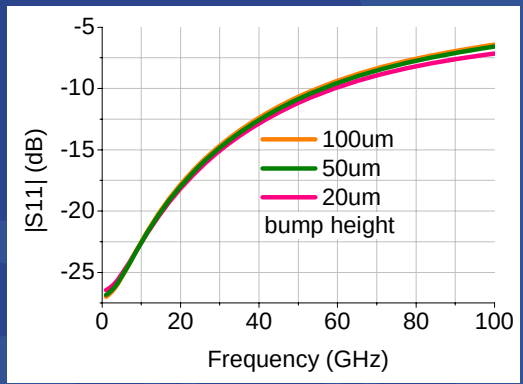
S_{11} for 80 µm bumps: Influence of bump height

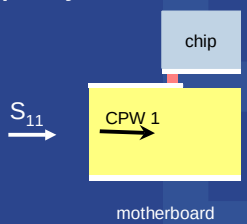
3D FDFD simulations

Bump geometry

- **diameter l = 80 µm**
- **pad size l_p = 100 µm**
- **height h = 20…100 µm**

$|S_{11}|$ for CPW mode vs. frequency





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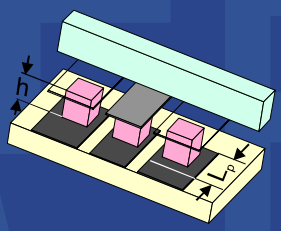
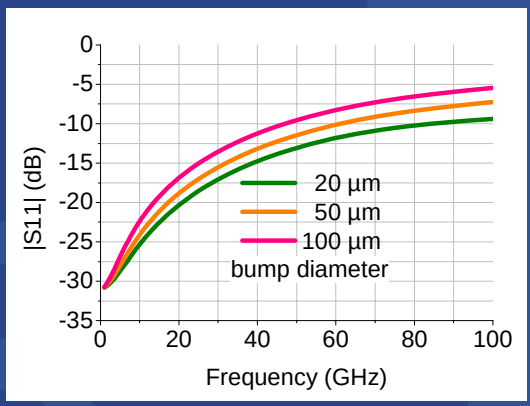
Influence of bump diameter

- constant pad size: 100 µm
- bump height = 50 µm
- bump diameter 20...100 µm
- Small deviations





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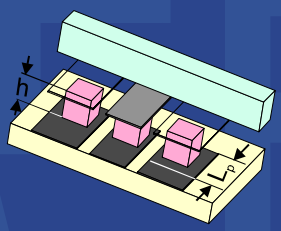
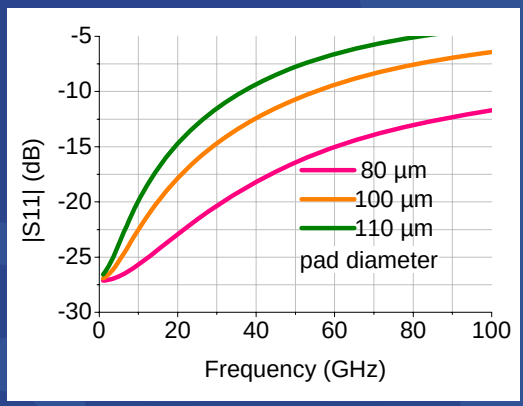
Influence of pad size

- bump height = 80 µm
- bump diameter = 80 µm
- pad size 80...110 µm
- most sensitive parameter





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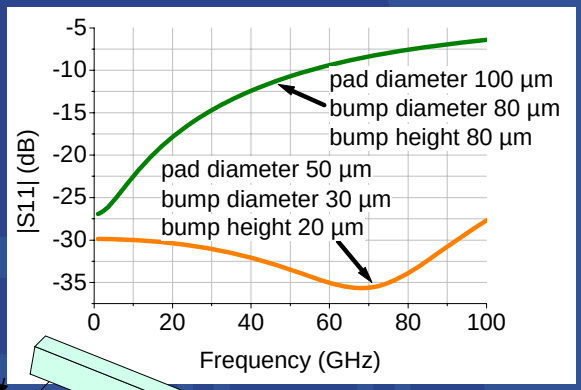
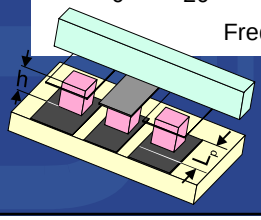
Comparison small / large bumps

- High-freqency performance depends on interconnect size
- 30 µm bumps: excellent broadband characteristics over 100 GHz
- In practice: 2 parameters dictate overall dimensions
  - bump size
  - min. pad size & spacing on carrier substrate





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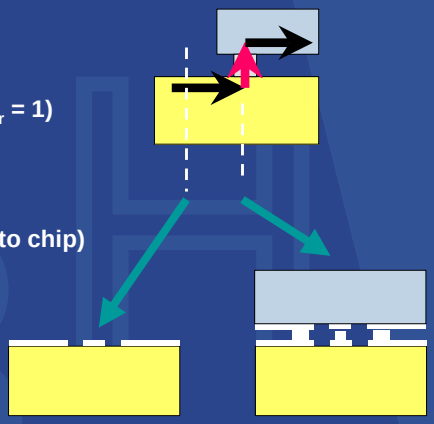
Electrical characteristics: capacitive or inductive ?

Two effects

- inductive
  (bumps: coplanar structure with $\varepsilon_r = 1$)
- capacitive (dielectric loading due to chip)



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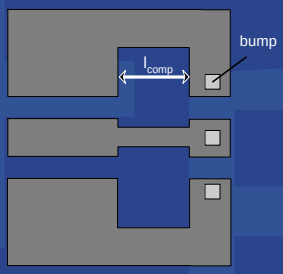
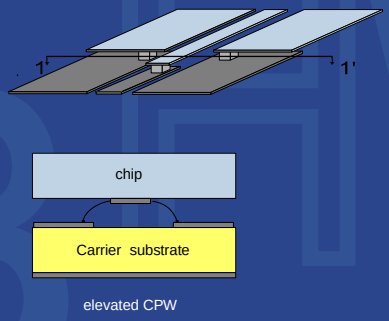
Optimized designs

Reduced reflection by means of compensation:

(i) high-impedance line section on motherboard



(ii) staggered bumps



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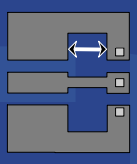
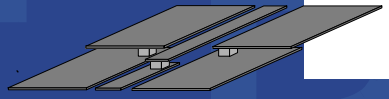
Reflection S11 w/o compensation

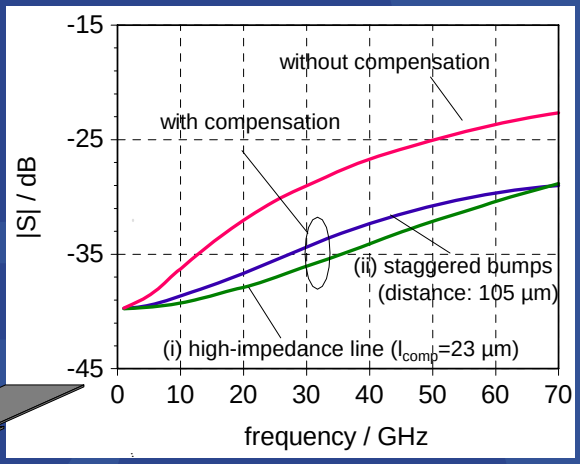
Bump height and diameter:
h = l = 25 µm
Pad length: lp = 50 µm

- **high-impedance line**



- **staggering**





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Flip-chip interconnect: design rules

Bump diameter and pad dimension critical parameter, not height (only detuning)

Capacitive behavior dominates

Bump / pad diameter

- **20...30 µm:** **good broadband mm-wave properties**
- **up to about 100 µm:** **possible with compensation**

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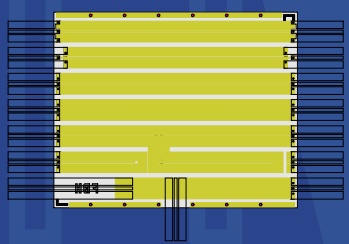
Verification by test structures

FC process by Alcatel (Stuttgart / Germany)

- **electroplated Au bumps**
- **thermo-compression bonding**

Bump geometry

- **diameter l = 35 µm**
- **pad length l_p = 60 µm**
- **height h = 22 µm**



GaAs test chips with passive structures

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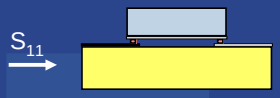
Measurement results on input reflection

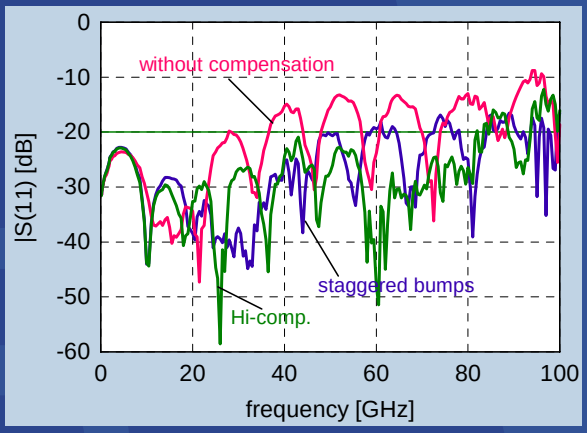
Back-to-back structure



$|S_{11}|$ for thru-line

- **uncompensated**
- **staggered bumps**

- **HI compensation**



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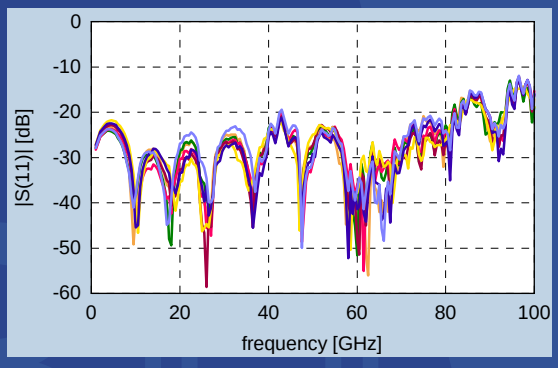
Measured results & reproducibility

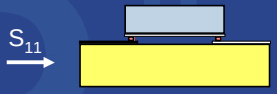
Compensated interconnect

- **20 dB return loss broad-band up to 80 GHz**
- **< 0.5 dB insertion loss per interconnect up to 100 GHz**

Excellent broadband performance

Good reproducibility (7 samples)





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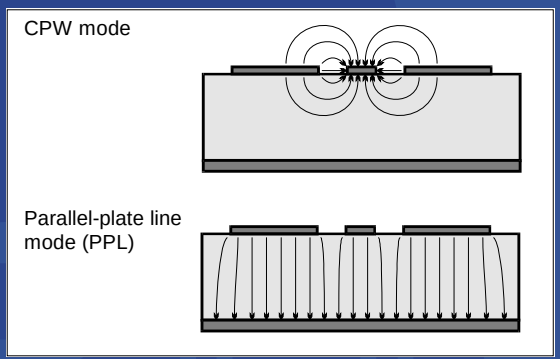
Be aware of parasitic modes

- Substrate modes due to multiple grounds
- Well known: PPL mode for conductor-backed CPW
- Package design must account for parasitic modes



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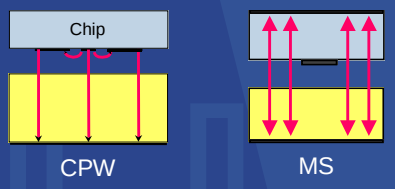
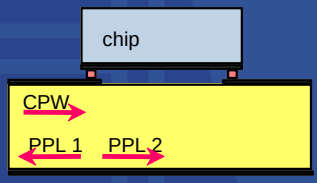
Parasitic substrate modes

Parallel-plate line (PPL) modes in flip-chip environment (below chip)

- for conductor-backed carriers
- present also in microstrip case



Excitation at interconnects & discontinuities



Result: unwanted crosstalk / coupling between chip interconnects and housing feedthroughs

- reduced isolation
- stability problems

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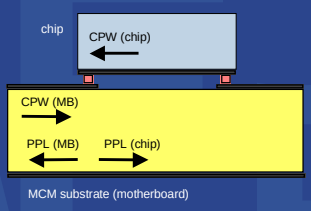
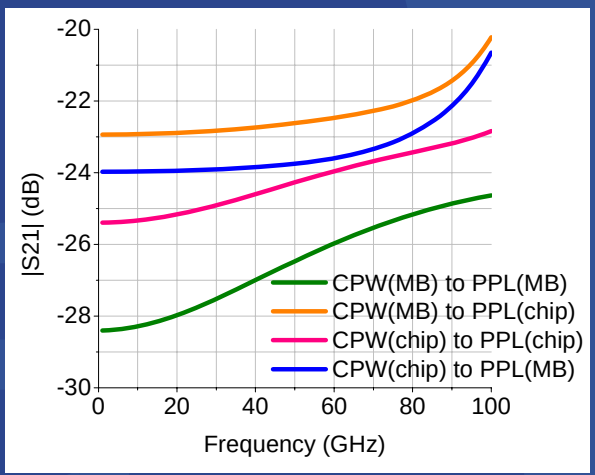
Coupling CPW to PPL modes : single transition

- bump diameter = 30 µm
- bump height = 20 µm
- pad diameter = 50 µm





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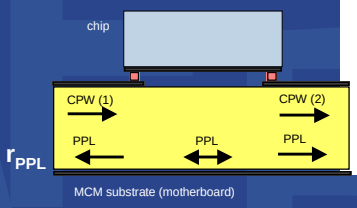
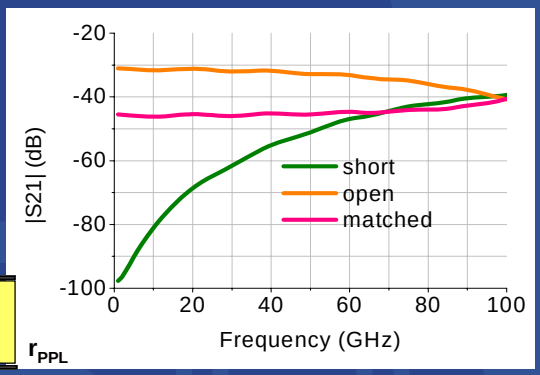
Coupling due to PPL modes: back-to-back structure (I)

- CPW stubs on chip
  - short
  - open
  - matched load
- $r_{ppl} = 0$



r_{PPL} r_{PPL}



bump diameter = 30 µm
bump height = 20 µm
pad diameter = 50 µm

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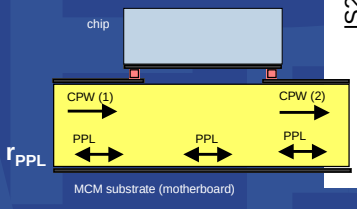
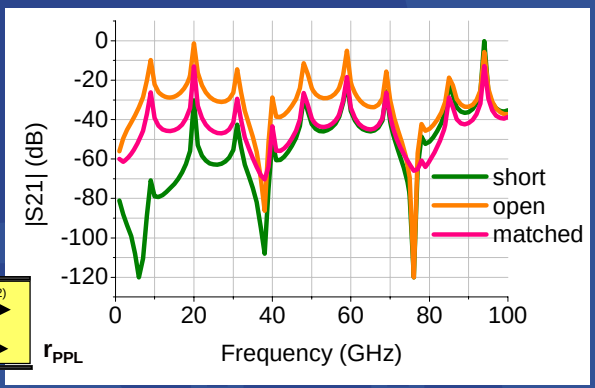
Coupling due to PPL modes: back-to-back structure (II)

- CPW stubs on chip
  - short
  - open
  - matched load
- $r_{ppl} = 1$ (resonator)



r_{PPL} r_{PPL}



bump diameter = 30 µm
bump height = 20 µm
pad diameter = 50 µm

- Reduced isolation -> instabilities

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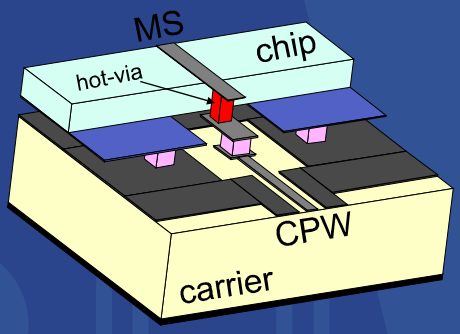
Flip-chip: The hot-via alternative

- Chip mounted frontside up
- Adapted to microstrip chips
- No detuning
- Requires chip backside process
- Higher reflections due to via interconnect



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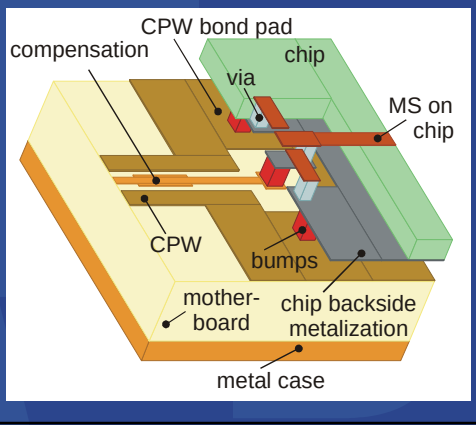
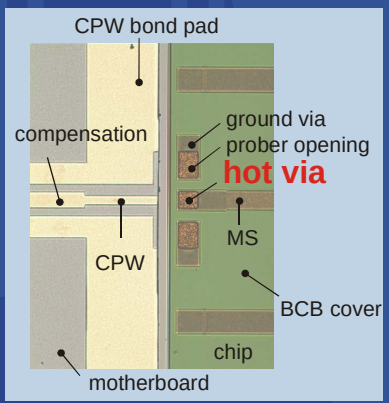
Hot-via design for 40 GHz (UMS / Ulm)

- Chip: in-out cell with on-wafer probing pads
- Compensation for 40 GHz





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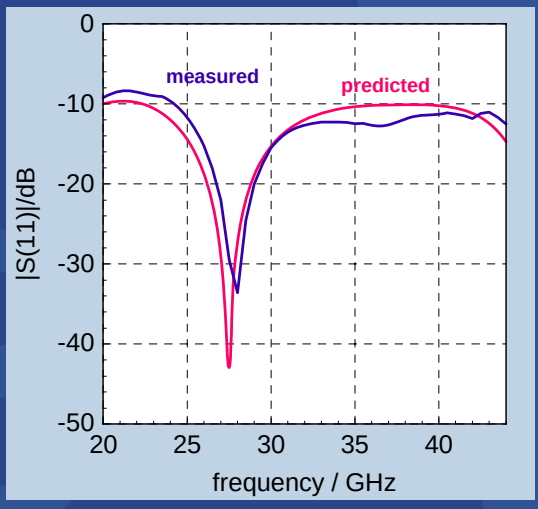
Hot-via: reflection (I)

- back-to-back structure; without compensation



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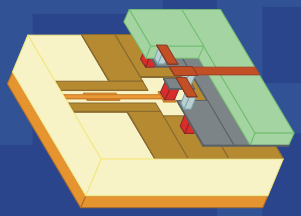
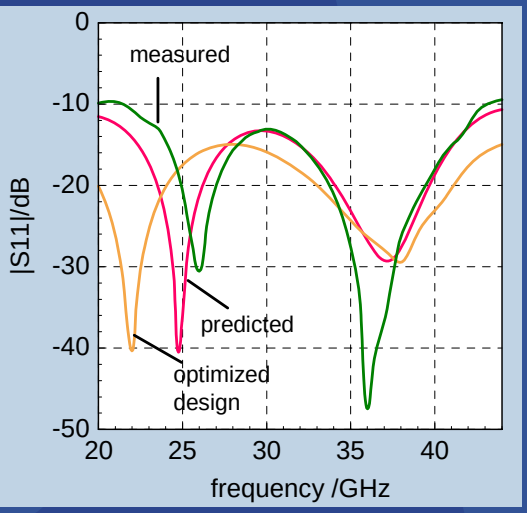
Hot-via: reflection (II)

- Back-to-back structure
- Compensation for 40 GHz
- Potential for frequencies beyond 40 GHz





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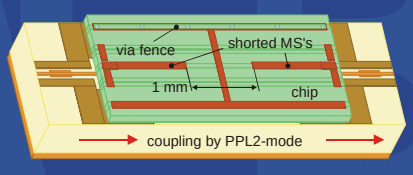
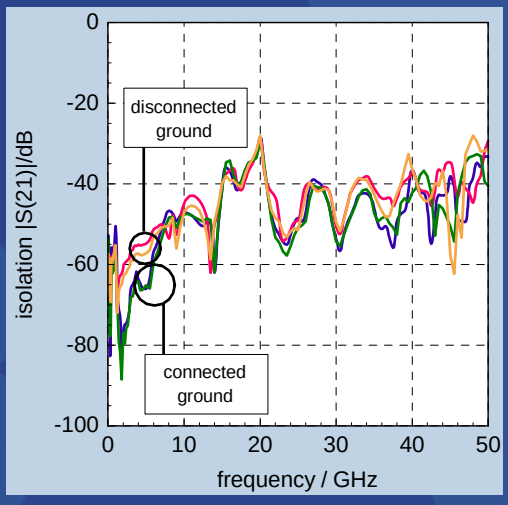
Hot-via: isolation

- Microstrip stubs on chip
- Ground on motherboard connected/non-connected
- Measured transmission below -30 dB up to 50 GHz





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Why thin-film (on carrier)?

Main limitation of frequency / bandwidth potential
of carrier-substrate approaches:

design rules for minimum dimensions
- strip width & spacing
- via diameter & pitch

Scaling
- Conventional ceramics (e.g. 127 µm thick Al_2O_3):
  300 µm diameter vias, 600 µm pitch -> $\lambda/2$ at 80 GHz
- LTCC: 130 µm vias, 400 µm pitch
- Thin-film substrate (e.g. 20 µm thick BCB):
  40...60 µm vias, 100 µm pitch

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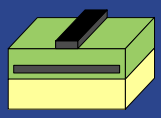
Thin-film & flip-chip

Thin-film microstrip (TFMSL) on carrier

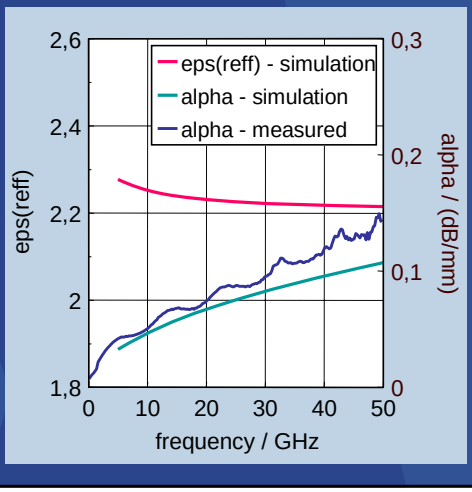
- surface-oriented as CPW
- suppression of parasitic modes (e.g. low-resistivity Si substrate)

Effective permittivity and attenuation vs. frequency (simulated & measured)

- quasi-TEM characteristics
- acceptable loss level



d = 25 µm
w = 64 µm
ε_r = 2.7



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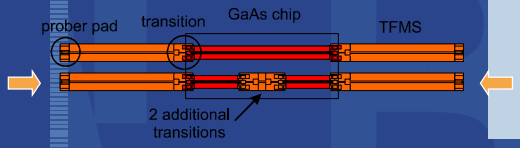
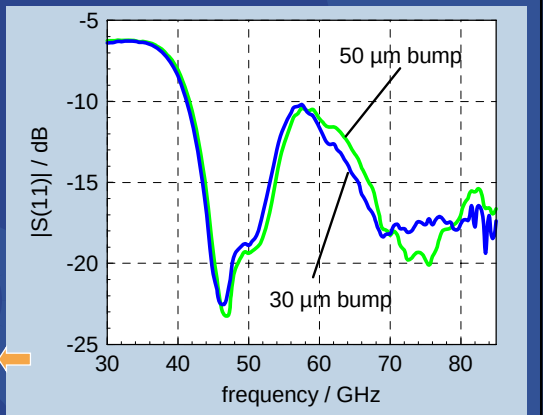
Approach with thin-film carrier for 77 GHz (UMS)

- Compensated flip-chip interconnect (design by 3D em simulation)
- Thin-film carrier (BCB on Si)
- Chips: GaAs, coplanar, bumped chips can be probed
- Measurement results for 4-interconnect structure





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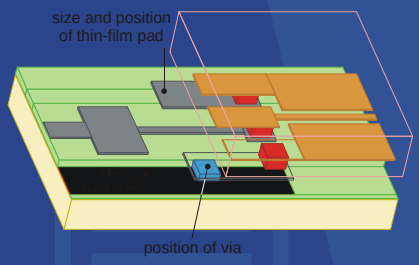
Thin-film & flip-chip: summary

Interesting solution

- feasible up to W band
- good isolation properties (lossy substrate)

To be clarified: CTE mismatch (chip - carrier substrate)



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LTCC as carrier substrate

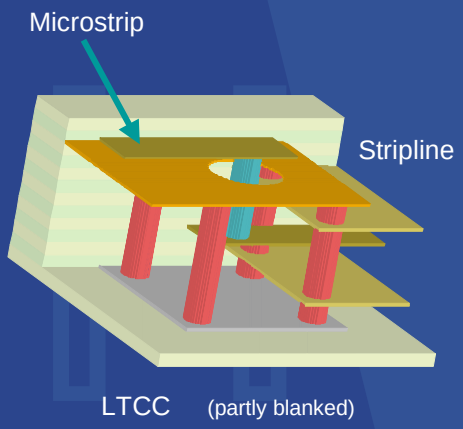
LTCC & thick-film process: cost-efficient solution

Pros

- multi-layer flexibility (line structures, routing, DC)
- low cost

Cons

- thick-film design rules dictate large dimensions (100 µm line width & spacing) -> reduced frequency limits



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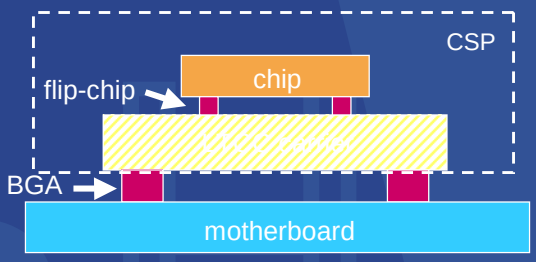
Example for LTCC solution: chip-scale package (CSP)

Approach

- flip-chip mounted coplanar chips
- LTCC intermediate substrate
- connected by BGA

Characteristics

- SMD compatible
- frequency limit: 40...50 GHz



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Conclusions (I)

Flip-chip: clearly excellent potential for mm-waves

Broad-band interconnects up to 80 GHz and more realized

Linked to concepts for carrier substrate

- **thin-film (BCB)**
  - small dimensions
  - frequencies up to W band
- **LTCC**
  - low-cost
  - but frequency limitations (ca. 40 GHz so far)

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Conclusions (II)

Status

- **flip-chip of great interest, but not yet the standard**

Transition to flip-chip requires decisions and additional efforts

- **MCM assembly:**
  - which flip-chip process?
  - which substrate?
  - needs qualification.
- **Chip designer**
  - GaAs: coplanar MMICs?
  - Si: thin-film microstrip is compatible!
- **foundries: provide bumped chips?**


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Conclusions (III)
Flip-chip is gaining ground !