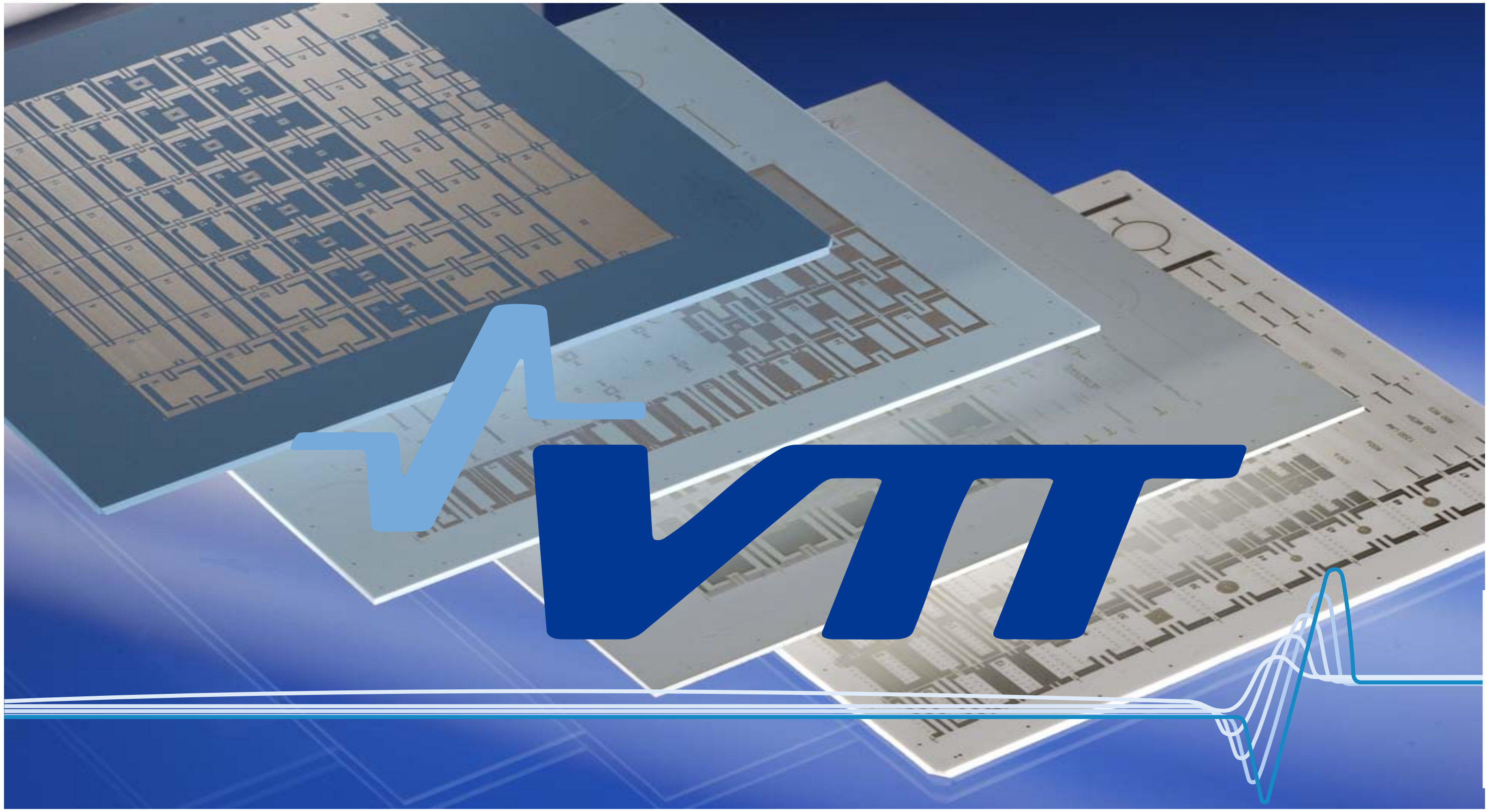


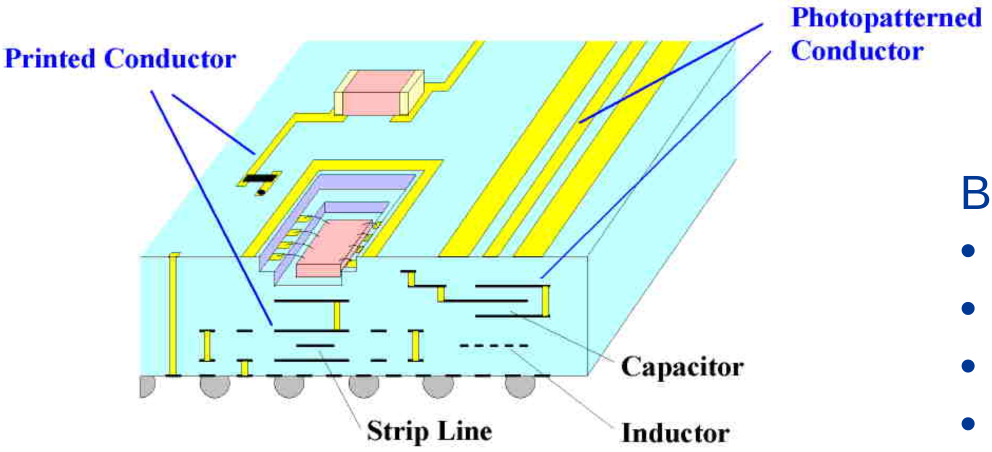
LTCC Packaging & Smart System Integration
Horten 19.9.2008

Kari Kautio

OUTLINE

- LTCC technology - processing and materials
- Thermal management
- Bare die assembly & sealing
- Application areas & demonstrators
- Fabrication of 3D- structures on LTCC
- Packaging projects

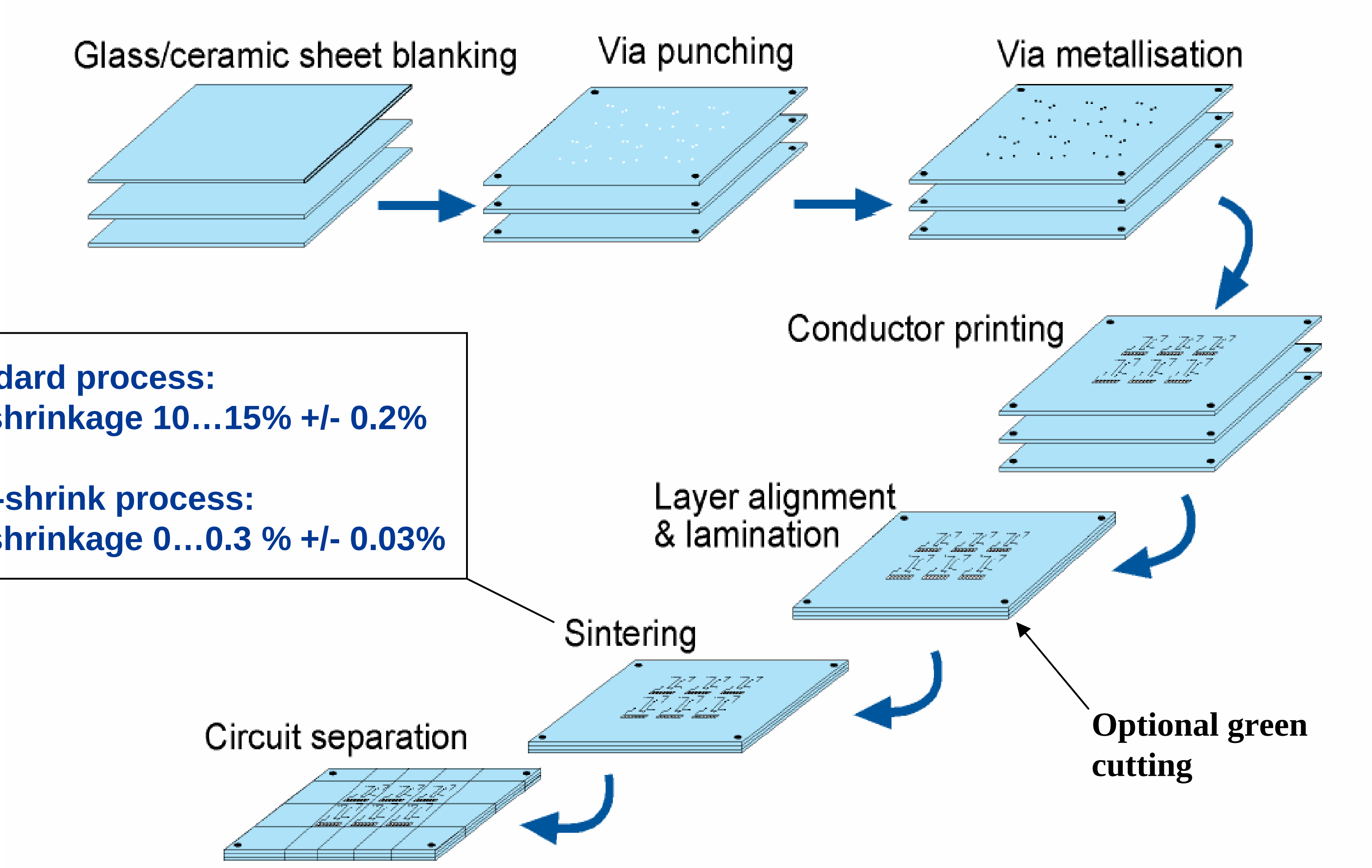
LTCC
Low Temperature Co-fired Ceramics



BENEFITS :
- high density, fine- line
- Good high frequency properties
- radiation / crosstalk management
- reliability & stability
- 3D - capability

APPLICATION AREAS:
- telecom & wireless
- automotive
- sensor & opto packaging
- medical
- high speed signal processing
- military & space

Low temperature cofired ceramics (LTCC) Process Flow



Standard process:
X,Y shrinkage 10…15% +/- 0.2%

Zero-shrink process:
X,Y shrinkage 0…0.3 % +/- 0.03%

LTCC Material Systems

- Several manufacturers: Du Pont , Heraeus, Ferro, CeramTec, NEC…
- LTCC tape is glass which is cast with organic additives on a polyester backing

- Different tape thicknesses can be used in the same substrate

- Metallization pastes for vias and conductors are matched to each tape

- Pure silver (Ag) is the mainly used low cost, high conductivity metallisation (Rs= 1…3 mohm/square, surface roughness Ra= 0.6μm)

- Ag/Pd or Ag/Pt is used for solderable conductors (Rs=20mohm/sq.)

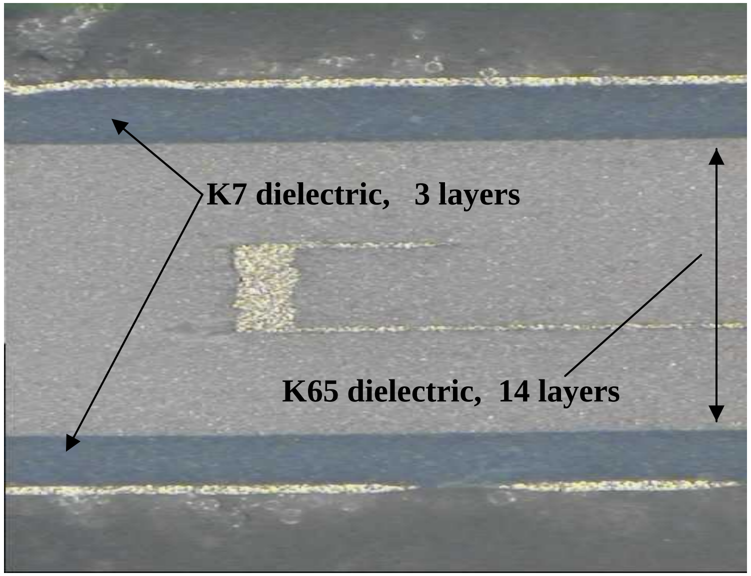
- Au conductors are used for bondable conductors (Rs= 5mohm/sq.)

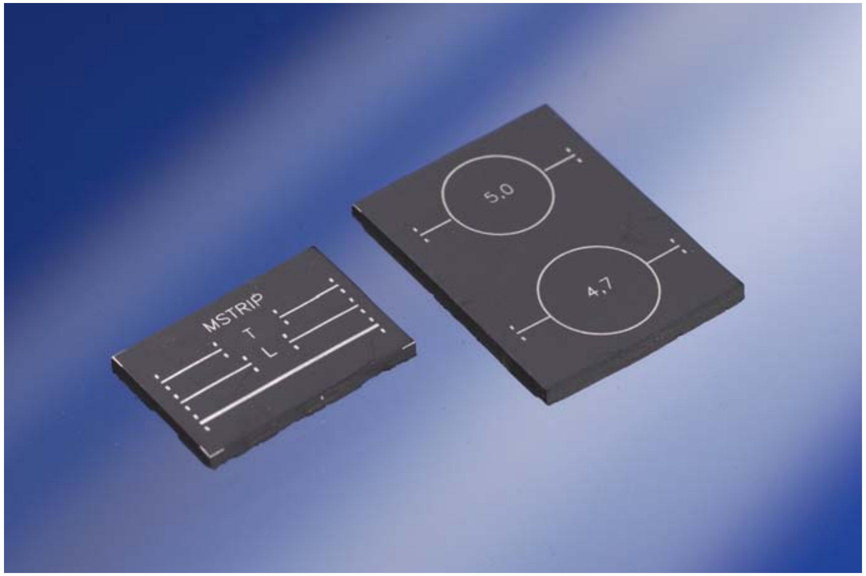
LTCC Tape Systems

TAPE	Fired thickness [µm]	Permittivity Er	Tan δ [%]	TCE [ppm/K]
Ferro A6M	**100, 200**	**5. 9**	**0.12 (2.5 GHz)**	**>8**
DuPont 951	**40, 90, 130, 200**	**7.8**	**0.15 (10 MHz)**	**5.8**
DuPont 943	**105**	**7. 4 (40GHz)**	**0.2 (40 GHz)**	**6.0**
Heraeus CT2000	**77**	**9.1**	**0.2 (2 GHz)**	**8.5**
Heraeus HL2000	**89**	**7.4**	**0.26 (2.5 GHz)**	**6.1**
Heraeus CT 800	**-**	**8.4**	**0.18 (1 kHz)**	**8.4**
Heraeus CT707	**105**	**6.4**	**0.46 (2.5 GHz)**	**8.1**
Heraeus CT765	**84**	**65**	**0.17 (2.5 GHz)**	**9.1**
Heraeus CT702	**-**	**5. 3 (30GHz)**	**<0. 2 (30 GHZ)**	**-**
Heraeus CT703	**-**	**7.0 (30GHz)**	**<0. 2 (30GHZ)**	**-**

Thermal conductivity 2…4 W/mK for all LTCC materials

Characterisation of novel LTCC materials for μ- wave and millimeter-wave frequencies



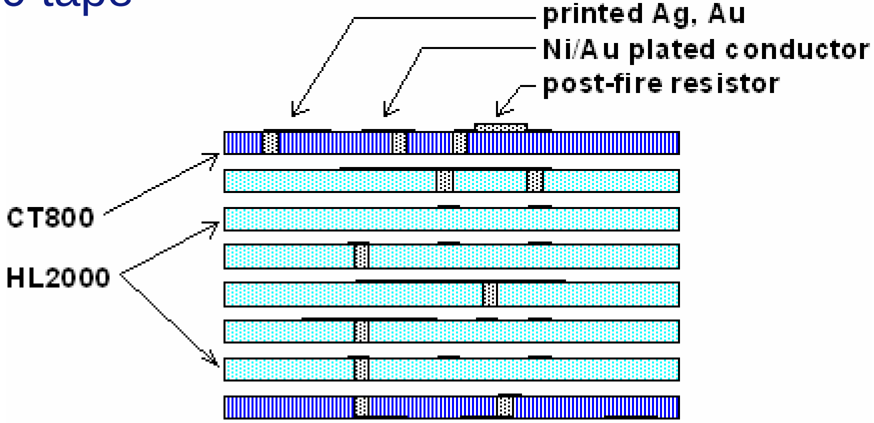


Mixed K LTCC resonator
Q=150 (2 GHz)

Characterisation of Ferrite LTCC

Heralock self-constraining tape system
(” Zero- Shrink ”)

Heralock clad substrate uses CT800 tape outer layers



+ X,Y shrinkage only 0.3%

+ Shrinkage tolerance 0.03% enables fine- pitch component assembly

+ Excellent substrate flatness

+ Clad system enables Ni/Au plating (reliability of interconnections)

- Cavities are difficult to make

- Number of tape layers limited to 8 - 10

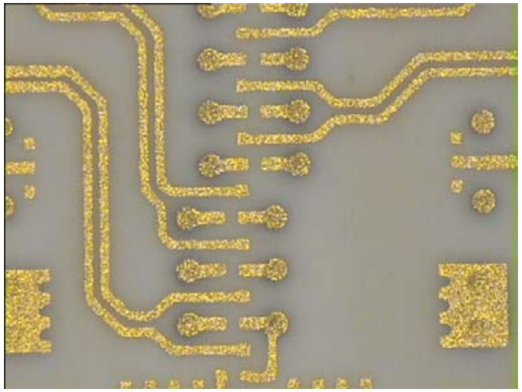
LTCC design limits

FEATURE	Production State-of-the art	Special applications
Number of tape layers	>20	>20
Substrate max. thickness	4mm	>4mm
Printed conductor line width / spacing	50 µm / 70 µm	40µm / 60 µm
photo-patterned line width / spacing	40µm / 50 µm	40µm / 50 µm
Via diameter	80 µm… 200 µm	50 µm
via pitch	2.5 x via diameter	2 x via diameter
layer alignment tolerance	15 µm	10 µm
shrinkage tolerances (x , y)	typical +/- 0.1%	0.03% (zero shrink)
Thickness tolerance (z)	typical +/- 2%	typical +/- 2%

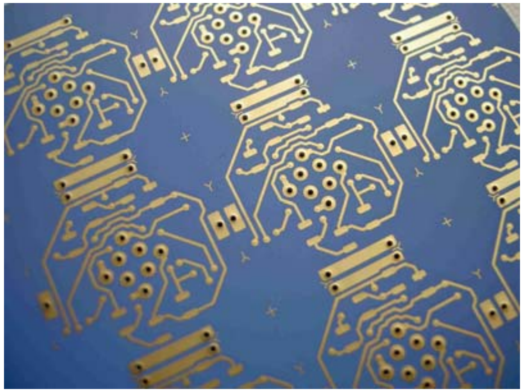
General design guidelines on VTT web pages

LTCC Patterning

- Screen printing is the main fabrication method
  - co-fireable conductors, resistors and overglaze
  - post-fireable conductors printed on fired substrate
- Photoimageable thick film pastes
  - limited to special applications (higher cost)
  - co-fired Ag, post-fired Ag, Au, glass
  - HF- properties comparable to printed conductors
- Etching of post-fired thick film or thin film metallization
  - 25 μm line and space is feasible.
  - limited to special applications (higher cost)
- Electroless Ni/Au plating of thick film conductor
  - Improved wire bond and solder joint reliability
  - Requires a plateable Ag paste



Printed line width 50μm, via 80μm



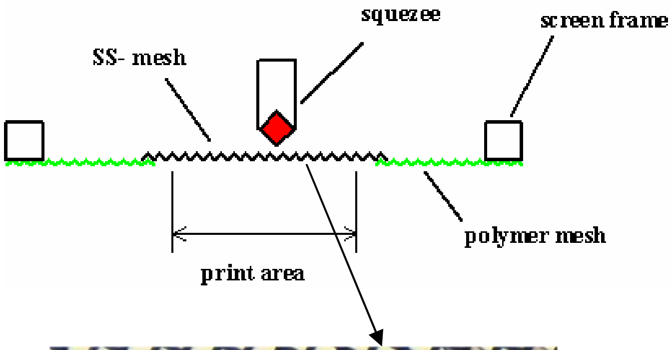
Ni/Au plating on LTCC

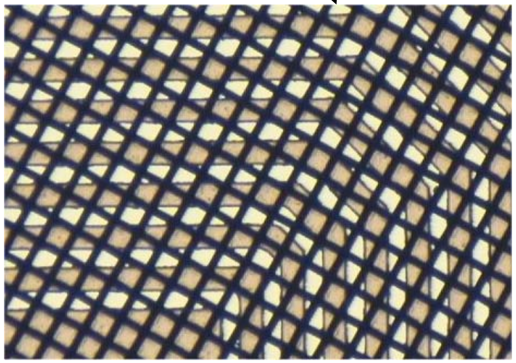
Fine-line screen printing

Typically minimum line width and spacing is >100 µm in volume production

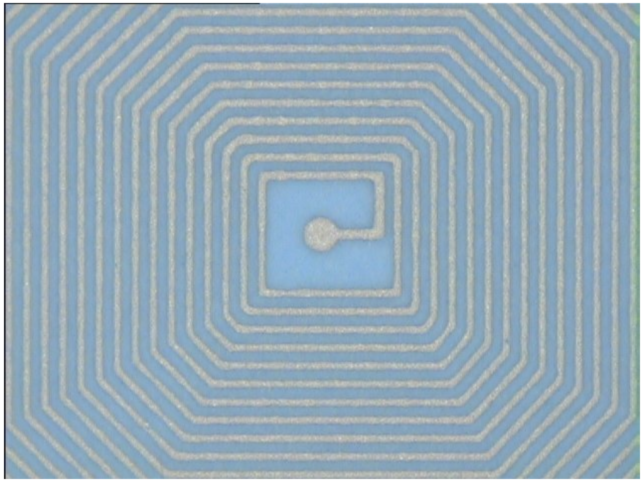
Fine-line screen printing (50...70µm) is possible in LTCC production using:

- advanced screen technology
- fine-line ink (only a few types are available)
- optimized layout design
- careful process control (cleanliness etc.)



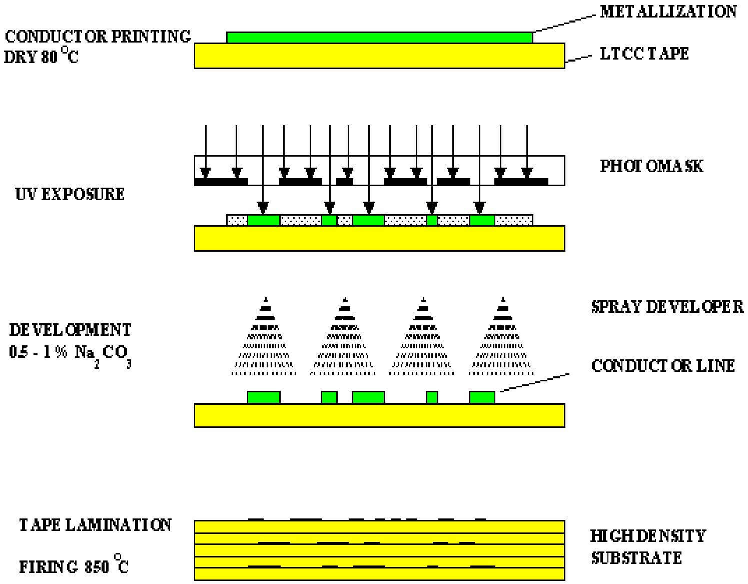


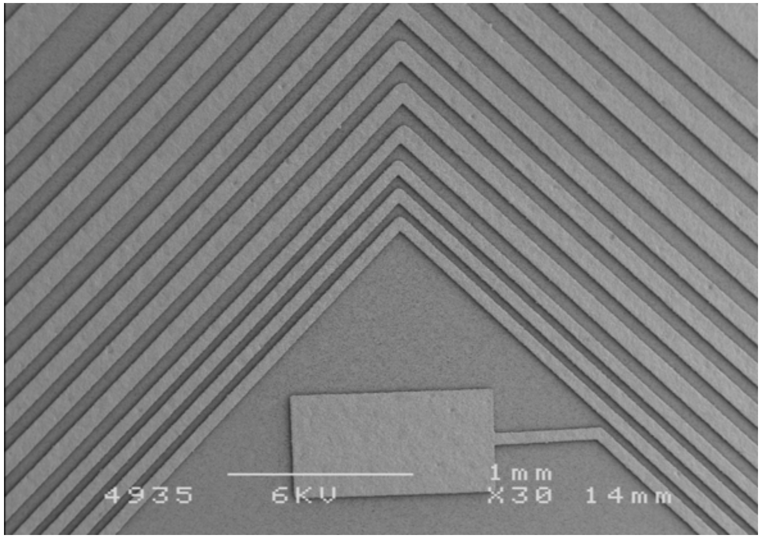
Trampoline Screen
mesh 500, 15 µm wire



Printed inductor 35 µm line / 55 µm space

Photoimaged conductors

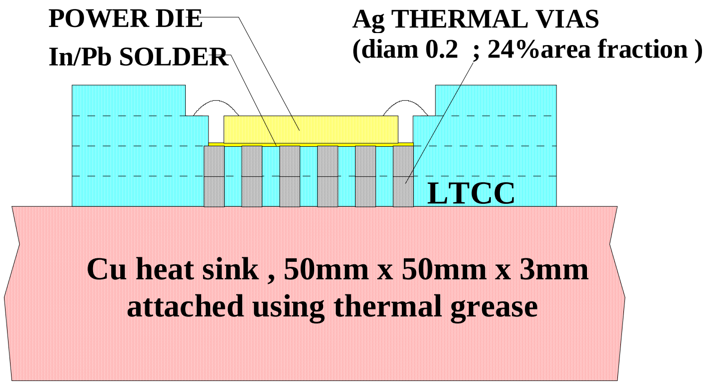


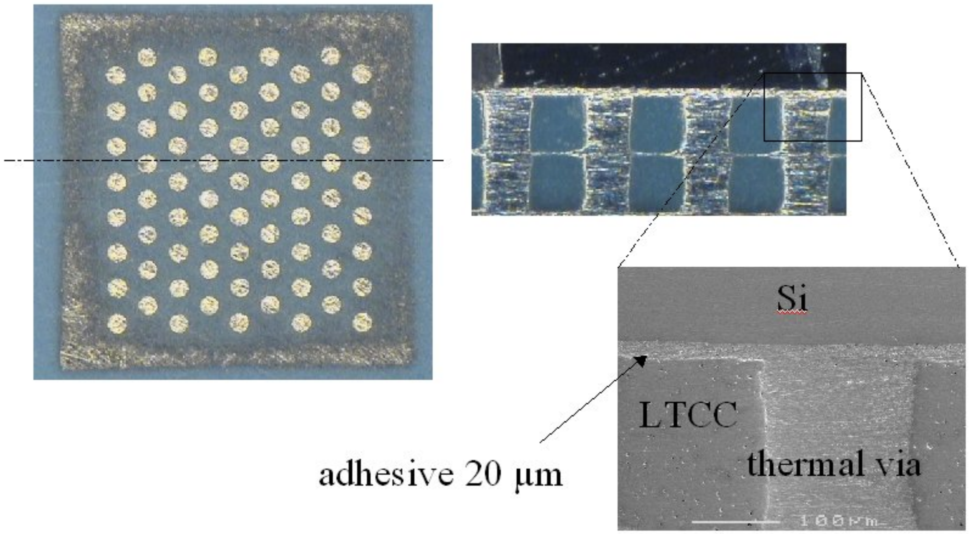


- Minimum line width 40 µm, minimum space 50 µm
- Improved edge resolution
- Line width tolerance: +/- 2 µm (with high quality exposure mask)
- Complicated process compared to screen printing

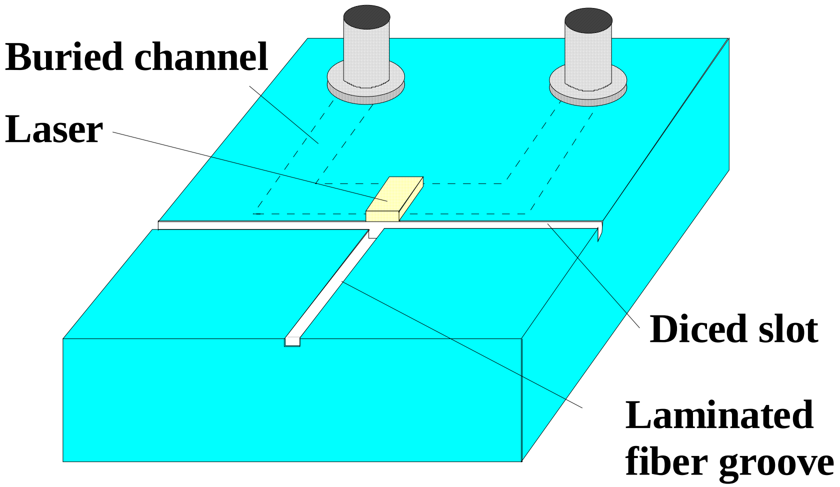
Thermal Management
Thermal vias

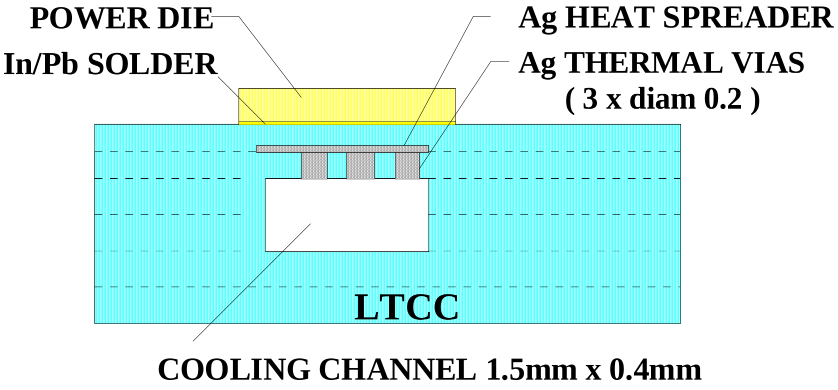
- LTCC dielectric thermal conductivity is 3…5 W/mK (FR-4: 0.2W/mK)
- Ag via thermal conductivity is typically 300 W/mK
- 24 % area fraction of vias can be readily achieved
- thermal resistance reduced by 1/20

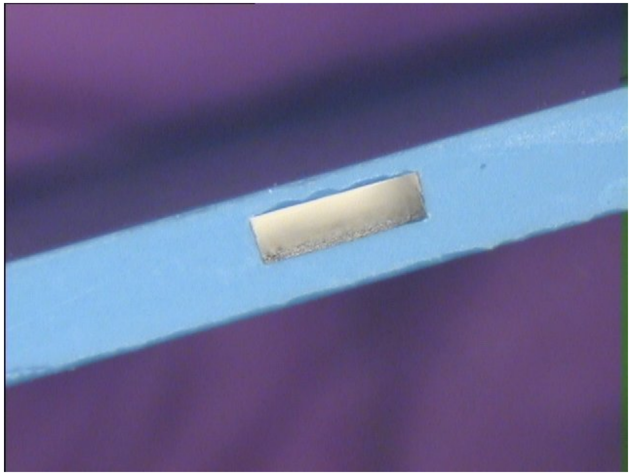




Thermal Management water cooling



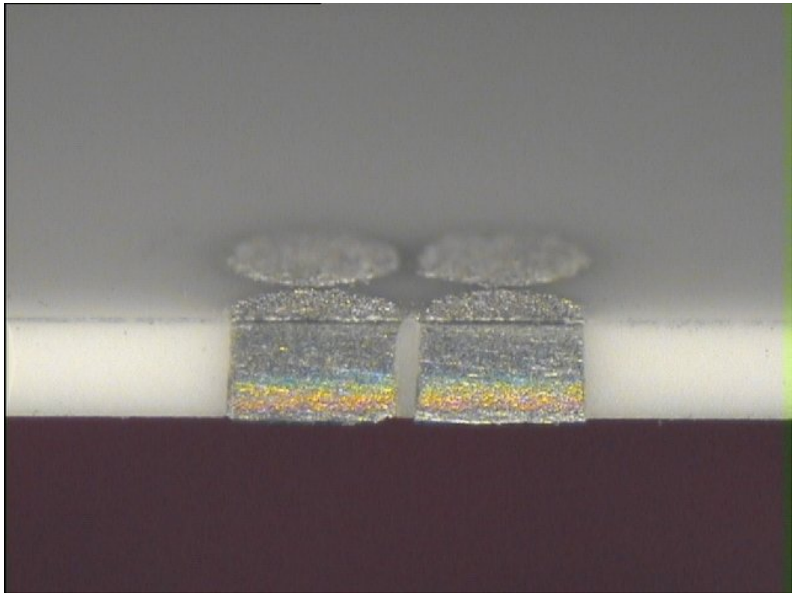




- Efficient cooling method
- Difficult to arrange pumping for portable equipment

Thermal Management
Thermal plug

Up to diameter 0.9mm hole can be filled with thermal plug paste
- Firing at 850^{o}C
- Suitable for alumina and LTCC



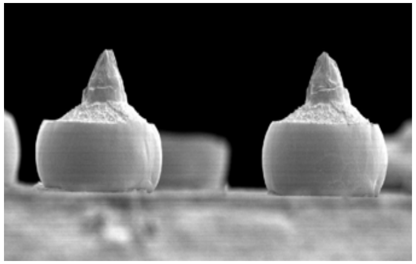
Cross-section of diam. 0.9mm Ag plugs for LED array

Chip assembly on LTCC

FLIP-CHIP

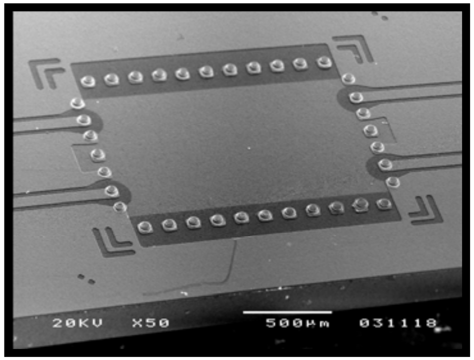
Solder bump on the chip side is recommended, if available

- Au metallization on LTCC for Au/Sn or bumps (without flux)
- Ag/Pd metallization on LTCC for Pb/Sn bumps (with flux)



Gold stud bumps for prototyping

- Bumps can be made on the chip (>3mmx3mm) or on the LTCC
- Typical bump diameter 75 µm (25 µm wire), height 30 µm
- joining by thermocompression, ultrasonics or adhesive



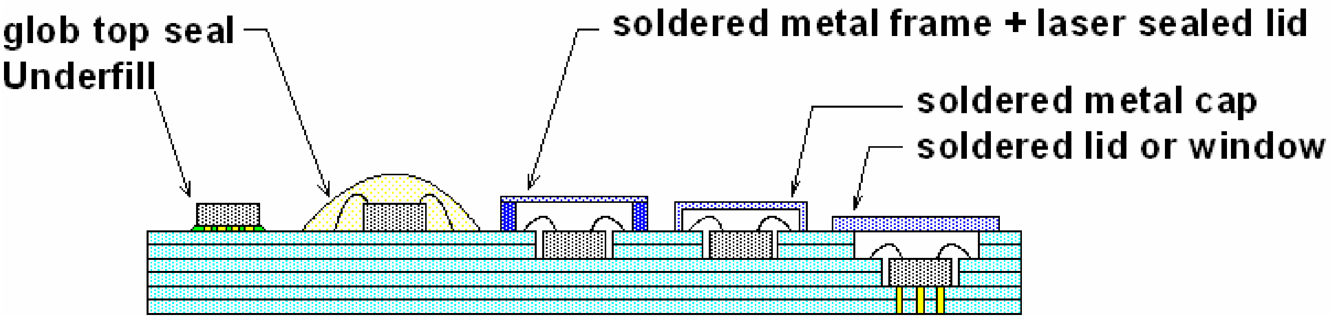
Stud-bumped substrate

CHIP&WIRE

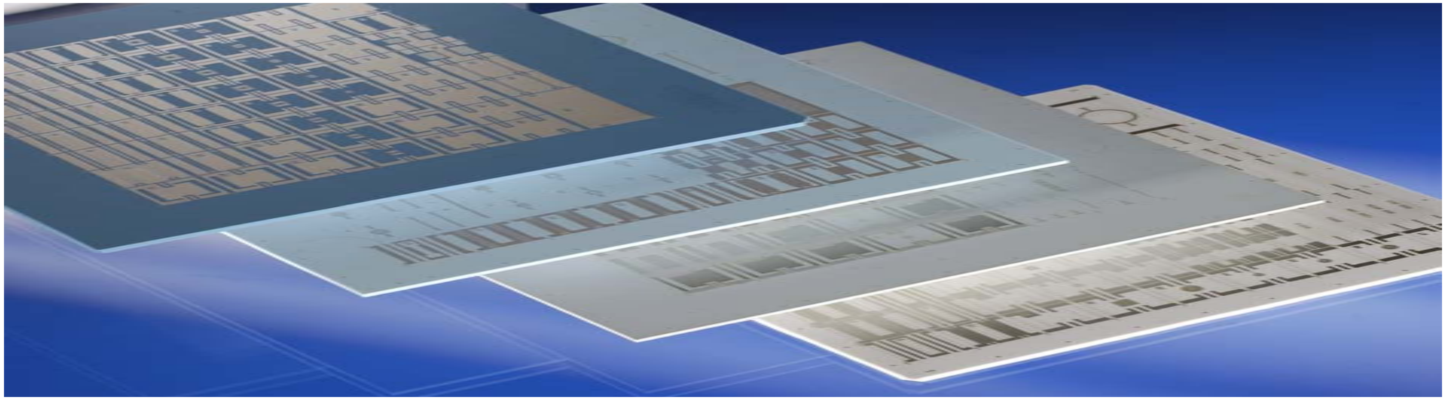
- A well proven and reliable technology on thick film and LTCC
- The chip is usually die bonded using conductive or non-conductive epoxy
- Thin gold or aluminium wire (typically 25µm) is used
- Alternatively Au ribbon for MMIC’s

LTCC
Sealing & hermeticity

- LTCC substrate itself is hermetic, stable and reliable
- Local hermetic sealing (Au/Sn solder) is possible
- Non-hermetic glob-top sealing
- Under fill support for flip-chip components
  - due to small TCE mismatch, underfill is often not needed

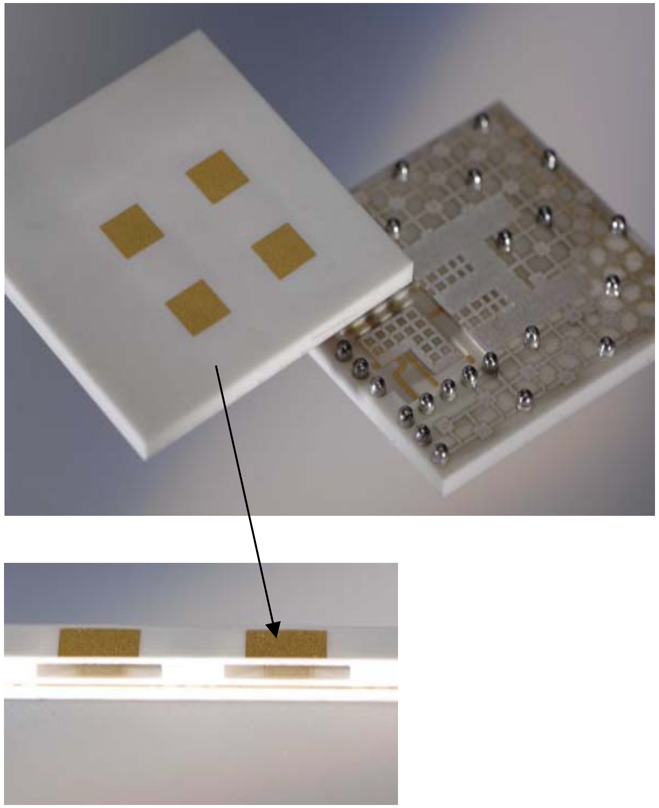


Why LTCC in RF- and Microwave Applications

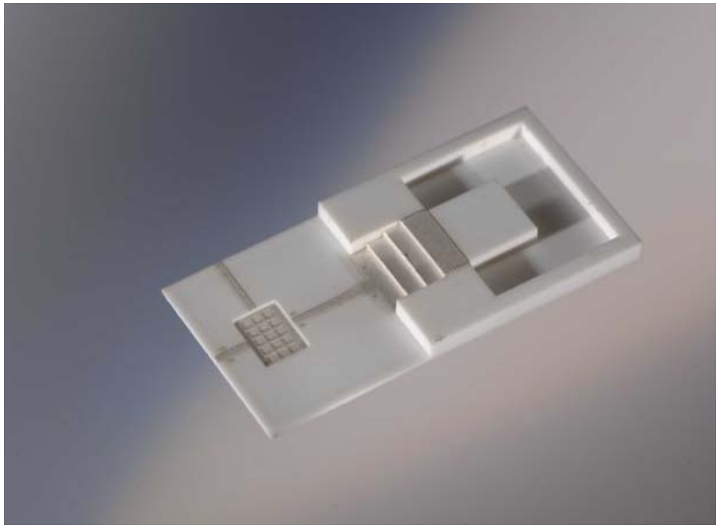


- Low loss materials up to 100 GHz
- Controlled impedance (3-D design, precise geometry)
- Low Tf (Temperature coefficient of resonant frequency)
- Radiation / crosstalk management
- Integrated passive components
  - inductors **-> 200 nH/layer (+/- 5%)**
  - capacitors **-> 10 pF (+/- 5%)**
  - resistors **-> 10 Ω - 10 MΩ, buried +/- 30%, surface +/- 1%**
  - filters, antennas, resonators

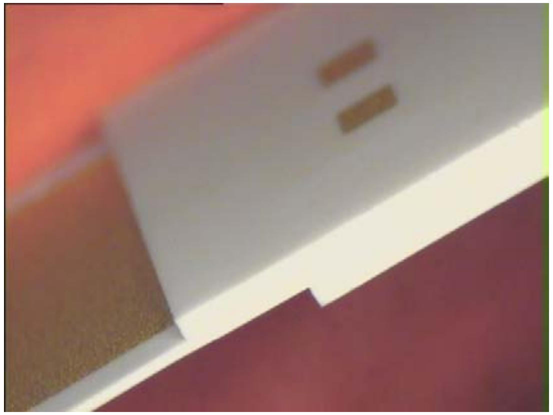
LTCC
Antenna demonstrators



Patch antenna array with air cavity
Communications Research Centre, Canada



24GHz dielectric resonator
Carleton University, Canada

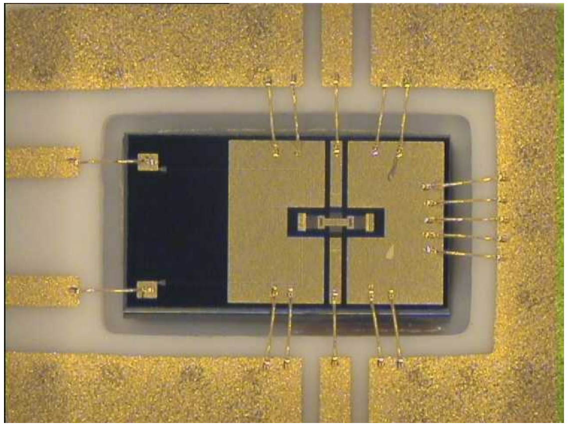


Patch antenna array (60GHz)

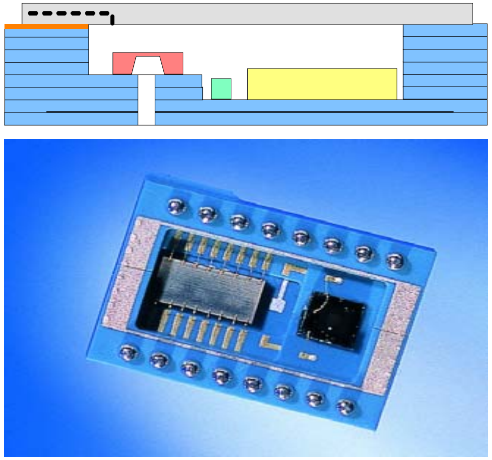
LTCC
MEMS packaging

LTCC technology meets the technical requirements for MEMS packaging

- Good high frequency properties
- Reliability (good TCE match to Si, stability, hermeticity)
- 3D microstructures, fluidistics

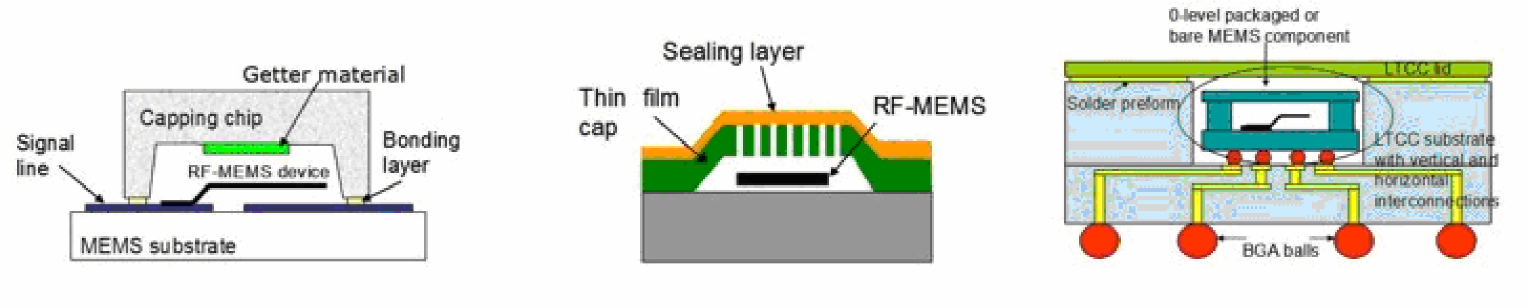


MEMS switch in LTCC package



Pressure transmitter

MEMSPACK- project
Zero- and First level Packaging of RF- MEMS



0-level "chip capping" with horizontal feedthroughs

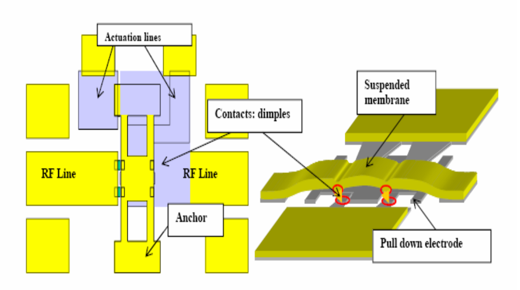
0-level "thin film capping"

1-level package based on LTCC

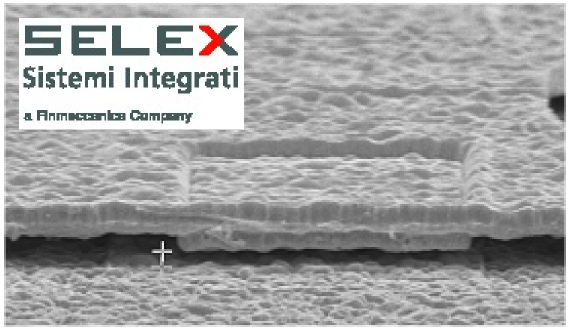
Packaging concepts for RF-MEMS

Critical packaging issues for RF- MEMS
- good RF- behaviour
- reliability
- low cost

TEMPO- project
Technologies for the Miniaturisation and the Packaging of True Time Delay Modules



Thin-film RF-MEMS switches on LTCC platform were successfully demonstrated



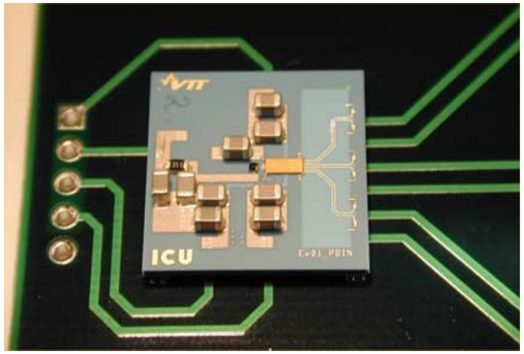
LTCC is readily suitable for high frequency but surface quality is not good enough for the most demanding thin-film post-processing, such as RF- MEMS

Polishing of LTCC was developed to obtain the required criteria:

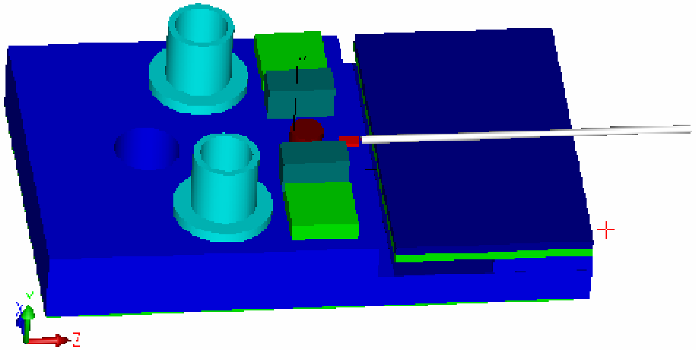
- LTCC as-fired roughness Rq= 600nm reduced to Rq = 14 nm
- Pore size: < 1 μm^2
- Pore depth: Rt < 200 nm
- Pore count: <30 pcs / mm^2

LTCC in photonic packaging

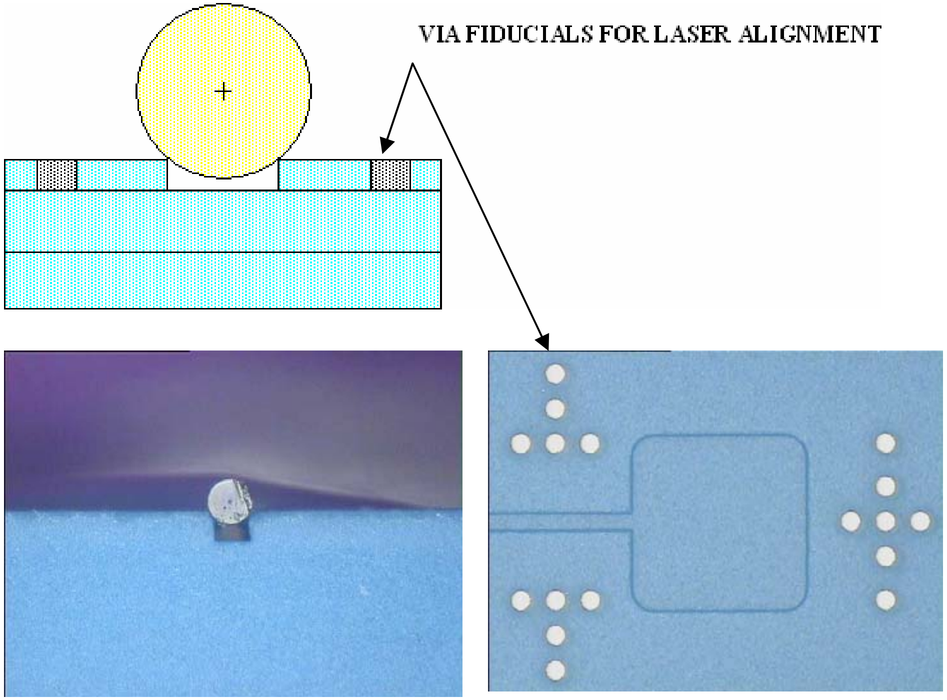
- High packaging density, integration of high speed/low noise/high-power electronics close to photonic devices
- Accurate 3D structures - passive alignment of photonic devices and fibres (cavities, grooves, holes, channels)
- Stable and hermetic substrate material
- Good power handling capability
- Hermetic sealing - eliminates expensive metal package
- Cost effective

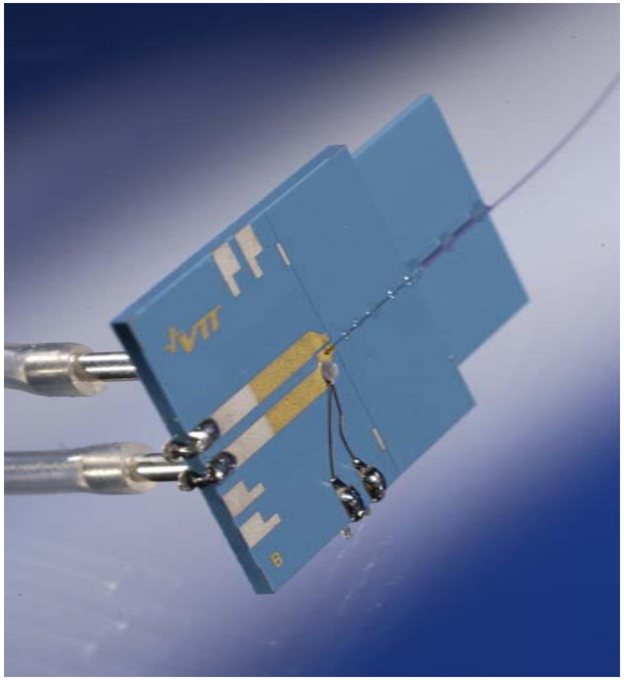


High-speed photo-detector array



Optical fibre passive alignment
Punched & laminated fiber groove



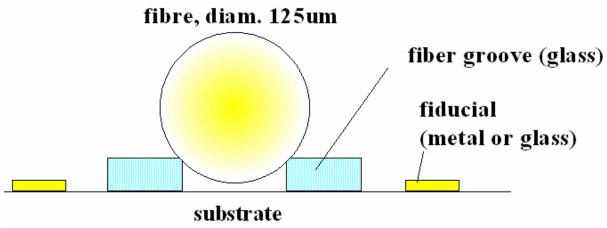


Laser transmitter demonstrator

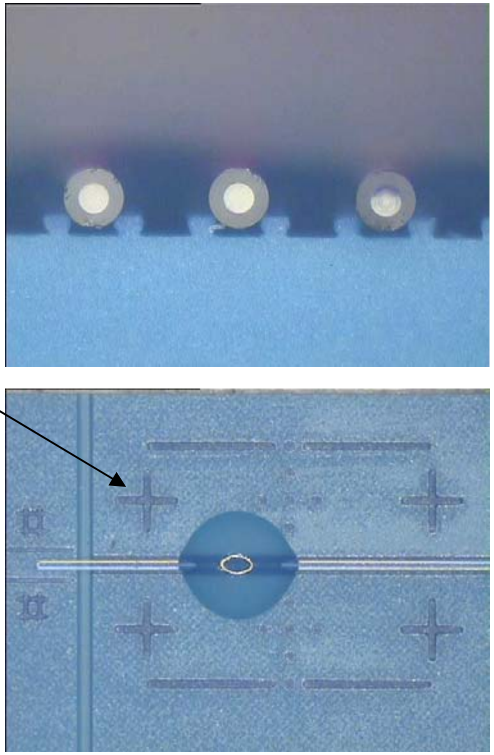
- Fibre groove nibbled to tape sheet with 150 μm round pin
- Lamination with low pressure
- Ag filled vias are used for laser die alignment

Optical fibre passive alignment
Photoimaged fiber groove and alignment marks

Process:
- FODEL Photoimaged glass print- dry-print-dry, up to six layers
- UV- exposure through photo mask
- Spray development
- Firing 850 °C



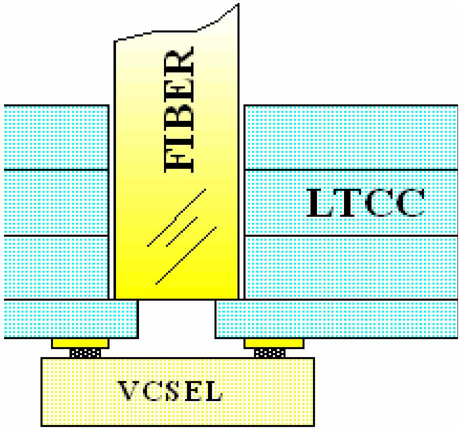
Precise alignment fiducials for the laser die alignment

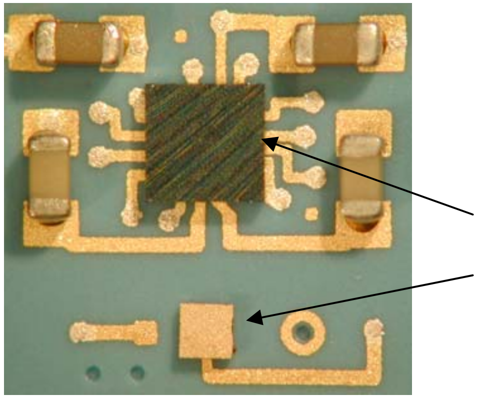


Optical fibre passive alignment
Passive alignment to VCSEL laser or receiver diode

Passive alignment of a 62.5/125µm multimode fibre to a VCSEL laser by the use of punched through hole in the LTCC substrate.

Hole diameter tolerance +/- 2 µm

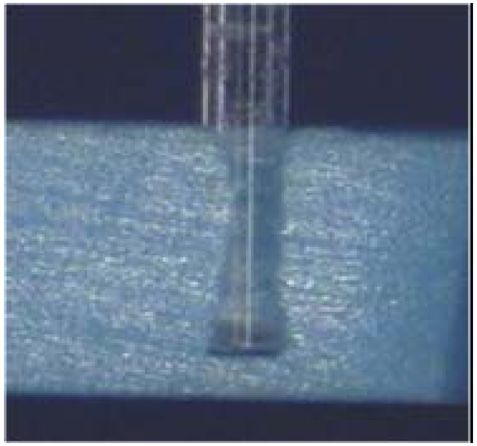




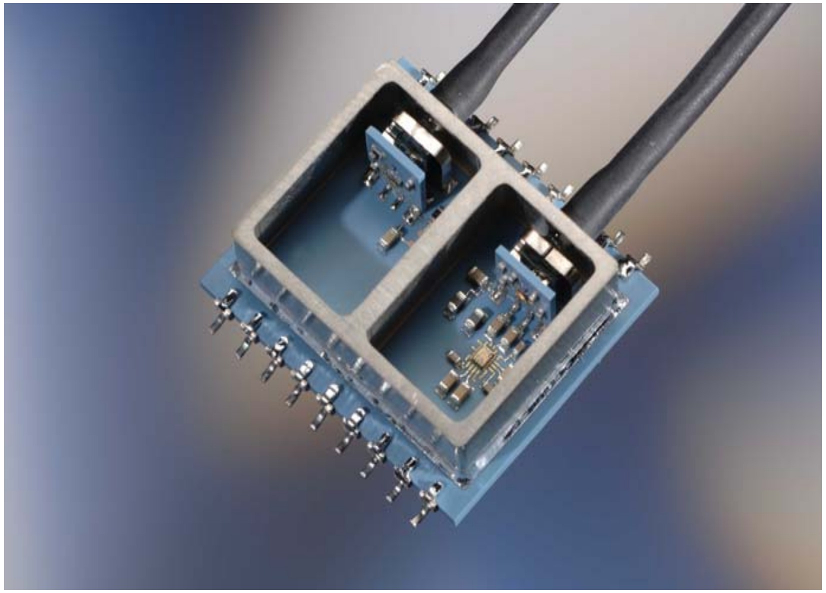
VCSEL driver

VCSEL

VCSEL transmitter

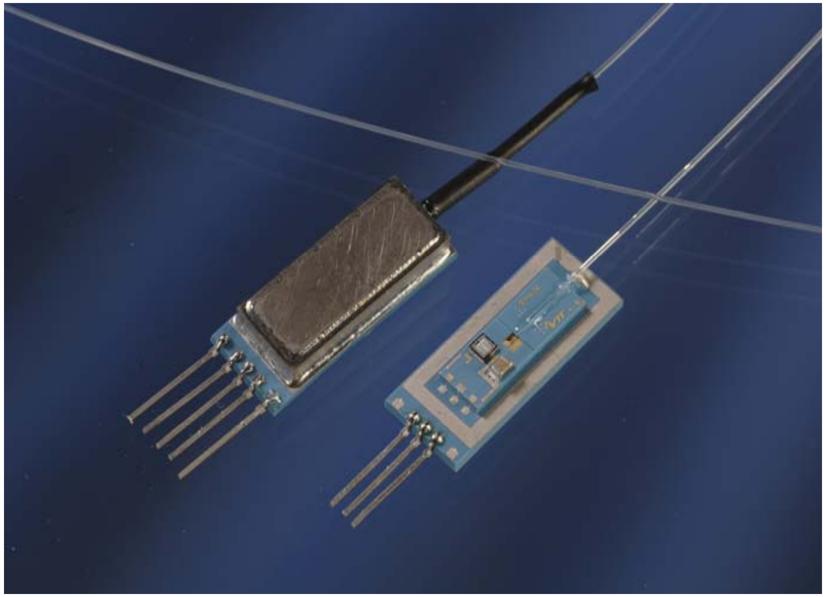


Fibre Optic Data Link Modules



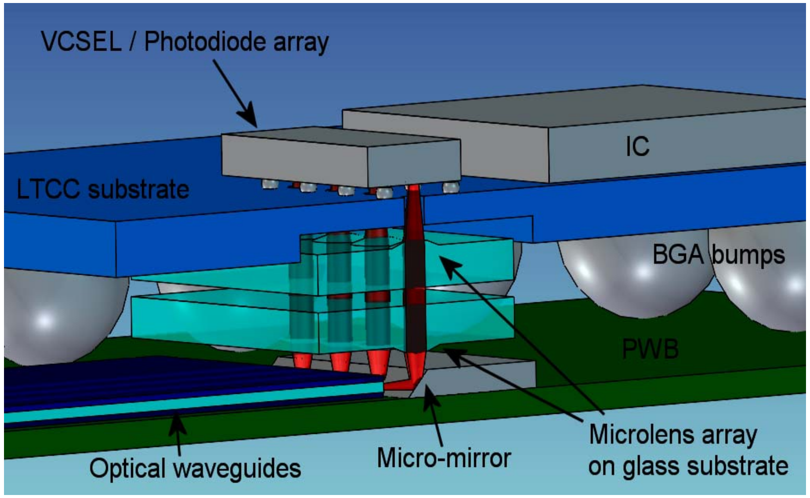
ESA ARTES-5

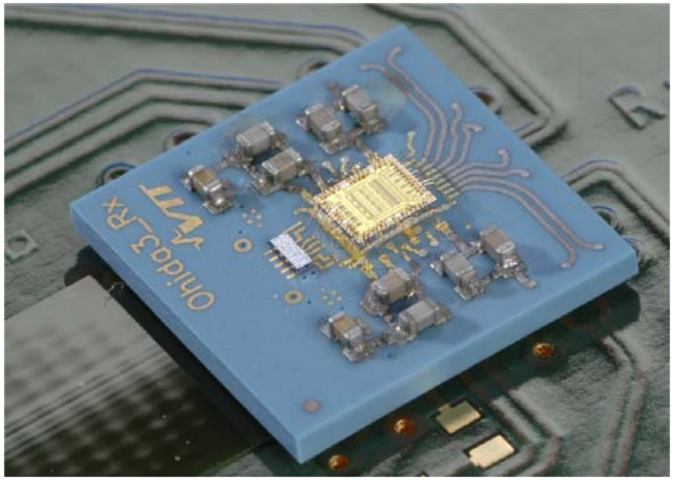
Intra-satellite 10Gbps fibre-optic data transceiver



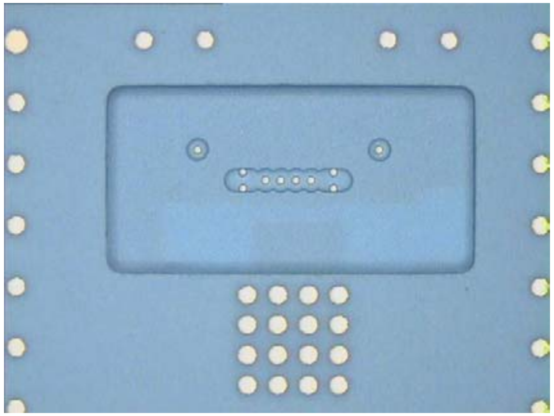
Hermetic fibre pigtailed laser module with fibre passive alignment

4x 10 Gb/s Optical Coupling Demonstrator

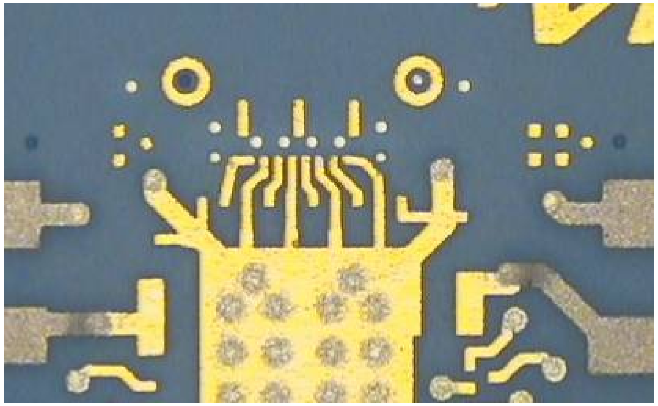




LTCC receiver



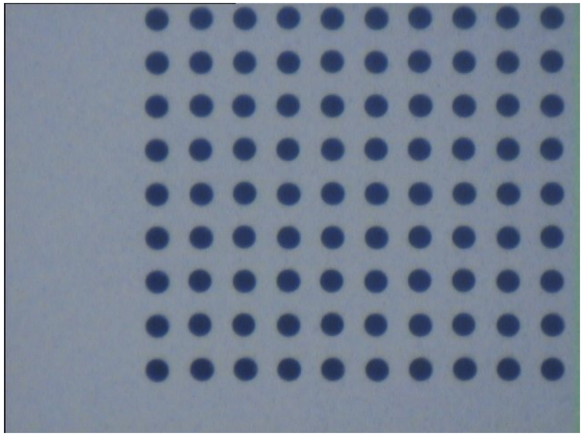
Cavity for microlens array with
’optical vias’ and alignment marks



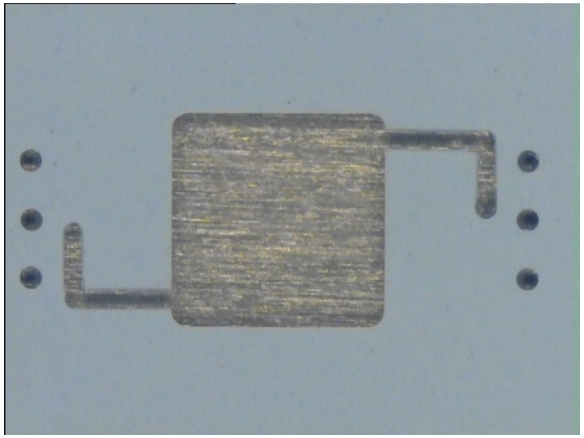
’optical vias’ and flip-chip pads

Fabrication of 3D LTCC Structures

Mechanical punching is the most common technique for LTCC tape structuring



Punched 80 µm vias on 160 µm pitch



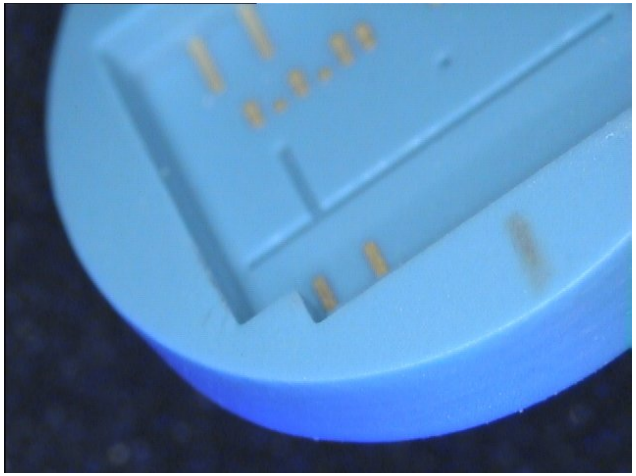
150 µm channels and cavity window nibbled to tape sheet

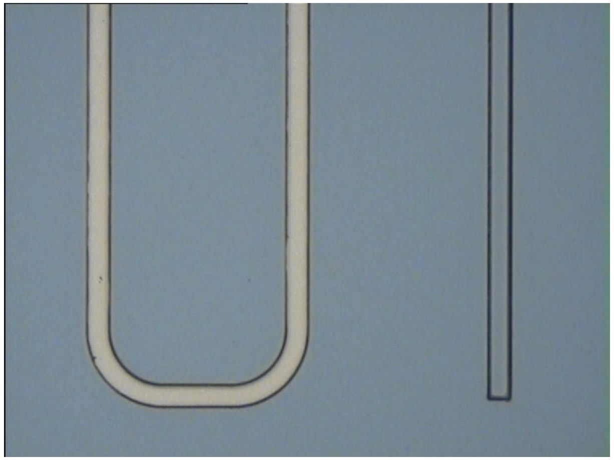
- Hundreds of holes per second can be punched using customised matrix tooling
- Punching method gives the best hole quality
- Holes can be punched through several laminated layers also
- Different punch tool geometries are available

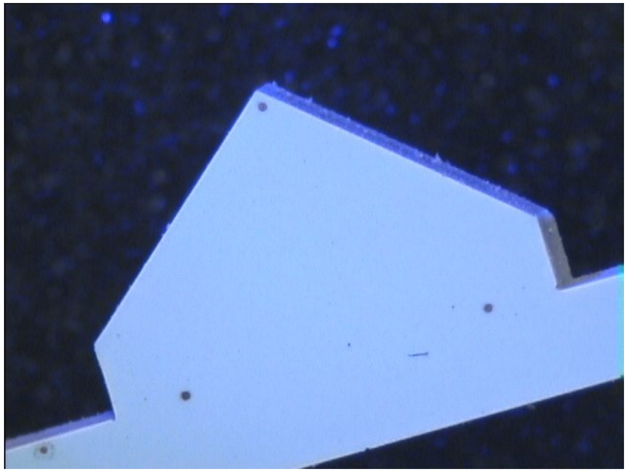
Laser Structuring of LTCC tape or laminate

Laser structuring of laminate and tape is fast in the un-fired state

- Narrow (<150µm) channels
- Complex shapes
- Laser cut edge is slightly inclined (beam shape)

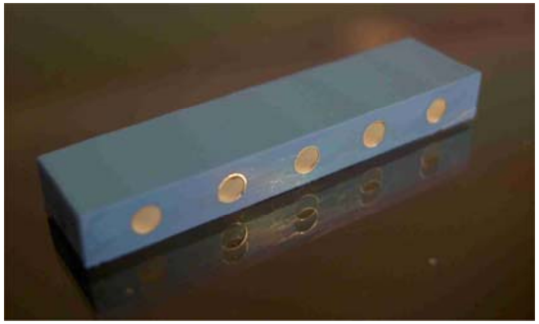






CNC machining of LTCC

- Accurate holes can be drilled to very thick laminates (un-fired)
- Wear of the hard-metal drill bit due to abrasive ceramic binder
- Final hole size tolerance (after firing) mainly depends on drill tool tolerances
- Hole placement tolerance depends on drilling accuracy and LTCC firing shrinkage tolerance (typically 0.1-0.2%)



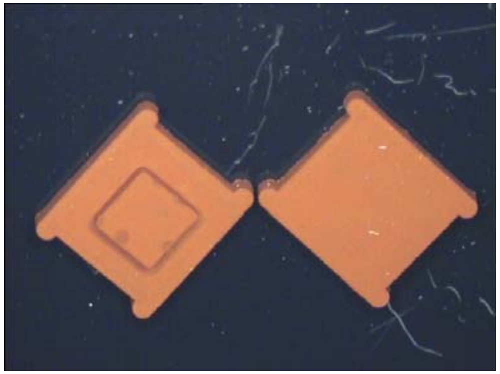
Drilled 2mm holes, metallised

- Accurate holes can be CNC- machined to fired substrates using diamond tooling
- Minimum hole diameter is typically 2.5mm on <50x50mm LTCC part
- Hole diameter can be controlled to **+/- 5µm tolerance**
- Hole-to hole distance can be controlled to **+/- 15µm tolerance**

Fabrication of surface cavities

Molded silicone inserts support the cavity structure during lamination (removed after lamination)

Typical cavity tolerance is +/- 50μm



Small inserts difficult to handle -> Insert mat can be used for lamination

Fabrication of buried cavities and channels
Lamination methods

Method 1: Lamination at very low pressure

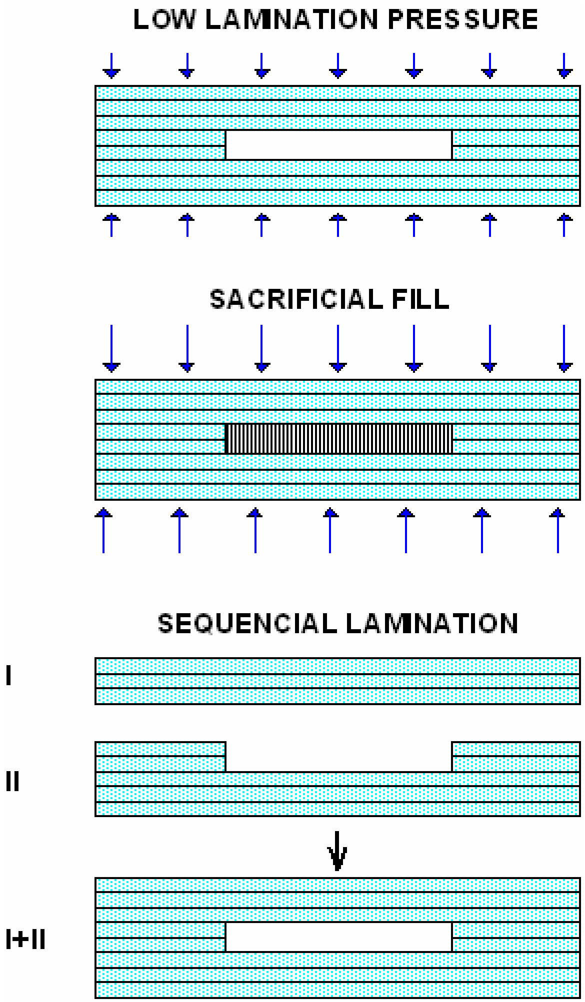
- tape layer delamination may happen
- channel width limited to about 0.5 mm
- substrate sagging problems

Method 2: Lamination with sacrificial filler

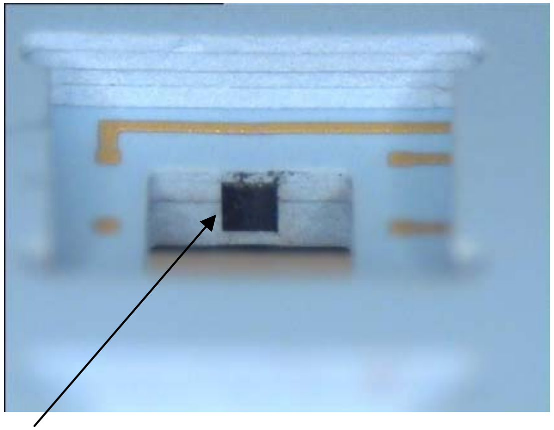
- sacrificial material supports the structure in lamination and burns off during substrate co-firing process
- possible sacrificial materials:carbon, wax…
- substrate cracking can be a problem

Method 3: Lamination in several steps

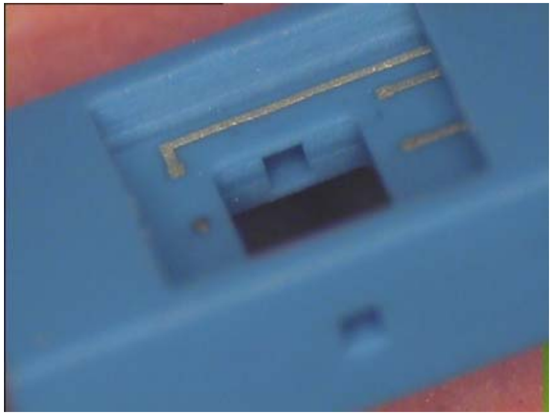
- Standard lamination for separate sub-laminates
- Final ”cold lamination” step = gluing of parts together with a glue that burns off during co-firing



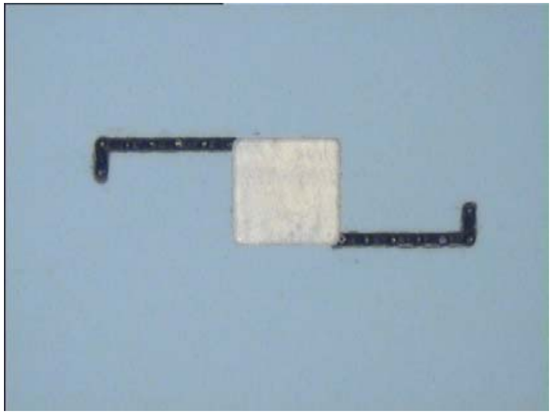
Fabrication of buried cavities and channels
Sacrificial carbon



Carbon insert 0.4 x 0.41 x 2.3 mm

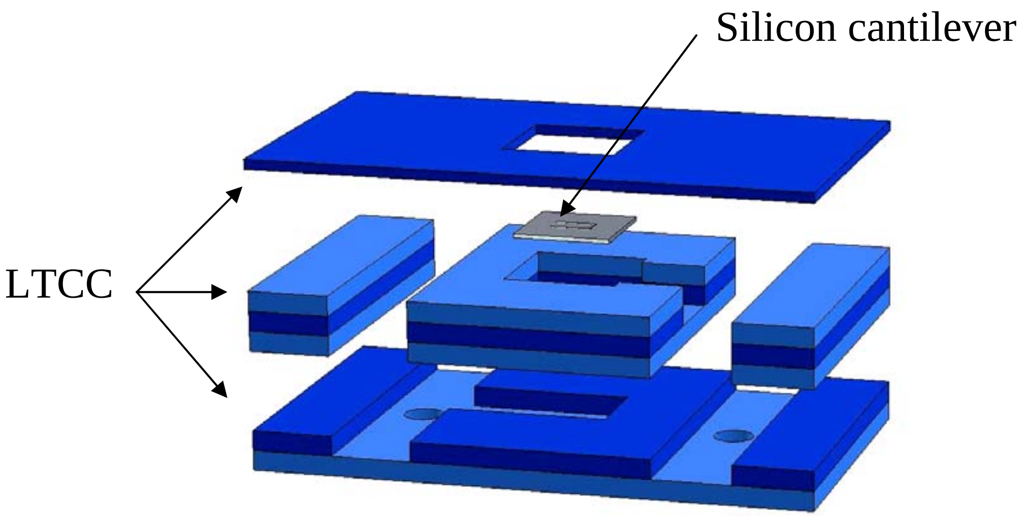


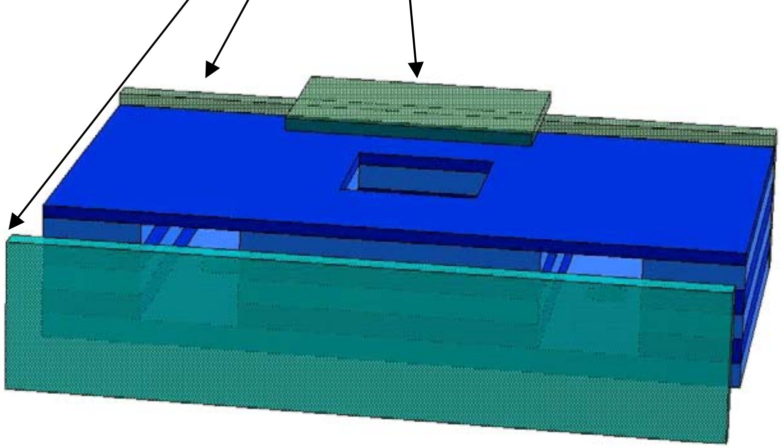
Co-fired cavity

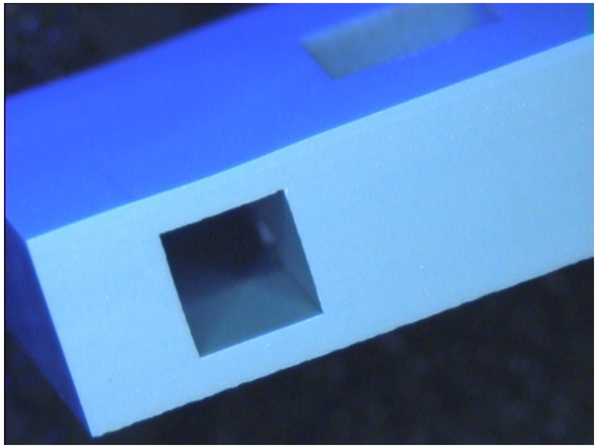


Channels filled with carbon paste

MINIGAS- Project
LTCC Platform for Miniature photo-acoustic gas sensor

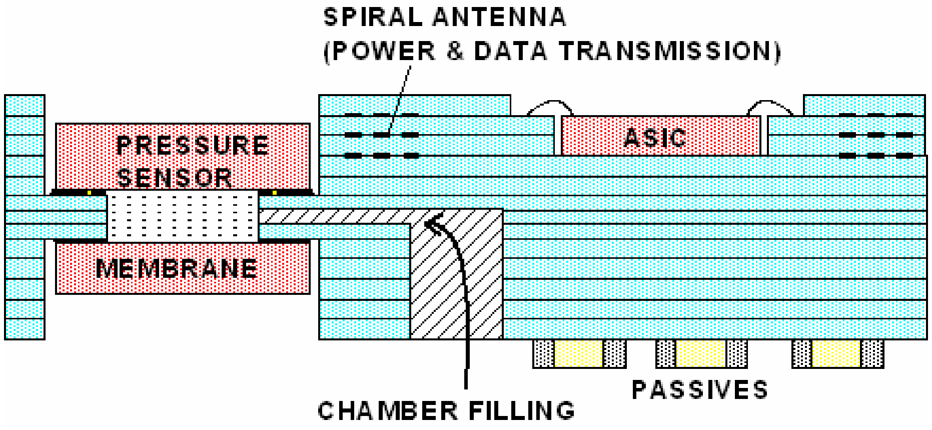


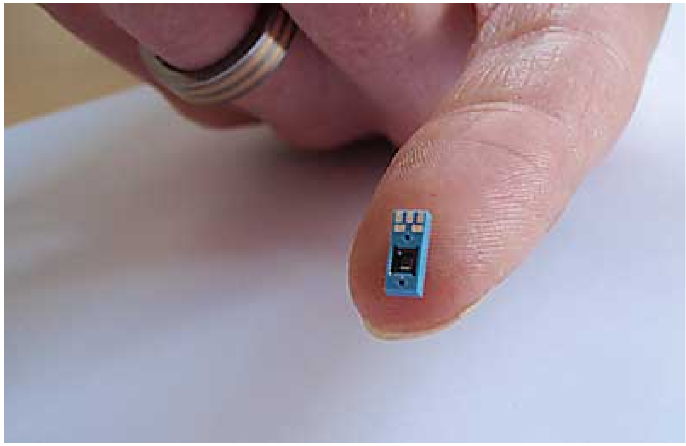




Realised LTCC platform
Channel 2 x 2 x 8mm

Implant for Continuous Blood Sugar Monitoring (Lifecare AS)





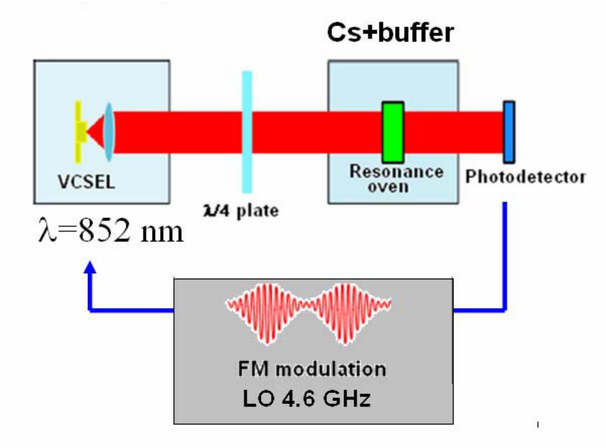
LTCC IMPLANT:

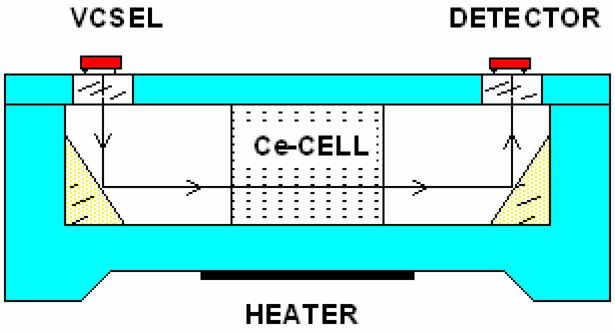
- Packaging of glucose measurement system
- microchannels for reference chamber filling and sealing
- Measurement electronics
- Inductive link for power supply and data transmission

MAC_TFC - project
MEMS Atomic Clocks for Timing, Frequency Control and Communications

- Size and power consumption of existing atomic clocks far exceed those of quartz-based clocks

- GOAL: *To develop an ultra-miniaturized and low-power cesium atomic clock in LTCC package presenting:*
  - *Small size*
  - *a short-term stability of* $5*10^{-11}$ *over 1 hour (Thermal stability important)*
  - *less than 200 mW power consumption*





Atomic clock package concept