RF IV Waveform Measurement and Engineering

- Role in Transistor Characterization and Amplifier Design -

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IEEE MTT-S Distinguished Microwave Lecturer 2008-2010

RF Waveform Measurement and Engineering

- powerful dynamic transistor characterization tool

- Basic Concept
  - Use RF Waveform Measurement and Engineering Systems to investigated both the transistors dynamic I-V (Current-Voltage) plane and its Q-V (Charge-Voltage) plane
    - Both qualitative and quantitative
    - Alternatives: DC I-V, Pulsed I-V, bias dependent s-parameters

- Applications
  - Technology Evaluation
    - *Observe and quantify its dynamic large signal response*
  - Technology Optimization
    - *Link technology design to system performance*
  - Technology Modelling
    - *support the development of CAD tools*
  - Circuit Design Tool
    - *Support the development of Power Amplifiers*

RF Waveform Measurement and Engineering

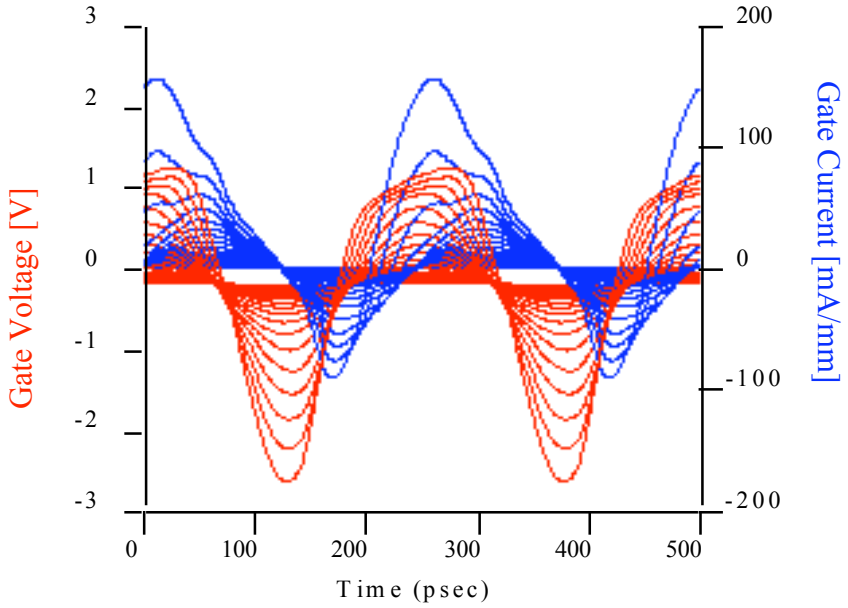
- powerful dynamic transistor characterization tool

- Transistor Characterization: Case Study
  - Use RF Waveform Measurement and Engineering Systems to investigated general performance of Transistor Technology
    - Current Limits, Modes of Operation, RF Cooling

Transistor RF I-V Waveforms

– *Detailed Insight into Dynamic Behaviour Limitations*

- Measure Input voltage and current waveforms
  - function of input drive level



AlGaAs/InGaAs HFET @ 4 GHz

- Detailed Insight into Dynamic Behaviour
  - Gate Diode: Forward Diode Conduction and Reverse Breakdown
  - Gate Capacitance
- Relevant information for both
  - Device Engineer
  - PA Circuit Designer

Transistor RF I-V Waveforms

– *Detailed Insight into Dynamic Behaviour Limitations*

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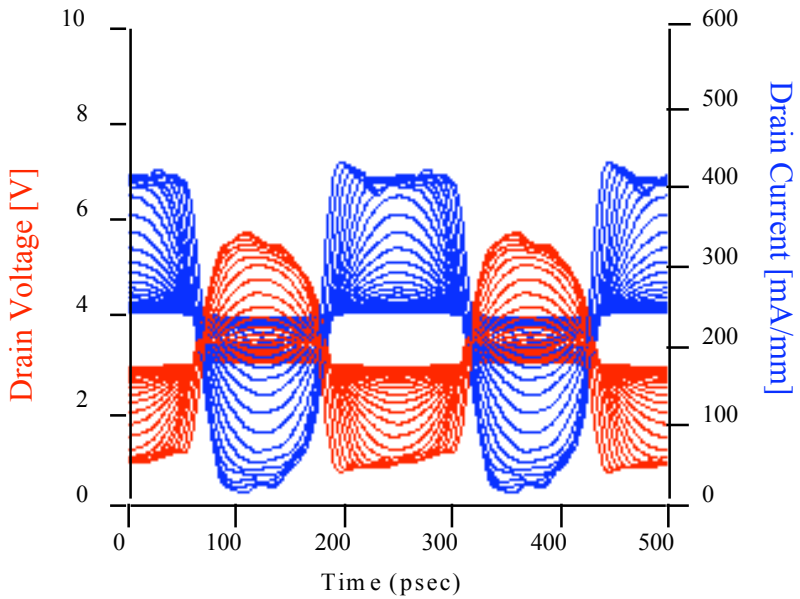
  - function of input drive level

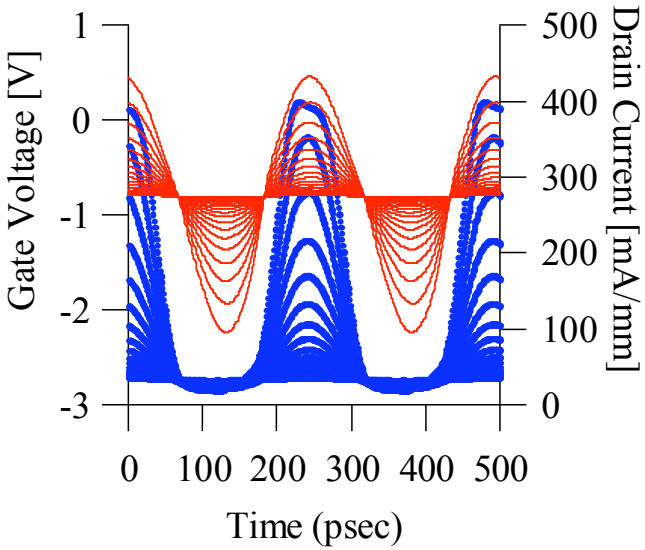


AlGaAs/InGaAs HFET @ 4 GHz

- Detailed Insight into Dynamic Behaviour
  - Drain Current Saturation: Knee Region and Breakdown
  - Gate-Drain Trans-capacitance
- Relevant information for both
  - Device Engineer
  - PA Circuit Designer

Transistor RF I-V Waveforms

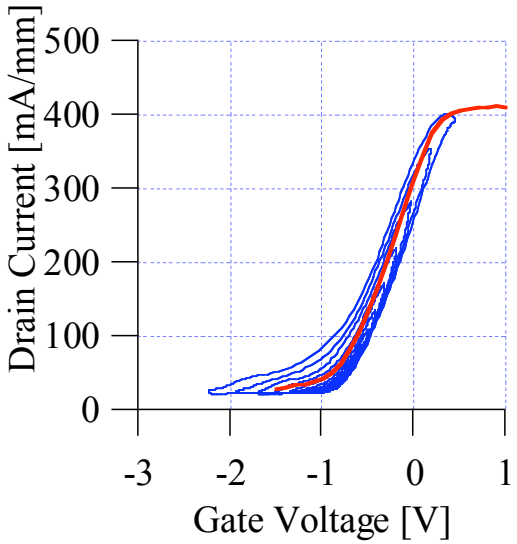
– *Detailed Insight into Dynamic Behaviour Limitations*



@ 4.0 GHz

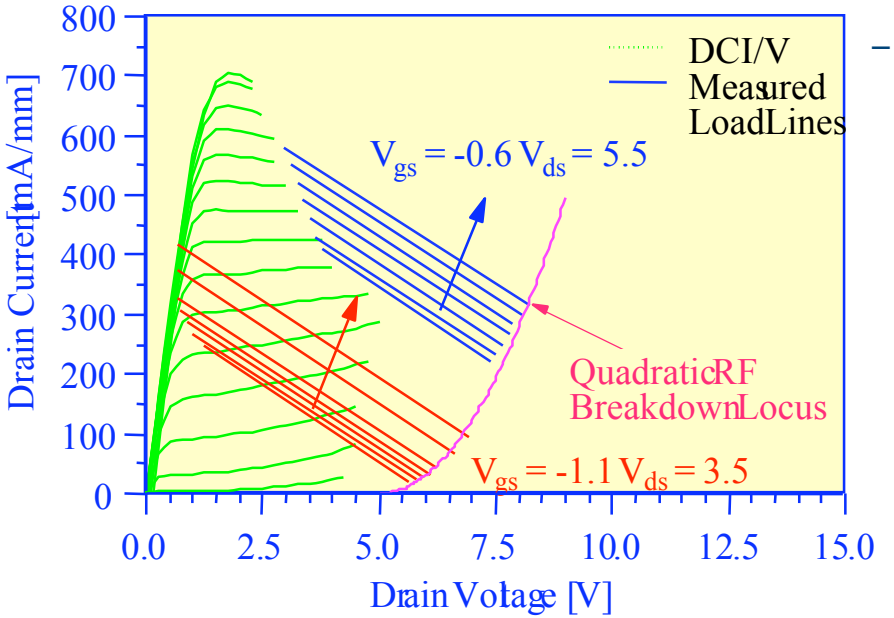
Dynamic Transfer Characteristic Measurements

- Device Response
  - Waveform Shapes
  - Insight provided by eliminating time axes
    - Effects of dynamic transfer characterisation clearly observed
      - DC/RF Dispersion
    - Effects of Delay/Trans-capacitance clearly observed
      - I-Q Extraction



Transistor RF I-V Waveforms

– *Detailed Insight into Dynamic Behaviour Limitations*

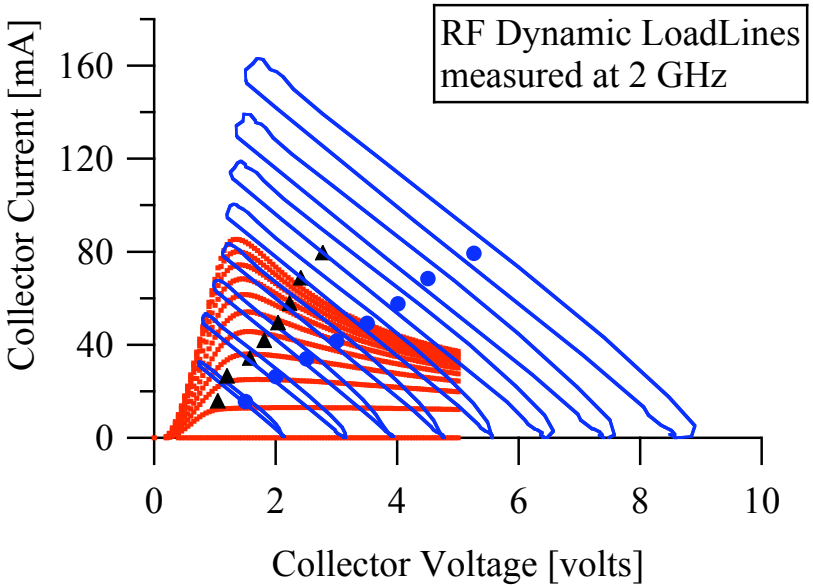


Dynamic Breakdown
in Low Noise
AlGaAs/InGaAs HFET's

- Device Response
  - Waveform Shapes
- Insight provided by eliminating time axes
  - Effects of dynamic gate-drain breakdown clearly observed

Transistor RF I-V Waveforms

– *Detailed Insight into Dynamic Behaviour Limitations*

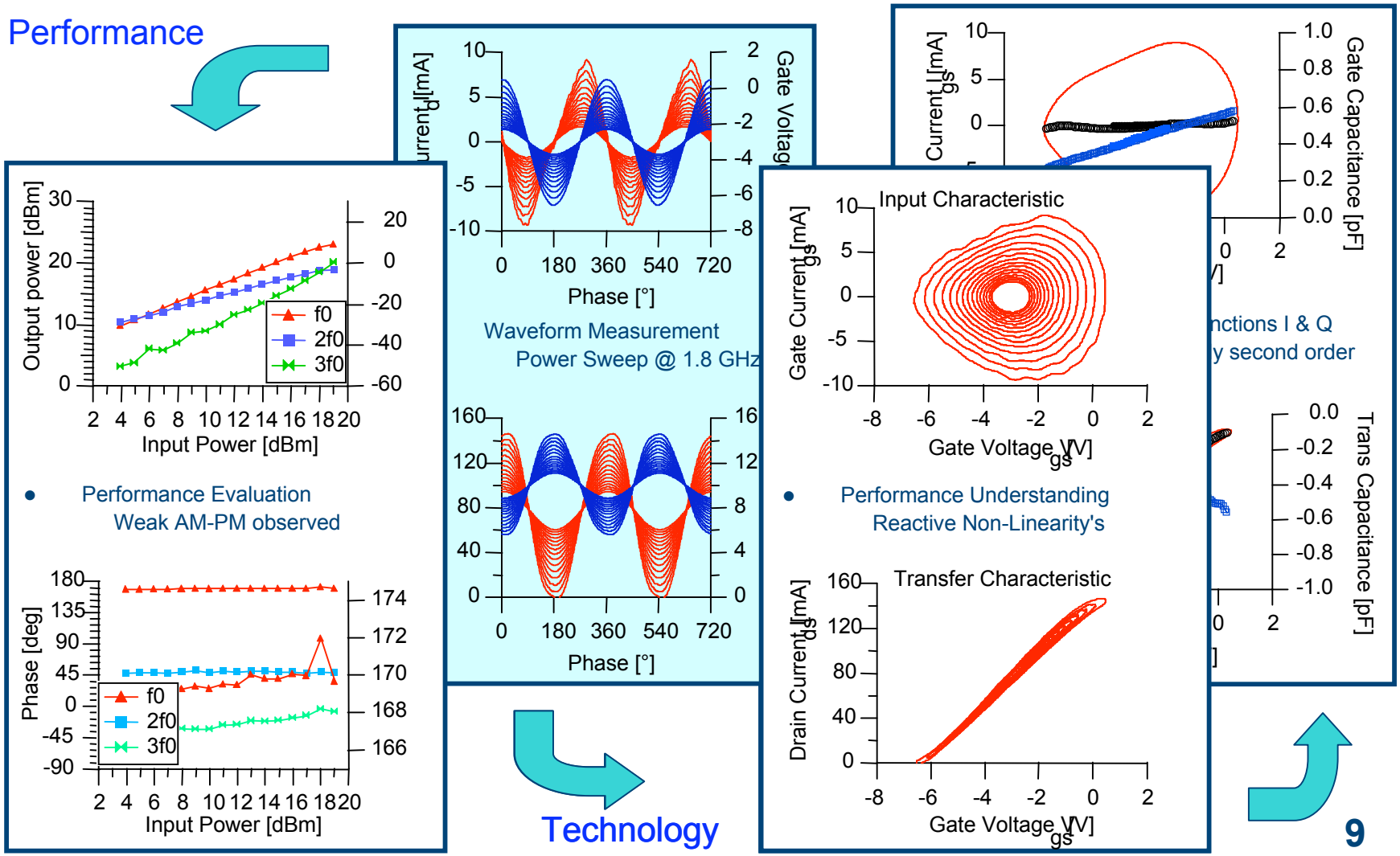


- Device Response
  - Waveform Shapes
- – Insight provided by eliminating time axes
  - Effects of dynamic RF cooling clearly observed
- – Linked with pulsed RF I-V technique

RF Cooling in
Handset PA
AlGaAs/InGaAs HBT's

Measured RF I-V Waveforms

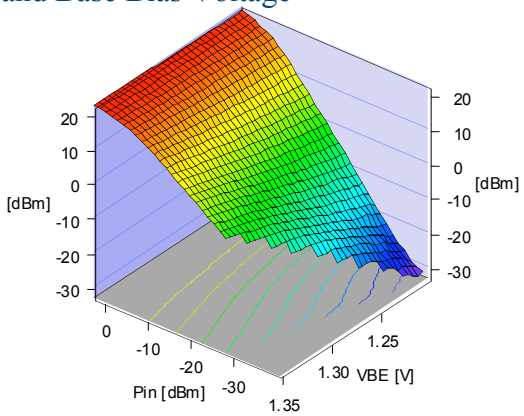
– *Unifying Analysis Tool*



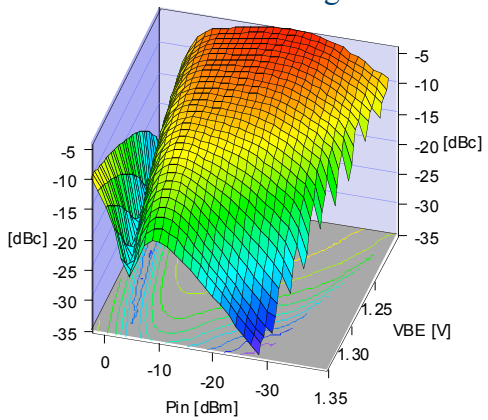
Measured RF I-V Waveforms

– *General purpose Analysis Tool*

Output Power versus Input Power and Base Bias Voltage



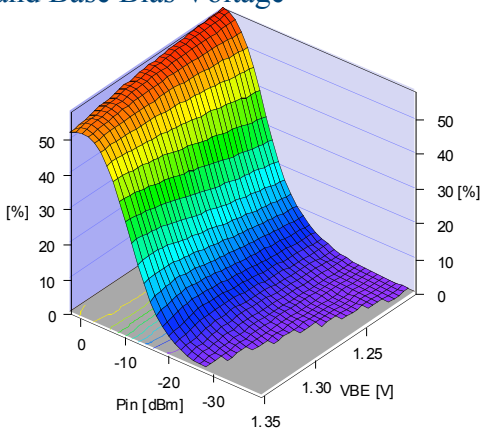
2nd Harmonic Output Power versus Input Power and Base Bias Voltage



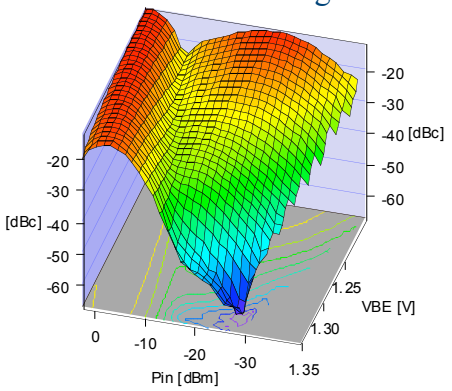
Experimental Emulate the affect of varying external parameters: In this case input drive level and input DC bias voltage

Note, have all information on magnitude and phase of all voltage and current Fourier components

Efficiency versus Input Power and Base Bias Voltage



3rd Harmonic Output Power versus Input Power and Base Bias Voltage



GaAs HBT Performance as a function of Load Impedance

RF Waveform Measurement and Engineering

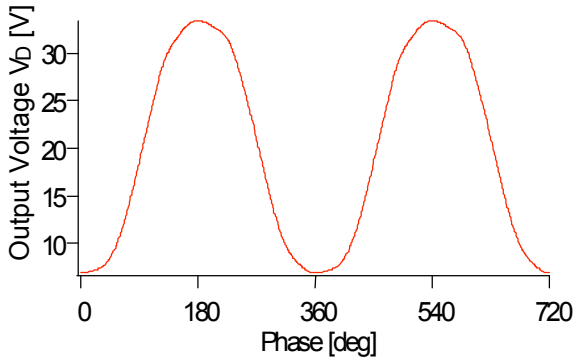
- powerful dynamic transistor characterization tool

- Transistor Characterization: Case Study
  - Use RF Waveform Measurement and Engineering Systems to investigated factor limiting the observed power performance of the emerging GaN Transistor Technology
    - Current Collapse, Knee Walkout, Poor Pinch-off

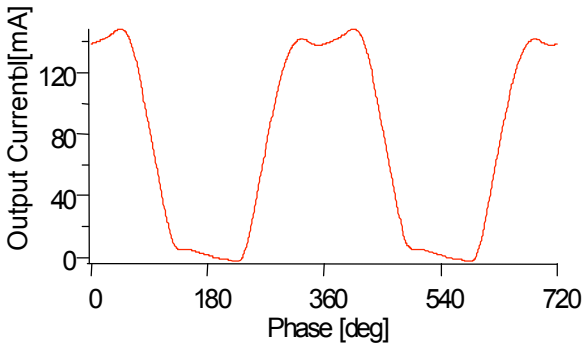
Transistor Characterization: GaN Case Study

- visualizing the DC-RF Dispersion Problem

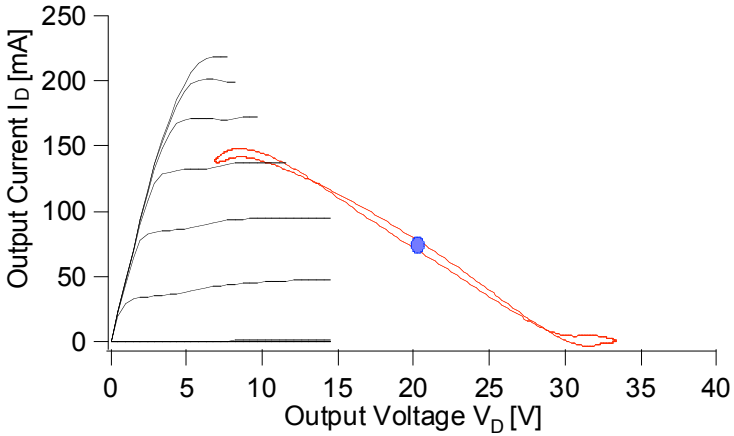
Commonly observed that the RF Power Performance of the GaN transistor was less than predicted (DC I-V & s-parameters)



Approach: Drive the GaN transitor in to compression while measuring RF Output V & I Waveforms (840MHz)



Plot against one another to give the RF Load-line

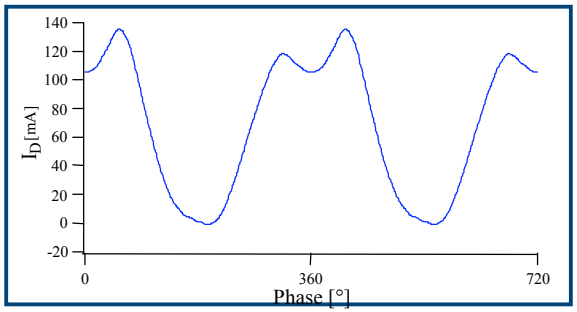


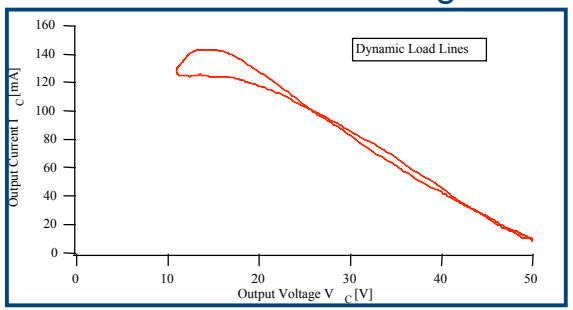
Waveforms show compression at RF Boundaries differs from the DC Boundaries, hence clearly identifying source of the problem: knee walkout or current collapse

Transistor Characterization: GaN Case Study

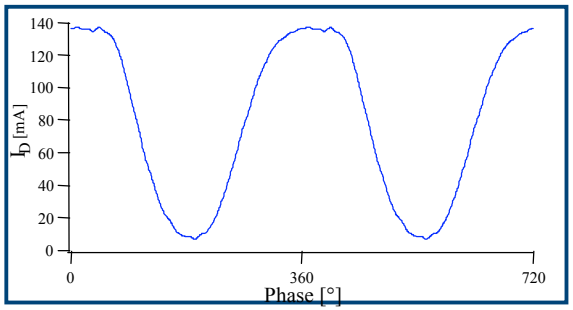
- visualizing the DC-RF Dispersion Problem

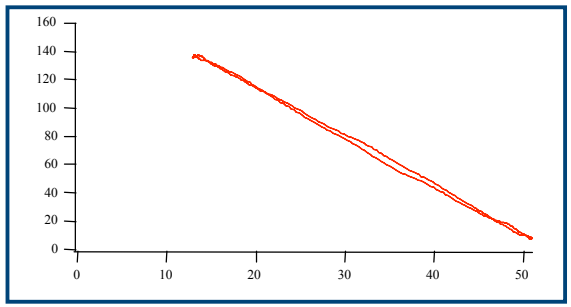
- Measured drain current with fundamental load-pull only
  - Complex load-lines are more difficult to interpret: cause concern in extracting boundaries





- Measured drain current with 3-harmonic load-pull
  - Simple load-lines are easy to interpret: no ambiguity in extracting boundaries



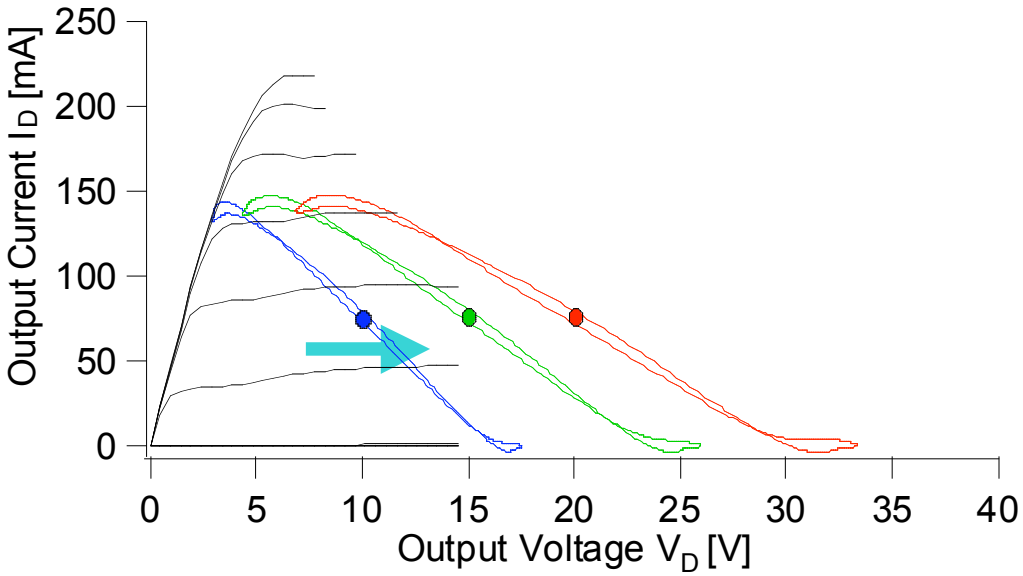


- For quantitative results make full use of waveform engineering, however, fundamental alone does provide for qualitative insight.

Transistor Characterization: GaN Case Study

- visualizing the DC-RF Dispersion Problem

- Investigate factors that influence the knee walkout or current collapse problem: Quiescent Drain Bias Voltage



The Dynamic RF knee boundary shifts as DC drain bias increases

(10, 15 and 20V)

This limits achievable power densities

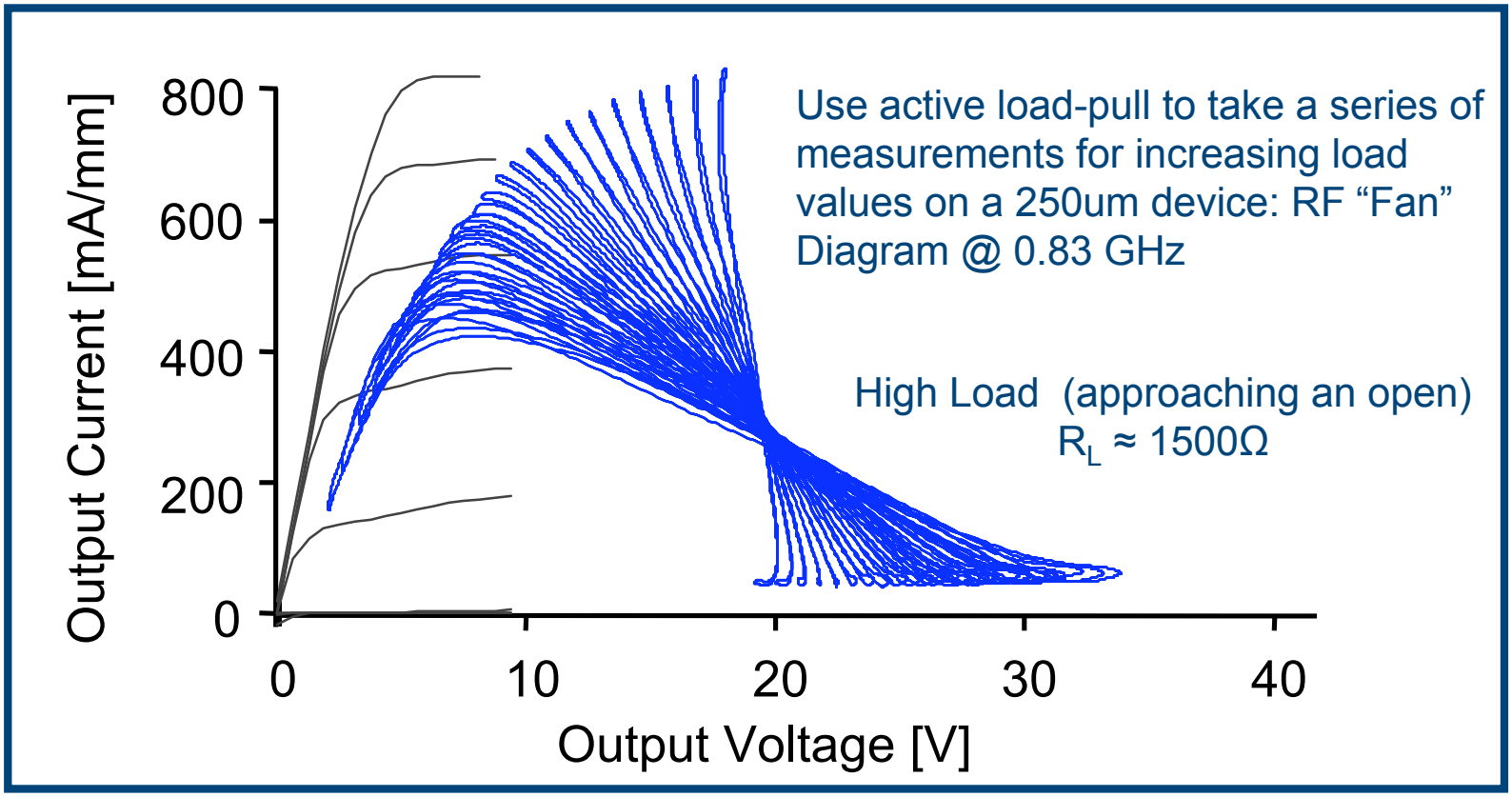
Still unclear whether should relate problem to knee walkout or current collapse

RF “Fan Diagram”: GaN HFET Application

- evaluation of trapping (“knee walkout”) problem

Harmonically rich waveforms

Small Load (almost a short) $R_L \approx 5\Omega$



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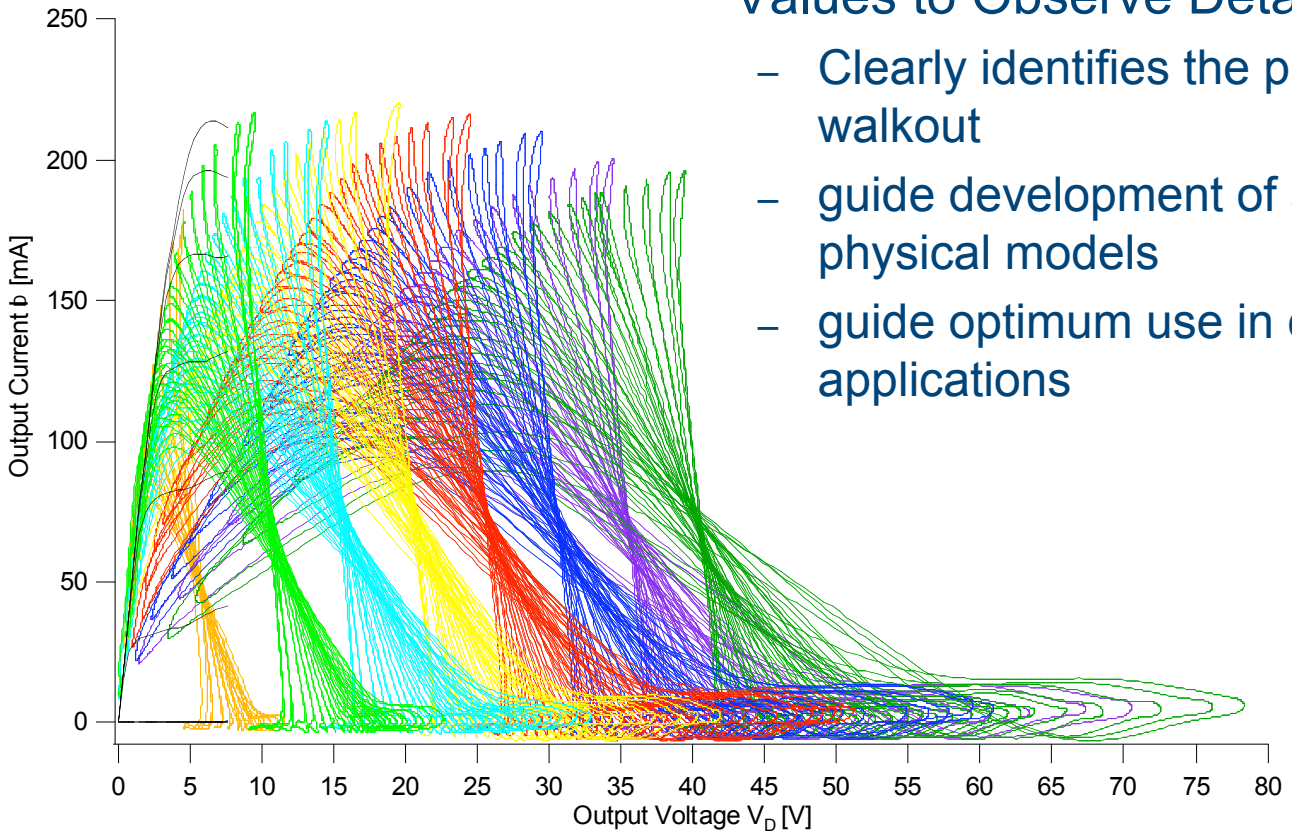


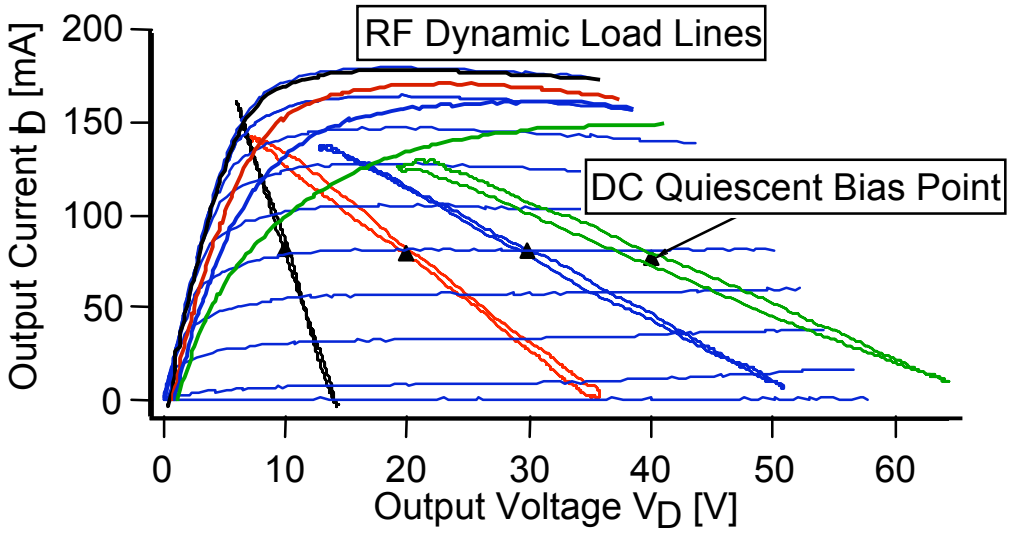
- Repeat for a Range of Drain Bias Values to Observe Detailed Features
  - Clearly identifies the problem: knee walkout
  - guide development of appropriate physical models
  - guide optimum use in circuit applications

Transistor Characterization: GaN Case Study

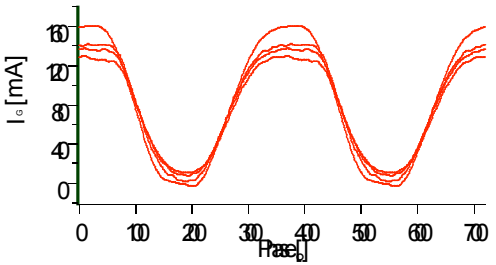
- Class A RF I-V Waveforms versus Pulsed I-V

- Comparison with pulsed I-V Measurements
  - Determine boundaries by simultaneously pulsing both gate and drain voltage (DIVA System) from quiescent Class A bias point

- Clearly observe both predict very similar “RF knee-walkout” as V_D increases



- Compressed current waveforms confirm that the device is in compression

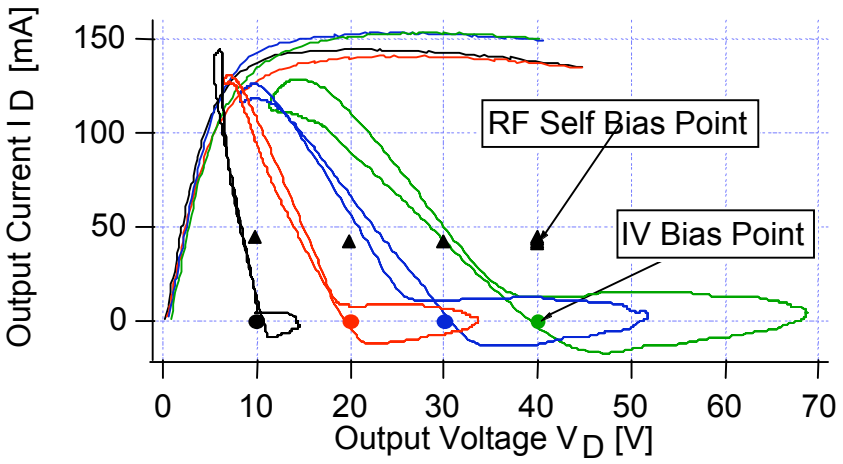


Transistor Characterization: GaN Case Study

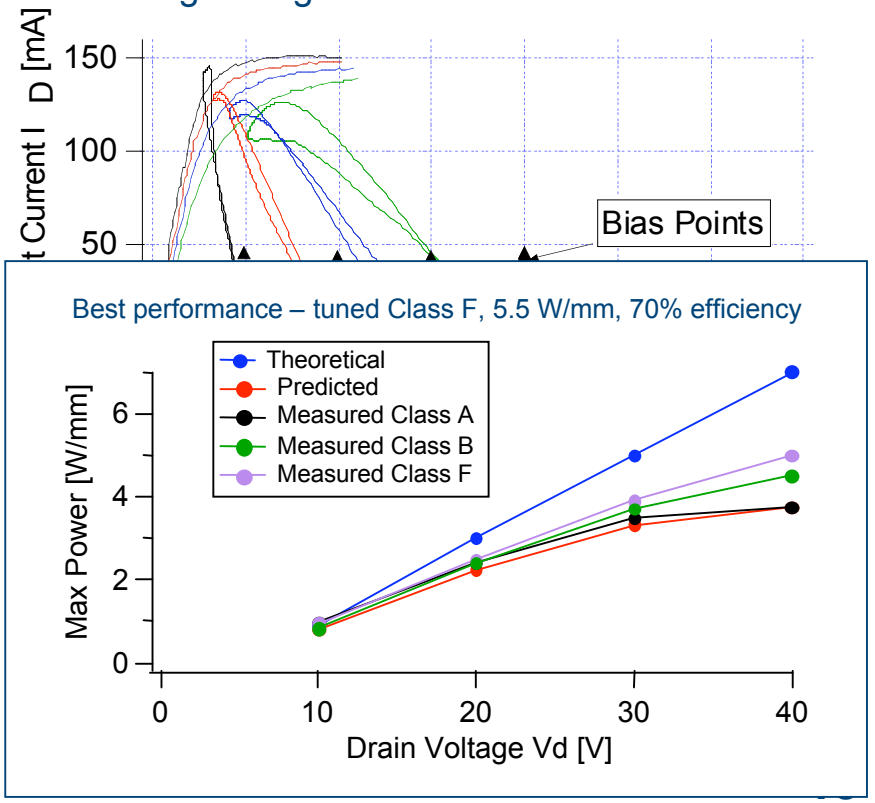
- Class B RF I-V Waveforms versus Pulsed I-V

- Comparison with pulsed I-V Measurements
  - Problem in this case is that the quiescent bias point is not on the DC I-V plane: Where do we pulse from?

- Same voltage V_G bias point
  - poor agreement



- Same current I_D bias point
  - good agreement



- "RF knee-walkout" is sensitive to mode of operation

RF Waveform Measurement and Engineering

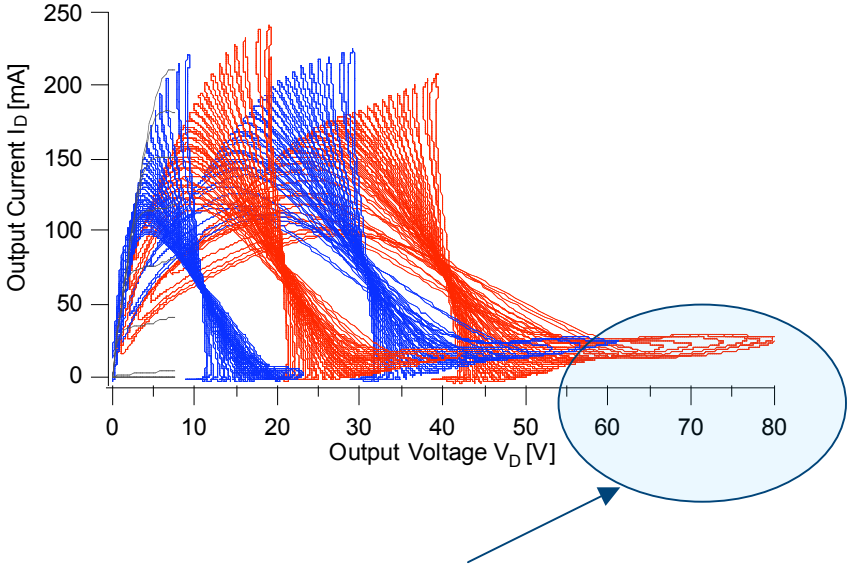
- powerful dynamic transistor characterization tool

- Transistor Characterization: Technology Evaluation and Optimization
  - Poor Pinch-off very similar to knee walkout investigations
  - Reliability and device stress: emerging area.

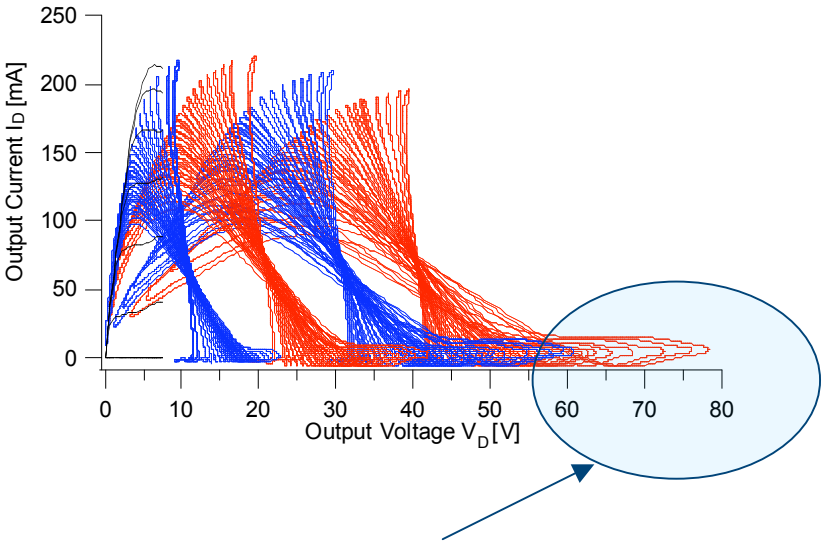
RF “Fan Diagram”: GaN HFET Application

- evaluation of buffer layer design (“soft pinch-off”)

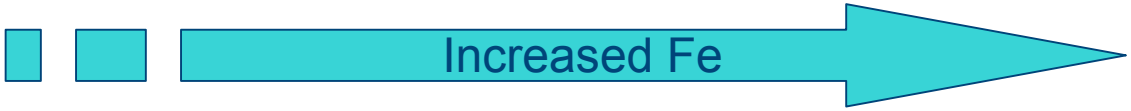
- Evaluate Different Buffer Layer Design (Level of Fe Doping)
  - Elimination of soft pinch-off
  - No significant effect at the Knee Region



Undesirable “Soft” Pinch-off Behaviour



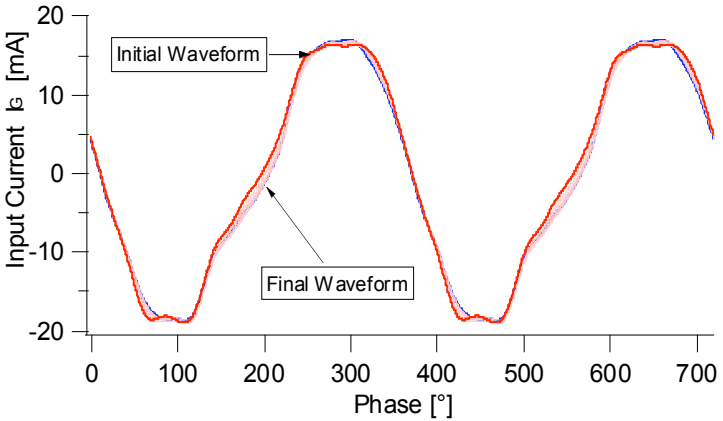
Improved Pinch-off Behaviour

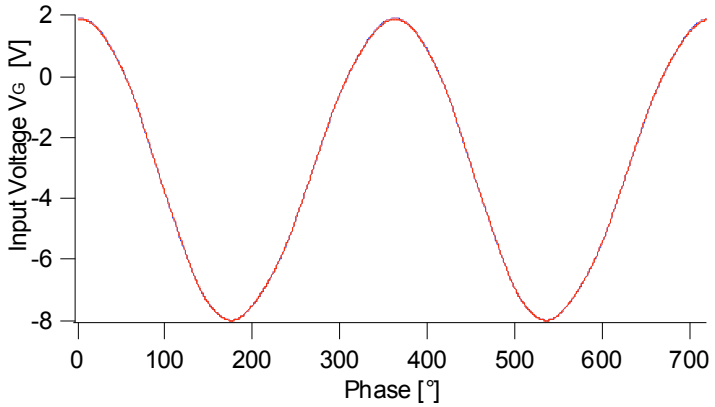


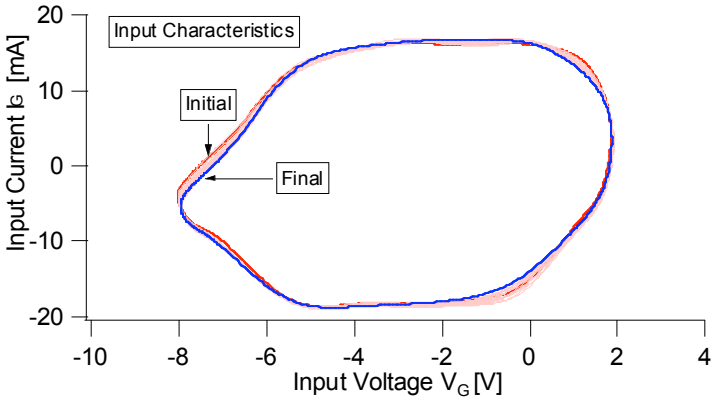
Transistor RF I-V Waveforms: GaN HFET Application

– Detailed Insight into Dynamic stress/reliability Limitations

- RF waveforms were periodically sampled 100 times during the 1.5hour RF stress period
- 1.8GHz Large-signal CW (≈ 3dB of gain compression), V_D = 20V, Class A, $Zf_0 \approx P_{OUT}$



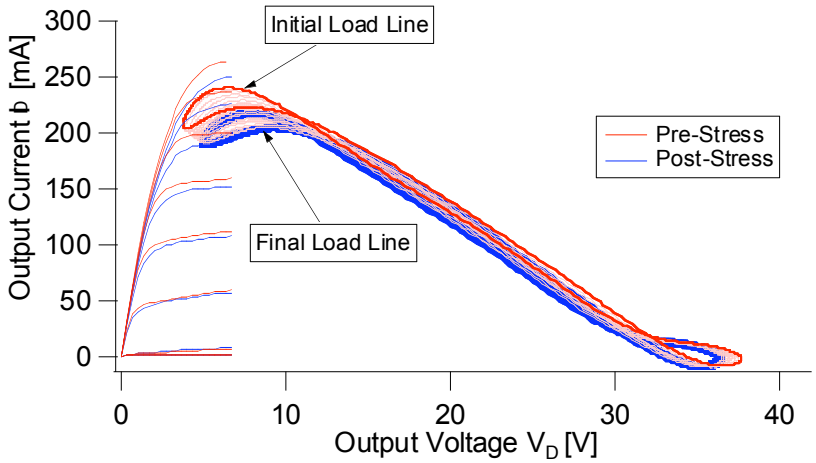




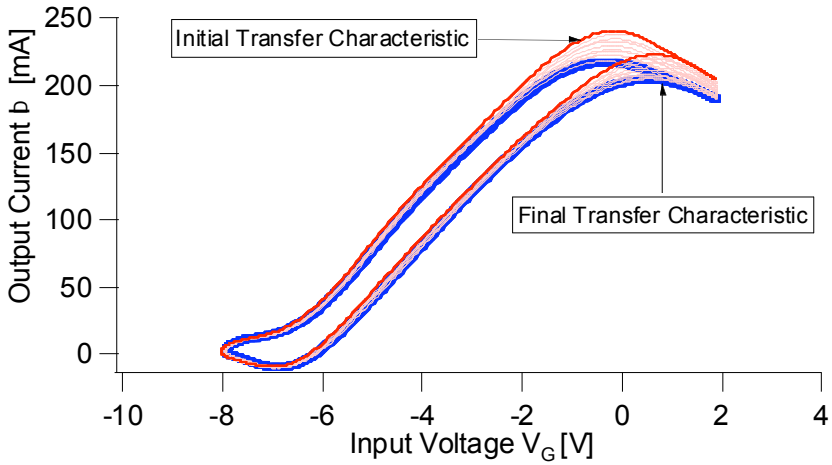
- Dynamic Input Characteristics
  - Highlights the displacement current through C_{GS}
  - A small increase in leakage can be seen at the breakdown end

Transistor RF I-V Waveforms: GaN HFET Application

– Detailed Insight into Dynamic stress/reliability Limitations



- Dynamic Load lines (overlaid on DC-IVs)
  - Useful for visualising DC-RF dispersion – a non-permanent problem
  - Here the degradation is permanent suggesting a different mechanism



- Dynamic Transfer Characteristics
  - Very little degradation until V_G swings above -3V
  - No change around $V_T \approx -6V$

RF Waveform Measurement and Engineering

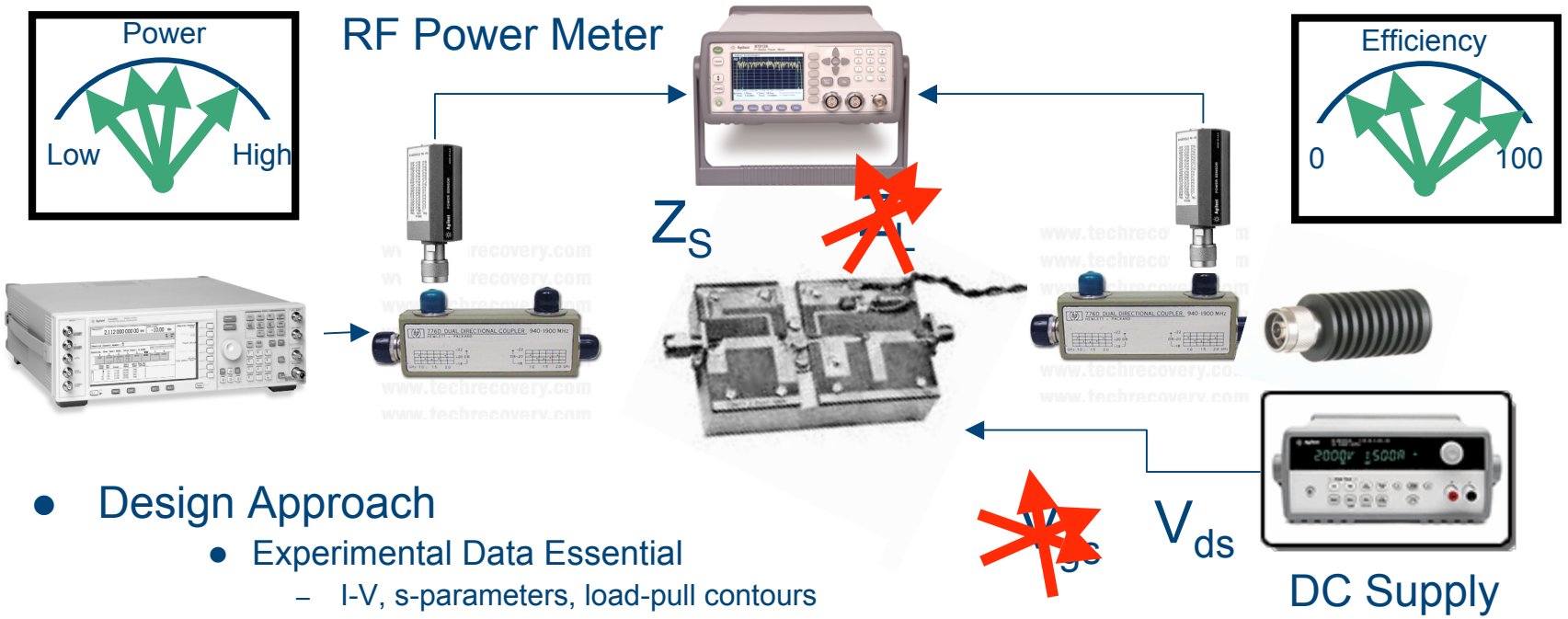
- powerful "real time" design tool

- Basic Concept
  - Use RF Waveform Measurement and Engineering Systems to investigated and achieve the required circuit/system performance.
    - Key: Performance is theoretically defined in terms of the voltage and/or current waveforms
    - Alternatives: build and test, CAD tools (*requires non-linear model*)

- Relevant Circuit Design Problem
  - Those that involve strongly non-linear ('large signal") device operation, not weakly non-linear or linear operation
    - **Power Amplifier Design beyond Class A/AB**
    - Switching Amplifiers
    - Frequency Multipliers/Dividers

Review PA Design Situation

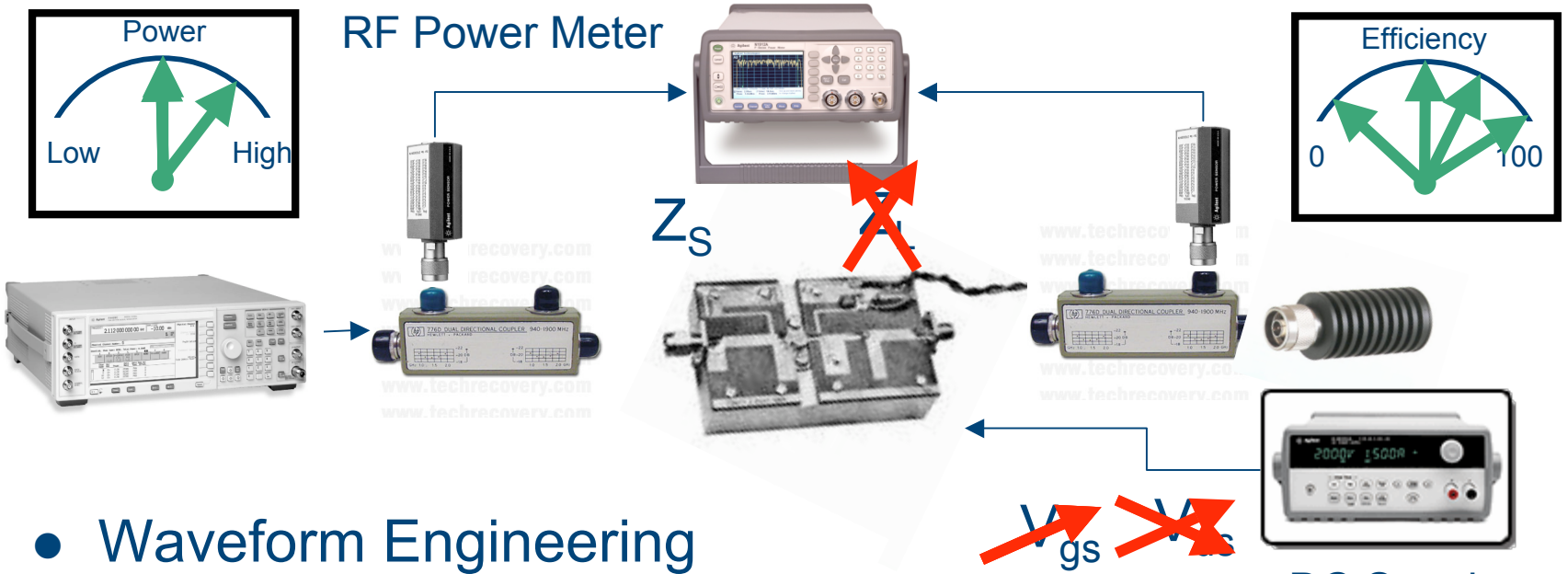
- too reliant on Build & Test



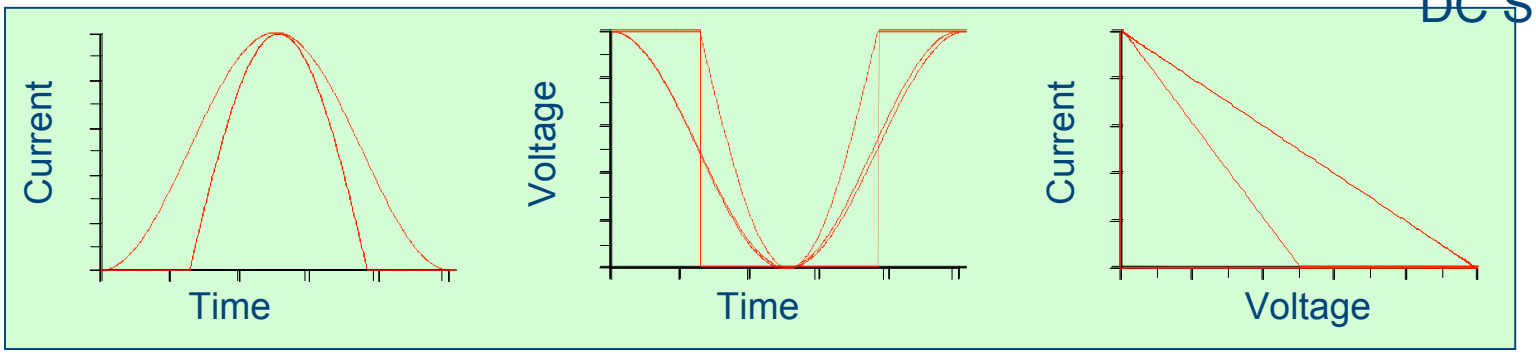
- Design Approach
  - Experimental Data Essential
    - I-V, s-parameters, load-pull contours
  - Design Knowledge: mode of operation, class A, AB,
    - Efficiency Demands: *Move to more complex modes B, F, E or switching modes*
  - Build, Evaluate and Adjust
    - Bias point
    - Load and Source impedance @ fundamental (*and harmonics*)

Review PA Design Situation

- incorporate Basic Principles: "Waveform Engineering"



- Waveform Engineering

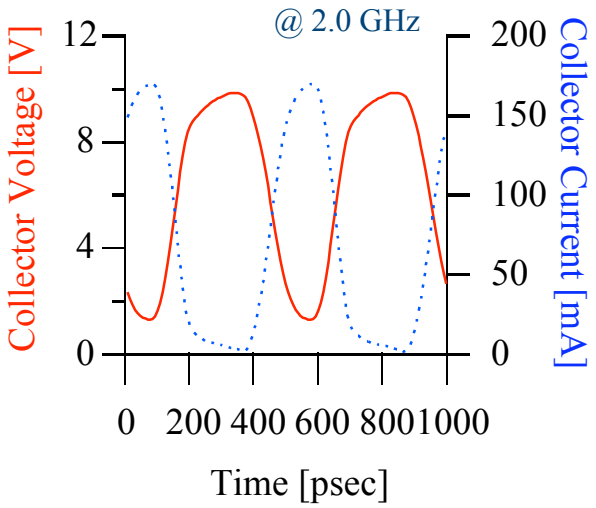


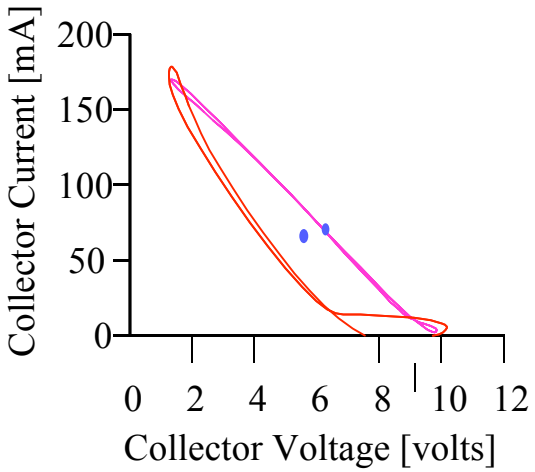
RF I-V Waveform Engineering

- insight provided by having measured waveforms

HBT biased to operate in class B, low quiescent current

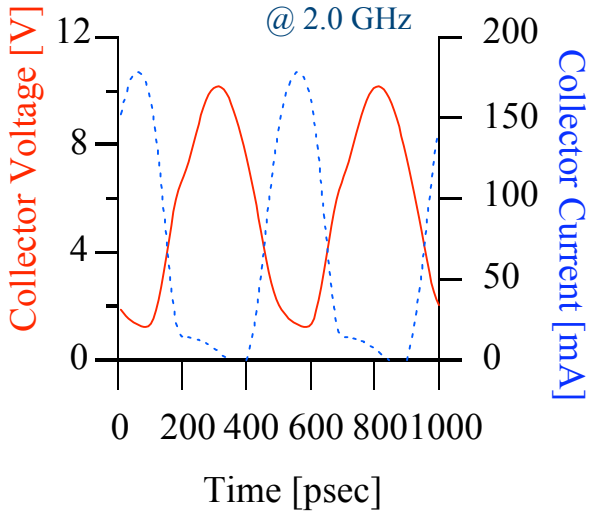
- Current waveform is half rectified
- Voltage waveform is not sinusoidal





Engineer harmonic impedances: Short second/third harmonic

- Current waveform is half rectified
- Voltage waveform is now sinusoidal



"Class B Operation"

Efficiency increased from 44% to 55%

Design Example: Class B Amplifier Emulation/Measurement

RF I-V Waveform Engineering

- insight provided by having measured waveforms

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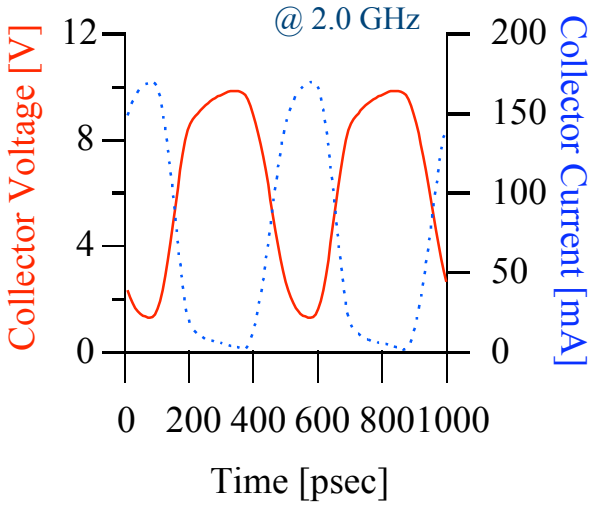
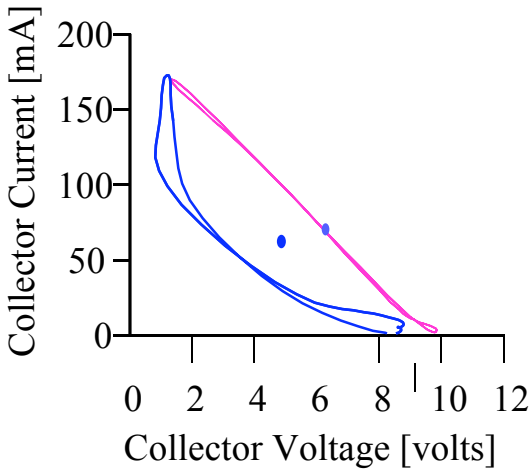
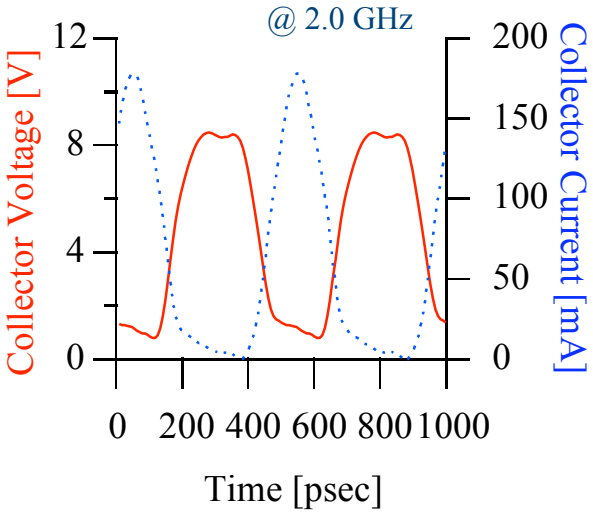
- Voltage waveform is not sinusoidal





Engineer harmonic impedances: Short/open second/third harmonic

- Current waveform is half rectified
- Voltage waveform is now a square wave



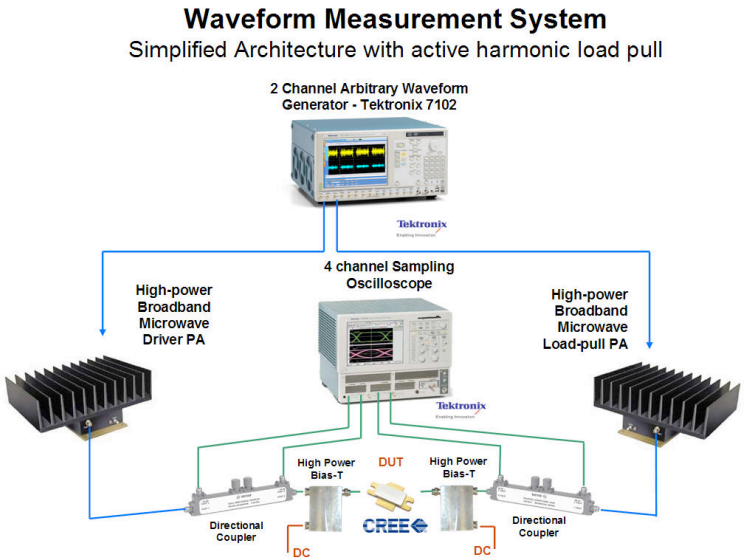
"Class F Operation"

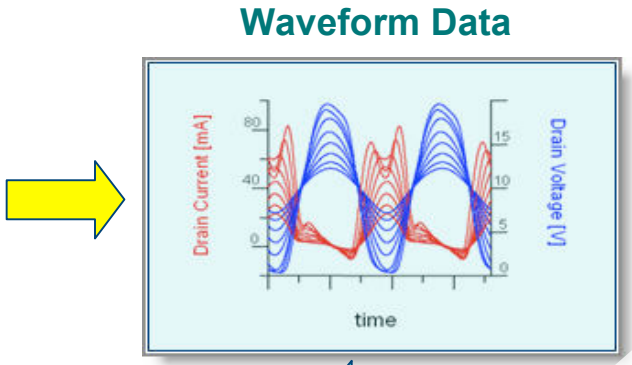
Efficiency increased from 44% to 65%

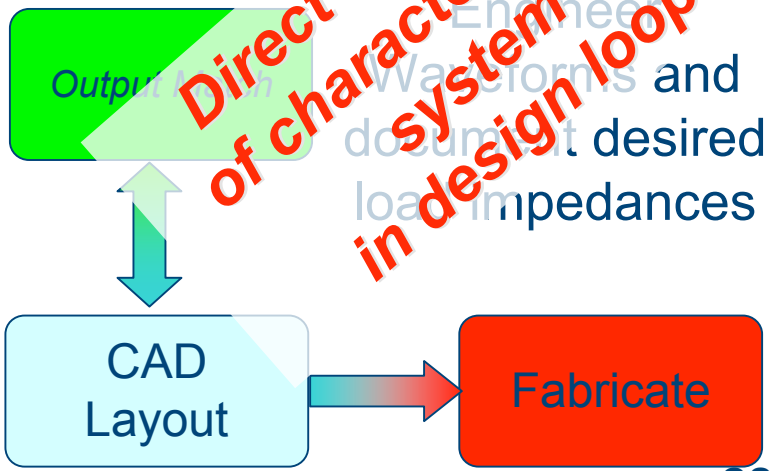
Design Example: Class F Amplifier Emulation/Measurement

RF Waveform Measurement and Engineering

- "on-line" direct utilization in amplifier design cycle







Direct utilization of characterization system in design loop

Engineer Waveforms and document desired load impedances

- Relevant Circuit Design Problems
  - Those that involve strongly non-linear ('large signal") device operation.
    - Power Amplifier Design beyond Class A/AB
    - Switching Amplifiers
    - Frequency Multipliers/Dividers
    - Etc.

RF Waveform Measurement and Engineering

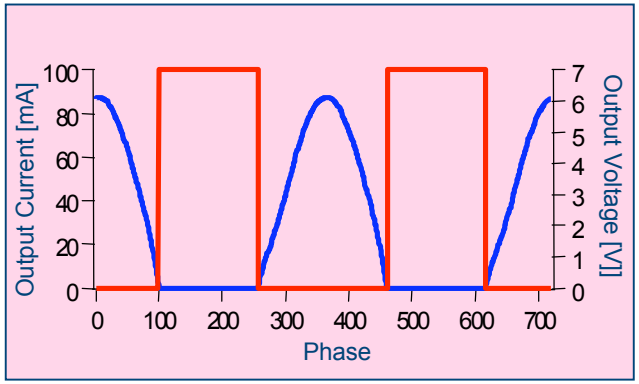
- powerful dynamic transistor amplifier design tool

- Transistor Amplifier Design: Case Study
  - Use RF Waveform Measurement and Engineering Systems to investigated how to realize in practice the theoretically predicted high efficiency modes of operation
    - Class B, Class F or their variants

Design of Highly Efficient RF Power Amplifier

- requires engineer of voltage and current waveforms

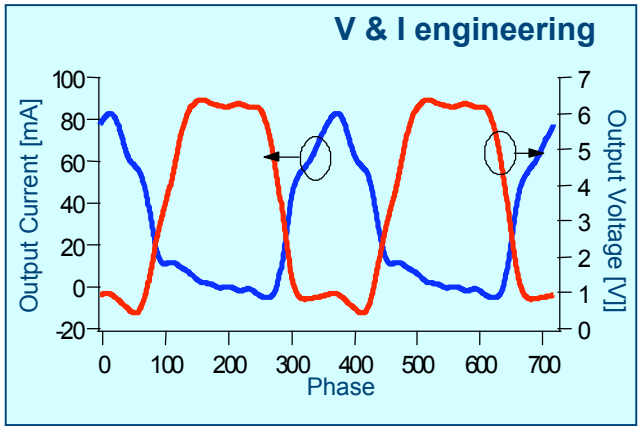
Simple Theoretical Understanding



Practical solution

Transistor characteristics

Circuit Bandwidth



Advanced Theoretical Understanding

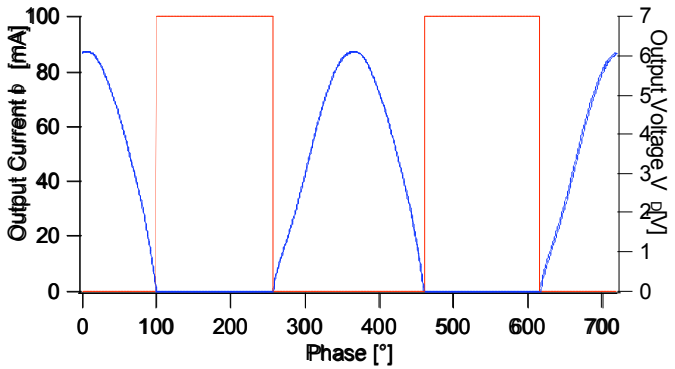
- Designed in an intelligent manner a class F efficient RF Power Amplifier
  - Maximized Output Power
  - Realized 75% PAE
- Ready for realization

Design of Highly Efficient RF Power Amplifier

- review of theoretical understanding: Class F

Ideal Class F occurs if the current and voltage waveforms are simultaneously engineered such that:

The current waveform contains f_0 and correct proportions of the even harmonics



The voltage waveform contains f_0 and correct proportions of the odd harmonics

If this is achieved there is no overlap between the waveforms, resulting in no dissipated power and 100% efficiency.

Design of Highly Efficient RF Power Amplifier

- review of practical constraints: System and Circuit Bandwidth

- The achievable efficiency in a real design is constrained by our ability to correctly engineer the ideal waveforms.
  - Circuit Bandwidth
    - In real PA designs harmonic control is commonly limited to $2f_0$ and $3f_0$ due to the complexity of matching circuits.
    - Following the analysis of Rhodes,* for a Class F design with harmonics only up to $3f_0$ ideally terminated, the maximum achievable efficiency is limited to an upper limit of 90.6% - assuming your matching network is lossless!

We can quantify the ability to engineer ideal waveforms by two factors $\eta_{current}$ and $\eta_{voltage}$ using the DC and fundamental RF components:

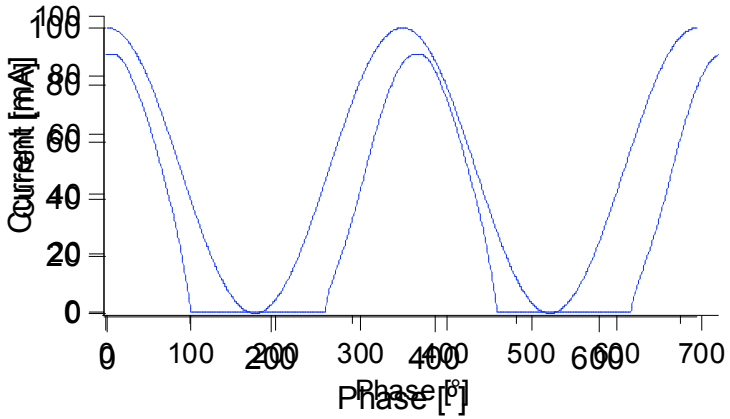
$$\eta_{current} = i_{RF} \Big/ \left(\sqrt{2} \times I_{DC}\right) \qquad \eta_{voltage} = v_{RF} \Big/ \left(\sqrt{2} \times V_{DC}\right)$$

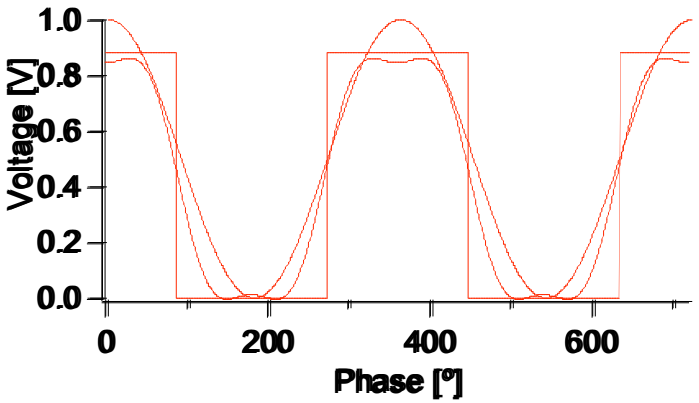
* J.D. Rhodes "Output universality in maximum efficiency linear power amplifiers" International Journal of Circuit Theory and Applications, volume 31, 2003, pp.385-405

Design of Highly Efficient RF Power Amplifier

- review of practical constraints: System and Circuit Bandwidth

Class	$\eta_{current}$	$\eta_{voltage}$	$\eta = \eta_{current} \times \eta_{voltage} \times 100$ [%]
A	0.707	0.707	**50**
B	1.111	0.707	**78.5**
F (Ideal)	1.111	0.900	**100**
F ($3f_0$)	1.111	0.816	**90.6**

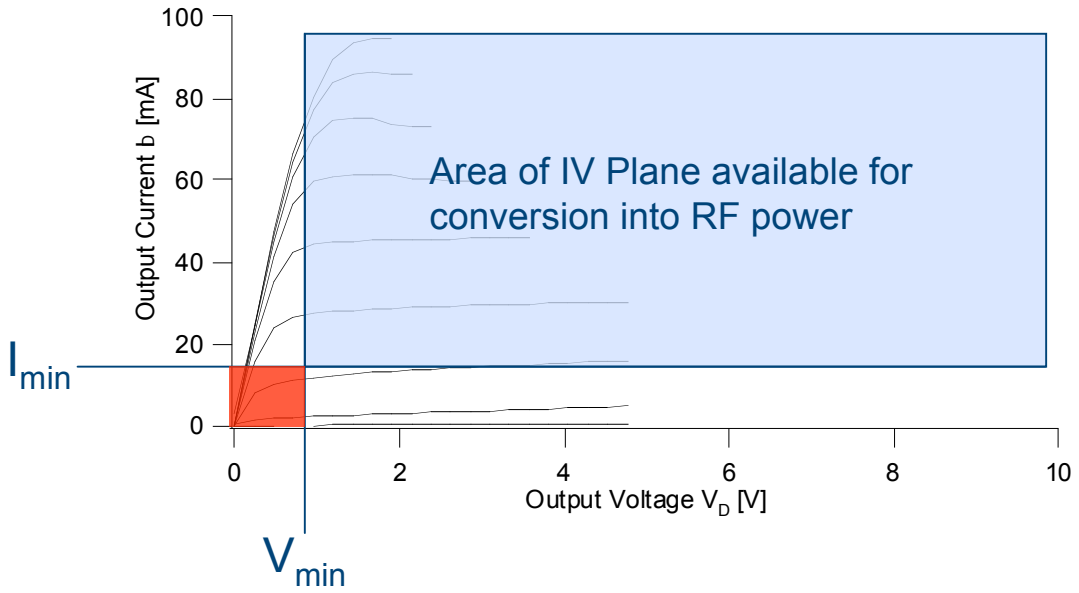




Design of Highly Efficient RF Power Amplifier

- review of practical constraints: Transistor Limitations

- A further limitation on achievable efficiency in practical designs arises from features of real transistor characteristics which make a fraction of the dc dissipated power unavailable for conversion to RF power:



Achievable efficiency is scaled by the ratio of Available to Unavailable IV plane Area

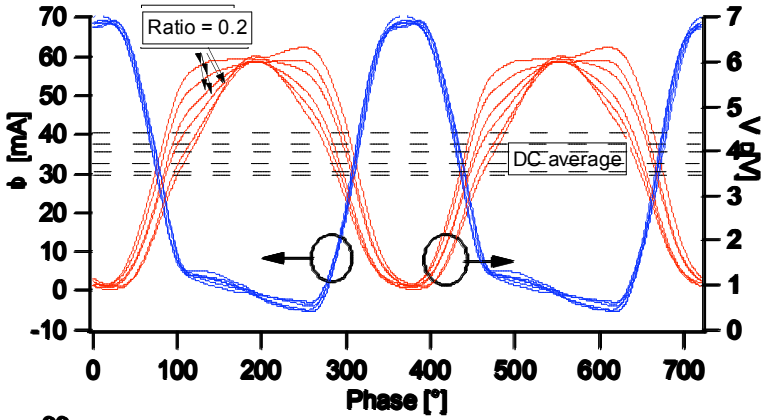
We can quantify the ability to engineer ideal waveforms by two factors $\eta_{current}$ and $\eta_{voltage}$ using the DC and fundamental RF components:

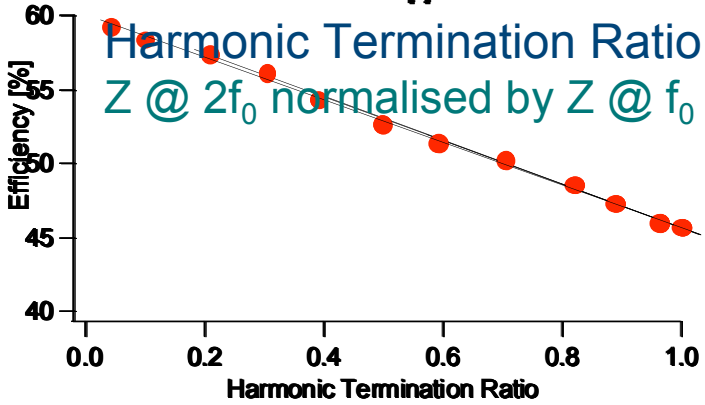
$$\eta_{current} = I_{RF} \Big/ \left(\sqrt{2} \times I_{DC}\right) \qquad \eta_{voltage} = v_{RF} \Big/ \left(\sqrt{2} \times V_{DC}\right)$$

Design of Highly Efficient RF Power Amplifier

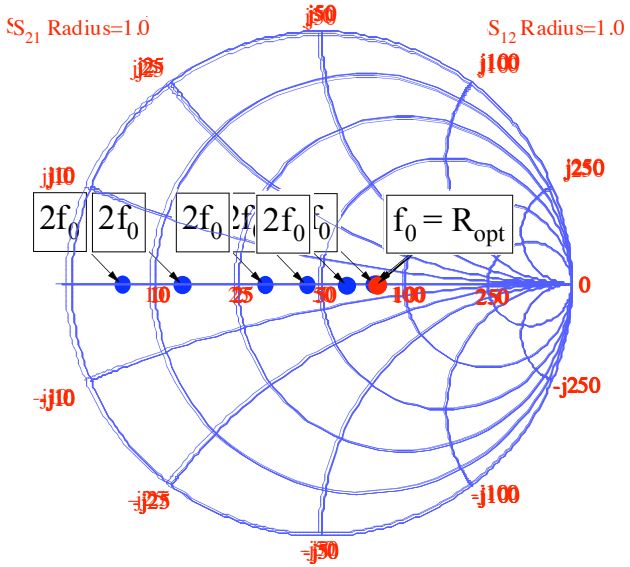
- review of practical constraints: Impedance Scaling

- Starting with Class B bias for a half rectified current waveform, what is the effect of tuning the second harmonic to a short?





Harmonic Termination Ratio:
Z @ $2f_0$ normalised by Z @ f_0

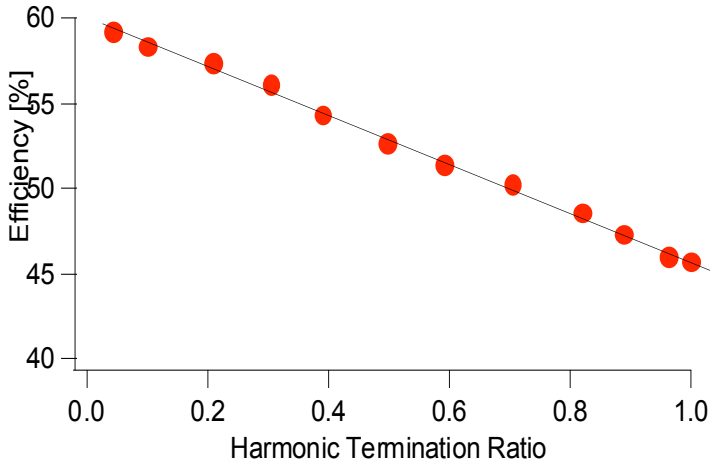


Eliminated 2nd harmonic from voltage waveform

Design of Highly Efficient RF Power Amplifier

- review of practical constraints: Impedance Scaling

- Good short circuits harder to achieve relative to a Small R_{opt}
- Makes high efficiency harder to achieve in large devices
- Possible solution - include numerous short circuits integrated onto the die to allow subsets of transistor cells to be given a better short…
- Packaging parasitics can form a filter blocking higher harmonics…



Harmonic Termination Ratio:
Z @ $2f_0$ normalised by Z @ f_0

Design of Highly Efficient RF Power Amplifier

- review of practical constraints: Transistor Transfer Characteristic

- Need to select a suitable drive level for harmonic generation (approaching P1dB)

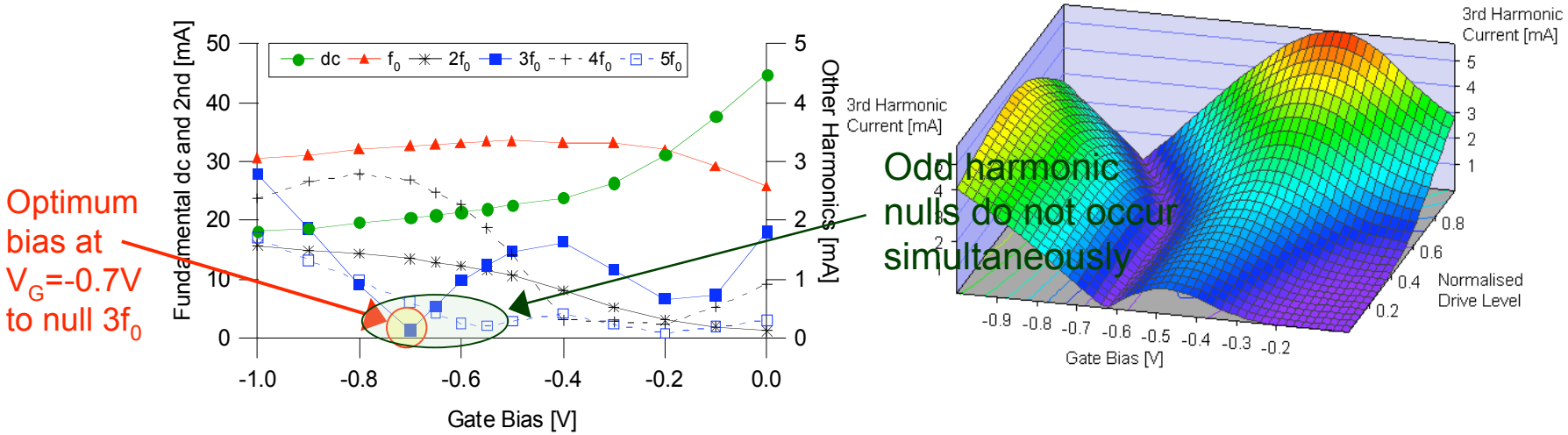
- Ideally we need to ensure we have separated the harmonics:
  - only odds in the voltage waveform
  - only evens in the current waveform

…but will the practical device allow this!

Engineering The Current Waveform

– *Gate bias control to null the odd harmonics*

- In class F optimum performance will only occur if the most significant odd harmonics (usually only consider $3f_0$) are not present in the current waveform.
- Using Fourier analysis of the measured current waveforms we can locate this optimal case…

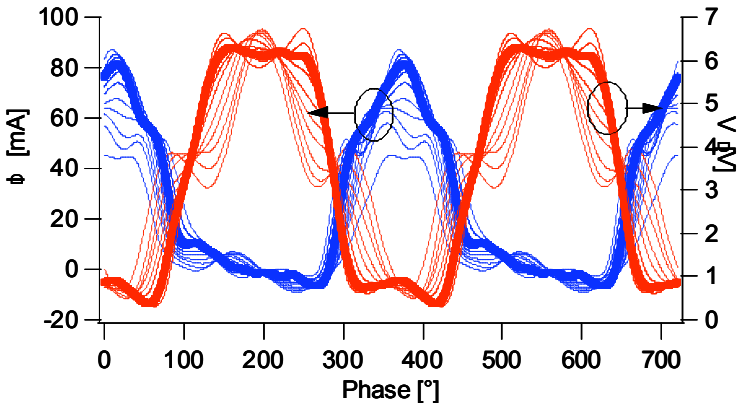


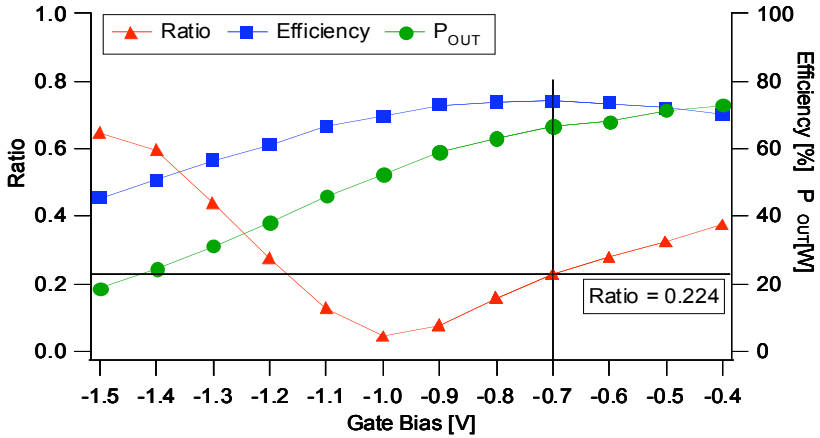
- Practical constraints:
  - Other harmonics are not zero
  - Optimum bias is a function of voltage waveform “shape” and RF drive level

Engineering The Voltage Waveform

- Open tuned 3rd harmonic gate bias sweep

- Engineering the voltage waveform to a square wave involves tuning the 3rd harmonic to an open and increasing the fundamental load to maintain the same current swing.
  - Note, the optimum Class F behaviour will only occur if the current at $3f_0$ remains null.



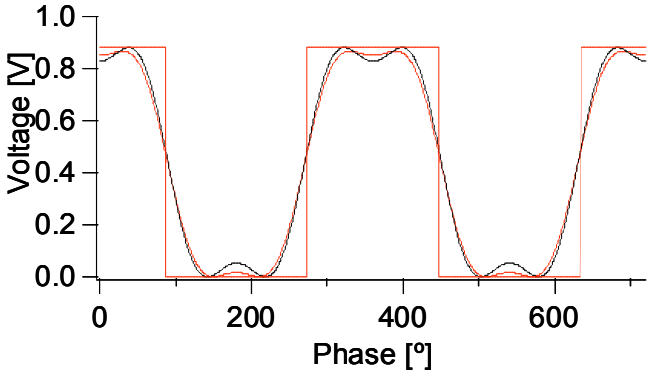


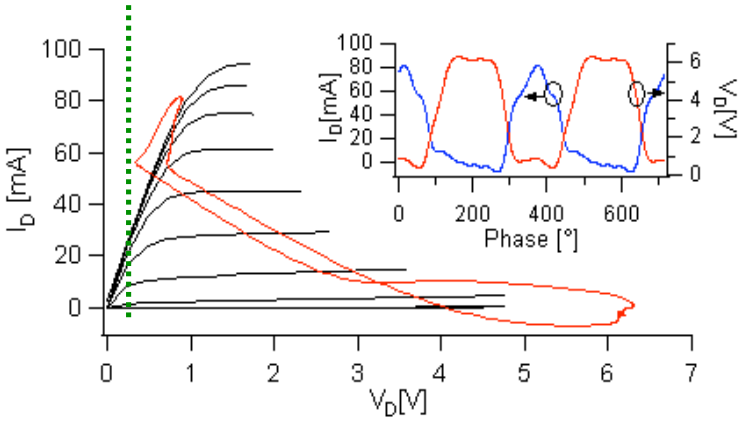
- Since Class F requires an open termination at $3f_0$, it is impossible to verify this condition has been met by direct measurement of the $3f_0$ harmonic current.
  - Consider v_{3rd}/v_{fund} ratio. Theory predicts 1/6 (=0.167)

Engineering The Voltage Waveform

- Why was extra third harmonic developed?

- Plotting the dynamic load-line for the final design shows the interaction of the waveforms with the knee region.
  - Ideal square wave requires all harmonics – we only control the first 3
  - Optimal 3 harmonic only voltage waveform has a v_{3rd}/v_{fund} ratio of 1/6 if the boundary conditions are ideal (vertical)
  - However due to the finite on-resistance of the real knee boundary the optimal ratio is higher, at almost 1/4



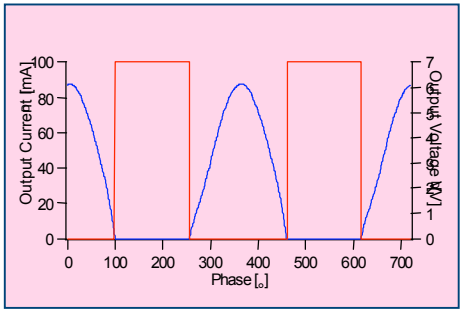


- The final experimentally engineered “class F” waveforms achieved a drain efficiency value of 75%,
- This is extremely high given the boundary conditions and drain bias of the real device used.

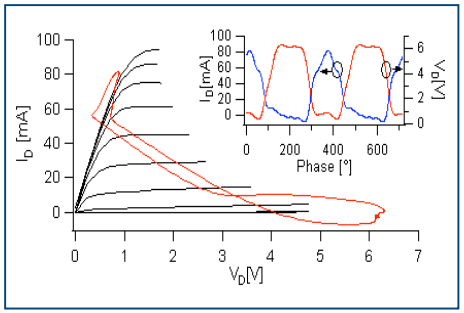
RF Waveform Measurement and Engineering

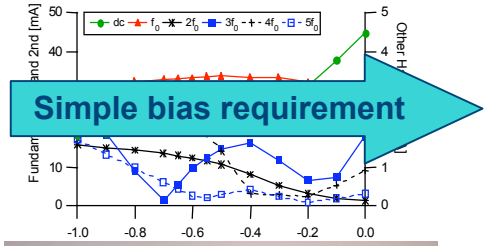
- "on-line" direct utilization in amplifier design cycle

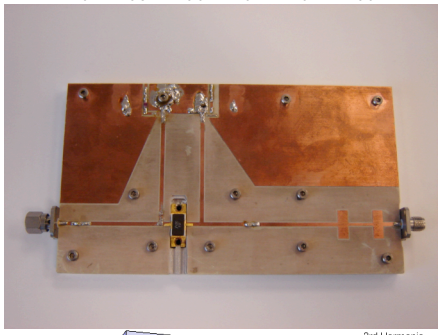
Simple Theoretical Understanding: *Provides If not How and Why*



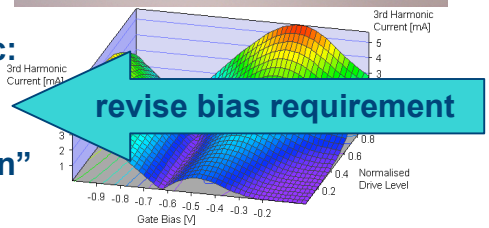
Transistor characteristics → **Circuit Bandwidth**

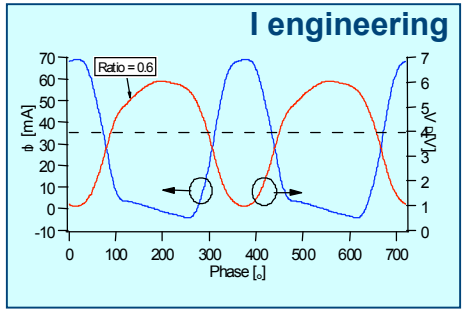




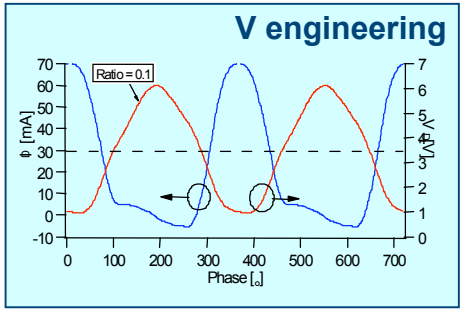


3rd harmonic: open circuit "relaxation"





2nd Harmonic short circuit



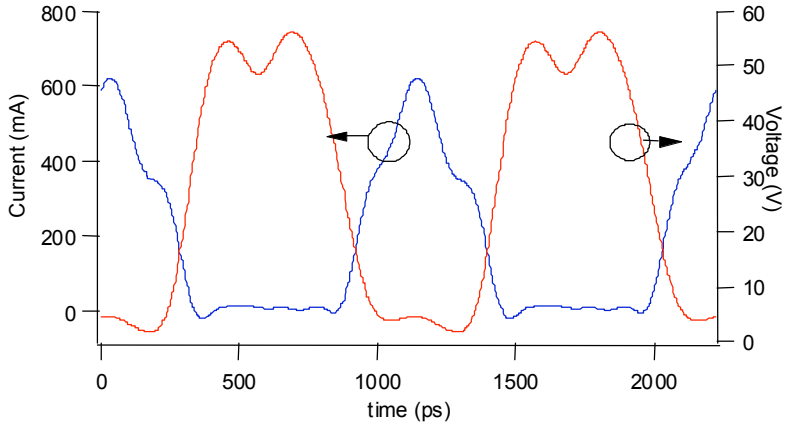
Advanced Theoretical Understanding: *Must provide How and Why*

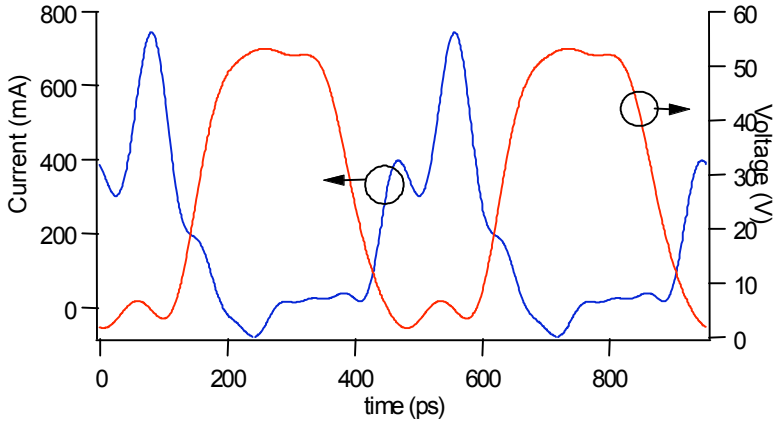
developing theoretically based but practically relevant waveform engineering design methodologies

Apply Waveform Design Methodology

- 5W Si LDMOS into Class F Emulation/Design

Engineered and Measured Intrinsic Waveforms: Design Aid





High Power Class F Design

5W Si LDMOS @ 900 MHz

- Class F clearly achieved
- High Power 36.0 dBm (4W)
- High Efficiency 77.2%

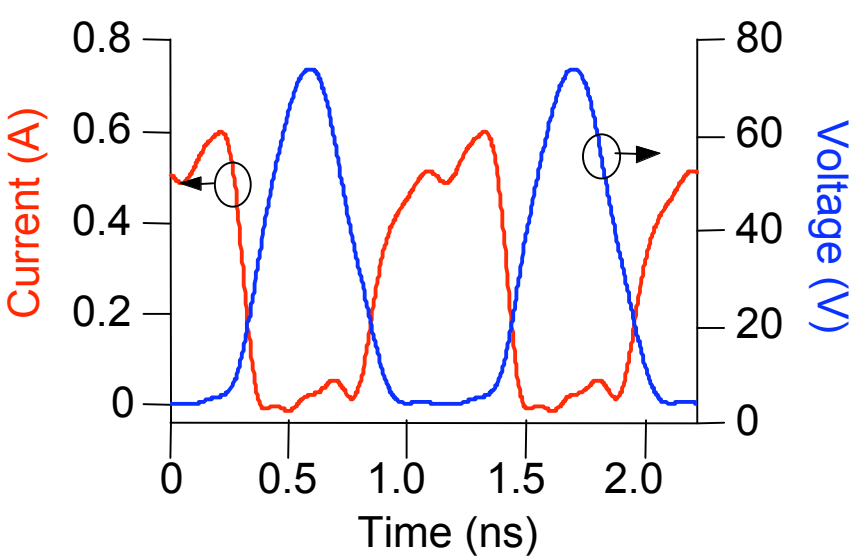
5W Si LDMOS @ 2100 MHz

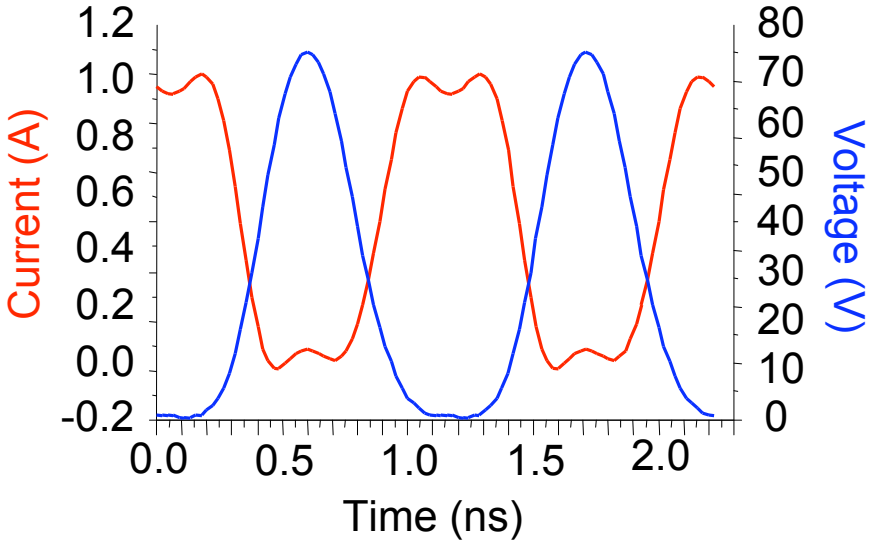
- Class F clearly achieved
- High Power 35.9 dBm (4W)
- High Efficiency 77.1%

Apply Waveform Design Methodology

- 10W GaN HFET & 5W Si LDMOS into Inverse Class F

Engineered and Measured Intrinsic Waveforms: Design Aid





5W Si LDMOS @ 900 MHz

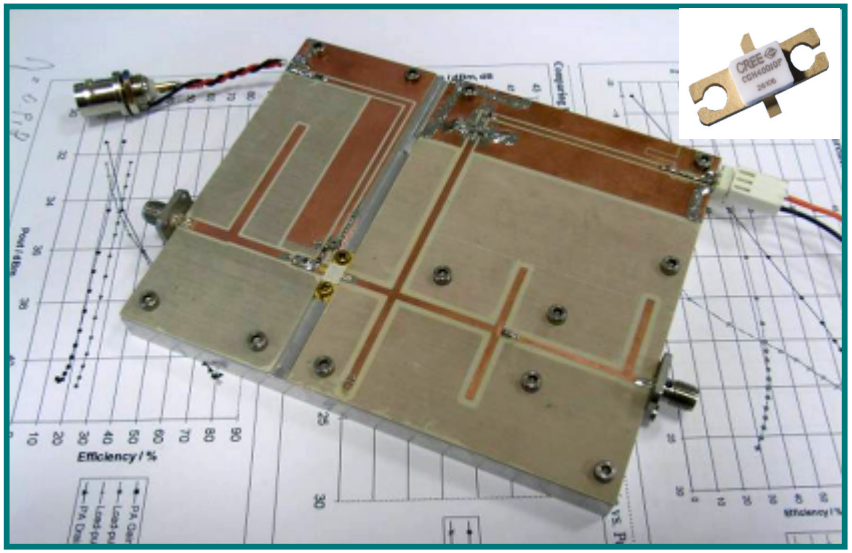
- Inverse Class F clearly achieved
- High Power 37.3 dBm (5.4W)
- High Efficiency 73%

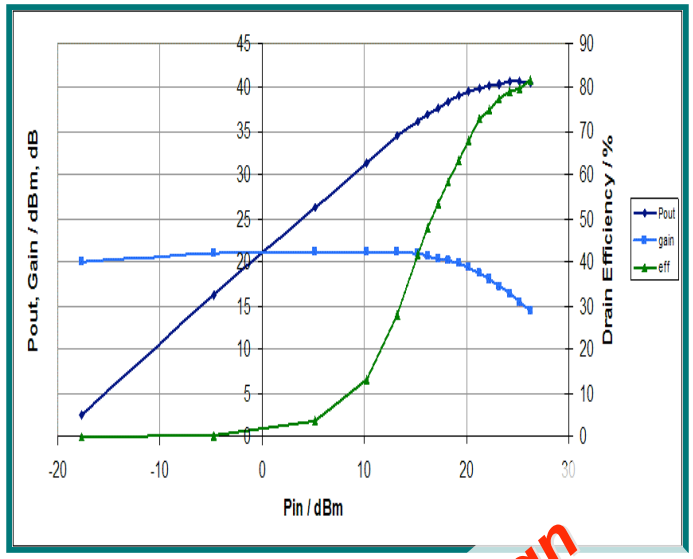
10W GaN HFET @ 900 MHz

- Inverse Class F clearly achieved
- High Power 40.8 dBm (12W)
- High Efficiency 81.5%

12W Inverse class-F Amplifier Realisation

– right first time design using CREE 10W device





- *'Right first time'* waveform based design through the realisation of a high-performance inverse class-F PA
- Impressive efficiency of 81% at high output powers
- High Power achieving 12W form a 10W device

Inverse Class-F PA Performance Summary	
Max. Pout:	41.6dBm
Max. Gain:	21.2dB
Compression @max. Pout:	Approx. 5dB
Max. Drain Efficiency:	81.8%

First Pass Design Success

RF Waveform Measurement and Engineering

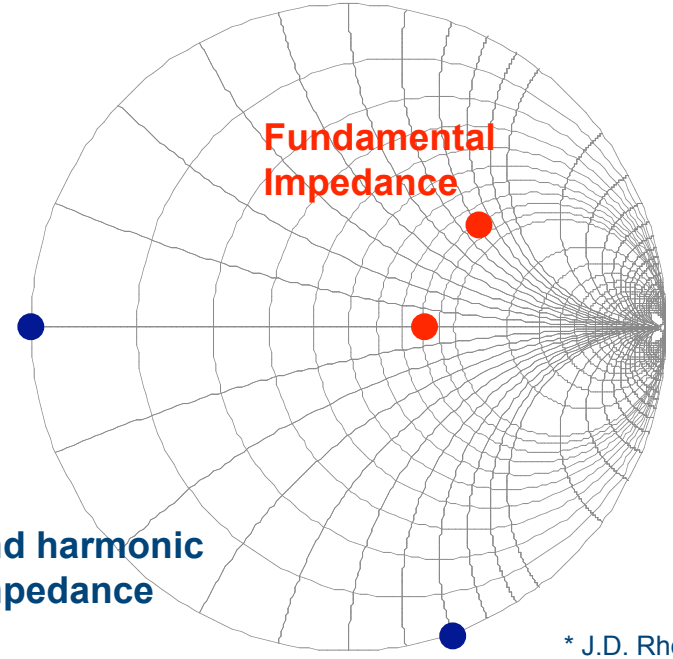
- powerful dynamic transistor amplifier design tool

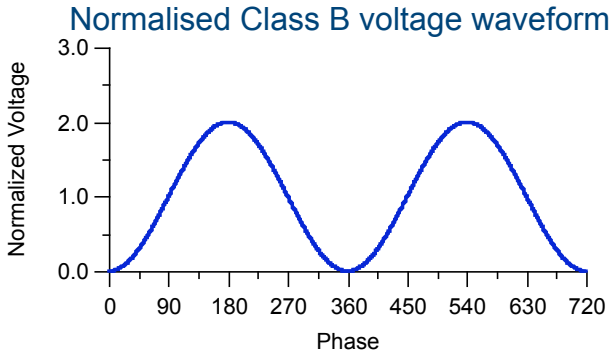
- Investigation of "New Design Space"
  - Use RF Waveform Measurement and Engineering Systems to stimulate new theoretically investigations in alternative high efficiency modes of operation
  - Move beyond the discrete design point thinking to design continuum thinking
  - The Class B to Class J Continuum
    - New Theory
    - Improved Bandwidth

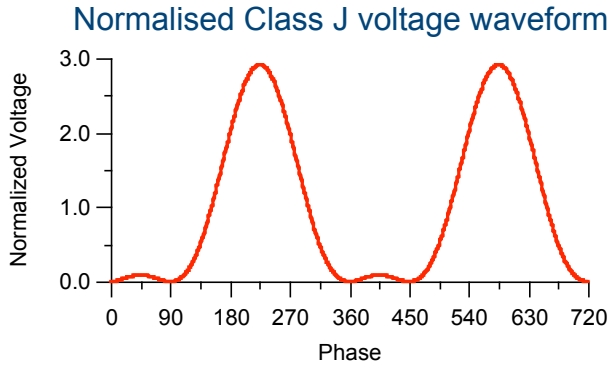
RF Waveform Measurement and Engineering

- provides for new theoretical insight

- Consider the Class B and Class J Mode of operation
  - Both have a half rectified current waveform
  - Both have the same theoretical power and efficiency values
  - But have very different voltages waveforms
    - Different fundamental and 2nd harmonic reactance's







- Are these not just different solutions of the same mode?
  - Rhodes* provide some mathematical insight
    - Optimum fundamental reactance is mathematical defined by harmonic reactive terminations

* J.D. Rhodes "Output universality in maximum efficiency linear power amplifiers" International Journal of Circuit Theory and Applications, volume 31, 2003, pp.385-405

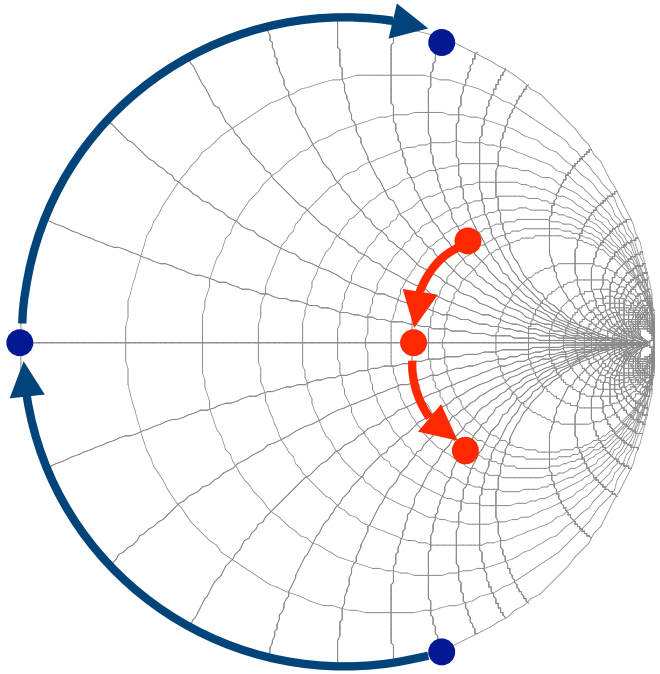
RF Waveform Measurement and Engineering

- provides for new theoretical insight

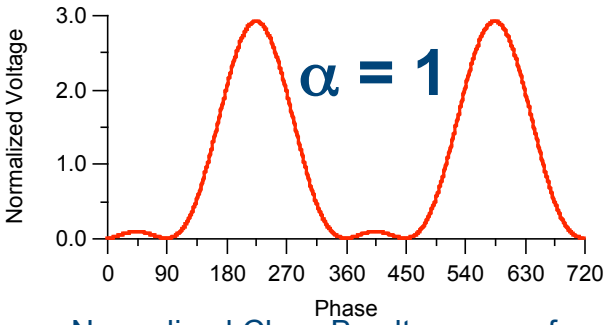
- They are just different solutions of the same mode?
  - The Class J - Class B - Class J* Continuum

$$v(\theta) = (1 - \beta\cos\theta)(1 - \alpha\sin\theta), \quad (-1 < \alpha < 1)$$

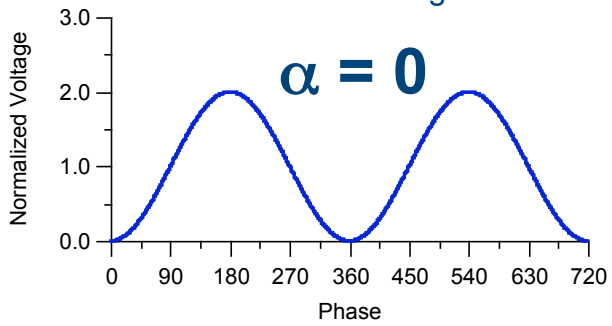
  - Many more possible solutions



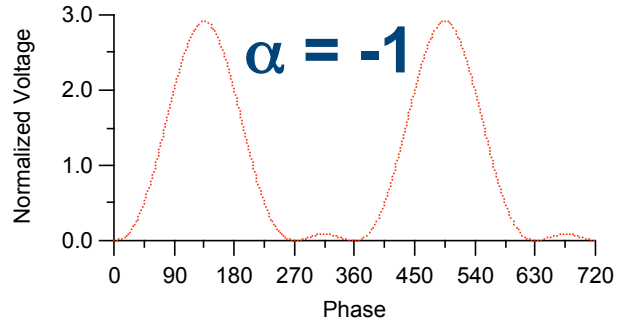
Normalised Class J voltage waveform



Normalised Class B voltage waveform



Normalised Class J voltage waveform



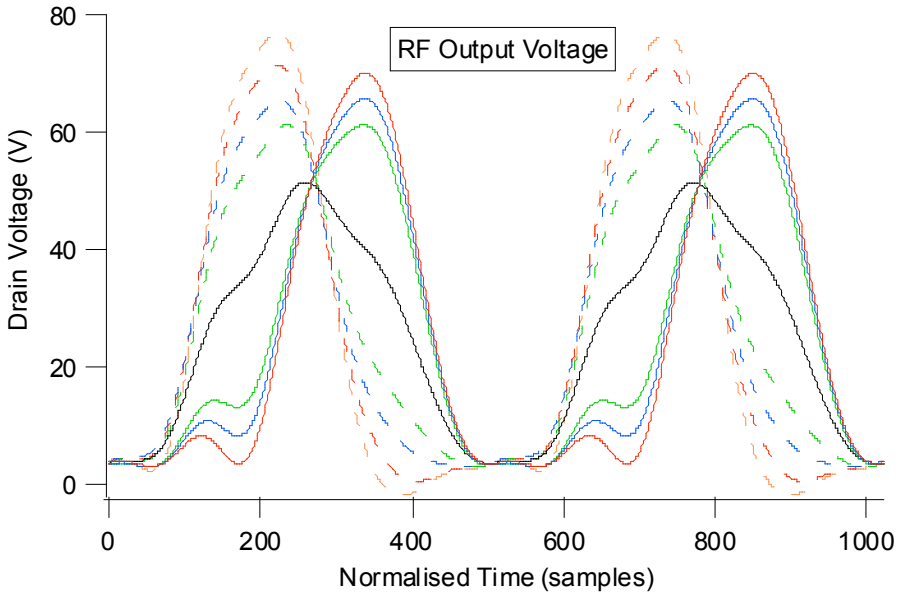
RF Waveform Measurement and Engineering

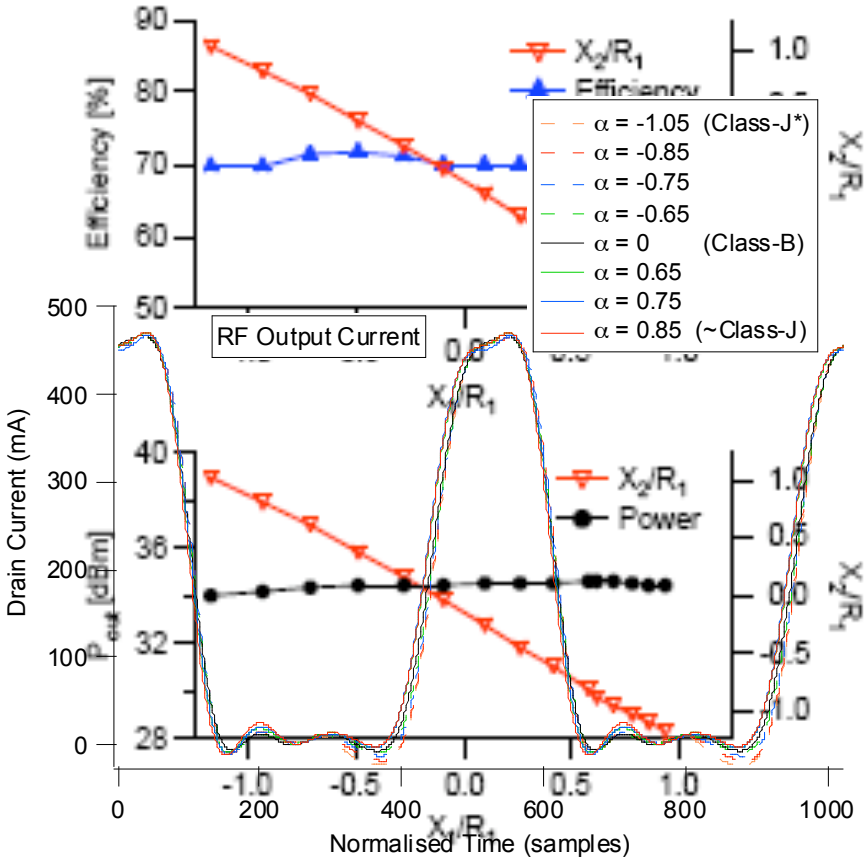
- experimental validation of new theoretical insight

$\alpha = X_1/R_1 = -X_2/R_1$

On Cree 2W on-wafer device:

- Maintain constant P_{in} to device
- Vary $Z(f_0) = R_{opt} + j\,k\,R_{opt}$
- Vary $Z(f_2) = -j\,k\,R_{opt}$ $\quad -1 \le k \le 1$



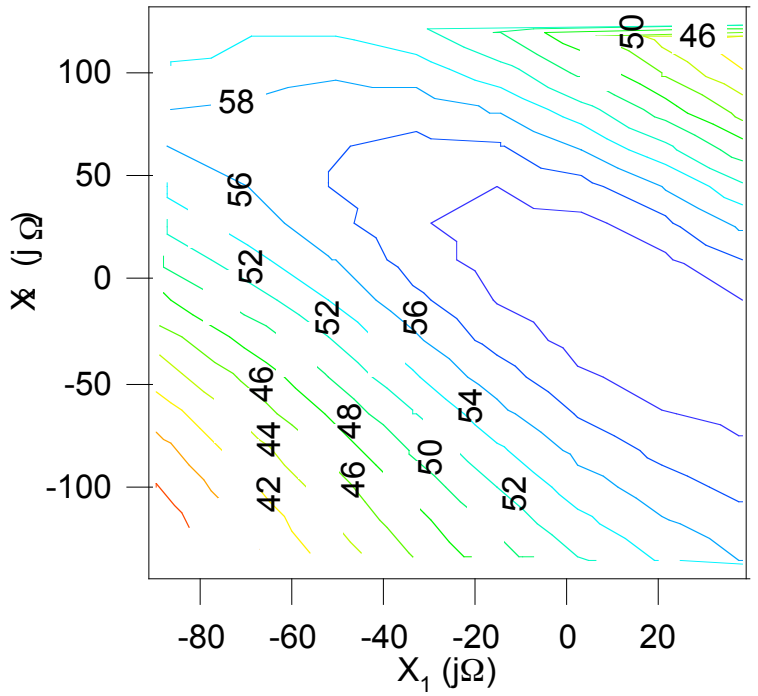


RF Waveform Measurement and Engineering

- Class J-B-J Continuum Sensitivity Analysis*

On Cree 2W on-wafer device:

- R_1 held to R_{opt}, R_2 held to 1.5Ω
- X_1 and X_2 were swept to examine the impact of the deviation off the Class-JB continuum contour



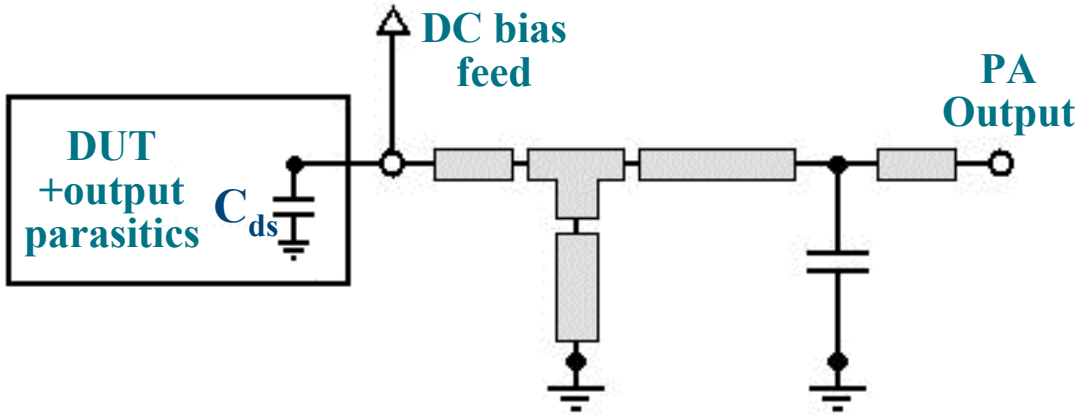
Results

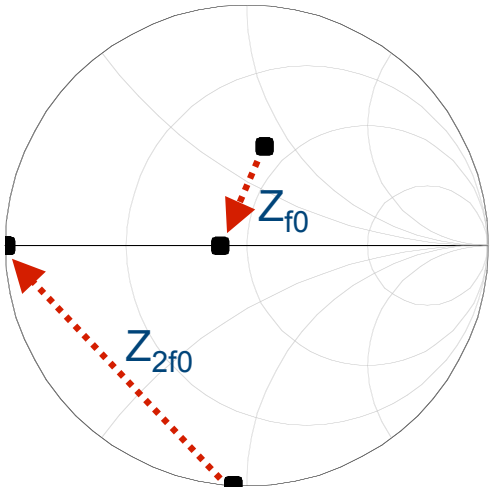
- Class-JB continuum visually identifiable with a high efficiency contour
- Roll-off of efficiency is greater for a deviation in fundamental load compared to second harmonic

Increased design flexibility

Realising Class-J Matching

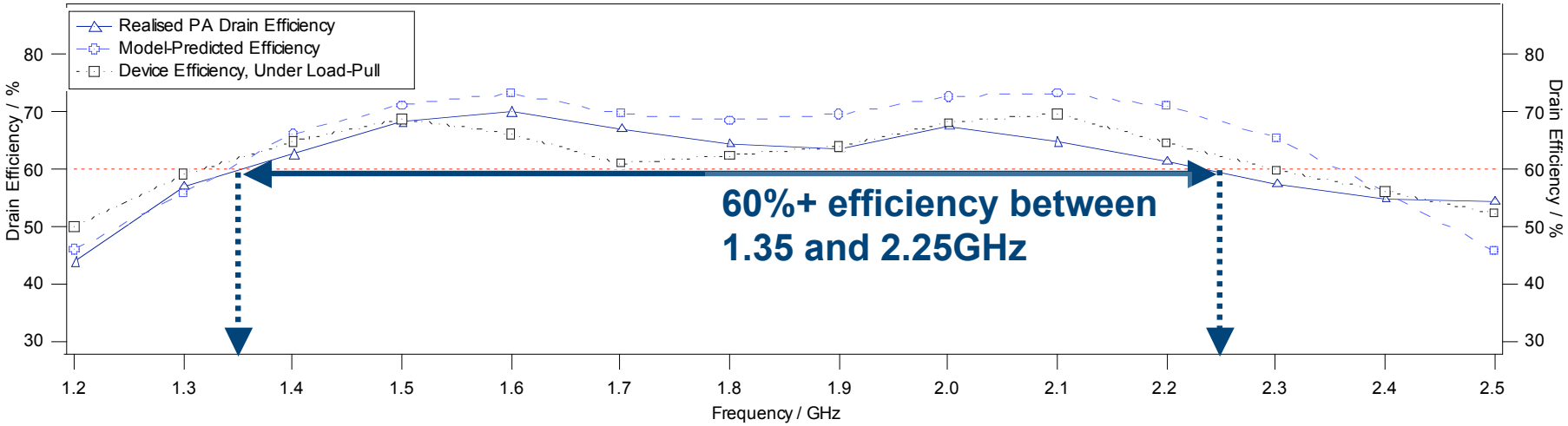
Class-J output matching schematic:





- Compromises need to be made/considered across this size of bandwidth.
- **Fundamental load impedance matching given priority.**
- Second harmonic already close to optimum class-J reactance at centre frequency of desired bandwidth as a result of output capacitance C_{ds}
  → **Z_{2f0} allowed more latitude during the design.**
- Shunt shorted-stub increases the effective capacitive reactance of second harmonic load at lower frequencies.

Performance of PA Prototype (1st it.)

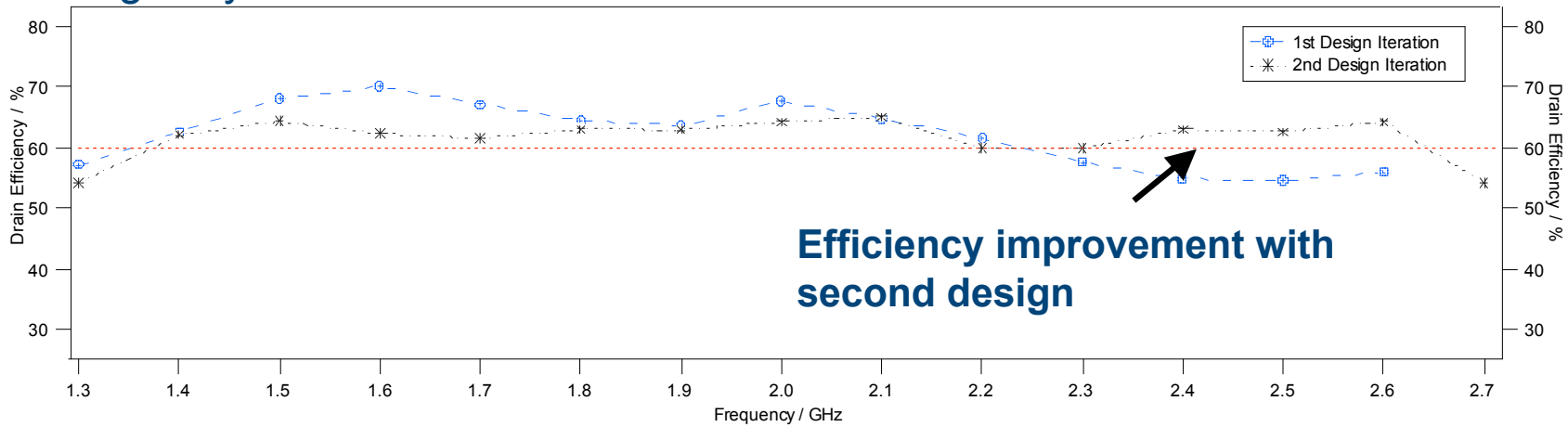


- The PA shows a measured 60%-and-above drain efficiency across the frequency range 1.35-2.25GHz.
- **Drain efficiency measured for PA, model simulation and load-pull emulation.**
- Closely agreeing results with the load-pull emulation.
- **Output power across this same bandwidth is 9-11Watts (device-rated power).**

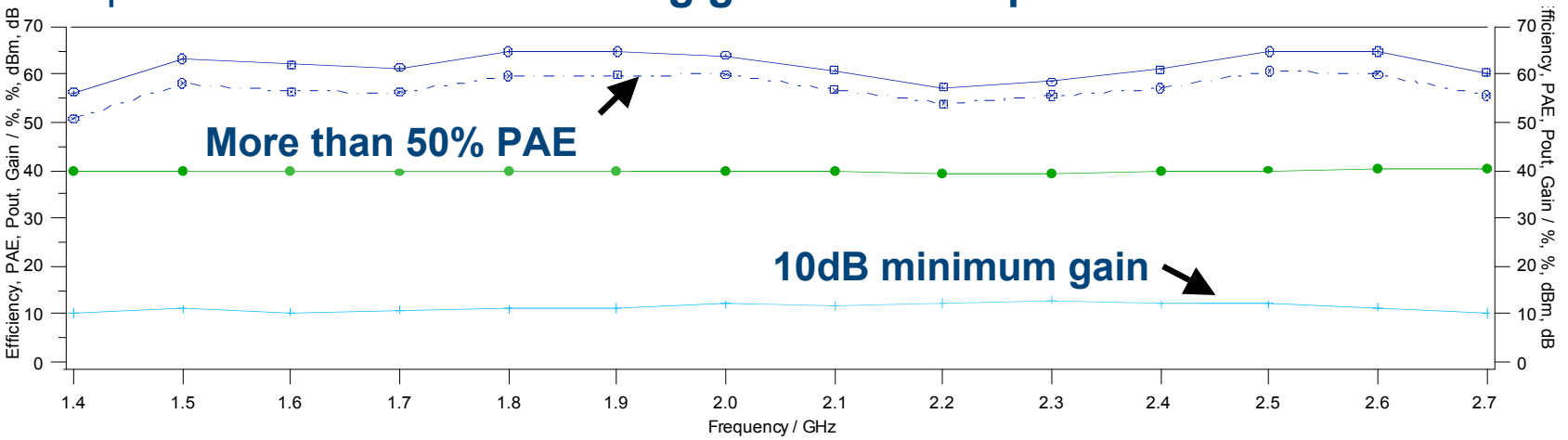
Proposed bandwidth not met entirely, but still a 50% bandwidth PA achieved.

Performance of PA Prototype (2nd it.)

- Second design iteration extending high-efficiency operation across the originally intended PA bandwidth of 1.5-2.5GHz



- Input matched PA → **Resulting gain and PAE profiles**

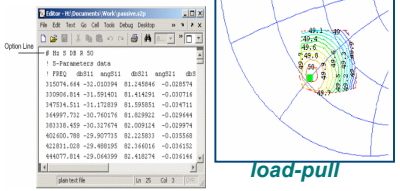


RF Waveform Measurements and Engineering

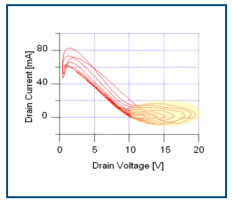
– a powerful tool and concept

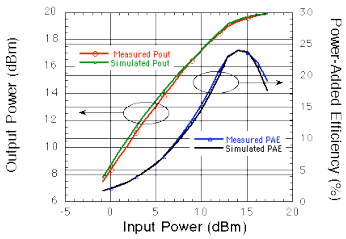
Device Technology → Circuit Design/Emulation → System Application

Design/CAD Tool

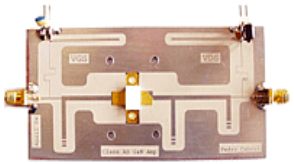


Analysis Tool

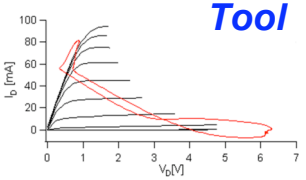


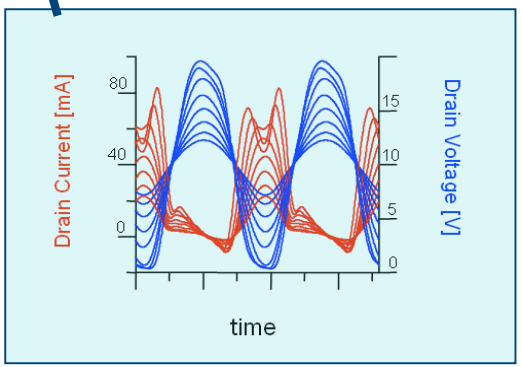


Circuit Emulation

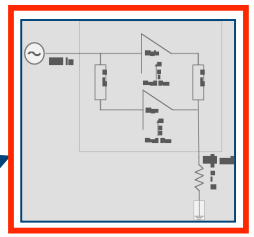


Design/Evaluation Tool





Doherty PA



Waveform are the unifying link between device technology, circuit design and system performance