

RF IV Waveform Measurement and Engineering - Emerging Multi-Tone Systems -



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- Demand for Multi-Tone Excitation
 - Synthesize "real" system stimulus







- Demand for Multi-Tone Excitation
- CW (Single Tone) to Modulated (Multi-Tone) Measurement System Development
 - RF Multi-Tone I-V Waveform Measurement
 - Intelligent Sampling
 - Inclusion of IF (Base-band signals)
 - RF Multi-Tone IV Waveform Engineering
 - IF (Base-band) active load-pull
- Application
 - Memory Investigations: Base-band Electrical Memory
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 - RF active load-pull (Digital ELP)



- Multi-Tone Measurement Requirements

- Need to extend sampling strategy to accommodate multi-tone excitation
 - folded and interleaved sampling
- Need test-set architecture to account for all frequency components
 - RF hardware between DUT and the sampling receivers ignores base-band components





- Intelligent Sampling: Review CW Case

• CW Period Stimulus on a Specific Frequency Grid

- Sample over many RF cycles (M.P + C.Prime)
 - M is the number of RF cycles contained within the sample period
- Engineer Sampling T_s=M.T_{rf} + C.Prime.T_{rf}/P (P=sampled points, C=cycles),
 - Multiple solutions $f_{rf} = f_s.(M.P+C.Prime)/P$ are sampled into Fourier location C
 - If Prime (prime number) is greater than 1, time interleaving also occurs
- Independently Engineer the Fourier location of frequency components





- Intelligent Sampling: Multi-Tone Case

- Multi-Tone Period Stimulus
 - Sample over many modulated RF Cycles
 - Independently engineer Fourier location of carrier (and harmonics) and modulation (and distortion)

• $T_s = N.T_{mod} + T_{mod}/P$ thus $f_{mod} = f_s.(N.P+1)/P$ (Fourier Location 1) • $T_s = M.T_{rf} + C.T_{rf}/P$ thus $f_{rf} = f_s.(M.P+C)/P$ (Fourier Location C)





- Multi-Tone versus CW





Non-Linear Vector Network Analyzer:

- Basic Architecture with RF and IF Test-set

- Requires a very broadband four channel receiver
- Utilizes integrated RF and IF directional couplers for detection/separation of waves
 - Critical components
 - Bias Tee/Diplexer
 - Bias-Tee/Combiner
 - IF Bis-Tee

Measures RF & IF a_n(t) and b_n(t) time varying Voltage Travelling Waves





- Need for IF Measurements



Waveform measurements necessitates all spectral components

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RF I-V Waveform Measurement & Engineering

- Classical IF Measurements and Data Presentation



- Classical 2-tone often used
- Observation of IM magnitude and <u>symmetry</u>
- Limitation Little insight into sources of memory – just the consequences
- Traditional Instrumentation Spectrum Analysers,
- New Instrumentation VSA, and recently PNA-X



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RF I-V Waveform Measurement & Engineering

- Non-Classical IF Measurements and Data Presentation

- What is envelope domain analysis
- Powerful approach intuitive
 - Critical to to capture all significant spectral components
 - DC, Baseband and RF spectra then used to 'rebuild' the modulation envelope.
 - Mag and Phase information key in this process.



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RF I-V Waveform Measurement & Engineering

- Non-Classical IF Measurements and Data Presentation





- Investigation Linearity Issues (i.e. Memory)

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Realization of IF (Base-band) Engineering

- initial focus on bias circuit electrical memory issues





Realization of IF (Base-band) Engineering

- initial focus on bias circuit electrical memory issues





- Effect on RF Carrier Output Power (HBT)





Control of interaction of output dynamic waveforms with knee region explains carrier Power and efficiency sensitive to IF load impedance.



- Effect of Amplitude on Intermodulation Distortion (HBT)



Control of interaction of output dynamic waveforms with knee region explains intermodulation sensitive to IF load impedance.



- Effect of Amplitude on Intermodulation Distortion (HBT)





- Effect of Phase on Intermodulation Distortion (HBT)



Mixing of transfer and output non-linearities caused by interaction of dynamic output waveforms with knee region explains sensitivity to IF load impedance. **19**



- Effect of Phase on Intermodulation Distortion (HBT)





IF Input Voltage Engineering (Pre-distortion)

- Effect on RF Carrier Output Power (HBT)





Waveform shape explains carrier power and efficiency sensitive to IF source impedance.



IF Input Voltage Engineering (Pre-distortion)

- Effect on Intermodulation Distortion (HBT)



 $i_o(t) = a_0 + a_1 \cdot v_i(t) + a_2 \cdot v_i(t)^2 + a_3 \cdot v_i(t)^3$ Transfer function explains intermodulation sensitivity to IF source impedance



IF Input Voltage Engineering (Pre-distortion)

- Optimization of Linearization Process (HBT)



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Realization of IF (Base-band) Engineering

- continue focus on bias circuit electrical memory issues





Linearity and Memory Investigations: - 20W Si LDMOS





- Optimum IF termination to simultaneously minimize IMD3 and IMD5





- Optimum IF termination to simultaneously minimize IMD3 and IMD5

Do these identified optimums change with tone-spacing?



- Indications are that the optimum IF impedances is independent of modulation frequency
- These impedances can be easily synthesised using an ET process



- Envelop Domain: Linearity Investigations





- Demystifying Memory: Envelop Domain Simulations

- 27ps delay line used as DUT
- 2-tone excitation
- 80 MHz tone separation used
- imparts 0.8 degree phase shift onto the envelope







- Demystifying Memory: Active Device Measurements

Device specifics

2W GAN Cree die. Fmax 40 GHz, gate width: 2x360um gate length 0.45um, Transit time 2.2ps Gm=180uS.

Observations

- Dynamic trajectories are well aligned with quasi-static case.
- Again, under controlled conditions, becomes possible to expose delay.
- The delay here is bigger however (~45ps) than that observed for the 27ps delay line.
- This can be explained here by transit time and charge time for intrinsic parasitics





- Demystifying Memory: Active Device Measurements

Observation

Majority of Looping can be removed by applying an approximate -45 ps linear delay to the output envelope



Observed delay can be explained (in this case) by intrinsic parasitic delay and transit time.



 $\begin{array}{c} Cgs \sim 0.72 \ pF \sim 35 \ ps \\ Cgd \sim 0.06 \ pF \sim \ 3 \ ps \\ Cds \sim 0.13 \ pF \sim \ 6 \ ps \\ Tgm \qquad \sim \ 2 \ ps \end{array}$

Total delay ~ 46 ps



- Envelop Domain: Linearity Investigations





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- consider in-band and harmonic circuit electrical memory issues





- consider in-band and harmonic circuit electrical memory issues





- Envelope load-pull solution: Envelop Tracking
 - Open loop at RF but a closed loop at envelope frequencies
 - No loop oscillations as no direct RF feedback
 - Reflection coefficient constant irrespective of the signal coming from DUT
 - Impedances set by simple electronics controlled by the X & Y inputs
 - Suitable for modulated signals





- Envelope load-pull solution: Envelop Tracking



9 Tone Modulated Signal => Confined to a few 100 kHz at present







- Envelope load-pull solution: 'Instantaneous' power sweeps





- Envelope load-pull solution: Envelop Tracking
 - Open loop at RF but a closed loop at envelope frequencies
 - No loop oscillations as no direct RF feedback
 - Reflection coefficient constant irrespective of the signal coming from DUT
 - Impedances set by simple electronics controlled by the X & Y inputs
 - Need high speed control electronics for relevant bandwidth modulated signals: Digital Solution Required





- Next generation ELP Systems: Digital control using FPGA

- DSP development board Stratix II edition
 - FPGA is Altera Stratix II clocked at 100 MHz
 - Two-channel, 12 bit, 125-MSPS A/D converter
 - Two-channel, 14 bit, 165-MSPS D/A converter
- The multi-tone measurement system is clocked by 10 MHz derived clocked from the FPGA master clock
- The control algorithm is implemented in time domain
- Frequency domain control will offer more functionality such as individual tone control
 - enable emulation of real world impedance matching network





- Next generation ELP Systems: Time Delay problem



- The control unit can support wideband stimulus albeit delay
- Phase variation over length of cable and components (group delay or envelope delay)
 - Must be compensated for accurate load impedance matching
- The repetitive nature of the measurement stimulus made delay compensation possible in the next repetition or N repetition later



- Next generation ELP Systems: Delay compensation determination

- Configurable FIFO RAM based unit delay
 - Unit delay is 10 ns (100 MHz clock)
 - Delay is compensated after 76 delay elements
 - Latest development of delay compensation is not limited to unit delay
- Linear group delay can be observed from the graph



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- Next generation ELP Systems: Digital control using FPGA using delay





- Next generation ELP Systems: Two-Tone Signal with 2MHz separation

