Foundries, MMICs, systems

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Content

→ MMIC foundries

→ Designs and trends

→ Examples

MMIC foundries

Foundries

IMST is a UMS certified design house

Memberships

MOSIS

GaAs in principal

→ 3,4 and 6 inch production

→ Target markets: High power and linearity, low noise, broad band

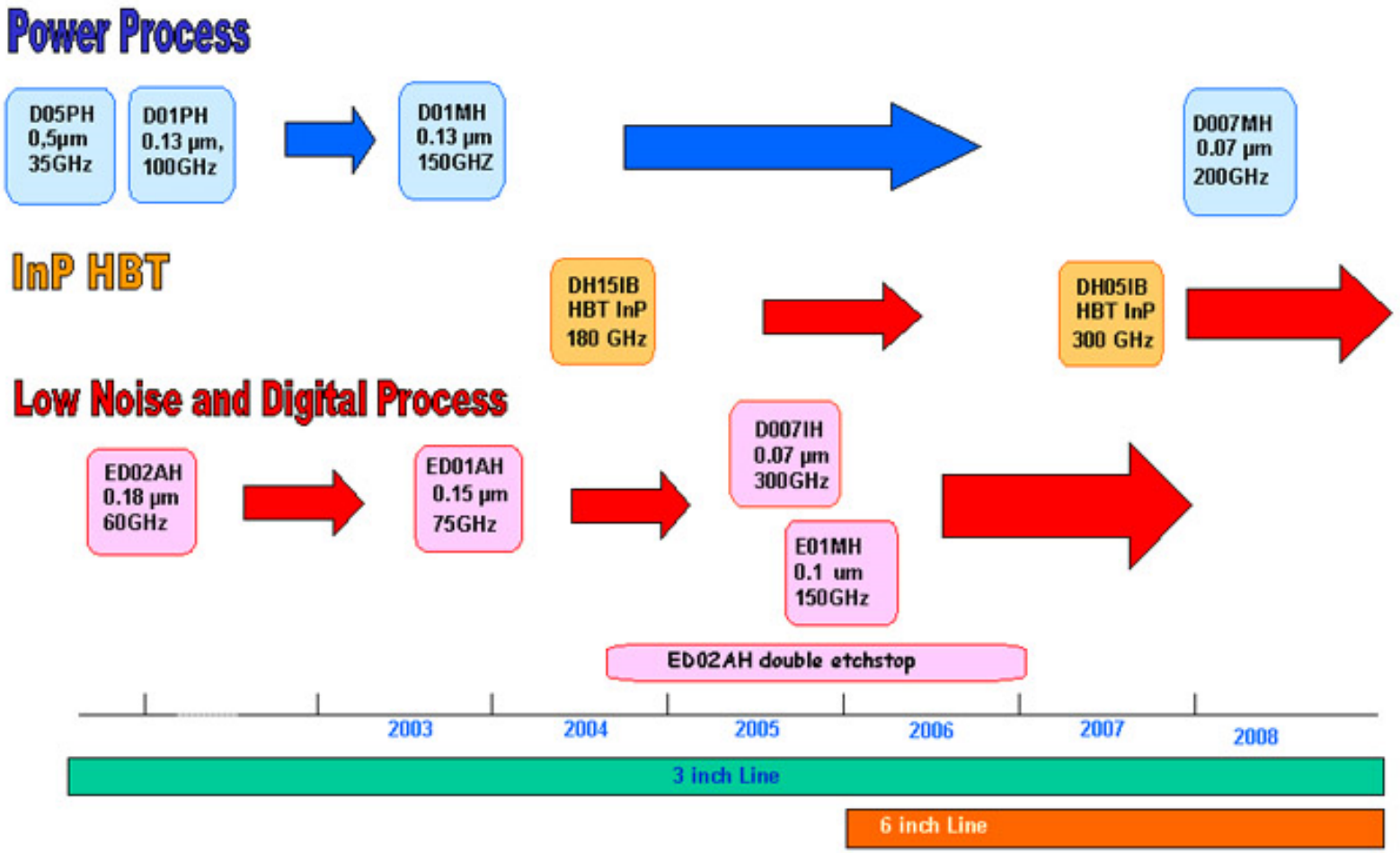
→ Specials available (e.g. E/D mode or HBT and pHEMT on same wafer)

→ Frequencies up to 100 GHz

→ Radiation hard

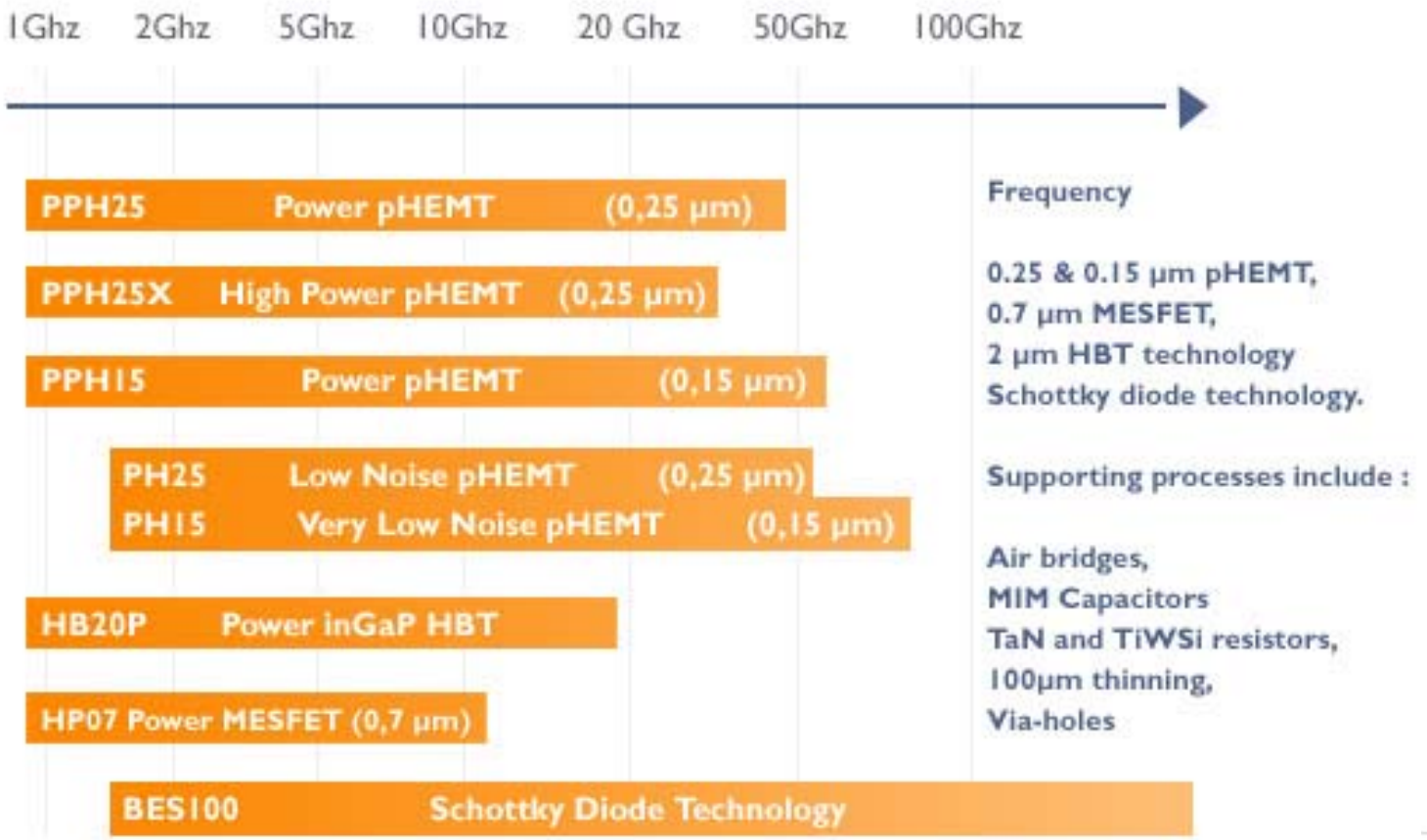
GaAs foundries

→ OMMIC, France



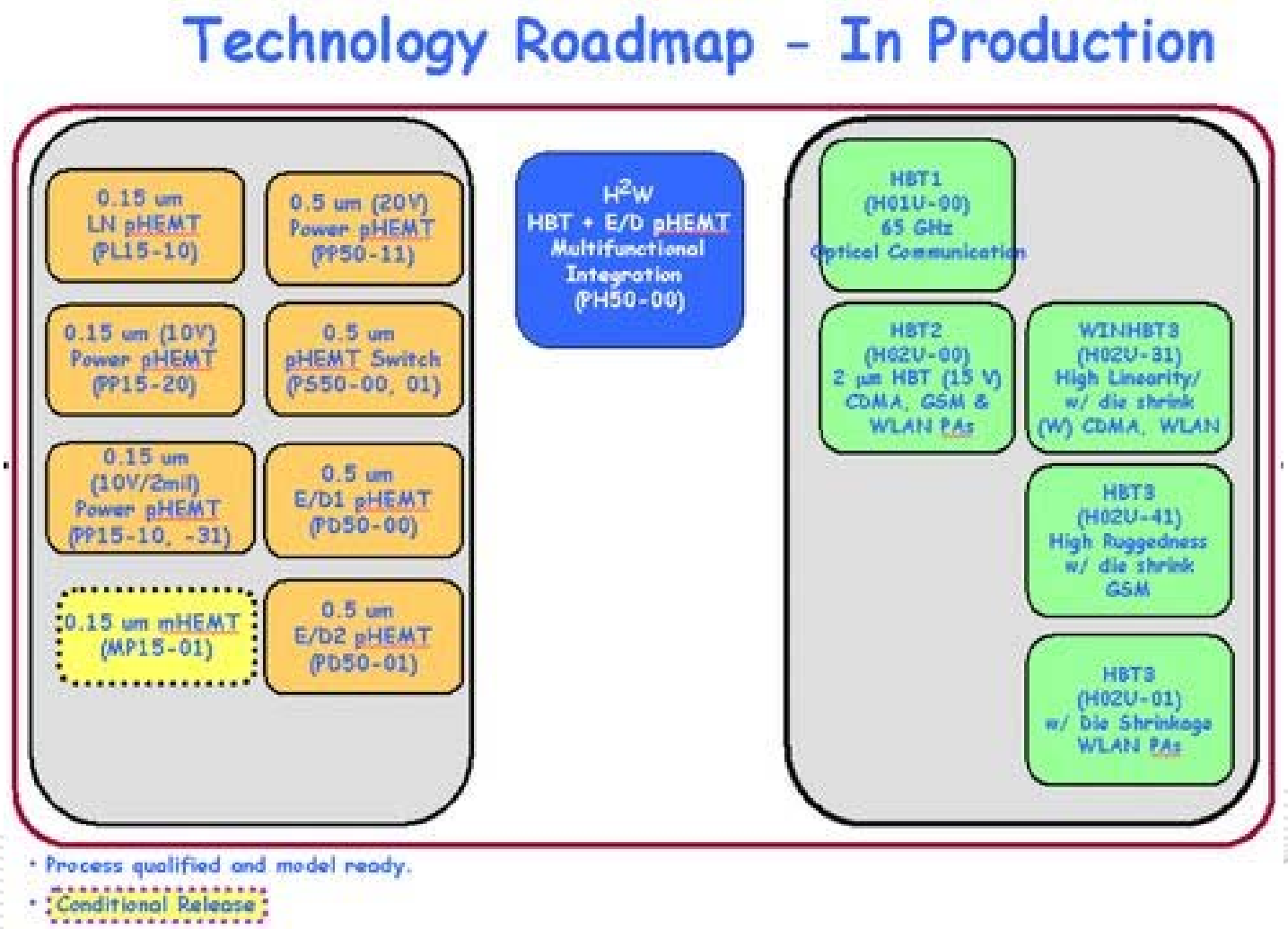
GaAs foundries

→ UMS, France (+ USA)



WIN, Taiwan

→ WIN, Taiwan



GaN

→ 4 inch to 6 inch wafers

→ Several foundries (TriQuint, UMS, Cree, Sandia and others)

→ Very high power possible

→ Defense market, radar, telecommunication

→ Single transistor devices available, very first MMICs launched (IMS 2008, Cree)

→ „Reliability“ problems

→ Frequencies up to 20 GHz and higher (100 GHz)

State-of-the-art

→ HRL examples

GaN HFET MMIC Power Amplifiers

GaN POWER AMPLIFIERS						
Part Number	Function	Frequency (GHz)	Gain (dB)	P1dB (dBm)	Psat (dBm)	Application Note
PA3C-76	High Power Amplifier	71-76	15	24	26	X
PA3C-86	High Power Amplifier	81-86	13	24	26	X
PA3C-96	High Power Amplifier	91-96	12	23.5	25.5	X

http://www.hrl.com/media/gan/gan.html

http://kiss.caltech.edu/mmic2008/presentations/micovic.pdf

Si(Ge)

→ 8 inch production

→ Combination of CMOS logic, ECL and BiCMOS

→ Frequencies up to 100 GHz

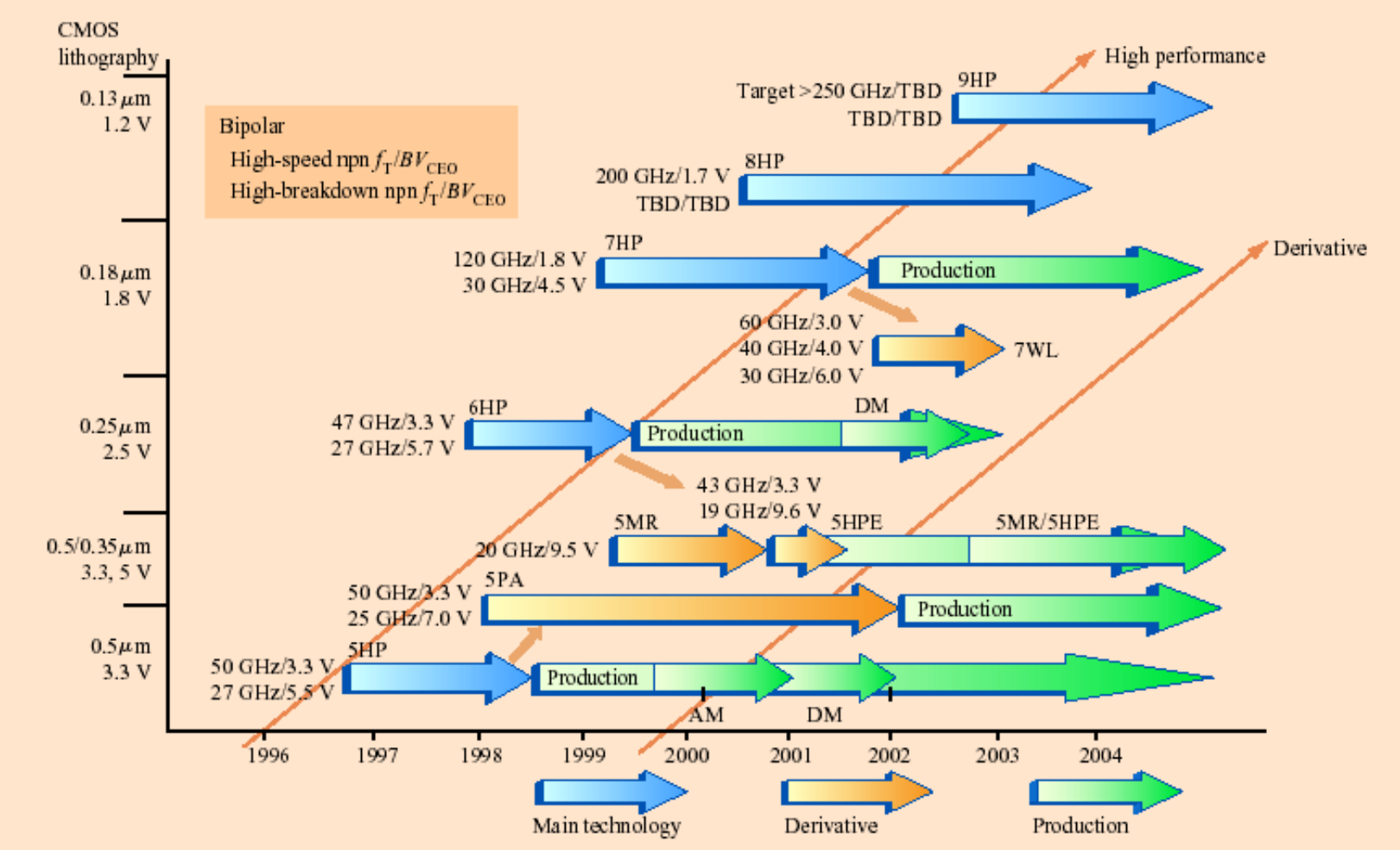
→ Complete transceiver chips possible (e.g. 60 GHz)

→ Well known foundries e.g. IBM (8HP)

→ Si LDMOS for high power

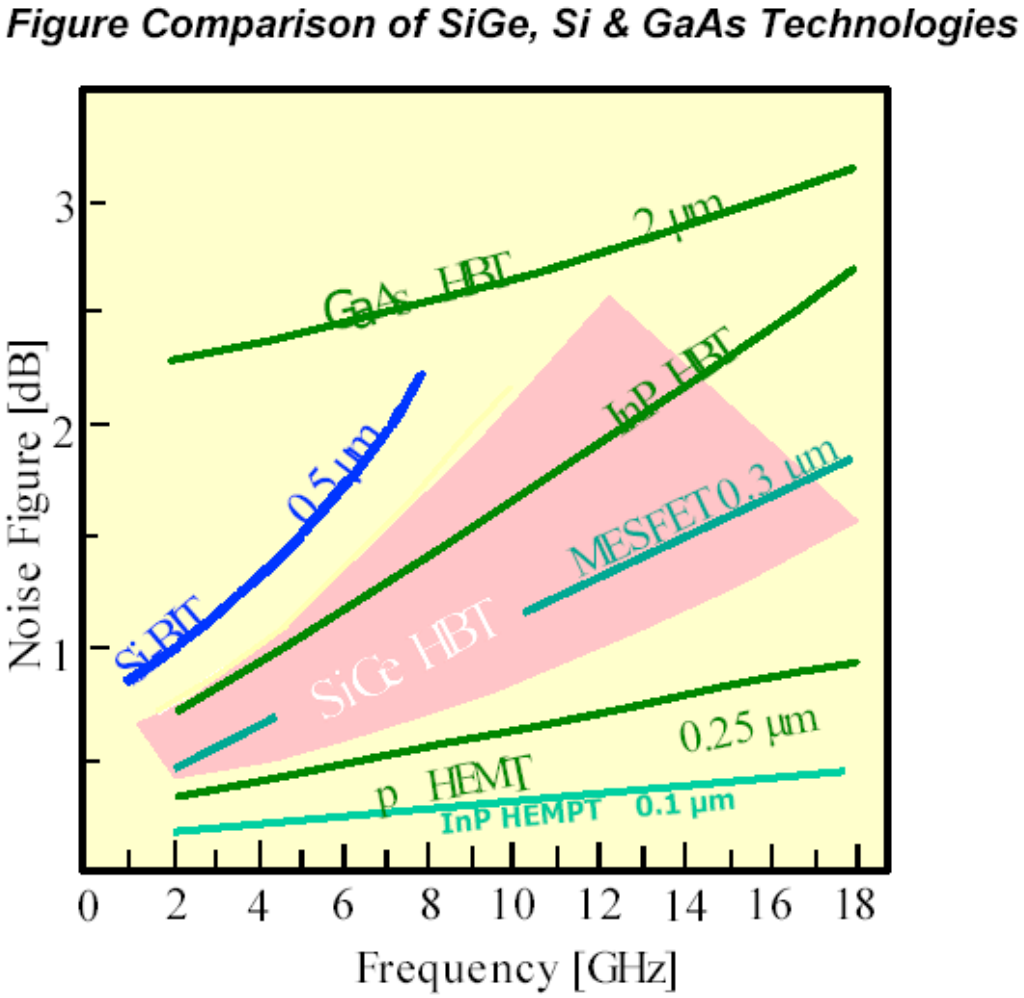
SiGe

→ IBM roadmap



Trade-offs

→ Noise figure

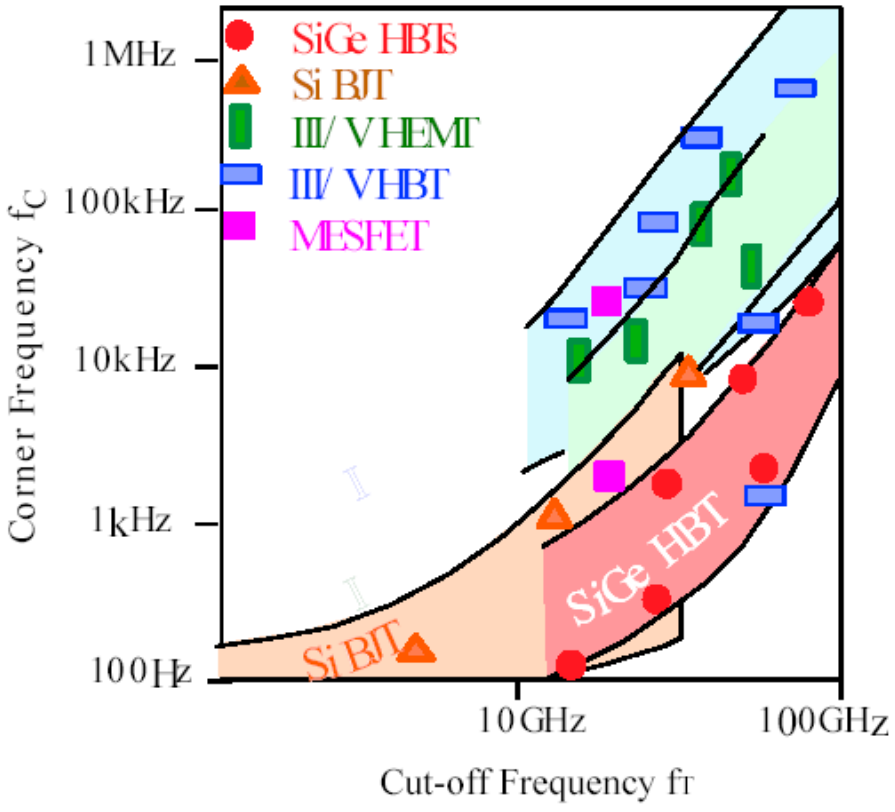


http://www.sirenza.com/pdfs/semiconductor%20technology.pdf

Trade-offs

→ 1/f noise

Low Frequency Phase Noise of SiGe, Si & GaAs Technologies



Trade-offs

→ Costs

Item	GaAs		SiGe		Units
	FET	HBT	HBT	BiCMOS	
Feature Size	0.5	2.0	0.5	0.5	µm
Starting Material	200	600	200	200	$
Mask steps	12	14	28	32	
Photo cost	1200	1400	2800	3200	$
Raw cost	1400	2000	3000	3400	$
Wafer Diameter	100	100	200	200	mm
Yield	80	70	95	95	%
Cost/mm^2	0.22	0.36	0.10	0.11	$/mm^2

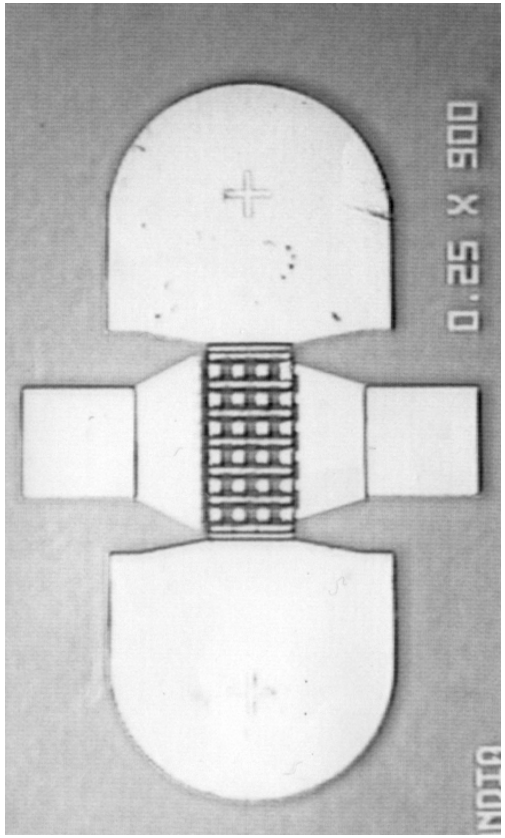
Trade-offs

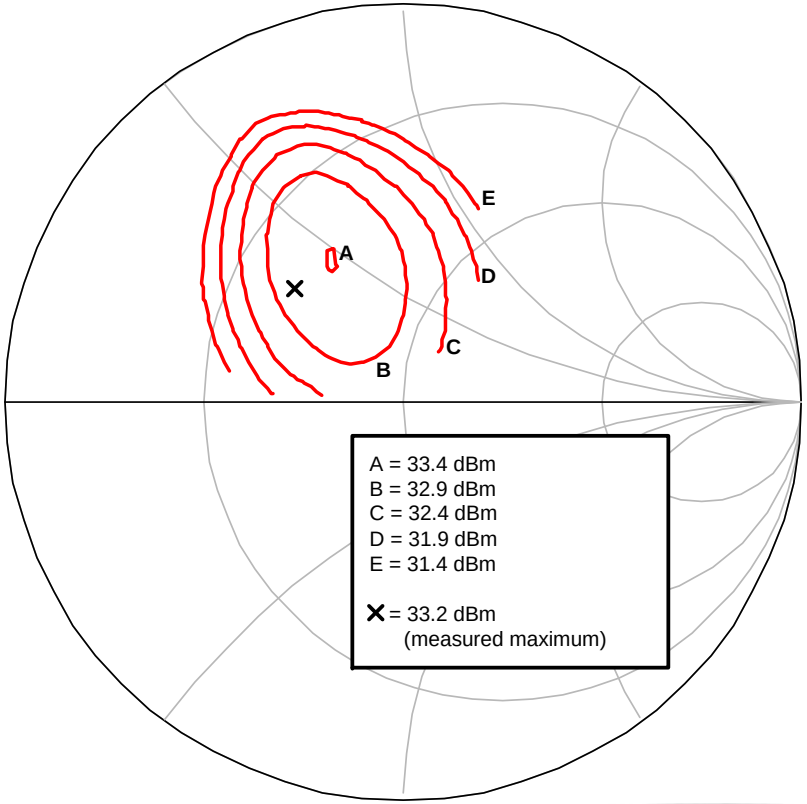
→ Power and linearity

Technology	Price/Watt	Power Density	Supply Voltage	Linearity	Frequency	PAE
Si BJT	Low Cost	Medium	26 V	Poor	<2 GHz	Low
SiGe BJT	Low Cost	Medium	<20 V	Good	>2 GHz	High
Si LDMOS	Low Cost	Low	26 V	Very Good	<3 GHz	Medium
GaAs MESFET	Competitive	Medium	12 V	Good	>2 GHz	Medium
GaAs pHEMT	Medium	Medium	8 V to 12 V	Very Good	>2 GHz	High
GaAs HBT	Competitive	High	8 V to 26 V	Good	>2 GHz	High
SiC MESFET	Competitive	Very High	48 V	Good	>4 GHz	Medium
GaN HEMT	N/A	Very High	48 V	Promising	>12 GHz	High

GaN devices

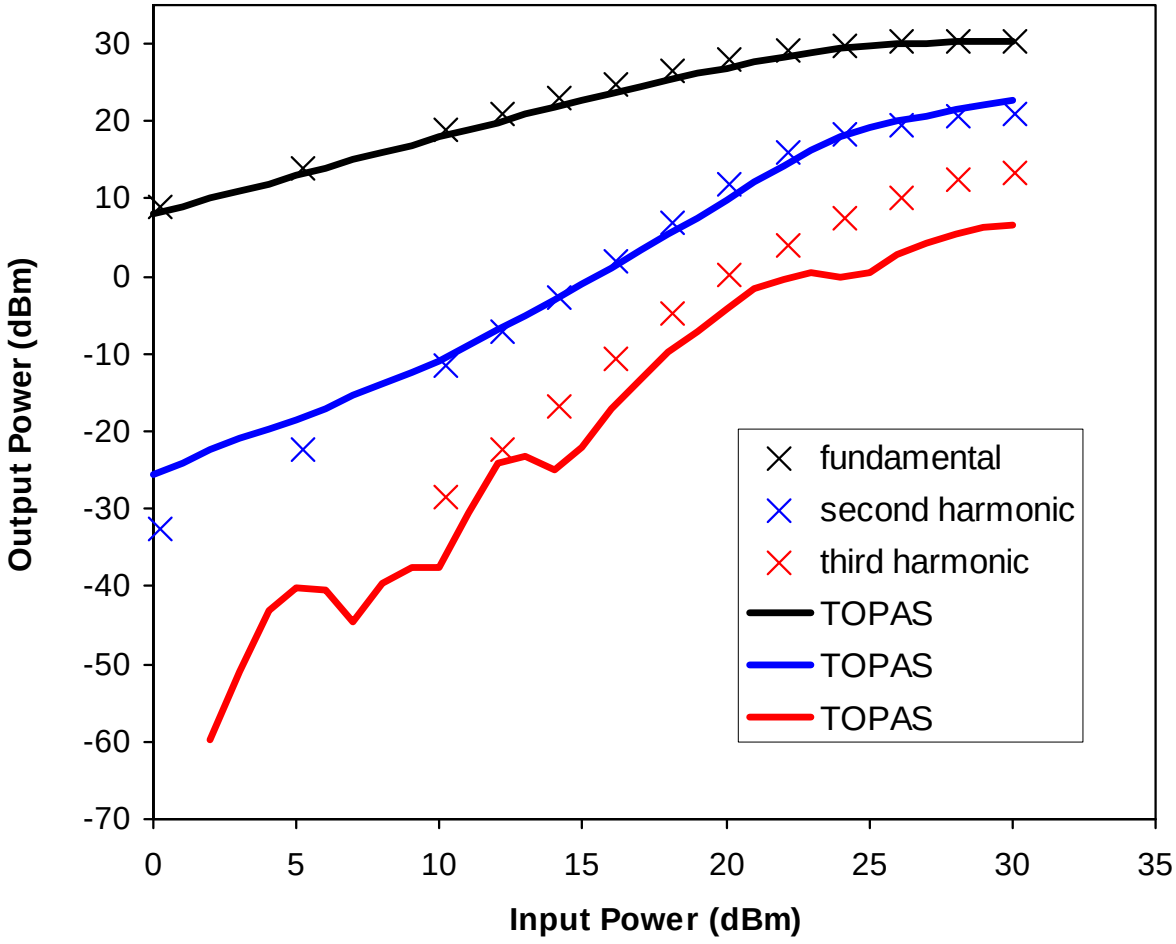
→ Non-linear model and measurement





GaN devices

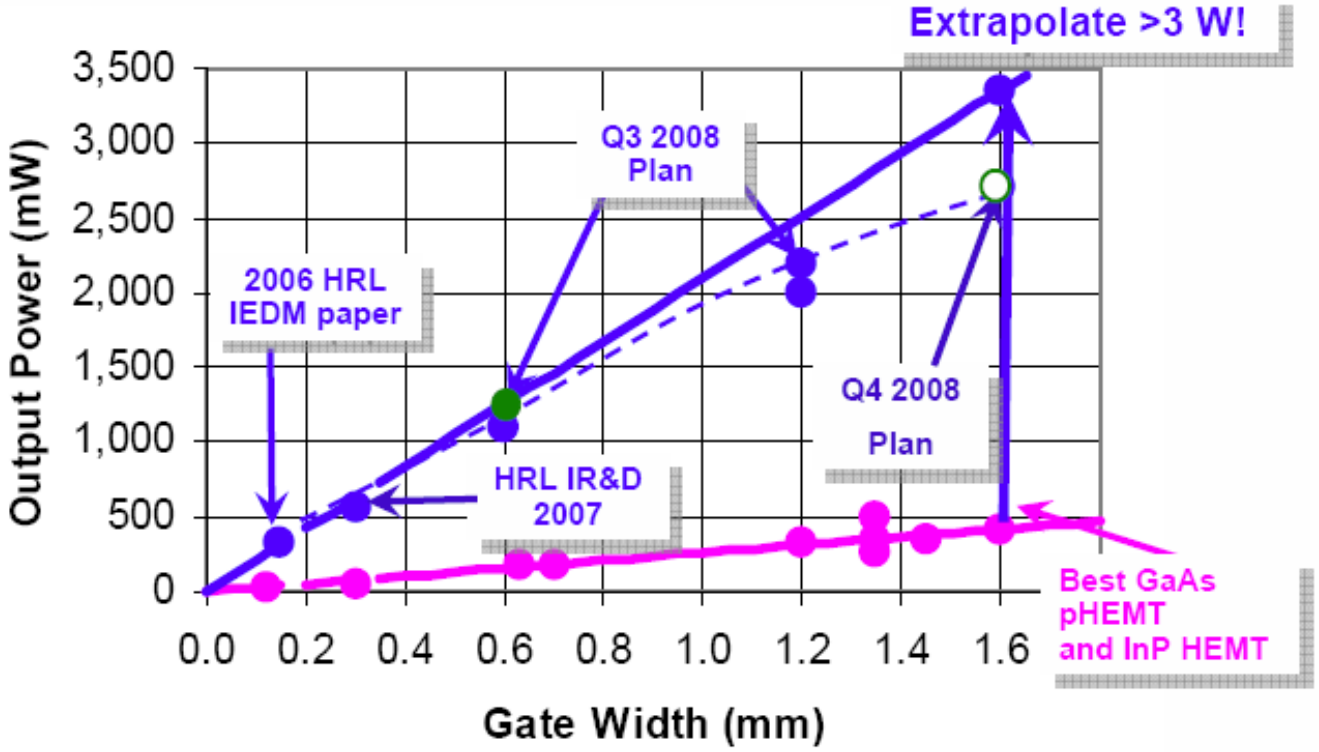
→ Model verification



GaN mmwave power

HRL LABORATORIES

HRL W-band GaN Roadmap



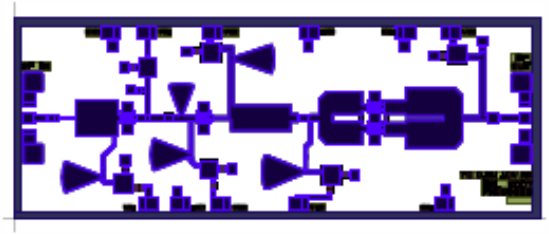
Disruptive W-band GaN Power MMICs

8X higher power density than mmW GaAs pHEMT

GaN mmwave PA

HRL LABORATORIES

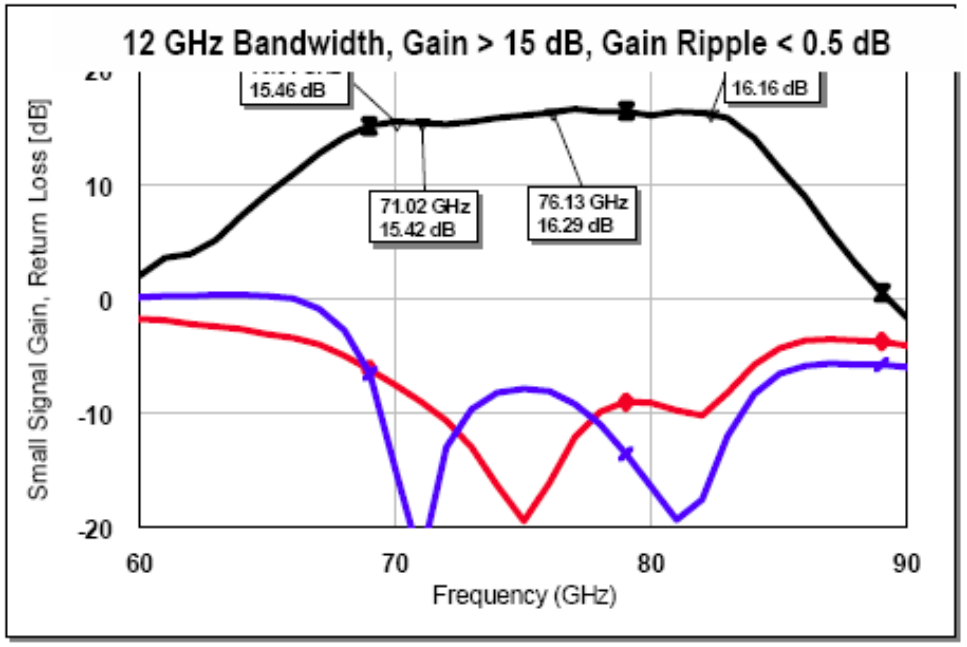
500 mW 70 GHz GaN MMIC PA



70 GHz MMIC Chip Layout
Size 3.4 mm x 1.3 mm

Operating Voltage = 15 V

Measured Gain > 15 dB



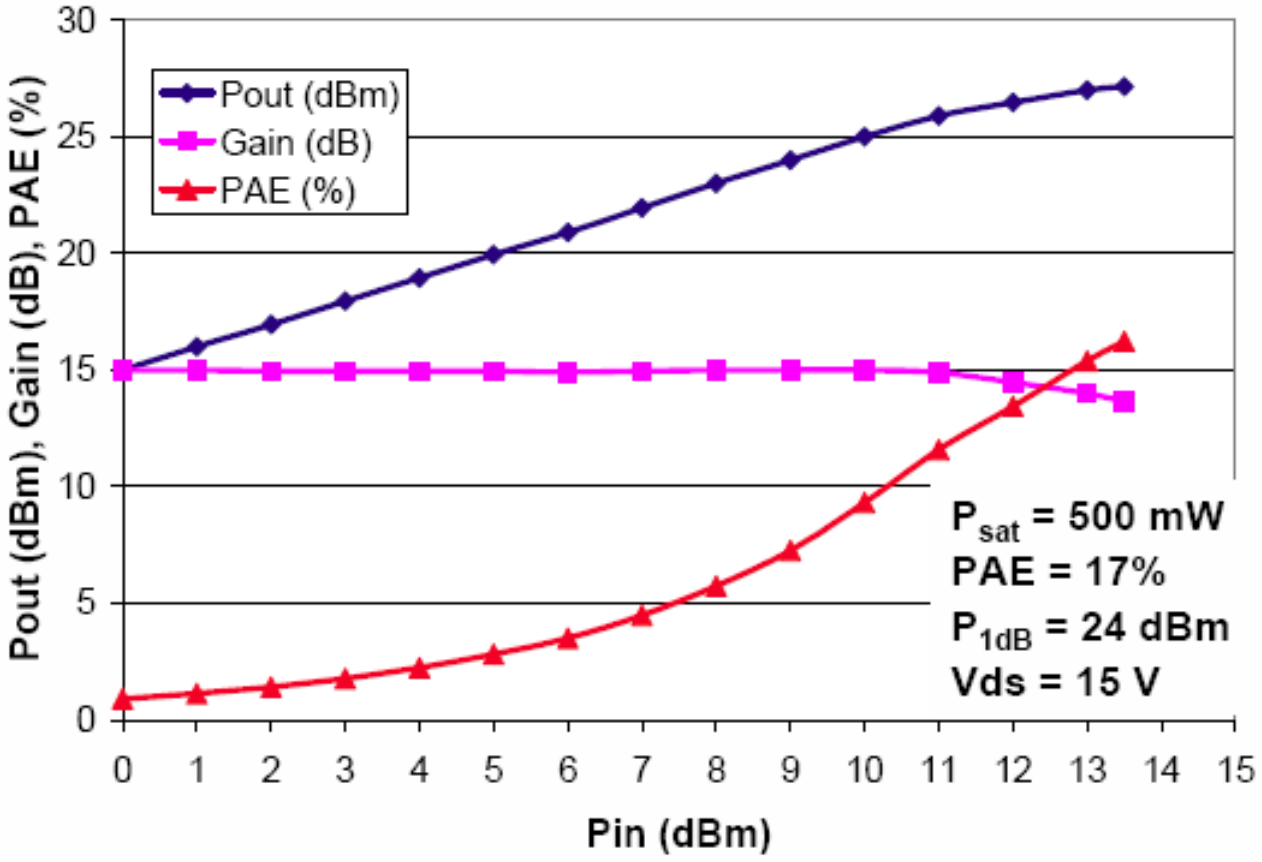
Measured small signal gain of 70 GHz 500 mW GaN MMIC PA.

Performance meets design goal.

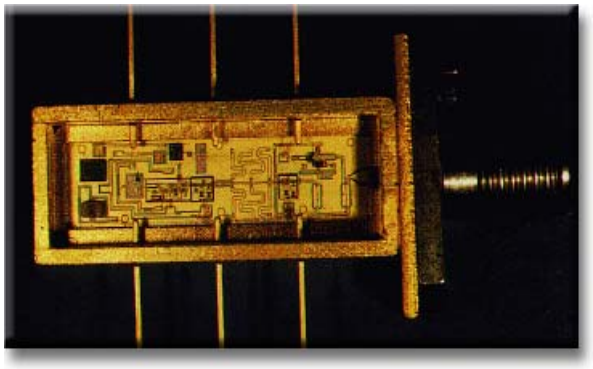
GaN mmwave PA

HRL LABORATORIES

Output power of 70 GHz MMIC measured at a frequency of 76 GHz



Integrated coplanar 24 GHz sensor

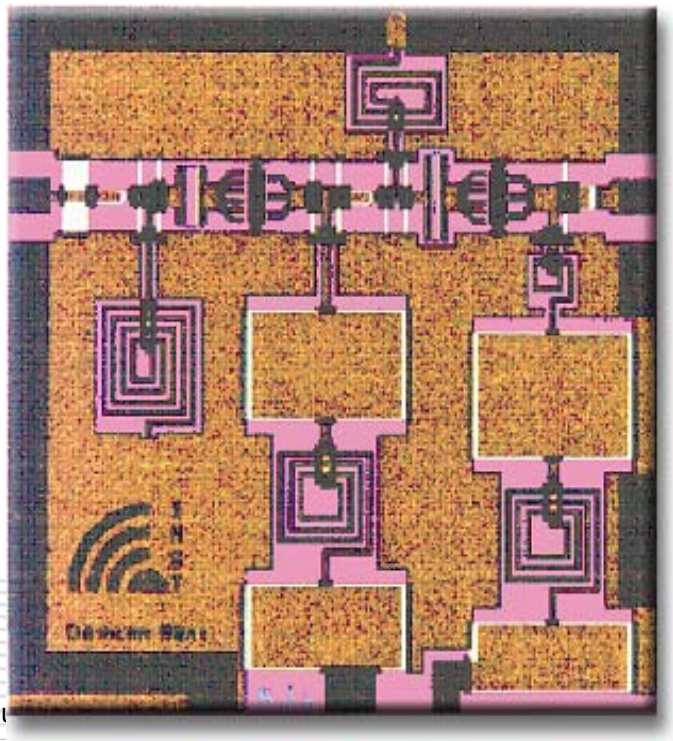


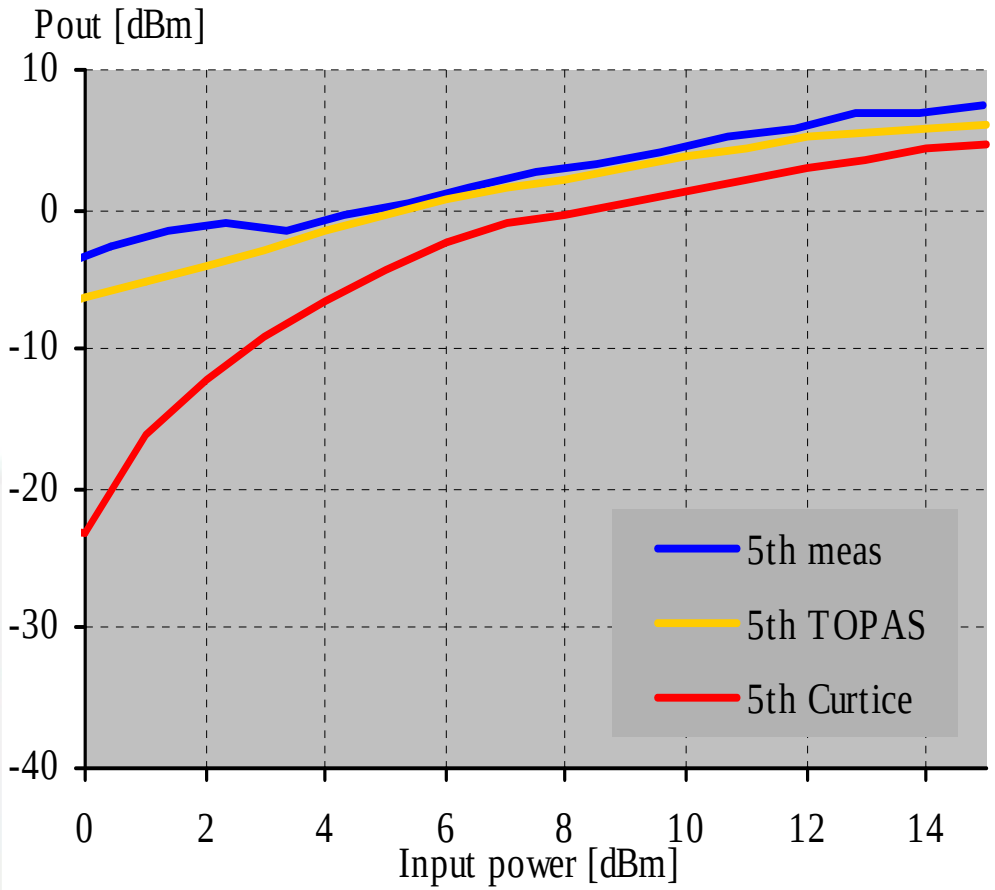
World‘s 1st 24 GHz coplanar sensor designed at IMST

Rosemount 24 GHz level sensor

Integrated GaAs circuits – 24 GHz sensor

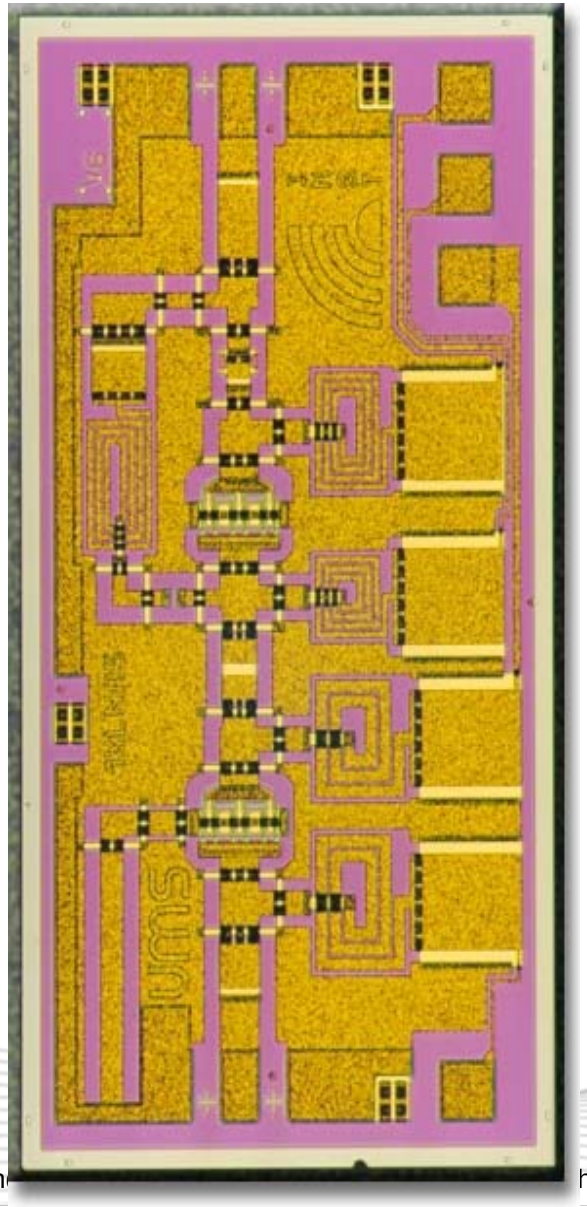
Simulated using



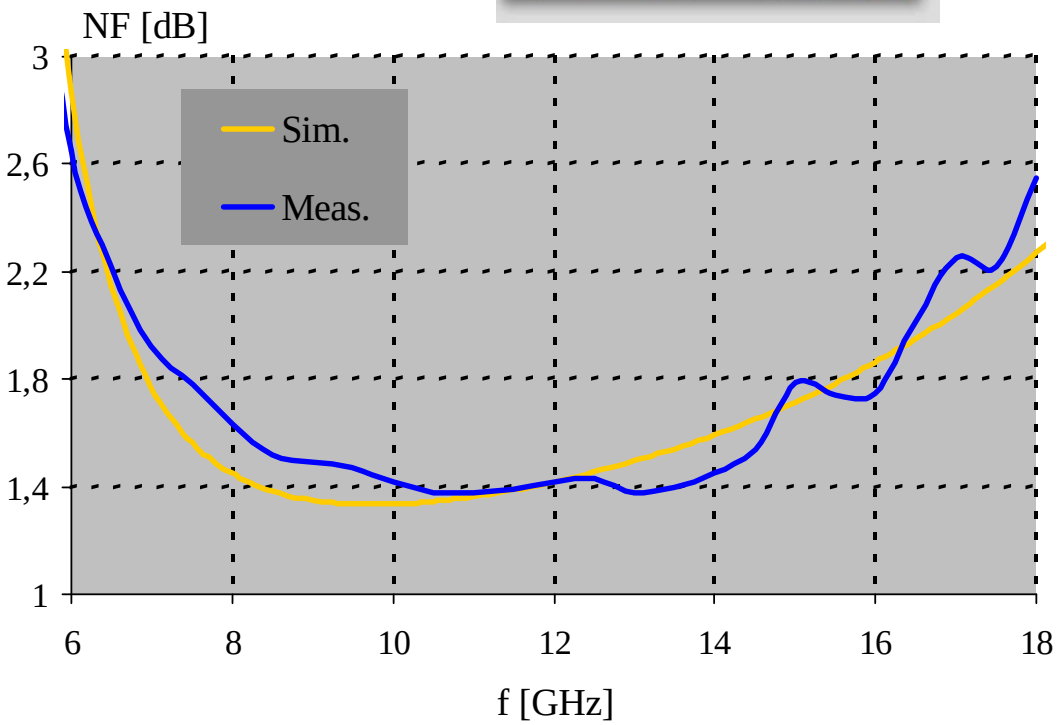


Frequency times 5 multiplier

GaAs circuits – 10 GHz LNA



Simulated using



Low noise amplifier

Core Chip Design : 2NLNA4PS2

Specifications:

- → Ku-band core chip including the 2-stage LNA and the 4-bit phase shifter
- → Technology: OMMIC - ED02AH
- → LNA bias supply: $V_{G1,2}$ = -0.2 V, $V_{D1,2}$ = 2.0 V, I_{D1} = 28.2 mA, I_{D2} = 29.0 mA
- → PS control voltages: V_C = 0 V / -2 V
- → f = 10.7 ... 12.7 GHz
- → $S_{11} \leq$ -13.3 dB (all states)
- → $S_{22} \leq$ -11.6 dB (all states)
- → S_{21} = 13.2 ... 14.4 dB (all states)
- → RMS amplitude error = 0.4 dB
- → RMS phase error = 2.6 °
- → A = 2.17 × 2.05 mm^2 = 4.45 mm^2

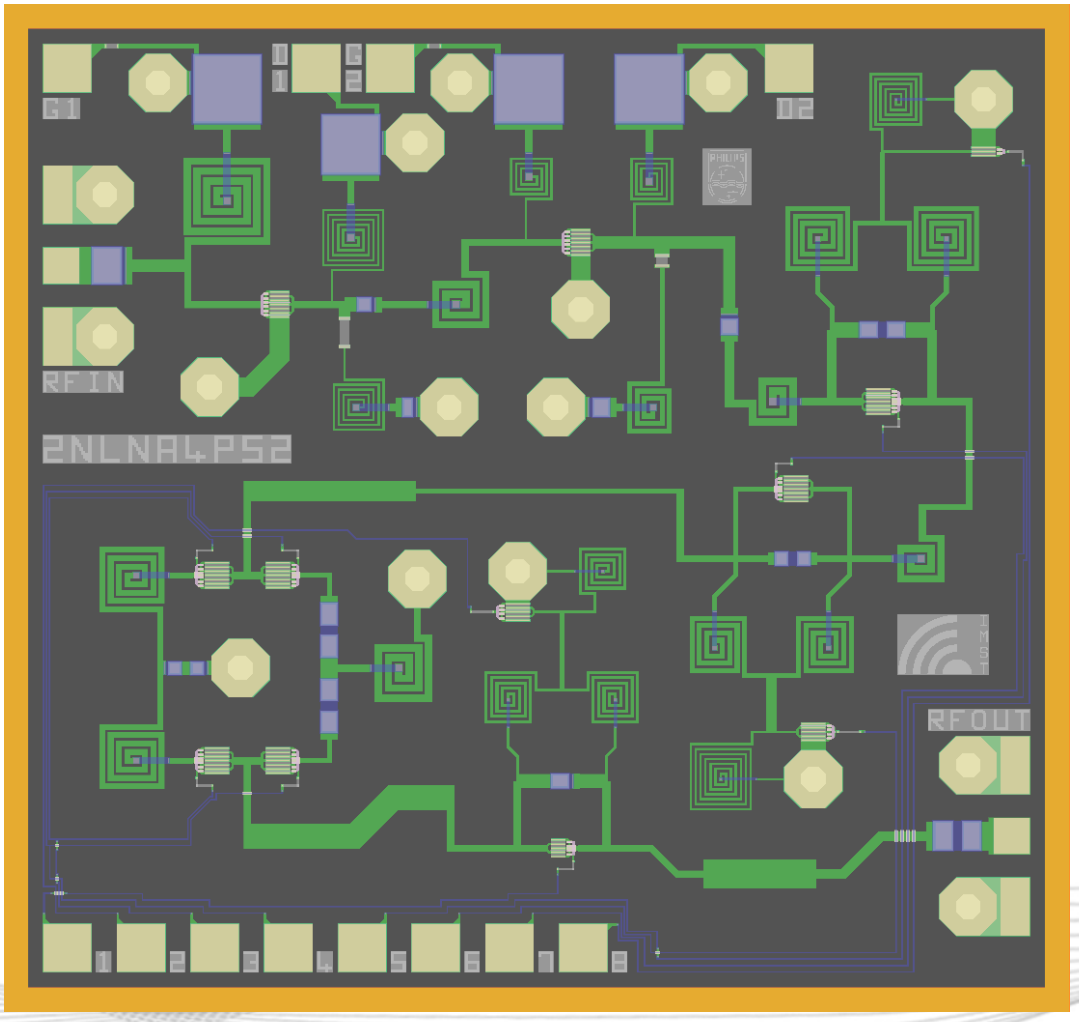
  ⇒ including half dicing street

  ⇒ including DC pads (#8) for the PS control (not necessary if using the DC control circuit)

  ⇒ excluding DC control circuit (serial to parallel converter + buffers)

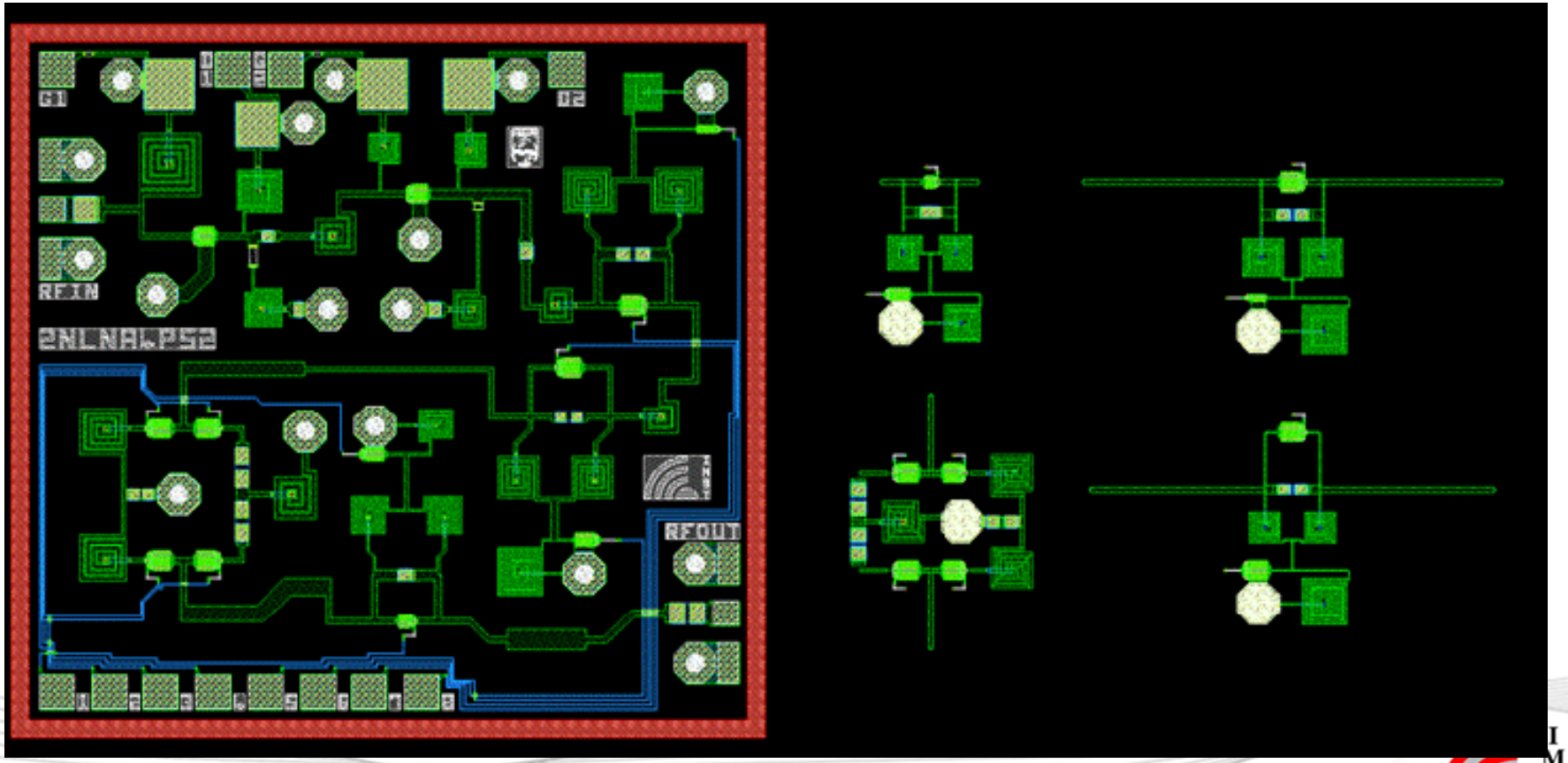
Core Chip Design : 2NLNA4PS2

Layout:

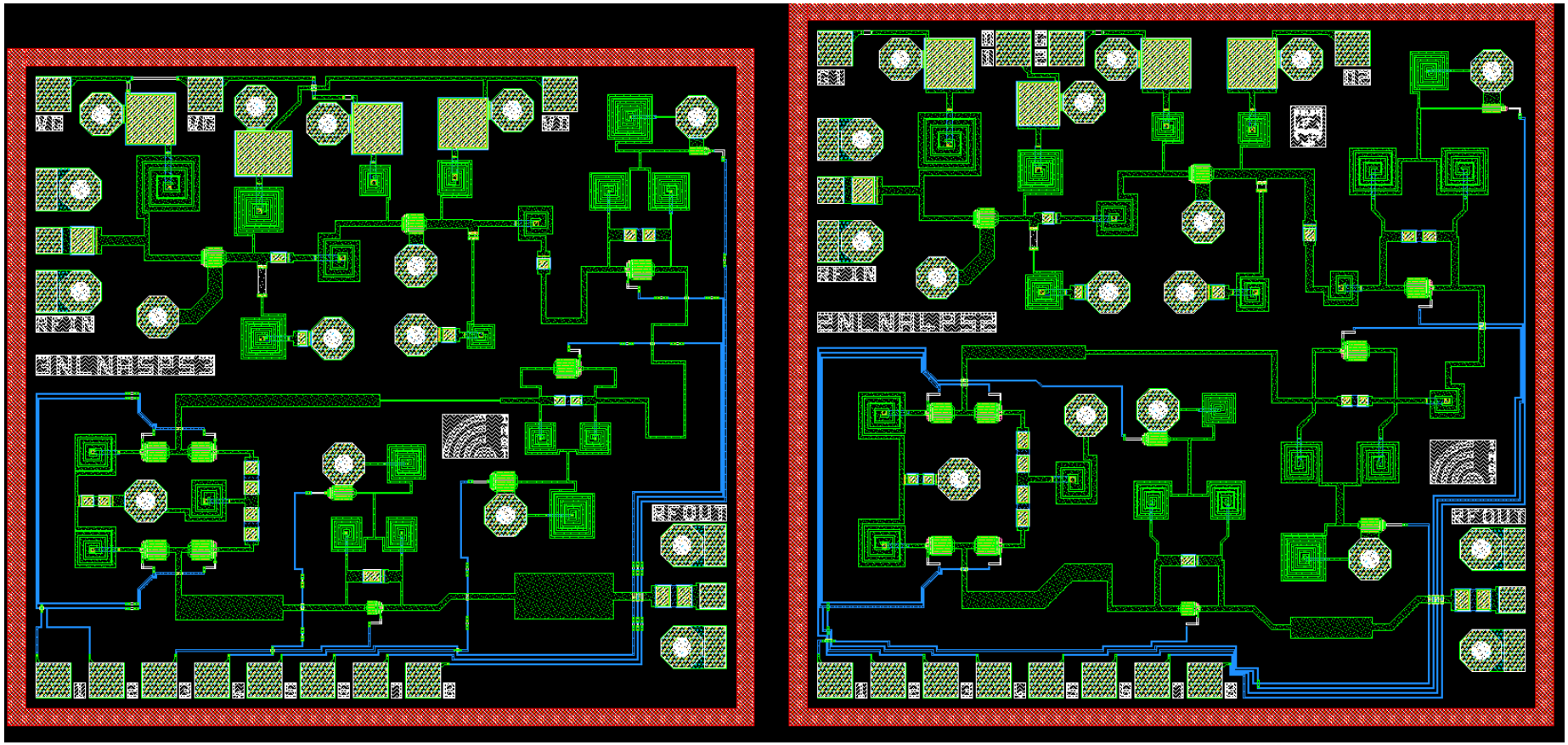


Momentum simulation

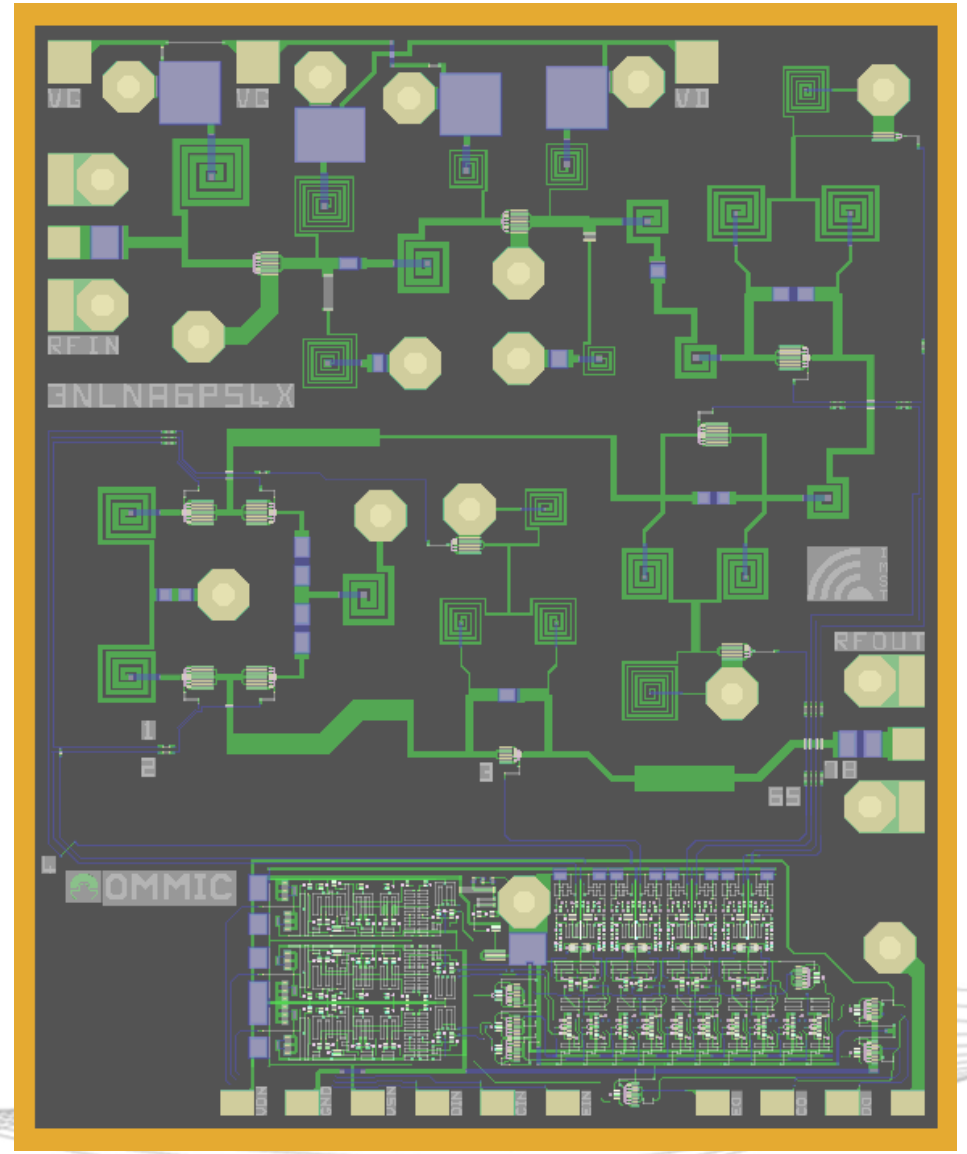
→ Higher integration possible



Size reduction



Including logic

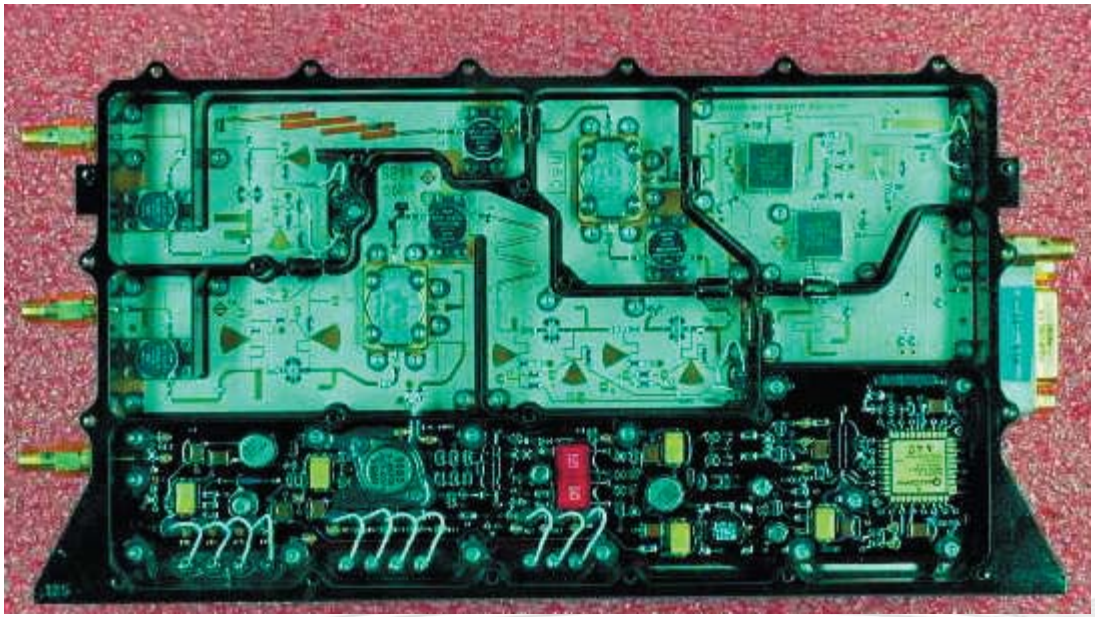


System example synthesizer

→ Large size (LO)

→ Heavy

→ Single frequency



→ small and integrated chip

http://www.saabgroup.com/en/ProductsServices/BusinessUnit/saab_ericsson_space.htm
http://products.saabgroup.com/PDBWebNew/GetFile.aspx?PathType=ProductFiles&FileType=Files&Id=6071

Phase noise

Simplified Leeson equation

$$L(f_m) = \frac{FkTG}{8Q_L P}\left(\frac{f_r}{f_m}\right)^2$$

$$|S_{21}| = \frac{1}{G} = 1 - \frac{Q_L}{Q_0}$$

G:	Gain of active part
F:	Noise figure of active part
Q_L:	Loaded Q of resonator
f_r:	Resonance frequency
f_m:	Offset frequency from carrier
P:	Output power of active part
S_{21}:	Transmission coefficient of resonator at resonance

VCO requirement

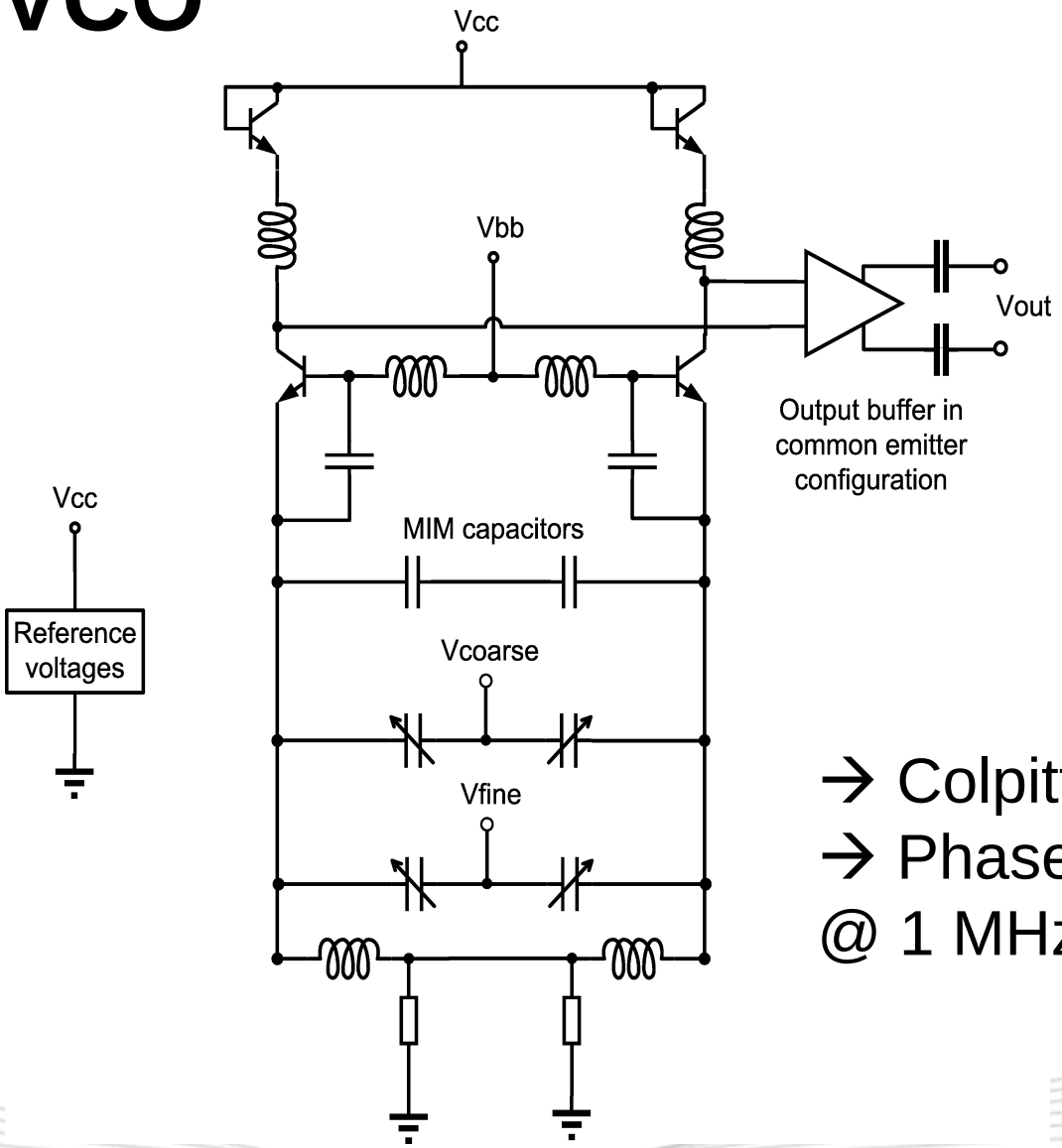
→High quality factor of the resonator

→Large voltage swing (high output power)

→High breakdown voltage for active part transistor technology

→Use a transistor with low 1/f noise

VCO



→ Colpitts
→ Phase noise: -115 dBc/Hz
@ 1 MHz offset (20 GHz)

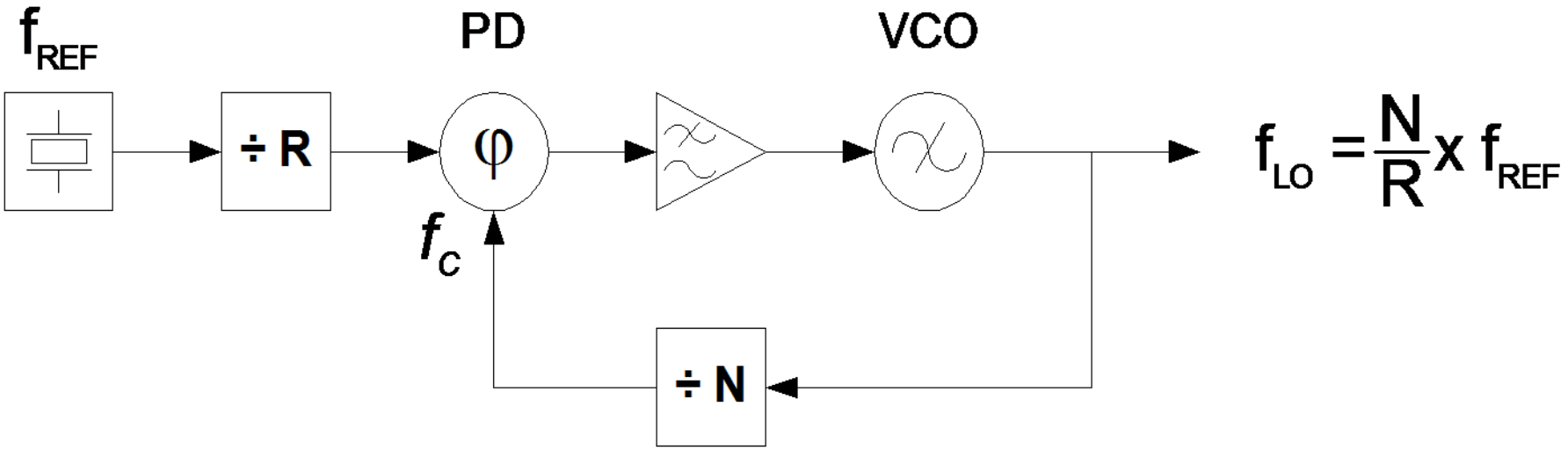
PLLs

→Close to the carrier phase noise is determined by the reference crystal

→Inside PLL loop the phase noise of a synthesizer is determined by the PLL (phase detector). VCO noise is attenuated.

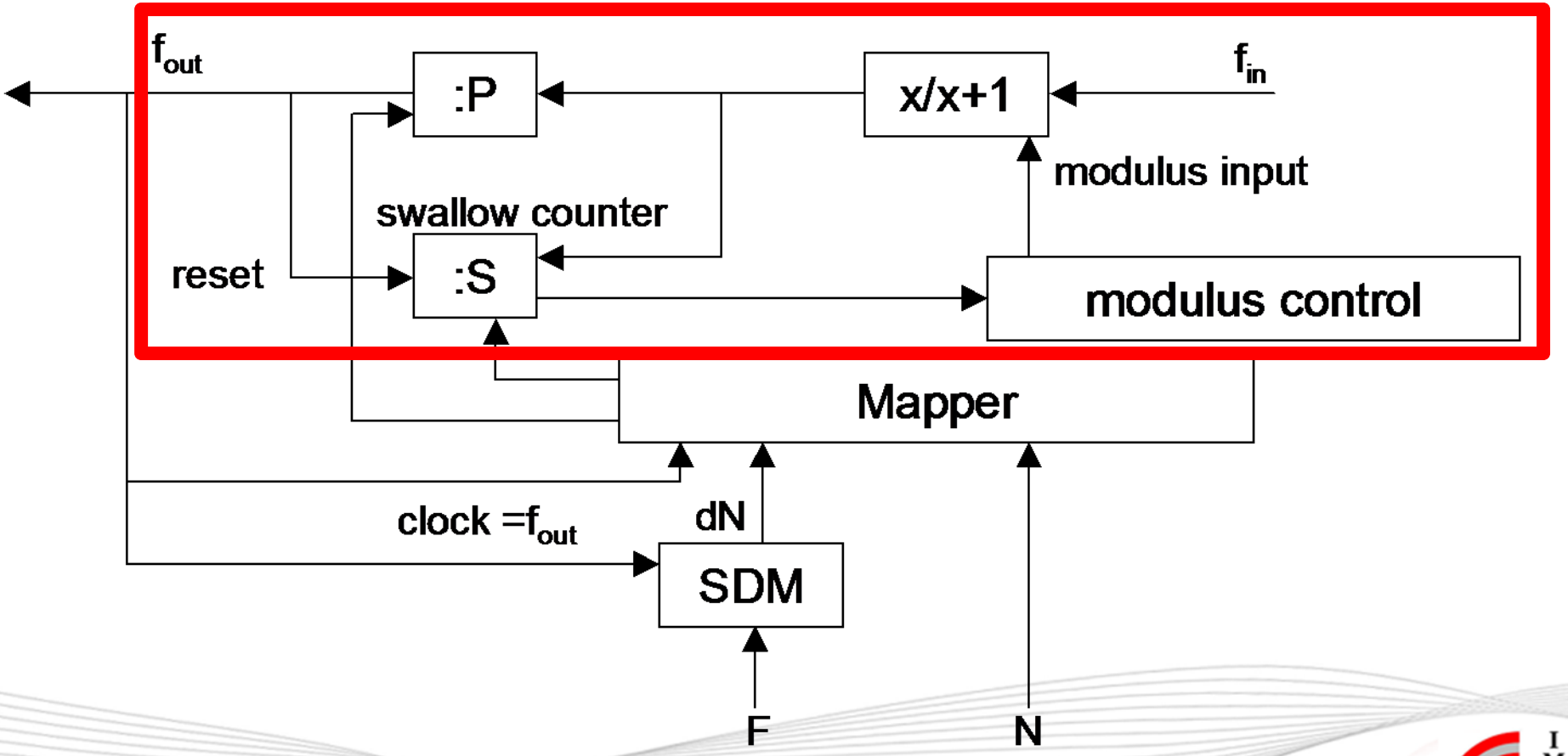
→Output PLL loop the phase noise of a synthesizer is determined by the VCO phase noise

Integer-N PLL with reference divider



How to generate arbitrary frequencies?

→ Build a programmable 1/N-divider



Continous division (example x=8)

→ Divide S times by x+1 and P-S times by x

N=(x+1)*S+x*(P-S)=8*P+S, P>S

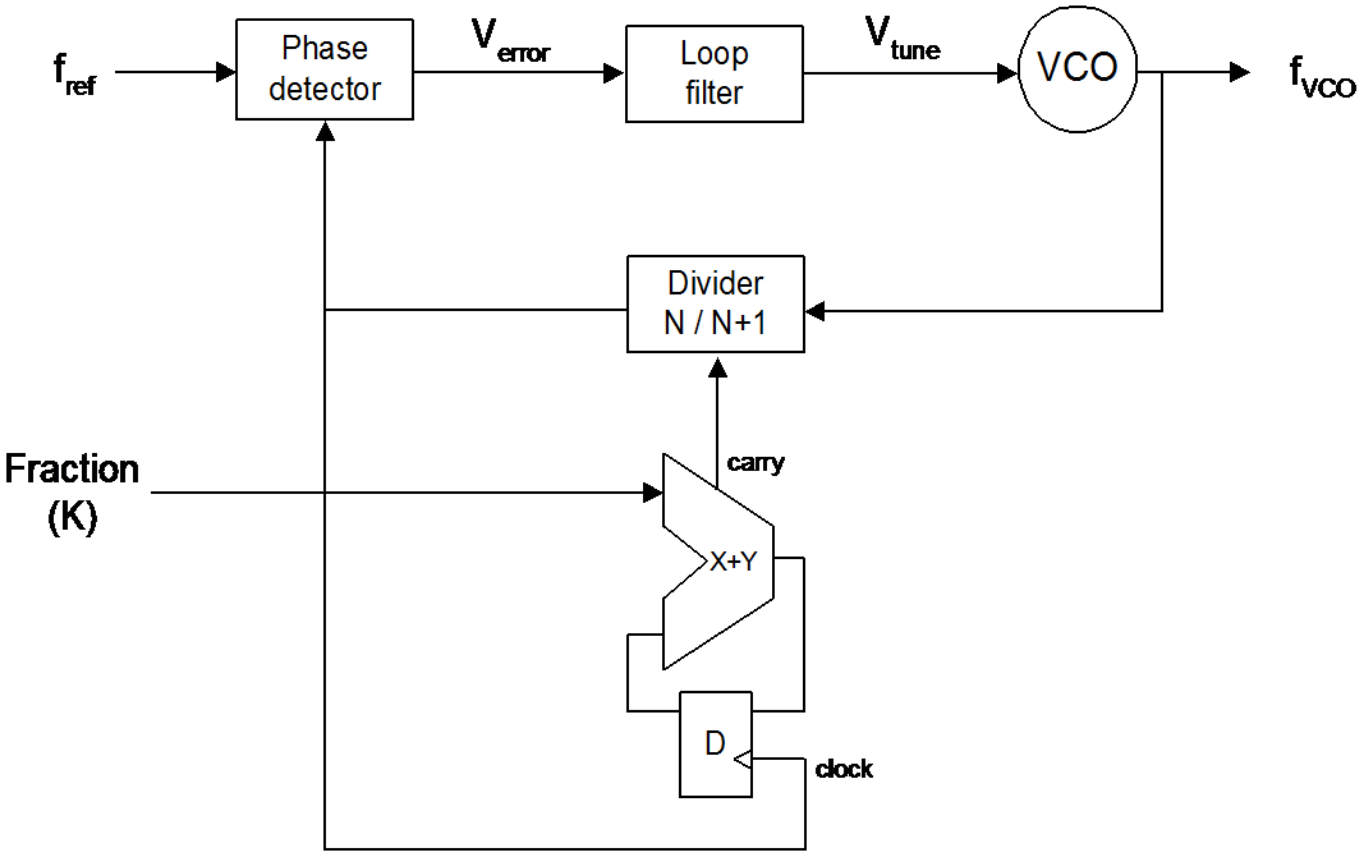
...

P=6,S=0..6: N=8*6+0..8*6+7=48..54, 55 not possible

P=7,S=0..7: N=8*7+0..8*7+7=56..63
P=8,S=0..7: N=8*8+0..8*8+7=64..71

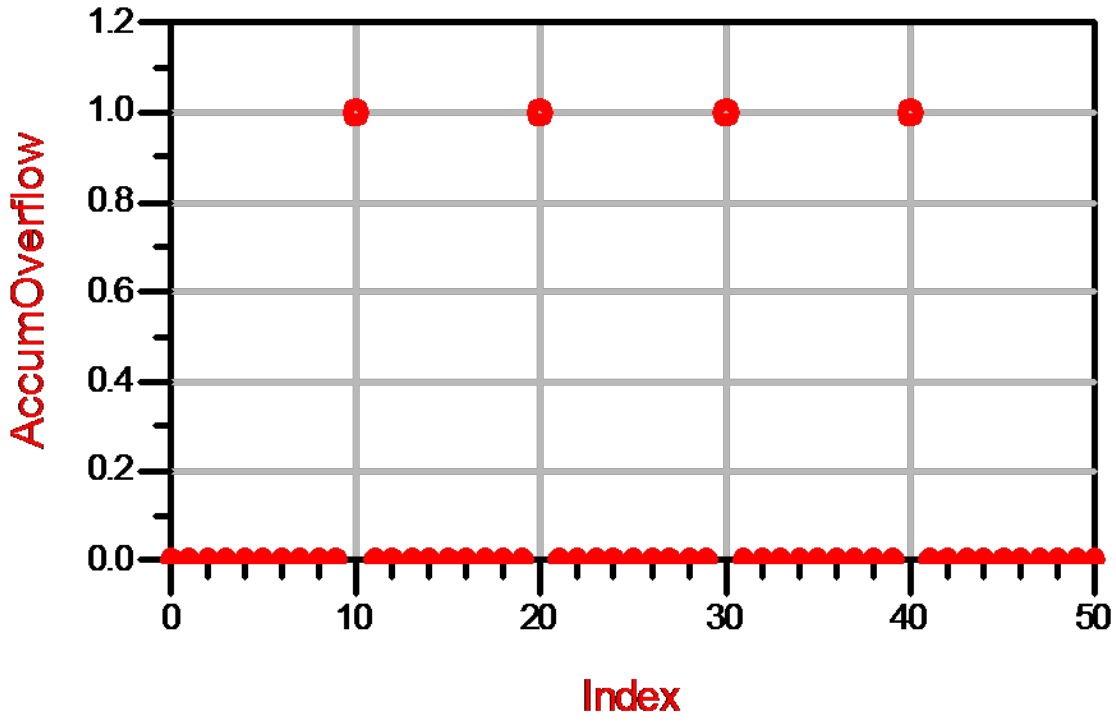
...

Simplified fractional-N PLL example



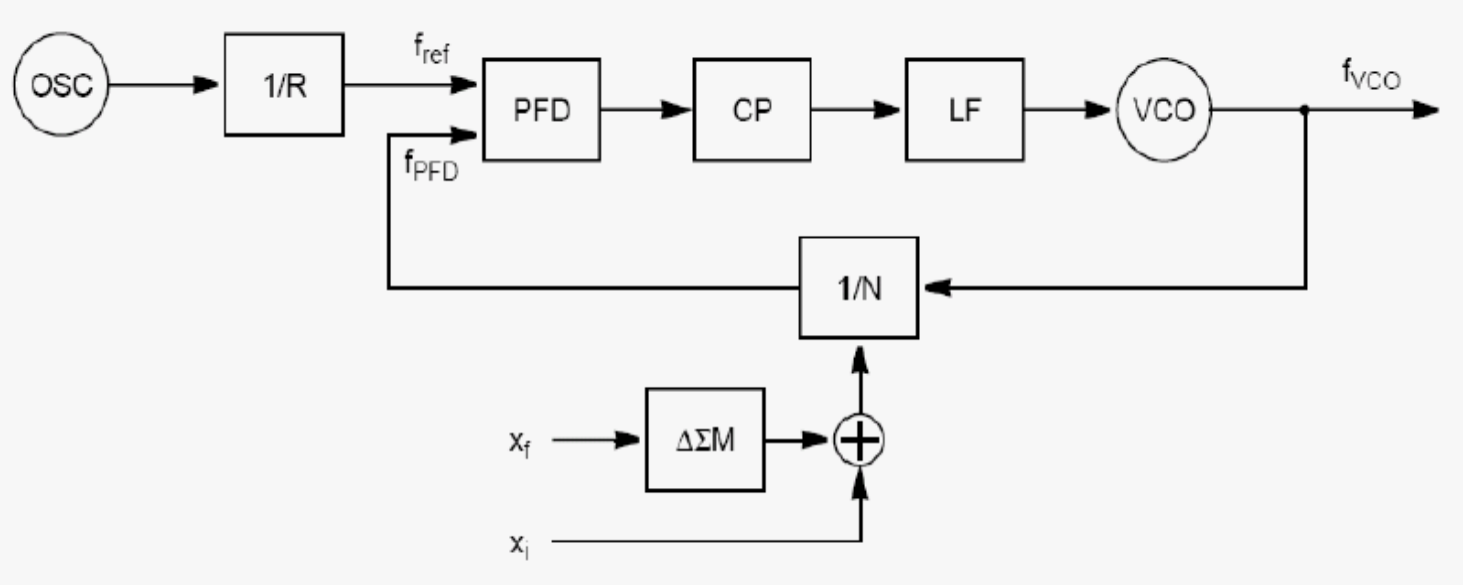
Ratio: 10.1: Divide 9 times by 10 and one time by 11 (next page)

Accumulator



This division schema generates large spurs.

Sigma Delta Modulator (SDM)



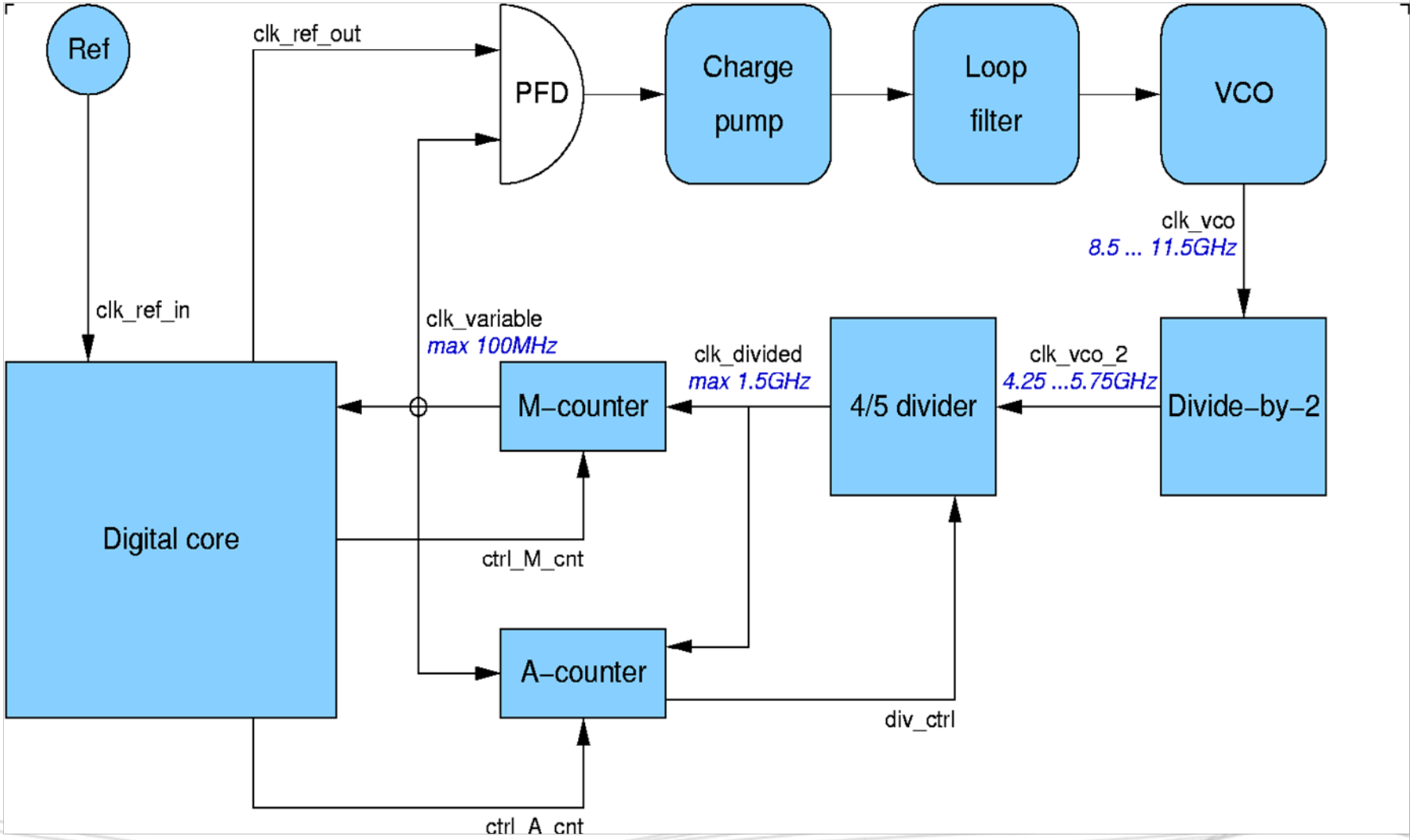
Modulator input: Only fractional part x_f
SDM generates series of integer numbers n_i
$n_i \in M$, 2^{μ} values are available for M

$$x_f = \bar{n}_i = \lim_{N\to\infty} \frac{1}{N} \sum_{i=1}^{N} n_i$$

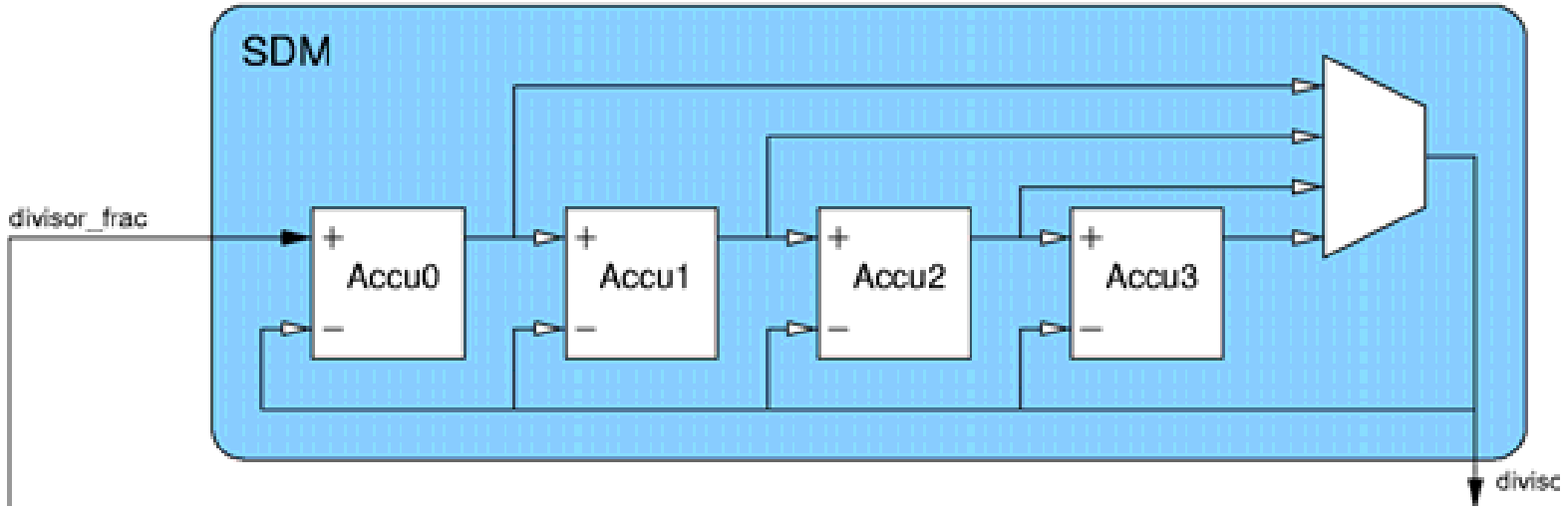
Time average value at SDM output

Example: 2, -4, -2, 3, 0, 3 –1, -3, 2, 1, ... for $x_f = 0.1$

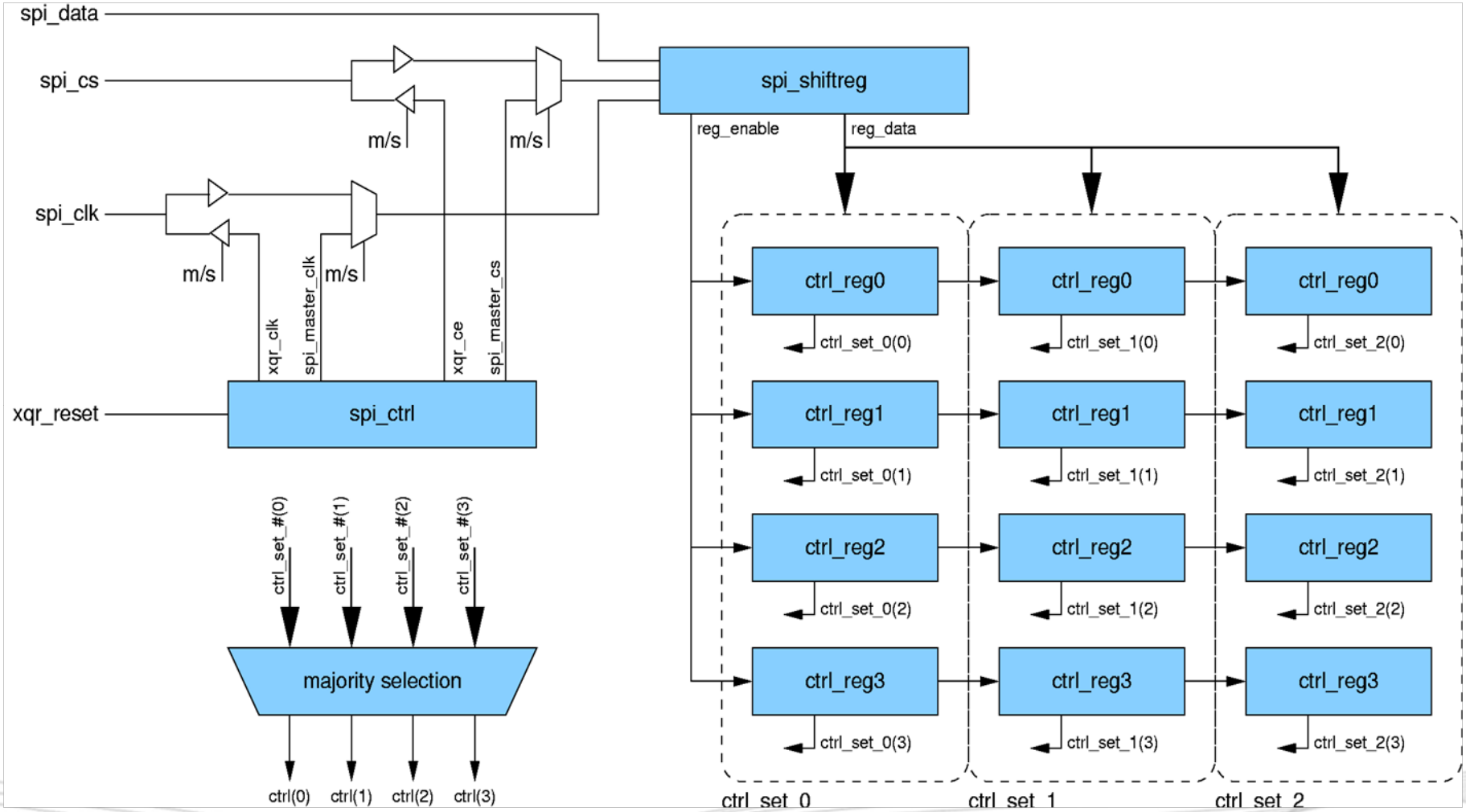
Synthesizer architecture (1)



Synthesizer architecture (2)



Synthesizer architecture (3)



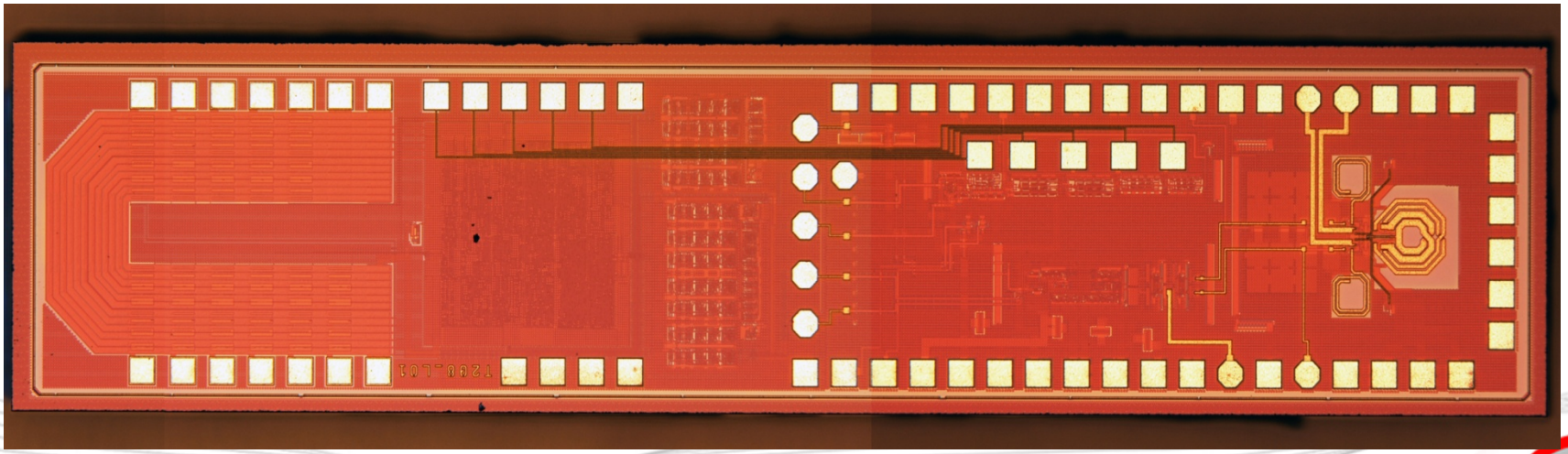
SiGe Design

→ World best 1-chip synthesizer

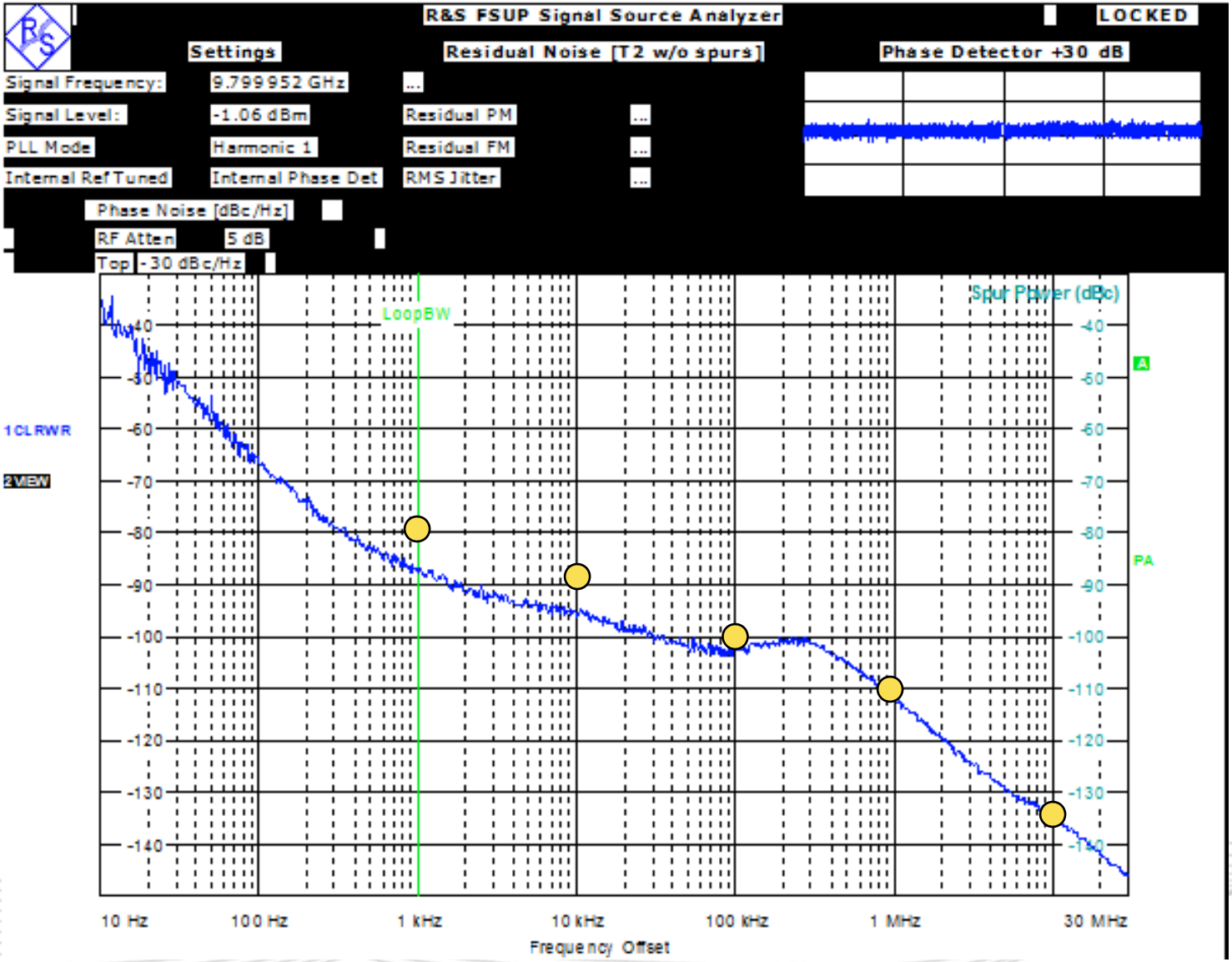
→ 250 MHz-24 GHz PLL

→ Integrated 17…20 GHz or 8…12 GHz VCO

→ Fractional-N



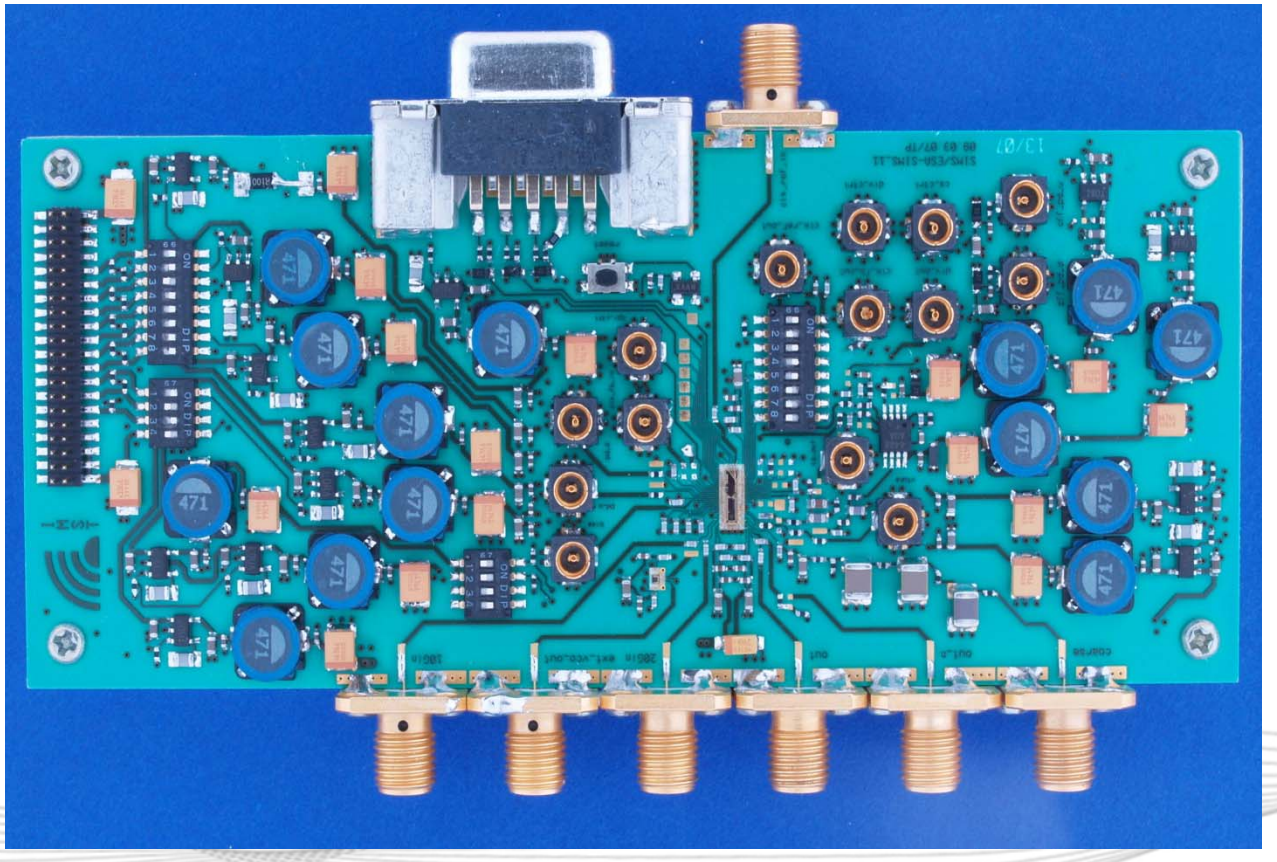
Measurement results



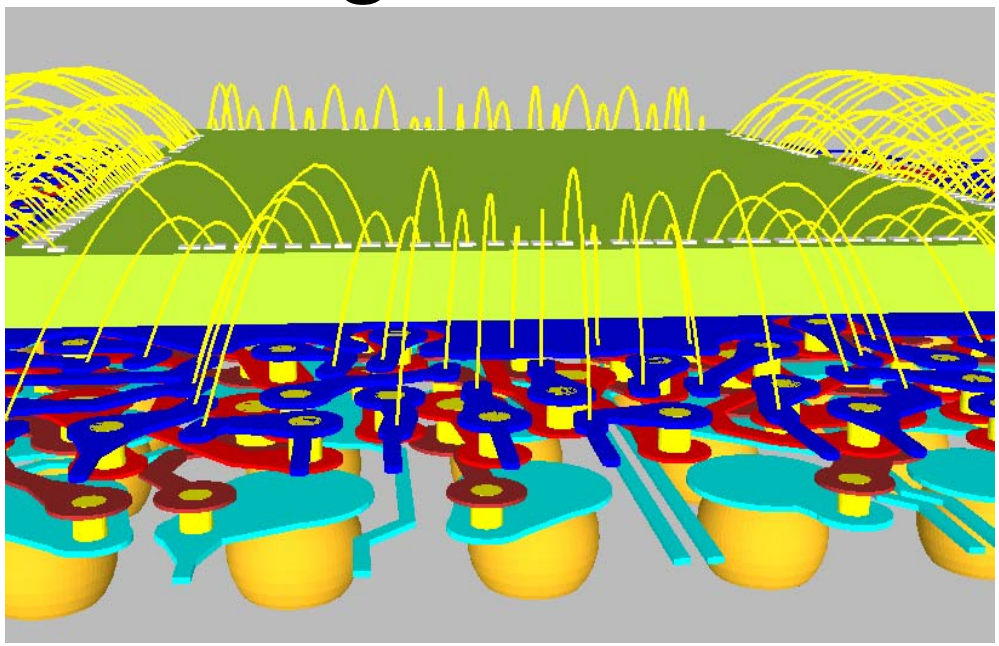
Synthesizer application test board

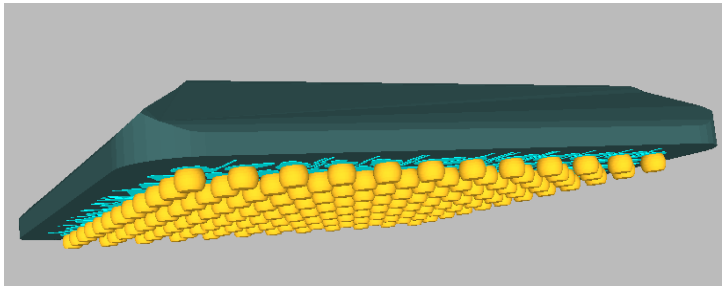
→PC interface

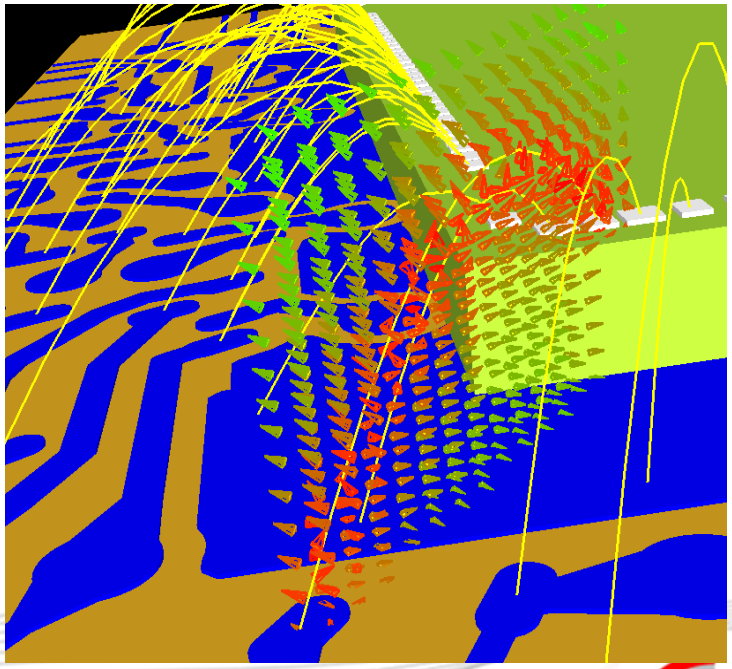
→Many test ports



Packages







→ BGA simulation

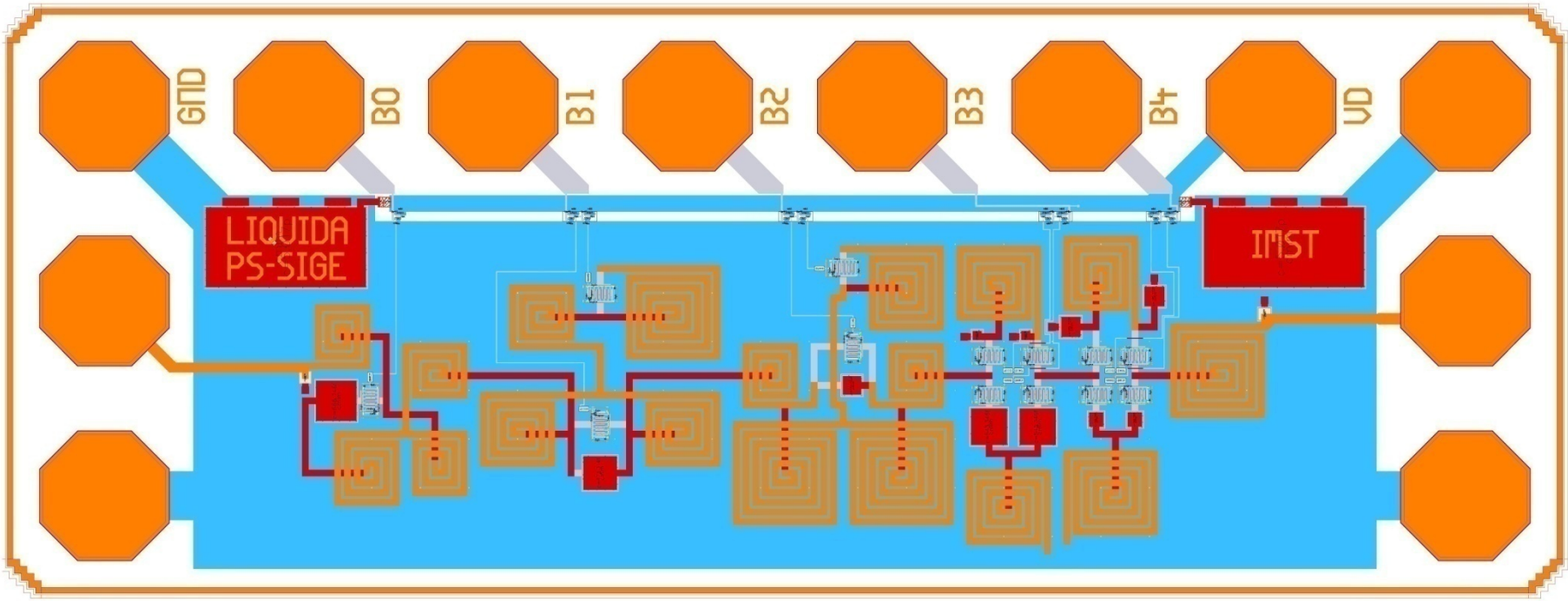
→ Equivalent circuits

→ S-parameter files

→ Magnetic field

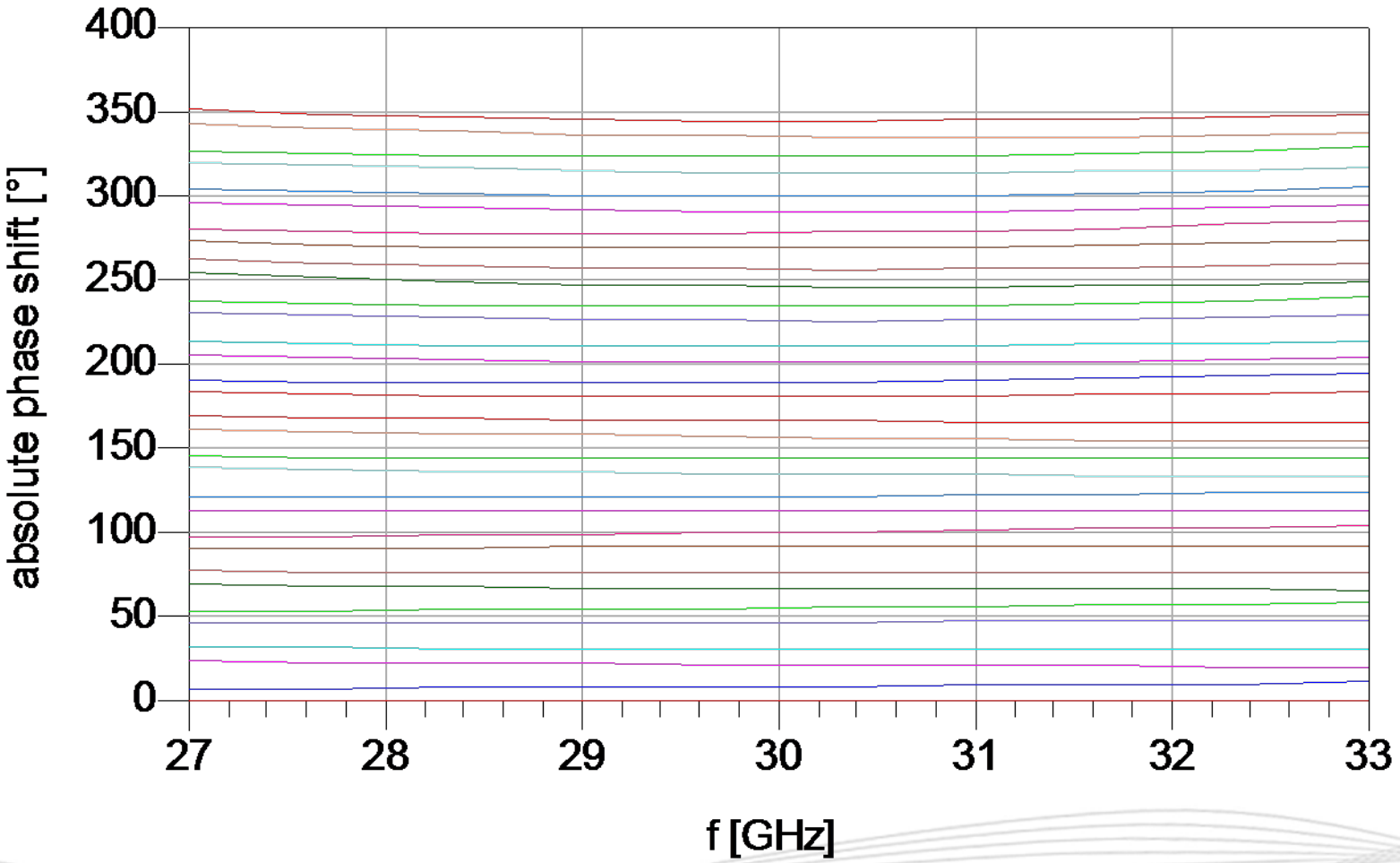
World smallest phase shifter (ka)

Size 960 x 360 µm², Core 620 x 210 µm²



V_D = 3 V, $V_{C\ (B0\text{-}B4)}$ = 0 V / 3 V (active / not active)

Phase diagram



Any questions?