28 / 40-Pin 8-Bit CMOS FLASH Microcontrollers

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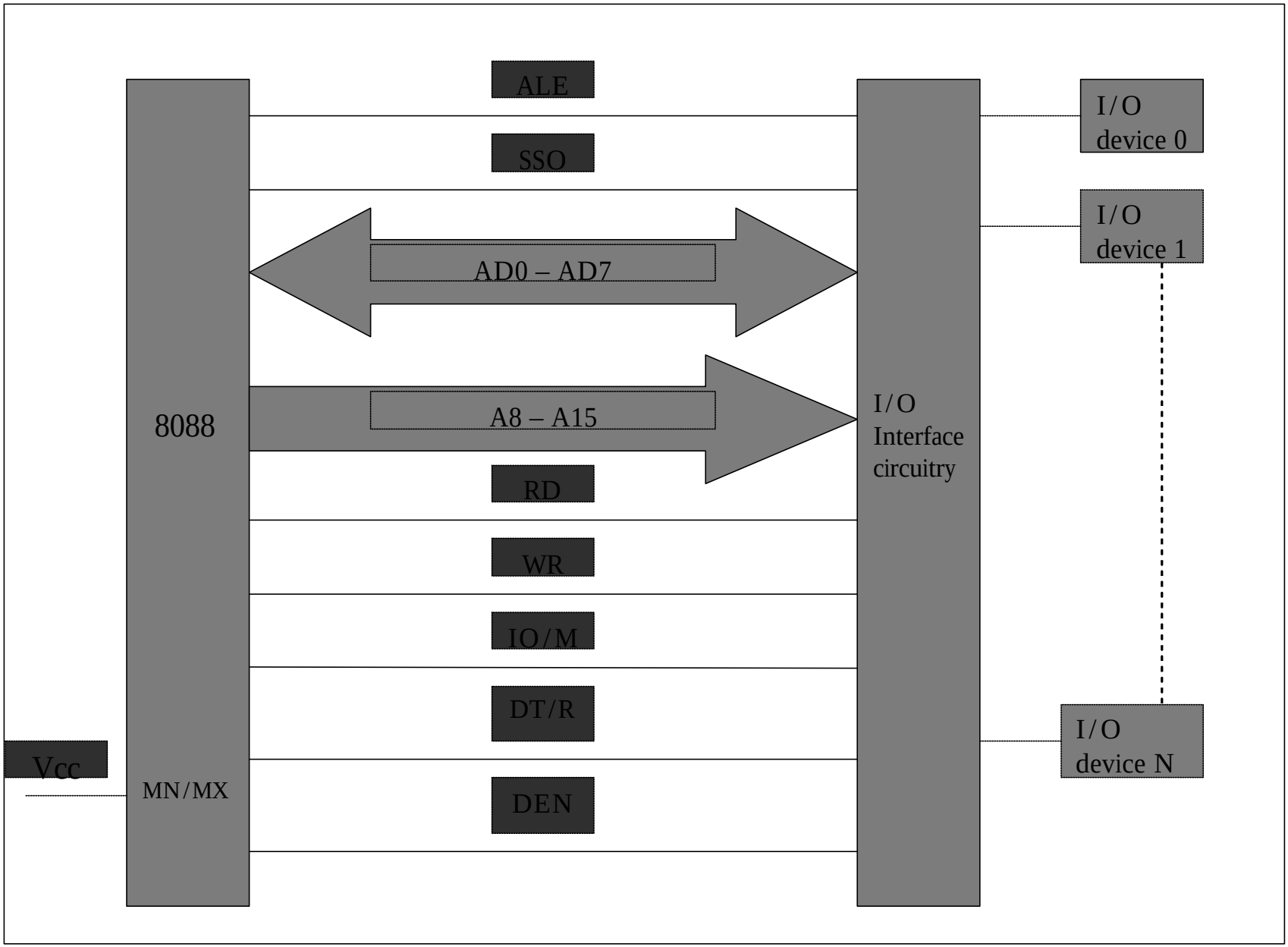
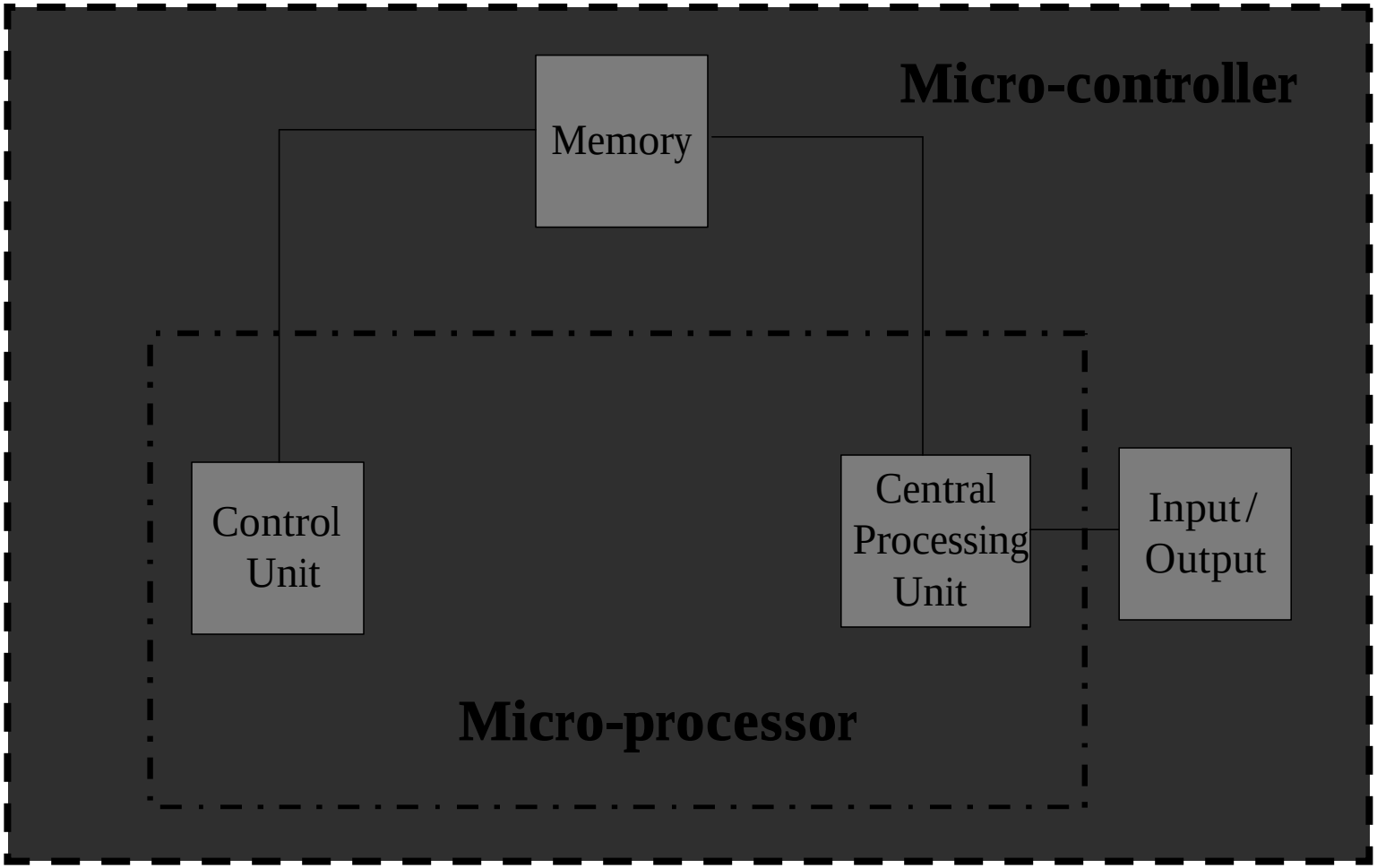
Minimum-Mode 8088 System I/O Interface



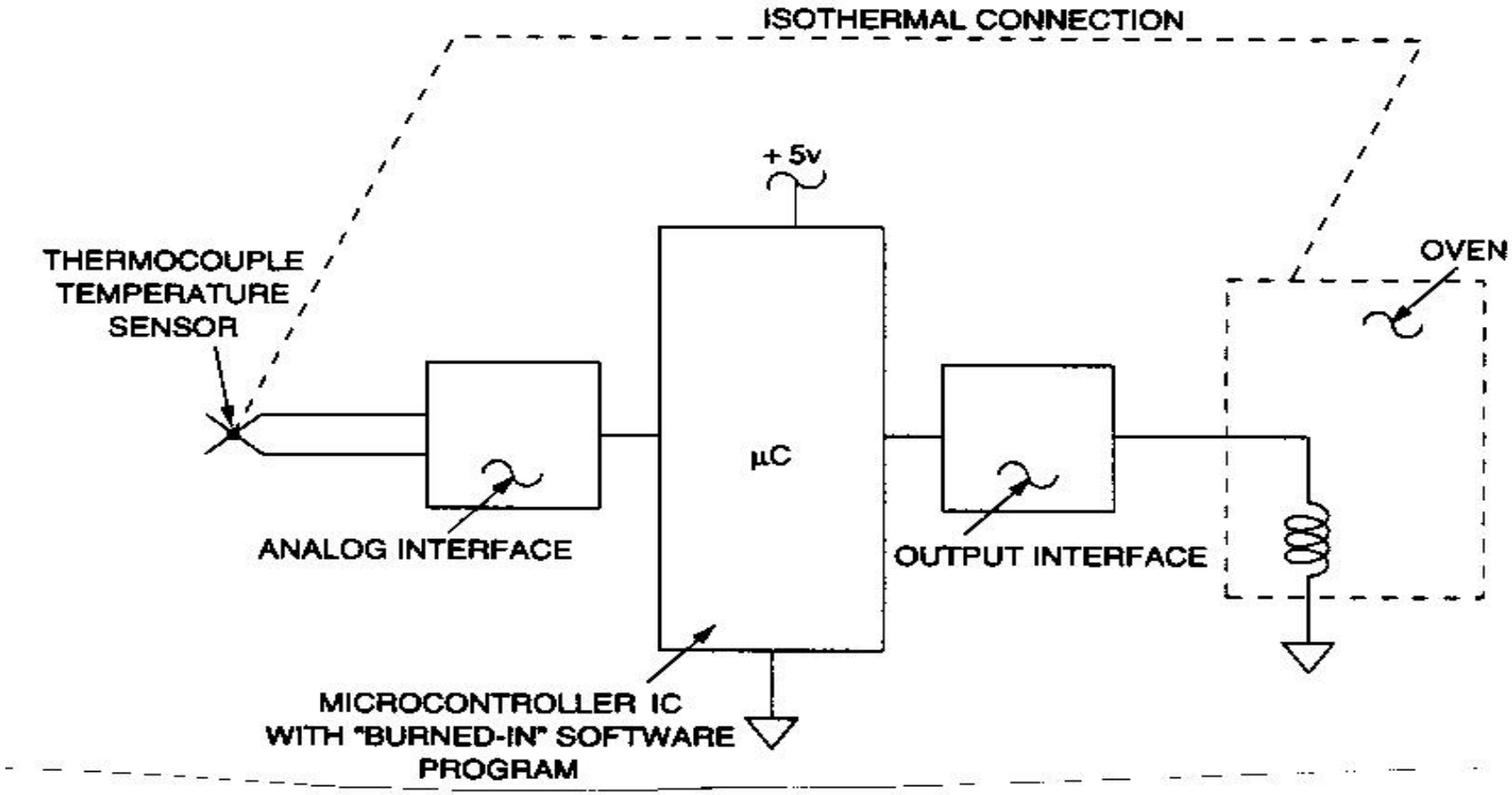
Microprocessor & Microcontroller



Microprocessor / Microcontroller Applications

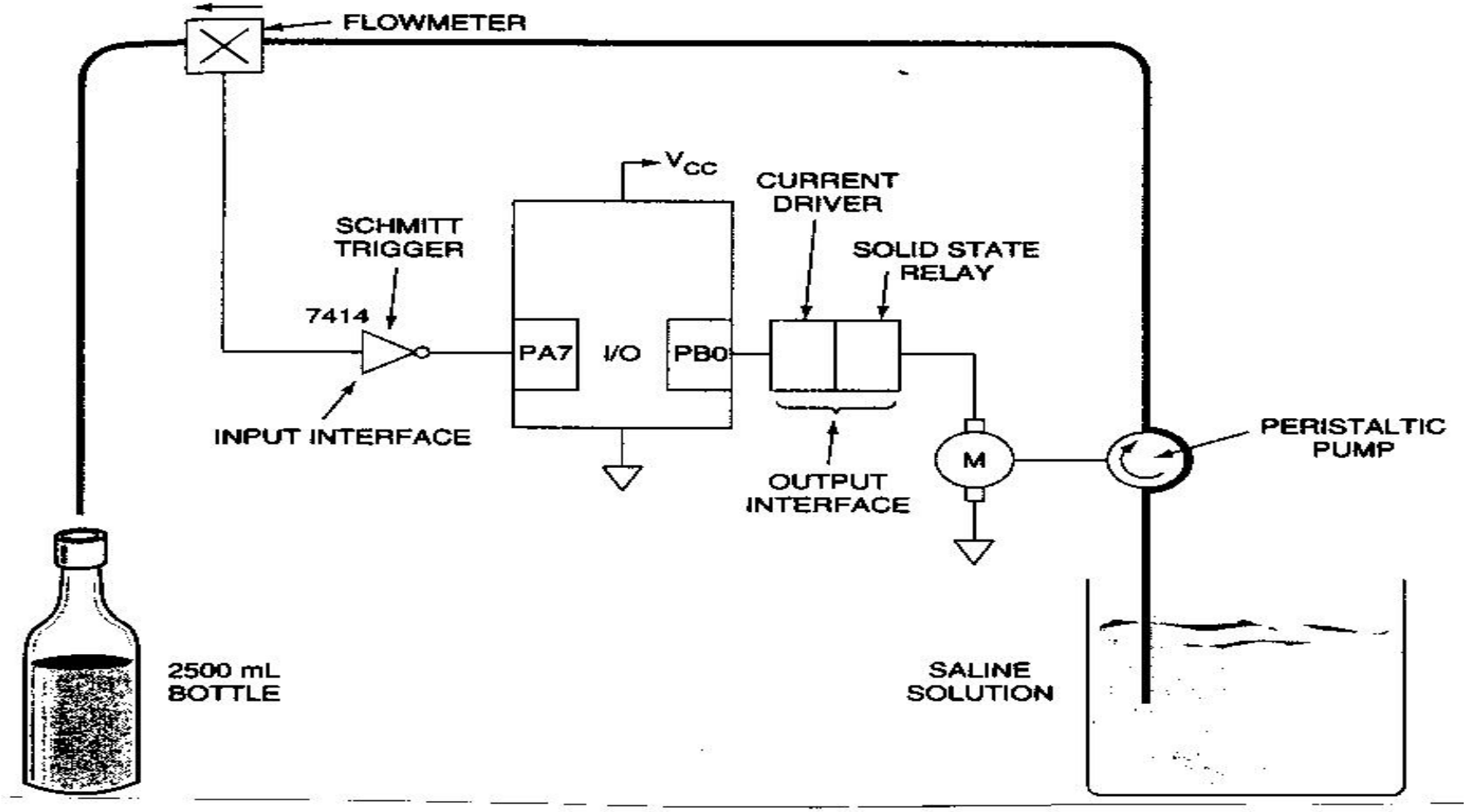
Perhaps the largest manufacturer of micro-computers is Delco Electronics, which makes the computer systems that go into General Motors automobiles and trucks. With a GM production of approximately 14 million cars and trucks per year, each containing roughly 12 microprocessors and microcontrollers, the number of microcomputer systems needed approaches 168 million per year!

Application Example 1



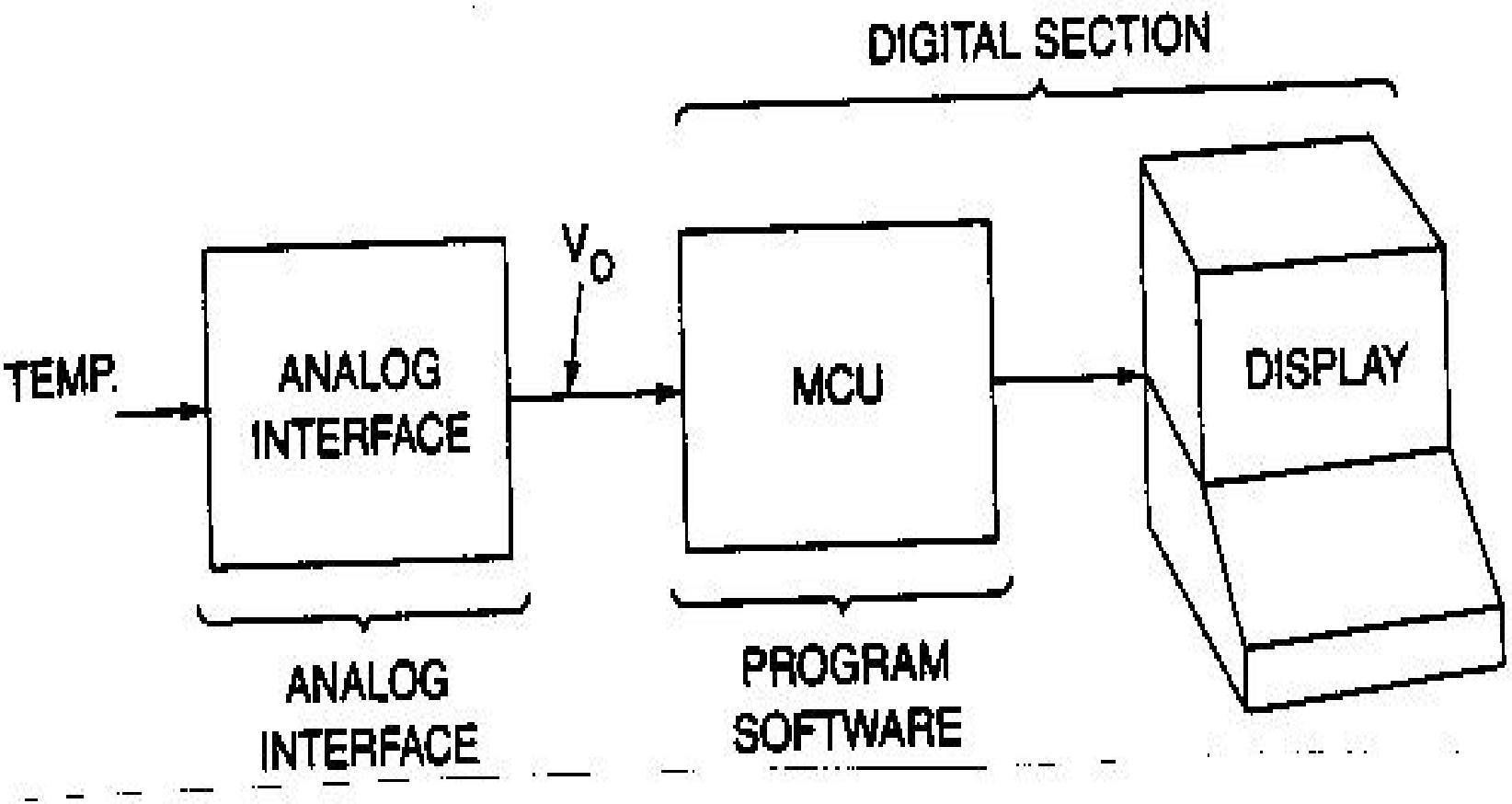
This microcontroller-based oven temperature control unit appears deceptively simple. However, a considerable amount of development time followed by extensive testing is needed to bring an application design to finished product stage.

Application Example 2



Block diagram illustrating the major elements of a closed-loop µC based bottle-fill

Application Example 3

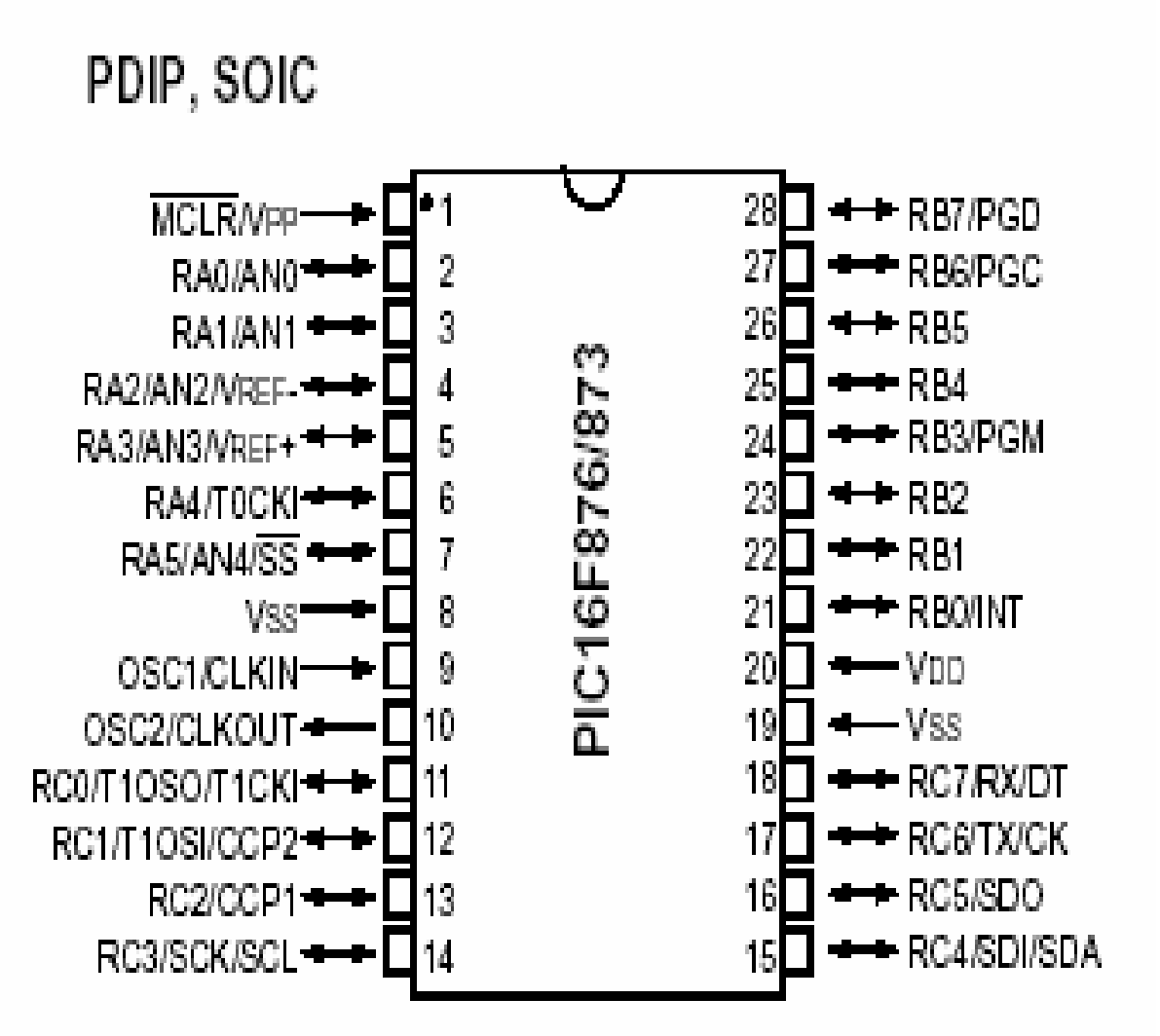


The block diagram of a microcontroller-based temperature measurement system consists of an analog interface section (transducer and SCC) and a digital section

Motorola Microcontroller

Pin assignments for the MC68HC11A8 (a) 52-pin PLCC, and (b) 48-pin DIP

Microchip Microcontroller



SECTION 1
MICROCONTROLLER GENERAL FEATURES

Microcontroller Core Features

- High performance RISC CPU,
- Only 35 single instructions to learn,
- All single cycle instructions except for program branches which are two cycles,
- Up to 8k x14 words of FLASH program memory, 368 x 8 bytes of RAM and 256x8 bytes of EEPROM,

Core Features Continue ….

- Operating speed: DC-20 MHz clock input. DC-200 ns instruction cycle
- Pin out compatible to PIC16C73B/ 74B/76/77
- Interrupt compatibility (14 sources)
- Eight level deep hardware stack
- Direct, indirect and relevant addressing modes
- Programmable code protection

Peripheral Features

- Timer0: 8-bit timer/counter
- Timer1: 16-bit timer/counter
- Timer2: 8-bit timer/counter with 8-bit period register, pre-scalar and post-scalar
- Two Capture, Compare, PWM modules
- 10-bit multi-channel Analog-to-digital converter
- Universal Sync Async. Receiver Transmitter with 9-bit address detection

Key Features PIC16F877

Operating Frequency	DC-20MHz
RESETS (and Delays)	POR, BOR (PWRT, OST)
FLASH program memory	8 K
Data Memory (bytes)	368
EEPROM Data Memory	256
Interrupts	14
I/O Ports	Ports A,B,C,D, E
Timers	3
Capture/Compare/PWM modules	2
Serial Communications	MSSP,USART
Parallel Communication	PSP
10-bit Analog to Digital	8input channel
Instruction Set	35 instructions

PIC16F877 PINOUT Description

Pin Name	DIP Pin#	I/O/P Type	Description
OSC1/CLKIN	13	I	Oscillator crystal input/external clock source input
OSC2/CLKOUT	14	O	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode, in RC mode, OSC2 pin outputs CLKOUT which has ¼ the frequency of OSC1, and denotes instruction cycle rate
MCLR/Vpp	1	I/P	Master Clear input or programming voltage input. Active low RESET to the device

PINOUT Description Continue …

Pin Name	Pin #	I/O/P Type	Description
RA0/AN0	2	I/O	RA0 can also be analog input0
RA1/AN1	3	I/O	RA1 can also be analog input1
RA2/AN2/Vref-	4	I/O	RA2 can also be analog input2 or negative analog ref. voltage
RA3/AN3/Vref+	5	I/O	RA3 can also be analog input3 or positive analog ref. voltage
RA4/T0CK1	6	I/O	RA4 can also be clock input to Timer0. Output is open drain type
RA5/SS/AN4	7	I/O	RA5 can also be analog input4 or the slave select for sync serial port

PINOUT Description Continue …

Pin Name	Pin#	I/O/P Type	Description
RB0/INT	33	I/O	RB0 can also be external interrupt pin
RB1	34	I/O	
RB2	35	I/O	
RB3/PGM	36	I/O	RB3 can also be low voltage programming input
RB4	37	I/O	Interrupt-on-change pin
RB5	38	I/O	Interrupt-on-change pin
RB6/PGC	39	I/O	Interrupt-on-change pin or In-Circuit Debugger pin. Serial programming clock
RB7/PGD	40	I/O	Interrupt-on-change pin or In-Circuit Debugger pin. Serial programming data

Pin Name	Pin #	I/O/P Type	Description
RC0/T1OSO/T1CK1	15	I/O	Port C is a bi-directional I/O port. RC0 can also be the Timer1 oscillator output of a Timer1 clock input.
RC1/T1OSI/CCP2	16	I/O	RC1 can also be Timer1 oscillator I or Capture2 I Compare2 O/PWM2 output
RC2/CCP1	17	I/O	RC2 can also be Capture1 I/Compare1 O/PWM1 O
RC3/SCK/SCL	18	I/O	RC3 can also be synchronous serial clock I/O for both SPI and I^2C mode
RC4/SDI/SDA	23	I/O	RC4 can also be SPI Data in (SPI mode) or data I/O (I^2C mode)
RC5/SDO	24	I/O	RC5 can also be SPI Data Out (SPI mode)
RC6/TX/CK	25	I/O	RC6 can also be USART Async Transmit or Sync Clock
RC7/RX/DT	26	I/O	RC7 can also be USART Async Receive or Sync Data

PINOUT Description Continue …

Pin Name	Pin #	I/O/P Type	Description
RD0/PSP0	19	I/O	PORT D is a bi-directional I/O port or slave port when interfacing to a microprocessor bus
RD1/PSP1	20	I/O	
RD2/PSP2	21	I/O	
RD3/PSP3	22	I/O	
RD4/PSP4	27	I/O	
RD5/PSP5	28	I/O	
RD6/PSP6	29	I/O	
RD7/PSP7	30	I/O	

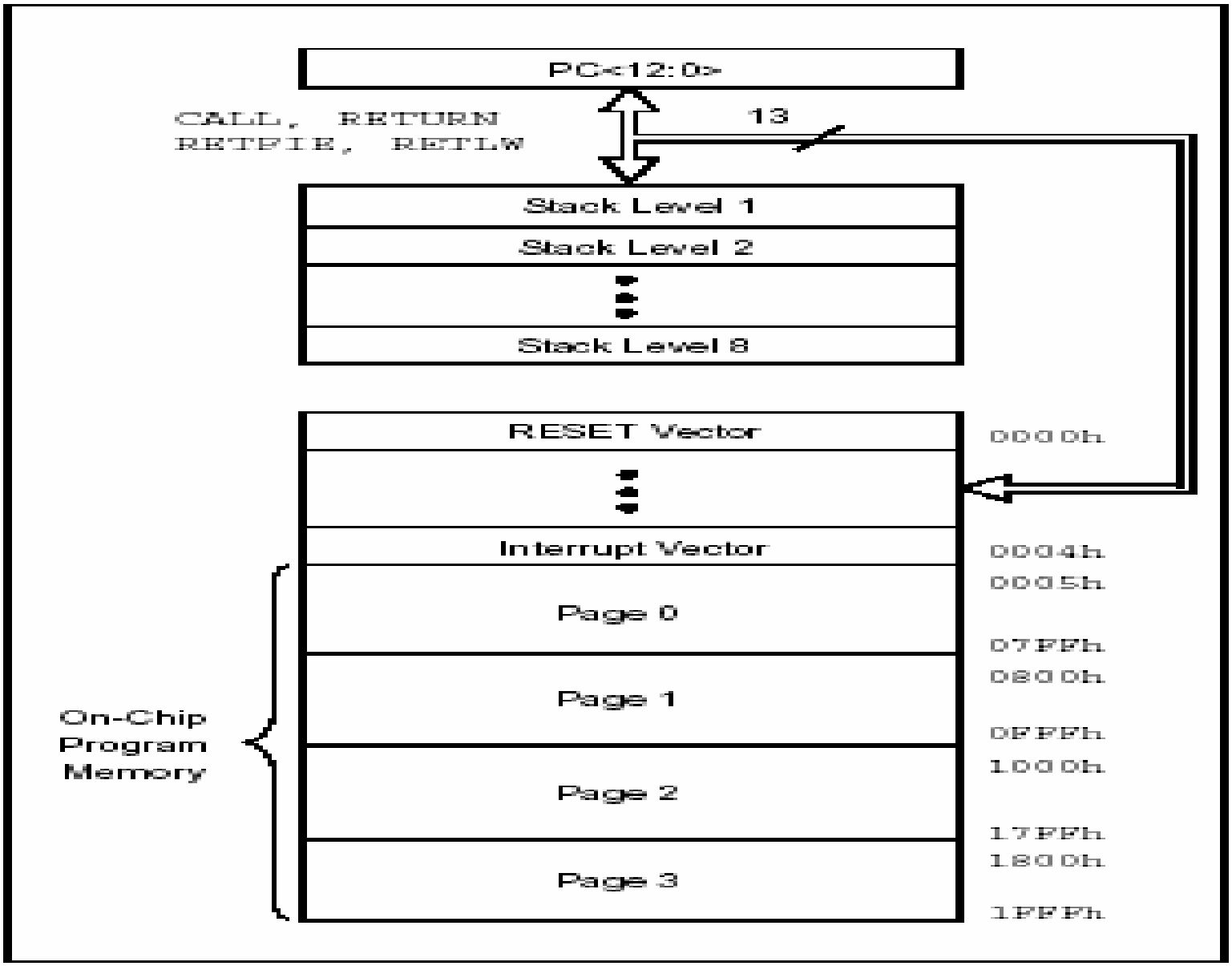
PINOUT Description Continue …

Pin Name	Pin#	I/O/P Type	Description
			PORT E is a bi-directional I/O port
RE0/RD/AN5	8	I/O	RE0 can also be read control for the parallel slave port, or analog input 5
RE1/WR/AN6	9	I/O	RE1 can also be write control for the parallel slave port, or analog input 6
RE2/CS/AN7	10	I/O	RE0 can also be select control for the parallel slave port, or analog input 7
VSS	12,31	P	Ground reference for logic and I/O pins
VDD	11,32	P	Positive supply for logic and I/O pins

MEMORY ORGANIZATION

- There are three memory blocks in each of the PIC16F87X MCUs.
  1. The Program memory
  2. Data Memory
  3. EEPROM Data Memory
- The Program Memory and Data Memory have separate buses so that concurrent access can occur

PIC16F877/876 Program Memory Map & Stack



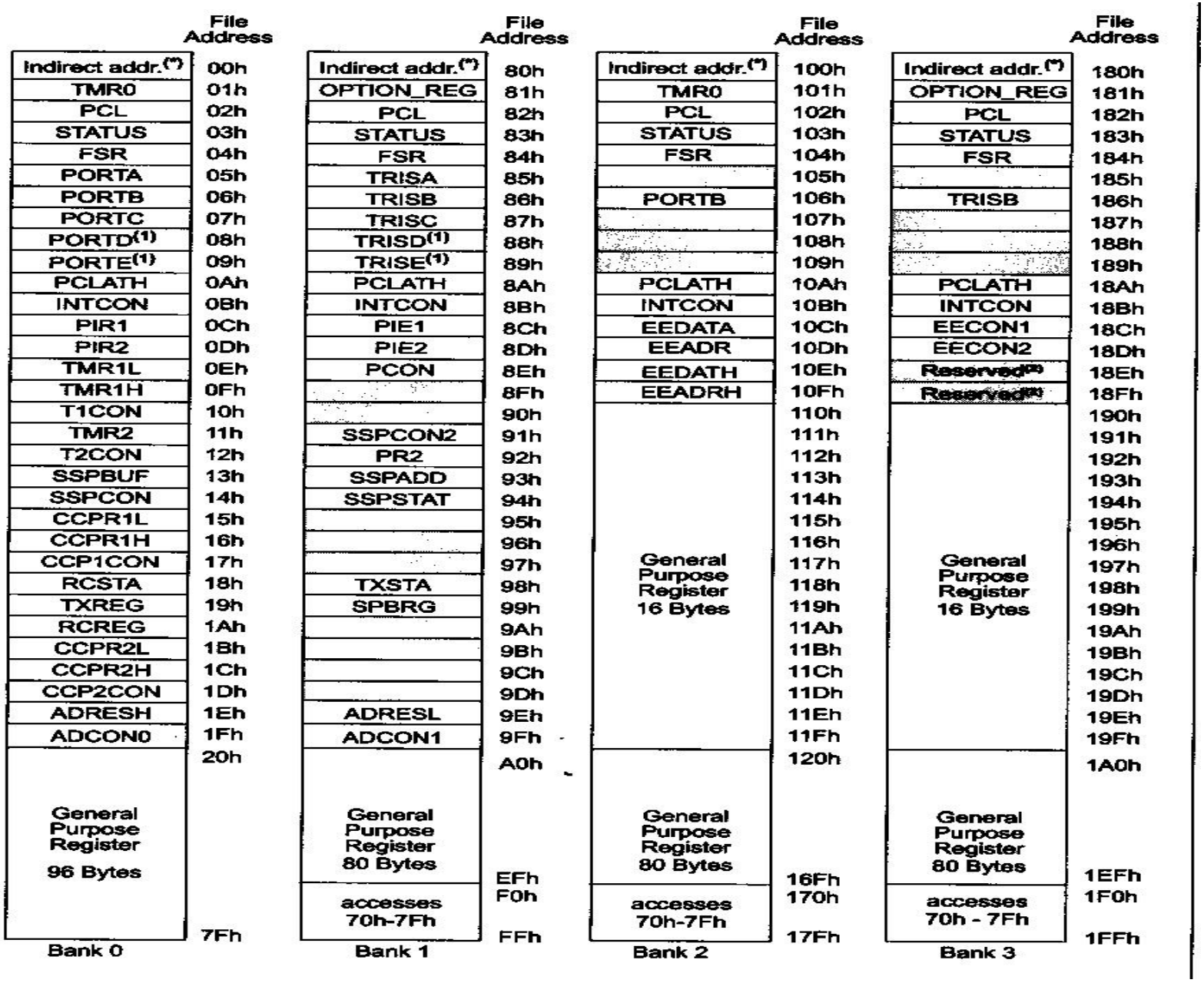
Program Memory Organization, Program Counter

- The PIC16F87X devices have a 13-bit program counter capable of addressing an 8K x 14 program memory space.

STACK

- The PIC16F87X family has an 8-level deep x 13-bit wide hardware stack.
- The stack space is not part of either program or data space and the stack pointer is not readable or writable.
- The PC is PUSHed onto the stack when a CALL instruction is executed, or an interrupt causes a branch.
- The stack is POPed in the event of a RETURN, RETLW or a RETFIE instruction execution.

Data Memory (Register File Map)



PIC16F877 / 876 Register File Map

Indirect addr	File Address
PCL	02h
STATUS	03h
FSR	04h
PCLATH	0Ah
INTCON	0Bh

Indirect addr	File Address
OPTION_REG	81h
PCL	82h
STATUS	83h
FSR	84h
PCLATH	8Ah
INTCON	8Bh

Indirect addr	File Address
TMR0	101h
PCL	102h
STATUS	103h
FSR	104h
PCLATH	10Ah
INTCON	10Bh

Indirect addr	File Address
OPTION_REG	181h
PCL	182h
STATUS	183h
FSR	184h
PCLATH	18Ah
INTCON	18Bh

Data Memory Bank Selection

- Bits RP1(STATUS<6>) and RP0(STATUS<6>) are the Bank Select bits

RP1:RP0	Bank
00	0
01	1
10	2
11	3

SPECIAL FUNCTION REGISTERS

- The Special Function Registers are registers used by the CPU and peripheral modules for controlling the desired operation of the device. These can be classified into two sets:

1. **Core (CPU) Registers:** Those registers associated with the core functions are described in detail in this section.
2. **Peripheral Registers:** Those related to the operation of the peripheral features are described in detail in the corresponding peripheral features sections.

Core (CPU) Registers

1. STATUS Register.
2. OPTION_REG Register.
3. INTCON Register.
4. PIE1 Register.
5. PIR1 Register.
6. PIE2 Register.
7. PIR2 Register.

STATUS Register (Address 03h, 83h, 103h, 183h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	TO	PD	Z	DC	C

bit7 bit0

- IRP: Register Bank Select bit (for indirect addressing)

  1=Bank 2, 3 (100h – 1FFh)

  0=Bank 1, 1 (00h – FFh)

- RP1:RP0: Register Bank Select bits (used for indirect addressing)

  11=Bank 3(180h – 1FFh)

  10=Bank 2(100h – 17Fh)

  01=Bank 1(80h – FFh)

  00=Bank 0(00h – 7Fh)

Each Bank is 128 bytes

STATUS Register Continue..

- TO: Time-out bit

  1=After power-up, CLRWDT instruction, or SLEEP instruction

  0=A WDT time-out occurred
- PD: Power-down bit

  1=After power-up or by the CLRWDT instruction

  0=By execution of the SLEEP instruction
- Z: Zero bit

  1=The result of an arithmetic or logic operation is 0

  0=The result of an arithmetic or logic operation is not 0

STATUS Register Continue..

- DC: Digit carry/borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions) (for borrow, the polarity is reversed)

  1=A carry-out from 4^{th} low order bit of the result occurred

  0= No carry-out from 4^{th} low order bit of the result
- C: Carry/borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)

  1=A carry-out from the Most Significant bit of the result occurred

  0=No carry-out from the Most Significant bit of the result occurred

OPTION_REG Register (Address 81h, 181h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	TO	PD	Z	DC	C

bit7 bit0

bit7 RBPU: PORT B Pull-up Enable bit

1=PORT B pull-ups are disabled

0=PORT B pull-ups are enabled by individual port latch values

bit6 INTEDG: Interrupt Edge Select bit

1=Interrupt on rising edge of RB0/INT pin

0=Interrupt on falling edge of RB0/INT pin

bit 5 T0CS: TMR0 Clock Source Select bit

1=Transition on RA4/T0CKI pin

0=Internal instruction cycle clock (CLKOUT)

bit 4 T0SE: TMR0 Source Edge Select bit

1=Increment on high-to-low transition on RA4/T0CK1 pin

0=Increment on low-to-high transition on RA4/T0CK1 pin

OPTION_REG Continue …

bit 3 PSA: Pre-scalar Assignment bit

1=Pres-scalar is assigned to the WDT

0=Pre-scalar is assigned to the Timer0 module

bit 2-0

PS2:PS0: Pre-scalar Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1:2	1:1
001	1:4	1:2
010	1:8	1:4
011	1:16	1:8
100	1:32	1:16
101	1:64	1:32
110	1:128	1:64
111	1:256	1:128

INTCON Register (ADDRESS 0Bh, 8Bh, 10Bh, 18Bh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF
bit7							bit0

bit 7 GIE: Global Interrupt Enable bit
1 = Enables all unmasked interrupts
0 = Disables all interrupts

bit 6 PEIE: Peripheral Interrupt Enable bit
1 = Enables all unmasked peripheral interrupts
0 = Disables all peripheral interrupts

bit 5 T0IE: TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 interrupt
0 = Disables the TMR0 interrupt

bit 4 INTE: RB0/INT External Interrupt Enable bit
1 = Enables the RB0/INT external interrupt
0 = Disables the RB0/INT external interrupt

INTCON Continue..

bit 3 RBIE: RB Port Change Interrupt Enable bit

1 = Enables the RB port change interrupt

0 = Disables the RB port change interrupt

bit 2 T0IF: TMR0 Overflow Interrupt Flag bit

1 = TMR0 register has overflowed (must be cleared in software)

0 = TMR0 register did not overflow

bit 1 INTF: RB0/INT External Interrupt Flag bit

1 = The RB0/INT external interrupt occurred (must be cleared in software)

0 = The RB0/INT external interrupt did not occur

bit 0 RBIF: RB Port Change Interrupt Flag bit

1 = At least one of the RB7:RB4 pins changed state; a mismatch condition will continue to set the bit. Reading PORTB will end the mismatch condition and allow the bit to be cleared (must be cleared in software).

0 = None of the RB7:RB4 pins have changed state

PIE1 REGISTER (ADDRESS 8Ch)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
PSPIE(1)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE
bit7							bit0

bit 7 **PSPIE(1):** Parallel Slave Port Read/Write Interrupt Enable bit

1 = Enables the PSP read/write interrupt

0 = Disables the PSP read/write interrupt

bit 6 **ADIE**: A/D Converter Interrupt Enable bit

1 = Enables the A/D converter interrupt

0 = Disables the A/D converter interrupt

bit 5 **RCIE**: USART Receive Interrupt Enable bit

1 = Enables the USART receive interrupt

0 = Disables the USART receive interrupt

PIE1 Continue …

bit 4 **TXIE**: USART Transmit Interrupt Enable bit
1 = Enables the USART transmit interrupt
0 = Disables the USART transmit interrupt

bit 3 **SSPIE**: Synchronous Serial Port Interrupt Enable bit
1 = Enables the SSP interrupt
0 = Disables the SSP interrupt

bit 2 **CCP1IE**: CCP1 Interrupt Enable bit
1 = Enables the CCP1 interrupt
0 = Disables the CCP1 interrupt

bit 1 **TMR2IE**: TMR2 to PR2 Match Interrupt Enable bit
1 = Enables the TMR2 to PR2 match interrupt
0 = Disables the TMR2 to PR2 match interrupt

bit 0 **TMR1IE**: TMR1 Overflow Interrupt Enable bit
1 = Enables the TMR1 overflow interrupt
0 = Disables the TMR1 overflow interrupt

PIE2 REGISTER (ADDRESS 8Dh)

U-0	R/W-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0
-	Reserved	-	EEIE	BCLIE	-	-	CCP2IE
bit7							bit0

bit 7 **Unimplemented:** Read as '0'

bit 6 **Reserved**: Always maintain this bit clear

bit 5 **Unimplemented:** Read as '0'

bit 4 **EEIE**: EEPROM Write Operation Interrupt Enable

1 = Enable EE Write Interrupt

0 = Disable EE Write Interrupt

bit 3 **BCLIE**: Bus Collision Interrupt Enable

1 = Enable Bus Collision Interrupt

0 = Disable Bus Collision Interrupt

bit 2-1 **Unimplemented:** Read as '0'

bit 0 **CCP2IE**: CCP2 Interrupt Enable bit

1 = Enables the CCP2 interrupt

0 = Disables the CCP2 interrupt

PIR1 REGISTER (ADDRESS 0Ch)

R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
PSPIF(1)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF
bit7							bit0

bit 7 **PSPIF(1):** Parallel Slave Port Read/Write Interrupt Flag bit

1 = A read or a write operation has taken place (must be cleared in software)

0 = No read or write has occurred

bit 6 **ADIF**: A/D Converter Interrupt Flag bit

1 = An A/D conversion completed

0 = The A/D conversion is not complete

bit 5 **RCIF**: USART Receive Interrupt Flag bit

1 = The USART receive buffer is full

0 = The USART receive buffer is empty

bit 4 **TXIF**: USART Transmit Interrupt Flag bit

1 = The USART transmit buffer is empty

0 = The USART transmit buffer is full

PIR1 Continue…

bit 3 **SSPIF**: Synchronous Serial Port (SSP) Interrupt Flag

1 = The SSP interrupt condition has occurred, and must be cleared in software before returning from the Interrupt Service Routine. The conditions that will set this bit are:

- SPI - A transmission/reception has taken place.
- I^2C Slave - A transmission/reception has taken place.
- I^2C Master- A transmission/reception has taken place.
  - The initiated START condition was completed by the SSP module.
  - The initiated STOP condition was completed by the SSP module.
  - The initiated Restart condition was completed by the SSP module.
  - The initiated Acknowledge condition was completed by the SSP module.
  - A START condition occurred while the SSP module was idle (Multi-Master system).
  - A STOP condition occurred while the SSP module was idle (Multi-Master system).

0 = No SSP interrupt condition has occurred.

PIR1 Continue…

bit 2 **CCP1IF**: CCP1 Interrupt Flag bit

Capture mode:

1 = A TMR1 register capture occurred (must be cleared in software)

0 = No TMR1 register capture occurred

Compare mode:

1 = A TMR1 register compare match occurred (must be cleared in software)

0 = No TMR1 register compare match occurred

PWM mode:

Unused in this mode

bit 1 **TMR2IF**: TMR2 to PR2 Match Interrupt Flag bit

1 = TMR2 to PR2 match occurred (must be cleared in software)

0 = No TMR2 to PR2 match occurred

bit 0 **TMR1IF**: TMR1 Overflow Interrupt Flag bit

1 = TMR1 register overflowed (must be cleared in software)

0 = TMR1 register did not overflow

PIR2 REGISTER (ADDRESS 0Dh)

R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
PSPIF(1)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF
bit7							bit0

bit 7 **Unimplemented:** Read as '0'

bit 6 **Reserved**: Always maintain this bit clear

bit 5 **Unimplemented:** Read as '0'

bit 4 **EEIF**: EEPROM Write Operation Interrupt Flag bit

1 = The write operation completed (must be cleared in software)

0 = The write operation is not complete or has not been started

bit 3 **BCLIF**: Bus Collision Interrupt Flag bit

1 = A bus collision has occurred in the SSP, when configured for I2C Master mode

0 = No bus collision has occurred

PIR2 Continue …

bit 2-1 **Unimplemented:** Read as '0'

bit 0 **CCP2IF**: CCP2 Interrupt Flag bit

Capture mode:

1 = A TMR1 register capture occurred (must be cleared in software)

0 = No TMR1 register capture occurred

Compare mode:

1 = A TMR1 register compare match occurred (must be cleared in software)

0 = No TMR1 register compare match occurred

PWM mode:

Unused

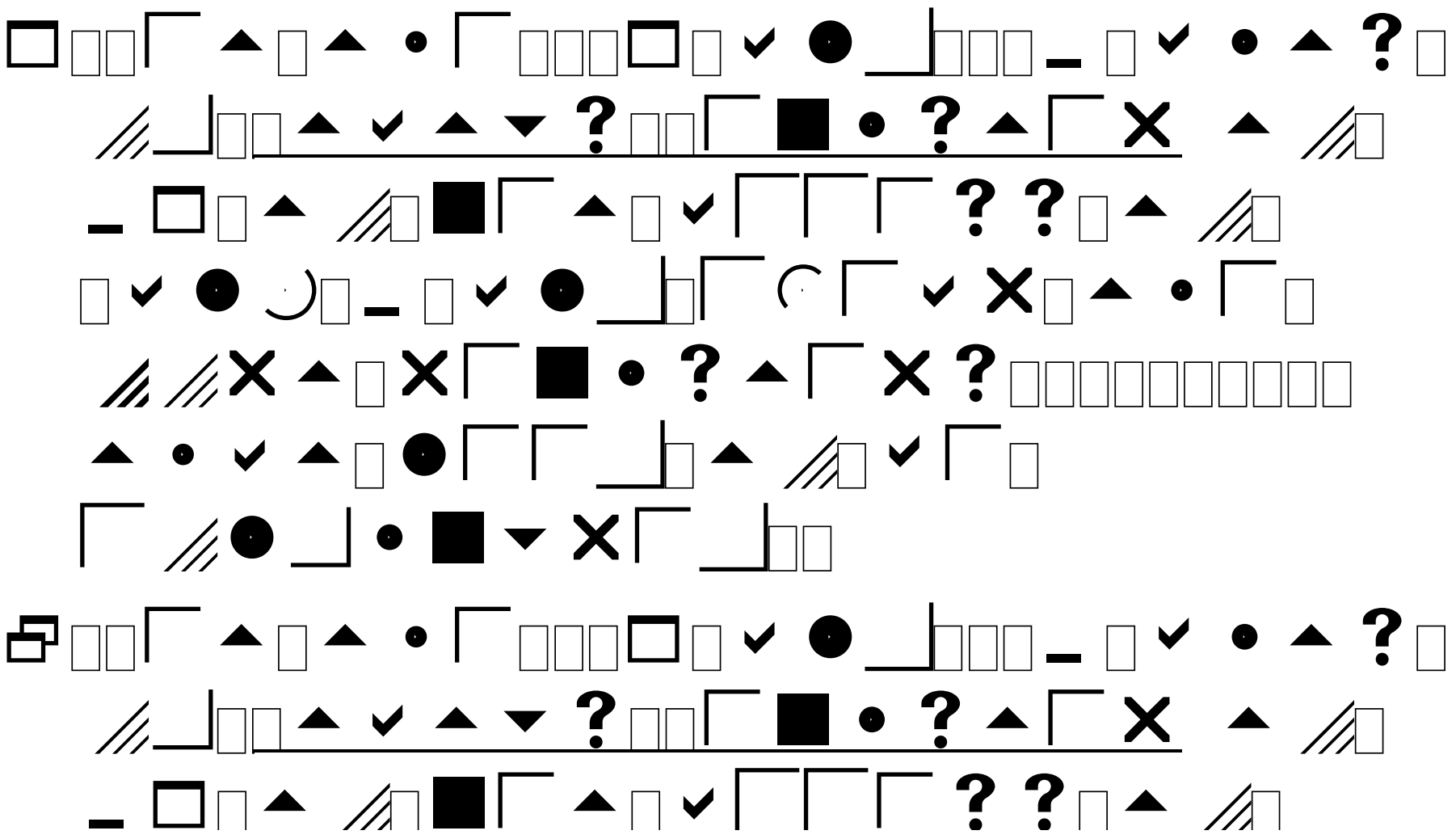
SECTION 2

INPUT/OUTPUT INTERFACE

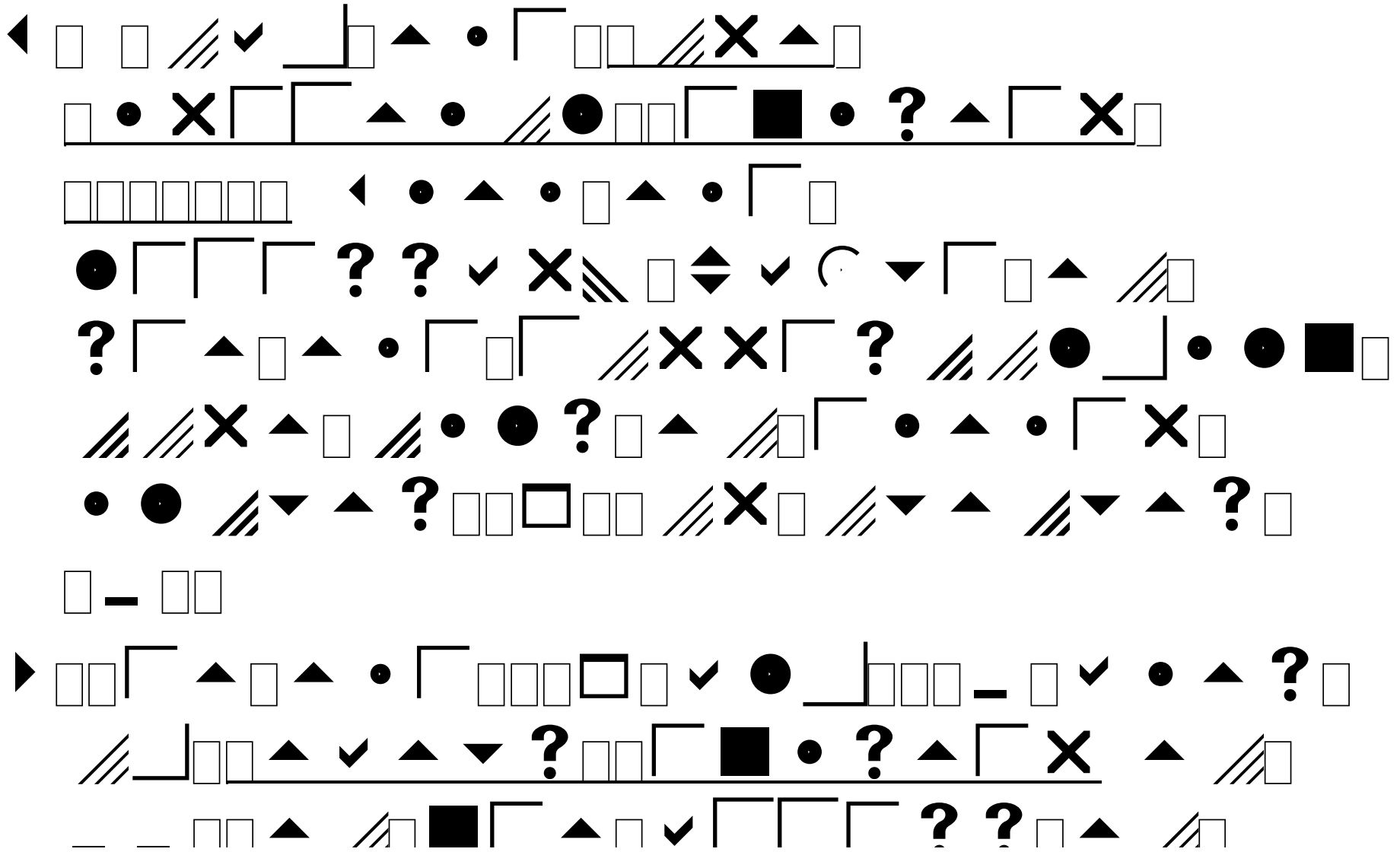
I/O PORTS

- Port A, B, C, D and E are I/O ports which can be configured based on the requirement,
- Some pins for these I/O ports are multiplexed with an alternate function for the peripheral features on the device,
- In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

I/O Ports Configuration



I/O Ports Configuration



PORTA and the TRISA Register

- PORTA is a 6-bit wide, bi-directional port.
- The corresponding data direction register is TRISA. Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a Hi-Impedance mode). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin).
- Reading the PORTA register reads the status of the pins, whereas writing to it will write to the port latch.

EXAMPLE : INITIALIZING PORTA

```
BCF     STATUS, RP0   ;
BCF     STATUS, RP1   ; Bank0
CLRF    PORTA         ; Initialize PORTA by
                      ; clearing output
                      ; data latches
BSF     STATUS, RP0   ; Select Bank 1
MOVLW   0x06          ; Configure all pins
MOVWF   ADCON1        ; as digital inputs
MOVLW   0xCF          ; Value used to
                      ; initialize data
                      ; direction
MOVWF   TRISA         ; Set RA<3:0> as inputs
                      ; RA<5:4> as outputs
                      ; TRISA<7:6>are always
                      ; read as '0'.
```

PORTB and the TRISB Register

- PORTB is an 8-bit wide, bi-directional port. The corresponding data direction register is TRISB.

- Four of the PORTB pins, RB7:RB4, have an interrupt-on-change feature. Only pins configured as inputs can cause this interrupt to occur (i.e., any RB7:RB4 pin configured as an output is excluded from the interrupt-on-change comparison). The input pins (of RB7:RB4) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB7:RB4 are OR'ed together to generate the RB Port Change Interrupt with flag bit RBIF (INTCON<0>).

PORTB and the TRISB Register

- The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

  a) Any read or write of PORTB. This will end the mismatch condition.

  b) Clear flag bit RBIF.

- A mismatch condition will continue to set flag bit RBIF. Reading PORTB will end the mismatch condition and allow flag bit RBIF to be cleared.
- This interrupt-on-mismatch feature, together with software configurable pull-ups on these four pins, allow easy interface to a keypad and make it possible for wake-up on key depression

PORTB FUNCTIONS

Name	Bit#	Function
RB0/INT	0	I/O pin or external interrupt input. Internal software programmable weak pull-up.
RB1	1	I/O pin. Internal software programmable weak pull-up.
RB2	2	I/O pin. Internal software programmable weak pull-up
RB3/PGM(3)	3	I/O pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB4	4	I/O pin (…). Internal software programmable weak pull-up.
RB5	5	I/O pin (…). Internal software programmable weak pull-up.
RB6/PGC	6	I/O pin (…) or In-Circuit Debugger pin. Internal software programmable weak pull-up. Serial programming clock.
RB7/PGD	7	I/O pin (…) or In-Circuit Debugger pin. Internal software programmable weak pull-up. Serial programming clock.

SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Value on: POR, BOR	Value on all other resets
06h, 106h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
86h, 186h	TRISB	PORTB Data Direction Register								1111 1111	1111 1111
81h, 181h	OPTION_REG	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111

PORTD FUNCTIONS

Name	Bit#	Function
RD0/PSP0	bit0	Input/output port pin or parallel slave port bit 0.
RD1/PSP1	bit1	Input/output port pin or parallel slave port bit 1.
RD2/PSP2	bit2	Input/output port pin or parallel slave port bit 2.
RD3/PSP3	bit3	Input/output port pin or parallel slave port bit 3.
RD4/PSP4	bit4	Input/output port pin or parallel slave port bit 4.
RD5/PSP5	Bit5	Input/output port pin or parallel slave port bit 5.
RD6/PSP6	bit6	Input/output port pin or parallel slave port bit 6.
RD7/PSP7	bit7	Input/output port pin or parallel slave port bit 7.

SUMMARY OF REGISTERS ASSOCIATED WITH PORTD

Address	Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Value on: POR, BOR	Value on all other RESETS
08h	PORTD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx xxxx	uuuu uuuu
88h	TRISD	PORTD Data Direction Register								1111 1111	1111 1111
89h	TRISE	IBF	OBF	IBOV	PSPMODE	-	PORTE Data Direction Bits			0000-1111	0000-1111

SECTION 3

TIMERS

TIMERS

There are three different TIMERS in PIC16F877.

1) TIMER0: 8 bit timer/counter with a prescaler,
2) TIMER1: 16 bit timer/counter,
3) TIMER2: 8 bit timer with a presacaler and a postscaler.

TIMER0 MODULE

- Timer0 module features:
  - 8-bit timer/counter
  - Readable and writable
  - 8-bit software programmable prescaler
  - Internal or external clock select
  - Interrupt on overflow from FFh to 00h
  - Edge select for external clock

TIMER0 MODULE

- **Timer Mode** is selected by clearing bit T0CS (OPTION_REG<5>). In Timer mode, the Timer0 module will increment every instruction cycle (without pre-scaler). If the TMR0 register is written, the increment is inhibited for the following two instruction cycles. The user can work around this by writing an adjusted value to the TMR0 register.

- **Counter Mode** is selected by setting bit T0CS (OPTION_REG<5>). In Counter mode, Timer0 will increment either on every rising, or falling edge of pin RA4/T0CKI.

Timer0 Interrupt

- The TMR0 interrupt is generated when the TMR0 register overflows from FFh to 00h.
- This overflow sets bit T0IF (INTCON<2>).
- The interrupt can be masked by clearing bit T0IE (INTCON<5>).
- Bit T0IF must be cleared in software by the Timer0 module Interrupt Service Routine before re-enabling this interrupt.

OPTION_REG Register (Address 81h, 181h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	TO	PD	Z	DC	C

bit7 bit0

bit7 RBPU: PORT B Pull-up Enable bit

1=PORT B pull-ups are disabled

0=PORT B pull-ups are enabled by individual port latch values

bit6 INTEDG: Interrupt Edge Select bit

1=Interrupt on rising edge of RB0/INT pin

0=Interrupt on falling edge of RB0/INT pin

bit 5 T0CS: TMR0 Clock Source Select bit

1=Transition on RA4/T0CKI pin

0=Internal instruction cycle clock (CLKOUT)

bit 4 T0SE: TMR0 Source Edge Select bit

1=Increment on high-to-low transition on RA4/T0CK1 pin

0=Increment on low-to-high transition on RA4/T0CK1 pin

OPTION Register Continue

bit 3 PSA: Pre-scalar Assignment bit

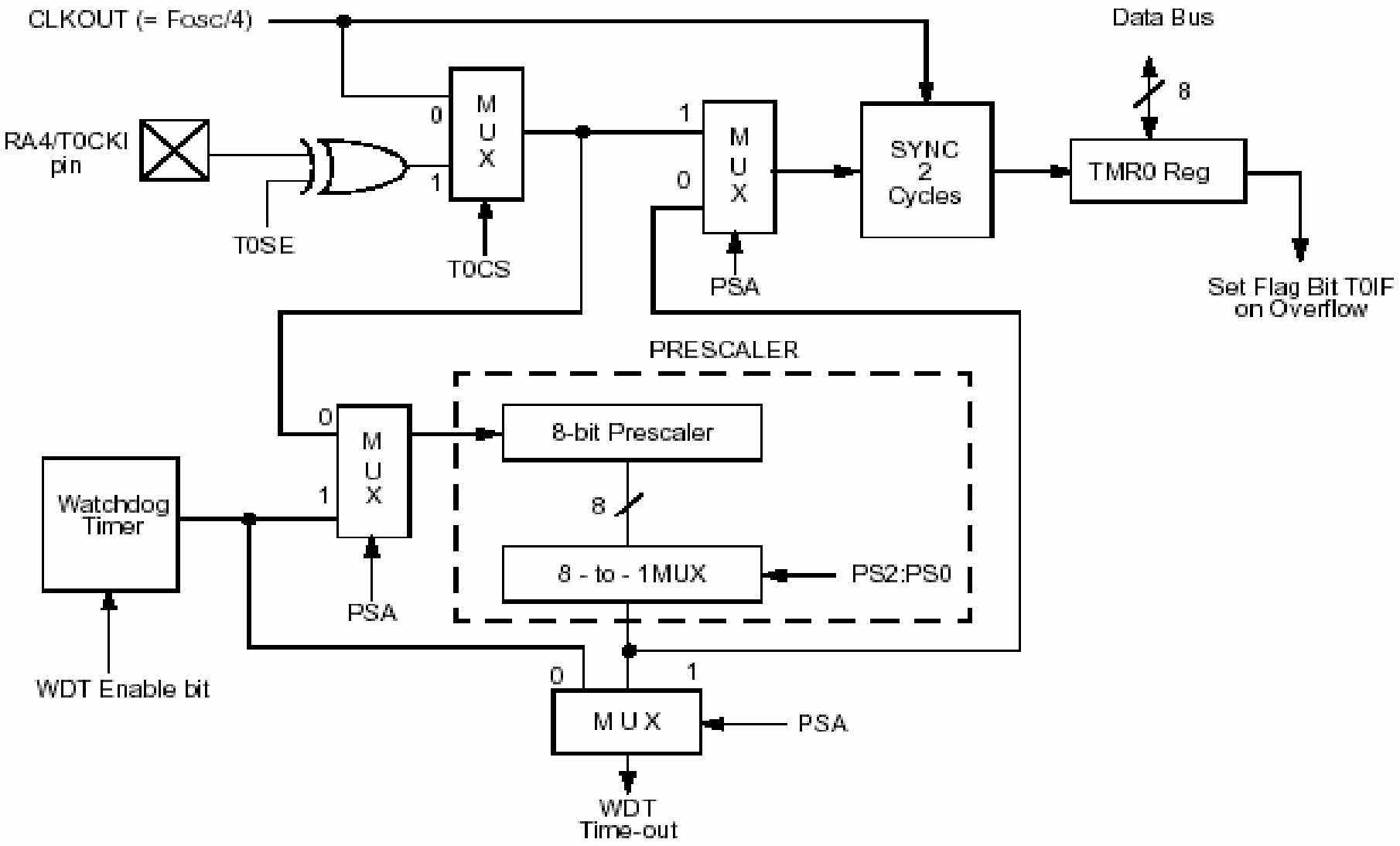
1=Pres-Scalar is assigned to the WDT

0=Pre-scalar is assigned to the Timer0 module

bit 2-0 PS2:PS0: Pre-scalar Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1:2	1:1
001	1:4	1:2
010	1:8	1:4
011	1:16	1:8
100	1:32	1:16
101	1:64	1:32
110	1:128	1:64
111	1:256	1:128

BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



SECTION 4

A/D (ANLOG TO DIGITAL) CONVERSION

ANALOG-TO-DIGITAL CONVERTION

- A very useful feature of the micorcontroller for sensing, monitoring and controlling the the external signals .
- The A/D converter converts the analog input signal (mostly in the range of 0 to 5 V) and then the result is stored in some specified register.
- The accuracy depends upon the number of the bits. 16F877 has 10 bit A/D converter.

ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

- Analog-to-Digital (A/D) Converter module has five inputs for the 28-pin devices and eight for the other devices.

- The A/D conversion of the analog input signal results in a corresponding 10-bit digital number.

- **A/D module Registers.**
  - A/D Result High Register (ADRESH)
  - A/D Result Low Register (ADRESL)
  - A/D Control Register0 (ADCON0)
  - A/D Control Register1 (ADCON1)

ADRESL Registers

- The ADRESL registers contain the 10-bit result of the A/D conversion.

- When the A/D conversion is complete, the result is loaded into this A/D result register pair, the GO/DONE bit (ADCON0<2>) is cleared and the A/D interrupt flag bit ADIF is set.

Configuring Analog Port Pins

- The ADCON1 and TRIS registers control the operation of the A/D port pins.

- The port pins that are desired as analog inputs must have their corresponding TRIS bits set (input).

A/D Conversions

- After the A/D conversion is aborted, a 2TAD wait is required before the next acquisition is started.
- After this 2TAD wait, acquisition on the selected channel is automatically started.
- The GO/DONE bit can then be set to start the conversion.

A/D RESULT REGISTERS

- The A/D module gives the flexibility to left or right justify the 10-bit result in the 16-bit result register.
- The A/D Format Select bit (ADFM) controls this justification.
- When an A/D result will not overwrite these locations (A/D disable), these registers may be used as two general purpose 8-bit registers.

A/D Conversion Steps

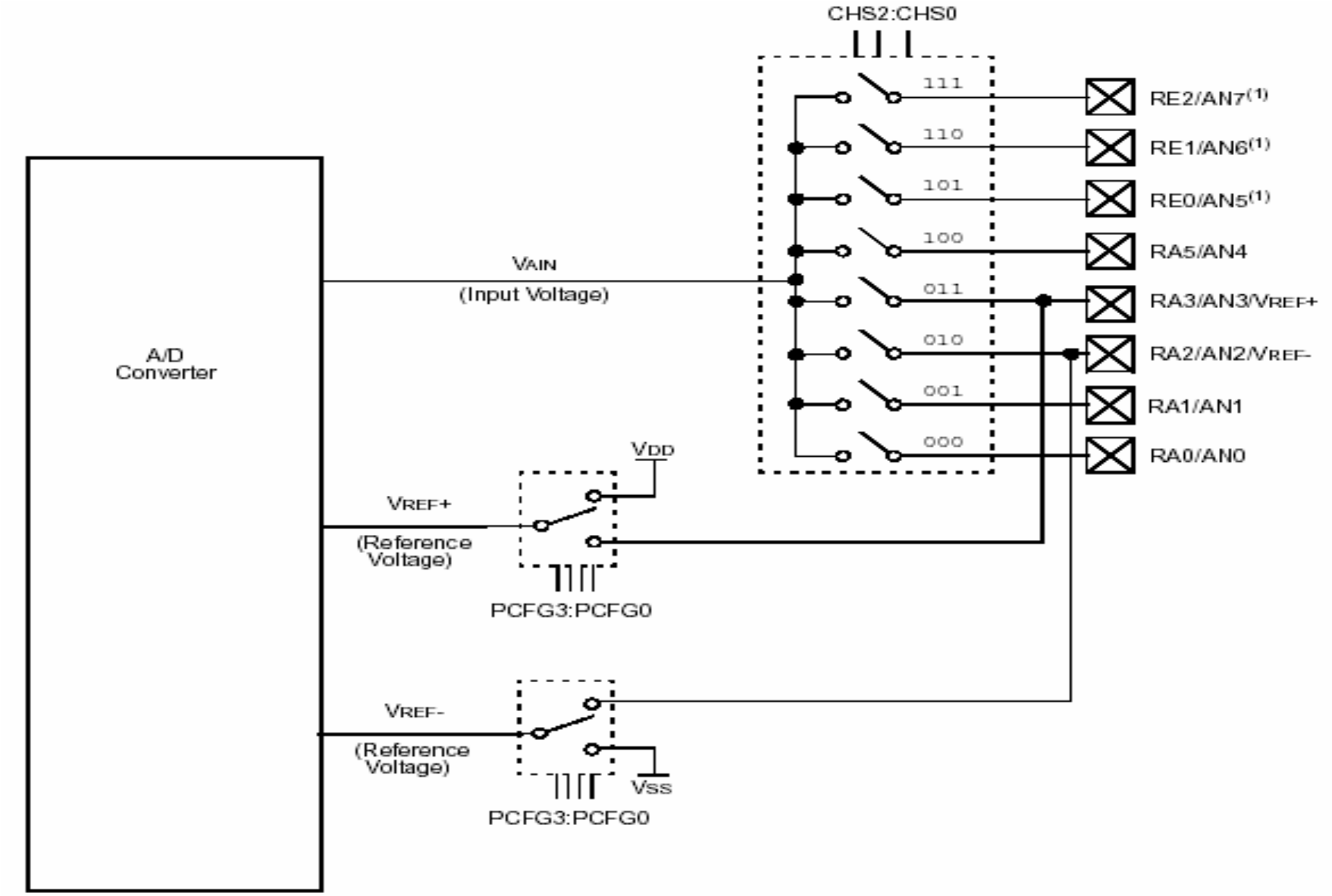
These steps should be followed for doing an A/D

- Conversion:
  1. Configure the A/D module:
     - Configure analog pins/voltage reference and digital I/O (ADCON1)
     - Select A/D input channel (ADCON0)
     - Select A/D conversion clock (ADCON0)
     - Turn on A/D module (ADCON0)
  2. Configure A/D interrupt (if desired):
     - Clear ADIF bit
     - Set ADIE bit
     - Set PEIE bit
     - Set GIE bit
  3. Wait the required acquisition time.

…continue

4. Start conversion:
    - Set GO/DONE bit (ADCON0)
5. Wait for A/D conversion to complete, by either:
    - Polling for the GO/DONE bit to be cleared (with interrupts enabled); OR
    - Waiting for the A/D interrupt
6. Read A/D result register pair (ADRESH: ADRESL), clear bit ADIF if required.
7. For the next conversion, go to step 1 or step 2, as required. The A/D conversion time per bit is defined as TAD. A minimum wait of 2TAD is required before the next acquisition starts.

A/D BLOCK DIAGRAM



ADCON0 REGISTER (ADDRESS: 1Fh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	-	ADON
bit7							bit0

bit 7-6 ADCS1:ADCS0: A/D Conversion Clock Select bits

00 = FOSC/2

01 = FOSC/8

10 = FOSC/32

11 = FRC (clock derived from the internal A/D module RC oscillator)

bit 5-3 CHS2:CHS0: Analog Channel Select bits

000 = channel 0, (RA0/AN0)

001 = channel 1, (RA1/AN1)

010 = channel 2, (RA2/AN2)

011 = channel 3, (RA3/AN3)

100 = channel 4, (RA5/AN4)

101 = channel 5, (RE0/AN5)**(1)**

110 = channel 6, (RE1/AN6)**(1)**

111 = channel 7, (RE2/AN7)**(1)**

ADCON0 Continue..

bit 2 **GO/DONE:** A/D Conversion Status bit

If ADON = 1:

1 = A/D conversion in progress (setting this bit starts the A/D conversion)

0 = A/D conversion not in progress (this bit is automatically cleared by hardware when the A/D conversion is complete)

bit 1 **Unimplemented**: Read as '0'

bit 0 **ADON**: A/D On bit

1 = A/D converter module is operating

0 = A/D converter module is shut-off and consumes no operating current

ADCON1 REGISTER (ADDRESS: 9Fh)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/DONE	-	ADON

bit7 bit0

bit 7 ADFM: A/D Result Format Select bit

1 = Right justified. 6 Most Significant bits of ADRESH are read as ‘0’.

0 = Left justified. 6 Least Significant bits of ADRESL are read as ‘0’.

bit 6-4 Unimplemented: Read as '0'

bit 3-0 PCFG3:PCFG0: A/D Port Configuration Control bits:

Port Configuration Control Bits

PCFG3:PCFG0	AN7[1] RE2	AN6[1] RE1	AN5[1] RE0	AN4 RA5	AN3 RA3	AN2 RA2	AN1 RA1	AN0 RA0	VREF+	VREF-	CHAN/ Refs[2]
0000	A	A	A	A	A	A	A	A	VDD	VSS	8/0
0001	A	A	A	A	VREF+	A	A	A	RA3	VSS	7/1
0010	D	D	D	A	A	A	A	A	VDD	VSS	5/0
0011	D	D	D	A	VREF+	A	A	A	RA3	VSS	4/1
0100	D	D	D	D	A	D	A	A	VDD	VSS	3/0
0101	D	D	D	D	VREF+	D	A	A	RA3	VSS	2/1
011x	D	D	D	D	D	D	D	D	VDD	VSS	0/0
1000	A	A	A	A	VREF+	VREF-	A	A	RA3	RA2	6/2

Configuration Control Bits Cont.

PCFG3:PCFG0	AN7[1]/RE2	AN6[1]/RE1	AN5[1]/RE0	AN4/RA5	AN3/RA3	AN2/RA2	AN1/RA1	AN0/RA0	V_{REF+}	V_{REF-}	CHAN/Refs[2]
1001	D	D	A	A	A	A	A	A	V_{DD}	V_{SS}	6/0
1010	D	D	A	A	V_{REF+}	A	A	A	RA3	V_{SS}	5/1
1011	D	D	A	A	V_{REF+}	V_{REF-}	A	A	RA3	RA2	4/2
1100	D	D	D	A	V_{REF+}	V_{REF-}	A	A	RA3	RA2	3/2
1101	D	D	D	D	V_{REF+}	V_{REF-}	A	A	RA3	RA2	2/2
1110	D	D	D	D	D	D	D	A	V_{DD}	V_{SS}	1/0
1111	D	D	D	D	V_{REF+}	V_{REF-}	D	A	RA3	RA2	½

A=Analog input D=Digital I/O

SECTION 5

RS 232 SERIAL COMMUNICAITON,

UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRNSMITTER (USART)

USART

- The Universal Synchronous Asynchronous Receiver Transmitter (USART) module is one of the two serial I/O modules. (USART is also known as a Serial communications Interface or SCI.)
- The USART can be configured as a full duplex asynchronous system that can communicate with peripheral devices such as CRT terminals and personal computers, or it can be configured as a half duplex synchronous system that can communicate with peripheral devices such as A/D or D/A integrated circuits, serial EEPROMs etc.

USART

- The USART can be configured in the following modes:
  - Asynchronous (full duplex)
  - Synchronous - Master (half duplex)
  - Synchronous - Slave (half duplex)
- Bit SPEN (RCSTA<7>) and bits TRISC<7:6> have to be set in order to configure pins RC6/TX/CK and RC7/RX/DT as the Universal Synchronous Asynchronous Receiver Transmitter.

TXSTA: TRANSMIT STATUS AND CONTROL REGISTER (ADDRESS 98h)

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R-1	R/W-0
CSRC	TX9	TXEN	SYNC	-	BRGH	TRMT	TX9D
bit7							bit0

bit 7 **CSRC:** Clock Source Select bit

Asynchronous mode:

Don't care

Synchronous mode:

1 = Master mode (clock generated internally from BRG)

0 = Slave mode (clock from external source)

bit 6 **TX9**: 9-bit Transmit Enable bit

1 = Selects 9-bit transmission

0 = Selects 8-bit transmission

bit 5 **TXEN**: Transmit Enable bit

1 = Transmit enabled

0 = Transmit disabled

Note: SREN/CREN overrides TXEN in SYNC mode.

TXSTA Continue…

bit 4 **SYNC**: USART Mode Select bit
1 = Synchronous mode
0 = Asynchronous mode

bit 3 **Unimplemented:** Read as '0'

bit 2 **BRGH**: High Baud Rate Select bit
Asynchronous mode:
1 = High speed 0; BRGH= F0SC/(64(X+1))
0 = Low speed 1; BRGH= F0SC(16(X+1))
Synchronous mode:
Unused in this mode

bit 1 **TRMT**: Transmit Shift Register Status bit
1 = TSR empty
0 = TSR full

bit 0 **TX9D:** 9th bit of Transmit Data, can be parity bit

RCSTA: RECEIVE STATUS AND CONTROL REGISTER (ADDRESS 18h)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-x
SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D
bit7							bit0

bit 7 **SPEN:** Serial Port Enable bit

1 = Serial port enabled (configures RC7/RX/DT and RC6/TX/CK pins as serial port pins)

0 = Serial port disabled

bit 6 **RX9**: 9-bit Receive Enable bit

1 = Selects 9-bit reception

0 = Selects 8-bit reception

bit 5 **SREN**: Single Receive Enable bit

Asynchronous mode:

Don’t care

Synchronous mode - master:

1 = Enables single receive

0 = Disables single receive

This bit is cleared after reception is complete.

Synchronous mode - slave:

Don’t care

RCSTA Continue…

bit 4 **CREN**: Continuous Receive Enable bit

Asynchronous mode:

1 = Enables continuous receive

0 = Disables continuous receive

Synchronous mode:

1 = Enables continuous receive until enable bit CREN is cleared (CREN overrides SREN)

0 = Disables continuous receive

bit 3 **ADDEN:** Address Detect Enable bit

Asynchronous mode 9-bit (RX9 = 1):

1 = Enables address detection, enables interrupt and load of the receive buffer when RSR<8> is set

0 = Disables address detection, all bytes are received, and ninth bit can be used as parity bit

bit 2 **FERR**: Framing Error bit

1 = Framing error (can be updated by reading RCREG register and receive next valid byte)

0 = No framing error

bit 1 **OERR**: Overrun Error bit

1 = Overrun error (can be cleared by clearing bit CREN)

0 = No overrun error

bit 0 **RX9D:** 9th bit of Received Data (can be parity bit, but must be calculated by user firmware)

USART Baud Rate Generator (BRG)

- Given the desired baud rate and FOSC, the nearest integer value for the SPBRG register can be calculated using the formula in Table 10-1.
- From Baud Rate Formula, the error in baud rate can be determined.

SYNC	BRGH = 0 (Low Speed)	BRGH = 1 (High Speed)
0	(Asynchronous) Baud Rate = Fosc/(64(X+1))	Baud Rate = Fosc/(16(X+1))
1	(Synchronous) Baud Rate = Fosc/(4(X+1))	N/A

X = value in SPBRG (0 to 255)

REGISTERS ASSOCIATED WITH BAUD RATE GENERATOR

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
98h	TXSTA	CSRC	TX9	TXEN	SYNC	–	BRGH	TRMT	TX9D	0000 -010	0000 -010
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented, read as '0'. Shaded cells are not used by the BRG.

USART Asynchronous Mode

- The most common data format is 8-bits.
- An on-chip, dedicated, 8-bit baud rate generator can be used to derive standard baud rate frequencies from the oscillator.
- The USART transmits and receives the LSb first.
- The transmitter and receiver are functionally independent, but use the same data format and baud rate.
- The baud rate generator produces a clock, either x16 or x64 of the bit shift rate, depending on bit BRGH (TXSTA<2>).

- Asynchronous mode is selected by clearing bit SYNC (TXSTA<4>).

- The USART Asynchronous module consists of the following important elements:
  - Baud Rate Generator
  - Sampling Circuit
  - Asynchronous Transmitter
  - Asynchronous Receiver

USART ASYNCHRONOUS TRANSMITTER

- The heart of the transmitter is the transmit (serial) shift register (TSR).
- The shift register obtains its data from the read/write transmit buffer, TXREG.
- The TXREG register is loaded with data in software.
- The TSR register is not loaded until the STOP bit has been transmitted from the previous load.
- As soon as the STOP bit is transmitted, the TSR is loaded with new data from the TXREG register (if available).
- Once the TXREG register transfers the data to the TSR register (occurs in one TCY), the TXREG register is empty and flag bit TXIF (PIR1<4>) is set.
- This interrupt can be enabled/disabled by setting/clearing enable bit TXIE (PIE1<4>).
- Flag bit TXIF will be set, regardless of the state of enable bit TXIE and cannot be cleared in software.
- Transmission is enabled by setting enable bit TXEN (TXSTA<5>).
- The actual transmission will not occur until the TXREG register has been loaded with data and the baud rate generator (BRG) has produced a shift clock (Figure 10-2).

Asynchronous Transmission Steps:

1. Initialize the SPBRG register for the appropriate baud rate. If a high speed baud rate is desired, set bit BRGH .
2. Enable the asynchronous serial port by clearing bit SYNC and setting bit SPEN.
3. If interrupts are desired, then set enable bit TXIE.
4. If 9-bit transmission is desired, then set transmit bit TX9.
5. Enable the transmission by setting bit TXEN, which will also set bit TXIF.
6. If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
7. Load data to the TXREG register (starts transmission).
8. If using interrupts, ensure that GIE and PEIE (bits 7 and 6) of the INTCON register are set.

REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
0Bh, 8Bh, 10Bh,18Bh	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	R0IF	0000 000x	0000 000u
0Ch	PIR1	PSPIF(1)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	—	FERR	OERR	RX9D	0000 -00x	0000 -00x
19h	TXREG	USART Transmit Register								0000 0000	0000 0000
8Ch	PIE1	PSPIE(1)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
99h	SPBRG	Baud Rate Generator Register								0000 0000	0000 0000

USART ASYNCHRONOUS RECEIVER

- The heart of the receiver is the receive (serial) shift register (RSR).
- After sampling the STOP bit, the received data in the RSR is transferred to the RCREG register (if it is empty).
- If the transfer is complete, flag bit RCIF (PIR1<5>) is set.
- The actual interrupt can be enabled/disabled by setting/clearing enable bit RCIE (PIE1<5>).
- Flag bit RCIF is a read only bit, which is cleared by the hardware. It is cleared when the RCREG register has been read and is empty.
- The RCREG is a double buffered register (i.e., it is a two deep FIFO). It is possible for two bytes of data to be received and transferred to the RCREG FIFO and a third byte to begin shifting to the RSR register. On the detection of the STOP bit of the third byte, if the RCREG register is still full, the overrun error bit OERR (RCSTA<1>) will be set. The word in the RSR will be lost. Framing error bit FERR (RCSTA<2>) is set if a STOP bit is detected as clear.

Asynchronous Reception Steps

1. Initialize the SPBRG register for the appropriate baud rate. If a high speed baud rate is desired, set bit BRGH (Section 10.1).
2. Enable the asynchronous serial port by clearing bit SYNC and setting bit SPEN.
3. If interrupts are desired, then set enable bit RCIE.
4. If 9-bit reception is desired, then set bit RX9.
5. Enable the reception by setting bit CREN.
6. Flag bit RCIF will be set when reception is complete and an interrupt will be generated if enable bit RCIE is set.
7. Read the RCSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
8. Read the 8-bit received data by reading the RCREG register.
9. If any error occurred, clear the error by clearing enable bit CREN.
10. If using interrupts, ensure that GIE and PEIE (bits 7 and 6) of the INTCON register are set.

Useful Web Links

Getting Software simulator, assembler and Programmer, MPLAB IDE
http://www.microchip.com/11110/pline/tools/picmicro/devenv/mplabi/index.htm

2) Getting Started with MPLAB IDE – A Tutorial Chapter # 3

http://www.microchip.com/11110/pline/tools/picmicro/devenv/mplabi/1460/index.htm

3) Data Sheet for the PIC16F877

http://www.microchip.com/11110/pline/picmicro/families/16f87x/devices/16f877/index.htm