IEEE
International Electron Devices Mini-Colloquium

Monday September 8, 2008
8:00 AM – 1:00PM

Pontificia Universidad Javeriana

Auditorio Marino Troncoso

Program

8:30	9:00	Coffee and Pastries	
9:00	9:15	Welcome Note	**German Yamhure**
9:15	10:15	Nanoelectronics: an overview of the Past, Present and Future of electronic devices	**Francisco Garcia**
10:15	11:15	Future Gate Stack Technology	**Hiroshi Iwai**
11:15	12:15	Microelectronic Reliability Topics for Advanced CMOS and SiGe Technologies	**Fernando Guarín**
12:15	12:20	Closing Remarks	**Jose David Cely**
12:15	2:00	Networking and Working Lunch (speakers and faculty)	

IEEE International Electron Devices Mini-Colloquium

Tuesday September 9, 2008
8:00 AM – 1:00PM

Universidad de los Andes

Auditorio Mario Laserna

Program

8:30	9:00	Coffee and Pastries	
9:00	9:15	Welcome Note	**Antonio García**
9:15	9:30	EDS Overview	**Francisco García**
9:30	10:30	Métodos basados en Integración para Extraer Parámetros y evaluar distorsión en Dispositivos y Circuitos	**Adelmo Ortiz**
10:30	11:30	The National Laboratory of Nanoelectronics *Research activities on fabrication of semiconductor devices in Mexico*	**Edmundo A. Gutiérrez**
11:30	12:30	Processing and Defect Control of Advanced Ge Devices	**Cor Claeys**
12:30	12:40	Closing Remarks	**Jose David Cely**
12:45	2:30	Networking and Working Lunch (speakers and faculty)	

Welcome

On behalf of the Electron Device chapter of the Colombia Section, we would like to welcome you to the IEEE International Electron Devices Mini-Colloquium. This colloquium is packed with wealth of knowledge and information, with six internationally recognized distinguished lecturers presenting on different fields of interest in Electron Device Society. The colloquium will provide an excellent opportunity to attendees to interact and exchange their ideas with these experts. This colloquium is also aimed at providing networking opportunity for the students and faculty of various universities with IEEE members and non-members in Colombia.

We would like to thank all the sponsors of this event that includes the IEEE Colombia Section, the Colombian Electron Device Chapter of, the IEEE Electron Devices Society

Last but not least, we thank all the distinguished lectures for taking time out of their busy schedules to come to Bogotá to participate in this event.

It is again our great honor and pleasure to extend a warm welcome to everyone attending this International Electron Devices Mini-Colloquium.

Colombia EDS Chapter

Acknowledgements

The organizers would like to thank following individuals for their help and support that made this Mini-Colloquium possible

José David Cely	IEEE Colombia Section President
Antonio García	Universidad de los Andes
German Yamhure	Universidad Javeriana
Cor Claeys	IMEC Belgium
Juin J. Liou	University of Central Florida U.S
Hiroshi Iwai	Tokio Insitute of Technology Japan
Francisco García	Universidad Simón Bolívar Venezuela
Adelmo Ortiz	Universidad Simón Bolívar Venezuela
Fernando Guarin	IBM Microelectronics, U.S

Hiroshi Iwai

Hiroshi Iwai was born in Tokyo, Japan, on April 25, 1949. He received the B.E. and Ph.D. degrees in electrical engineering from the University of Tokyo, Japan in 1972 and 1992, respectively. In 1973, he joined the Research and Development Center of Toshiba Corporation, Kawasaki, Japan, where he developed the first generation of Toshiba's NMOS LSI technology. From April of 1999 to present, he is a professor of Dept. of Advanced Applied Electronics, Interdisciplinary Graduate School of Science and Engineering, Tokyo Institute of Technology, Nagatsuta, Yokohama, Japan. Currently, he is also a professor of Frontier Collaborative Research Center and a Research Planning Officer of Strategic Research Planning Office in the institute. Since joining Toshiba, he has developed several generations of high density static RAM's, dynamic RAM's and logic LSI's including CMOS, bipolar, and Bi-CMOS devices. He has authored and coauthored more than 200 papers. He has served on many committees of conferences and editors of journals. His awards include Local Commendation for Invention from Japan Institute of Invention and Innovation (1990, 2005), Grand Prize of Nikkei BP Technology Awards (1994), IEEE EDS Paul Rappaport Award (1994), IEICE ES Electronics Award (1998), IEEE EDS J.J.Ebers Award (2001). His current research interests are Nano CMOS and Emerging Technologies: High–k gate insulator, plasma doping, Ni salicide, RF CMOS modeling, Ge transistor, etc. Dr. Iwai is, a fellow of IEEE, a member of Electrochemical Society, a member of the Japan Society Applied Physics, a member of the Institute of Electronics, Information and Communication Engineers of Japan, and a member of the Institute of Electrical Engineers of Japan.

Future Gate Stack Technology

So far HfO_2 based gate dielectrics are being introduced to advanced logic integrated circuits from 45 nm commercial technology node, there are many issues for the high-k and metal gate stack for use for the next generation.

First of all, the current HfO_2 based oxides need intentionally grown interfacial layer in order to arrange a good interface between the silicon surface and the gate insulator, and hence to suppress the mobility degradation of the channel carrier of MOSFETs. This interfacial layer is typically made of SiO_xN_y and its typical EOT is 0.7 nm. Maybe the interfacial layer EOT could be reduced to around 0.5 nm. However, the SiO_xN_y interfacial layer will certainly prevent the total gate dielectric EOT reduction less than 0.7 nm almost impossible, and thus, direct contact of the high-k gate dielectrics with silicon would be inevitable. For the rare earth oxide material such as La_2O_3, we have already demonstrated very low interface state density of 6 X 10^{10} cm^{-2}, and nice peak mobility value of more than 300 $cm^2V^{-1}s^{-1}$ for channel electrons. However, this is supposed to be the hydrogen or maybe even OH termination effects of the dangling bonds at the Si surface. The hydrogen and OH are supposed to be introduced moisture absorption of water with the La_2O_3 exposure to air before the gate electrode deposition. The problem for this termination is that at least the interfacial concentration of the hydrogen decreases during the anneal at higher temperature above 300°C. Thus, the interface state density increases and the mobility degrades after higher temperature. Another problem is that higher temperature anneal around at 500°C make an interfacial silicate layer grow and this silicate layer increases the EOT of the gate oxide and interface state density. It is known that higher temperature annealing in hydrogen ambient decreases the interface state density, however the interfacial silicate layer formation is a problem. Another way to improve the interfacial layer is to add other 3rd elements, such as Al. It seems that the Al repairs the oxygen

vacancy and probably annihilates the interface states. We did confirm these effects but they are not sufficiently large at this moment and process optimization or maybe quest of more effective another 3rd element is necessary.

Further solution is to insert higher k interfacial layer than that of SiO_xN_y. Using Sc_2O_3 as the interfacial layer, we have achieved good suppression of the silicate interfacial layer growth at 500^oC. However, interface state density between the Sc_2O_3 and Si is still necessary to be improved at this moment.

Fermi level pinning is another important factor to be considered. Eventually, the process temperature for the high-k will goes down to 400 ~ 500^oC, as the gate stack process moves from ‘gate first’ to ‘gate last’ process and the Fermi level pinning effect will become less significant. However, it cannot be ignored. Addition of the 3rd element will be again a solution.

When, the EOT value of the gate insulator becomes less than 1 nm, the channel carrier mobility degradation due to the remote Coulomb and remote roughness scattering caused by the charge and roughness at the interface of high-k gate dielectrics and gate electrode becomes very significant. Thus, good mobility cannot be obtained without improving that interface.

For the middle and long term issues for the gate stack, we have to consider that the MOSFETs structure will change from planar to 3-dimensional structure, such as FinFET. Eventually, the FinFET will changes to nanowire MOSFETs, and maybe to CNT MOSFETs. Or maybe other semiconductor substrate such as GaAs or Ge could be used. Source and drain will be changed from semiconductor to metal. In the case of metal source drain, maybe process temperature could be decreased to 300~400oC, which would solve some critical issues of interfacial problems of high-k/semiconductor and high-k/metal gate. Some more details of gate stack for next 25 years will be explained.

Fernando Guarín

Dr. Guarín is a Senior Engineer/Scientist at the IBM Microelectronics Semiconductor Research Development Center SRDC in East Fishkill N.Y. He received his BSEE from the "Pontificia Universidad Javeriana", in Bogotá, Colombia, the M.S.E.E. degree from the University of Arizona, and the Ph.D. in Electrical Engineering form Columbia University. His doctoral research studied the Molecular Beam Epitaxial growth of Silicon based alloys for device applications. He has been actively working in microelectronic reliability for over 27 years.

From 1980 until 1988 he was a member of the Military and Aerospace Operations division of National Semiconductor Corporation where he held positions both in engineering and management.

In 1988 he joined the IBM microelectronics division where he has worked in the reliability physics and modeling of Advanced Silicon Bipolar, CMOS and Silicon Germanium BiCMOS technologies. He has been the team leader for the qualification of several of IBM's deep submicron CMOS and SiGe technologies. He has also served as team leader for the reliability qualification of products across several fabrication lines including Burlington, Vt., Essonnes, France and the new 300 mm line in East Fishkill, NY. He is currently the team leader for the 32 nm Bulk CMOS Technology. Dr. Guarín holds 9 patents, has published more than 60 papers and several tutorials at the IEEE's International Reliability Physics Symposium. He is the Chair for the Electron Devices Society in the IEEE's Hudson Valley NY Chapter and is the local president of the Society of Hispanic Professional Engineers. Dr Guarín is an IEEE Fellow and a Distinguished Lecturer for the IEEE Electron Device Society.

Microelectronic Reliability Topics for Advanced CMOS and SiGe Technologies

As we continue the relentless drive towards smaller device feature sizes and higher levels of integration at the chip level, it has become increasingly evident that a judicious review and very complete understanding of the reliability mechanisms will be crucial for the successful introduction of the most advanced technologies that will be introduced in the near future.

The increased device count and process complexity, coupled with ever decreasing margins in voltage, geometry and the incorporation of new material systems like high and low k dielectrics, stress/strain layers, high conductivity interconnects will be discussed from the reliability perspective. A closer look will be given to the current status and challenges imposed by the major reliability mechanisms like; Hot Carriers, Bias Temperature Instabilities, self-heating effects, statistical variations (process and geometric), Power Supply Decoupling and Silicon Germanium Heterojunction Bipolar Transistors as well as electromigration issues. The implications of reliability induced parameter degradation and the mitigation of these effects will be analyzed and positioned in a practical perspective. The innovative practical use of reliability degradation mechanisms in circuit applications will also be discussed.

Edmundo A. Gutiérrez

Edmundo A. Gutiérrez-D., Ph.D.
Department of Electronics
National Institute for Astrophysics, Optics and Electronics (INAOE)
Puebla, MEXICO.

Prof. Dr. Edmundo A. Gutiérrez has published more than 100 papers and international conferences in the field of semiconductor device physics, modeling, simulation, sensors, and circuits. He is author of the book "Low Temperature Electronics, Physics, Devices, Circuits and Applications" (Academic Press, 2000). Prof. Gutierrez has supervised 4 M.Sc. and 10 PhD theses. He got his PhD on Applied Sciences from The catholic University of Leuven, Belgium, where he also spent 6 years as a research assistant at the Interuniversity MicroElectronics Center (IMEC) in the Advanced Silicon Processing Division.

He has been invited Professor at Simon Fraser University (Vancouver, Canada), University of Sao Paulo (Brazil), and the Technical University of Vienna, (Austria). From 2000 to 2002 was the Design Manager of the Motorola Mexico Center for Semiconductor Technology, and from 2005 to 2007 Research Manager of the Intel Mexico Research Center. Currently Prof. Gutierrez is with the Department of Electronics of the National Institute of Astrophysics, Optics and Electronics (INAOE) in Puebla, Mexico. Prof. Gutiérrez is member of the National Systems of Researchers (SNI level 2) of Mexico, and member of different Review Committees of the Mexico National Council of Science and Technology (CONACyT).

The National Laboratory of Nanoelectronics Research activities on fabrication of semiconductor devices in Mexico.

The National Laboratory of Nanoelectronics (LNN) is a Mexican initiatitive focused to strengthen the research activities on fabrication techniques for semiconductor devices, nano-structured semiconductor materials, and CMOS- and SiGe-compatibles semiconductor devices, such as sensors and transistors. The LNN is a 0.5 μm CMOS fabrication facility that besides the research activities, offers design and fabrication services to schools, universities, and research centers in Mexico. The LNN is also part of the Mexican network of MEM's,where it has the responsibility for the manufacturing of MEM's devices. The LNN is part of the Department of Electronics of the National Institute of Astrophysics, Optics and Electronics (INAOE), a federal research institute in Mexico, where the M.Sc. and Ph.D. students have access for the fabrication of semiconductor devices.

The research activities and industry projects that are related to the LNN activities will be presented, such as; low- and high-K dielectric for inter-dielectrics and gate oxides, GHz-CMOS compatible photodetectors, on-chip magnetic RFI detection, a-SiGe sensors, high-index Si crystal transistors, micro-machined devices, etc.

Cor L. Claeys

Cor Claeys was born in Antwerp, Belgium. He received the electrical-mechanical engineering degree in 1974 and the Ph.D. degree in 1979, both from the Katholieke Universiteit Leuven (KU Leuven), Belgium.

From 1974 to 1984 he was a Research Assistant and Staff Member, respectively, of the ESAT Laboratory of the KU Leuven and since 1990, a Professor. In 1984, he joined IMEC as Head of Silicon Processing Group. He is for IMEC on the management board of several projects funded by the European Commission. He is also a member of the European Expert Group on Nanosciences. His main interests are in general silicon technology for ULSI, device physics, including low-temperature operation, low frequency noise phenomena and radiation effects, and defect engineering and material characterization. He also authored and co-authored eight book chapters and more than 700 technical papers and conference contributions related to the above fields. He has been involved in the organization of a large number of international conferences and edited more than 35 Proceedings Volumes. He is an associated Editor for the *Journal of the Electrochemical Society*.

Prof. Claeys is a member of the European Material Research Society, a Senior Member of IEEE and a Fellow of the Electrochemical Society. He was the founder of the IEEE Electron Devices Benelux Chapter and was EDS Vice-President for Chapters and Regions during 2000-2006. Since 2000 he is an EDS Distinguished Lecture. In 2006, he has been elected as EDS President-Elect. He also received the IEEE Third Millennium Medal. Within the Electrochemical Society he has been serving in different committees and was Chair of the Electronics Division (2001-2003). In 2004 he received the Electronics Division Award of the ECS.

Processing and Defect Control of Advanced Ge Devices

The boost up the device performance, strain engineering is gaining much interest and has already been successfully implemented for 65 and 45 nm technology nodes. However, for sub 32 nm another interesting approach is based on using again Ge as a substrate. Worldwide there has been much interest in investigating the potential of Ge processing.

This presentation will review the advantages and challenges of advanced Ge processing for future logic applications. Attention will be given on the processing challenges such as ion implantation, shallow junctions, passivation, germanidation, contact technology, etc. For all the steps a good control of both the grown-in and the process-induced defects is crucial. Although very good electrical performances have been achieved for p-channel devices processed on Ge and GeOI high-mobility substrates, this is not the case for the n-channel ones. The future outlook will be briefly addressed.

Francisco García Sánchez

Ingeniero Electrónico, Magíster y Ph.D. por la Catholic University of America, Washington, D.C., EUA. Ha alcanzado el máximo nivel académico de Profesor Titular en el Departamento de Electrónica de la Universidad Simón Bolívar (USB), Caracas, Venezuela, en la que ha trabajado desde 1977.

Actualmente se desempeña en la USB como profesor contratado de investigación, y sirve de consultor técnico en áreas de su competencia. El Prof. García Sánchez ha desempeñado en la USB diversos cargos, tales como Coordinador de Estudios Profesionales y de Estudios de Postgrado en Ingeniería Electrónica, Coordinador de Investigación y Desarrollo de Ingeniería y Ciencias Aplicadas, Jefe del Laboratorio de Electrónica del Estado Sólido, y miembro electo de los Consejos Académico y Superior de la Universidad. En 1979 fundó el Laboratorio de Electrónica del Estado Sólido de la USB.

La actividad docente del Prof. García Sánchez, tanto de pregrado como de postgrado, se ha orientado principalmente a dispositivos semiconductores y sus aplicaciones en microelectrónica. También ha sido tutor de proyectos de grado y de maestría en ingeniería electrónica y física, y de tesis de doctorado en ingeniería.

El Prof. García Sánchez ha participado y ha sido responsable de proyectos nacionales e internacionales de investigación, y su grupo de investigación mantiene relaciones de colaboración con centros e investigadores a nivel mundial. Las áreas de investigación en las que ha trabajado, junto a sus compañeros de grupo durante su trayectoria profesional, abarcan temas sobre semiconductores policristalinos binarios y ternarios, el desarrollo de métodos sencillos para su fabricación, tales como la impresión serigráfica y la pulverización pirolítica, y su uso en dispositivos fotovoltaicos de película delgada; la caracterización dieléctrica de materiales compuestos, cerámicas y tejidos biológicos; y la modelación y extracción de parámetros de modelos compactos de dispositivos semiconductores, uniones, celdas solares, y transistores de efecto de campo, TFT, SOI, amorfos, multicompuerta, y nanométricos. Ha publicado más de 120 de trabajos de investigación en revistas especializadas y memorias de conferencias arbitradas internacionales de reconocido prestigio, incluyendo numerosos artículos invitados y conferencias invitadas y plenarias. Es coautor de un libro de texto, de capítulos de libros, y ha sido editor de obras colectivas.

El Prof. García Sánchez ha formado parte y presidido numerosos comités de congresos nacionales e internacionales. Fue fundador y pertenece al comité de seguimiento de la “IEEE International Caribbean Conference on Devices, Circuits, and Systems” que se viene realizando en la cuenca del Caribe bianualmente desde 1995. El Prof. García Sánchez forma parte de consejos editoriales y es árbitro de revistas técnicas nacionales e internacionales. Su nombre aparece en el “Golden List of Reviewers” de las publicaciones de la “Electron Devices Society” (EDS) del “Institute of Electrical and Electronics Engineers” (IEEE). También cuenta con amplia experiencia en asesoría, promoción, planificación, gerencia y evaluación de actividades de investigación científica a nivel tanto nacional como internacional. Entre otras actividades, fue Coordinador Nacional del área de Electrónica del Programa BID-CONICIT de Nuevas Tecnologías de Venezuela, ha sido Presidente de la Comisión de Ingeniería, Tecnología y Ciencias de la Tierra del Sistema de Promoción del Investigador (SPI) de Venezuela, durante seis años fue miembro de la Comisión Dictaminadora Externa del Instituto Nacional de Astrofísica, Óptica y Electrónica (INAOE) de México, ha formado parte del “IEEE Undergraduate Teaching Award and Leon K. Kirchmayer Graduate Teaching Award Committee”, y actualmente es miembro del “Masters Student Fellowship and PhD Student Fellowship Committee” de la EDS del IEEE. El Prof. García Sánchez

está clasificado en el Sistema de Promoción del Investigador de Venezuela (SPI) como Investigador *IV* (máximo nivel). Su trabajo de investigación ha merecido diversos premios y distinciones nacionales e internacionales. En 2003 fue designado como "Distinguished Lecturer" de la EDS del IEEE. En febrero de 2007, justo al cumplir treinta años de actividad académica, le fue conferido el título honorario de "Profesor Emérito de la Universidad Simón Bolívar". El Prof. García Sánchez participa activamente en sociedades científicas y profesionales. En Venezuela es miembro fundador de la Sociedad Galileana, en la que se ha desempeñado como su Tesorero, Secretario, y Vicepresidente. Pertenece a la Asociación Venezolana para el Avance de la Ciencia. Fue Presidente fundador del Capítulo Venezolano conjunto de las Sociedades de "Electron Devices" (EDS), "Circuits and Systems", y "Power Electronics" del IEEE. Actualmente el Prof. García Sánchez es Vicepresidente para Latinoamérica y el Caribe del Subcomité de Regiones y Capítulos de la EDS del IEEE, y ha sido reelecto como miembro de su Comité Administrativo (EDS AdCom).

Nanoelectrónica: una rápida mirada al pasado, presente y futuro de los dispositivos electrónicos

Adelmo Ortiz Conde

Ingeniero Electrónico de la Universidad Simón Bolívar, (Caracas, 1979), y Maestría y Ph.D de "University of Florida" (Gainesville, 1982 y 1985 respectivamente).Desde 1979 a 1980, trabajo como instructor en el Departamento de Electrónica de la Universidad Simón Bolívar. Desde 1985 a 1987, trabajo con "Bell Laboratories", en Reading, PA, en el área de circuitos integrados de alto voltaje. Desde 1987 ha estado con el Departamento de Electrónica de la Universidad Simón Bolívar y fue ascendido a Profesor Titular en 1995. El ha estado de permiso con Florida International University (Miami, FL), desde Septiembre a Diciembre de 1993, con "University of Central Florida" (Orlando, FL), desde Enero a Agosto de 1994, y nuevamente de Julio a Diciembre de 1998, y con CINVESTAV-IPN (Ciudad de México, México), desde Octubre 2000 a Febrero 2001.El Prof. Ortiz-Conde es coautor de un libro de texto, "Analysis and Design of MOSFETs: Modeling, Simulation and Parameter Extraction" (Boston, MA: Kluwer, 1998), de 76 publicaciones de investigación en revistas (incluyendo 4 artículos de revisión invitados) y 66 publicaciones de investigación en congresos internacionales (incluyendo 9 invitadas). Su área principal de interés es el modelaje y la extracción de parámetros en dispositivos semiconductores. El Prof. Ortiz-Conde es Miembro de Eta Kappa Nu, Tau Beta Pi, Phi Kappa Phi y la Sociedad Galileana. El es "IEEE EDS Distinguished Lecturer" y el presidente del capitulo "IEEE's CAS/ED/PE Venezuela". El fue Editor para la Región 9 de "IEEE EDS Newsletter" desde 2000 al 2005.El es Miembro del "Editorial Advisory Board" de "Microelectronics and Reliability". El ha sido miembro de la Comisión de Ingeniería y Ciencias Aplicadas del Programa de Promoción al Investigador. El está clasificado en el Sistema de Promoción del Investigador de Venezuela (SPI) como Investigador IV (máximo nivel). El ha sido Revisor de revistas y conferencias internacionales. Su nombre aparece en el "Golden List of Reviewers" de las publicaciones de la "Electron Devices Society" (EDS) del "Institute of Electrical and Electronics Engineers" (IEEE). El fue "General Chairperson" de "first IEEE International Caracas Conference on Devices, Circuits, and Systems" en 1995, el "Technical Chairperson" de la segunda, cuarta y quinta ediciones de esta conferencia en 1998, 2002 y 2004 respectivamente, y el "Chairperson of the Steering Committee" en el 2000.

Métodos basados en Integración para Extraer Parámetros y evaluar distorsión en Dispositivos y Circuitos

Se presenta una revisión del desarrollo de los métodos basados en integración para extraer parámetros en dispositivos semiconductores y circuitos. Estos métodos han originado procedimientos para evaluar la linealidad y la distorsión, basados en integración. El primer método, basado en integración, fue propuesto por Araujo en 1982, para la determinación de la resistencia en serie de una celda solar. La integración actúa como un filtro pasa bajo y por lo tanto tiende a disminuir los efectos de los errores experimentales en el procedimiento de extracción. El método de Araujo fue generalizado en 1995 para un dispositivo arbitrario de dos terminales y una resistencia en serie. En 1996 fue presentada la función integral D que elimina los efectos lineales cuando es aplicada a una función arbitraria. La primera aplicación de esta función fue la eliminación de los efectos de la resistencia en serie de un diodo. Esta función fue generalizada a una familia de funciones las cuales son capaces de eliminar cualquier coeficiente de un polinomio arbitrario. La función D fue usada en 2002 para diseñar, optimizar y fabricar un transconductor bipolar con máxima linealidad de la función de transferencia estática. Este transconductor estaba compuesto de dos bloques alineales paralelos

conectados: un transconductor del tipo tangente hiperbólica y un transconductor seno hiperbólico. Este diseño inspiró el desarrollo de un procedimiento para evaluar la distorsión armónica, usando la función D, cuando existe una armónica dominante. Un nuevo método, basado en integraciones sucesivas, fue presentado en 2007 para la extracción de coeficientes de un polinomio de orden n. Este nuevo método permite evaluar la distorsión armónica teniendo dos armónicas dominantes pero no es totalmente inmune al ruido experimental, debido a que involucra operaciones sin integraciones. Esta última limitación fue removida este año con un nuevo método que puede ser usado eficientemente para calcular la distorsión armónica en un dispositivo o circuito para cualquier amplitud, sin necesidad de realizar el análisis de Fourier. También revisaremos y escudriñaremos los siguientes métodos basados en integración para extraer el voltaje de umbral en MOSFETs, polarizados en la región lineal: (1) método integral; (2) método de transición; y (3) método de la diferencia normalizada de la integral mutua. También revisaremos los siguientes dos métodos basados en integración para extraer el voltaje de umbral en MOSFETs, polarizados en la región de saturación: (1) método de la función H y (2) método de la función G_1. Finalmente revisaremos un método, basado en integración, para evaluar la ubicación del máximo valor de una función con alto nivel de ruido.