(Please write your Exam Roll No.) Exam Roll No. 07716415 07

END TERM EXAMINATION

SIXTH SEMESTER [B.TECH/M.TECH] MAY-2010

Paper Code: IT 314
Paper ID: 15314
Subject: Digital system design (Batch 2006 Onwards)
Time: 3 Hours
Maximum Marks: 60

Note: Q no. 1 is compulsory. Attempt one question from each unit.

Q.1 (a) A gated D latch will hold its output value if G is 0, and the output follow D if G is 1. Write a VHDL description of a gated D latch using a process. (3)

(b) Briefly outline the purposes of the following VHDL modeling constructs: Entity declaration, behavioral architecture body, and Signal assignment statement. (3)

(c) Differentiate between Generate and Loop statement. (3)

(d) Explain the following with example: (3)

S'event
S'transaction
S'active
S'last active
S'last value
S'last event

(e) Draw the waveform of following: (3)

Z1 <= **transport** x **after** 10 ns;
Z2 <= x **after** 10 ns;
Z3 <= **reject** 4 ns x **after** 10 ns;

(f) Differentiate between compiler and synthesizer. (1)

(g) Differentiate between Simulator and Emulator. (1)

(h) Name any five HDLs. (1)

(i) Explain Delta delay. (1)

(j) Explain aliases. (1)

Unit - I

Q.2 (a) Design a 4-bitadder using a macro of half adder using VHDL. (5)

(b) Design a 3:8 Decoder using when-else statement using VHDL. (5)

OR

Q.2 (a) Explain Block statement with example. (5)

P.T.O.