/	(6)	Design a 7-segment display converter using VHDL.	(5)
0.4	(a)	us hanna tama dosener	(5)
	(b)	Explain the difference between Signal and Variable with example. Design a 4-bit asynchronous counter using VHDL.	(5)
() 5		OR	(5)
Q.5	(a)	Design a RAM using VHDL.	(5)
	(b)	Design universal shift register using VHDL.	(5)
0.7	(a) '(a	Place and the state and the state Unit -III	(5)
Q.6	(a)	Differentiate between Procedure and Functions.	(5)
	(b)	Explain Operator overloading. Give example.	(5)
- 10	1	OR OR	(5)
Q.7/	(a)	Explain organization of RTL system.	
	(b)	Explain Data subsystem of RTL system.	(5)
		Unit-IV	(5)
0.8/	(a)	Write a short note on FPGA.	
1	(b))	Explain the writing procedure of the state o	(5)
	(,)	Explain the writing procedure of Test bench in VHDL.	(5)
0.9	(0)	Water and	£ 2 /.
Q.7	(a)	Write a short note on CPLD.	(5)
	(b)	Explain declaration procedure of File and Tex I/O.	(5)
			(3)

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Deceder us are when the statement using VIII