	(b)	Design a 7-segment display converter using VHDL.	(5)
		Unit - II	
Q. 4	(a)	Explain the difference between Signal and Variable with example.	(5)
	(b)	Design a 4-bit asynchronous counter using VHDL.	(5)
		OR	
Q.5	(a)	Design a RAM using VHDL.	(5)
	(b)	Design universal shift register using VHDL.	(5)
		Unit -III	
Q.6	(a)	Differentiate between Procedure and Functions.	(5)
	(b)	Explain Operator overloading. Give example.	(5)
		OR	
Q.7	(a)	Explain organization of RTL system.	(5)
	(b)	Explain Data subsystem of RTL system.	(5)
		Unit-IV	
Q.8	(a)	Write a short note on FPGA.	(5)
	(b))	Explain the writing procedure of Test bench in VHDL.	(5)
		OR	
Q.9	(a)	Write a short note on CPLD.	(5)
	(b)	Explain declaration procedure of File and Tex I/O.	(5)

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