Novel Frame Buffer Pixel Circuits for Liquid-Crystal-on-Silicon Microdisplays

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***Abstract*—A 32×16 liquid-crystal-on-silicon (LCOS) backplane with novel frame buffer pixels is designed and fabricated using the AMI Semiconductor's 0.5-μm double-poly triple-metal CMOS process. The three novel pixel circuits described herein increase the brightness of an XGA LCOS microdisplay by at least 36% without sacrificing image contrast ratio. The increase of brightness is attributed to maximizing overall image view time, allowing an image to be displayed at full contrast while the next image is buffered onto the backplane. The new circuits achieve this by removing charge sharing and charge inducement problems shown in previously proposed frame buffer pixel circuits. Voltages on the pixel electrodes measured through rail-to-rail operational amplifiers with negative feedback vary from 0 to 4.25 V (6-V power source). All data voltage levels remain constant over a frame time with less than 1% drop, thus ensuring maximum contrast ratio. Modeling and experimental measurement on the fabricated chip show that these pixel circuits outperform all others to date based on storage time, data storage level, and potential for highest contrast ratio with maximum brightness.**

***Index Terms*—Frame buffer pixel, liquid-crystal-on-silicon (LCOS), microdisplay.**

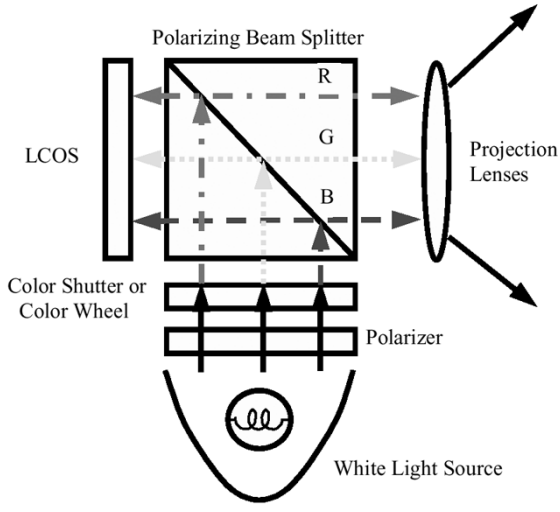

Fig. 1. Field sequential color projection display with a single microdisplay.

I. Introduction

LIQUID-crystal-on-silicon (LCOS) microdisplays utilize high birefringence and low operating voltage liquid crystal (LC) materials aligned on top of a single crystal silicon circuit to control and maintain the director distribution of the LC for high-resolution small-sized displays [3]. Single crystal silicon VLSI technology is well recognized as a competitive alternative to active matrix liquid crystal display (AMLCD) [4]. The advantages include higher electron mobility producing better electron characteristics and the use of more mature, off the shelf technology. Furthermore, complicated column and row driver circuits and pixel arrays can be achieved through a high level of integration, yielding a compact-sized display with higher resolution and potentially very low cost. Microdisplays based on single crystal silicon generically operate in reflective mode for achieving higher pixel fill factors, as compared with transmissive-mode devices that do not employ expensive microlens arrays. Due to the low cost, high efficiency of light, and compact system size achievable with LCOS technology, these devices have been integrated into camera view finders, head mounted displays (HMD) [5], head-up-displays [6], and projection display systems such as front and rear projectors for high-definition televisions and computer monitors [7].

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One of the main applications of LCOS technology is in projection display systems. The front projector is very commonly used in business and educational settings, while rear projection displays are considered promising candidates for home theater systems. The contemporary standard LCOS projection display uses three microdisplay panels, one for each primary color. The advantage of the three-panel design is that the images have maximum brightness. However, the disadvantage is the need for complicated and expensive optics to separate the colors and difficulty in alignment of red, green, and blue images, which increases manufacturing cost. These disadvantages go away with single panel architecture known as field sequential color (FSC) systems, as shown in Fig. 1. With FSC displays, a full color image is divided into three subframes in which red, green, and blue beams are separately modulated by a single LCOS microdisplay in rapid sequence and projected onto a screen. The three images are temporally integrated by the eye over one frame time and a full color image is perceived. The optical architecture of the single panel system is simple in that it contains a single PBS, an LCOS display, a polarizer and an RGB shutter or a color wheel, which temporally filters red, green, and blue beams from a white light source. The simplicity increases manufacturing yield and provides the added advantages of a more compact size and lower cost system. Moreover, the single or two panel design has a shorter back focal length compared with the three panel structure, which improves system etendue and brightness [8]. However, the disadvantage of single-panel architecture is that it is inherently one-third as bright as its three-panel

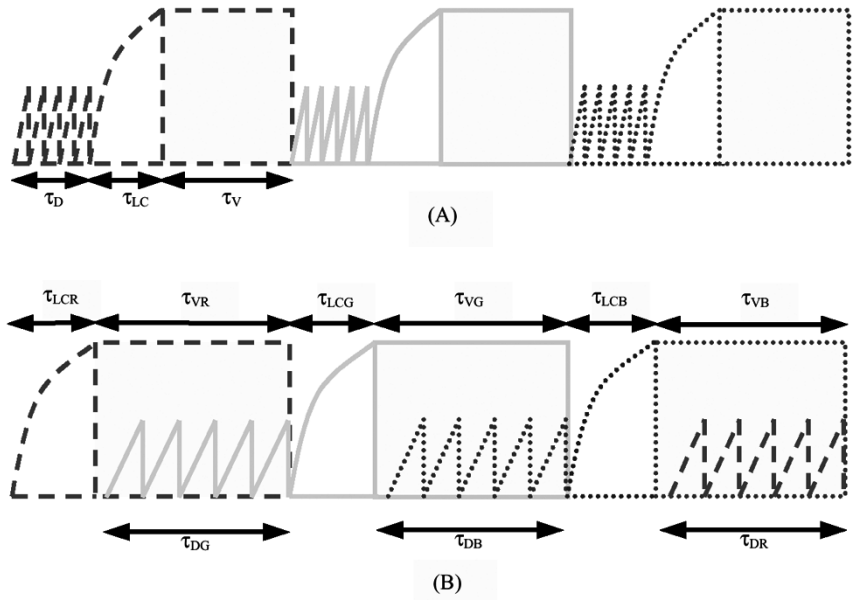

Fig. 2. Illustrations of (a) line-at-a-time driving scheme and (b) frame-at-a-time driving scheme.

cousin because FSC systems filter out at least two-thirds of light while displaying each image subframe.

AMLCDs employ a single thin-film transistor (TFT) or two terminal devices such as metal–insulator–metal (MIM) and various diodes integrated at each element to isolate the pixel storage node from the row and column bus lines. AMLCDs using amorphous silicon TFT played a major role in liquid crystal display evolution because of the better image quality and higher resolution [9]. In these displays, data is addressed line-at-a-time. Three panel projectors take the full advantage of this driving method. In FSC system, however, the line-at-a-time driving method shown in Fig. 2(a) causes a critical tradeoff between brightness and contrast ratio due to three light sources (red, green, and blue) alternating in time. The image view time, indicated by τ_V, starts only after the data write time, $\tau_{\rm D}$, and LC switching time, $\tau_{\rm LC}$, has completed. The light sources illuminate the display only during the view time to achieve high image contrast ratio. In general, if the light source is turned ON during data write time and LC switching time, the image brightness increases and the image contrast ratio decreases. An XGA (1024×768 pixels) display, with 64 parallel digital inputs and shift registers operating at a shift register clock speed of 100 MHz (with 1 μs analog data settling time) requires a $\tau_{\rm D}$ of at least one millisecond. As display resolution grows from XGA to high-definition format SXGA (1696×1024 pixels) [10], $\tau_{\rm D}$ increases to several milliseconds. The increased data write time in a higher resolution display results in loss of image brightness, since the display is blanked during $\tau_{\rm D}$.

The loss of brightness in a color sequential multimedia projector in which a new image is updated at the frame rate of 180 Hz (5.5-ms sub-frame time) is significant (18%). An FSC projector operating at 360 Hz experiences a 36% loss of brightness for the same contrast. A minimum frame rate of 420 Hz is required for the FSC to overcome color breakup and other color sequential artifacts [11]. The tradeoff between brightness and contrast ratio gets worse as the display resolution increases or as frame frequency increases since the data write time becomes a greater fraction of the overall frame time. A frame buffer pixel delivers maximum brightness without decreasing image contrast ratio [12]. That is because it provides frame-at-a-time drive capability. In a frame-at-a-time driving scheme enabled by frame buffer pixel circuitry, data is written into a frame buffer while previous data is being displayed. The $\tau_{\rm D}$ is contained within τ_V as illustrated in Fig. 2(b). The image contrast ratio is defined by

$$\text{C.R.} = \frac{I_{\rm ON} - I_{\rm DARK}}{I_{\rm OFF} - I_{\rm DARK}} \tag{1}$$

where $I_{\rm ON}$, $I_{\rm OFF}$, and $I_{\rm DARK}$ represents the mean intensity of on, off, and dark states, respectively. The higher contrast ratio can compensate for loss of brightness in the FSC projector, improving the system brightness, since it can accommodate a brighter light source.

The frame-at-a-time driving scheme lessens the requirement on the operation speed of electronic circuits such as column and row shift registers and pixel as long as $\tau_{\rm D}$ is less than τ_V. In the line-at-a-time driving method, these circuits need to be designed for the fastest operation to keep the brightness loss small. However, with the frame-at-a-time driving scheme, the circuits can be designed moderately only to satisfy $\tau_{\rm D} < \tau_V$.

II. Background

The concept of a frame buffer pixel was first proposed by Shields [12] and more advanced alternatives for microdisplays were reported recently [13], [14]. The schematic of original pixel is given in Fig. 3(a). Initially, a voltage proportional to the data level is stored at the memory capacitor $C_{\rm mem}$ during $\tau_{\rm D}$ when the write signal is ON. The stored voltage is transferred to the pixel capacitor $C_{\rm pixel}$ when the read signal is applied

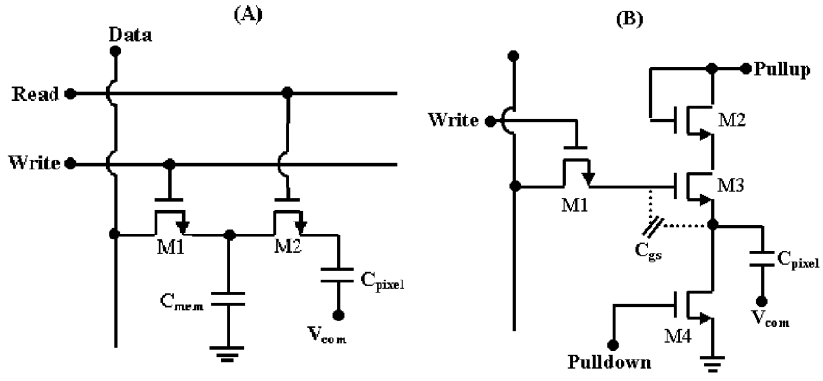

Fig. 3. Frame buffer pixel circuits. a) Proposed by Shields.b) Proposed by McKnight.

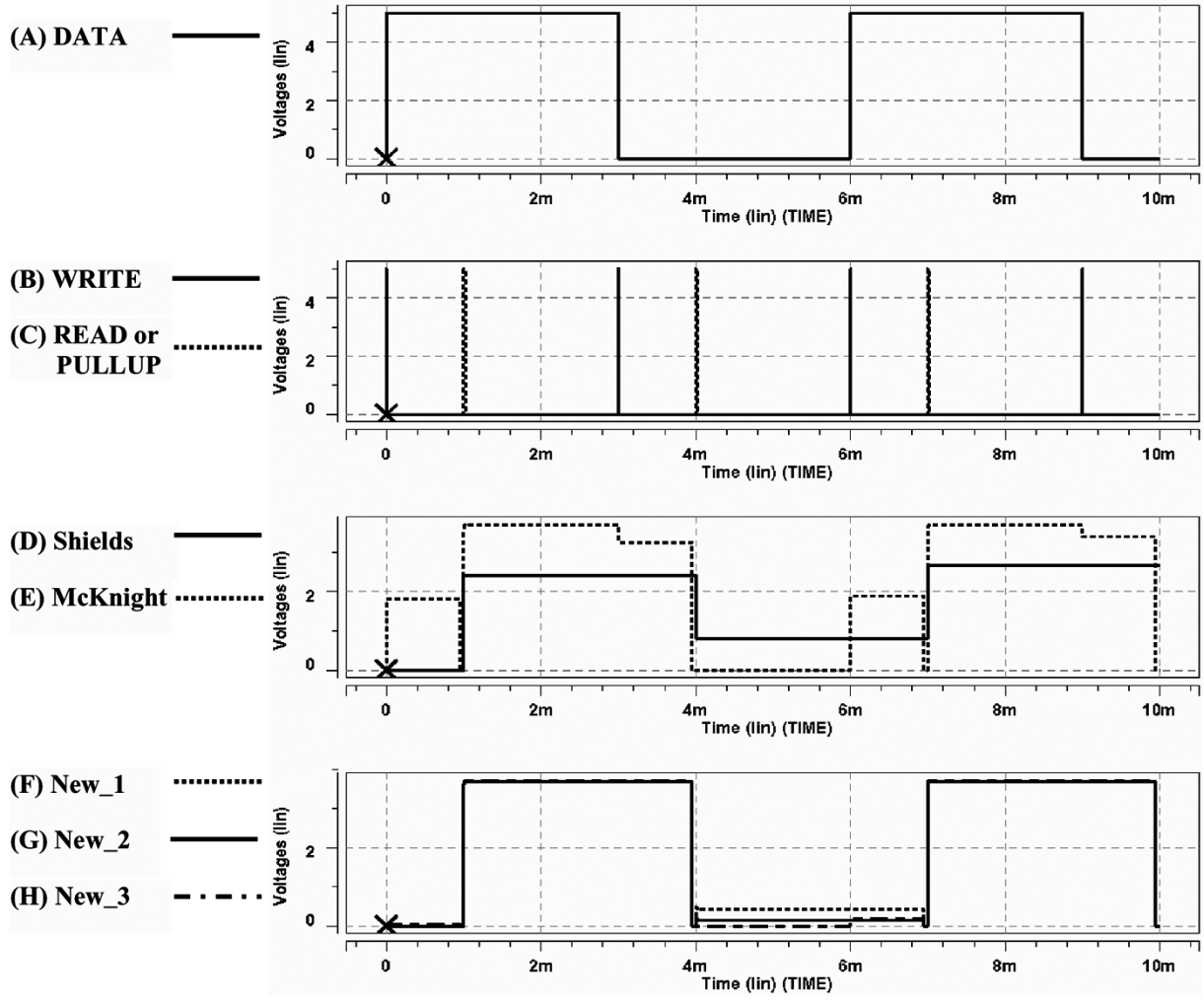

Fig. 4. HSPICE simulation results for the frame buffer pixels. Input signals: (a) data, (b) write, and (c) read. Voltages at $C_{\rm pixel}$: (d) Shields pixel; charge sharing between $C_{\rm pixel}$ and $C_{\rm mem}$ creates inconsistent voltage levels. (e) McKnight pixel; charge is induced at the $C_{\rm pixel}$ when data write signal is ON and the charge is maintained until the end of the frame. (f) New pixel with a gate capacitor. (g) New pixel with a separate poly–poly capacitor. (h) Modified pixel from McKnight to have a separate capacitor. New frame buffer pixels hold consistent and unchanging voltages during a frame time.

after data is written to the pixel. $V_{\rm com}$ is the voltage applied on the common electrode across liquid crystal layers. Some disadvantages of this pixel are revealed from HSPICE simulation as shown in Fig. 4(d). Using a memory capacitor of 400 fF and a pixel capacitor of 200 fF, we see charge sharing between $C_{\rm mem}$ and $C_{\rm pixel}$ when the read signal turned ON. The voltage written to the memory capacitor is determined from

$$\begin{aligned} V_{\rm mem} &= V_{\rm dd} - V_{\rm th} \quad \text{if } V_{\rm data} > V_{\rm dd} - V_{\rm th} \\ V_{\rm mem} &= V_{\rm data} \qquad\quad \text{if } V_{\rm data} \le V_{\rm dd} - V_{\rm th} \end{aligned} \tag{2}$$

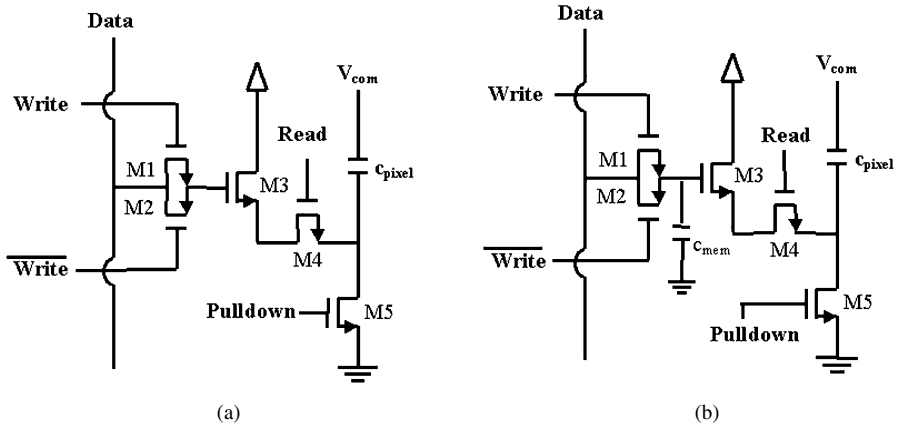

Fig. 5. New frame buffer pixel circuits: (a) with intrinsic gate capacitor and (b) with separate capacitor.

where $V_{\rm dd}$ is the power source voltage and $V_{\rm th}$ is the threshold voltage of the NMOS transistor M1. The voltage at the memory capacitor due to charge sharing can be approximated by

$$V_{\rm pixel} = V_{\rm mem}\left(\frac{C_{\rm mem}}{C_{\rm mem}+C_{\rm pixel}}\right) \tag{3}$$

where $V_{\rm mem}$ is the voltage written to the memory capacitor and $V_{\rm pixel}$ is the voltage at the pixel capacitor. The simulation shows that the voltage stored at the pixel capacitor is 2.39 V with the voltage drop of 1.0 V from the voltage initially stored at the memory capacitor. The voltage at the pixel calculated from (3) gives 2.41 V. The close agreement between the simulated value and calculation using the capacitance of the capacitors without parasitic capacitance and turn-on-resistance of the transistor controlled by the read signal is obtained. The capacitance of the memory capacitor has to be much larger than that of the pixel capacitor to minimize charge sharing, i.e., $C_{\rm mem} \gg C_{\rm pixel}$. This condition reduces the voltage drop at the pixel capacitor, but charge sharing always results in some voltage drop.

Notice that in the pixel circuit there is no way to drain off the charge stored on $C_{\rm pixel}$. This residual voltage produces inconsistent voltage level at the pixel capacitor regardless of input data. The direction of charge flow alternates back and forth from the higher voltage to the lower voltage between the $C_{\rm mem}$ and $C_{\rm pixel}$. It is difficult to optimize the memory and pixel capacitors to satisfy $C_{\rm mem} \gg C_{\rm pixel}$ with the voltage holding time of a few milliseconds and the pixel pitch of $10 \sim 20$ μm, which are the typical requirements of LCOS microdisplays. The optimization leads to either larger than normal pixel space or shorter holding time than one sub-frame time.

To overcome charge sharing and other drawbacks of Shield's frame buffer pixel, McKnight proposed the pixel circuit shown in Fig. 3(b) [13]. The buffered pixel has two additional transistors and utilizes the gate oxide of an NMOS transistor, M3, to serve as a memory capacitor. A voltage proportional to the data voltage is stored at the gate capacitor of M3 during the data write time when the write signal is ON. When the stored voltage increases such that $V_{\rm gs}$ of transistor M3 exceeds its threshold voltage, the transistor M3 conducts and current flows through the transistor. The pixel capacitor is charged by the current whose amount is controlled by the voltage at the memory capacitor. Charging the pixel capacitor does not happen until the pull-up transistor M2 is turned ON, since there is no actual current flowing through transistor M3 when transistor M2 is in the OFF state. A pull-down signal is applied just before the pull-up signal to drain all charge previously stored at the pixel capacitor. HSPICE simulation results are shown in Fig. 4(e). The conditions for the simulation are that the gate capacitance of M3 is 191.8 fF and the pixel capacitance is 200 fF.

There is no charge sharing between the memory capacitor and the pixel capacitor, and the brightness and contrast ratio can be expected to increase as compared with Shield's frame buffer pixel. The pixel capacitor is driven directly from the external power source and controlled only by the voltage stored at the gate capacitor of the transistor M3. However, as shown in Fig. 4(e), undesired charge is induced at the pixel capacitor when the write signal is applied. This charge inducement results from the parasitic capacitor $C_{\rm gs}$ of M3. The $C_{\rm gs}$ and $C_{\rm pixel}$ capacitors work as a voltage divider to determine the value of the induced voltage at the pixel capacitor during the data write time. With the parameters used in the simulation, a significant voltage is induced at the pixel capacitor during data writing time as shown in Fig. 4(e). The induced charge influences image quality and in particular degrades contrast ratio. To mitigate this effect, the ratio of the gate capacitance $C_{\rm gs}$ to the pixel capacitance $C_{\rm pixel}$ has to be decreased. McKnight's frame buffer pixel also has the disadvantage of a voltage-dependent gate capacitance, as described in Section III.

III. New Frame Buffer Pixel Designs

A. Using Transistor Gate as a Storage Element

A new frame buffer pixel circuit described in this paper and shown in Fig. 5(a) improves image quality by removing charge sharing and charge inducement [1]. The pass transistor M4 [see Fig. 5(a)] isolates the parasitic gate capacitance of transistor M3 from the pixel capacitor, preventing charge inducement when the write signal is turned ON. During this part of the cycle, the quantized data voltage level is stored at the memory capacitor, which is the gate of transistor M3. The stored voltage controls the current through it, charging the pixel capacitor in proportion to the voltage level when the read signal is applied. HSPICE

simulation shows there is no charge sharing and charge inducement during the data write time, as shown in Fig. 4(f). The HSPICE simulation was performed with the extracted netlist from the actual layout of the frame buffer pixel. The netlist includes transistor parasitics and interconnect routing. The transistor model used for the simulation contains BSIM v3.3, level 49 parameters for AMI Semiconductor's 0.5-μm process provided by MOSIS.[1] The gate capacitance of transistor M3 is 223 fF and that of the pixel capacitor is 200 fF. Voltage levels at the pixel capacitor remain constant with no fluctuation for entire frame time. The lowest voltage level displaying zero data has an offset voltage of 0.4 V. The offset voltage results from the charge stored at the source capacitor $C_{\rm S}$ of transistor M3. The charge stored at the source capacitor of transistor M3 is shared with the pixel capacitor when transistor M4 is turned ON. The offset voltage can be calculated from (2). This offset occurs only during data read time so that the offset voltage does not reduce contrast ratio, since we can set this offset voltage corresponding to the dark state to a new zero voltage. Thus, potentially maximum contrast ratio can be achieved.

The capacitance of $C_{\rm mem}$ and $C_{\rm pixel}$ can be optimized independently to hold the charge stored for one frame time since there is neither charge sharing between the capacitors nor charge inducement during the data write time. The capacitor optimization needs to take into account the subthreshold drain and photo-generated currents. The subthreshold current is defined by [15]

$$I_{\rm DS} \propto \left[1 - \exp\left(-\frac{qV_{\rm DS}}{kT}\right)\right] \times \exp\left(\frac{q(V_{\rm GS} - V_T)}{nkT}\right) \quad \text{for } V_{\rm GS} \ll V_{\rm VT} \quad (4)$$

where n is the ideality factor of the subthreshold current, varying between a value of one and two. The subthreshold current is much smaller than the photo-generated current, which depends on the illumination intensity and the specific device structures. The optimization is conducted with an assumed photo-generated current of $\sim$1 pA by adjusting the Gmin value in the HSPICE simulation. Under this condition, the capacitance of 200 fF is required to hold the charge to 95% of its initial value for a frame time of 5.5 ms, the sub-frame time for a color sequential display operating at 180 Hz. The size of the transistor and the poly-poly capacitor is adjusted to have the required capacitance using BSIM v3.3, level 49 parameters for AMI Semiconductor's 0.5-μm process parameters.

The gate capacitor used in this pixel design has a voltage-dependent capacitance. The value of the gate capacitance is acquired from HSPICE simulation with NMOS and PMOS transistors whose width and length are 7.5 and 9.5 μm, respectively. The threshold voltages for PMOS and NMOS transistors are -0.94 and 0.77 V, respectively. If the voltage applied to the gate of a transistor is close to the threshold voltage of the device, the gate capacitance decreases and becomes very small under threshold voltage, as shown in Fig. 6. Due to this voltage-dependent capacitance, frame buffer pixels with a gate capacitor as a storage element require stored voltage larger than the threshold voltage of the M3, hence the voltage range of operation is narrowed.

[1][Online.] Available: http://www.mosis.org/

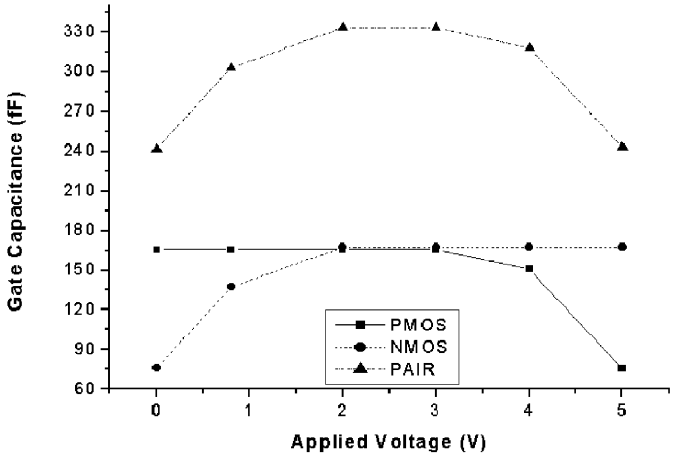

Fig. 6. Voltage-dependent gate capacitance of PMOS and NMOS. Width and length are 7.5 and 9.5 μm, respectively.

B. Pixels With a Separate Capacitor Storage Element

The voltage-dependent gate capacitance in the new frame buffer pixel can be easily replaced by a separate capacitor made from a double-poly CMOS technology, as shown in Fig. 5(b). A poly–poly capacitor in AMI Semiconductor's 0.5-μm CMOS process and paired PMOS and NMOS transistors are good examples of the separate capacitor design. Since the poly–poly capacitor has voltage-independent capacitance and the combined NMOS and PMOS transistors possess capacitance larger than 200 fF for all ranges of applied data voltage, the dynamic range is not reduced. The separate capacitor also minimizes parasitic capacitances. The minimized $C_{\rm S}$ of transistor M3 in Fig. 5(b) further lowers the offset voltage generated during data read time to 0.1 V, as shown in Fig. 4(g). The offset occurs consistently at all voltage levels. Thus resetting the lowest voltage level to a new zero level will maximize the contrast ratio. Similarly, the frame buffer pixel proposed by McKnight can be improved by employing a separate capacitor and minimum geometry transistor (for transistor M3), as shown in Fig. 3(b). The charge amount induced when the write signal turns ON results in only 0.18 V, as exhibited in Fig. 4(h). This value is 10 times less when compared with the value of about 1.88 V for the McKnight pixel, in Fig. 4(e). The modified pixel removes unnecessary parasitic electrical path and reduces the charge inducement during data write time significantly, yielding a much better image contrast ratio than previous frame pixel design.

IV. Experimental Results

A 63×32 LCOS SLM with three novel frame buffer pixel circuits discussed in Sections III-A and III-B was laid out using Mentor IC station tools and fabricated with the AMI Semiconductor's 0.5-μm double-poly triple-metal CMOS process through the MOSIS foundry. The left upper corner of a column driver, a row driver and the pixel array of the fabricated backplane are shown in Fig. 7. The pixel electrodes of interest are connected to analog pads through an rail-to-rail operational amplifier with negative feedback to buffer the voltage applied to the pixel electrodes for measurement [16]. The output voltage of the operational amplifier ranges from 0.05 to 4.94 V,

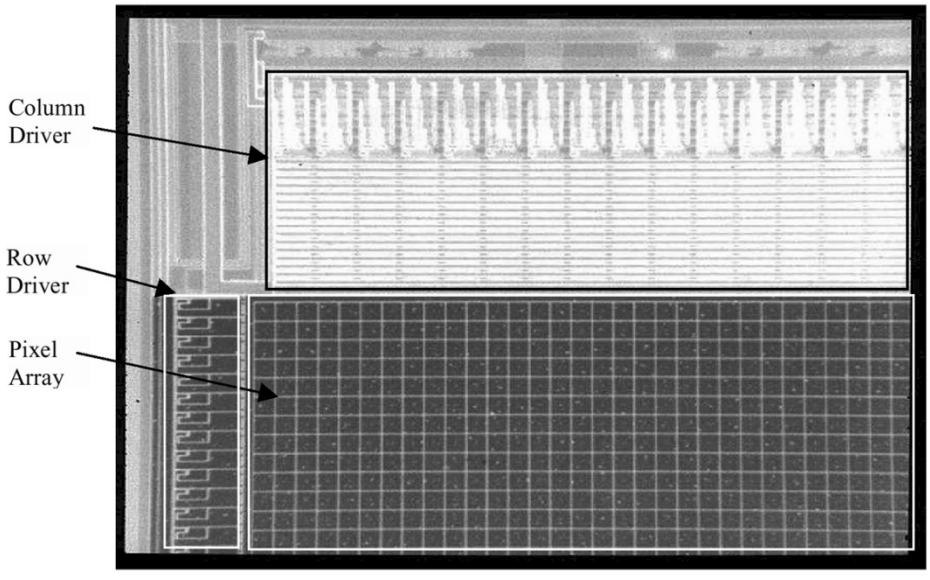

Fig. 7. Left upper corner of the fabricated 64 × 32 microdisplay with frame buffer pixels.

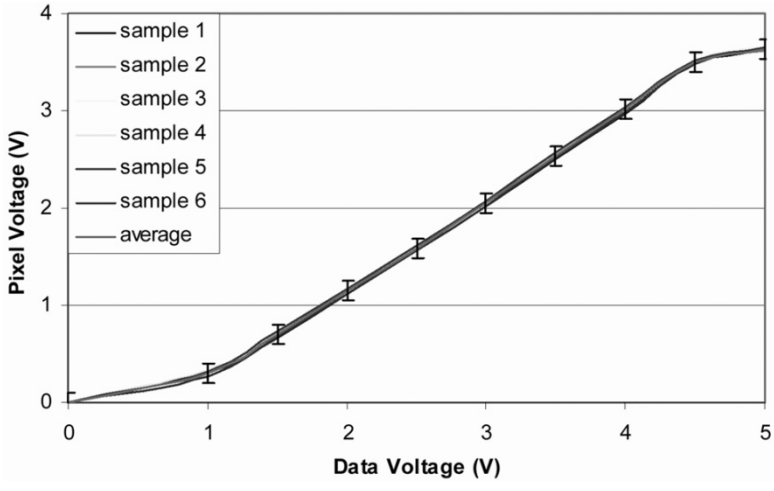

Fig. 8. Voltage on the pixel electrodes with respect to the data voltage.

buffering the input voltage linearly except near rail voltages where a tiny offset voltage of about 50 mV occurs. The slew rate of the amplifier, measured with only an oscilloscope probe whose capacitance is 14 pF, was 88 V/μs and 80 V/μs for rising and falling edges, respectively. The slew rate of the operational amplifier is fast enough to probe pixel voltages whose the rising and falling time of the pixel voltage is $\sim$96 V/μs with the load of 200 fF.

Video signals such as vertical synchronization, horizontal synchronization, video data, and master clock are generated from an Altera field programmable gate array (FPGA) board[2] and fed to the backplane to characterize the frame buffer pixels. The voltage stored at the pixel electrodes according to the data voltage with the application of the read signal is measured and converted to the unbuffered voltage using the output curve of the operational amplifier. The voltage range on the pixel electrodes is 0$\sim$3.64 V, when $V_{\rm dd}$ is 5 V, as shown in Fig. 8. The output voltage saturates after the data voltage reaches 4.5 V. The voltage range depends on the pulsewidth of signals used to control the frame buffer pixels. The measurement was performed with signals whose pulsewidth is 2.56 μs. The longer pulsewidth generates the wider output voltage range. The measurement was made with six different samples and data was averaged and plotted. Fig. 8 includes 0.1-V error bars centered on the average value from all measured data with different samples are consistently reproducible. The voltage swings from 0 to 4.25 V when $V_{\rm dd}$ changes to 6 V. The maximum voltage on the pixel electrode is limited by the threshold voltage of the NMOS transistors used in the frame buffer pixels. The threshold voltage of the transistors is strongly dependent on the ratio of the width and length of the transistors. It can be further optimized to have wider voltage range since the typical threshold voltage of the CMOS process is 0.79 V for NMOS.

Fig. 9 shows measured voltage levels of input signals such as write, read, and data, and four frame buffer pixels. Upper three traces (A, B, C) represent read, write, and data. Four frame buffer pixels include new pixel with a gate capacitor (new_1), modified new pixel with a separate capacitor (new_2),

[2][Online.] Available: http://www.altera.com/education/univ/unv-kits.html

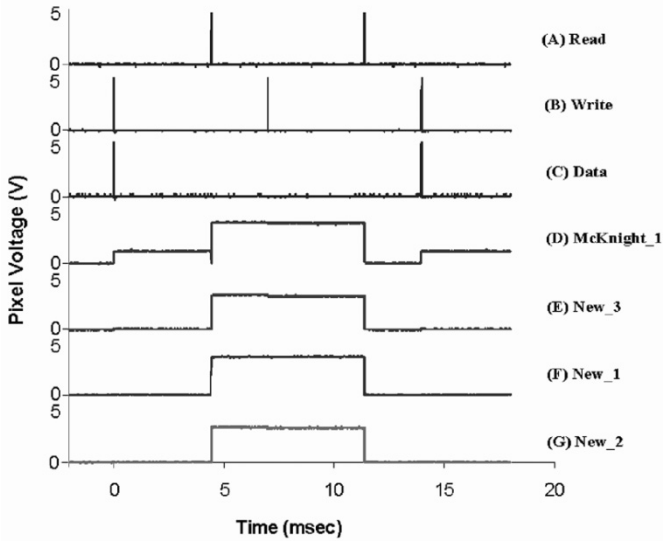

Fig. 9. Measured voltage levels of input signals and four frame buffer pixel capacitors.

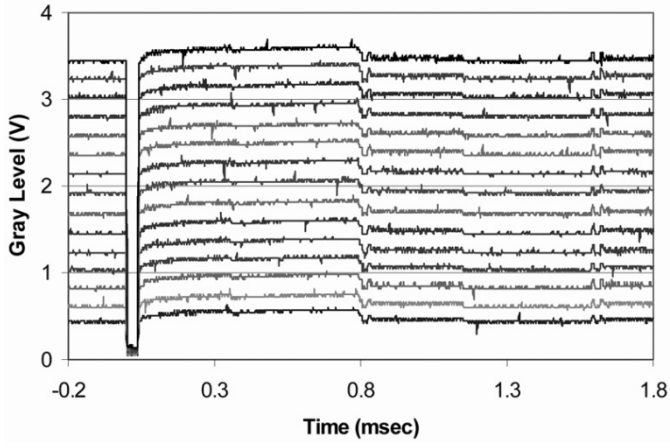

Fig. 10. Fifteen levels of voltage at the pixel electrode formed according to data voltage.

McKnight pixel with a gate capacitor (McKnight_1), and modified McKnight pixel with a separate capacitor (New_3). Voltages on those pixel electrodes are displayed in lower traces (D, E, F, G). Five volts for odd frames and 0 V for even frames are provided for the data for a pixel of interest. Data written to the memory capacitor with write signal in a frame is transferred to the pixel capacitor with read signal in the next frame. An even frame starts at 4.4 ms and an odd frame at 11.4 ms.

Confirming the simulation results, the McKnight pixel exhibits charge induced at $C_{\rm pixel}$ when the data signal is written, as shown in Fig. 9(d). A voltage of 1.085 is induced on the pixel electrode when write signal is turned ON. The induced charge increases the brightness of the odd frames, which are supposed to display zero data. The induced voltage is minimized to 0.085 V by replacing the gate capacitor with a separate capacitor as displayed in Fig. 9(e). Fig. 9(f) and (g) verifies that the new frame buffer pixel does not have charge sharing between the memory and the pixel capacitors and charge inducement during data write time. The voltage level of odd frames remains nearly zero with no fluctuation. New_1 has an offset voltage of 0.02 V for the odd frames due to $C_{\rm D}$ of transistor M3 in Fig. 5(a). Again, this offset is further reduced to almost zero by replacing the gate capacitor with a separate capacitor. For the three frame buffer pixels (New_1, New_2, and New_3), it is obvious that the contrast ratio, which critically relies on the dark level more than the bright level, can be increased significantly without loss of image brightness as compared to all previous frame buffer pixel circuits, to our knowledge. These frame buffer pixels used for an XGA FSC display improve brightness by 36% with maximum contrast ratio when it operates at the frame frequency of 360 Hz. The increase of brightness is attributed to the utilization of data writing time in image frames, which will be wasted otherwise.

There is charge induced at the pixel electrode in all pixel circuits when the read signal is turned ON, as shown in Fig. 10, which displays 15 levels of output voltage at a pixel electrode. This induced charge occurs due to the parasitic $C_{\rm GS}$ of transistor M4 in Fig. 5(b) controlled by the read signal. Since the ratio of the $C_{\rm GS}$ to the capacitance of the pixel capacitor is so small, the induced charge is approximately 0.06 V. Moreover, the induced charge is same for all levels of pixel voltage regardless of the data voltage and it disappears when the read signal turns back to zero after data read is done. The voltage retention time ($>$95%) is larger than 1 s. The voltage on the pixel electrode remained with no charge decay over one frame time of 5.5 ms for our application. The long retention time results from the subthreshold leakage current of 2 fA.

V. Conclusion

Three new frame buffer pixel circuits were designed, fabricated, and thoroughly tested using the AMI Semiconductor's 0.5-μm double-poly triple-level metals CMOS process. Output voltages at the pixel electrodes were measured through rail-to-rail operational amplifiers with negative feedback. Converted output voltage ranges from 0 to 3.65 V for a 5-V power source. The new frame buffer pixels (New_1 and New_2) do not show charge sharing and do not induce charge at the pixel electrode during data write time. This is confirmed by all voltage levels remaining constant during one frame time of 5.5 ms. The offset voltage generated during data read time is minimal and consistent over one frame time. Since this offset occurs evenly in all voltage levels, the contrast ratio is not affected. The measured voltage retention time (95%) is approximately 1 s and the corresponding leakage current is 2 fA. There is absolutely no charge decay over one frame time of 5.5 ms.

The three new pixel circuits take full advantage of the frame-at-a-time driving method due to no charge sharing and charge inducement at the pixel electrode. These advantages are maximum image contrast ratio and brightness, and reduced speed requirement on driver electronics. The memory and pixel capacitors for the new three pixels can be optimized independently to have proper voltage retention time with minimum space. This allows for a low-cost and high-resolution display such as high-definition television. The frame buffer pixels play very valuable roles in the FSC projector whose image brightness is lower than the three-panel projector due to the intrinsic loss of two-thirds of the source brightness. Their roles will be more significant as the resolution of the displays becomes dense, such that the data write time becomes comparable to one frame time of the displays.

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