Dallas Chapter, IEEE Circuits and Systems

Digital Radio Processor (DRP) Alternative to Conventional RF

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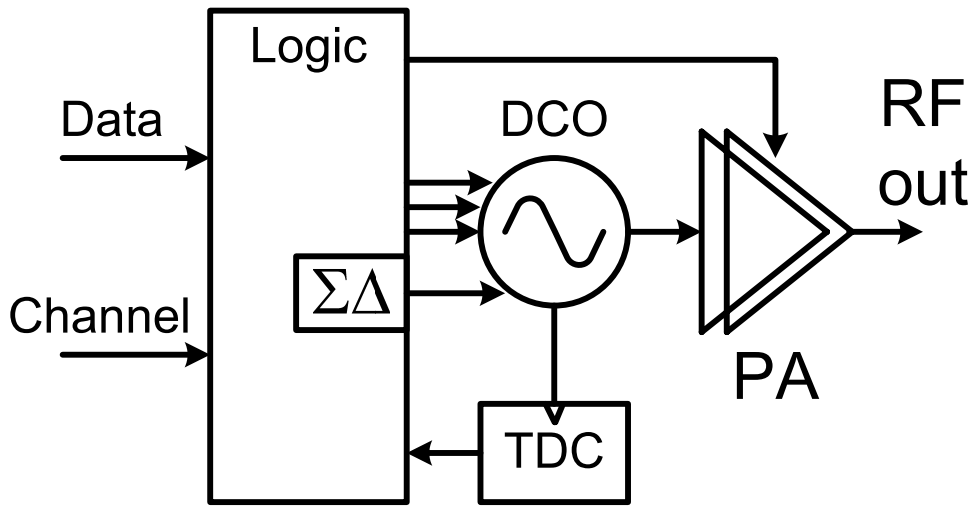
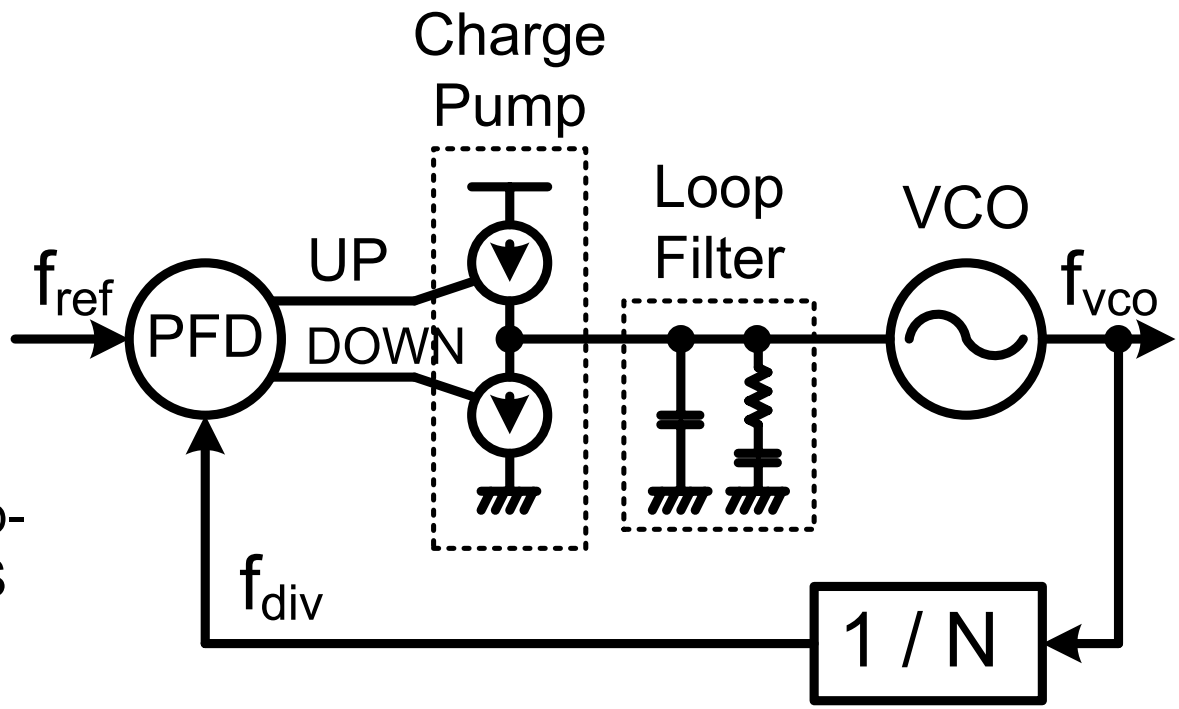
Outline

- Motivation
- Digitally-Controlled Oscillator (DCO)
- Sigma-Delta dithering of DCO varactors
- Time-to-digital converter
- Digital loop filter
- All-Digital PLL (ADPLL) architecture
- Transmitter
- Development timeline
- Testchips and results
- Conclusion



Motivation

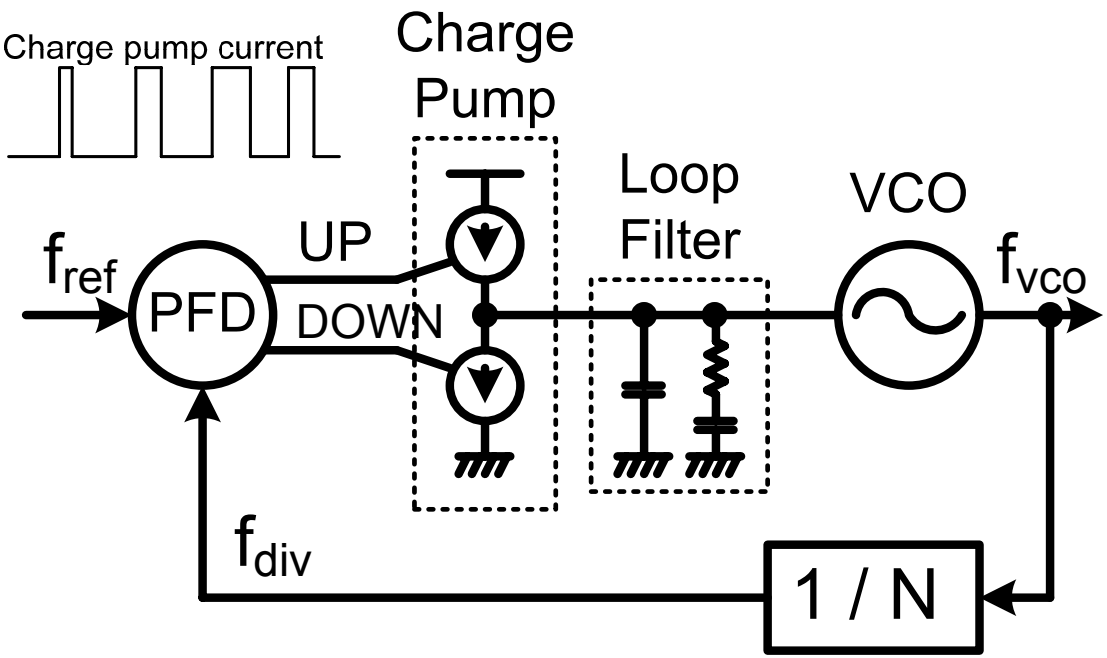
- Frequency synthesizers in commercial wireless applications traditionally use charge-pump PLL's
  - Used as a LO for frequency translation in TX and RX
- Design flow and circuit techniques are analog intensive
- Technology incompatible with modern digital baseband and application processor
  - Low-voltage deep-submicron CMOS



Charge-pump PLL

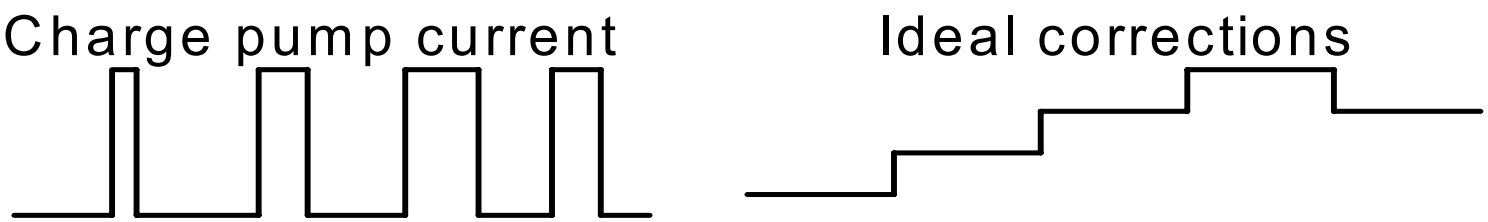
- Found in all commercial RF synthesizers for mobile applications
- Frequency difference estimated by means of the phase difference, hence fundamentally slow acquisition
- Phase difference estimated in PFD by measuring time difference between f_{ref} and f_{div} closest edges
- PFD produces current pulse with proportional duty cycle

- Loop filter converts the current into a VCO tuning voltage
- The integrating capacitor and introduces a pole at dc



Motivation (Cont.)

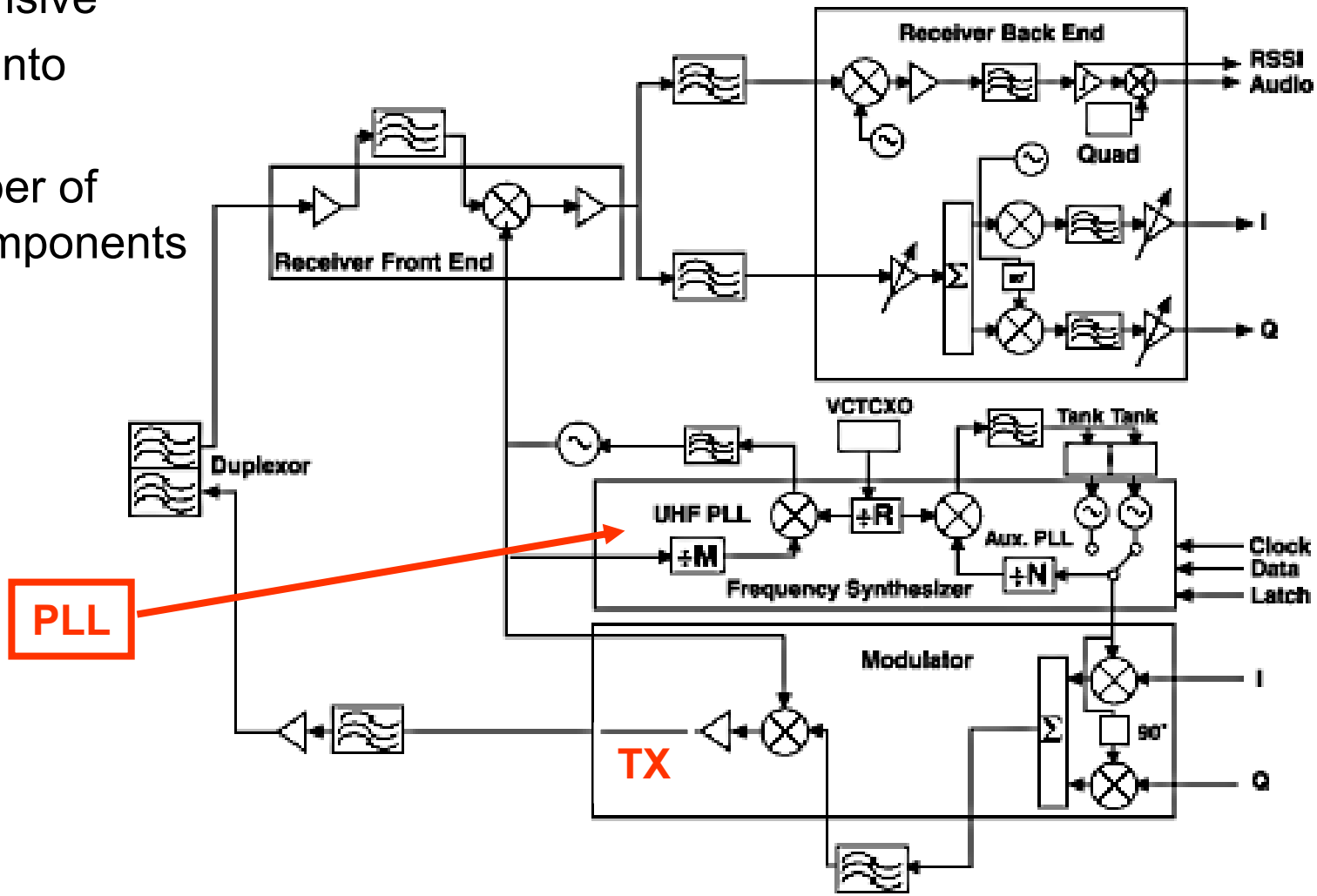
- Charge-pump PLL does not truly operate in the phase domain: only approximation under lock
  - [F. Gardner, 1980] describes: “converting the timed logic levels into analog quantities”
  - Generates reference spurs that require filter



- Aggressive cost and power reductions of mass-produced mobile wireless terminals require the highest level (i.e., single chip) of integration
  - Digitally-intensive approach to conventional RF and analog functions

Commercial GSM RX/TX Architecture

- Analog intensive
- Partitioned into several IC's
- Large number of external components



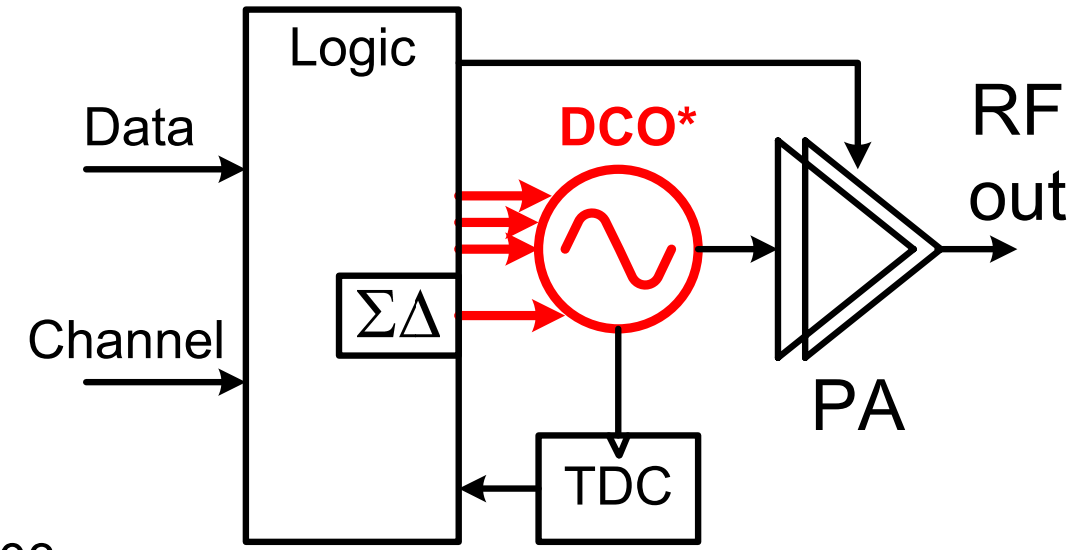
Digitally-Controlled Oscillator (DCO)

ΣΔ Dithering of DCO

Time-to-Digital Converter (TDC)

Digital Loop Filter (LF)

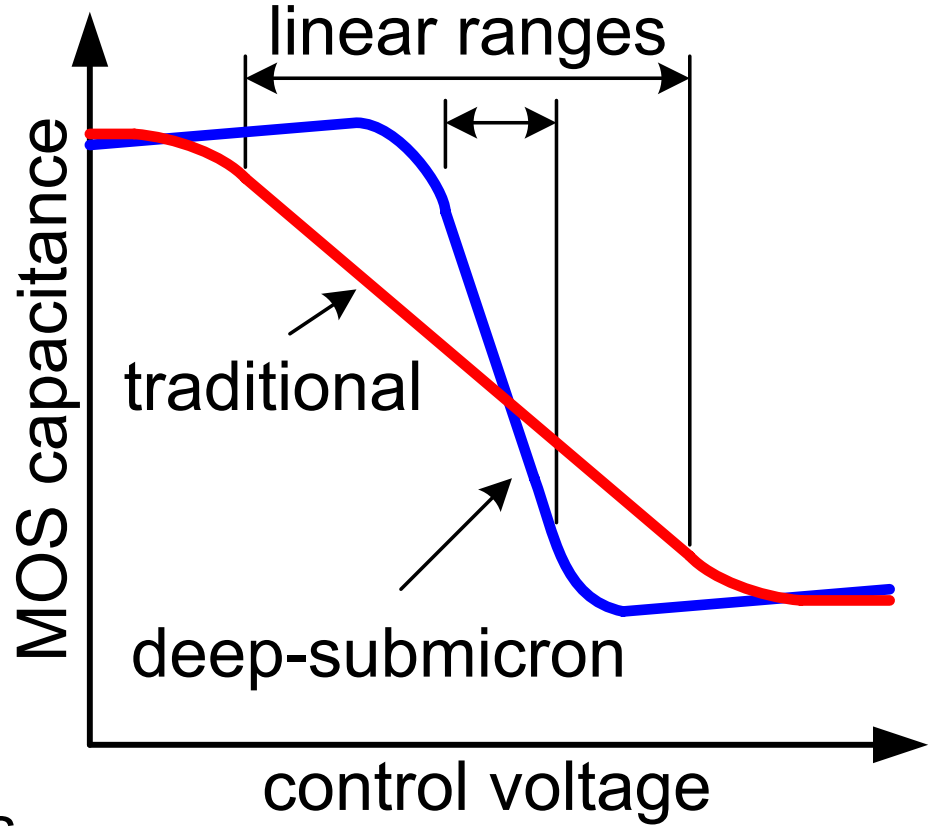
All-Digital PLL (ADPLL)



*RFIC'03 and T-MTT'03

MOS Varactor

- Only simplest varactors in the digital CMOS
- Perceived poor quality of varactors in a deep-submicron CMOS for conventional VCO's



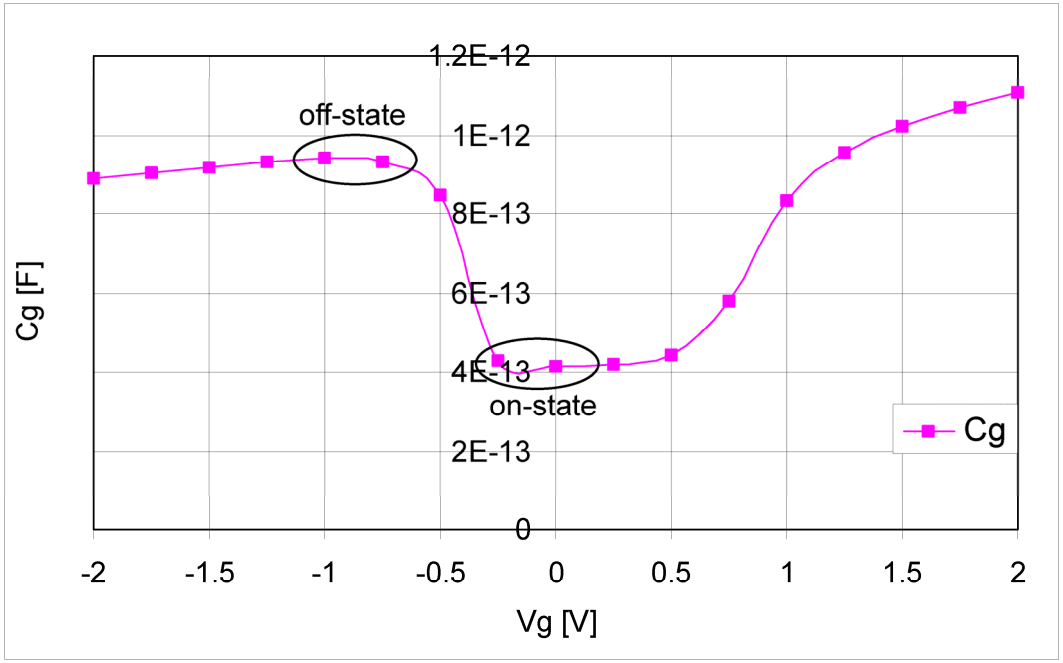
- Conventional CMOS varactors
  - Large linear range for precise and wide frequency control
- Deep-submicron CMOS varactor
  - Linear range is compressed with high noise sensitivity

New Paradigm

In a deep-submicron CMOS process, time-domain resolution of a digital signal edge transition is superior to voltage resolution of an analog signal

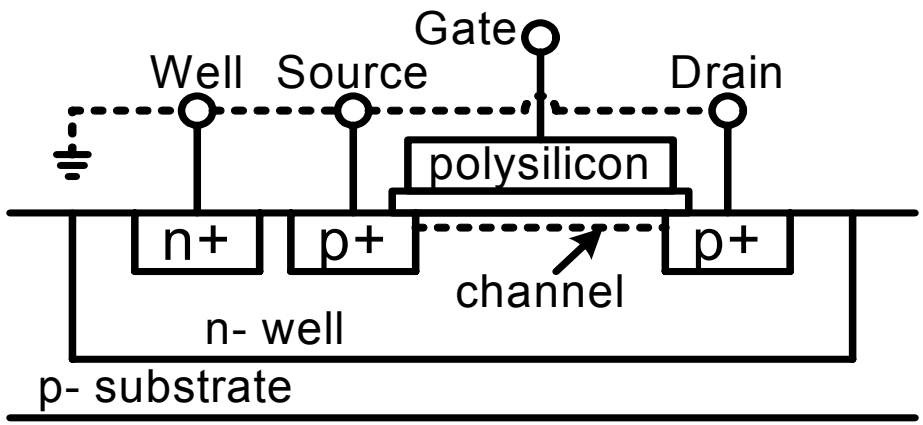
Varactor in Deep-Submicron CMOS

- Actual extracted and de-embedded C-V curve
- Two distinct and flat operational regions



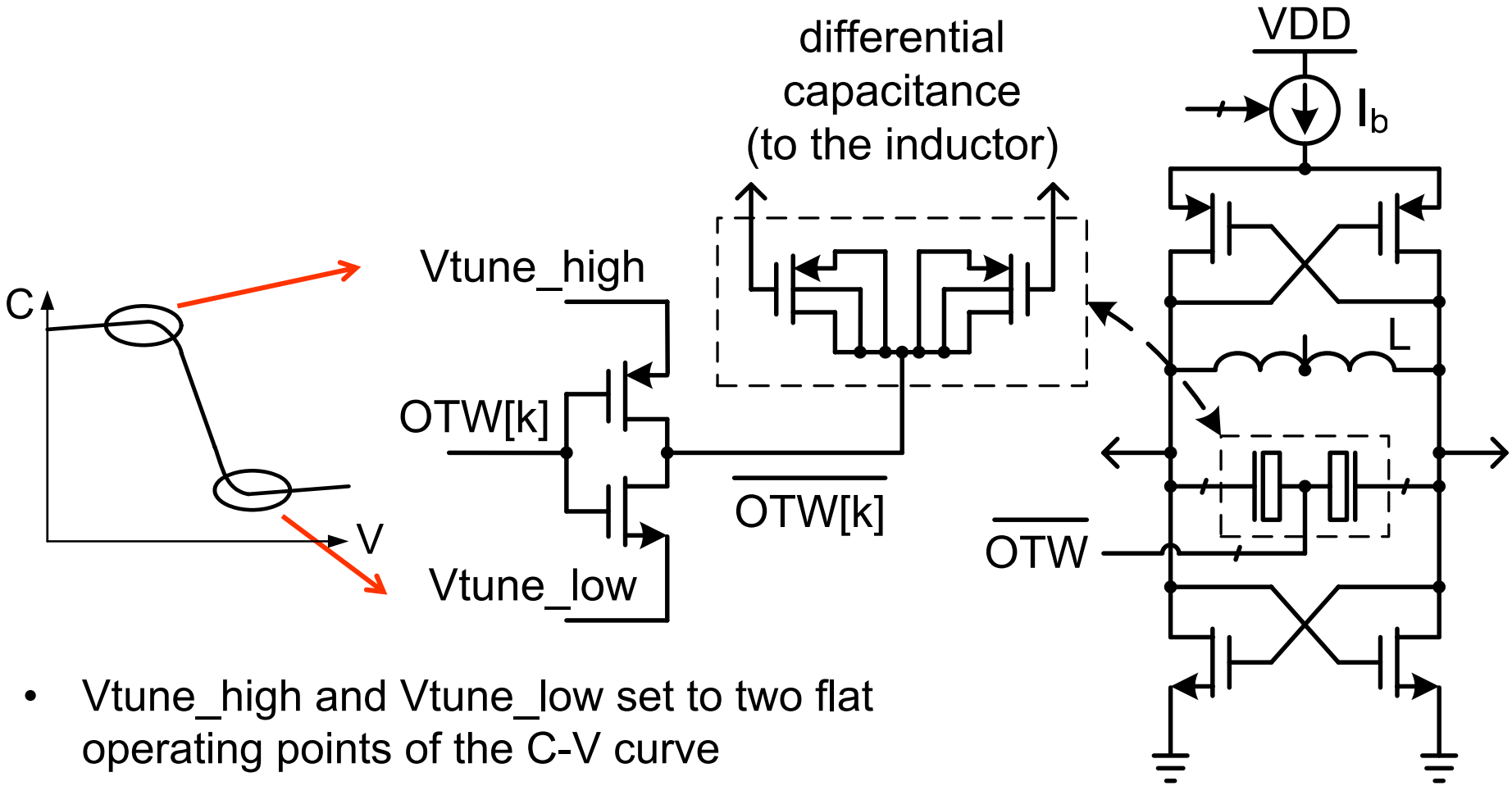
Ppoly/Nwell inversion-type varactor

- Extremely fine switchable capacitance
  - 40 attoFarad



Digitally-Controlled Oscillator (DCO)

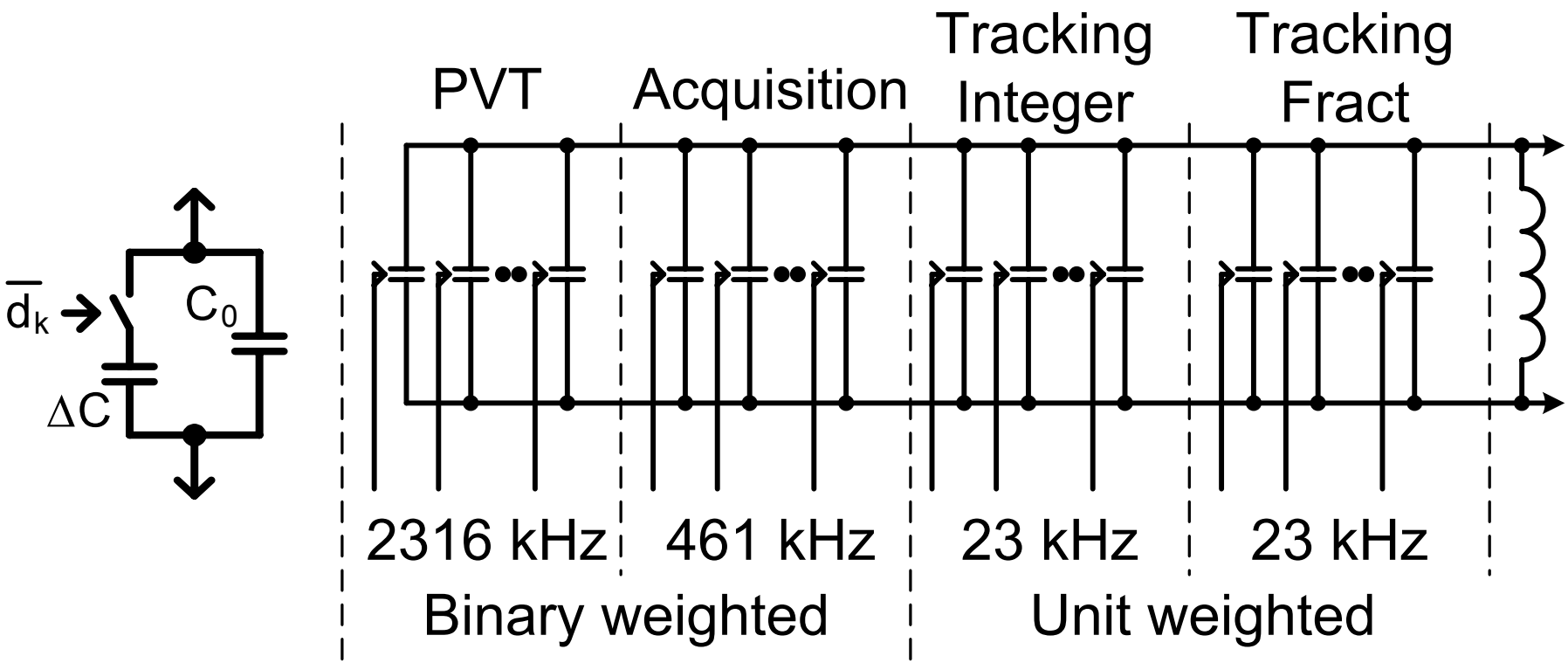
- First DCO for wireless: no analog tuning controls



- Vtune_high and Vtune_low set to two flat operating points of the C-V curve

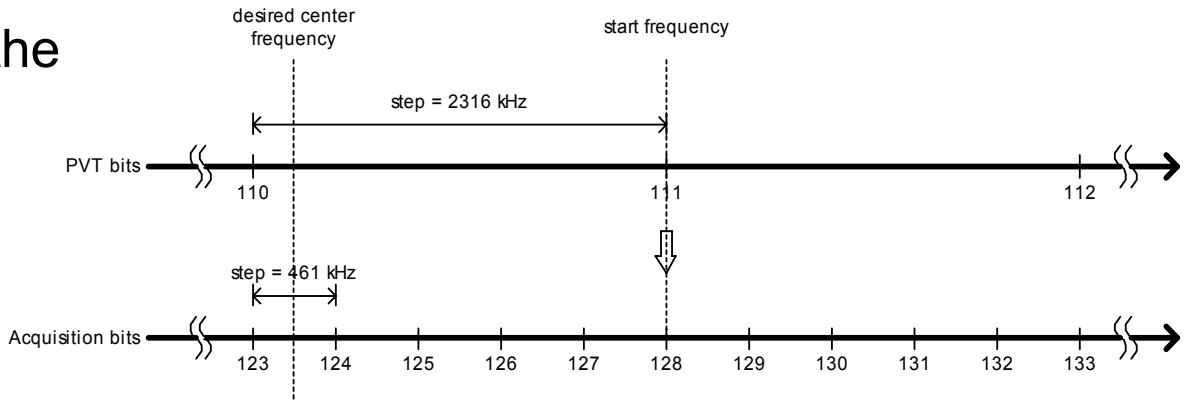
DCO Varactor Functional Banks

- Process/voltage/temperature (PVT) calibration mode
- Acquisition mode (during channel select)
- Tracking mode (during the actual TX and RX)

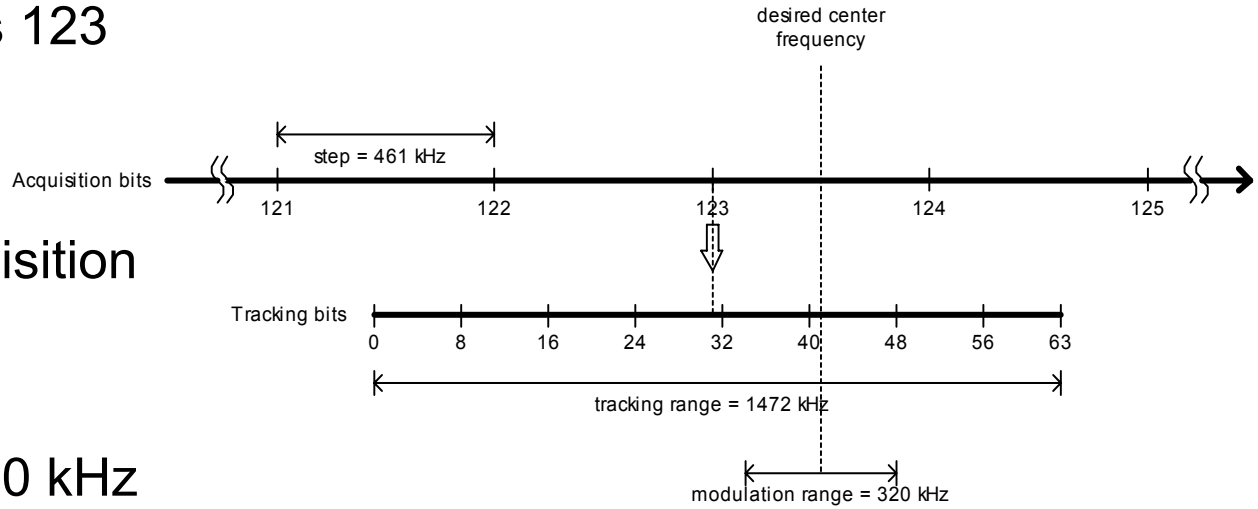


DCO Modes Transversal Example

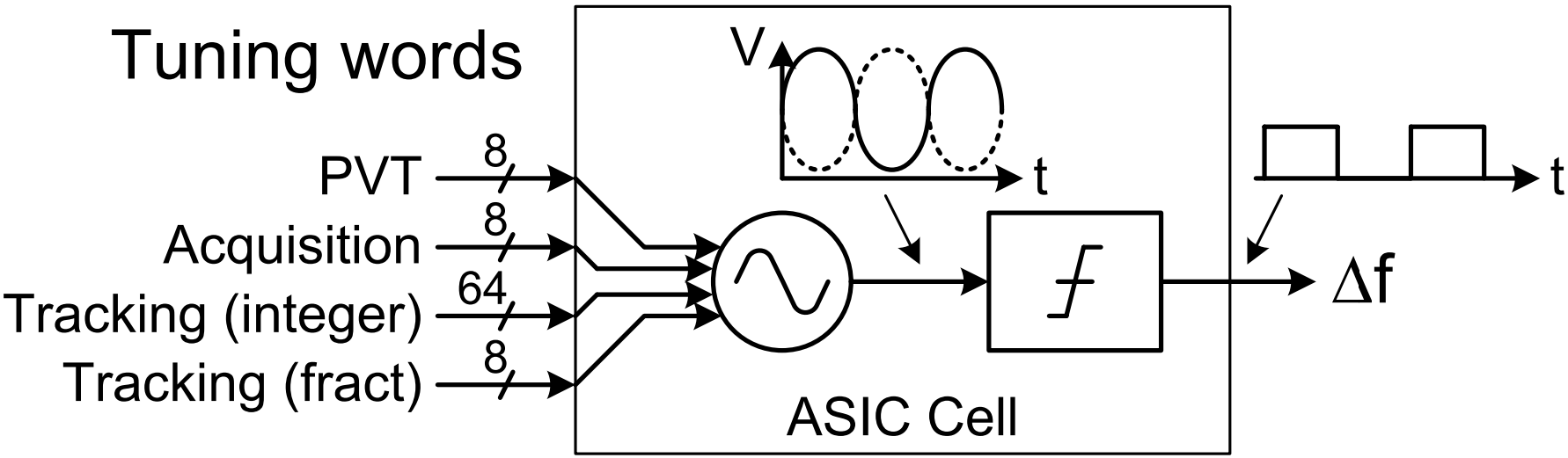
- PVT mode calibrated to the middle of the Bluetooth band (code 111)
- Acquisition starts at 128
- Desired channel 2 MHz lower quickly reached
- Dither between codes 123 and 124



- Switchover from acquisition to tracking at 123
- Tracking starts at 31
- Desired channel is 230 kHz higher (10 tracking steps)



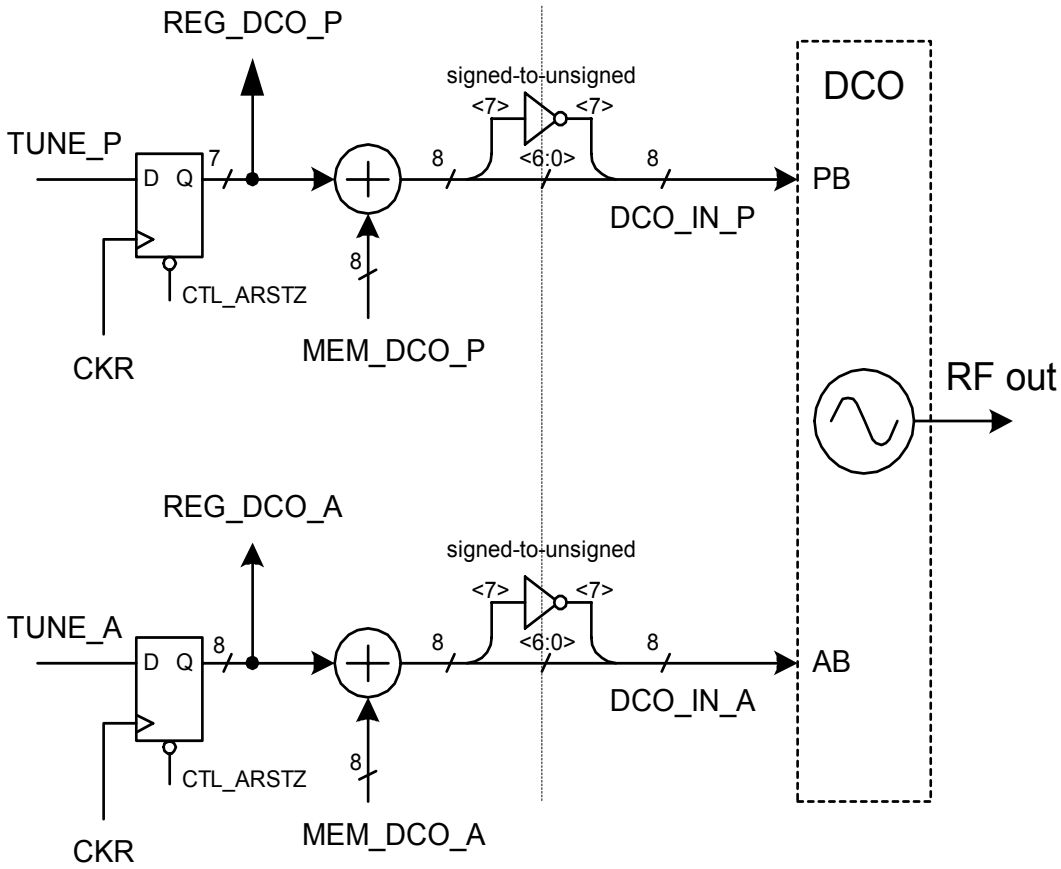
DCO ASIC Cell



- Truly digital I/O's even at 2.4 GHz output – t_r<50 ps
- DCO built as a digital ASIC cell despite analog underlying internals
- DCO analog nature does not propagate
- Circuitry around it can be digital

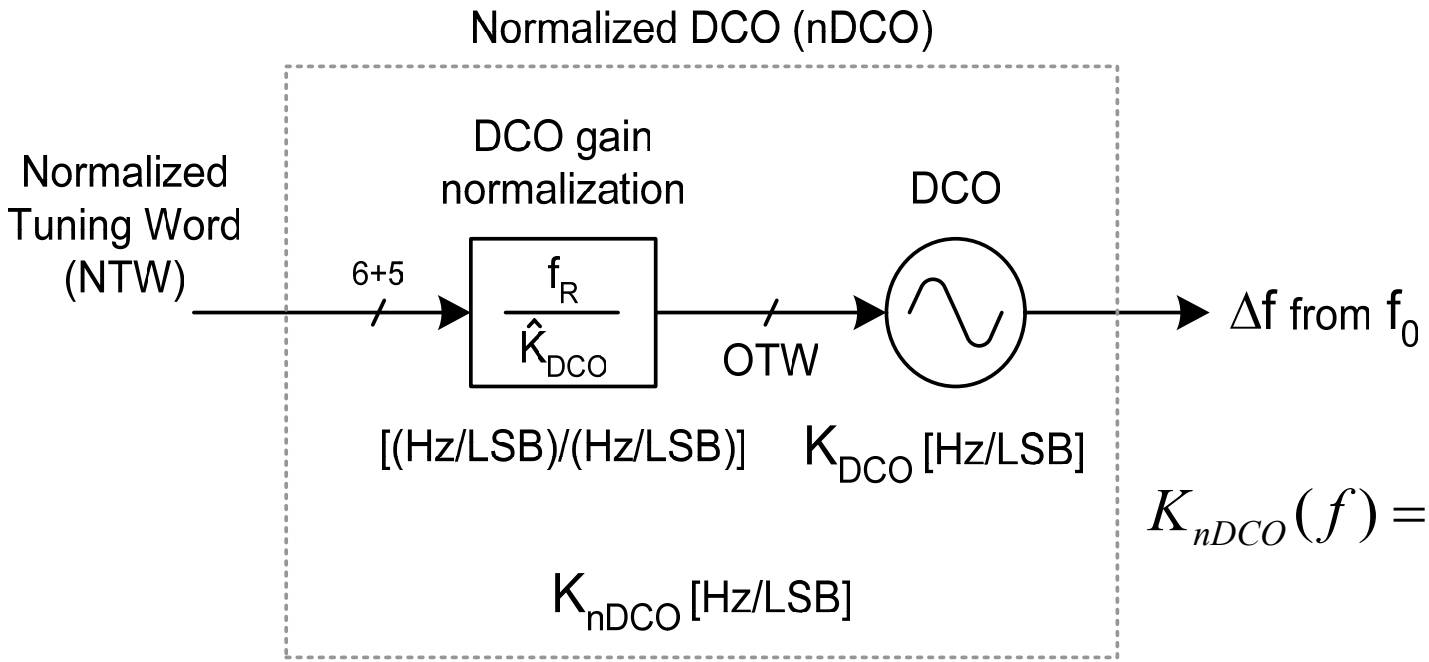
Oscillator Interface

- MEM_DCO_P could be the last frequency estimate from the controller's lookup table
- REG_DCO_P is the frequency offset reported back to the controller



- Identical circuit for both PVT and acquisition modes

Normalized DCO (nDCO)

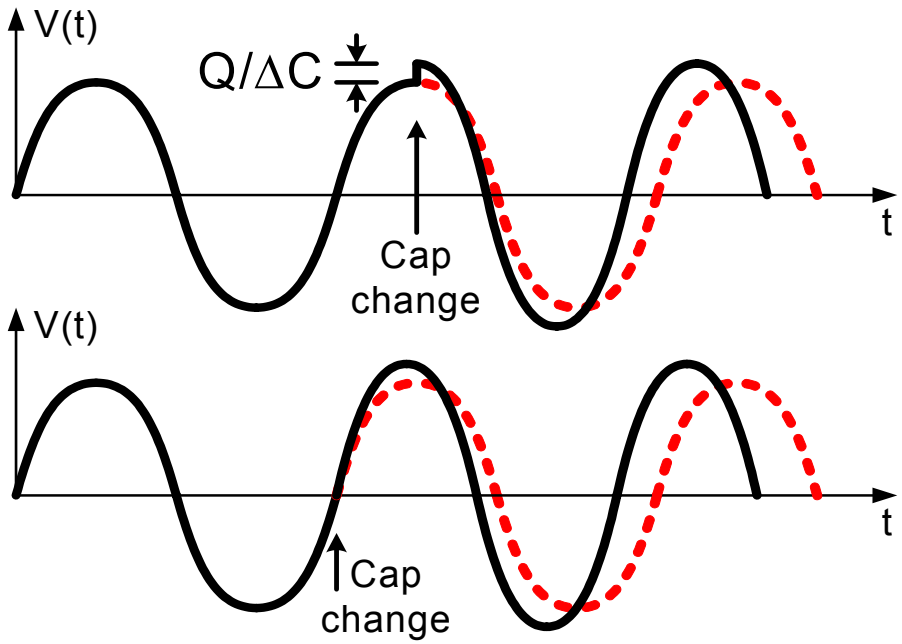


$$K_{nDCO}(f) = f_R \frac{K_{DCO}}{\hat{K}_{DCO}} = f_R \cdot r$$

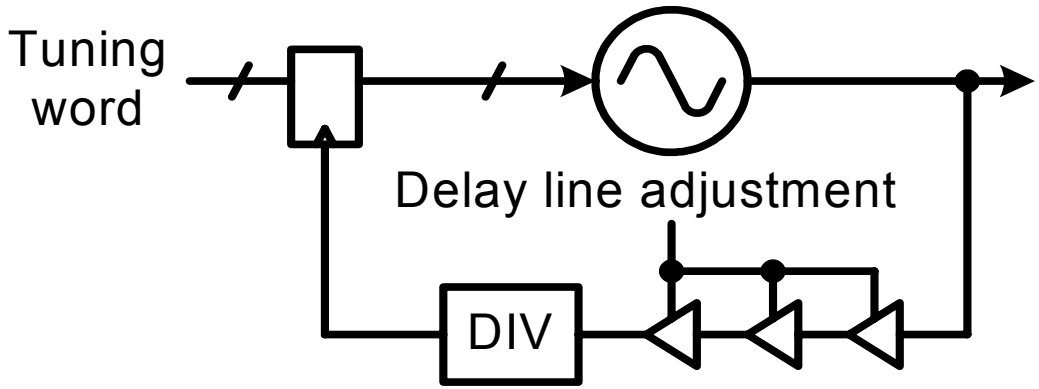
- K_{DCO} is dependent upon PVT
- K_{DCO} is tracked and normalized
- Decouples the phase and frequency info from process, voltage and temperature

Synchronously-Optimal Sampling

- DCO is a time-variant system
- Digital input controls the oscillating frequency by modifying the total capacitance



- Oscillator input word changes only at precise DCO state where it causes least amount of perturbations



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ΣΔ Dithering of DCO

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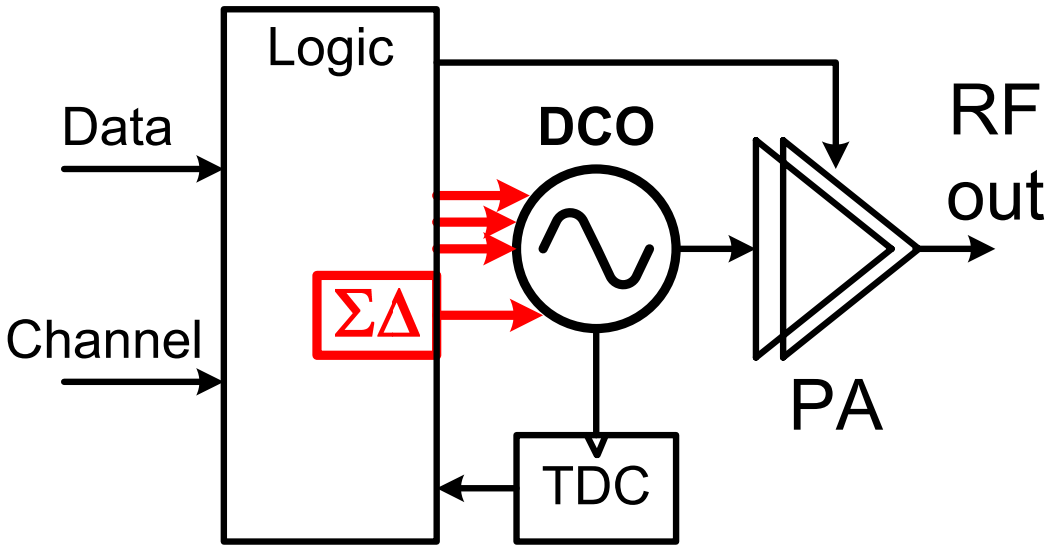
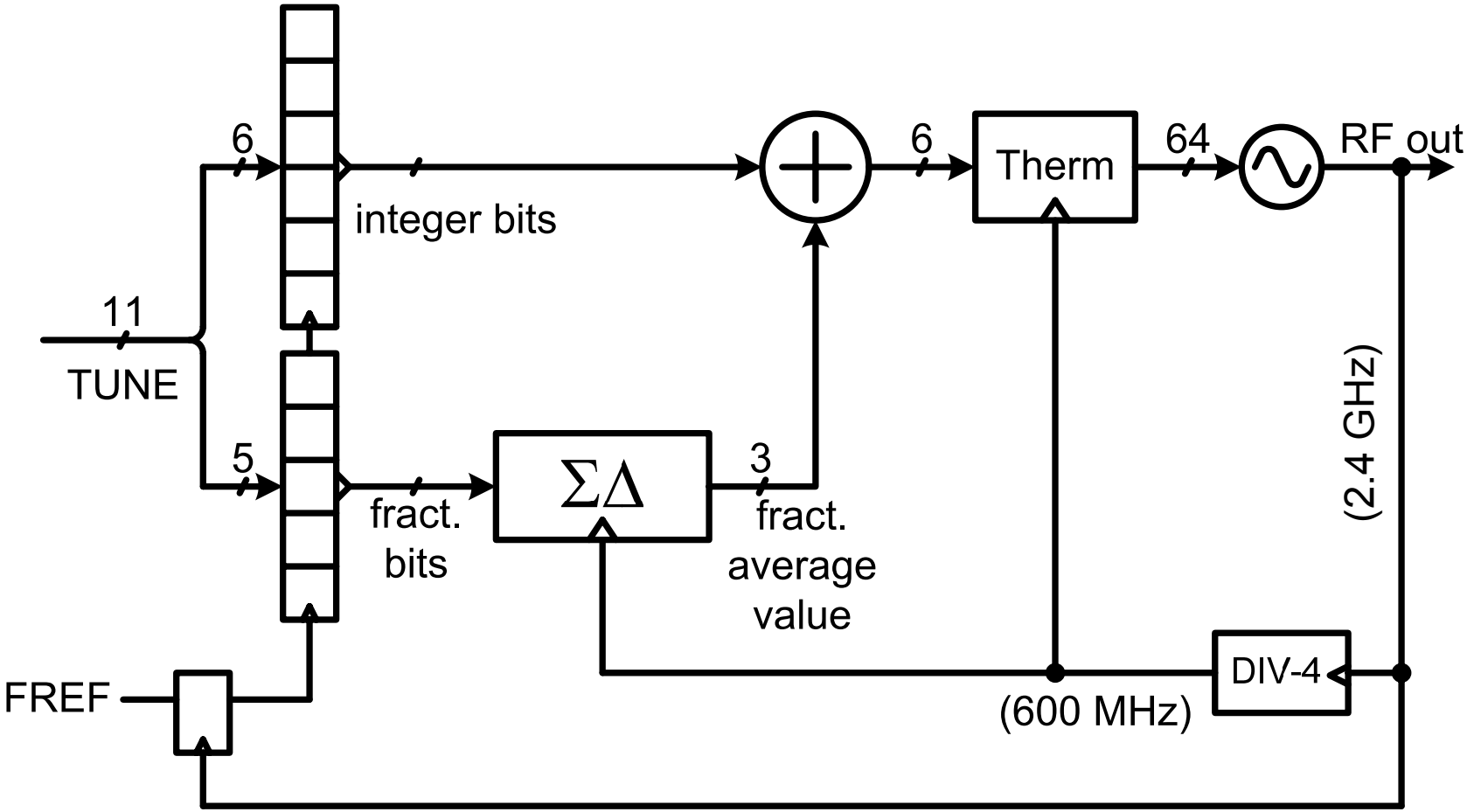
Digital Loop Filter (LF)

All-Digital PLL (ADPLL)



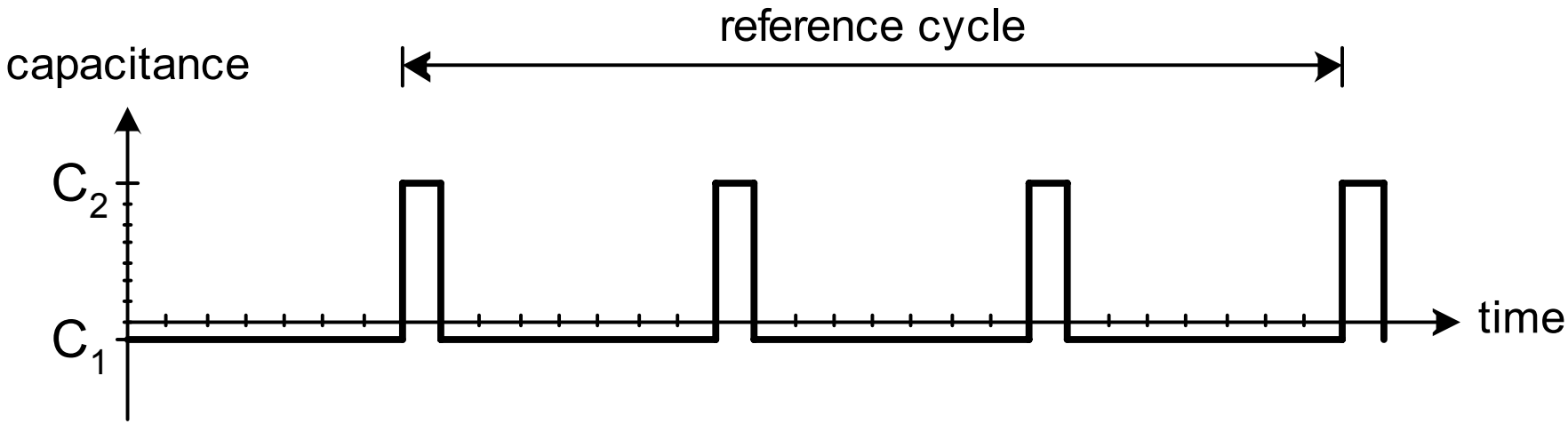
Sigma-Delta DCO Dither

- Improves time-averaged DCO frequency resolution over the basic 23 kHz/LSB to 23 kHz/32



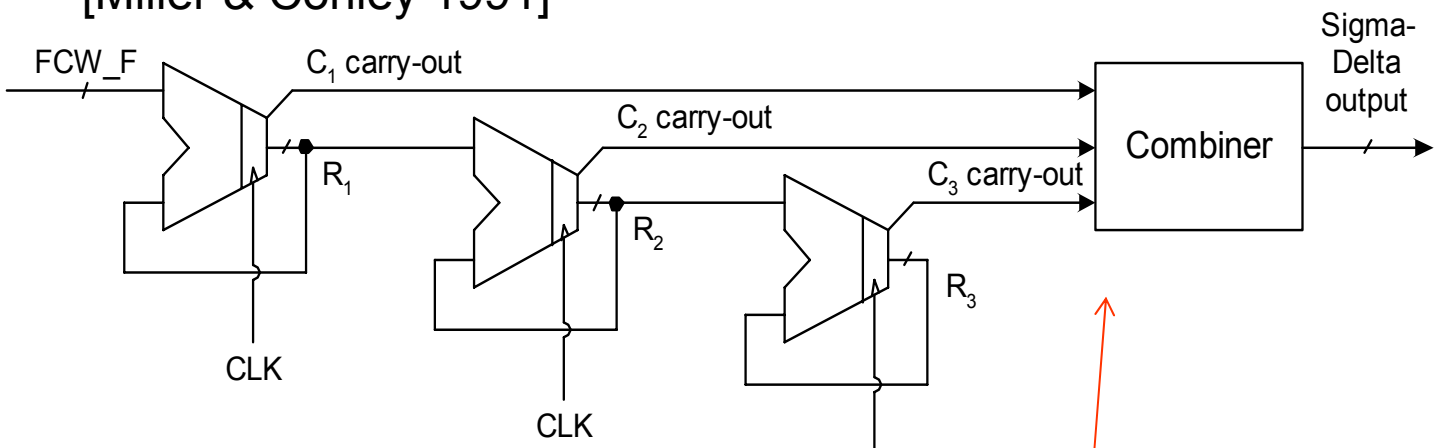
Varactor Dithering

- Frequency resolution enhanced by high-speed dithering of an LSB capacitors
- Produces spurious tone at the oscillator output with power inversely proportional to the dithering speed
  - Spur power = -20 log(β/2) [dBc], where β is a dimensionless ratio of the peak frequency deviation to the modulating frequency

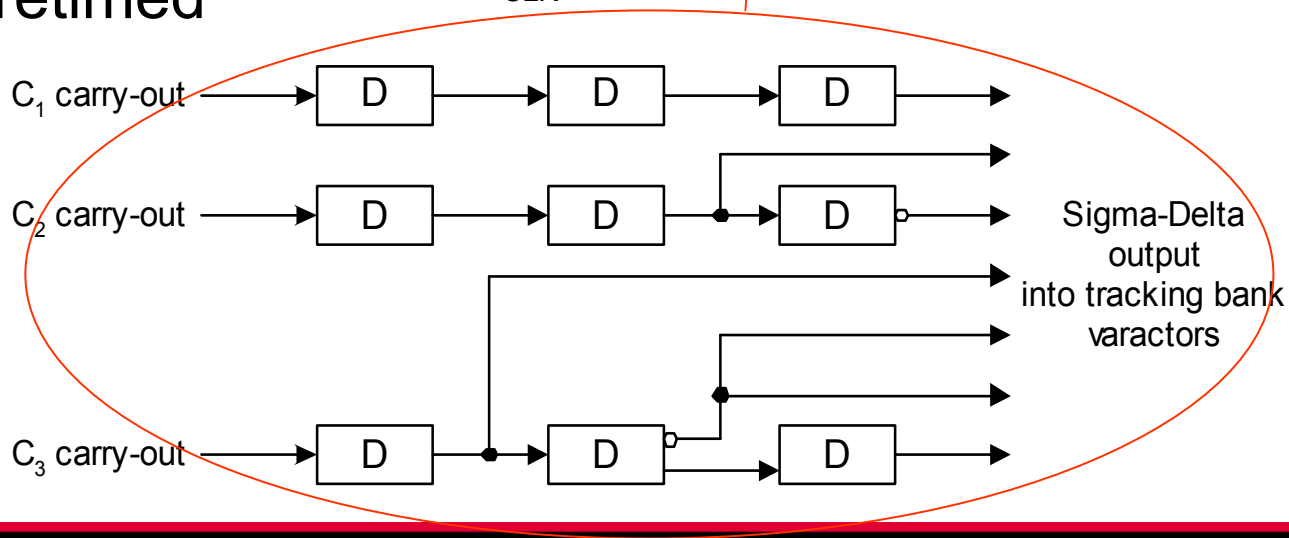


Sigma-Delta Modulator

- 3rd order MASH structure
  - [Miller & Conley 1991]

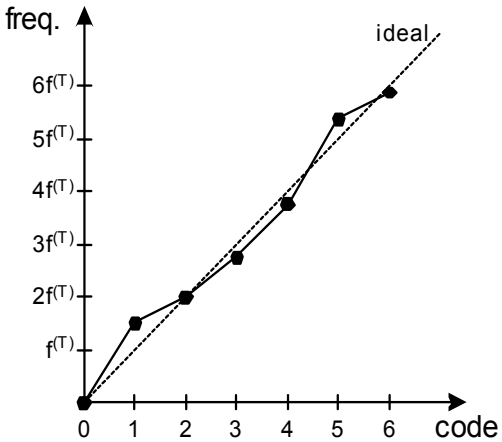


- Critical path retimed

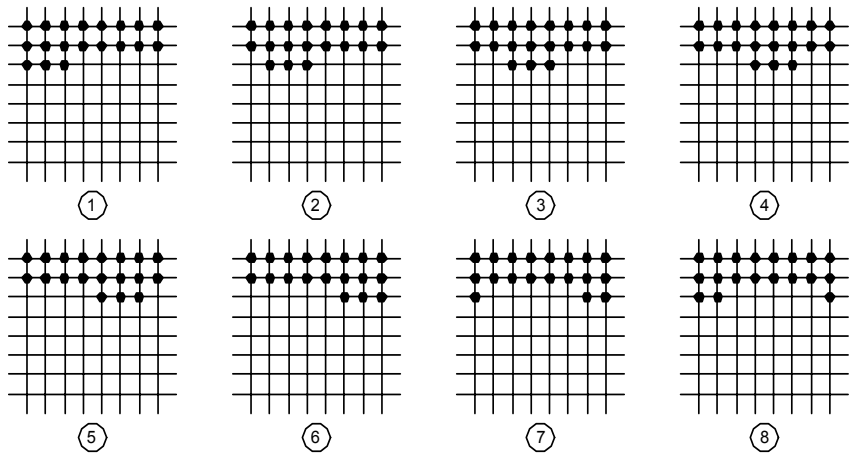


Dynamic Element Matching

- Unit-weighted capacitors of the tracking bank have slightly different capacitative values
- As capacitors are turned on and off, non-linearities will be evident in the output
- Dynamic element matching (DEM) to improve digital-to-frequency conversion linearity
  - Cyclic shift of unit-weight varactors

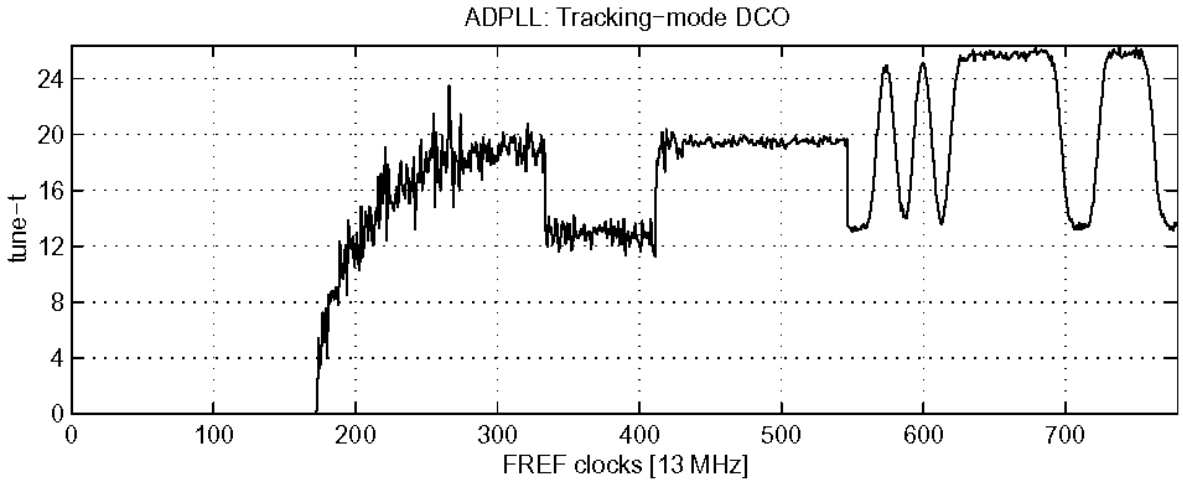


Example: cyclic shift of three “next-row” varactors

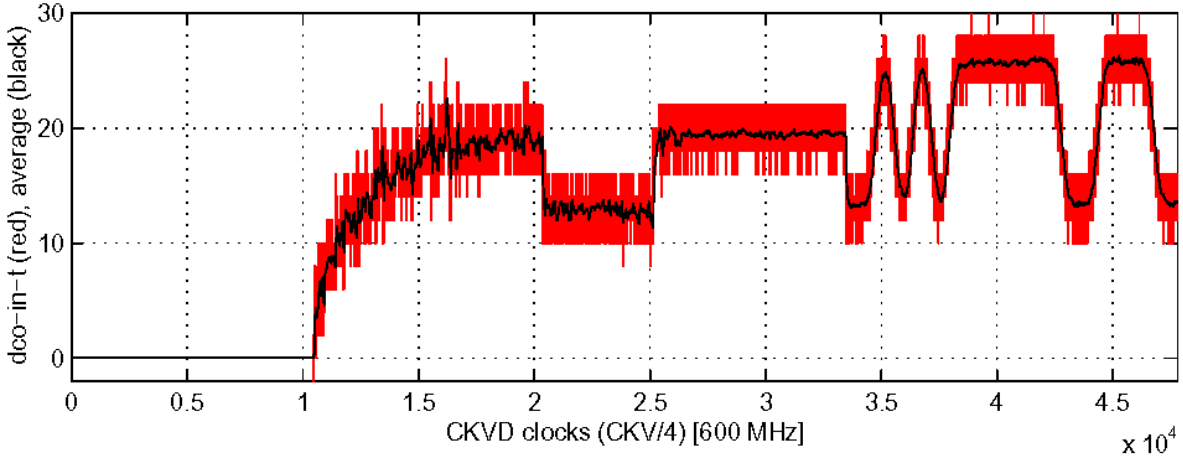


Second Order MESH ΣΔ Modulator

- Fixed-point (with 5 sub-LSB bits) DCO tuning word operating at 13 MHz FREF



- Integer DCO input word operating at 600 MHz CKVD
  - Black line is the running average



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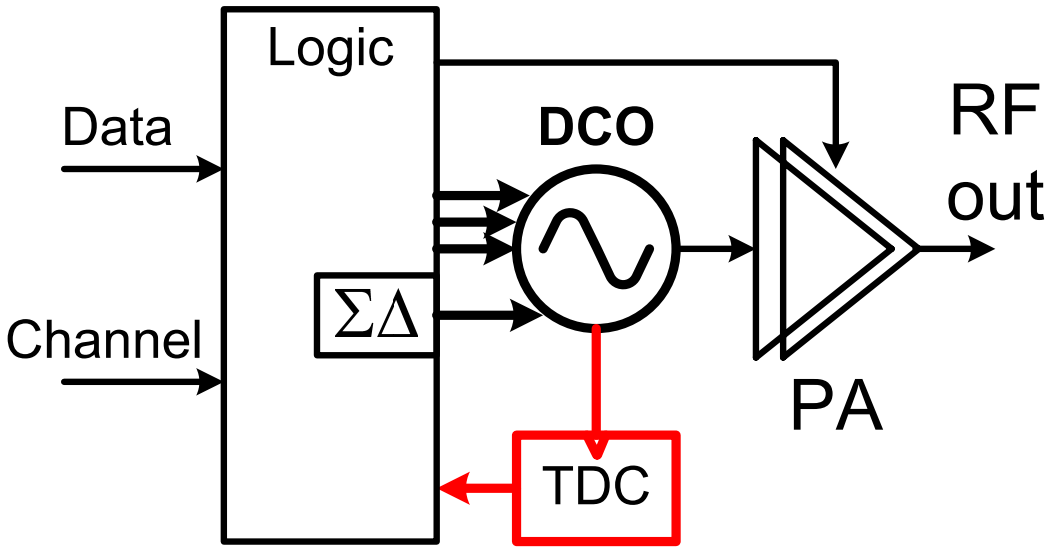
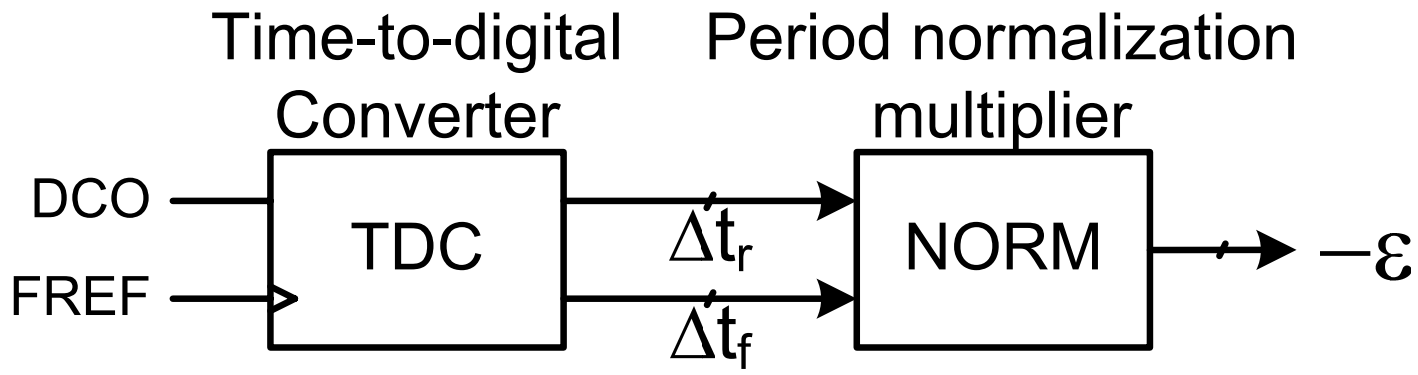
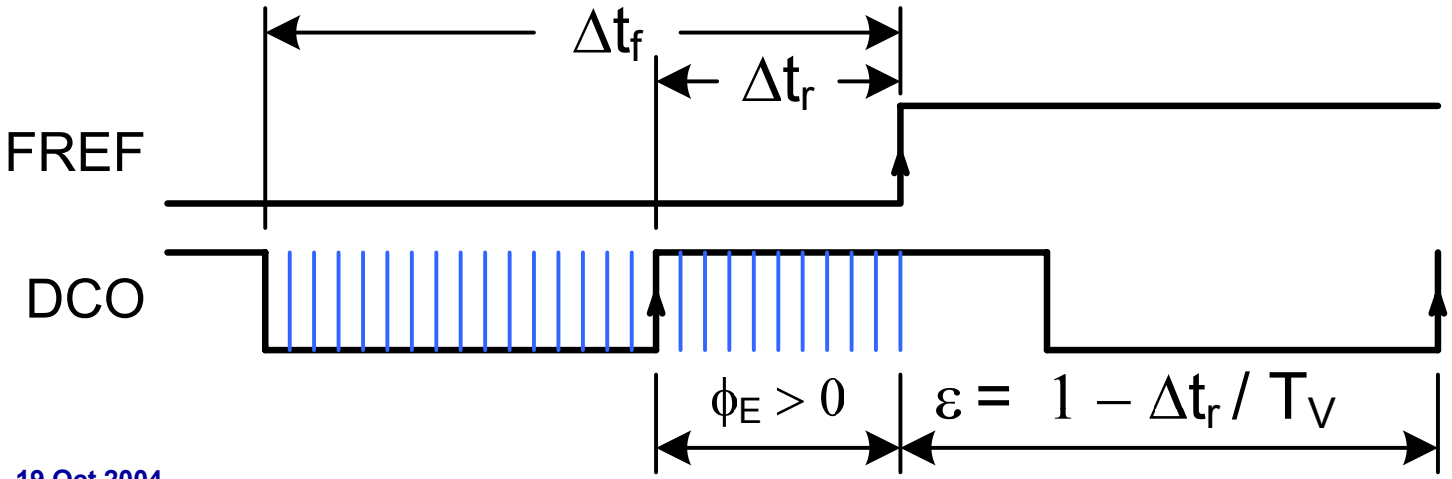


Fractional Phase Error Estimation

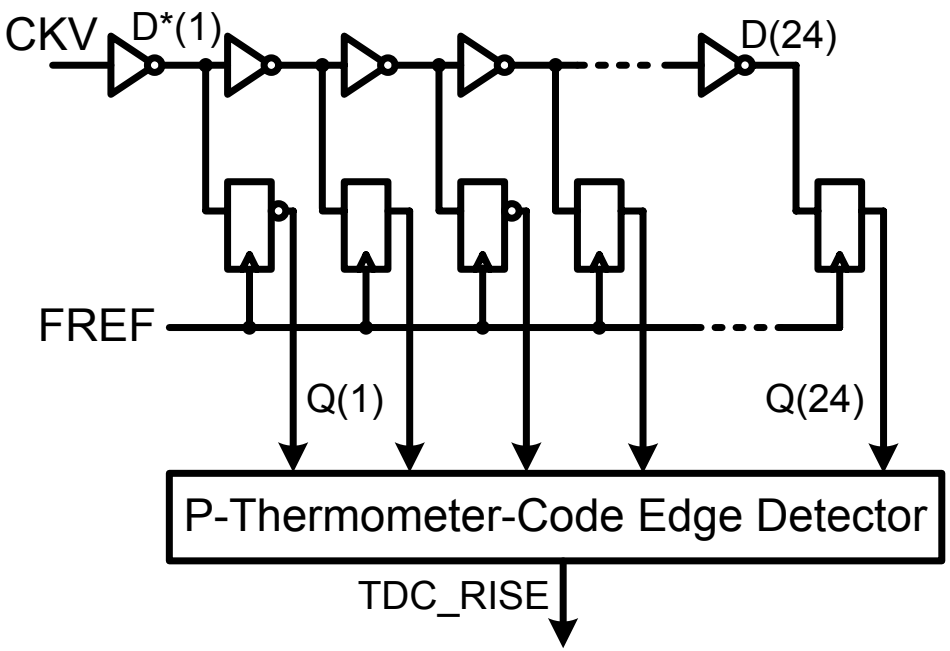
- Quantized phase detector with resolution of <40 ps

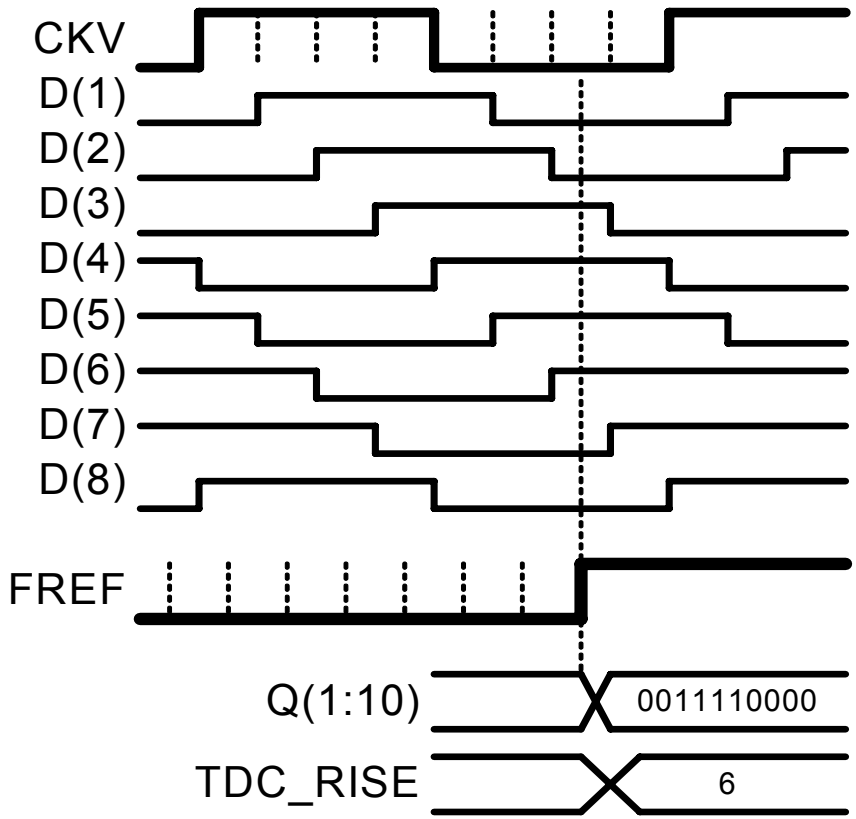




Time-to-digital Converter (TDC)

- Quantized phase detector with resolution of 30 ps
- DCO clock passes through the inverter chain
- Delayed outputs are sampled by FREF

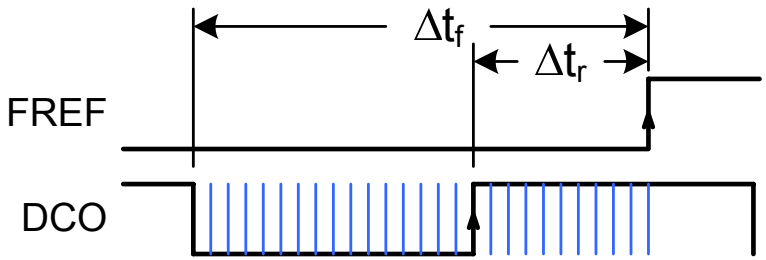




Period Normalization

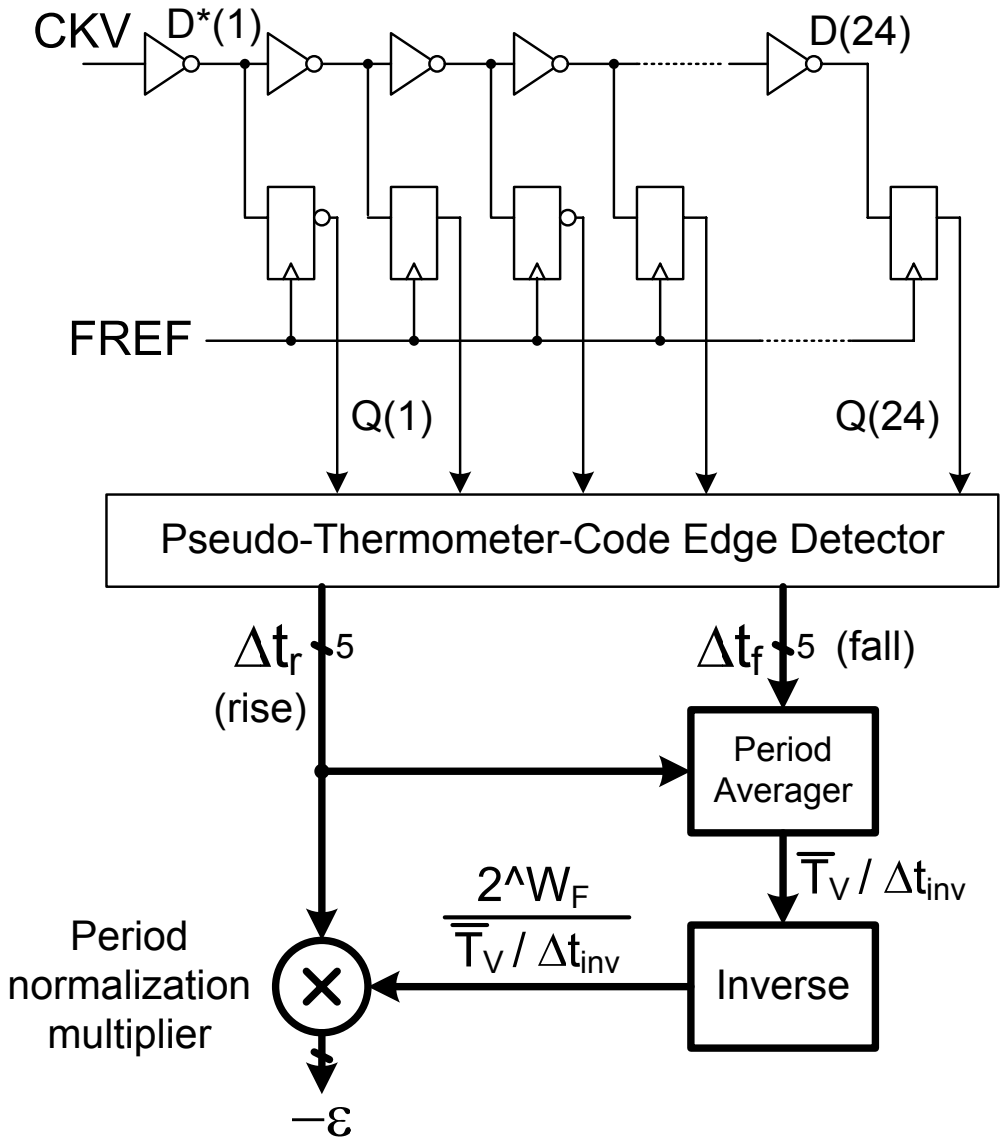
- Expected output between 0.0 – 1.0 UI

$$-\varepsilon = \frac{2^{W_F}}{\overline{T}_V / \Delta t_{inv}}$$



- Accurate calibration of the inverter delay

$$\overline{T}_V = \frac{1}{N_{avg}} \sum_{k=1}^{N_{avg}} T_V[k]$$



Phase Noise Due to TDC

- In-band phase noise at RF output

$$L = \frac{(2\pi)^2}{12}\left(\frac{\Delta t_{inv}}{T_V}\right)^2 \cdot \frac{1}{f_R}$$

  - E.g., Δt_{inv}=40ps, f_v=2.4GHz, f_R=13MHz, **L = -86.3dBc/Hz**

- 1-Hz normalized phase noise floor [5]

$$BFM = \frac{(2\pi)^2}{12} \cdot \Delta t_{inv}{}^2$$

  - E.g., Δt_{inv}=40ps, **BFM = -203dB**
  - Good enough for GSM

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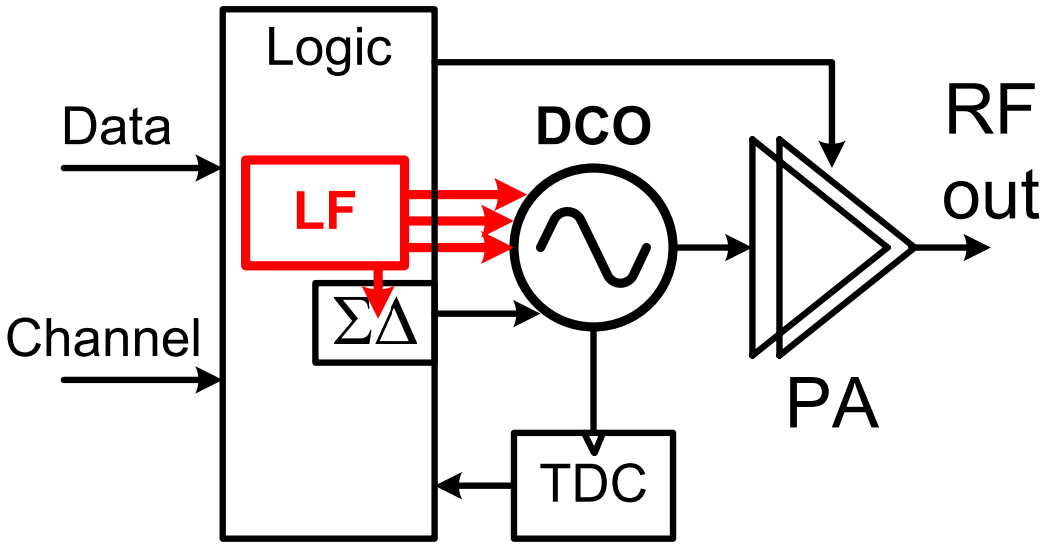
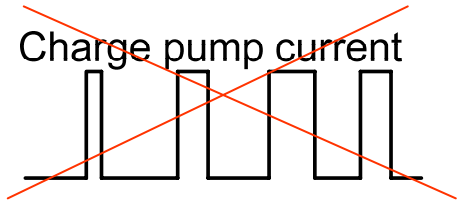
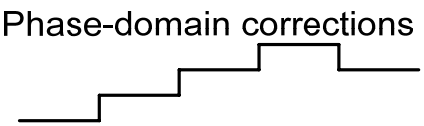


Type-II Loop Filter

- No correlative detection spurs
  - No filtering needed for Bluetooth
- Software programmed PLL loop:
  - Gentle transition of type-I to type-II
- Two "knobs" α, ρ





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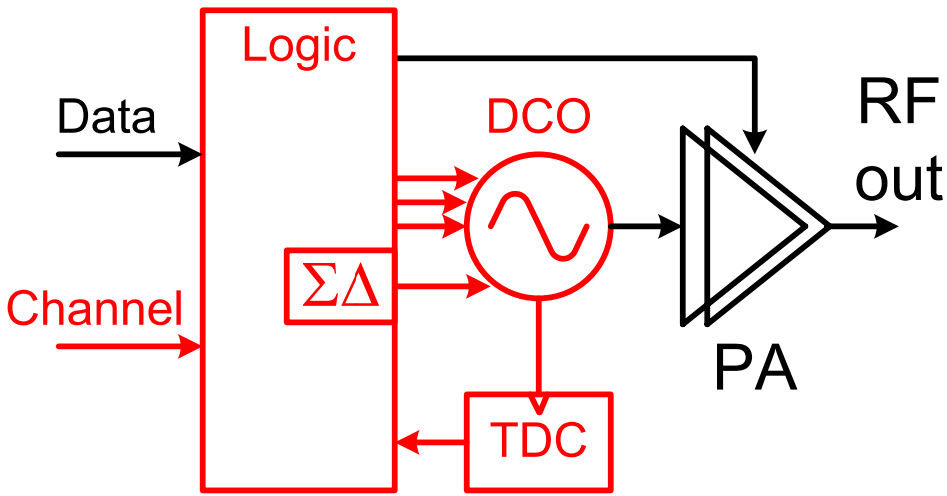
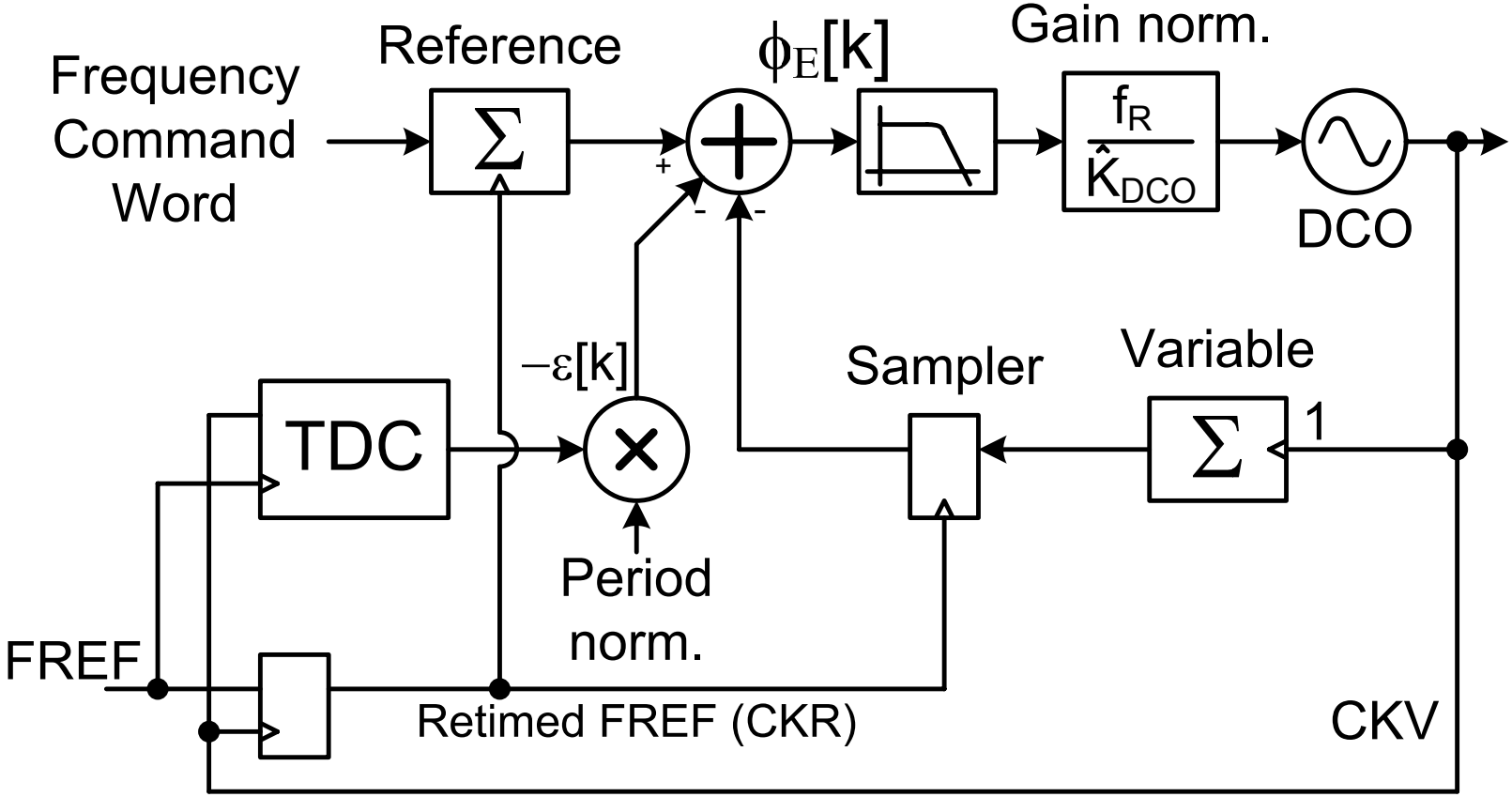


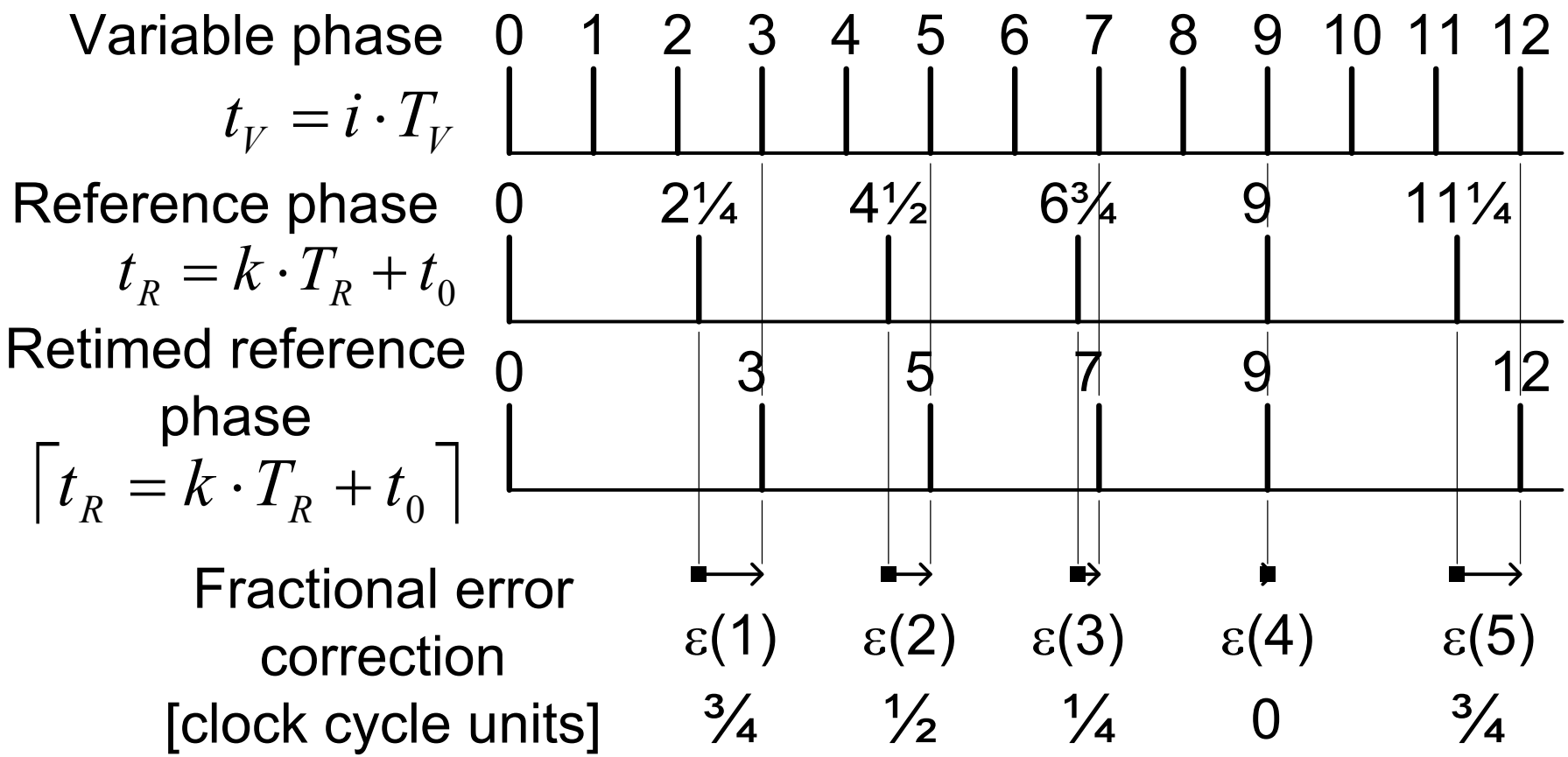
All-Digital PLL (ADPLL)

- Phase domain operation
- Digitally synchronous fixed-point arithmetic
- Phase signals cannot be corrupted by noise



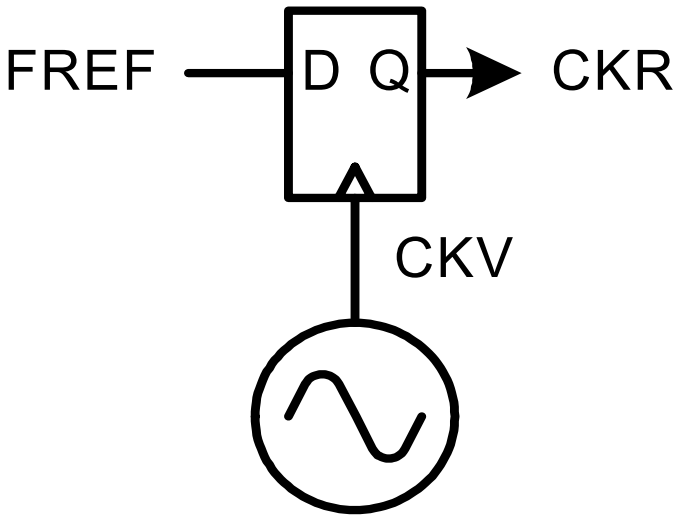
Phase Domain Operation

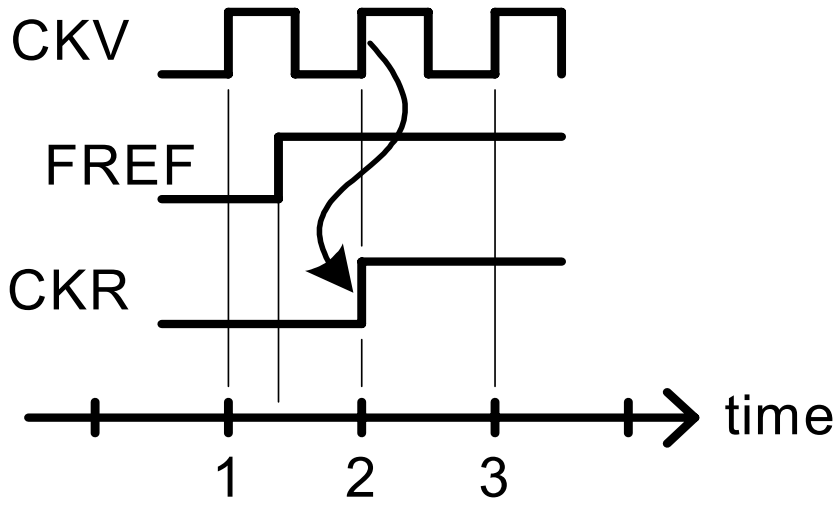
e.g., N=2.25



Reference Phase Retiming

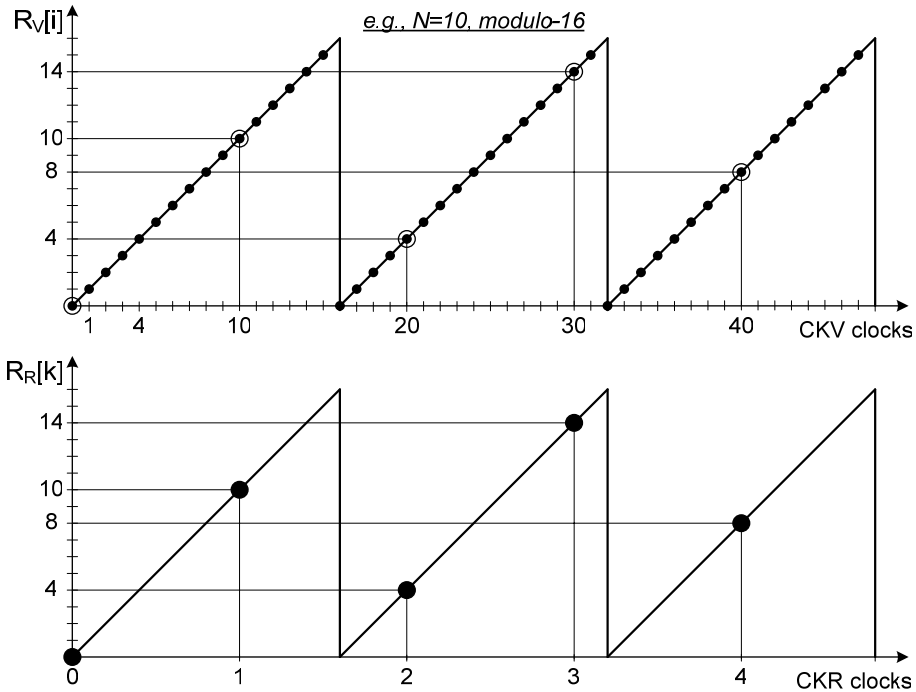
- DCO clock and FREF domains are not entirely synchronous despite being in phase lock
- Variable and reference phases cannot be compared in hardware: metastability!
- Solution: Oversampling FREF by CKV and using the resulting CKR

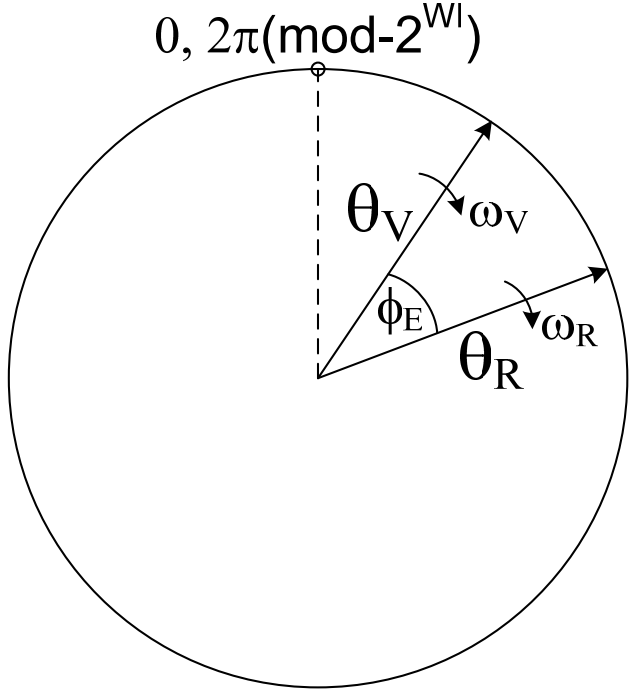




Modulo Arithmetic

- Theoretically, reference and variable phases are linear and grow without bound with the development of time
- R_R and R_V implemented in modulo arithmetic in order to practically limit wordlength
  - $W_I = 8$, $W_F = 15$
- Introduces aliasing: 0 indistinguishable from 2^{WI}

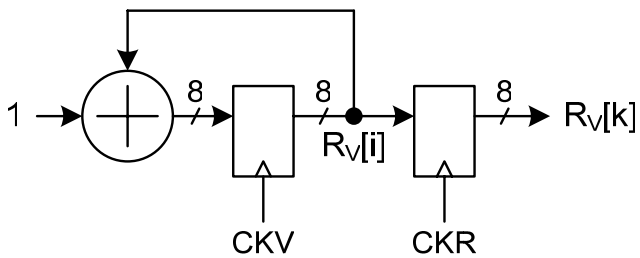




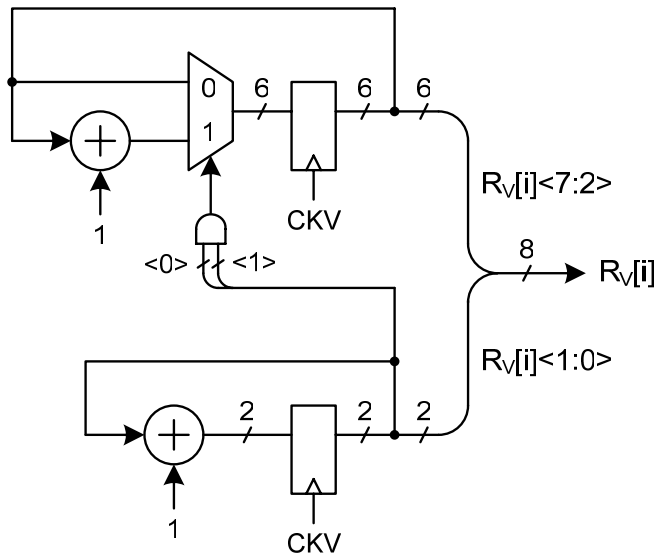
Variable Phase Accumulator

- Implements DCO clock count incrementing
- Deep-submicron process capable of 8-bit incrementing at 2.4 GHz
- Extra timing margin required to guarantee robust operation
- Separated calculation between lower and higher order bits

Function:



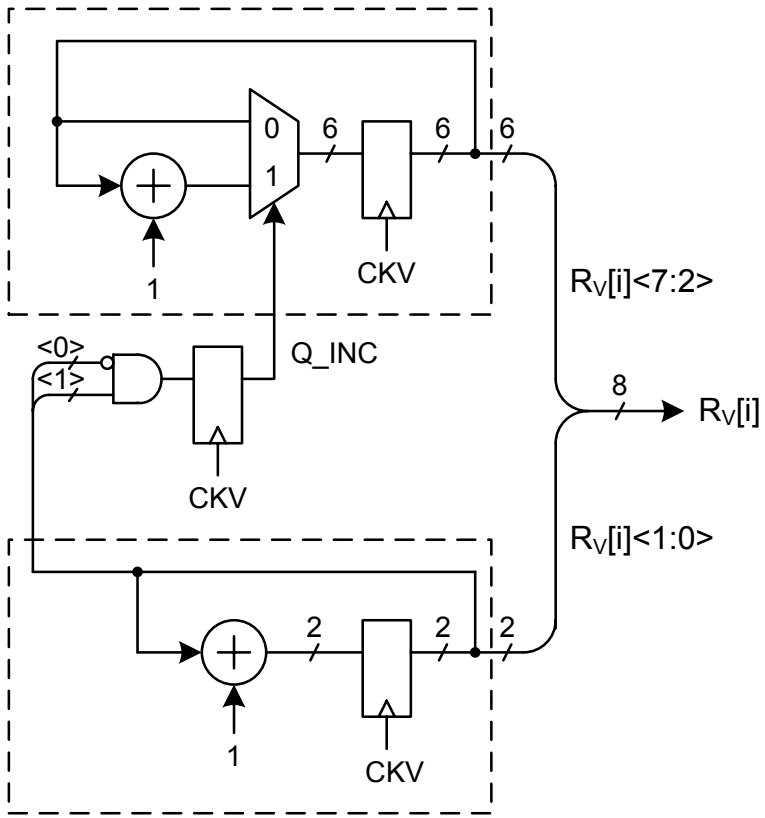
Using pipelining:



bits	
765432	10
000000	00
000000	01
000000	10
000000	11
000001	00
000001	01
000001	10
000001	11
000010	00
000010	01
000010	10
000010	11

Variable Phase Accumulator: Actual Implementation

- High-speed implementation:
- Additional retiming of the carry out signals

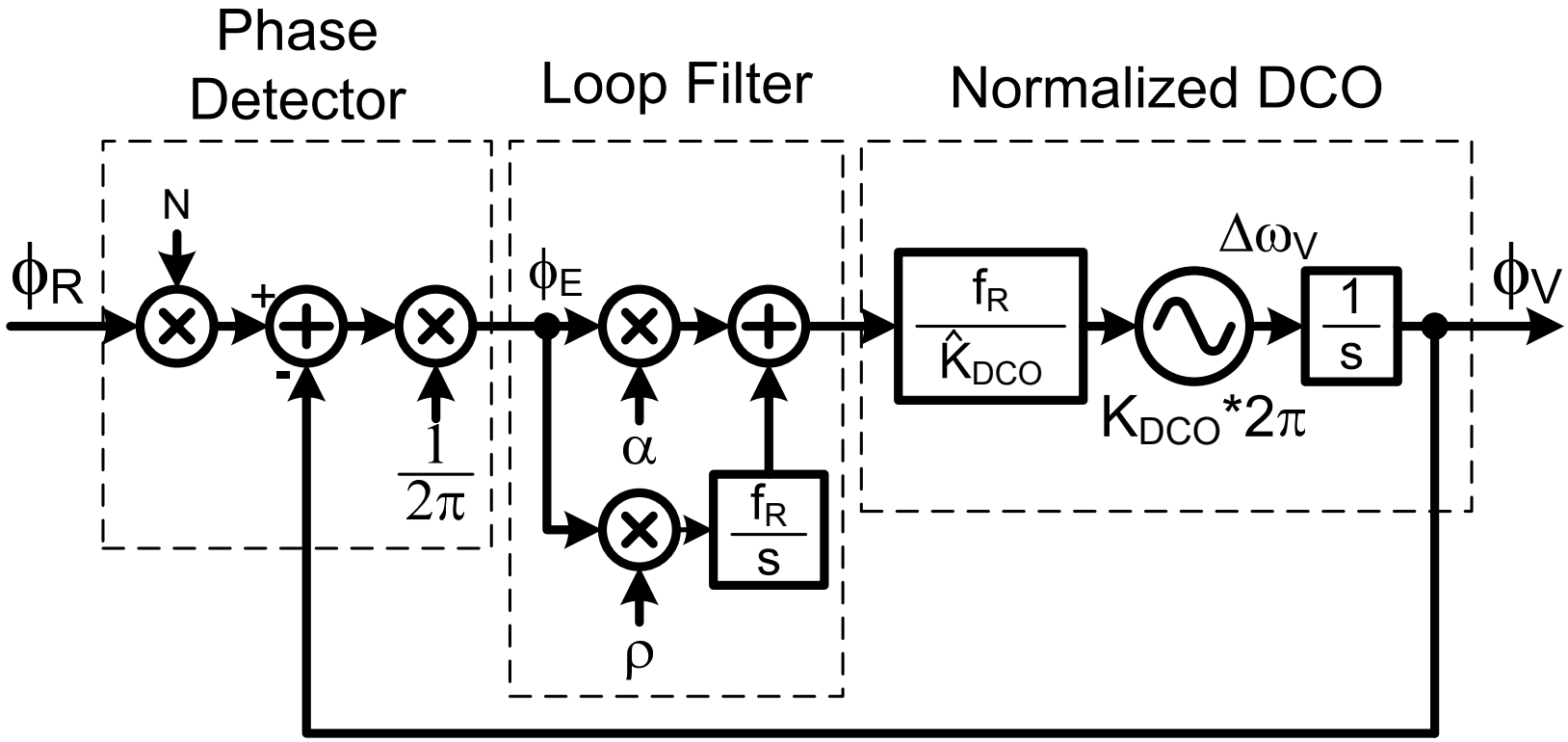


bits 765432	10
000000	00
000000	01
000000	10
000000	11
000001	00
000001	01
000001	10
000001	11
000010	00
000010	01
000010	10
000010	11

Frequency Response

- Type-II second-order PLL loop
- "knobs" α, ρ

$$H_{ol}(s) = (\alpha + \frac{\rho f_R}{s}) \frac{f_R}{s}$$



Closed-Loop Frequency Response

- Closed-loop transfer function

$$H_{cl}(s) = N\frac{\alpha f_R s + \rho f_R^2}{s^2 + \alpha f_R s + \rho f_R^2}$$

- Canonical two-pole control system

$$H_{cl}(s) = N\frac{2\xi\omega_n s + \omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2}$$

Natural frequency

$$\omega_n = \sqrt{\rho} f_R$$

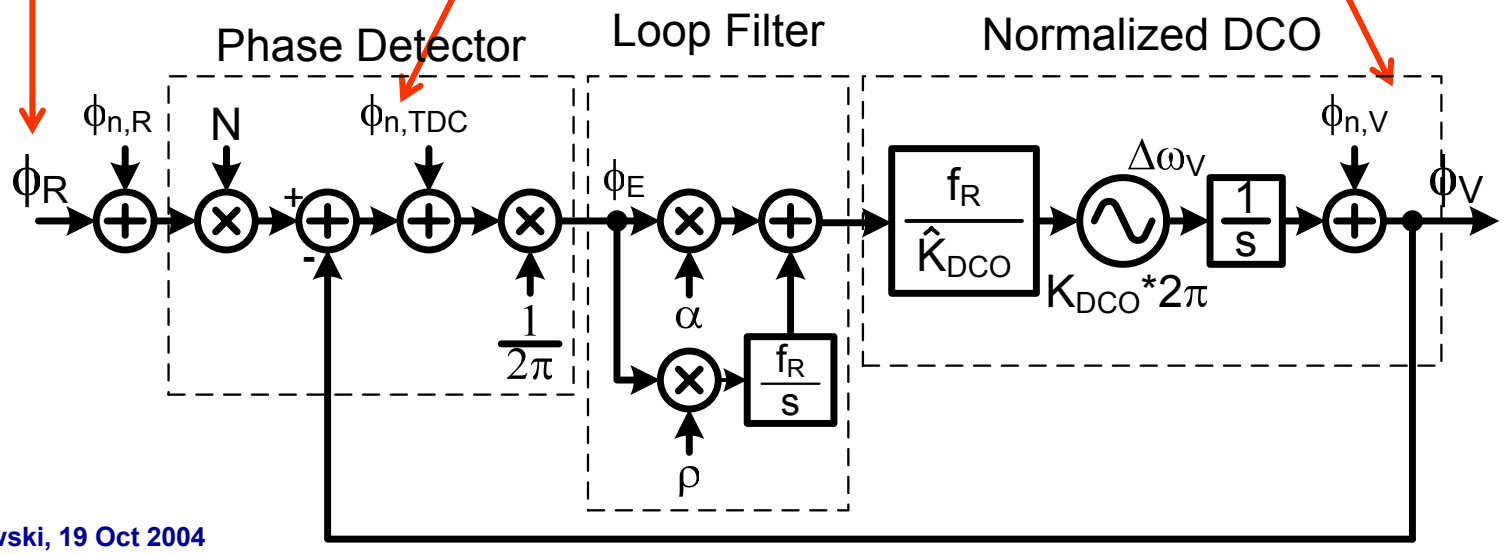
Damping factor

$$\xi = \frac{1}{2}\frac{\alpha}{\sqrt{\rho}}$$

Noise and Error Sources

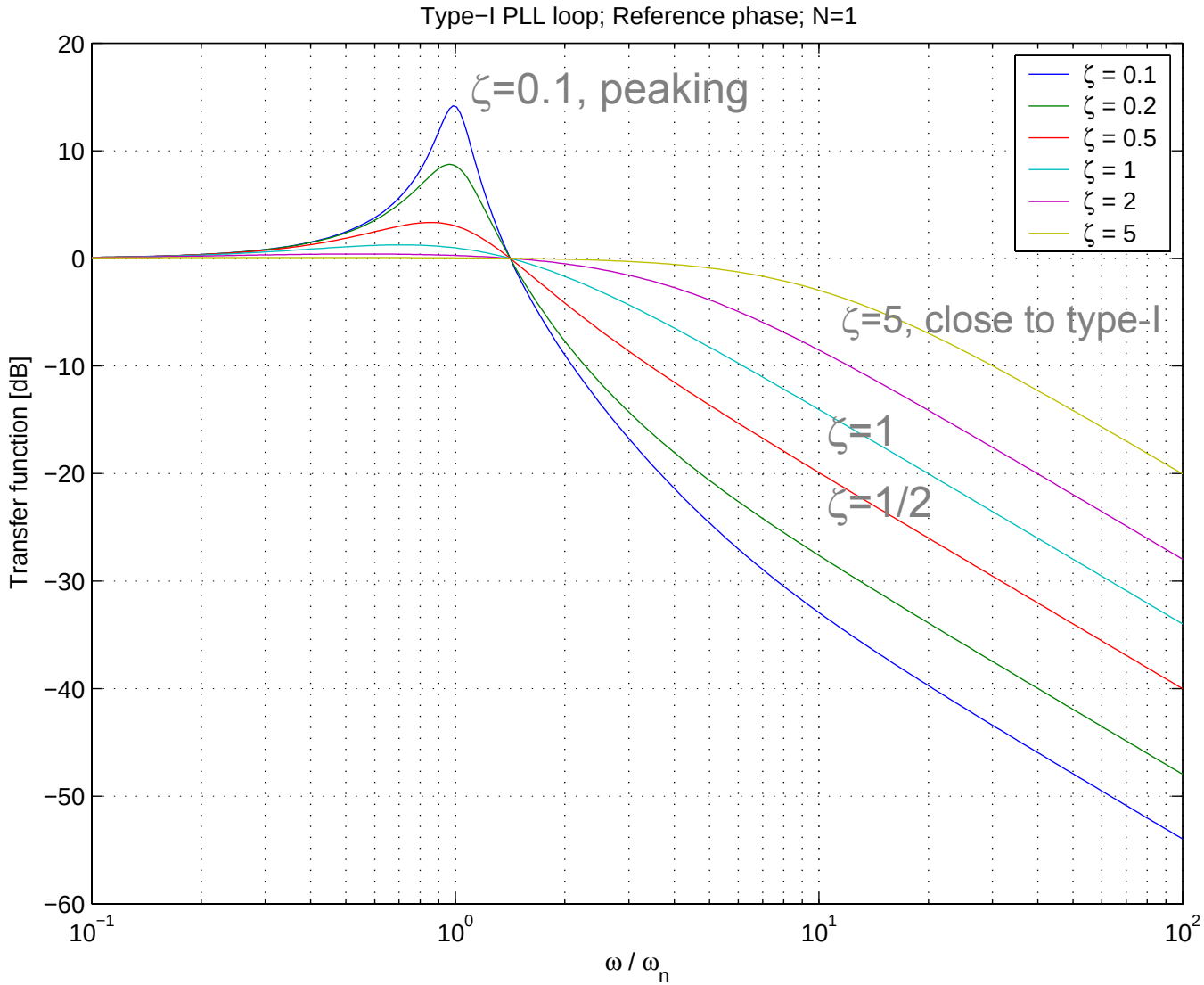
- Only three noise sources
  - Frequency reference (external to ADPLL) – low pass
  - TDC quantization – low pass
  - DCO oscillator – high pass

$$H_{cl,R}(s) = N\frac{H_{ol}}{1+H_{ol}} \qquad H_{cl,TDC}(s) = \frac{H_{ol}}{1+H_{ol}} \qquad H_{cl,V}(s) = \frac{1}{1+H_{ol}}$$



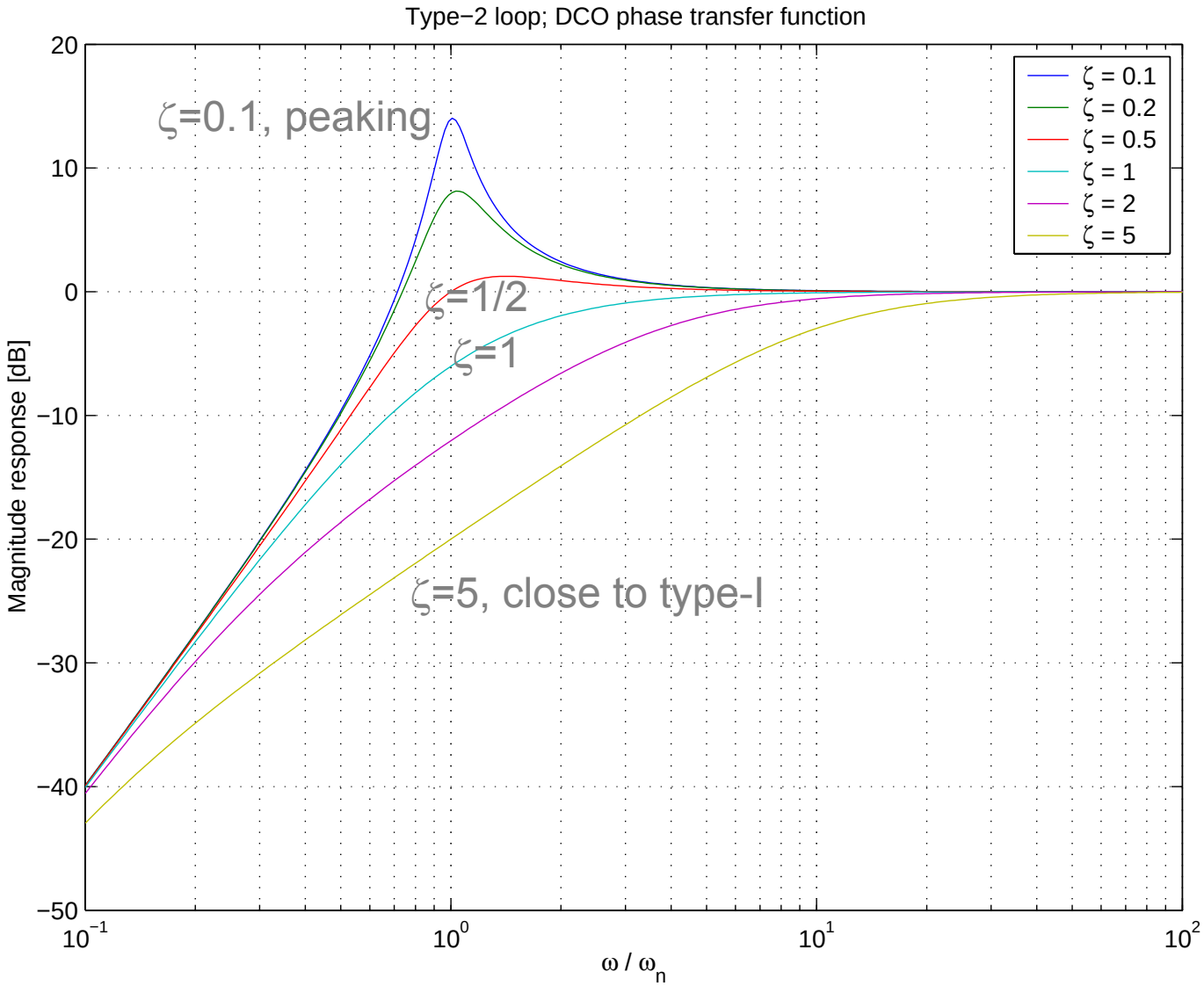
FREF / TDC Transfer Function

- Type-II 2nd order
- Weak filtering



DCO Transfer Function

- 20 dB/dec
  - Type-I
- 40 dB/dec
  - Type-II
- 1/f noise attenuation



Digitally-Controlled Oscillator (DCO)

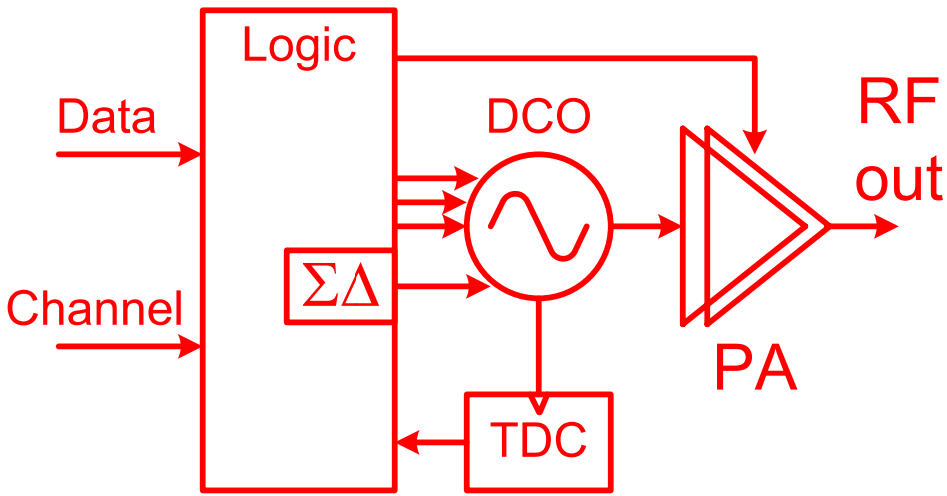
ΣΔ Dithering of DCO

Time-to-Digital Converter (TDC)

Digital Loop Filter (LF)

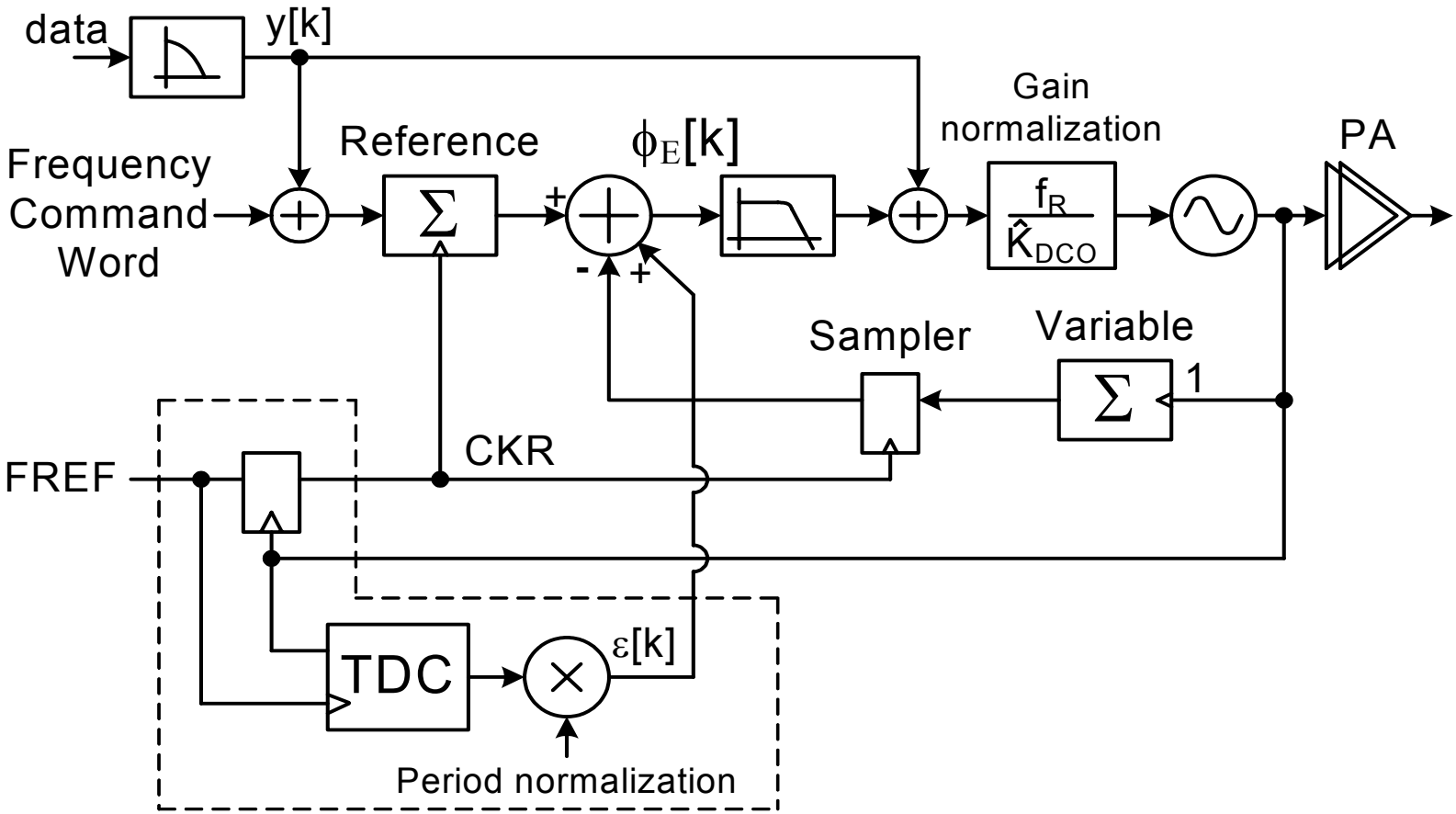
All-Digital PLL (ADPLL)

All-Digital Transmitter



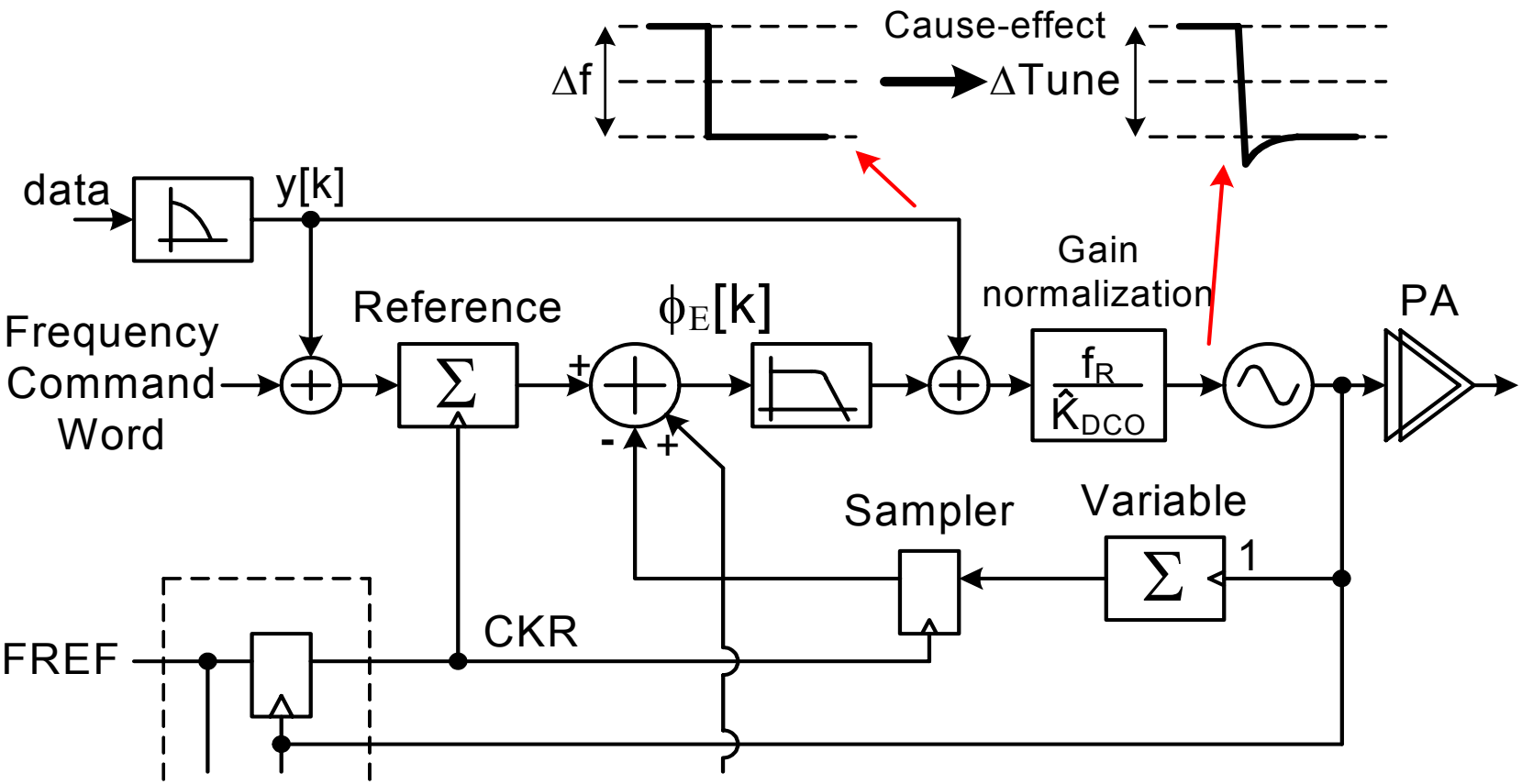
ADPLL-Based Transmitter

- ADPLL provides a wideband modulation
- Class-E power amplifier

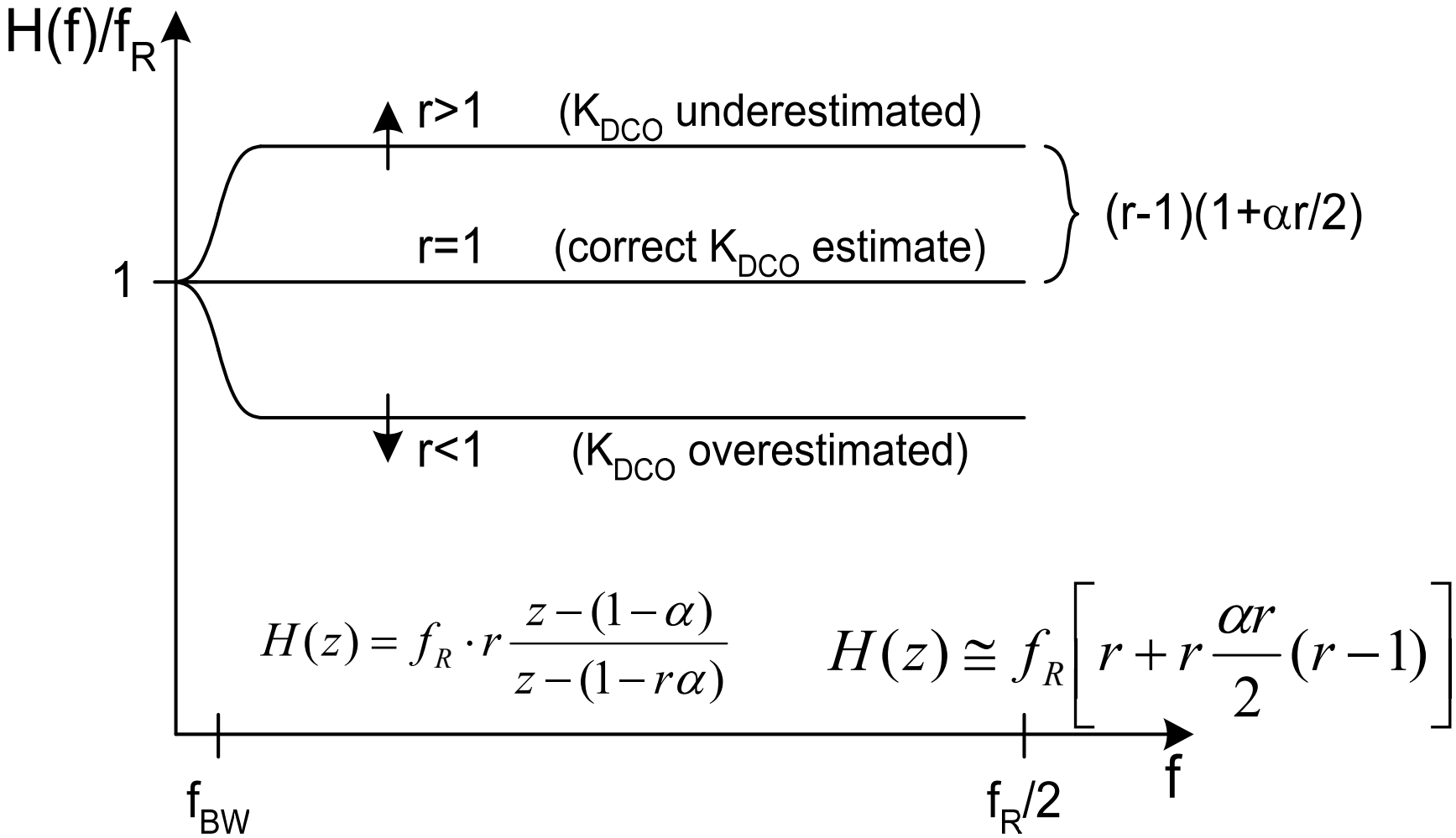


Predictive/Close Loop PLL

- Two-point modulation
  - Direct feedforward path – y[k] directly drives the DCO
  - Compensating path – y[k] added to the channel FCW

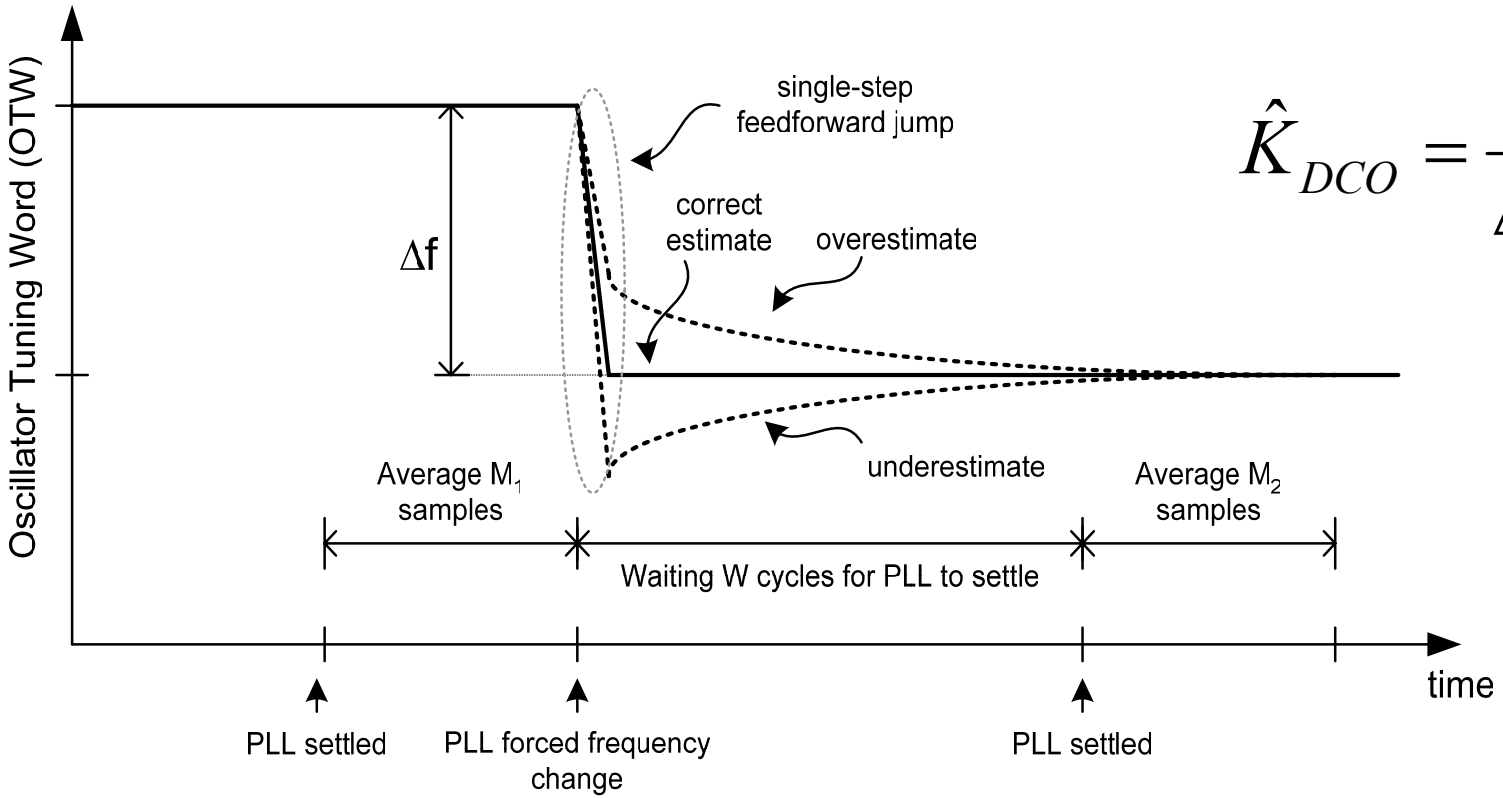


Error in DCO Gain Estimation



- Transfer function somewhat high-pass or low-pass

Just-in-time DCO Gain Estimation

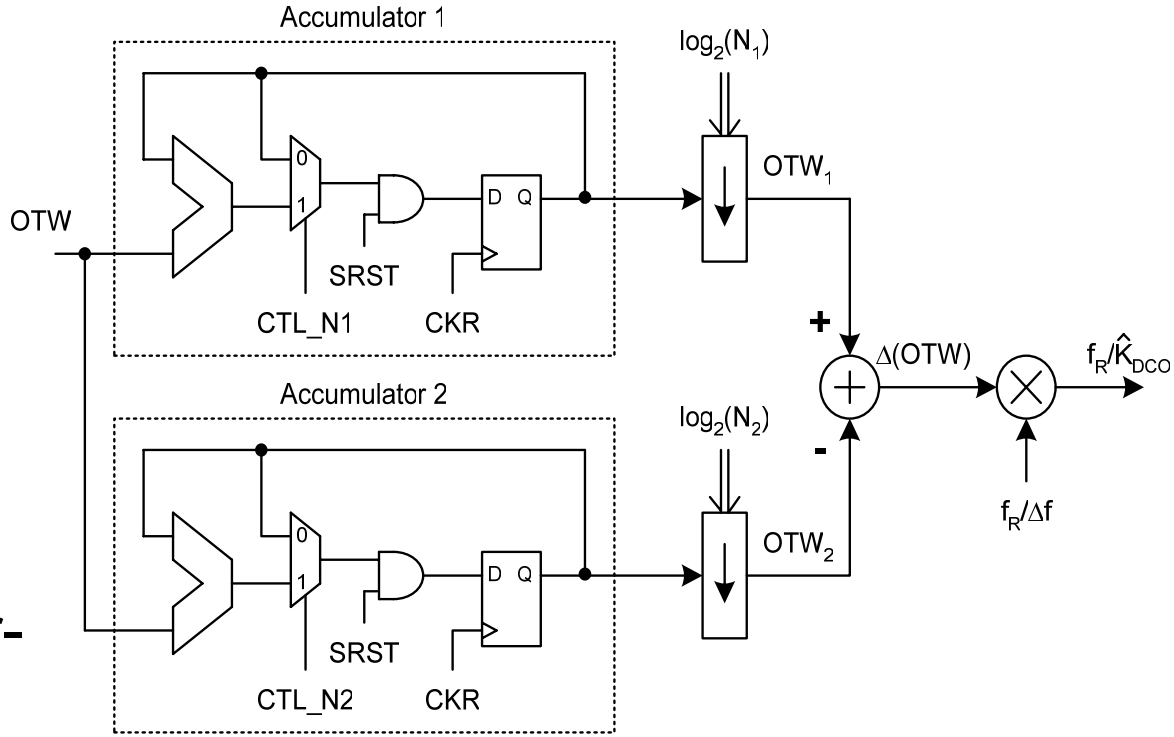


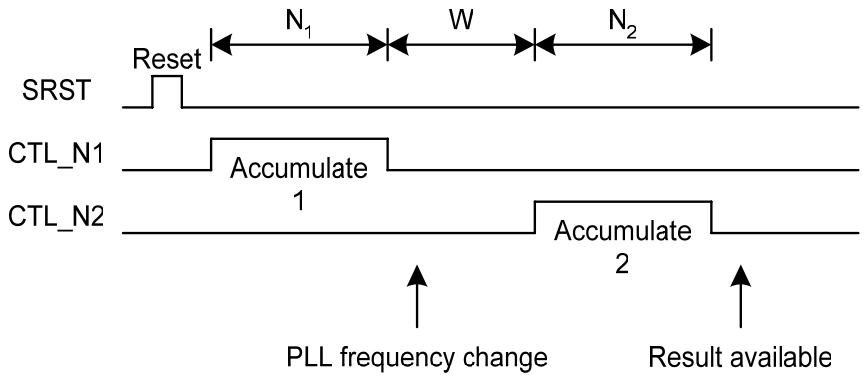
$$\hat{K}_{DCO} = \frac{\Delta f}{\Delta OTW}$$

- Forces Δf through the PLL
  - Δf is accurate since it is represented in digital manner
- Measures steady-state ΔOTW
  - Measured digitally

Hardware Realization

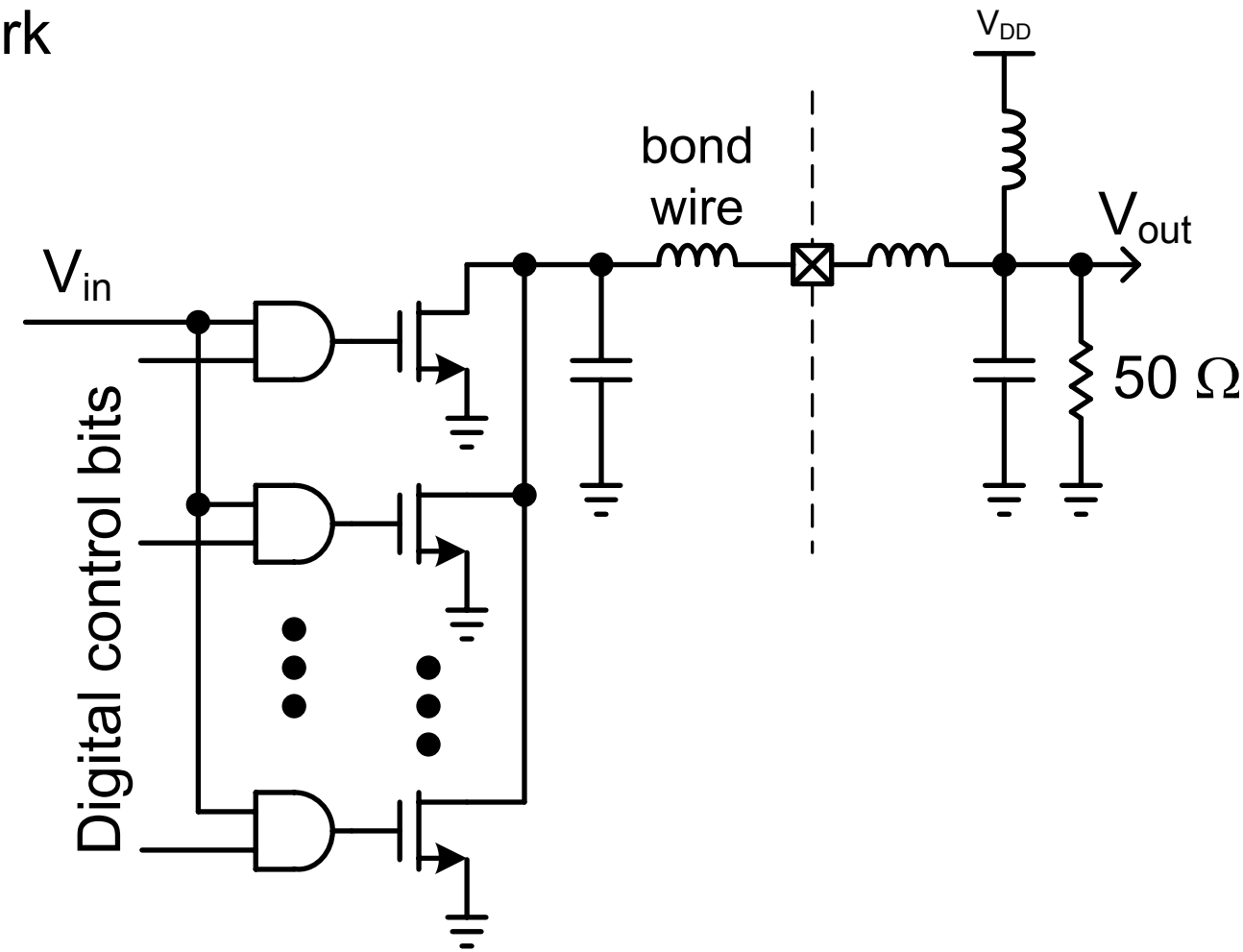
- Synchronous register reset
- N1 samples summed up by Accumulator 1
- N2 samples summed up by Accumulator 2
- N1 and N2 are power-of-two integers
- Division operation is a trivial right-bit-shift





RF Power Amplifier

- Binary weighted MOS switches: 3.5 bits
- Matching network
- Near class-E



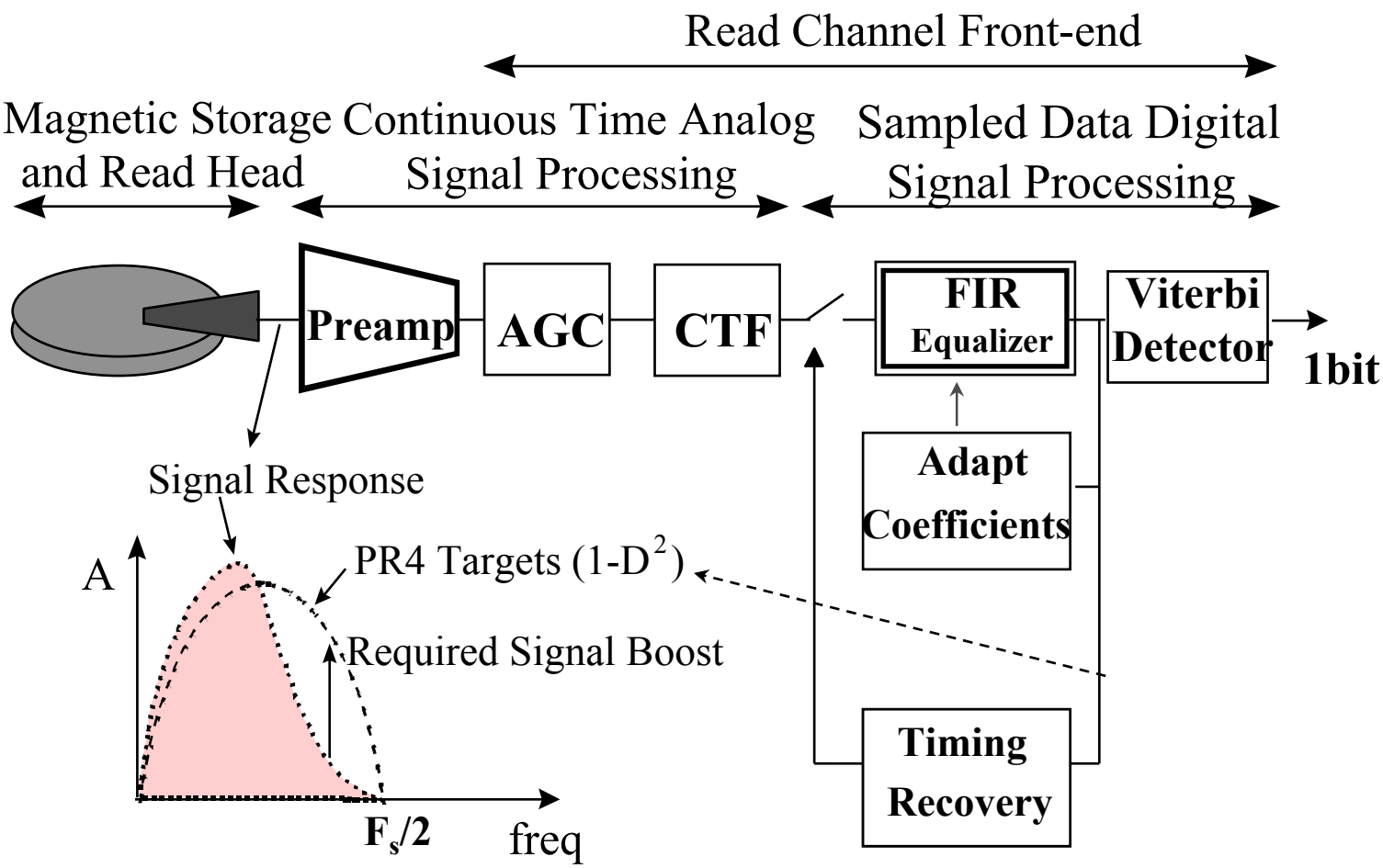
Summary of ADPLL Architecture

- All-digital PLL (ADPLL) frequency synthesizer for wireless applications
  - Digitally-controlled oscillator (DCO)
  - Time-to-digital converter (TDC)
  - Digital PLL loop filter
- Uses digital techniques from the ground up
  - Digital design, simulation, verification, layout and testing
- Only two internal phase noise sources
  - Potentially better phase noise performance
- All-digital TX
  - Wideband frequency modulation capability of ADPLL
  - Class-E PA

Timeline

- **1999: DRP idea conceived**
- 2000: X1734 testchip: Digitally-controlled oscillator (DCO)
- 2001: X1743 testchip: Full Bluetooth transmitter
- 2002: Single-chip commercial Bluetooth radio
- 2003: Single-chip GSM transceiver
- 2004: Single-chip commercial GSM radio

PRML Read Channel



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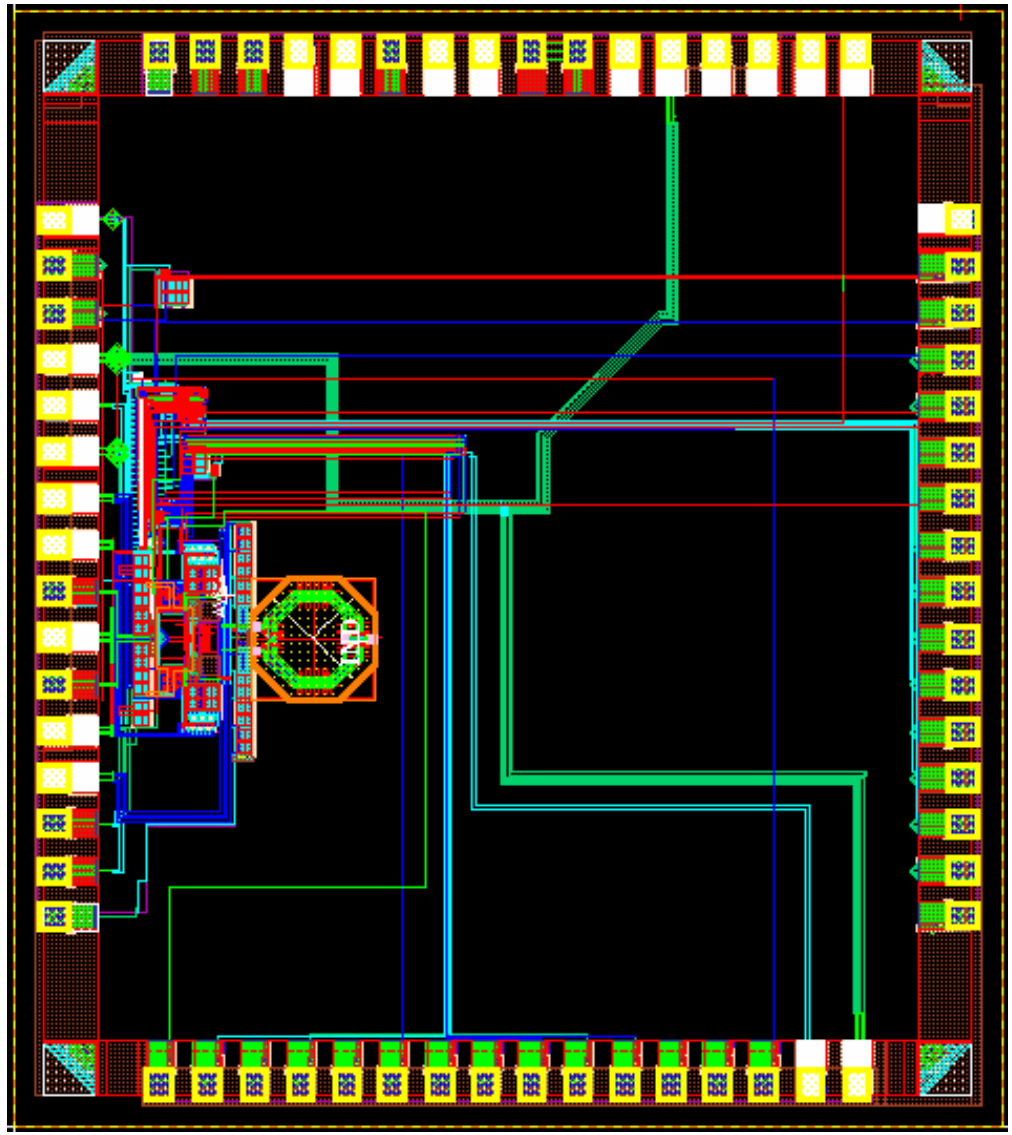
X1734 Testchip Layout

- Digitally-controlled oscillator (DCO)
- DCO digital interface logic

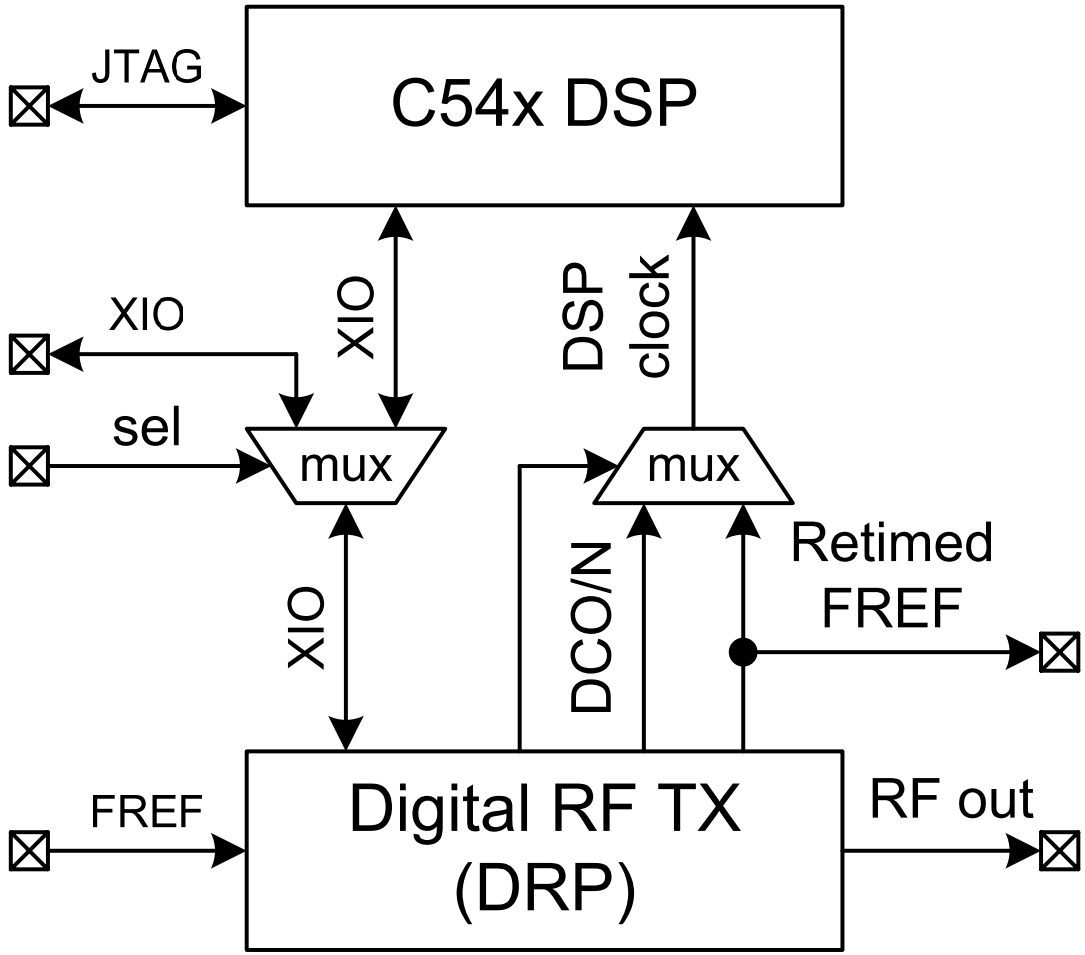


Timeline

- 1997: Beginning of a journey: CMOS hard-disk drive read channel
- 1999: DRP idea conceived
- 2000: X1734 testchip: Digitally-controlled oscillator (DCO)
- **2001: X1743 testchip: Full Bluetooth transmitter & DSP**
- 2002: Single-chip commercial Bluetooth radio
- 2003: Single-chip GSM transceiver
- 2004: Single-chip commercial GSM radio

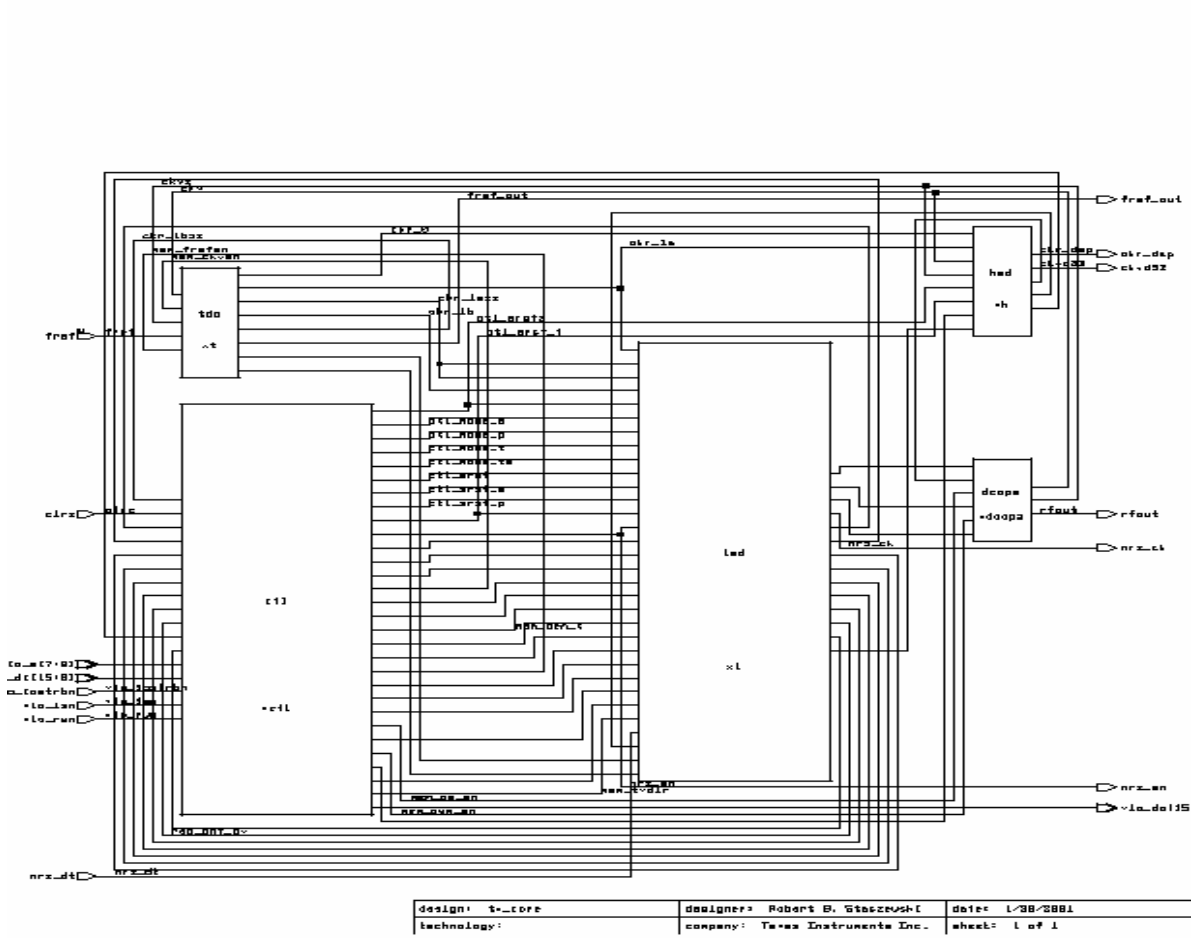
SoC: DSP and Digital RF Transmitter

- C54X DSP tightly integrated with a digital RF transmitter
- TX registers mapped into the DSP space
- Digital Radio Processor (DRP)
- The clocks are retimed to the DRP oscillator
- DRP provides all the DSP clocks
- **First ever IC to integrate RF into a processor core**



X1743 Transmitter Implementation

- Top-level “tx_core” schematics viewed in Synopsys Design Analyzer
- Automatically generated from VHDL code (RTL)



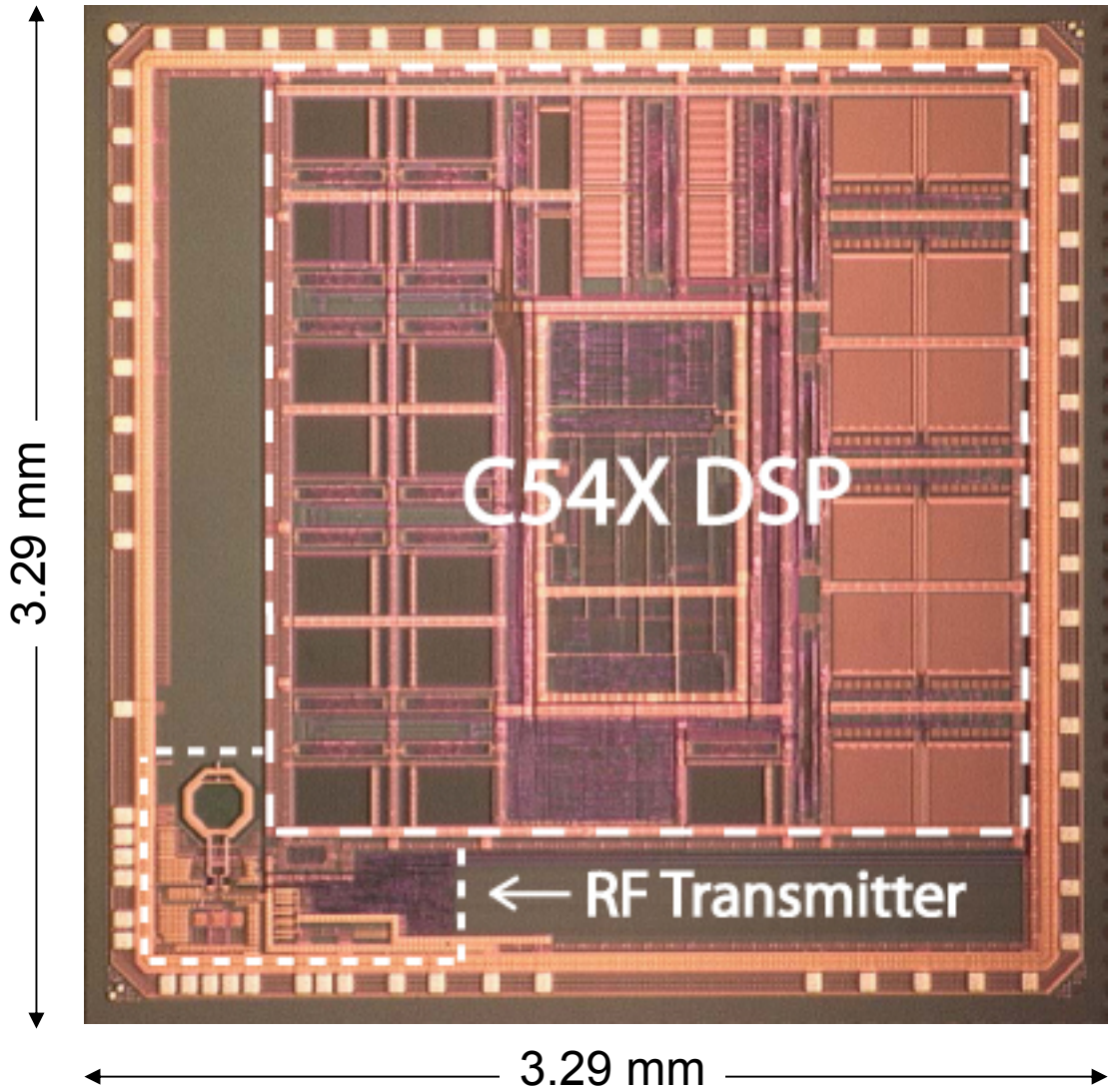
Implementation

- Digital deep-submicron 0.13μm CMOS process with no analog extensions
- RF and analog integrated with digital

Interconnect material	copper
Minimum metal pitch	0.35 um
Transistor nom. voltage	1.5 V
L drawn	0.11 um
L effective	0.08 um
Gate oxide	29 A

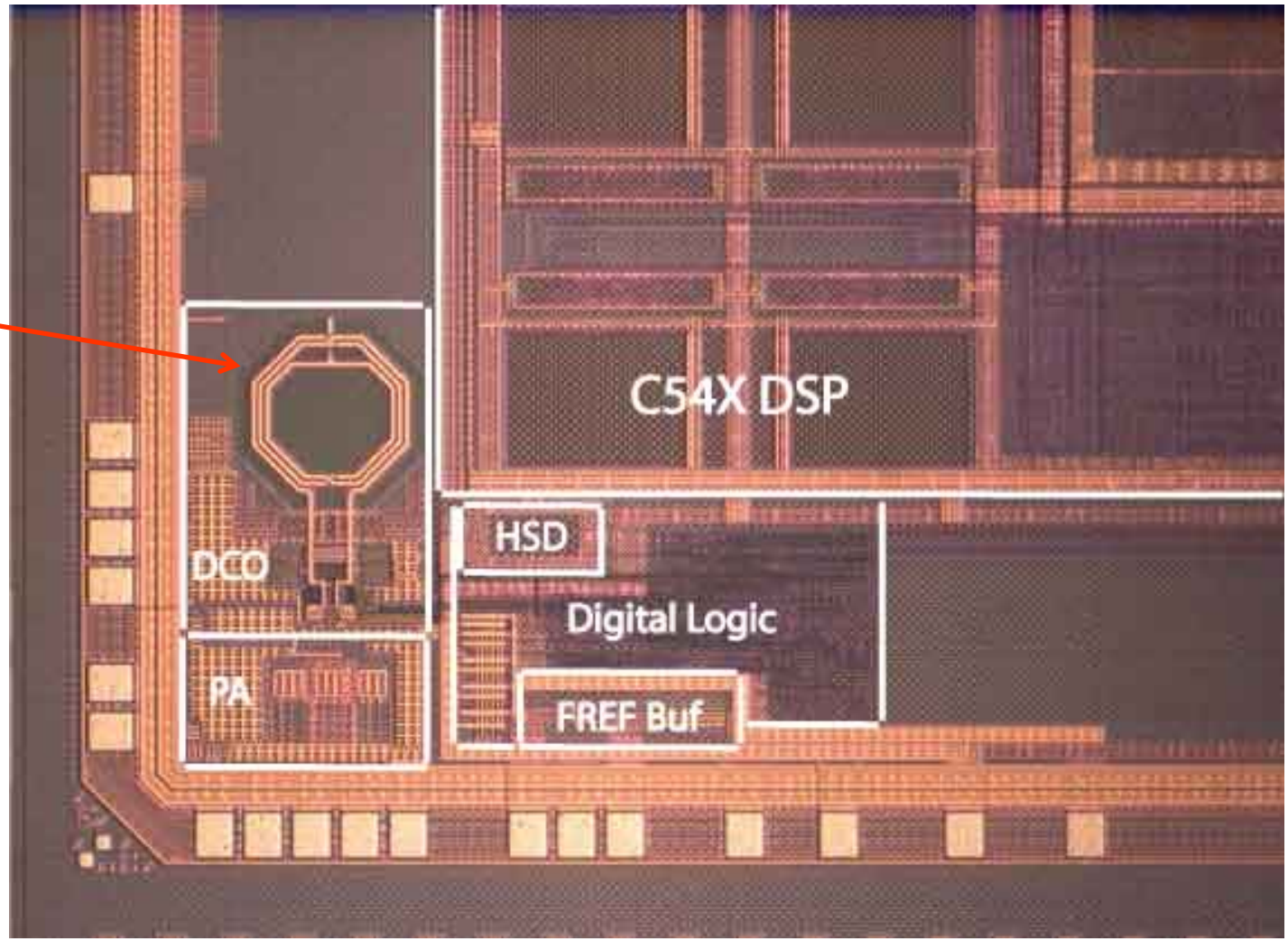
X1743 Chip Micrograph

- C54X DSP used in 2.5G cellular phones
- DSP occupies 2.43 mm x 2.47 mm
- I/O pads: 160 um
- 150 Kgates / mm^2



X1743 RF Area Micrograph

Inductor:
270x270 um



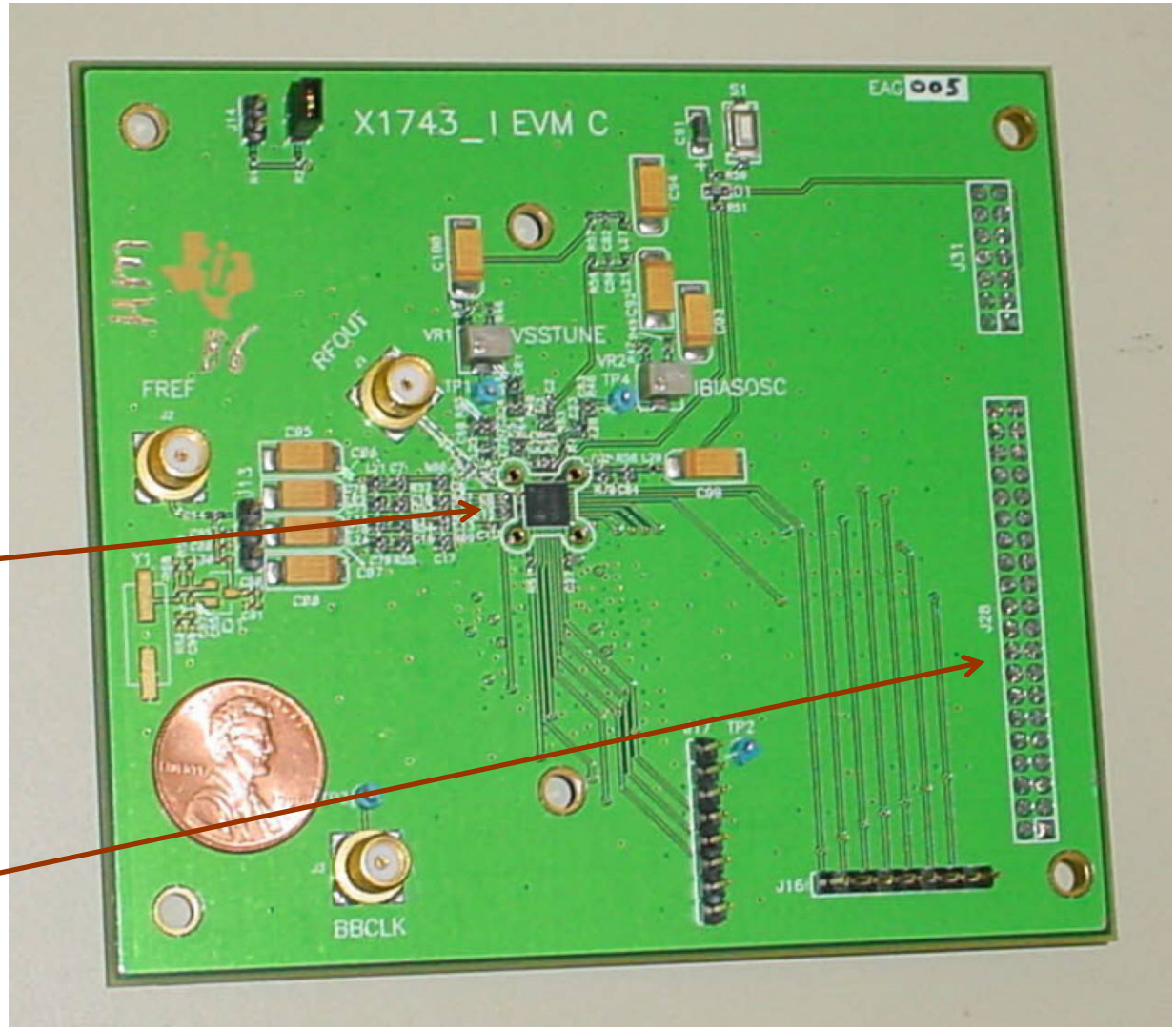
RF transmitter area: 0.54 mm^2

X1743 Evaluation Board

6-layer printed circuit board (PCB) of standard FR4 material

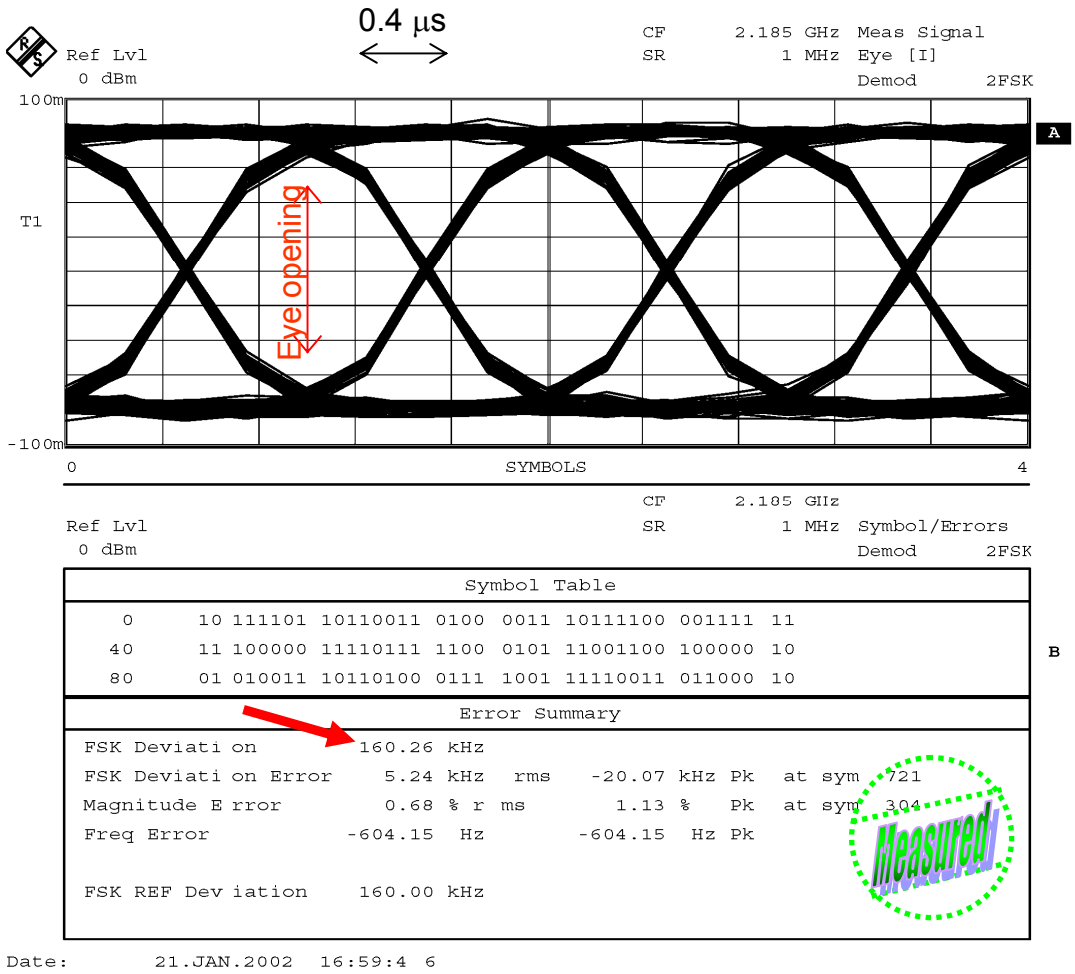
X1743 test chip: 5x5 mm MicroStar Junior ball-grid array (BGA) package

To: PC interface board

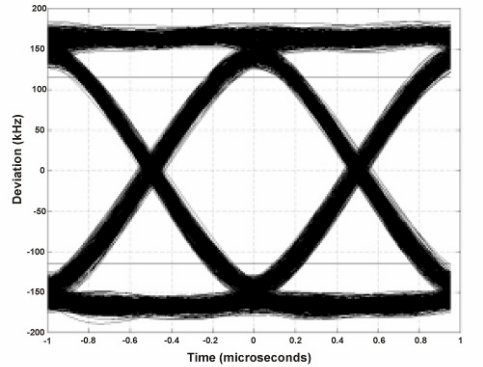


Eye Diagram

- Pseudo-random modulated data
- Measured with Rohde&Schwarz RFIQ-7 signal analyzer
  - Downconversion and FM demodulation
- X-axis: time evolution in 1 μs symbols

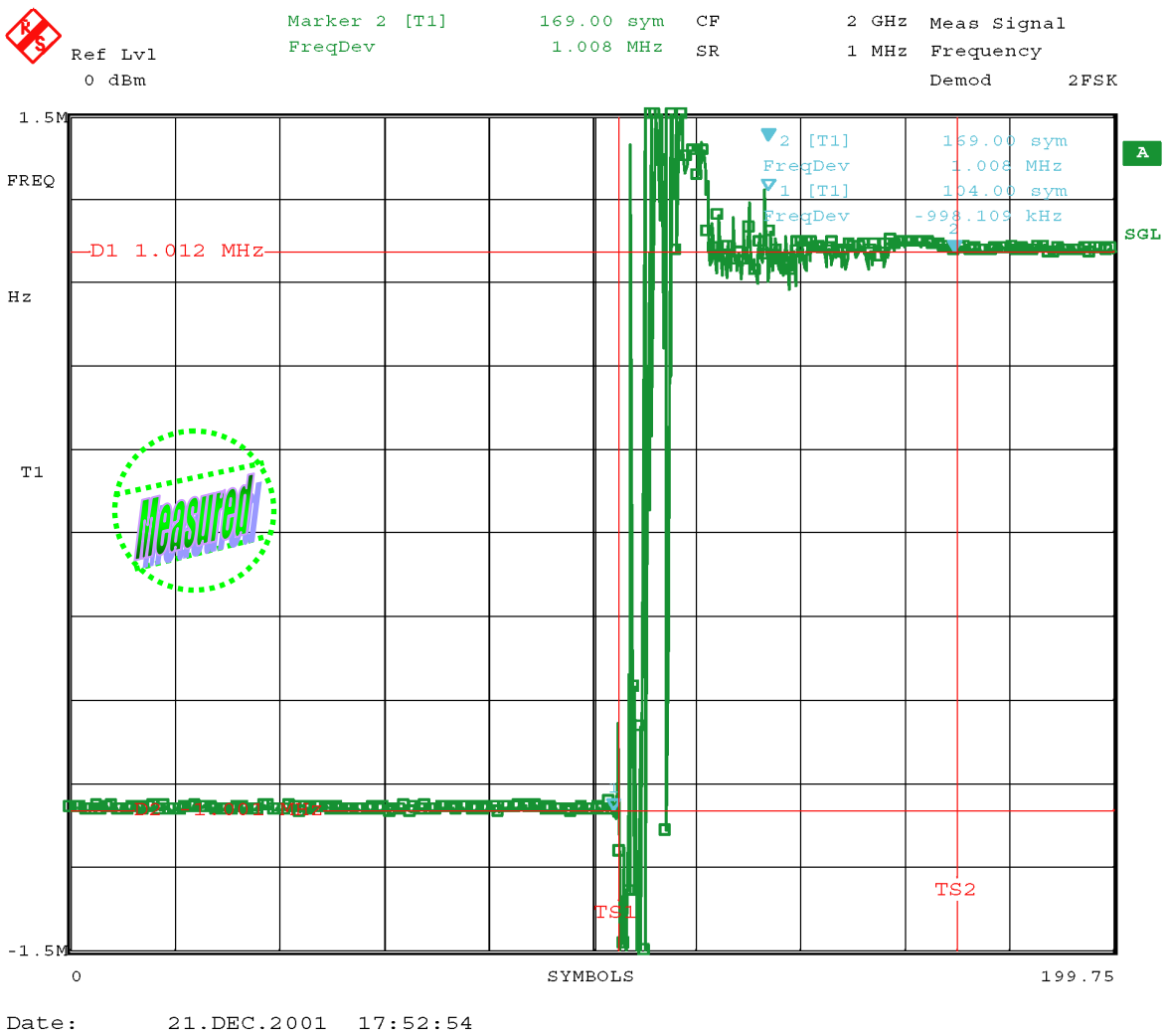


Compare with best-in-class: CSR Bluecore2 (www.csr.com)



Switching Transients

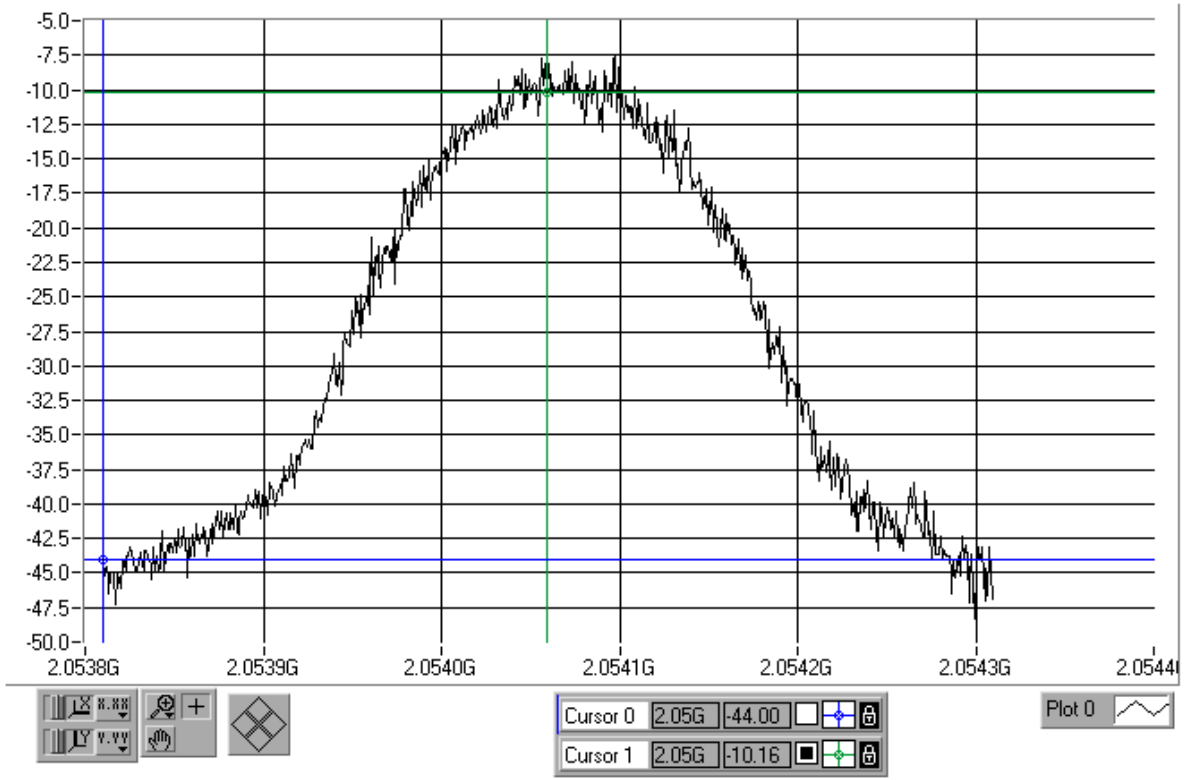
- DSP program written to step ADPLL through the three operational modes
- RF output measured by Rohde&Schwarz FSIQ-7 signal analyzer
- Y-axis: 300 kHz per grid
- X-axis: time progression of 1 μs symbols; 20 μs per grid
- Forced frequency step of 2 MHz
  - PVT: 5 μs
  - Acquisition: 25 μs
  - Fast tracking: 18 μs
- Settling time: 65 μs



DSP-driven Modulation

- Demonstrates tight integration between DSP and RF
- DSP C-program to perform GSM modulation of the transmitter instead of Bluetooth modulation in a dedicated hardware
- Precalculated data resides in RAM: fetched every 6 FREF cycles and added to FCW

- GSM data rate: 270.833 kHz
- FREF = 13 MHz
- OSR = 48



X1743 Performance Summary

Phase noise	<114 dBc/Hz @ 500 kHz
Spurious noise	< 62.5 dBm (with antenna filter)
DCO frequency pushing	600 kHz/V
PA output power	4 mW @ 50 ohm load
RMS phase error	2.06 deg
ADPLL settling time	< 50 us

Outline

- Introduction: Conventional RF
- Why digital RF / Digital Radio Processor (DRP)?
- 1997: Beginning of a journey: CMOS hard-disk drive read channel
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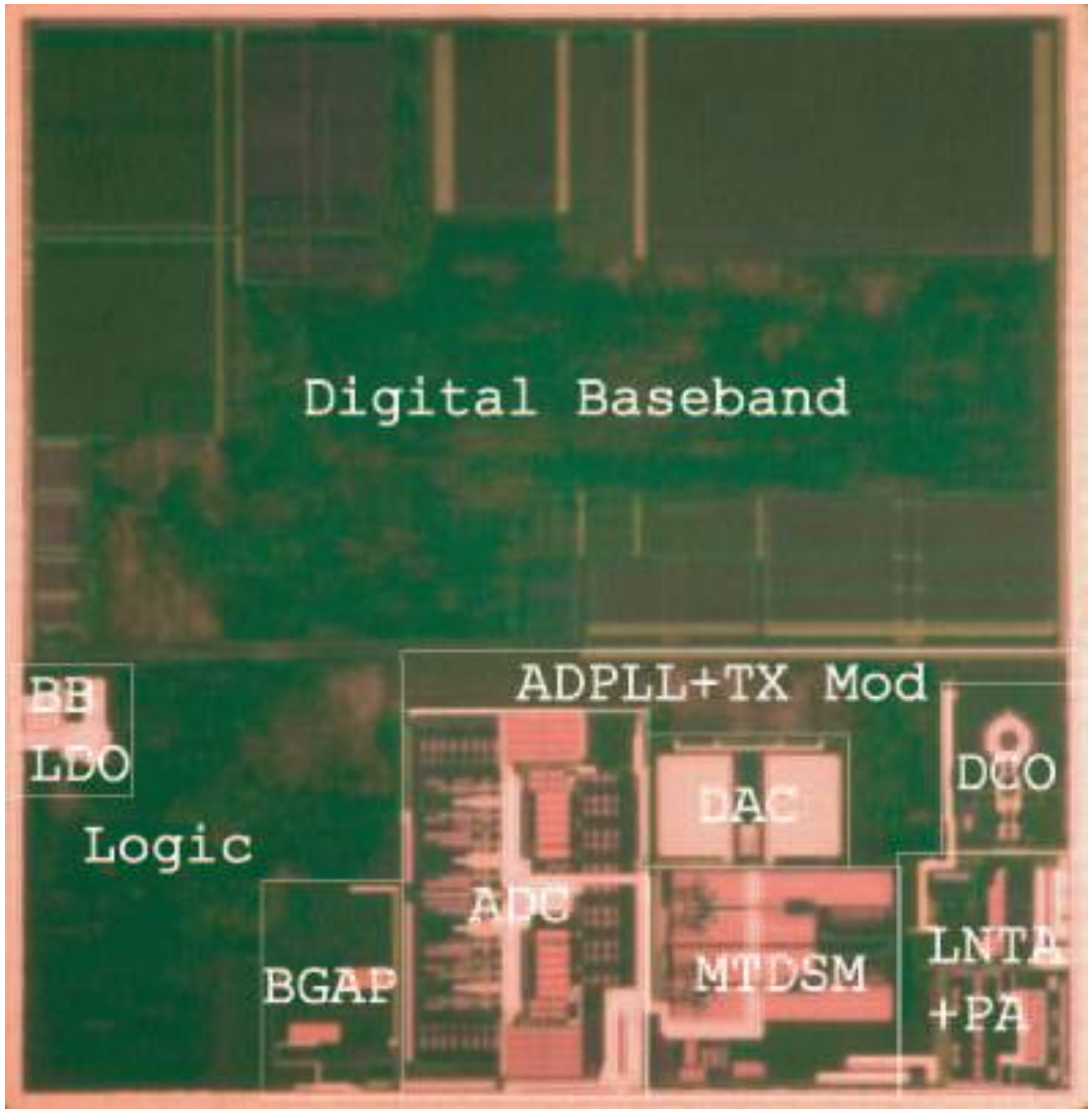
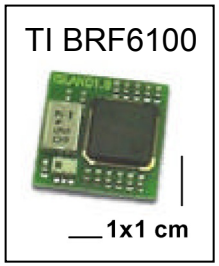
- **2002: Single-chip commercial Bluetooth radio**
- 2003: Single-chip GSM transceiver
- 2004: Single-chip commercial GSM radio
- Conclusions

“Island” Chip Micrograph

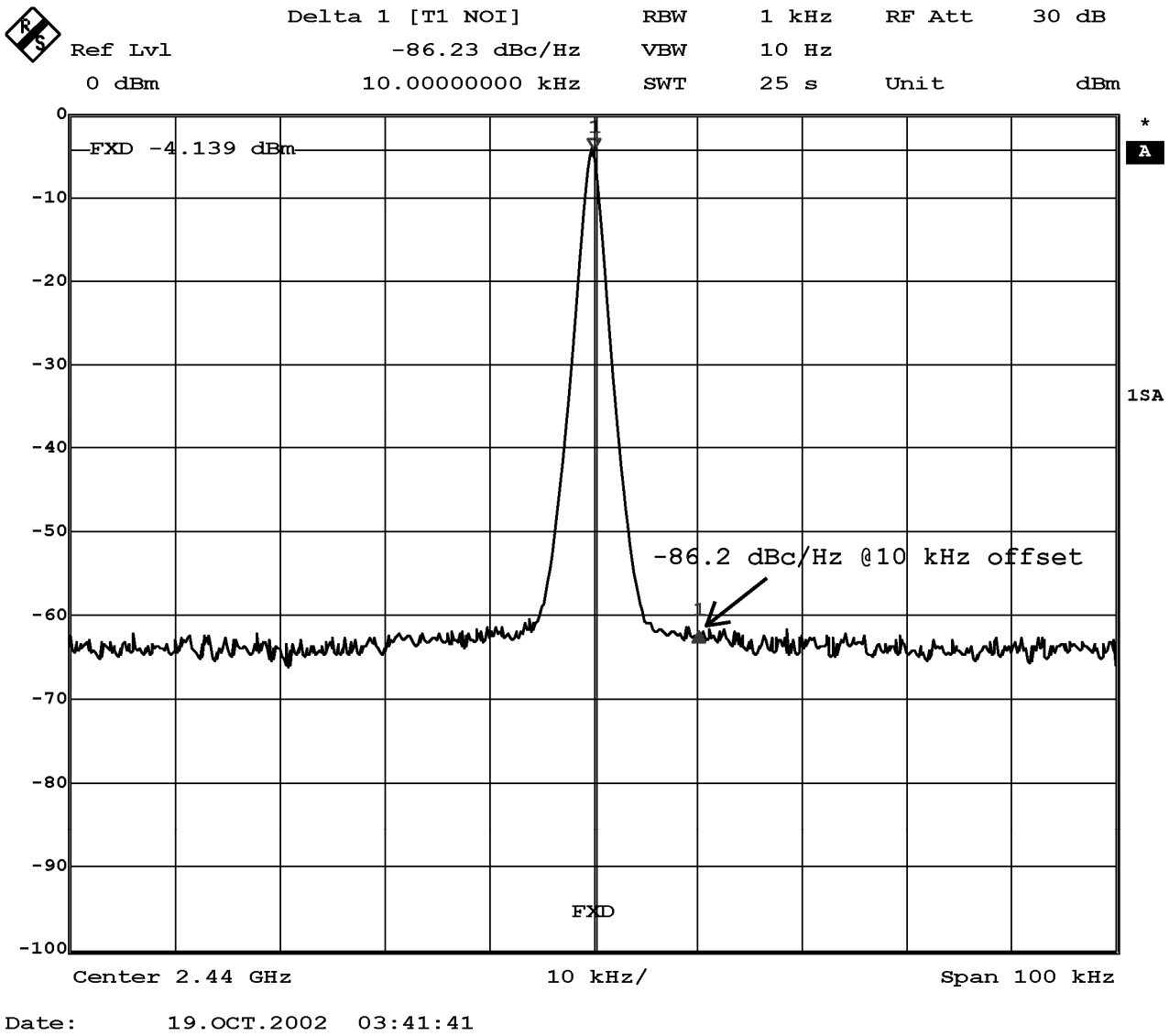


- Commercial single-chip Bluetooth radio
- 0.13um CMOS
- TX path
  - DCO
  - ADPLL
  - TX Modulator
  - Digital PA
- Low TX current
  - 25 mA @ 1.5 V (continuous mode)
  - 2.5 dBm PA power



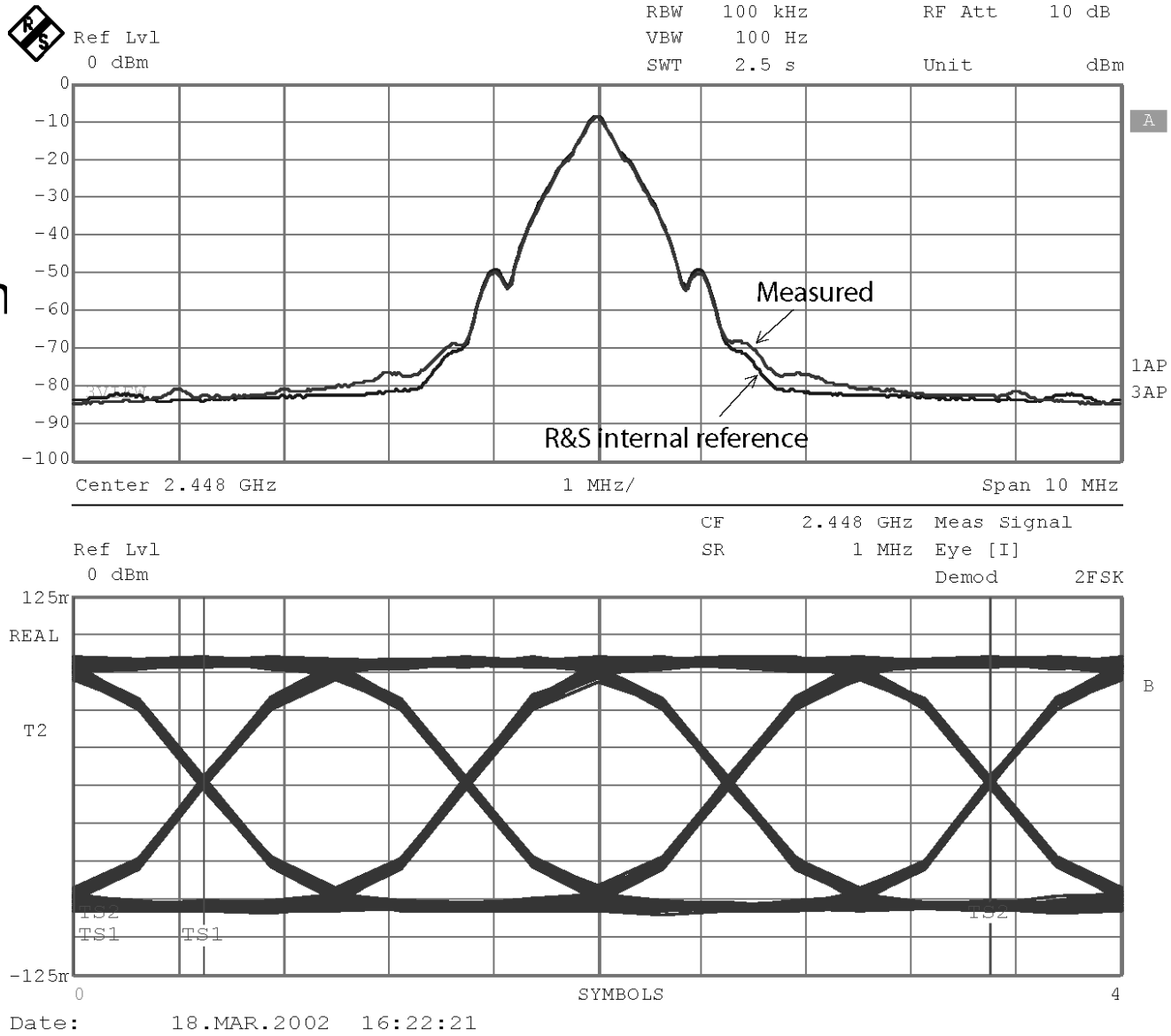
Close-In Phase Noise

- -86.2 dBc/Hz
  - 10 kHz offset
  - 2440 MHz carrier
  - 13 MHz FREF
- Adequate for GSM
  - 0.9 deg rms phase noise
  - Spec: 5 deg



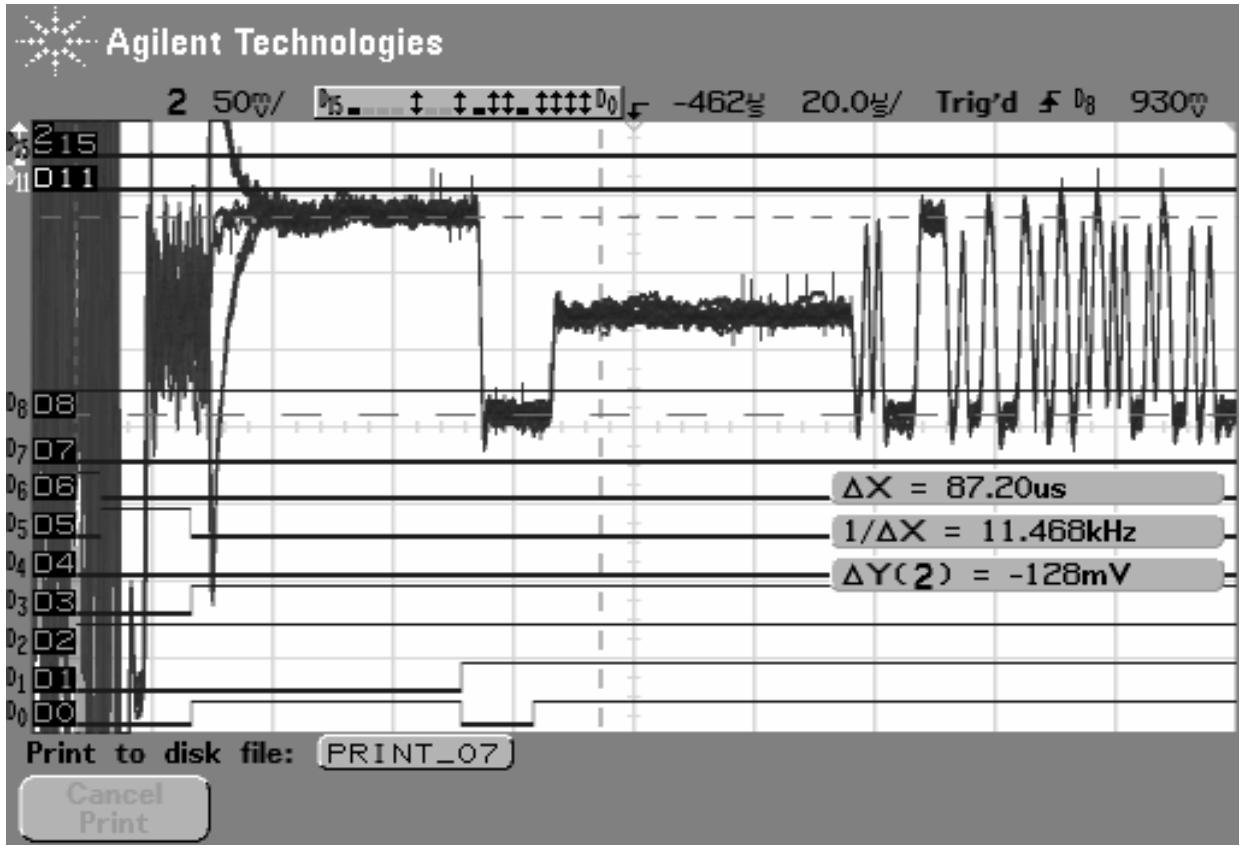
TX Modulation

- Wide modulation transfer function
  - 1 Mb/s
- Wide eye openings
- Narrow zero crossings



TX Output

- FM-demodulated TX signal at the 2.4 GHz RF port
- Bluetooth 1 Mbps pseudo-random data
- Fixed and correct DCO gain estimate
- 79 channels hopping



Performance Summary

- Passed the official Bluetooth qualification and is in production

Close-in phase noise	-86 dBc/Hz @ 10 kHz
Far-out spurs	< -80 dBc
Settling time	< 50 us
PA output power	2.5 dBm @ 50 ohm load
Current consumption	25 mA @ 1.5V

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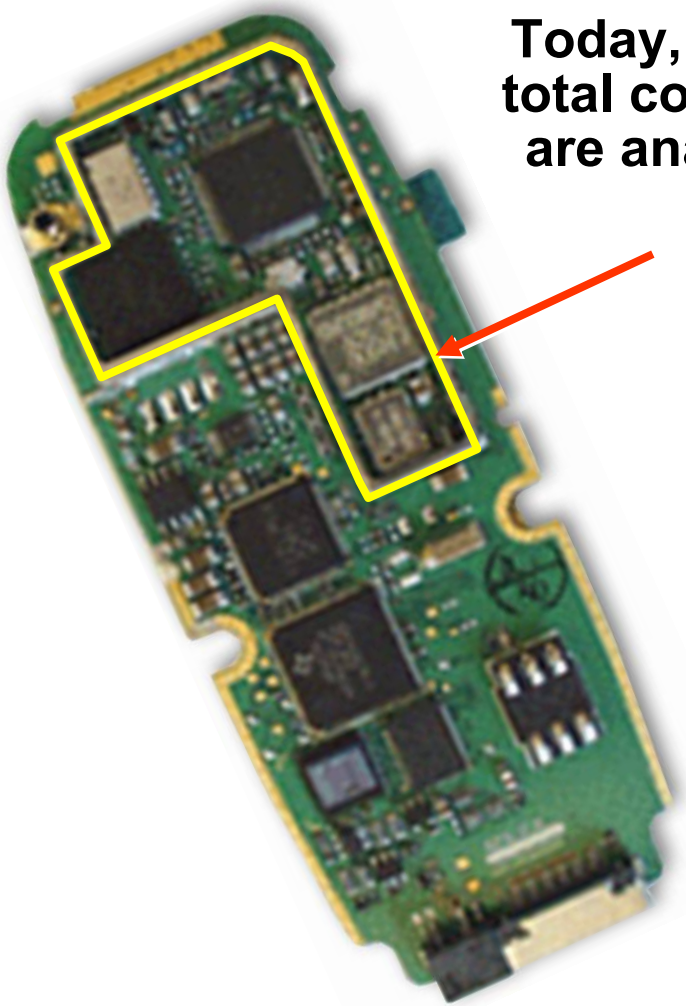
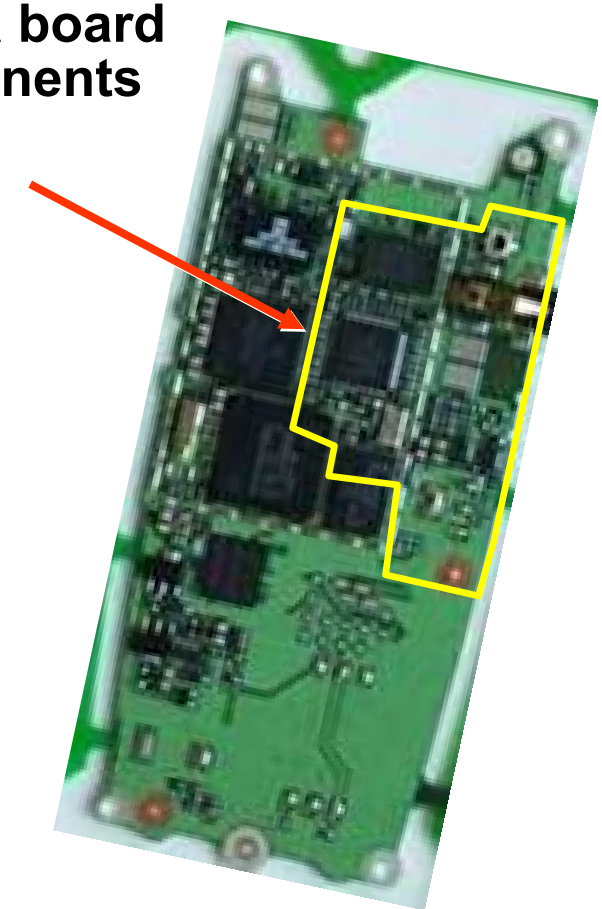
- **2003: Single-chip GSM transceiver**
- **2004: Single-chip commercial GSM radio**
- Conclusions

RF Transceivers Require Significant Board Area

Today, more than half of the total components on a board are analog RF components





Single-chip GSM Transceiver

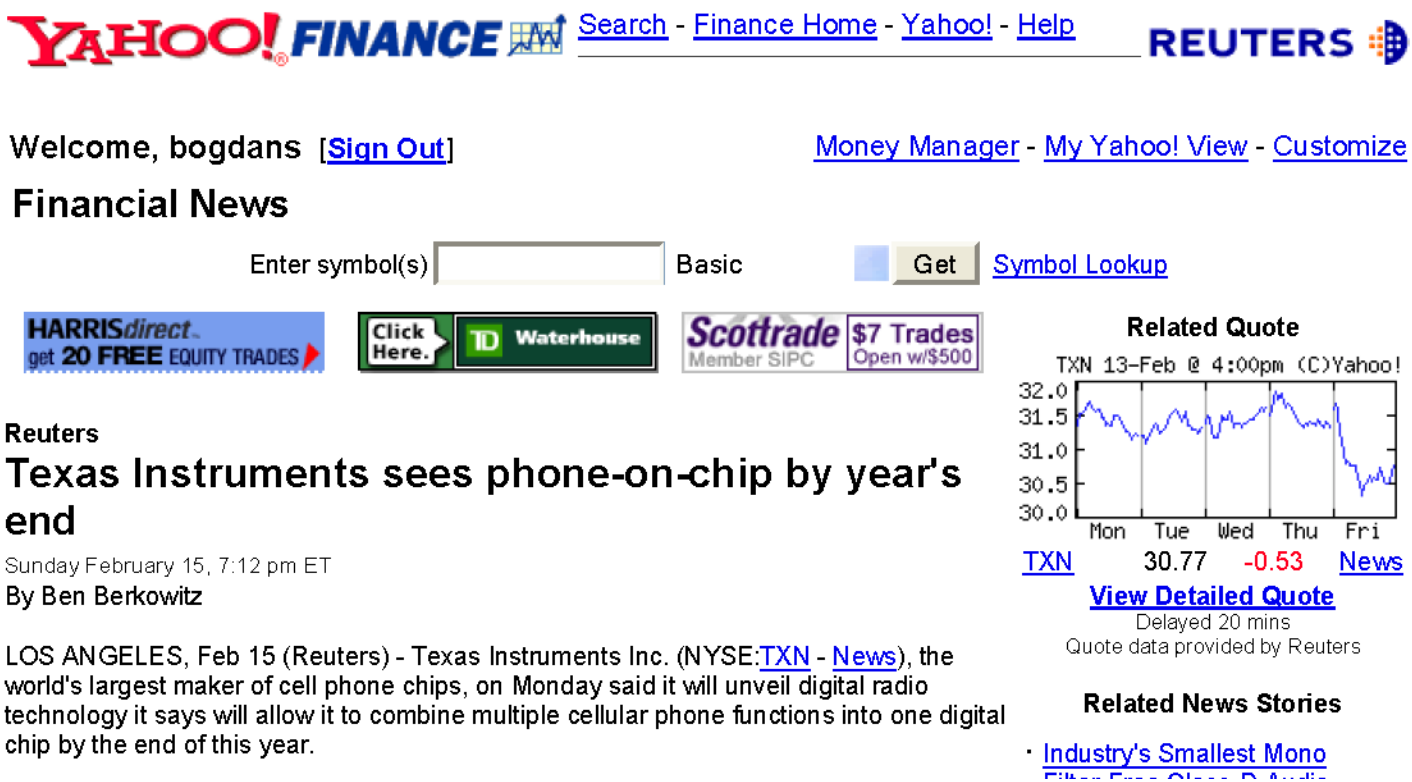
- First ever fully-integrated GSM transceiver in a deep submicron CMOS
  - C027 process (90 nm)
  - 150 Kgates / mm^2

- Jan 2004: Successful cellular phone call over the GSM public network in Nice, France

First GSM Single-Chip Radio

- Production-ready single-chip GSM expected by the end of 2004
  - Tom Engibous', former CEO, commitment to TI shareholders in 2002

Texas Instruments sees phone-on-chip by year's end http://biz.yahoo.com/rc/040215/media_texasinstruments_1.html



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Reuters

Texas Instruments sees phone-on-chip by year's end

Sunday February 15, 7:12 pm ET
By Ben Berkowitz

LOS ANGELES, Feb 15 (Reuters) - Texas Instruments Inc. (NYSE:TXN - News), the world's largest maker of cell phone chips, on Monday said it will unveil digital radio technology it says will allow it to combine multiple cellular phone functions into one digital chip by the end of this year.

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TXN 13-Feb @ 4:00pm (C)Yahoo!

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· Industry's Smallest Mono

Summary & Conclusions

- Digital Radio Processor (DRP)
- Focus on a multi-GHz RF frequency synthesizer and transmitter
- Showed a 5-year journey from DRP concept to a single-chip GSM radio
- Traditional RF circuits are difficult to design, manufacture, characterize and test
  - Require a truly unique set of skills
- All-digital architecture in a deep-submicron CMOS can replace traditional RF circuits
- Demonstrated in commercial single-chip Bluetooth and GSM radios

Thank you!

Questions?

Bogdan Staszewski

b-staszewski@ti.com