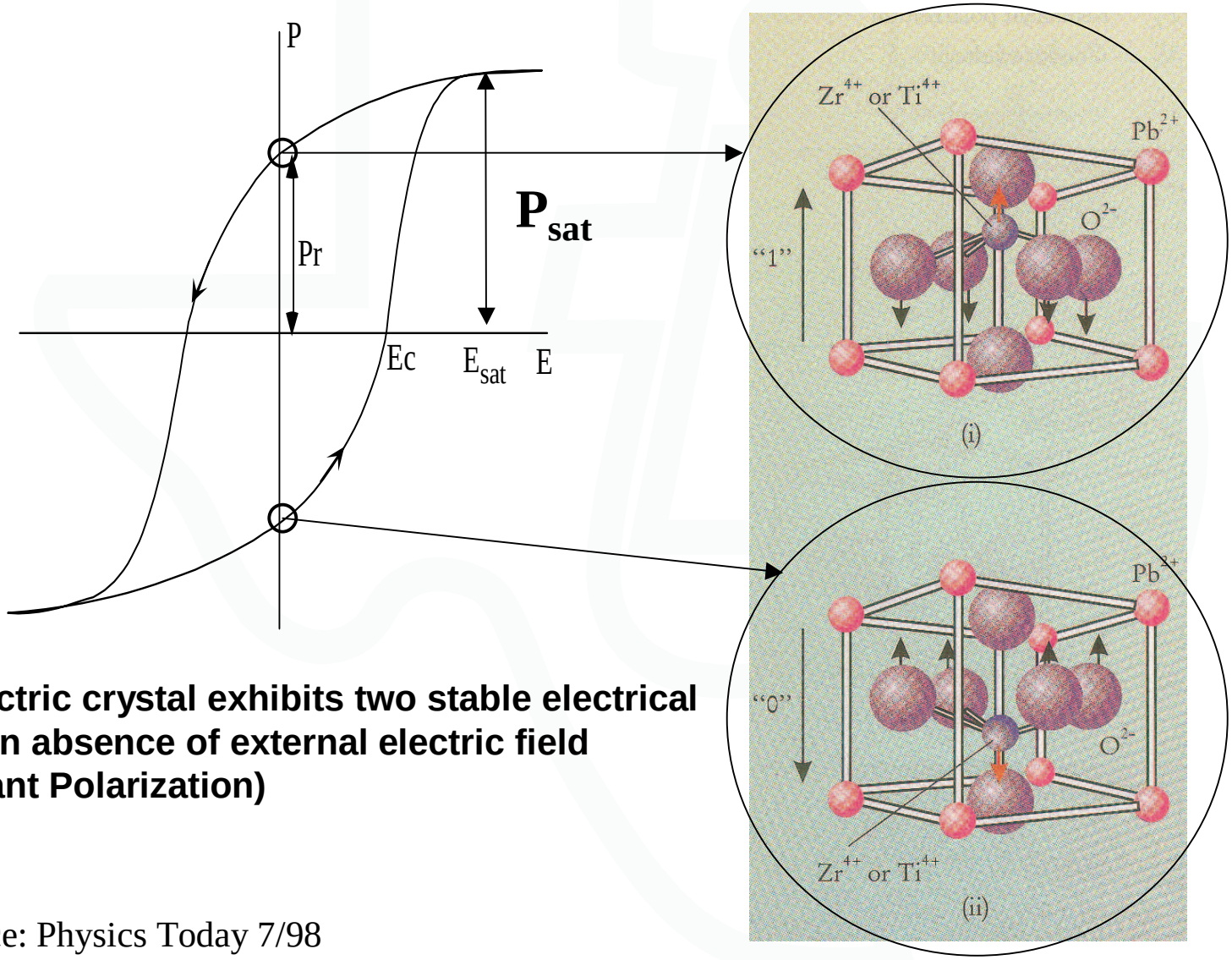
System Directions and Implications for Memory

- As systems go from MHz to GHz
  - Increasing processor performance requires greater instruction/data bandwidth
    - Greater internal bus widths
    - Smaller memory access time
  - Requires Embedded memory to keep from starving the processor
- Higher MHz increases power
  - Off-chip accesses have higher capacitance and voltage which increases memory power consumption
- Advanced CMOS technology nodes have leaky off-transistors
  - SRAM memories will consume more power from leakage than from access switching
  - Leakage reduction techniques degrade static noise margins and increase SER
  - SRAMs >16Mb are costly – Yield & Chip Area

Need for New Embedded Memory Technology

- Desired Characteristics
  - Compatible with logic process
    - As low mask adder as possible
    - Materials compatible with standard logic flow / thermal budget
  - Small cell size
  - Low power
    - Non-volatility desired for standby power reduction
    - Low voltage so no special/additional process steps required
  - Fast and near infinite number of read / write cycles
- Existing Technologies
  - eDRAM
    - Special process steps for capacitor / passgate, refresh current
  - Flash / EEPROM
    - Slow write, large added process cost, high voltages, limited write cycles
- New Technologies under development
  - Ferroelectric
  - Magnetic Tunnel Junction
  - Phase Change (Ovonics)

Ferroelectric Fundamentals

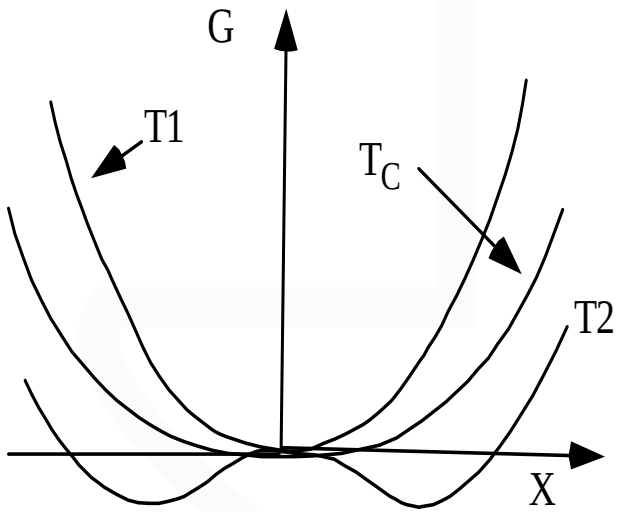


Ferroelectric crystal exhibits two stable electrical dipoles in absence of external electric field (Remanant Polarization)

Source: Physics Today 7/98

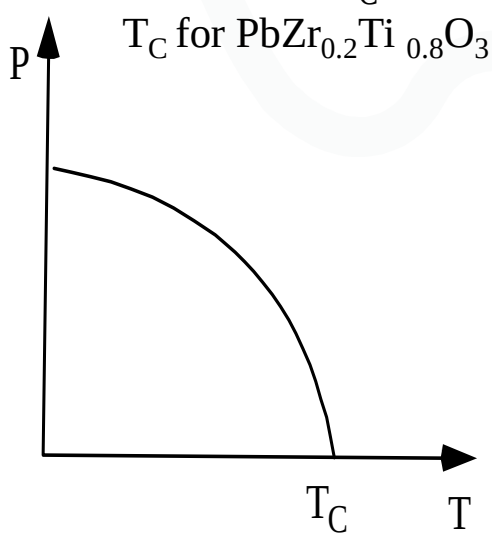
Fundamental Ferroelectricity

Gibbs Energy vs. Atomic Displacement

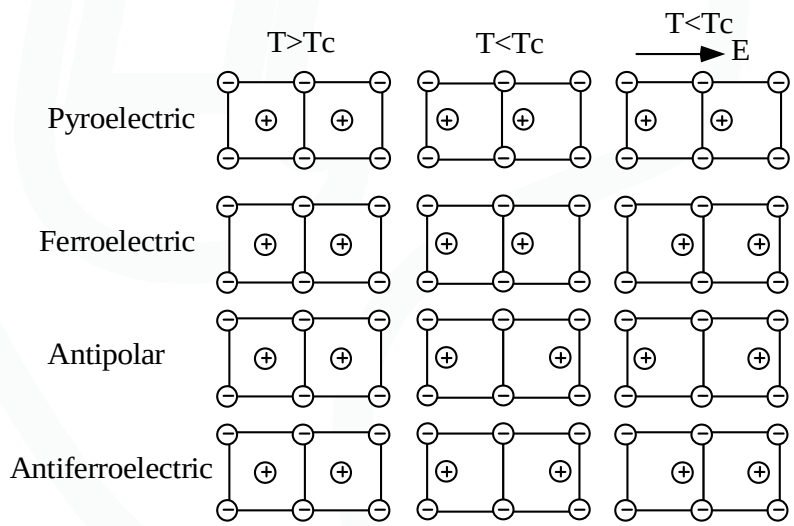


$T1 > T_C > T2$

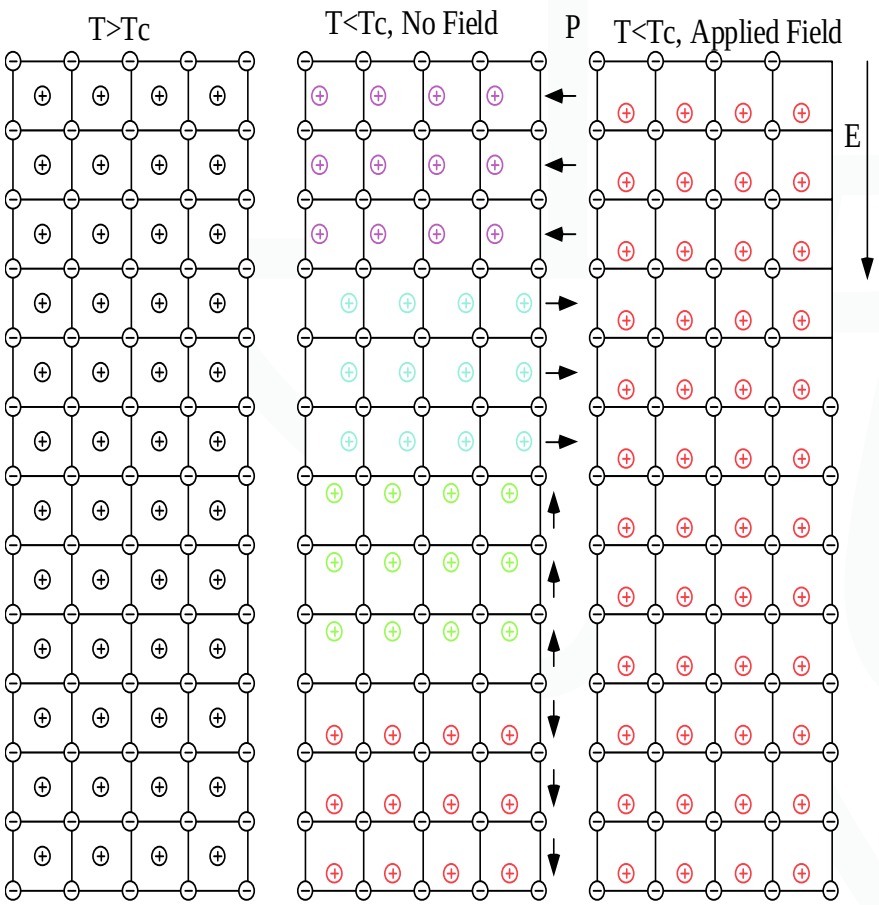
T_C for $PbZr_{0.2}Ti_{0.8}O_3$ ~ 470C



- **Plot of Energy versus Atomic Displacement**
  - **Displacive model.**
- **Plot of Polarization versus Temperature.**
  - **Second order phase transition.**
- **Possible Structural Phase Transition**

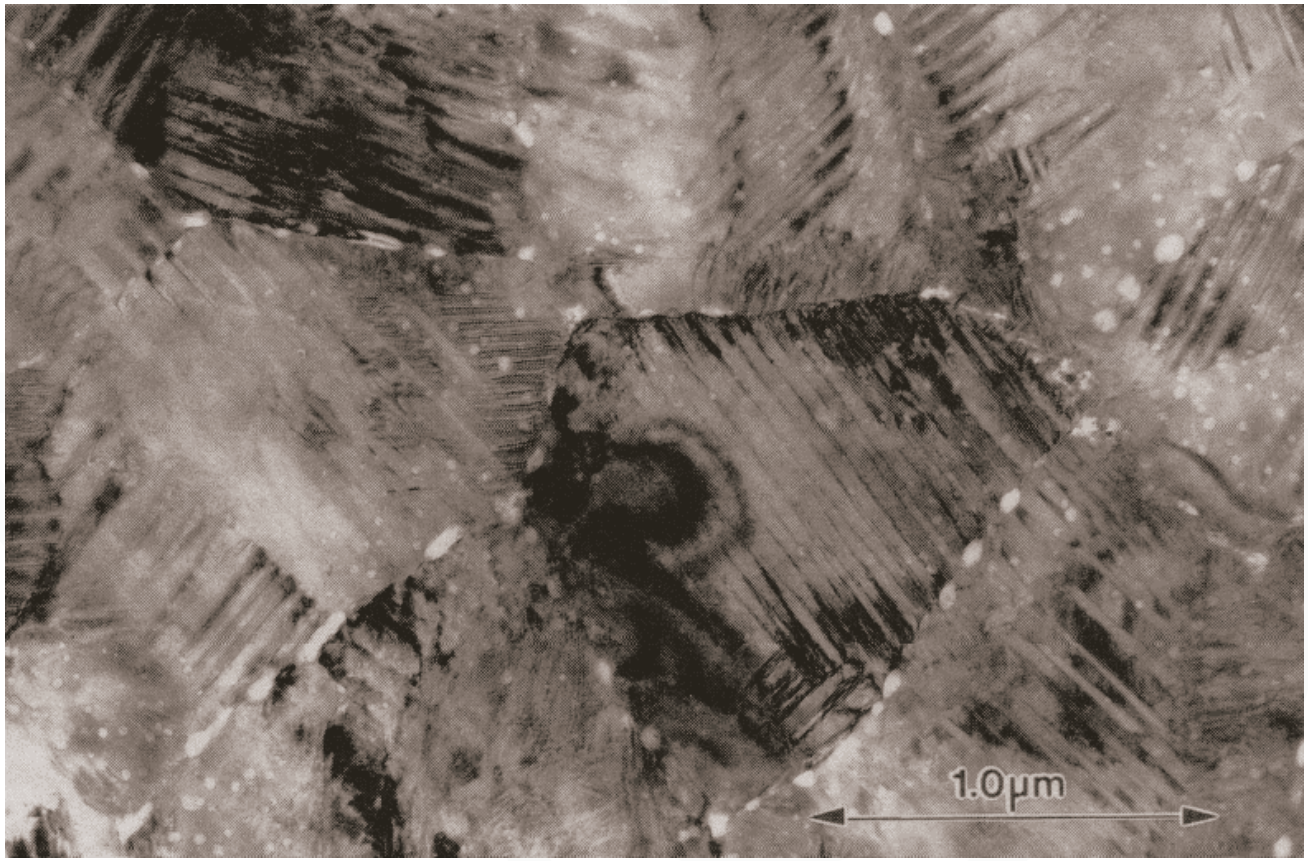


Ferroelectric Domains



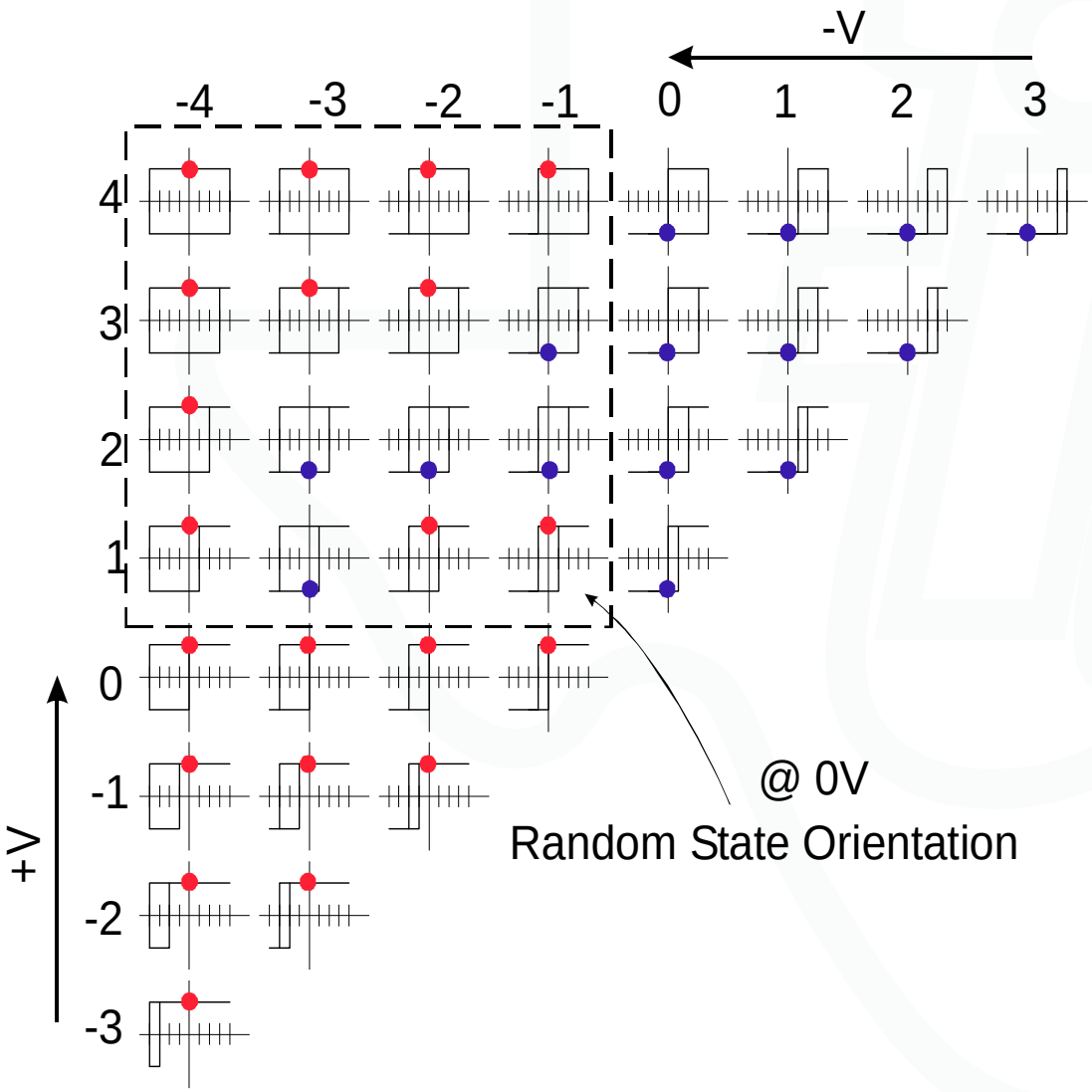
- Cubic material is not ferroelectric and has no domains. (T>Tc)
- Below Curie temperature (Tc) domains form.
  - Middle figure shows 4 different domains.
  - Domains only exist inside a grain.
  - Two 180 degree domain boundaries shown.
  - One 90 degree domain boundary shown.
- Domains nucleate and grow under electric field.

TEM of Domains

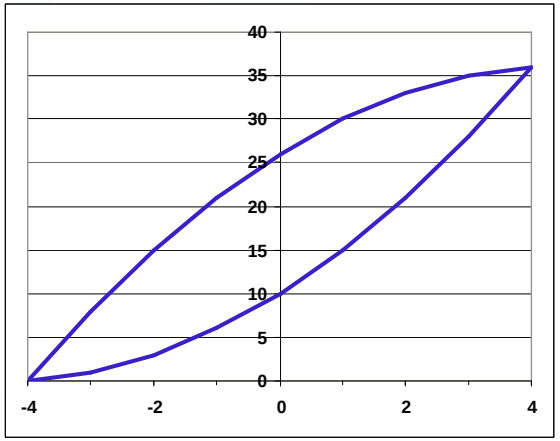


S. A. Myers and L. N. Chapin Mat. Res. Soc. Symp. Proc. **200,** p. 231 (1990).

Preisach Theory of Hysteresis

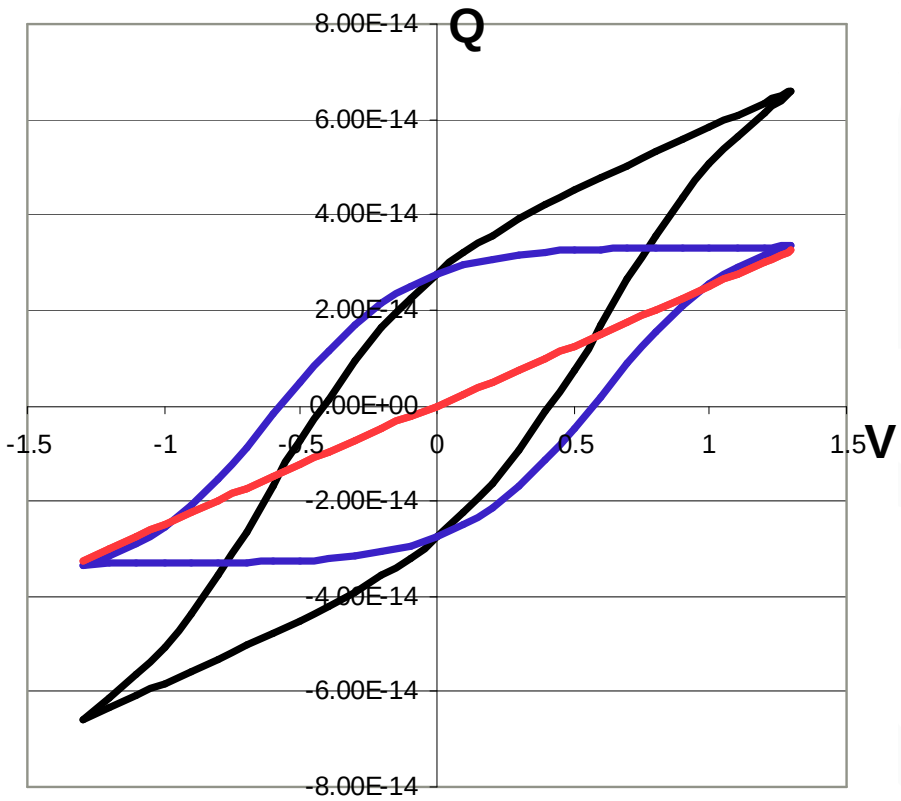


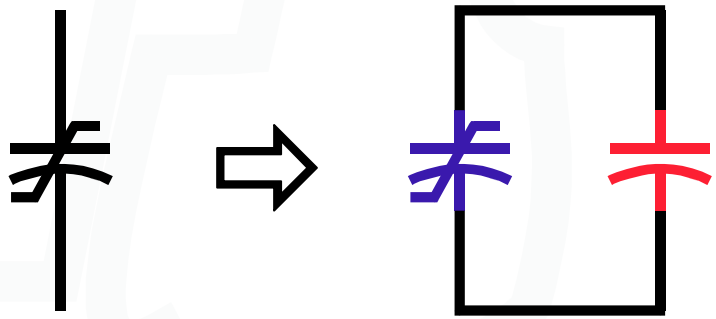
V	# Domains	# +Doms
-4	0	0
-3	1	1
-2	2	3
-1	3	6
0	4	10
1	5	15
2	6	21
3	7	28
4	8	36
3	-1	35
2	-2	33
1	-3	30
0	-4	26
-1	-5	21
-2	-6	15
-3	-7	8
-4	-8	0



Ferroelectric SPICE Model

$$Q = Area_{cap} * (Ps * \tanh (A * (V - Vc)) + C_lin * V)$$



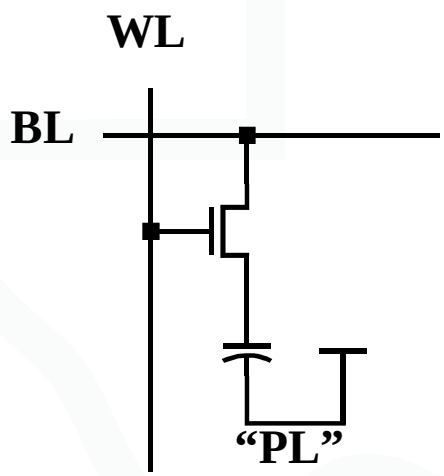


Ps = 15 μC/cm²
Vcp = 0.6 V
Vcn = -0.6 V
A = 2 V^{-1}
C_lin = 10 μF/cm²

$Area_{cap}$ = 0.25μm²

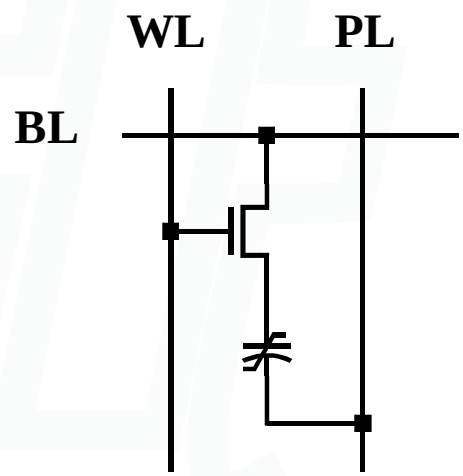
FRAM Comparison to DRAM

DRAM



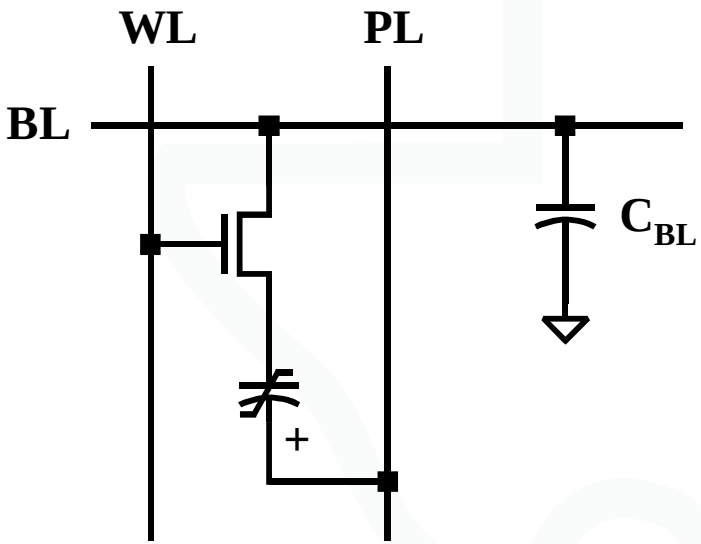
- State variable is charge across the plates of the capacitor (q=cv)
- "Plate" terminal of capacitor is a DC voltage
- Read is destructive – state must be restored
- Requires reference voltage and sense amplifier for state detection

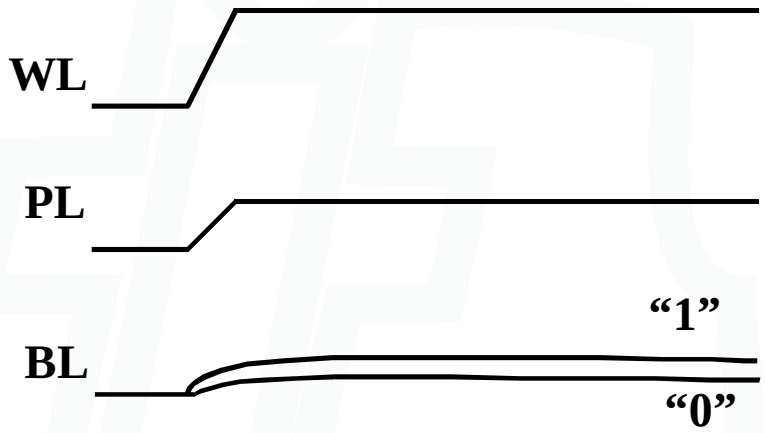
FRAM

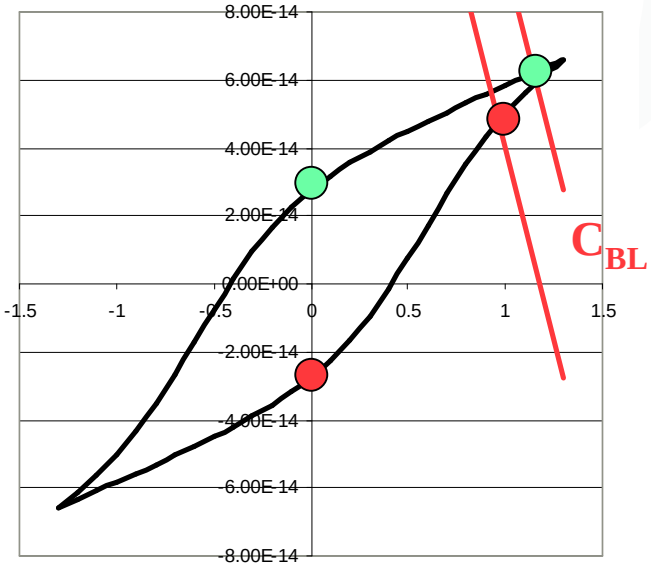


- State variable is direction of polarization in the dielectric material
- "Plate" terminal of capacitor is switched
- Read is destructive – state must be restored
- Requires reference voltage and sense amplifier for state detection

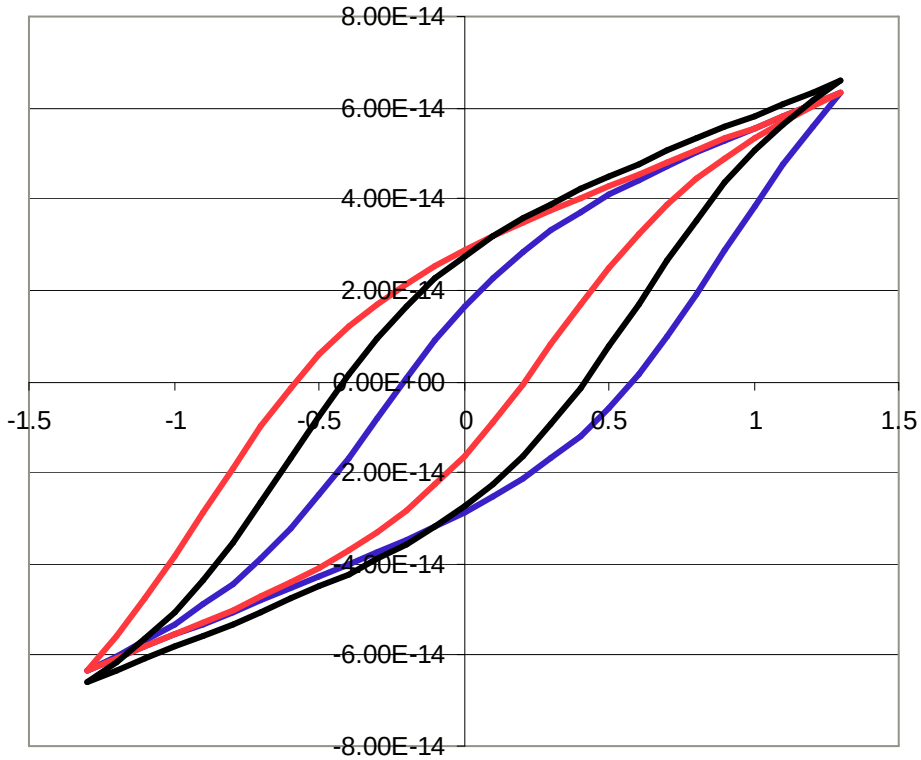
How is FRAM Cell Read?





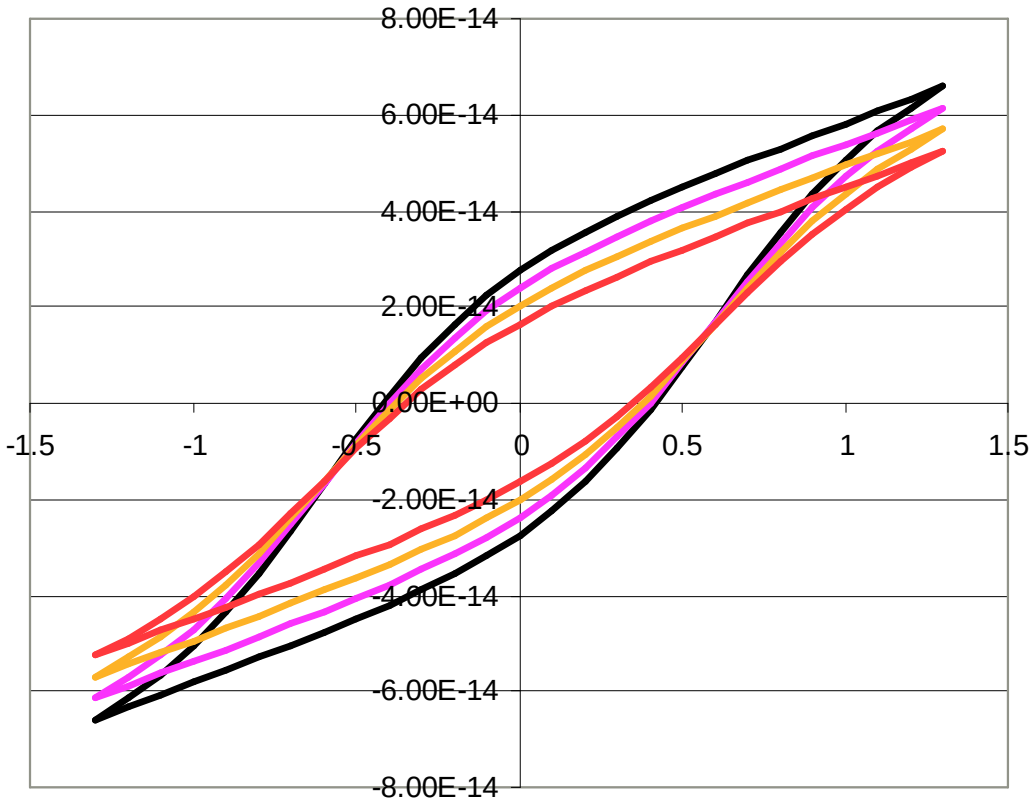


Ferroelectric Reliability Issues - Imprint



- **Voltage shift in hysterisis curve**
- **Device Degradation:**
  - **Loss of switched charge**
- **Theoretical Mechanism**
  - **Motion of charged defects**

Ferroelectric Reliability Issues - Fatigue



- **Endurance**
  - **Loss in switched polarization**
- **Theoretical Mechanism**
  - **(Sandia Model)**
  - **Point defects diffuse creating large concentrations near electrode interfaces**
  - **Injection of electrons from electrodes converts point defects to charged state**
  - **Domains are pinned by large concentration of charged point defects**

A 64Mbit Embedded FeRAM Utilizing a 130nm, 5LM Cu/FSG Logic Process

H. McAdams, R. Acklin, T. Blake, J. Fong, D. Liu, S. Madan, T. Moise, S. Natarajan, N. Qian, Y. Qui, J. Roscher, A. Seshadri, S. Summerfelt

Texas Instruments, 13560 N. Central Expy, MS-3737, Dallas, TX 75243

X. Du, J. Eliason, W. Kraus

Ramtron International Corporation, 1850 Ramtron Drive, Colorado Springs, CO 80921

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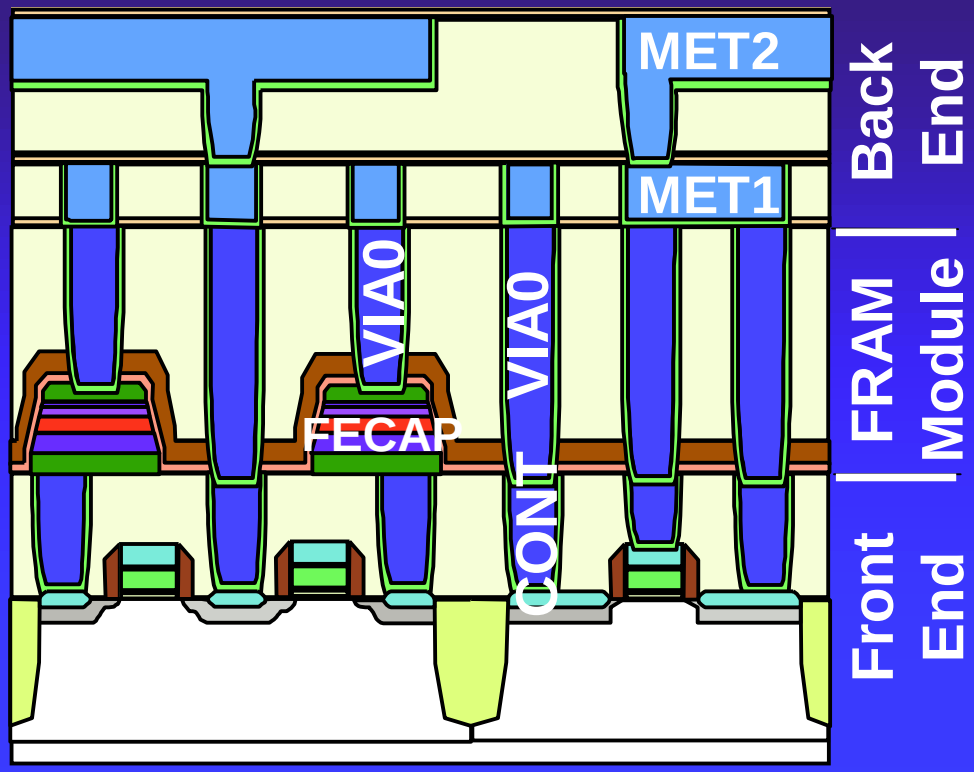
Agilent Technologies, 5301 Stevens Creek Blvd, Santa Clara, CA 95051

Embedded Ferroelectric Memory (eFRAM) Requirements

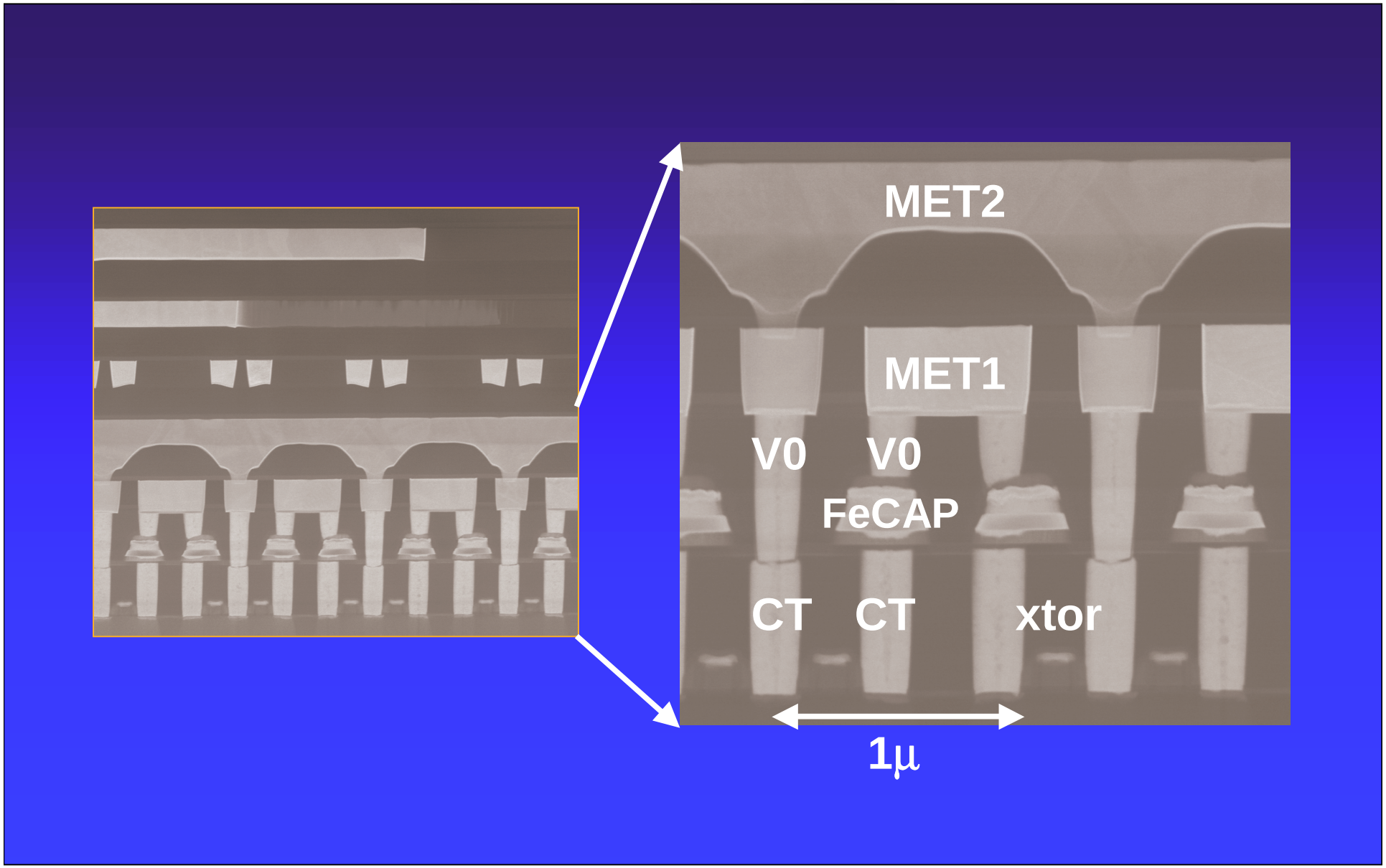
- **Must operate at voltages compatible with low voltage logic**
- **Memory must be reliable**
  - **Endurance (>1E14), Retention (>10yrs)**
- **High density is required**
  - **Must be >SRAM and competitive to commodity memory solutions**
- **Must easily integrate into logic process**
  - **Minimum mask adder, no logic degradation**
  - **Use same base logic libraries**

eFRAM Process Module



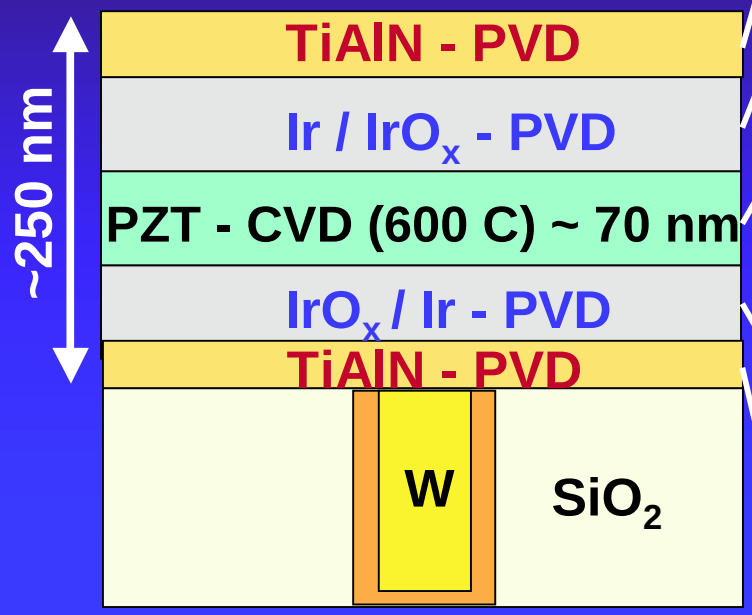
- Single memory & logic transistor oxide
- 2 added masks
  - FECAP – single mask stack-etch capacitor formation
  - VIA0 – top electrode & CONT feed-thru
- Standard front & back end logic processing

130nm eFRAM Cross-Section



Ferroelectric Capacitor Stack

Layer Structure



Hardmask
- High selectivity relative to Ir

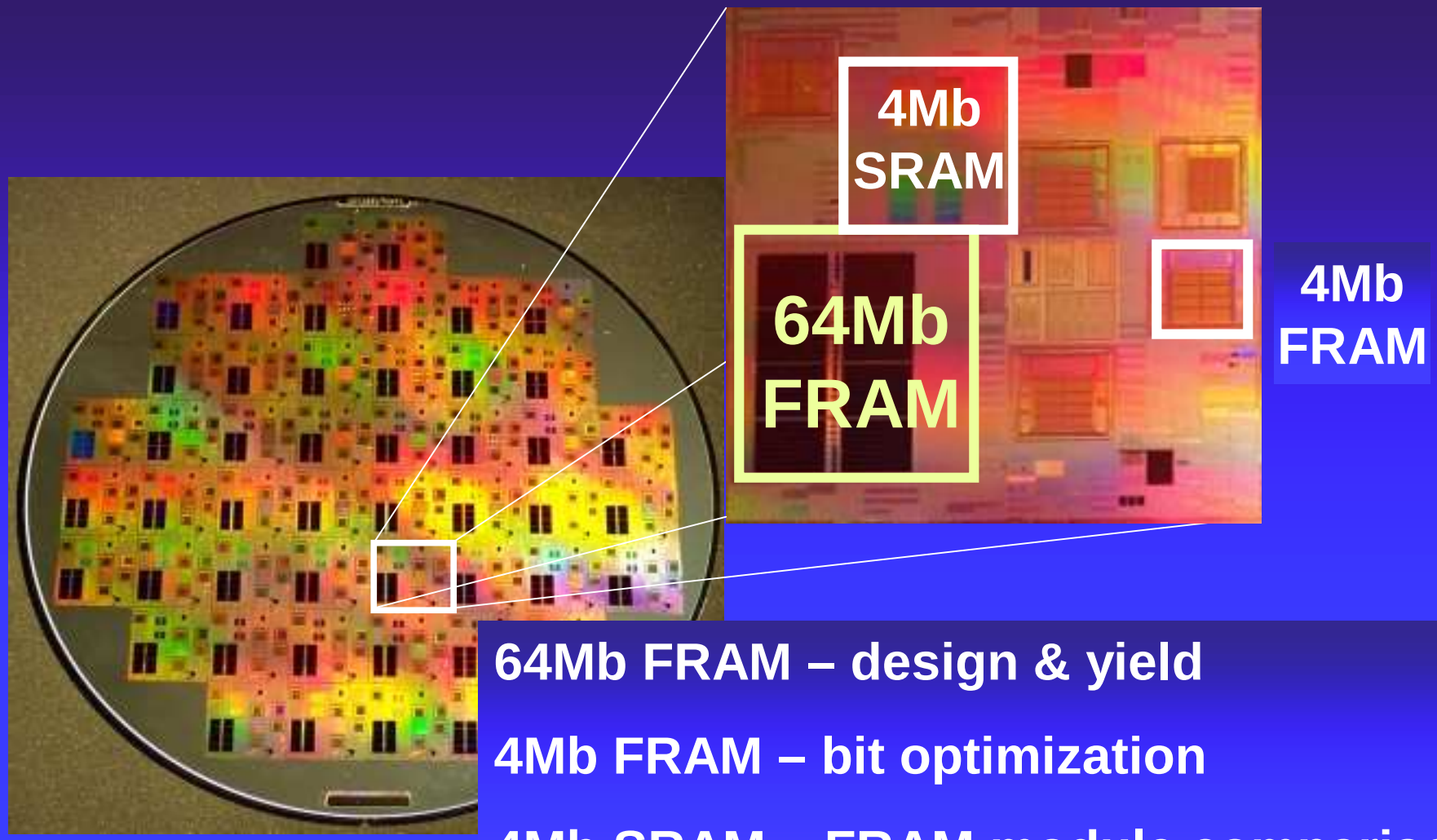
Top Electrode
- Oxidized to maximize endurance

Ferroelectric - $Pb(Zr_{0.25}Ti_{0.75})O_3$
- Large polarization
- Low coercive field
- Low formation temperature
- Small grain size

Bottom Electrode
- Conductive after PZT dep.
- Diffusion barrier

Conductive Diffusion Barrier
- Adhesion
- Low oxidation rate

eFRAM Test Chip

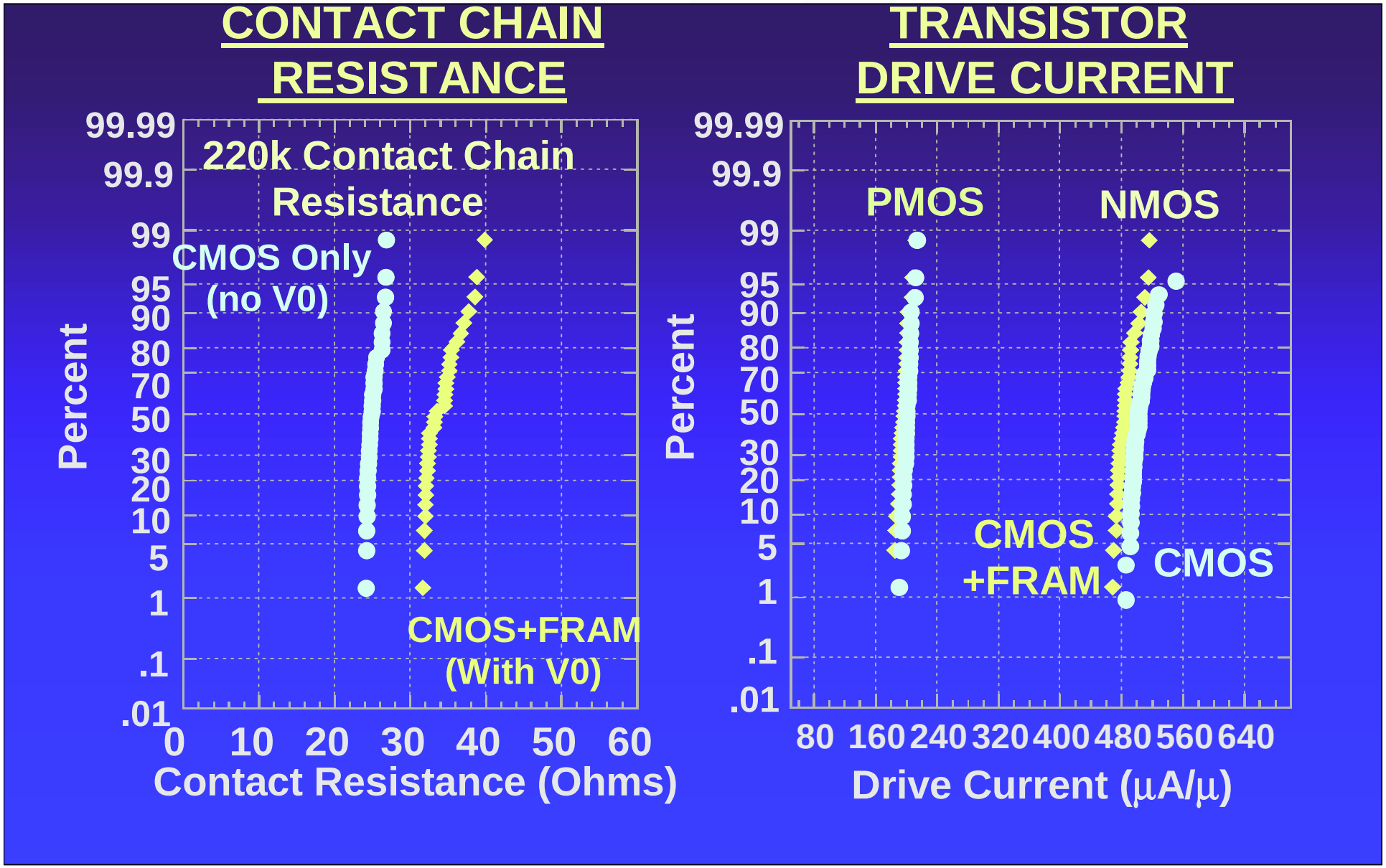


64Mb FRAM – design & yield

4Mb FRAM – bit optimization

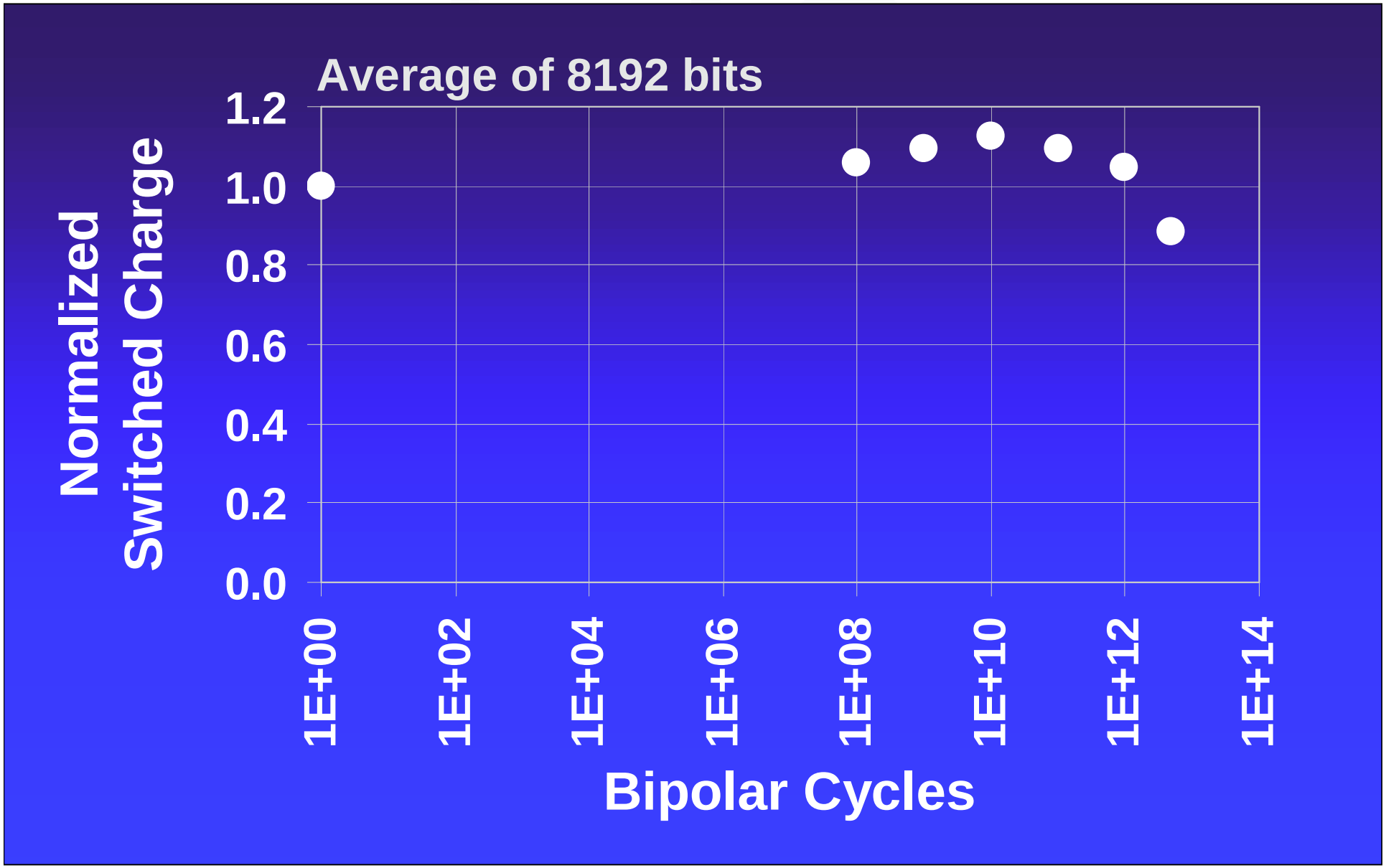
4Mb SRAM – FRAM module comparison

eFRAM Integration Impact on CMOS



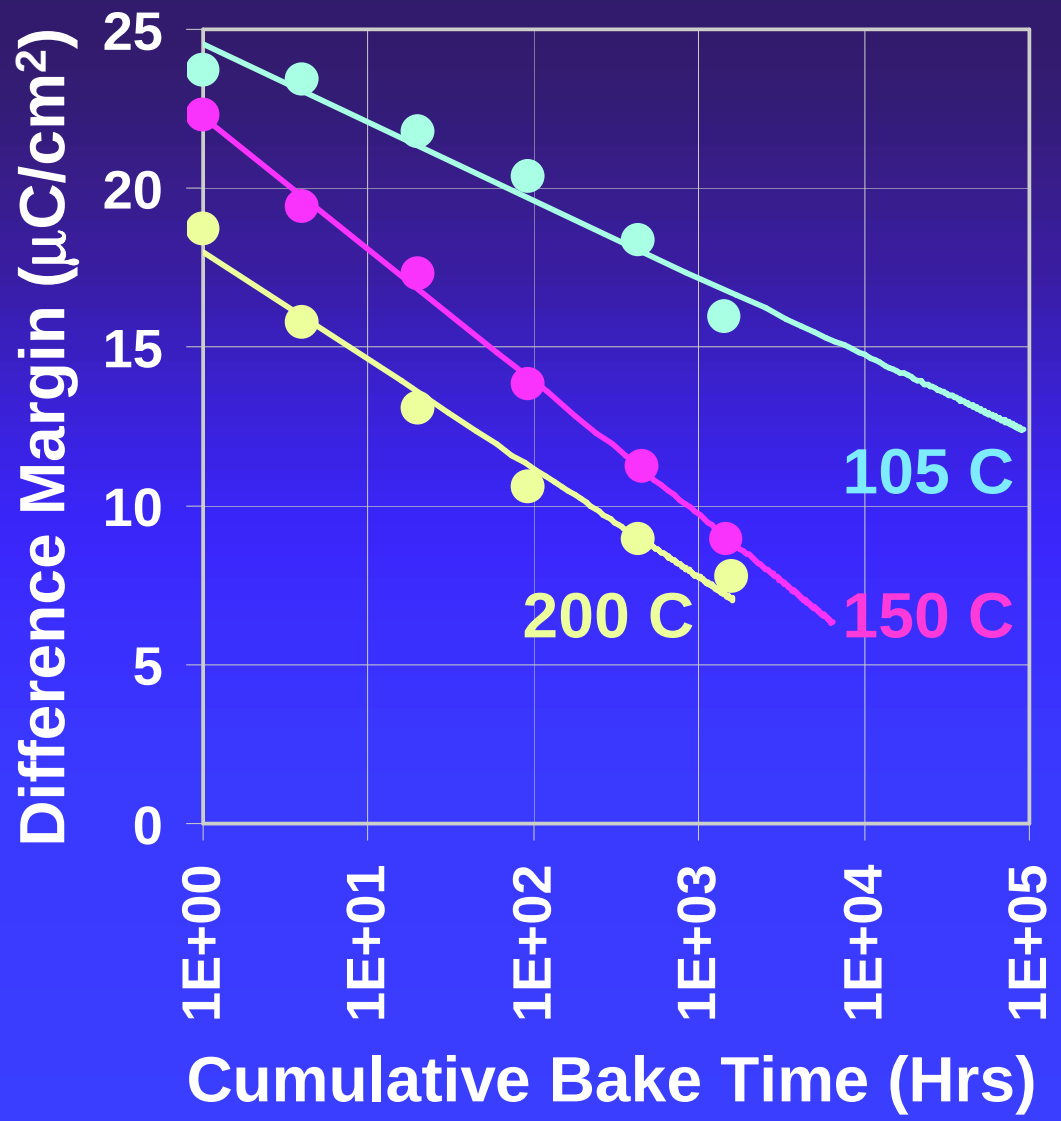
Endurance

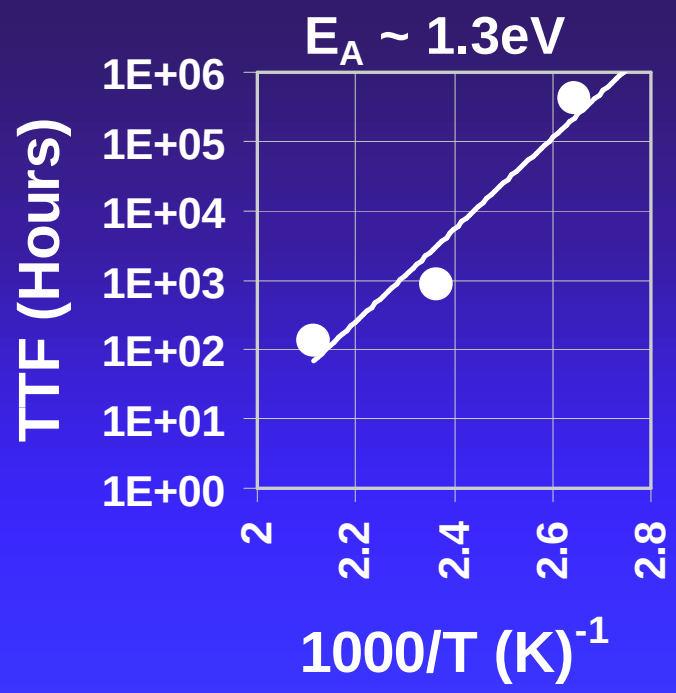
(Measured on 4Mb FRAM circuit)



Retention

(Measured on stand-alone capacitors)

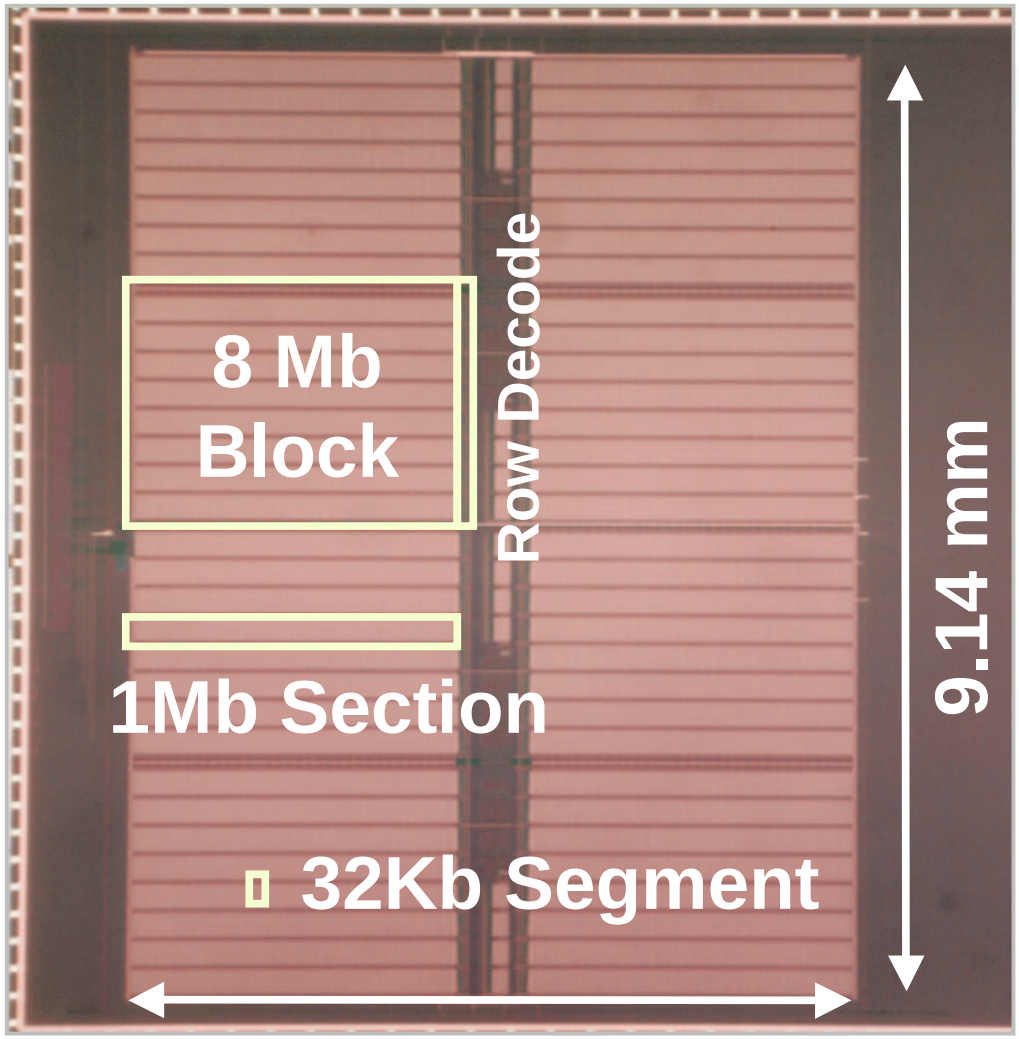




- 100mV S/A offset + reference noise -> ~10μC/cm² diff. margin

64Mb Test Chip

Device Features

64Mb Macro Size	56.5 mm^2
Memory Density	1.13 Mb / mm^2
Array Efficiency	64%
Cell Size	0.54 μ^2
Capacitor Size	0.25 μ^2
Cell Type	1T1C, CUB
Architecture	Folded, Twisted BL
Access/Cycle Time	30 ns / 35 ns
Operating Voltage	1.3 V

64Mb Die Photo