Chameleon: A Dual-Mode Bluetooth/WiFi Receiver Design

IEEE CAS Society
Chapter at Dallas, Texas

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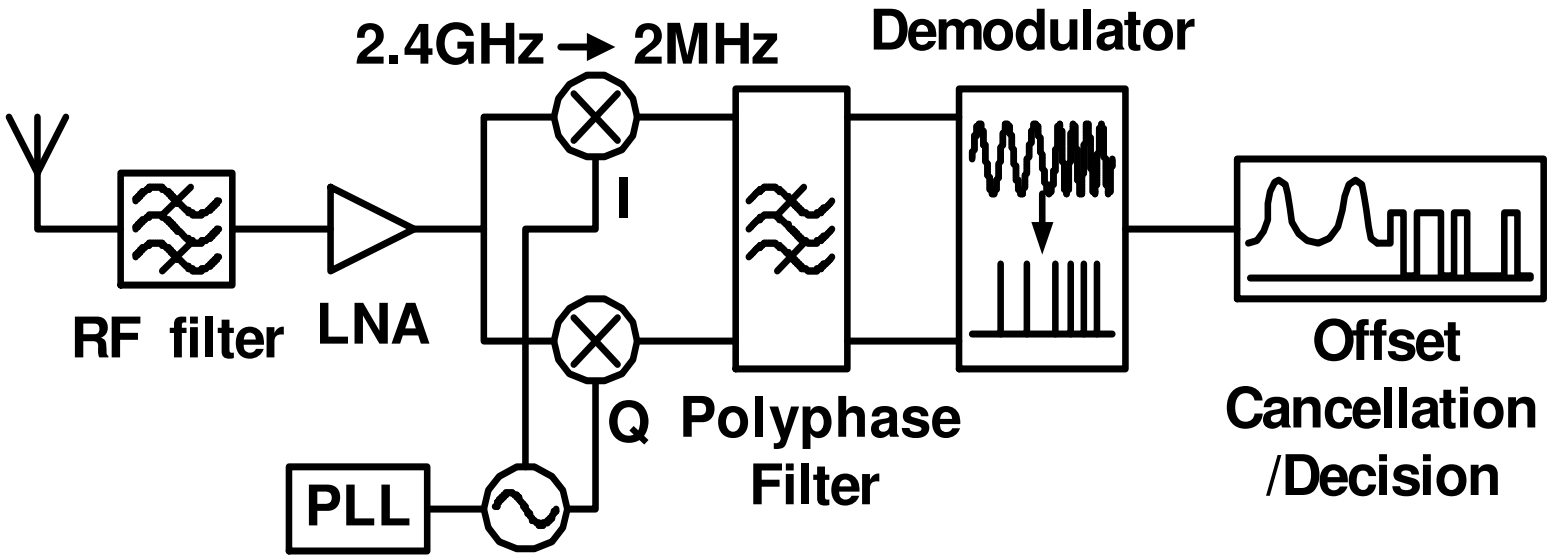
Texas A&M University

Outline

- Previous work: Bluetooth Receiver in CMOS 0.35μm
- System Level Design
  - Technology features
  - Main Bluetooth and Wi-Fi specs
  - Previously reported architectures
  - Proposed dual-mode architecture
  - Impact of non-idealities on the BER performance
- Building Blocks
  - LNA
  - Mixer
  - VCO and PLL
  - VGA
  - ADC
- Experimental Results

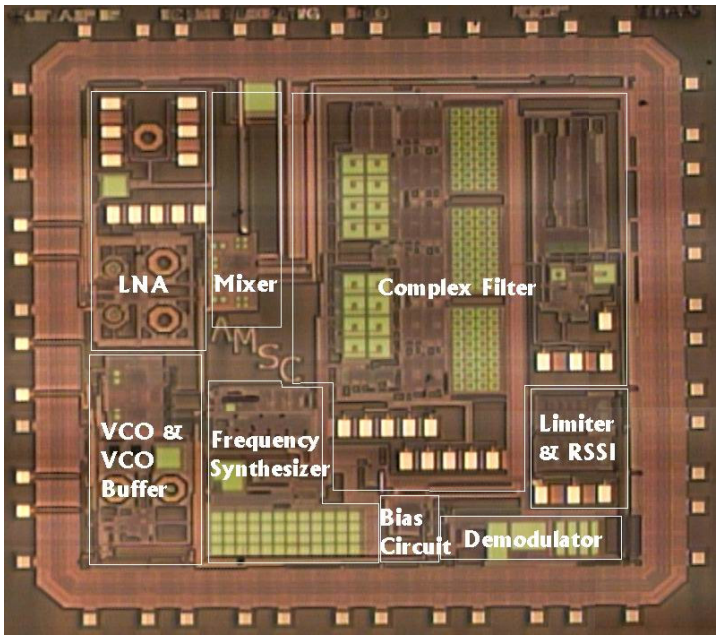
0.35μm CMOS Bluetooth Low-IF Receiver IC

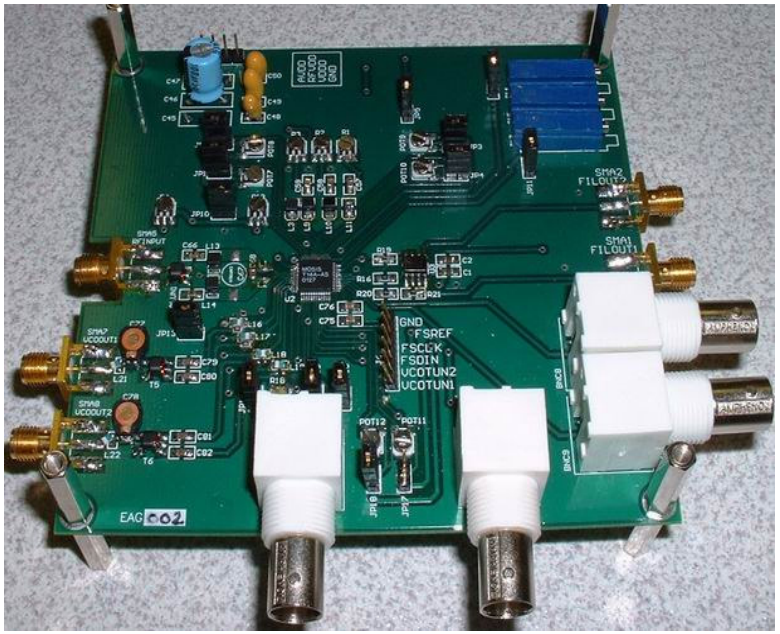


Developed during 2001 and 2002 at the AMSC.

Authors: Wenjun Sheng, Bo Xia,Ahmed Emira, Chunyu Xin, Ari Ari Valero-Lopez, Sung Tae Moon and Edgar Sanchez-Sinencio.

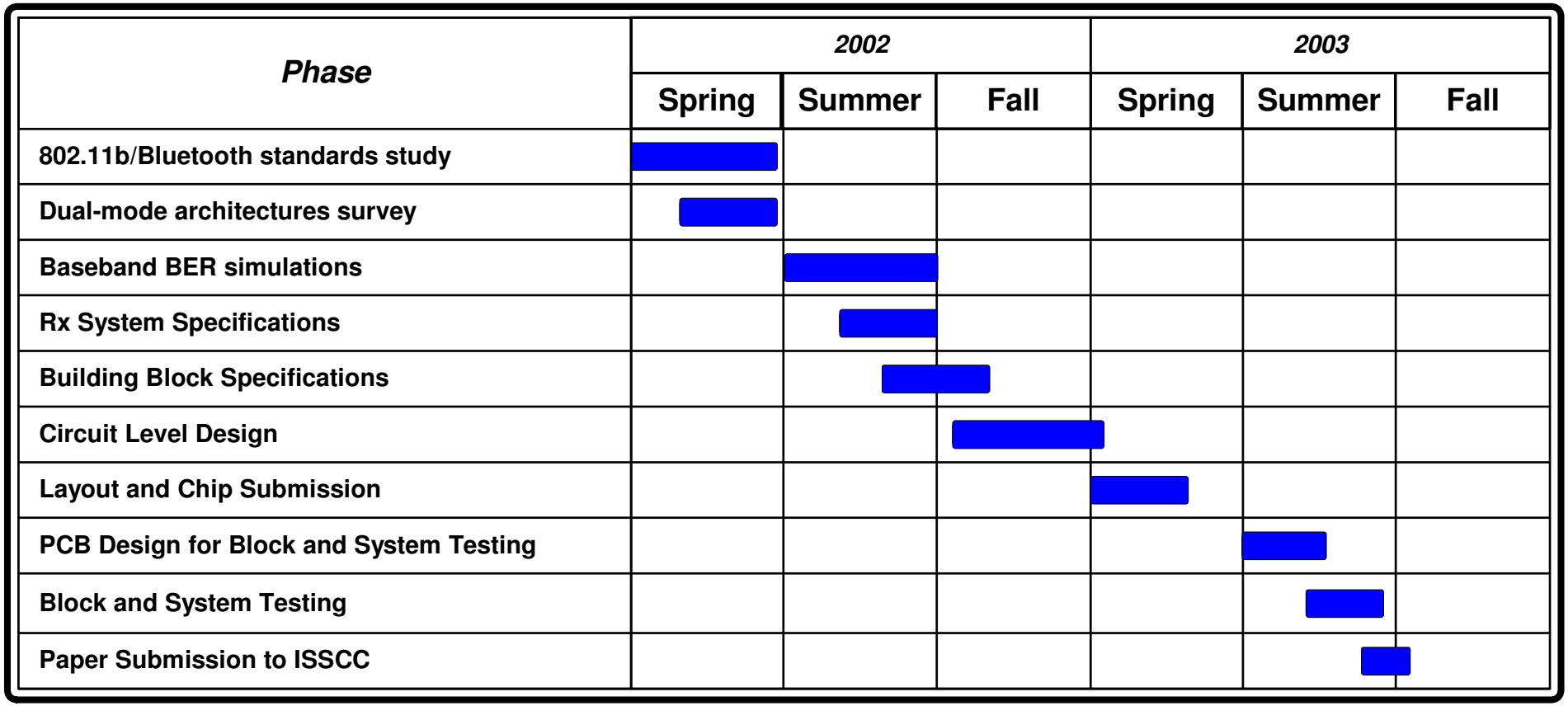
0.35μm CMOS Bluetooth Low-IF Receiver IC





- Publications:
  - 2002 RFIC Conference, Best Student Paper Award (third place).
  - Journal of Solid-State Circuits: January 2003 (Receiver) and August 2003 (Demodulator).
  - Transactions on Circuits and Systems – II: November 2003 (Complex Filter).

Chameleon Receiver: Timeline



Chameleon Receiver

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  - Technology features
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Technology features

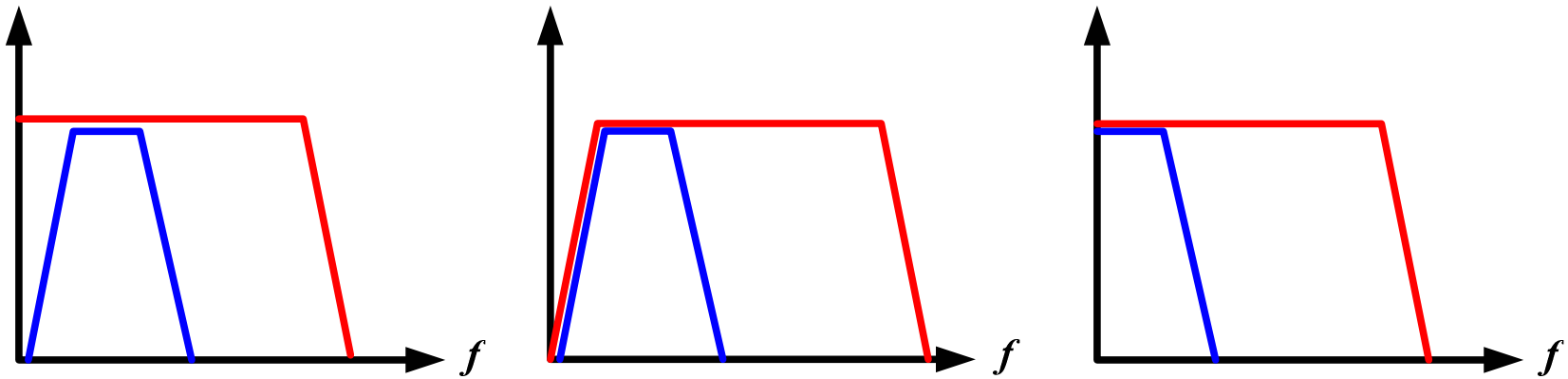
- IBM SiGe BiCMOS 6HP 0.25um
- Transit frequency (f_T) 47GHz
- 6 aluminum metal layers
- Analog metal (4um thick, 0.00725 Ω/□)
- Varactor diode (intrinsic base-collector diode)
- Metal to metal cap (1.4fF/um^2)
- MOS cap (3.1±15%fF/um^2)
- Poly resistors (210±20%, 3600±25% Ω□)

Standards Overview

	Bluetooth	802.11b
Data rate	1Mb/s	1-11Mb/s
Power	Lower	**Higher**
Modulation	FH-GFSK	DSSS-CCK
Freq band	2.4 – 2.48GHz	2.4 – 2.48GHz

Dual-Mode Receiver Architecture

- 3 possible alternatives for Bluetooth and Wi-Fi dual mode architectures:



Low-IF and DCR

Best fit for each standard ☺
Sharing ↓ ☹

Low-IF and Low-IF

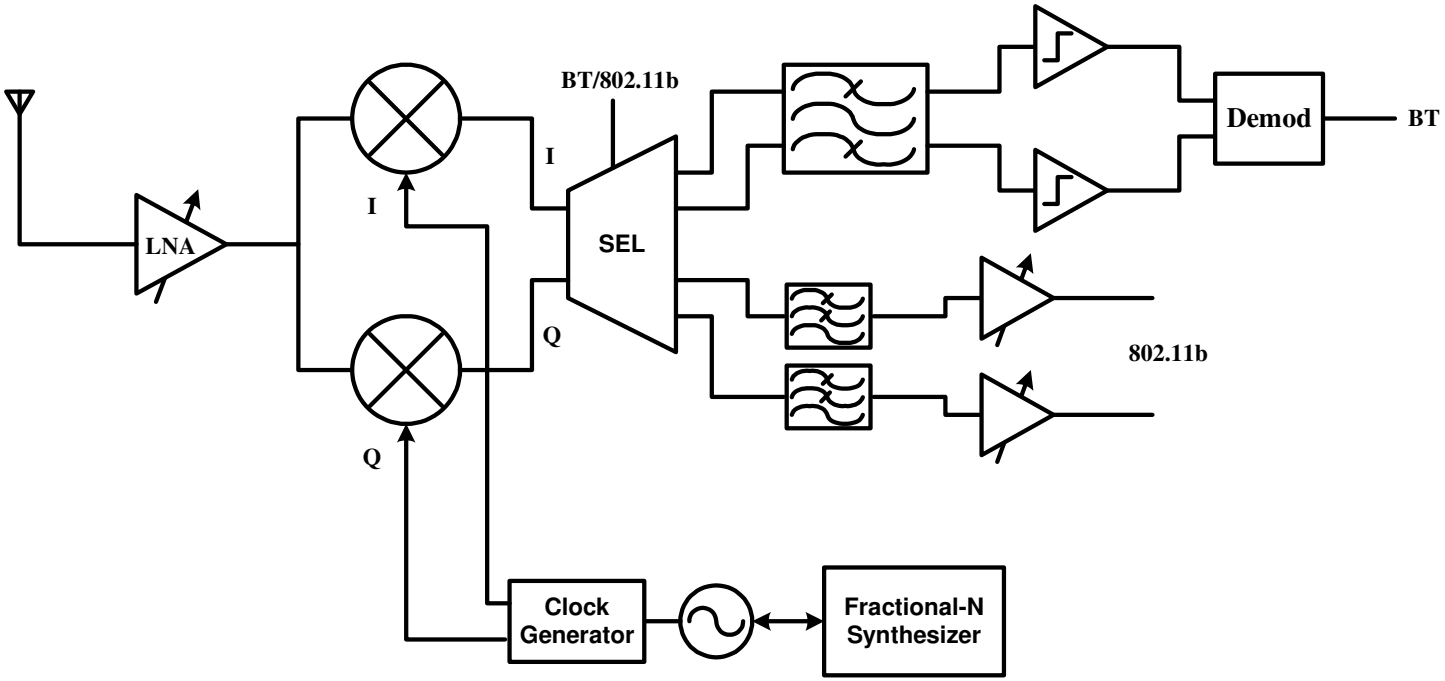
Power ↑ ☹ ☹
Sharing ↓ ☹

DCR and DCR

Area and power ↓ ☺
Sharing ↑ ☺
DC offset & 1/f noise ↑ ☹

Previously Reported Dual-Mode Receivers

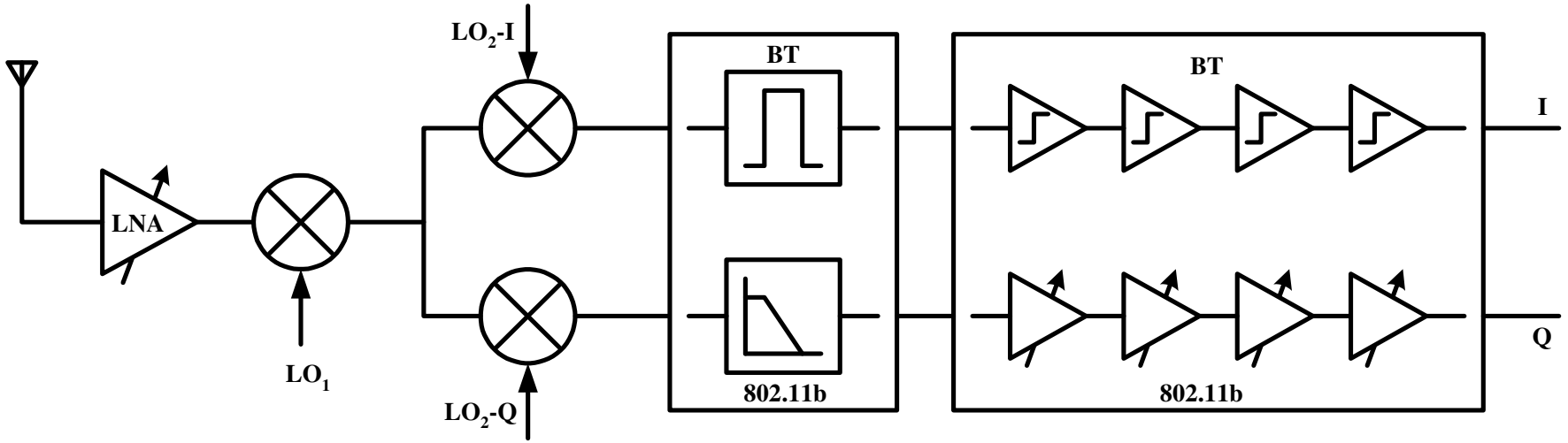
- DCR for WiFi, low-IF for Bluetooth.
- Shared RF front-end.
- Separate baseband circuits



[1] J. C. H. Darabi, et al "A Dual Mode 802.11b/Bluetooth Radio in 0.35mm CMOS," ISSCC 2003, San Francisco, CA.

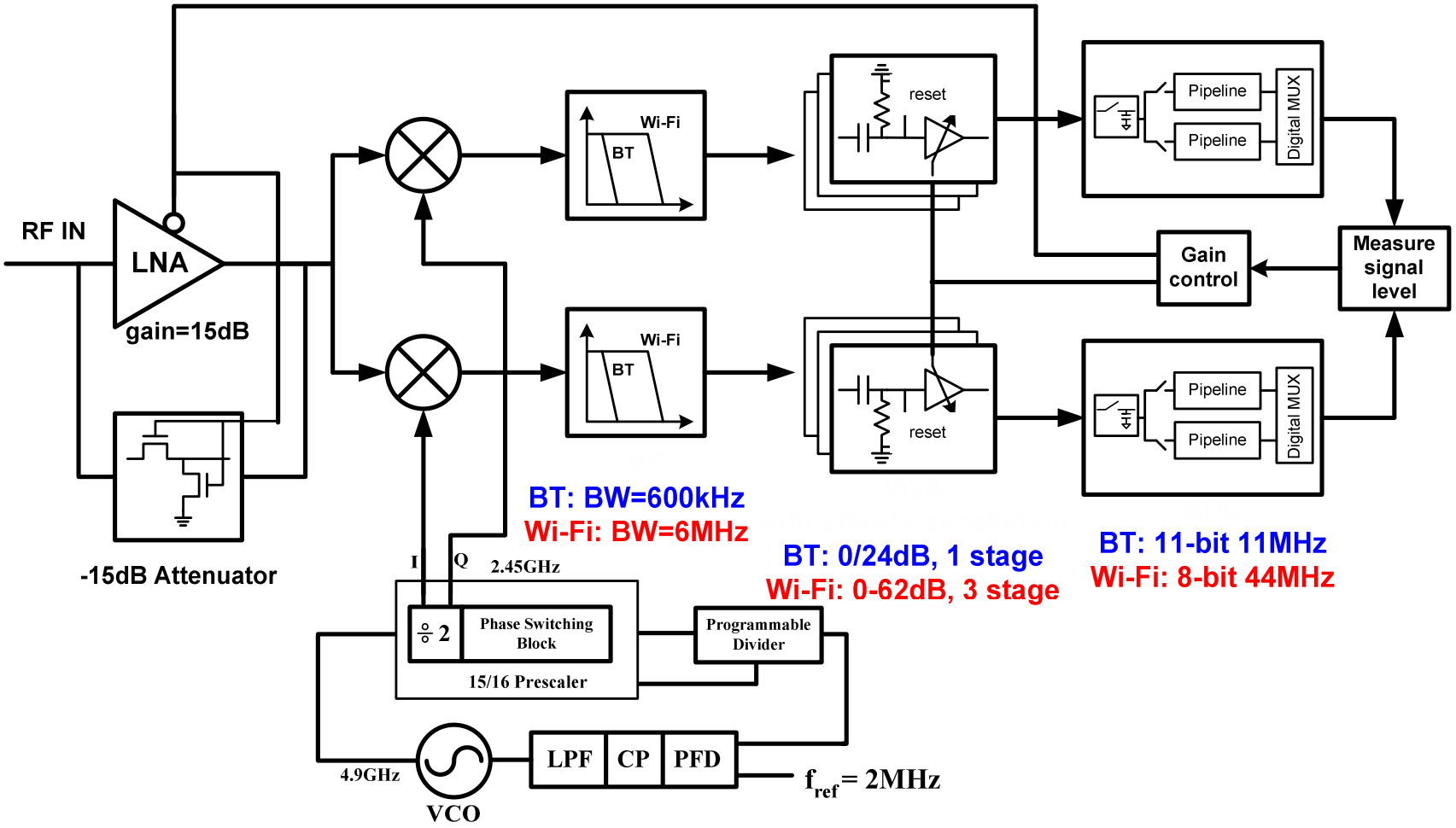
Previously Reported Dual-Mode Receivers

- Double downconversion to avoid LO self mixing and injection locking between PA and VCO.
- DCR for Wi-Fi and low-IF for Bluetooth.
- Shared RF and programmable dual-mode baseband.



[2] D. K. T. Cho, et al "A 2.4Ghz Dual-Mode 0.18mm CMOS Transceiver for Bluetooth and 802.11b," ISSCC 2003, San Francisco, CA.

Proposed Dual-Mode Architecture

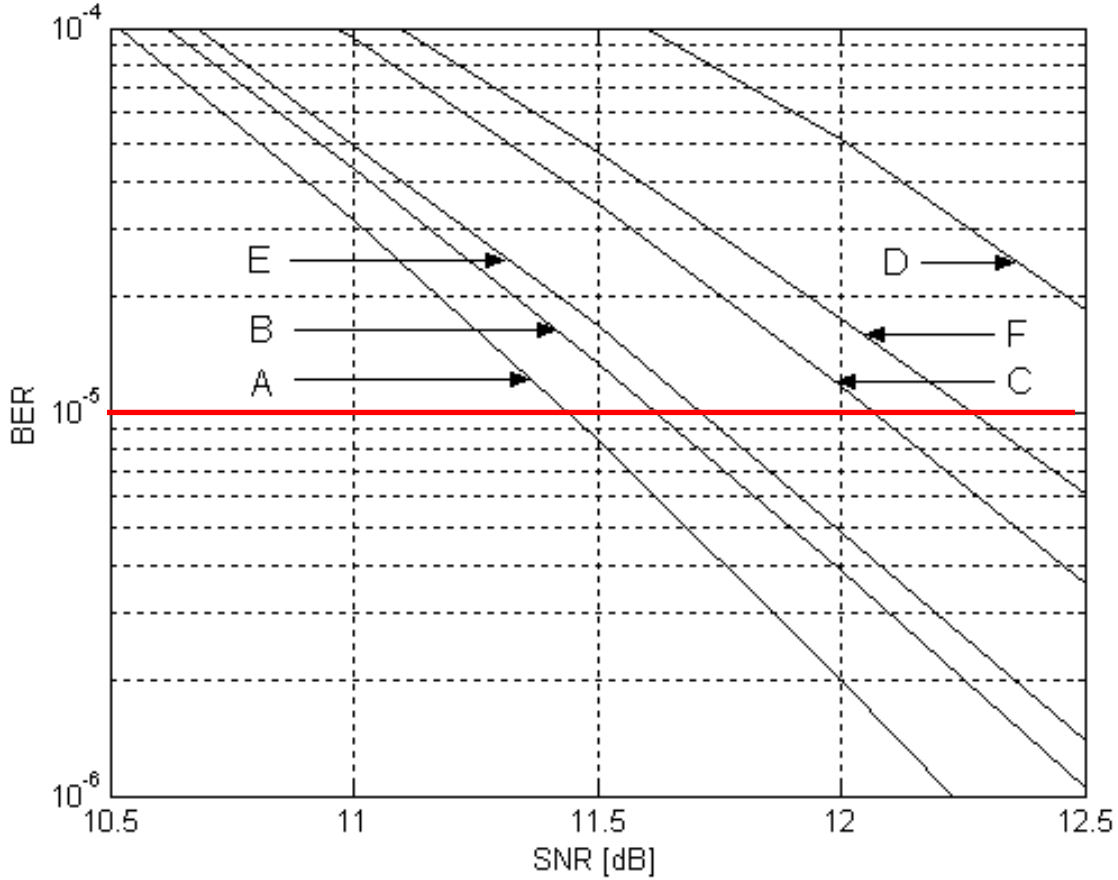


Direct-conversion BT/WiFi receiver architecture

Remarks

- Direct-conversion architecture is used for both standards to save power and avoid the image problem in IF architectures.
- LNA & Mixer are shared between BT and Wi-Fi.
- Gm-C LPF with programmable bandwidth is used to accommodate both standards.
- Parallel Pipeline ADC architecture is used:
  - BT: sampling rate = 11MHz, 11bits
  - Wi-Fi: sampling rate 44MHz, 8bits
- Due to the short allowed settling time, the VGA has only two gain steps in BT mode and the signal level at the ADC input will vary by 24dB.
- In Wi-Fi mode, gain steps of 2dB are employed.

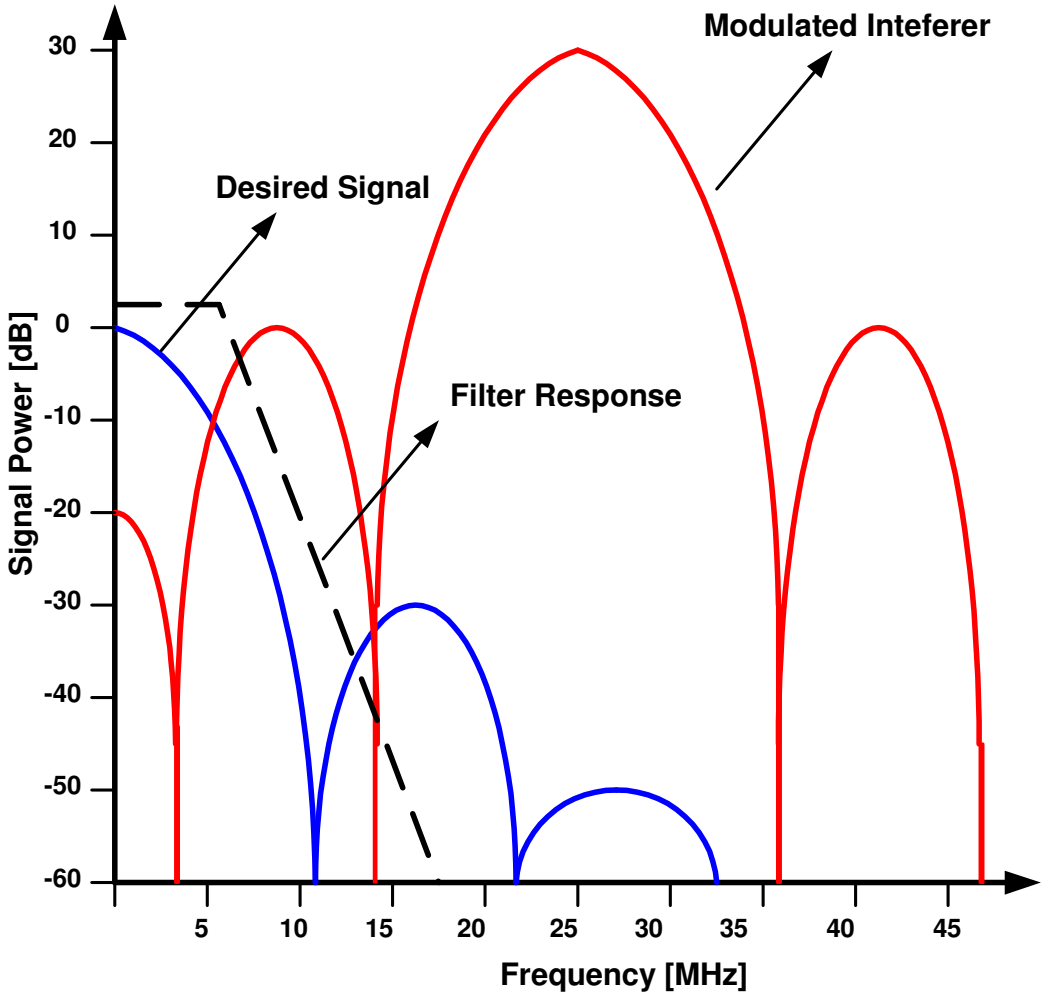
Impact of DC offset and DC offset correction on the BER performance (Wi-Fi mode)



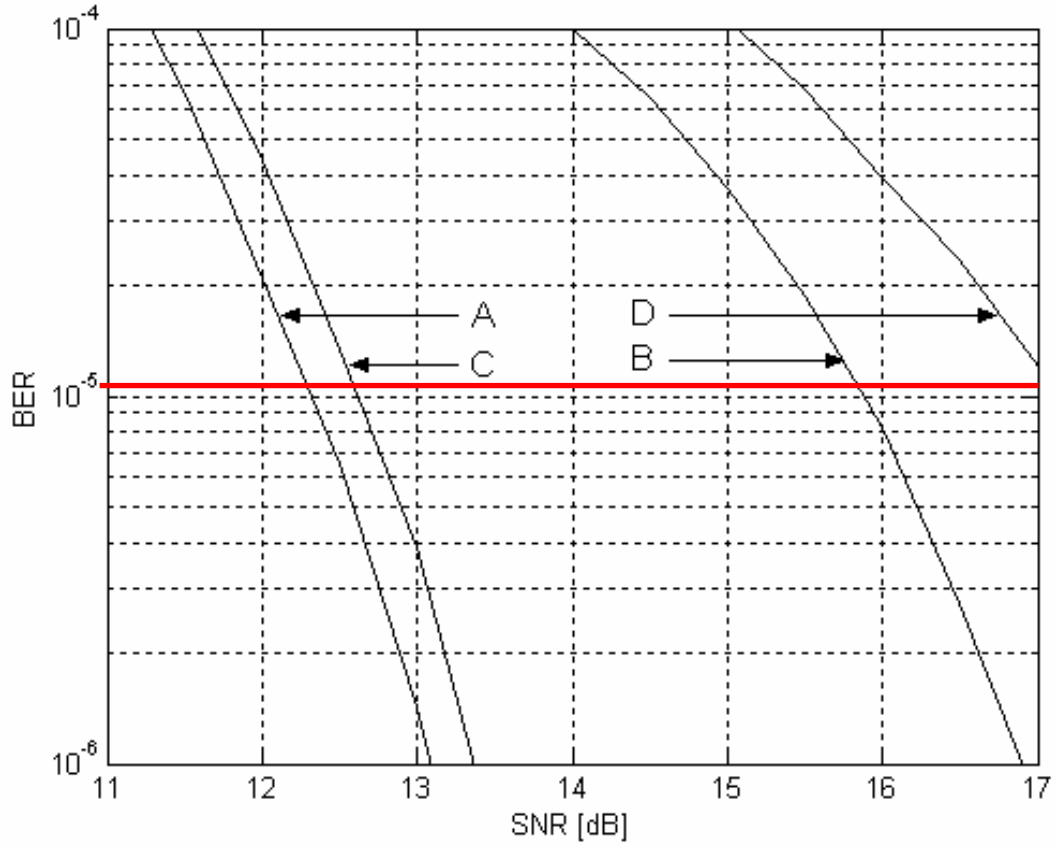
A: 0 offset. **B:** 5% offset, **C:** 10% offset, **D:** 15% offset **E:** offset cancelled with 4 HP poles at 5KHz, **F:** offset cancelled with 4 HP poles at 10KHz.

Wi-Fi Interferer Rejection Requirements

- In the presence of a modulated interferer at 25MHz with a power 35dB above the signal of interest, the receiver should show 1E-5 BER for an SNR 6dB above the minimum sensitivity.
- The channel selection filter should reject an strong interferer while not affecting the spectrum of interest.

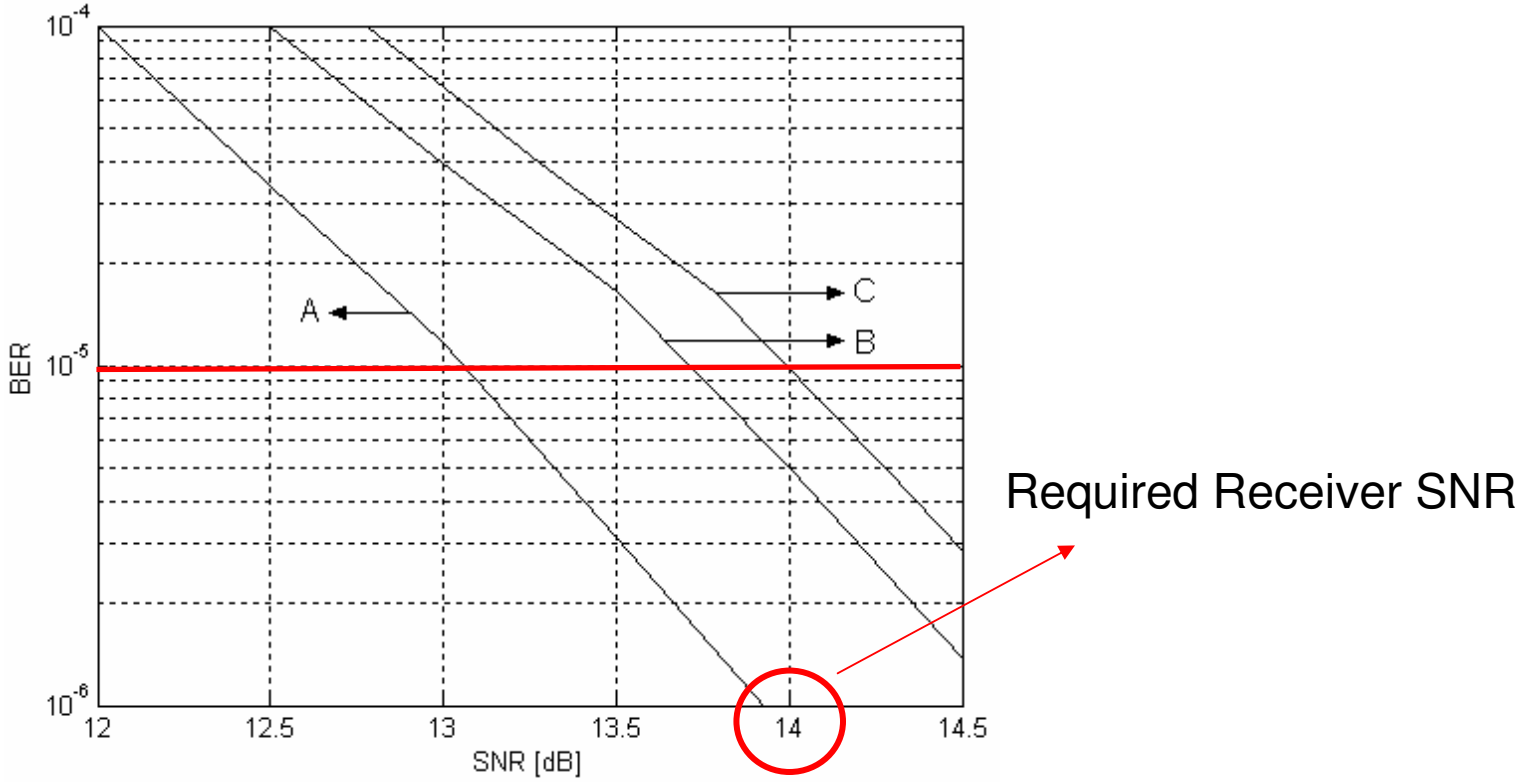


Impact of the channel selection filter characteristics on the BER performance (Wi-Fi mode)



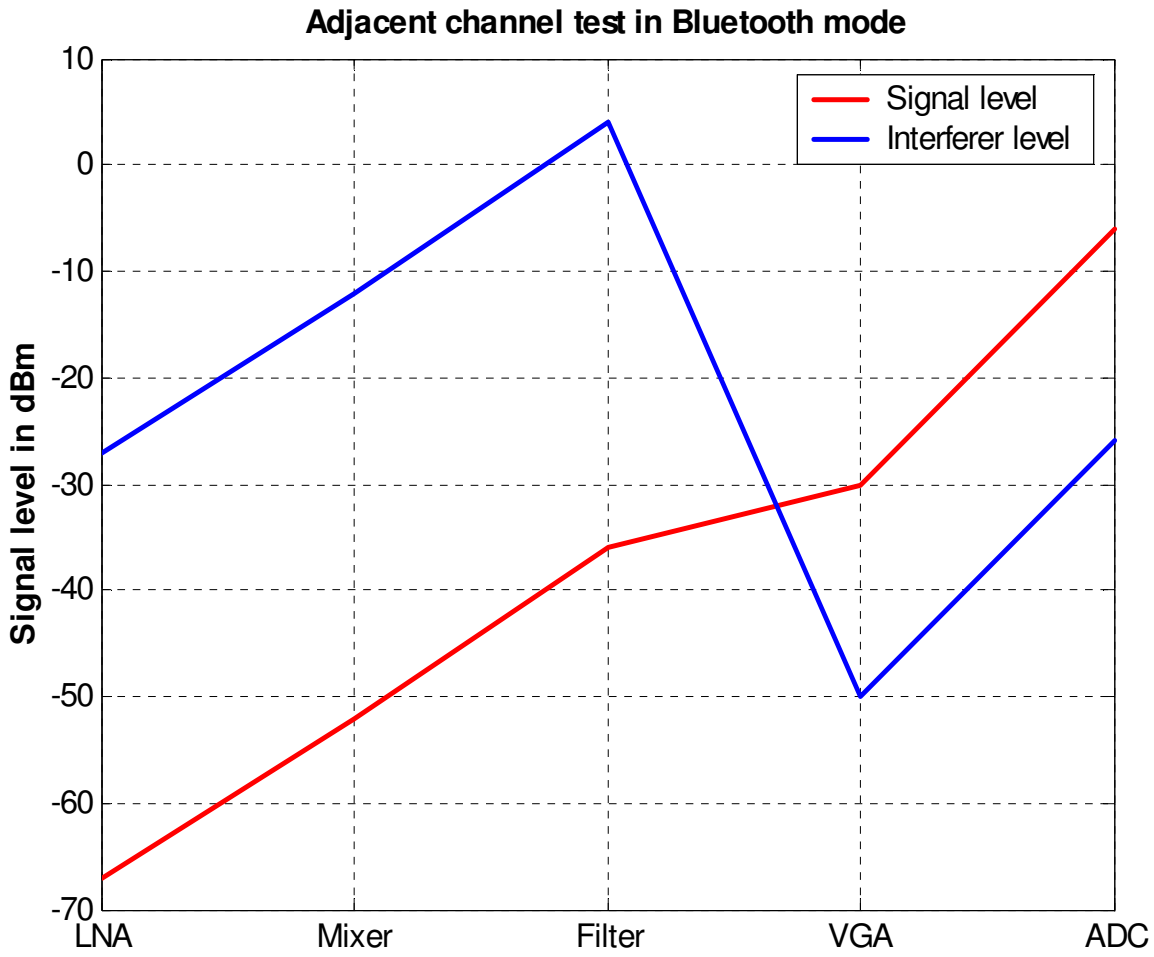
- 5th order Butterworth filter with f_C=5.5MHz with (B) and without an interferer (A).
- 4th Chebyshev filter with f_c=6MHz with (D) and without an interferer (C).

Impact of the mismatch between I and Q channels on the BER performance (Wi-Fi mode)

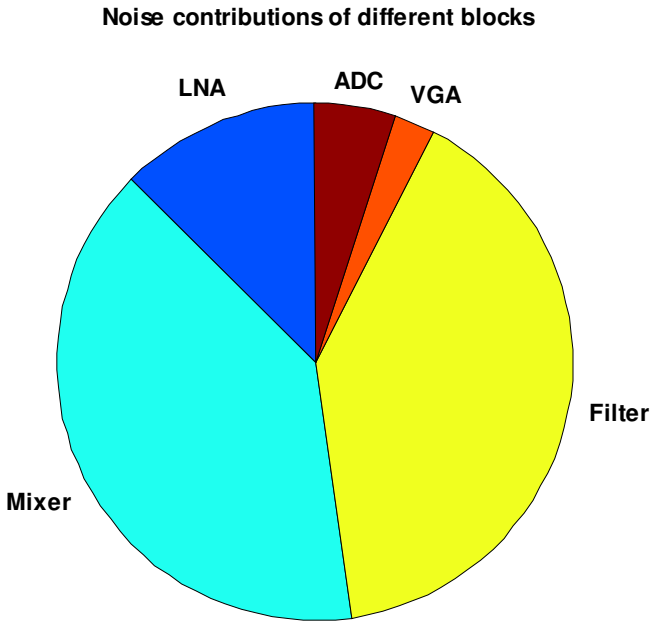


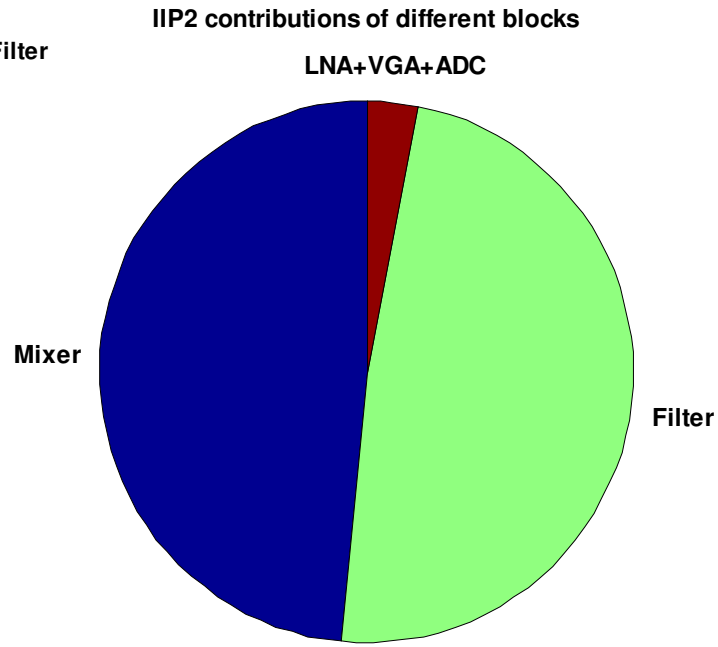
- A: Receiver performance including channel selection filter and DC offset correction.
- B: Performance with a 10º error in the generation of I and Q signals.
- C: Performance with 1.5dB gain mismatch between I and Q channels in addition to the phase error.

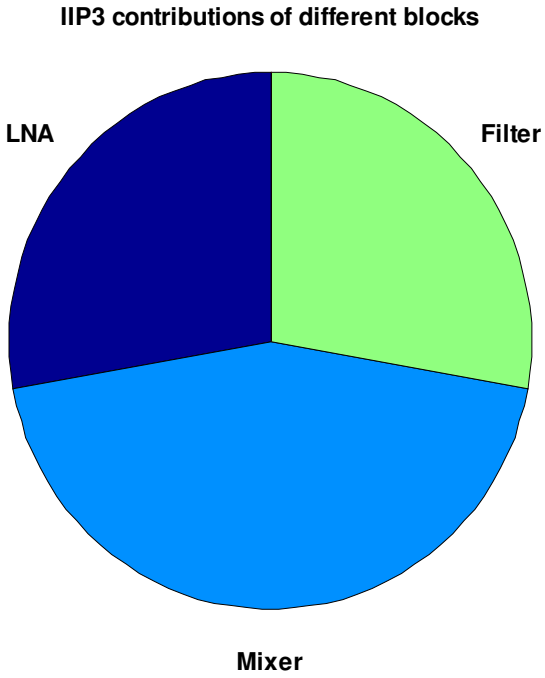
Adjacent Channel Test



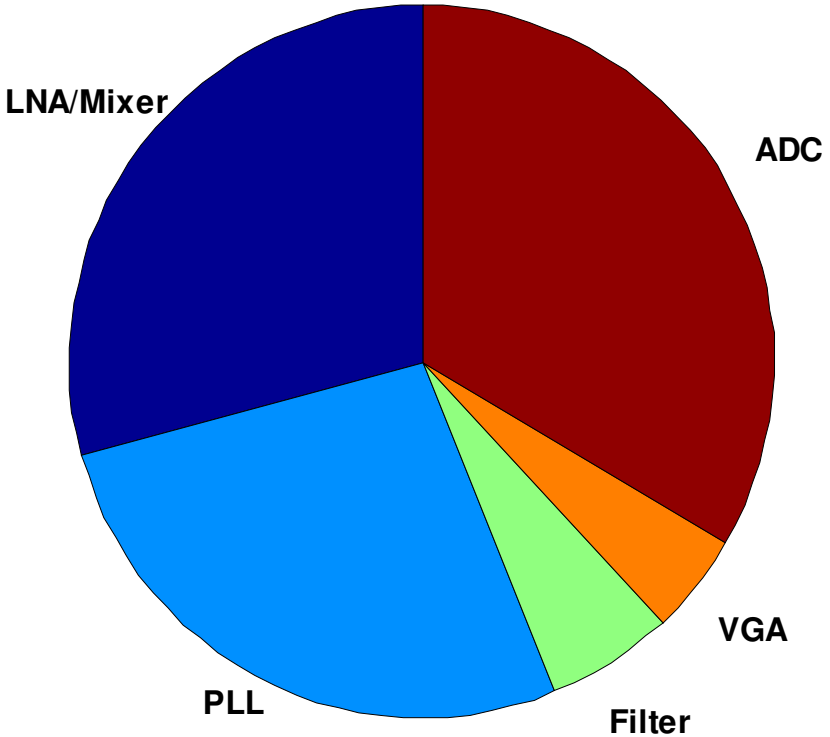
NF, IIP3, and IIP2 contributions



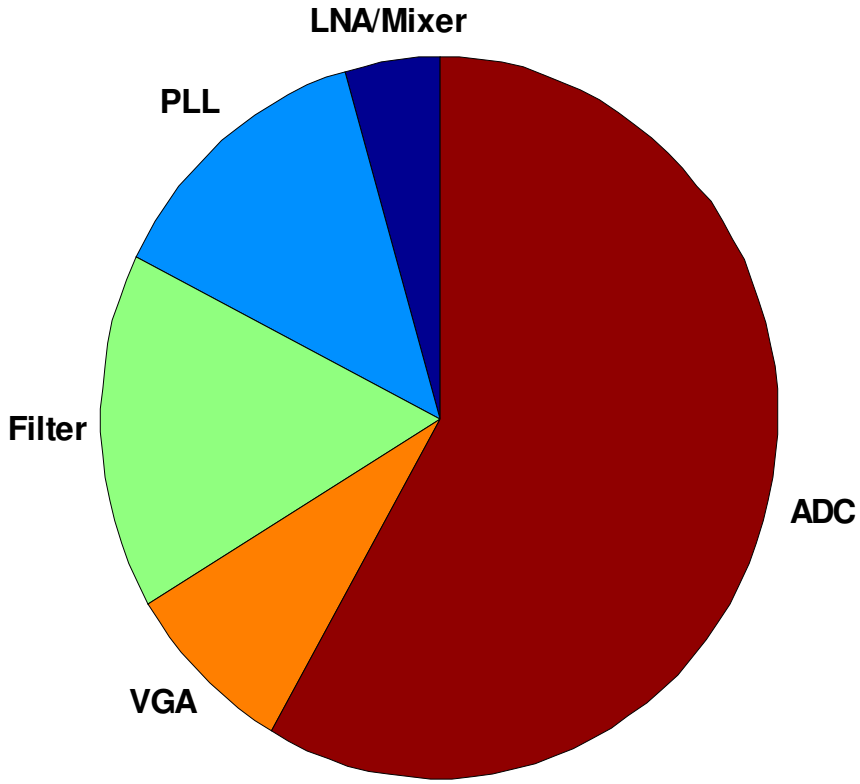




Power consumption and area contributions



Power consumption contributions of different blocks in WiFi mode



Area contributions of different blocks in WiFi mode

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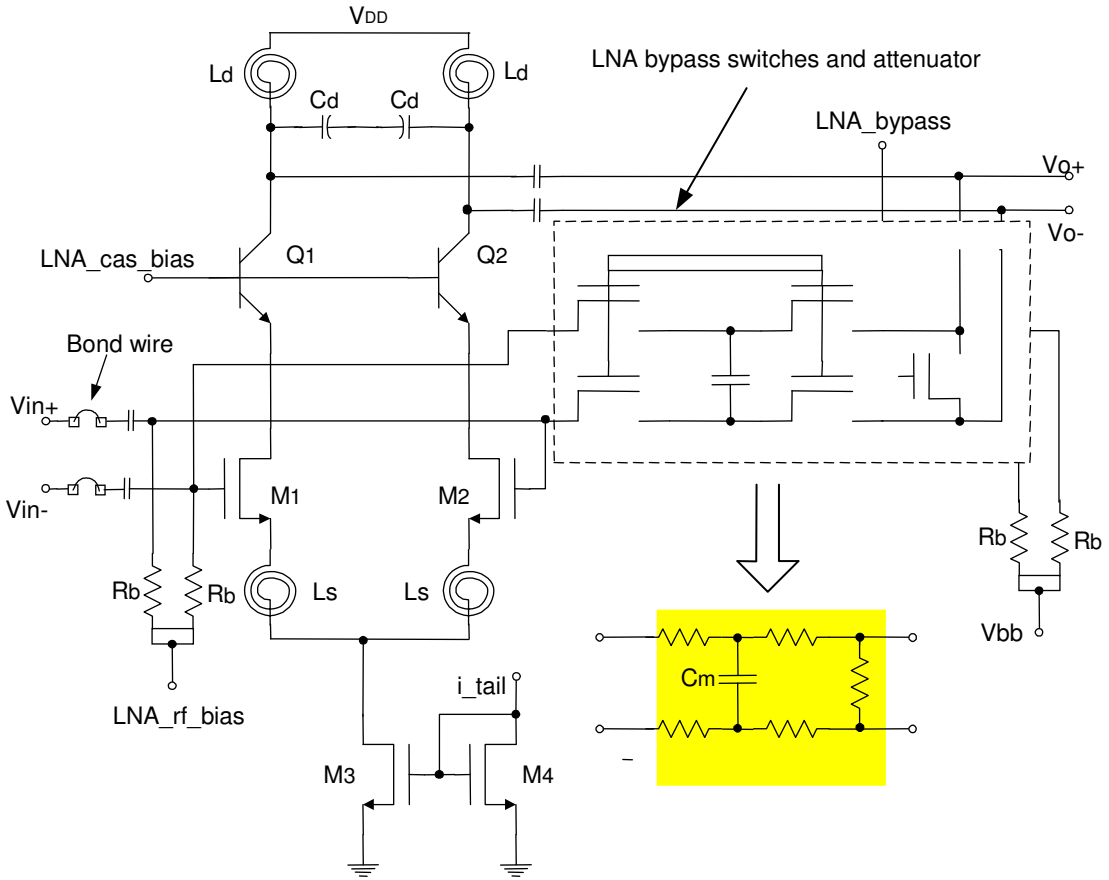
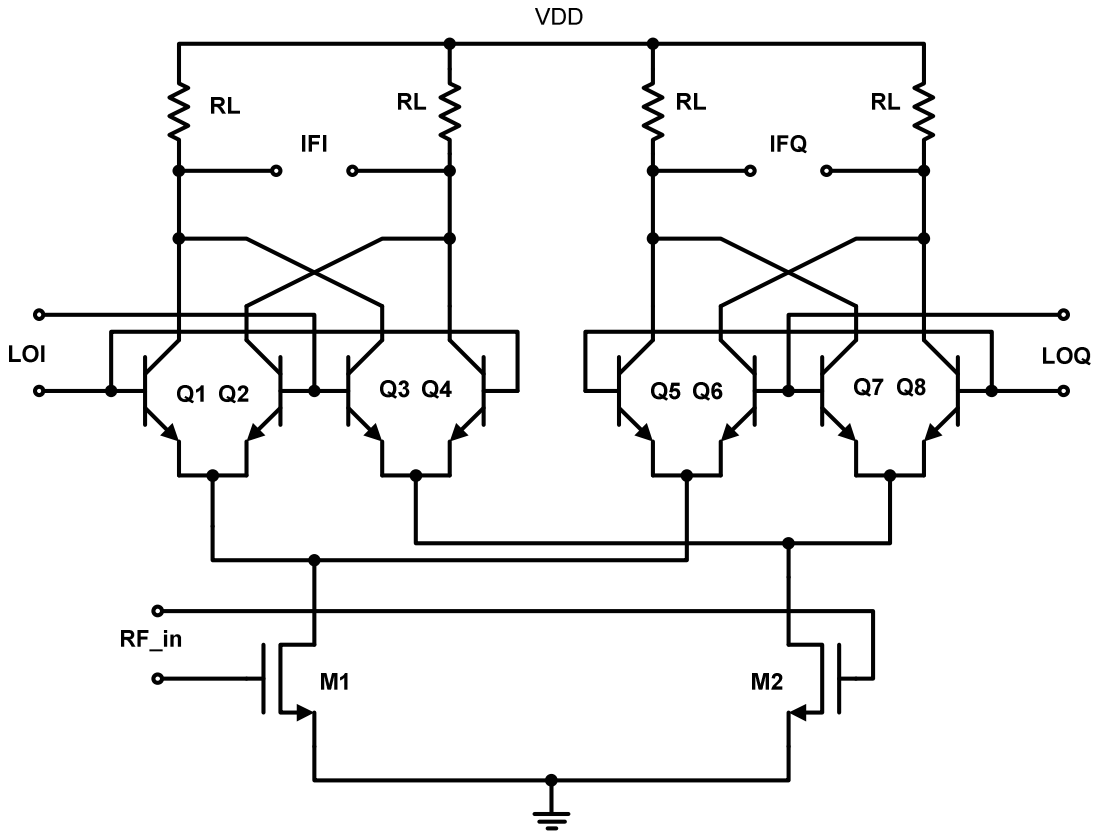
Low Noise Amplifier

- Gain = 15/-15dB
- NMOS drive is used for better linearity.
- C_m ensures matching in low-gain mode.



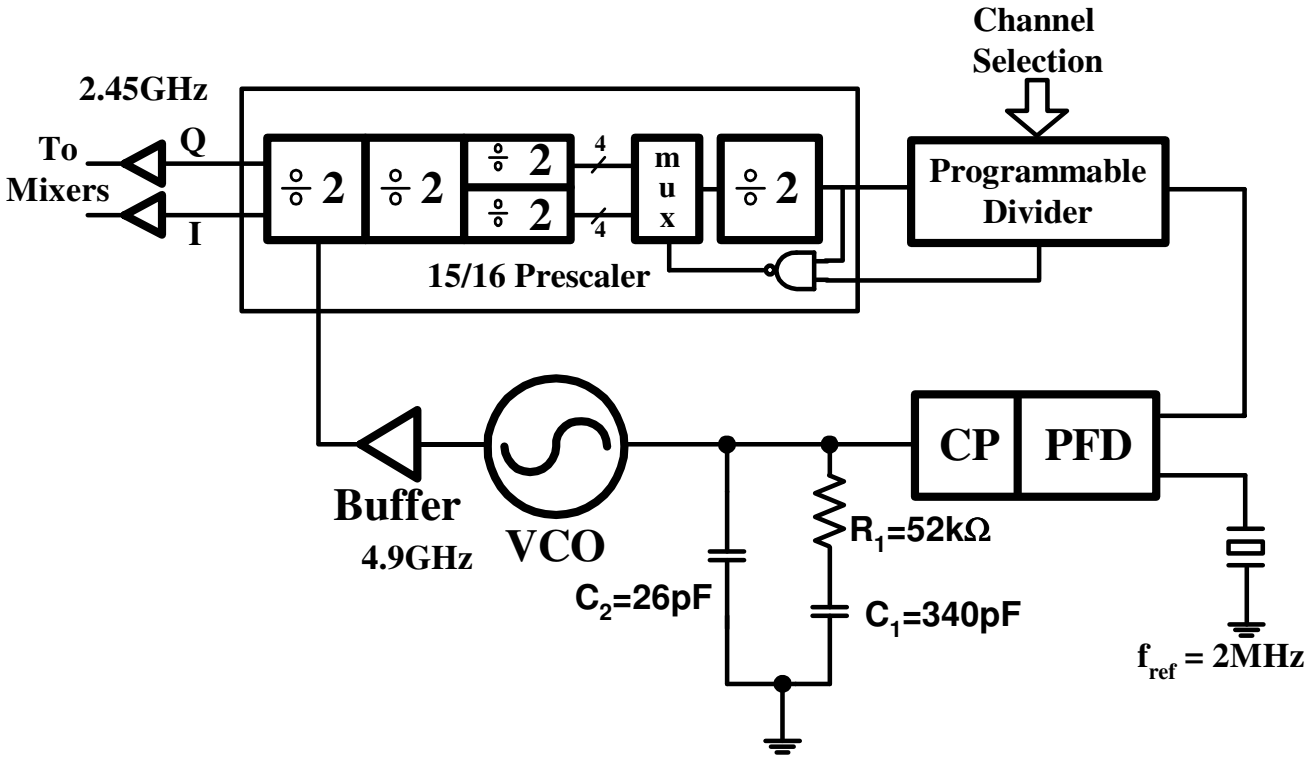
I/Q Downconversion Mixer



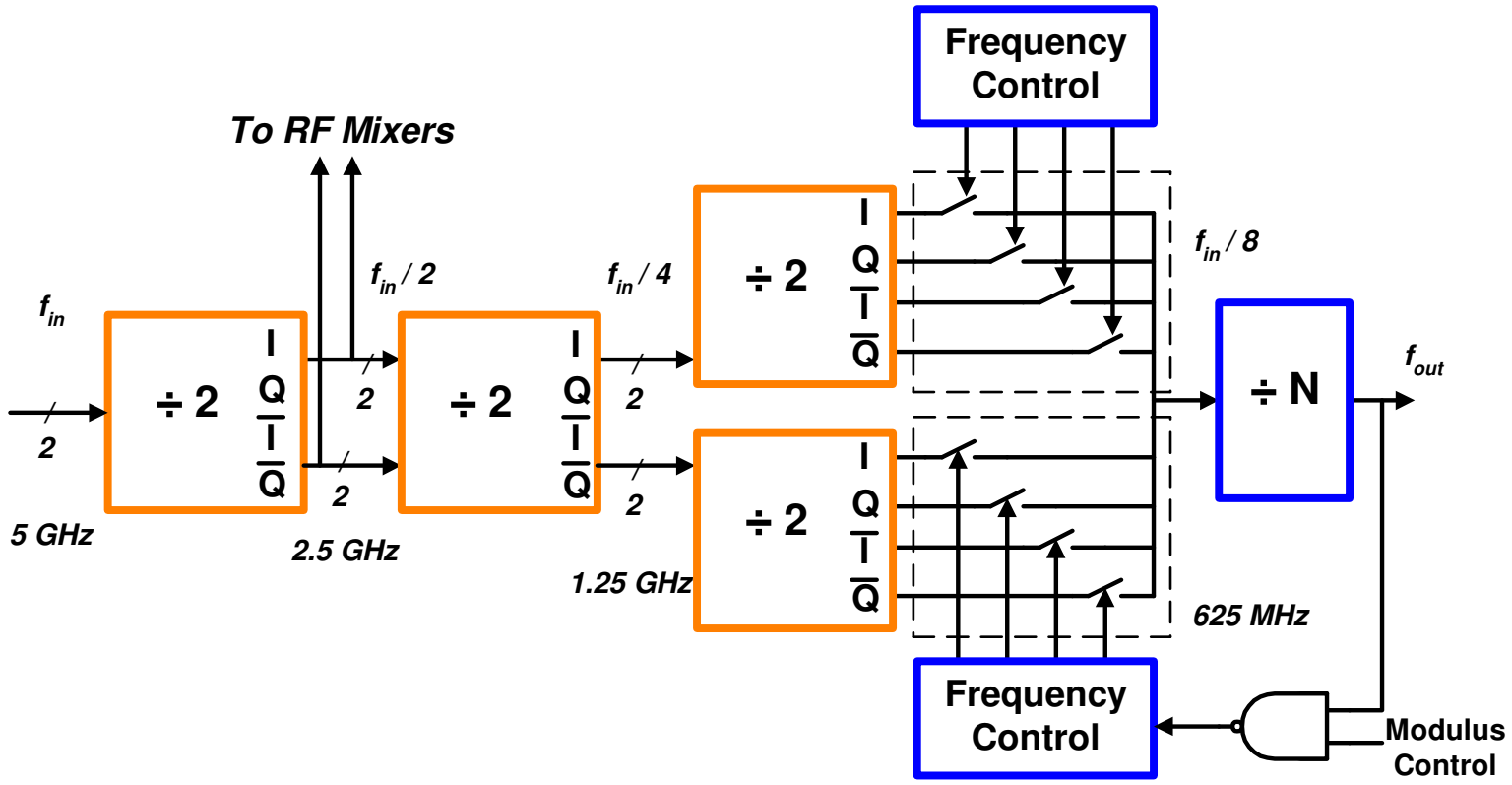
- I & Q share the same RF drive stage
- NMOS drive for better linearity
- NPN switch to reduce LO drive and 1/f noise

Frequency Synthesizer

- VCO running at $2f_o$
- I/Q generation using divide-by-2 flip flop.
- Capacitor multiplier to integrate loop filter cap.

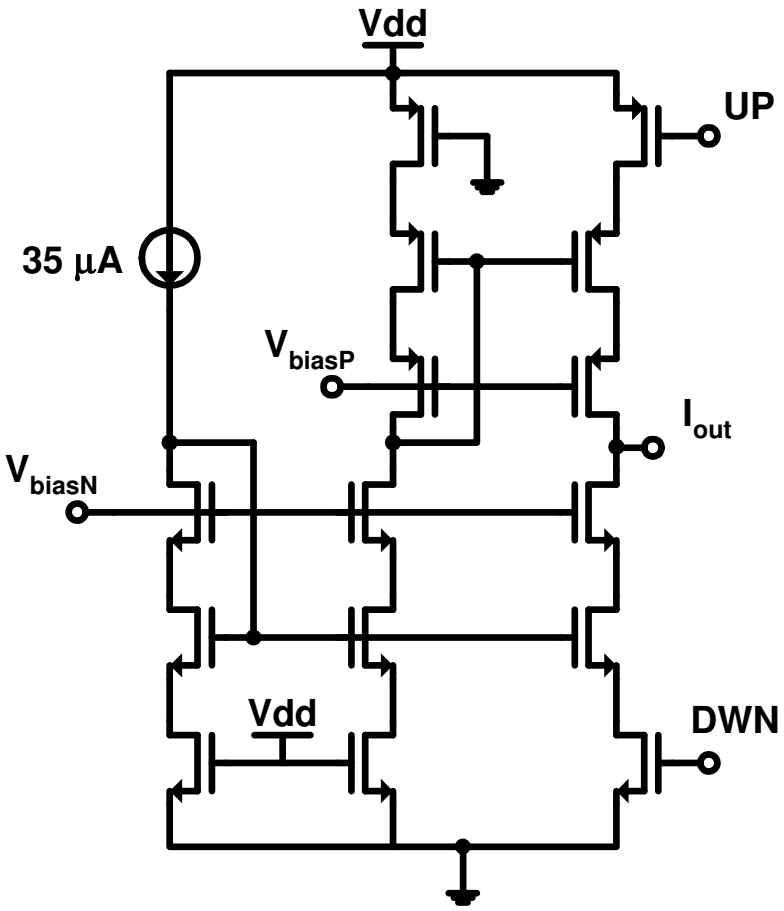


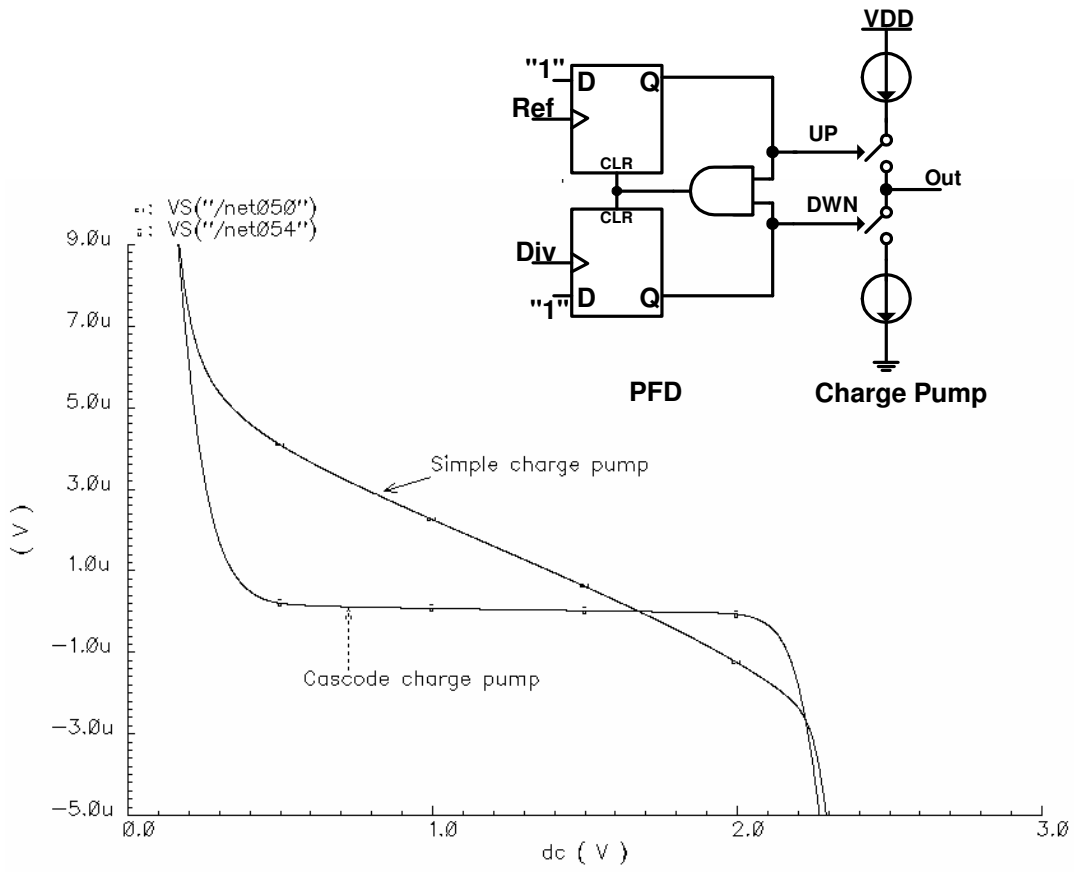
Phase Switching Prescaler



- Phase switching prescaler for reduced power consumption compared with traditional architectures.
- No feedback in flip-flops.

Charge Pump

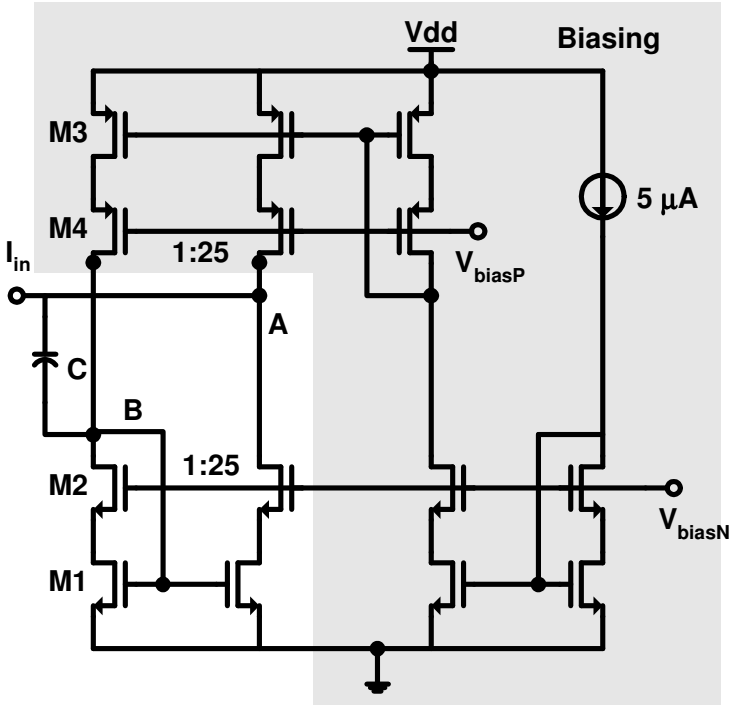




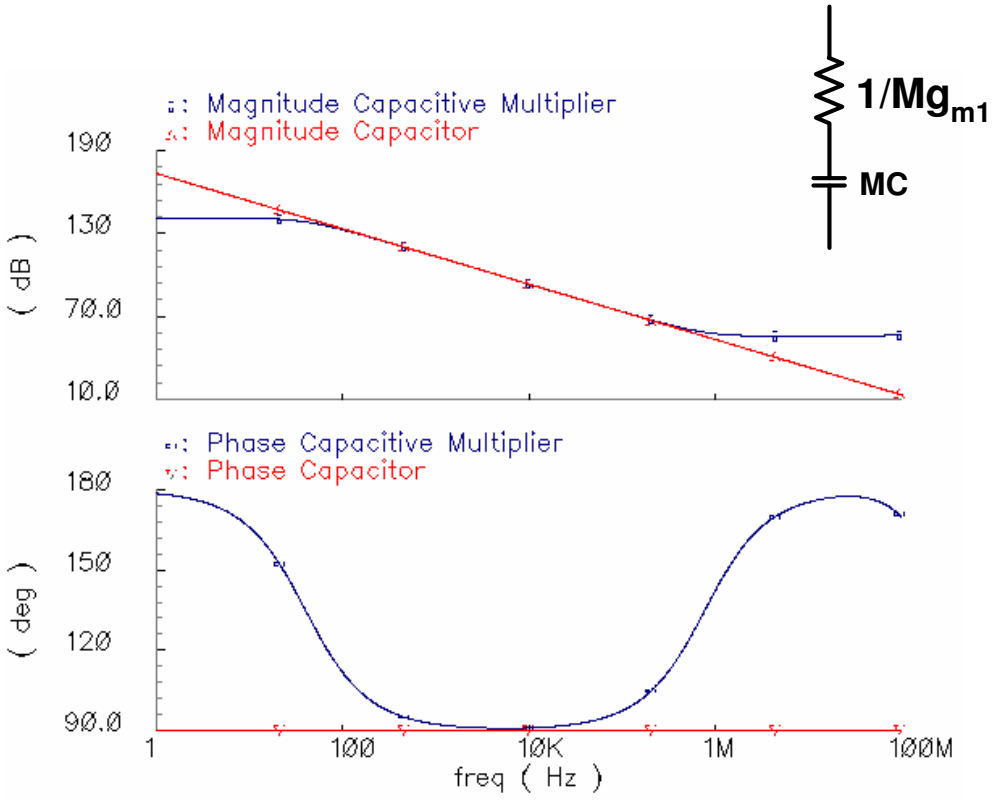
Cascode current mirrors minimize the current mismatch in Up and Dwn operation.

Capacitance Multiplier

$$z_{in} = \frac{z_0}{M+1}$$

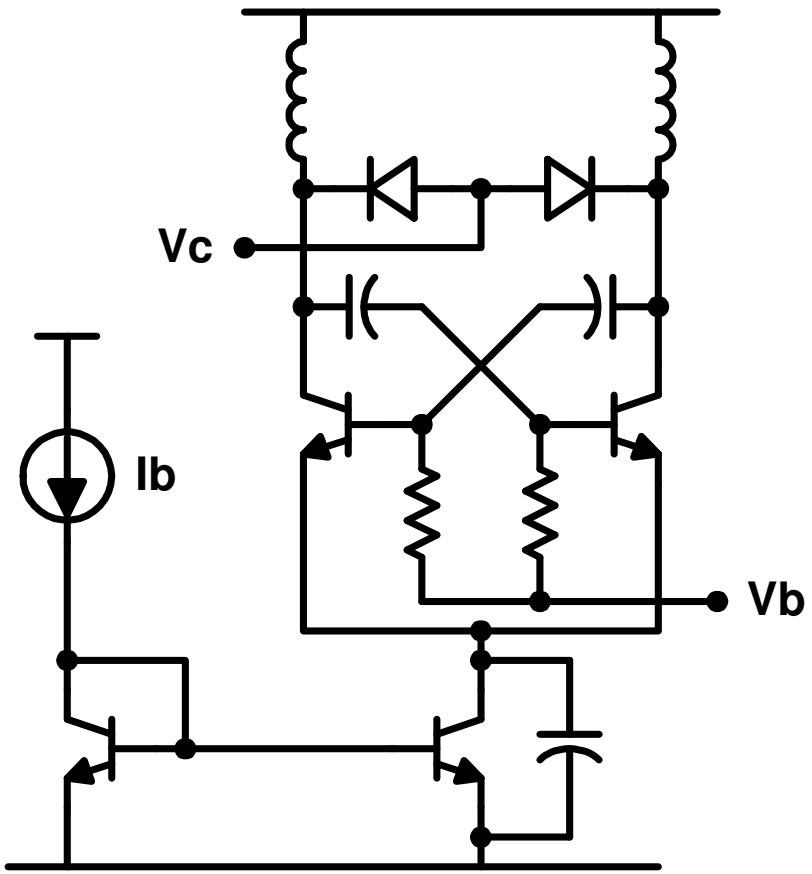


$1/Mg_{m1}<<R1$



Total Current: 150 µA

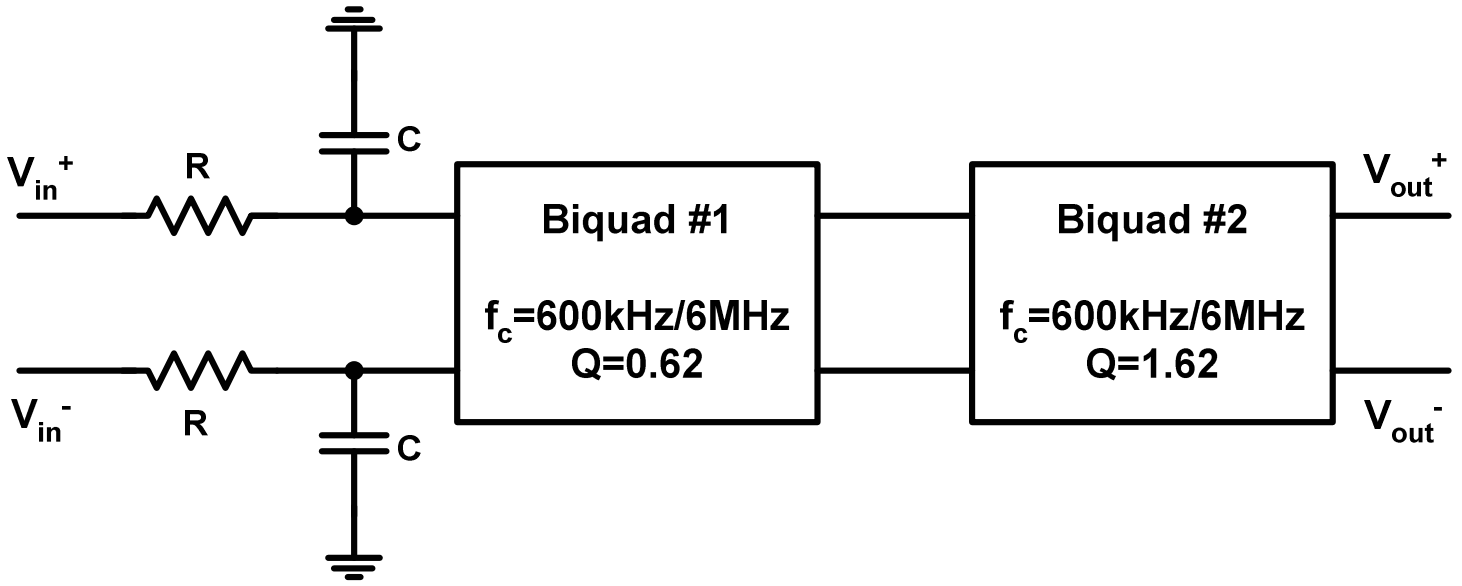
VCO



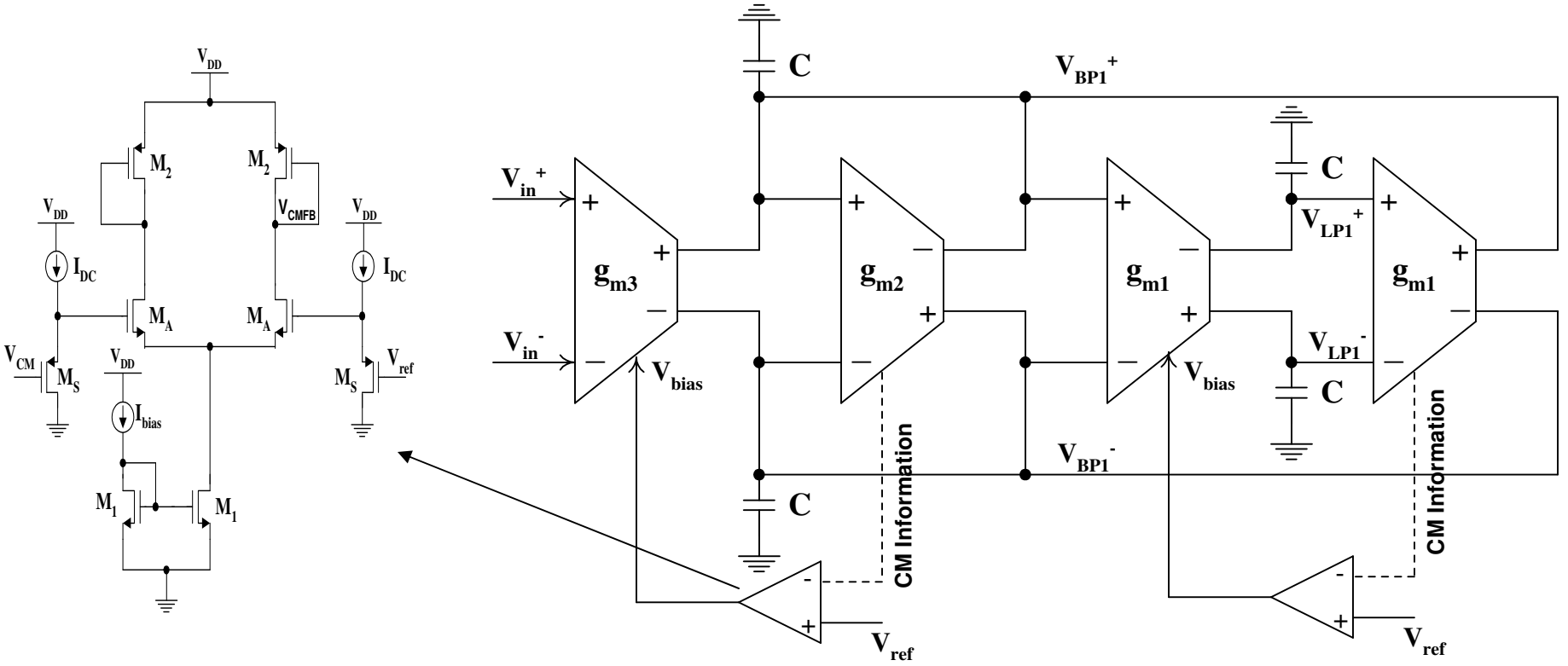
- LC tuned negative-g_m VCO
- Analog metal inductor
- Varactor diode
- DC-decoupling for driver base to improve linearity and noise
- Bypass capacitor improves phase noise 2dB
- L=1.5nH, Q=13

Channel Selection Filter

- 5^{th} order Butterworth OTA-C filter.
- Passive 1^{st} pole is used to relax the biquad (OTA) linearity requirements.
- Programmable bandwidth through switching R&C.



Biquadratic Section

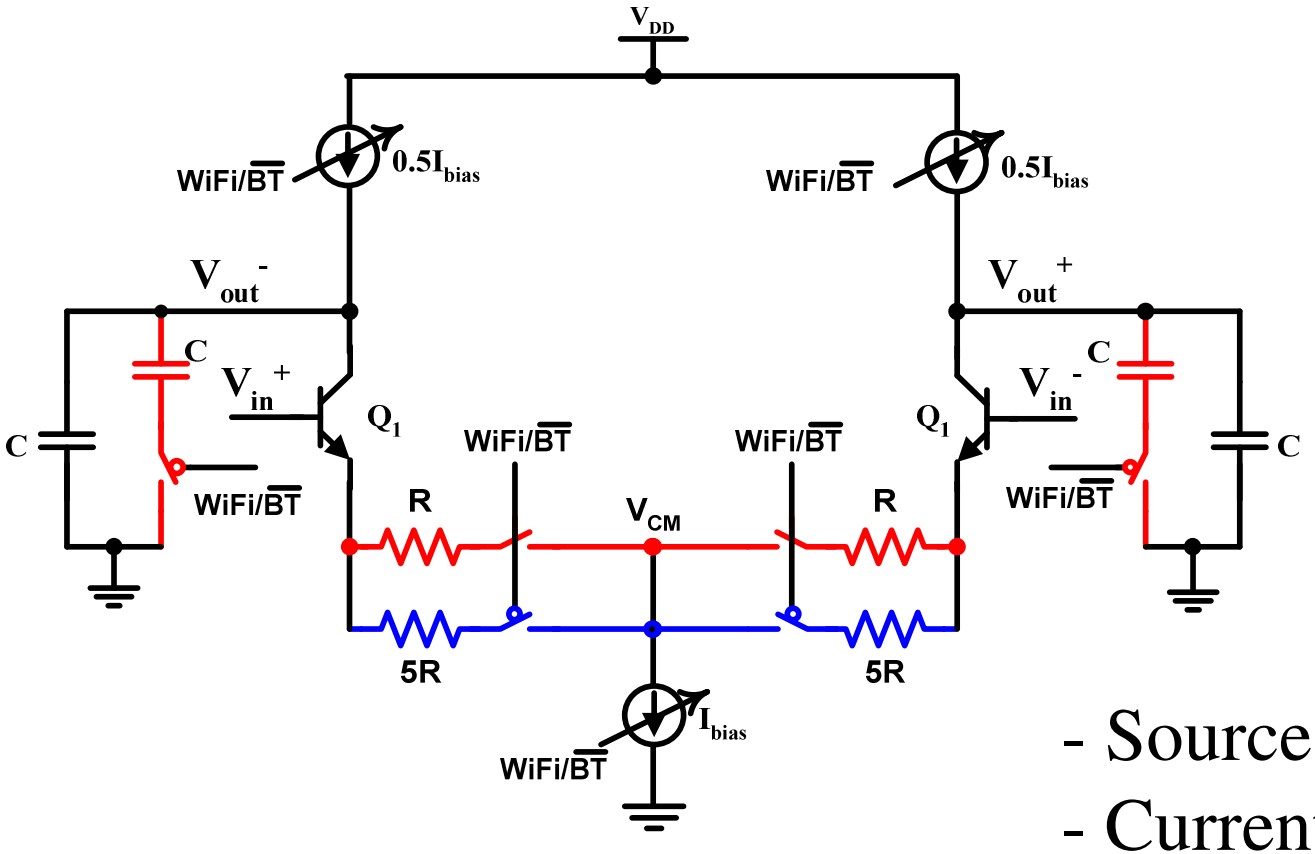


$$\omega_0 = \frac{g_{m1}}{C} \qquad Q = \frac{g_{m1}}{g_{m2}}$$

V_{DC}=1.6V

Direct connection between consecutive OTAs in the filter is exploited in the implementation of the CMFB circuit.

Dual-mode OTA

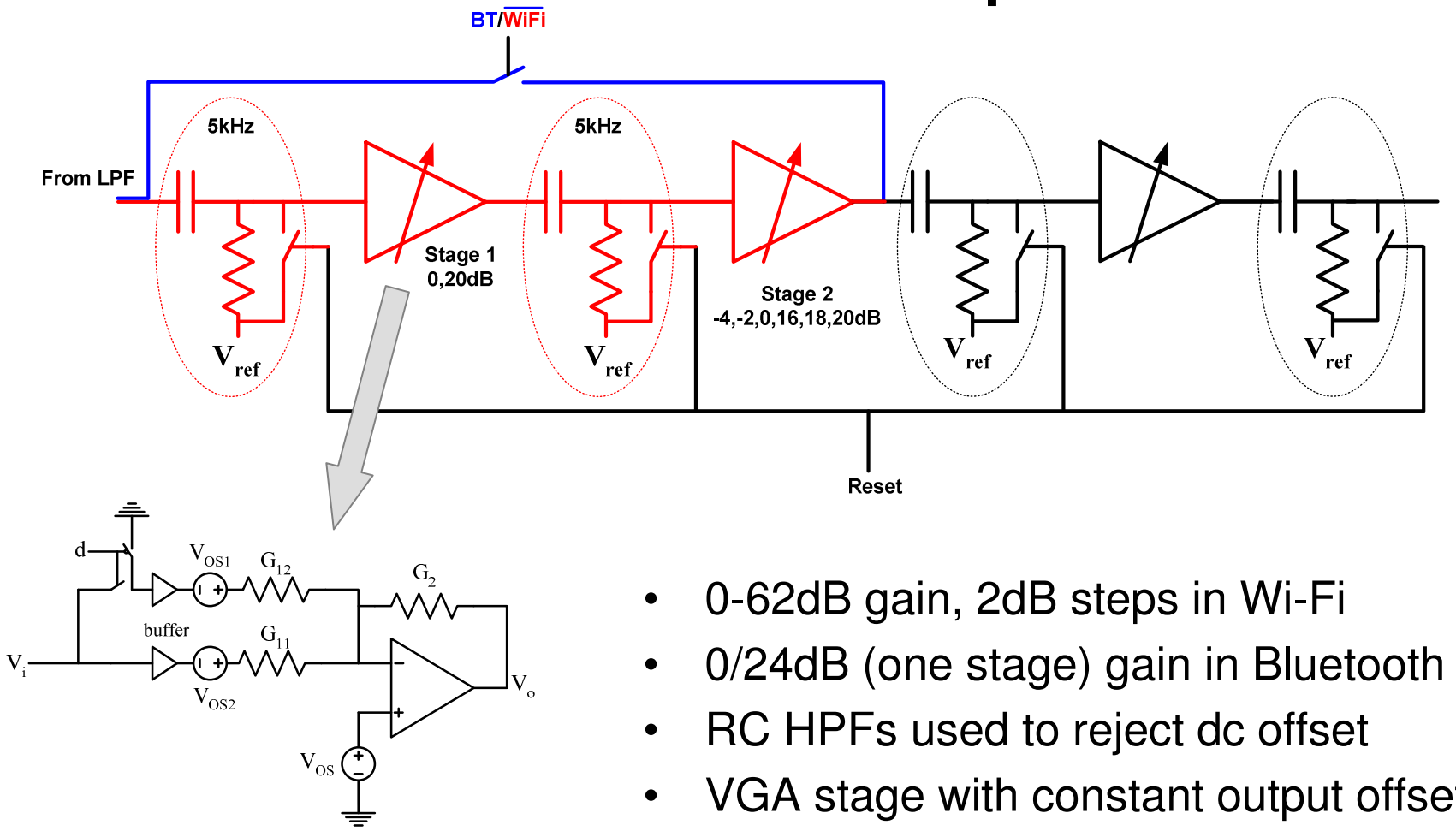


- Source degeneration
- Current scaling

$I_{bias} \times R = constant$

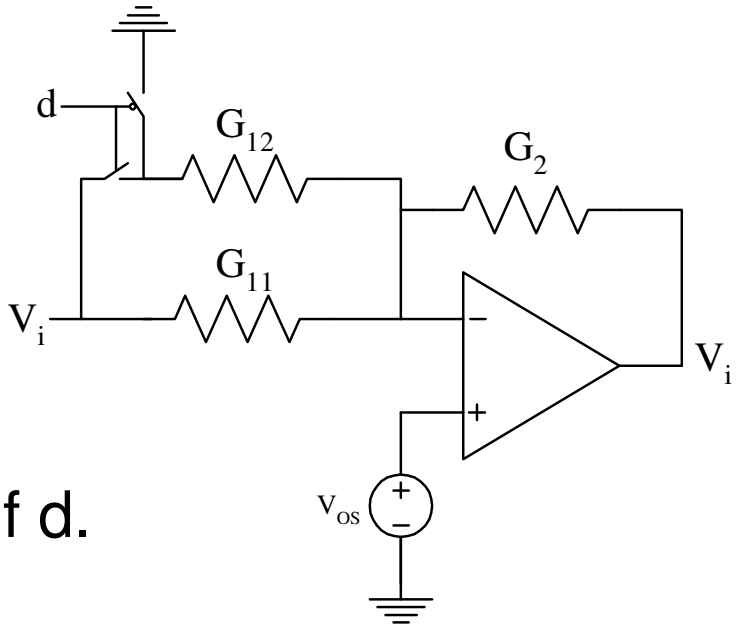
- The standard is chosen by switching R (coarse tuning)
- Fine frequency tuning using bank of capacitors C

Variable Gain Amplifier



- 0-62dB gain, 2dB steps in Wi-Fi
- 0/24dB (one stage) gain in Bluetooth
- RC HPFs used to reject dc offset
- VGA stage with constant output offset

Constant output offset VGA



- The gain is controlled by d:

$$Gain = \frac{G_{11} + dG_{12}}{G_2}$$

- The output offset is independent of d.

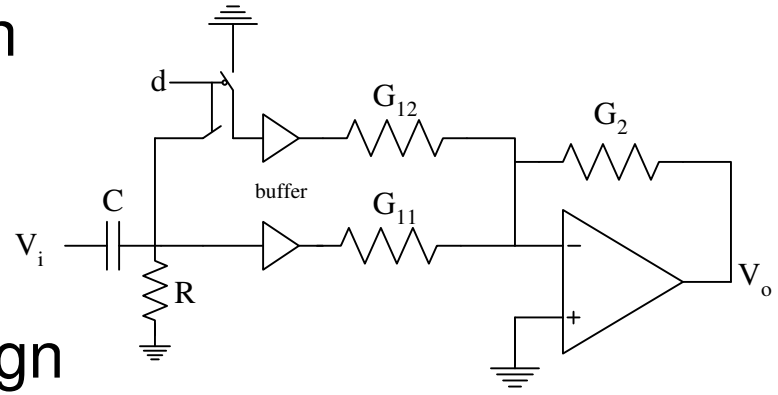
$$output\ offset = \frac{G_{11} + G_{12}}{G_2} V_{OS}$$

- This assumes that the offset in Vi is completely removed by the RC HPF.

- Problem: G_{11} and G_{12} will load the HPF $\Rightarrow$ we have to use a buffer at each input resistor

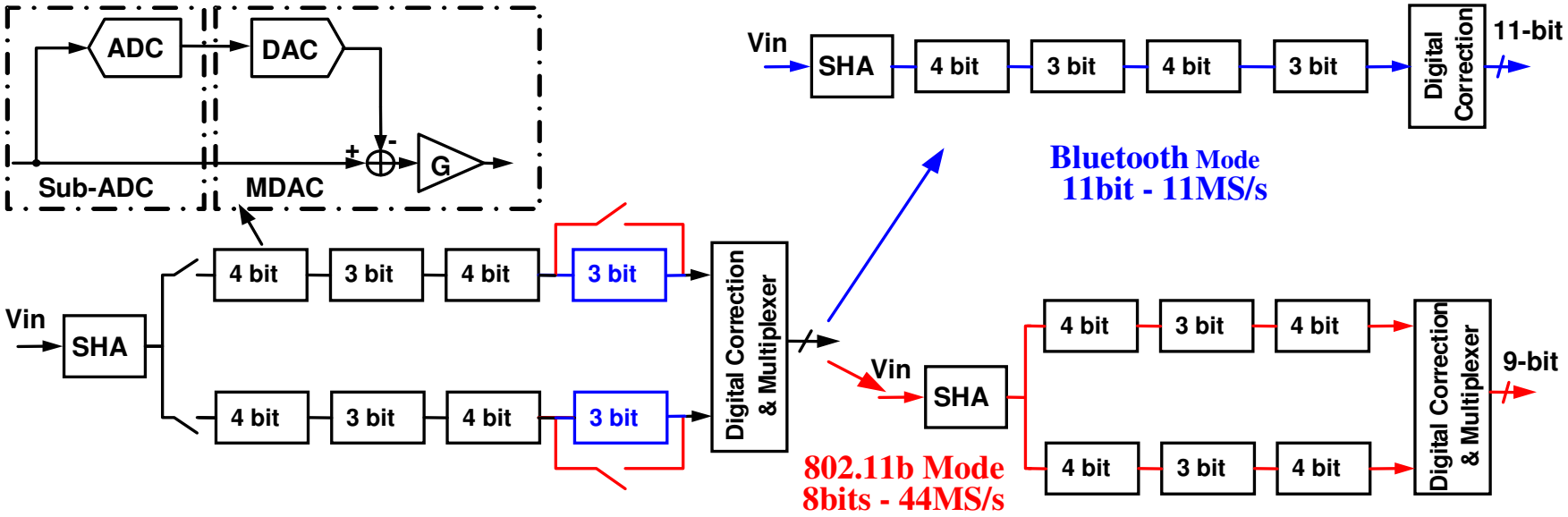
Constant output offset VGA, Cont'd

- A buffer is used to drive each input resistor.
- The feedback factor is independent of the gain. This makes the OpAmp design easier.



- Bandwidth and phase margin are independent of the gain.
- Note that the capacitor C does not load the previous stage since it is in series.
- However, the parasitic capacitance of the top and bottom plates to ground will load the previous stage!

Time-Interleaved Pipeline ADC



- Programmable resolution and sampling rate.
- On line digital calibration.

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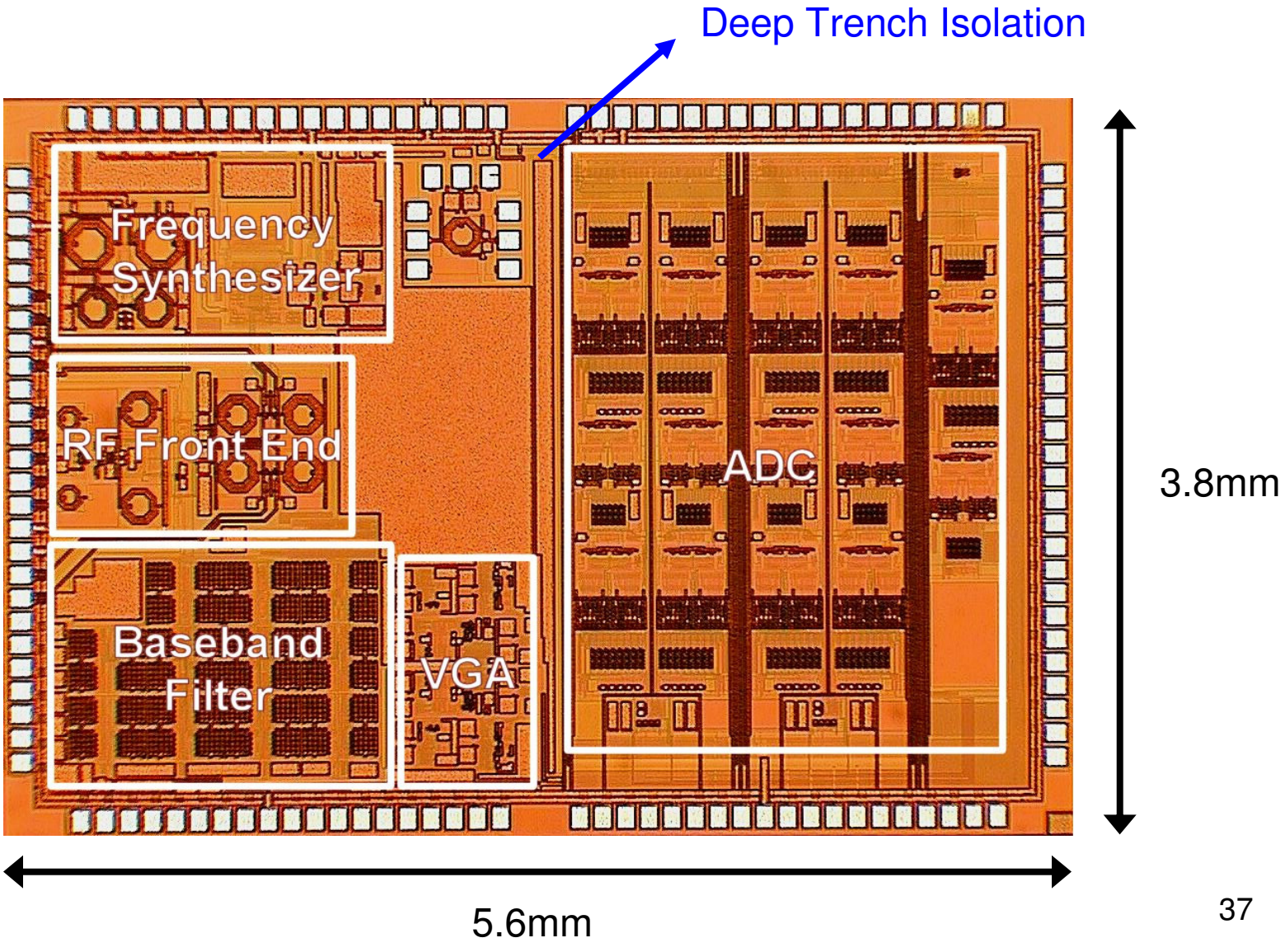
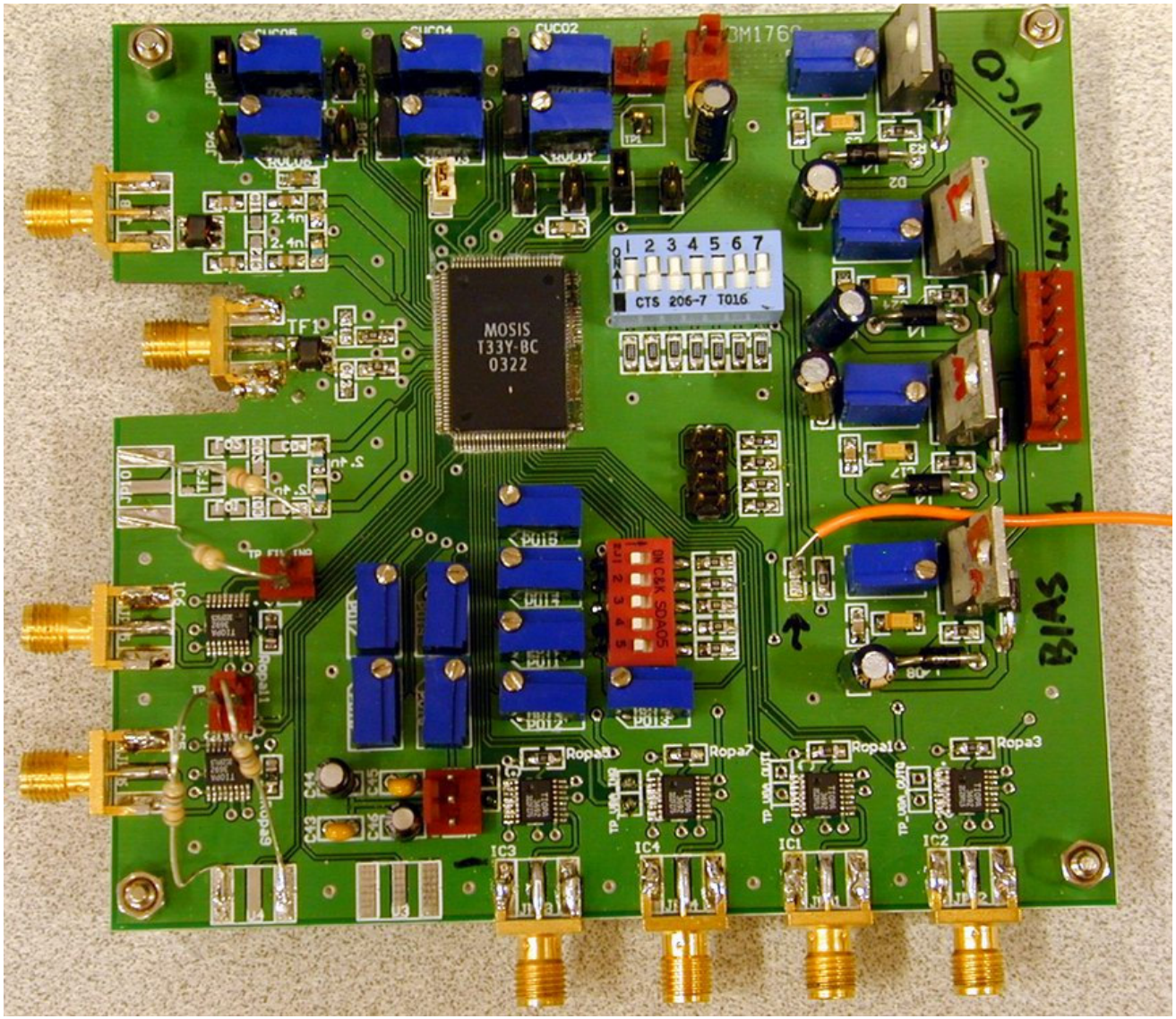
Receiver Die Photo

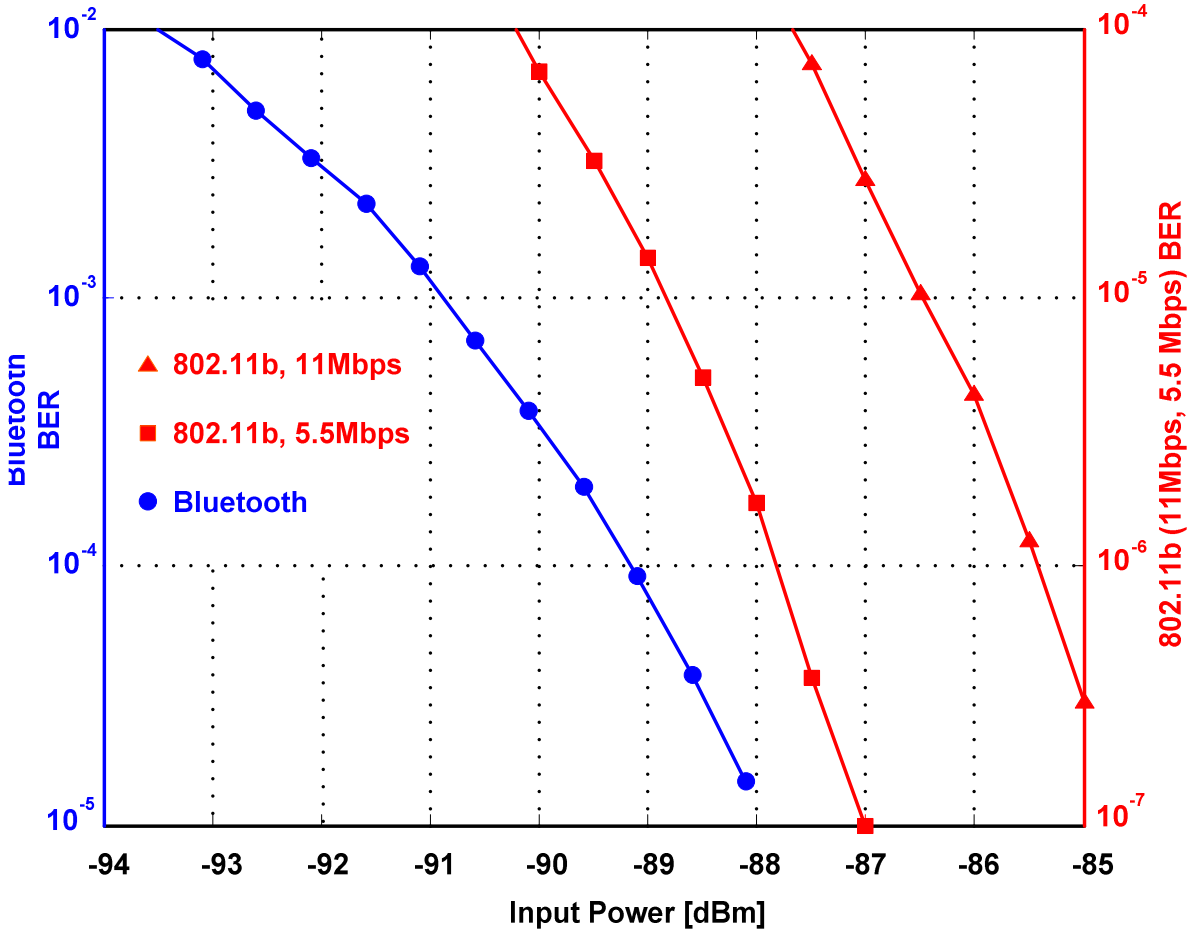


Testing Board



Receiver Sensitivity

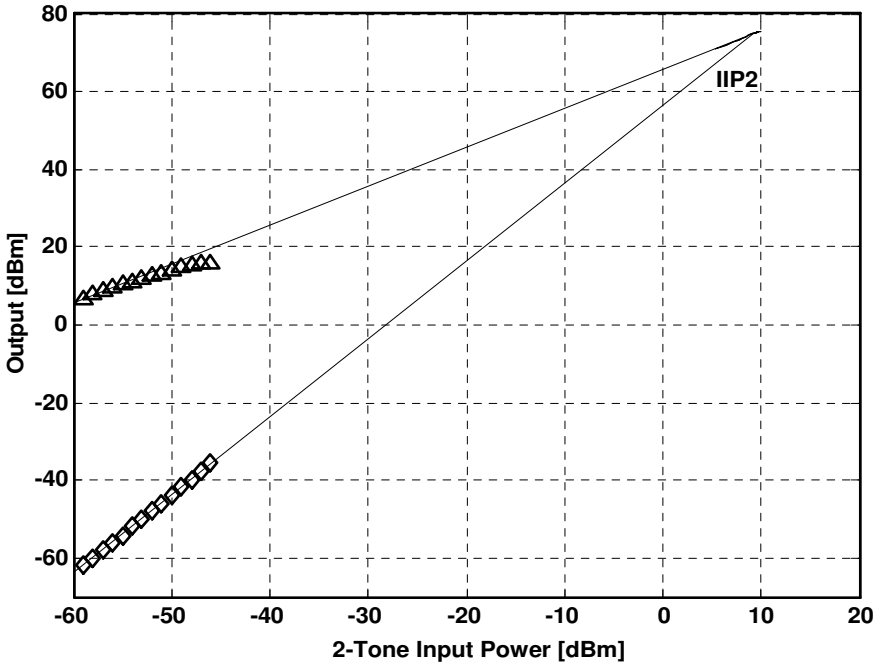
Bluetooth = -91dBm Wi-Fi (11Mb/s) = -86.5dBm



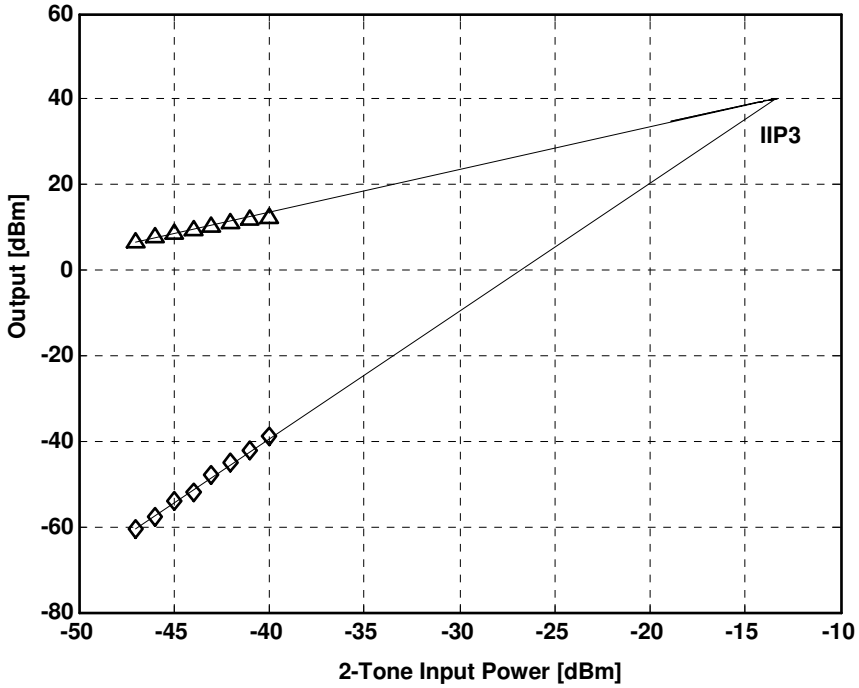
Receiver Linearity

Both BT / Wi-Fi modes

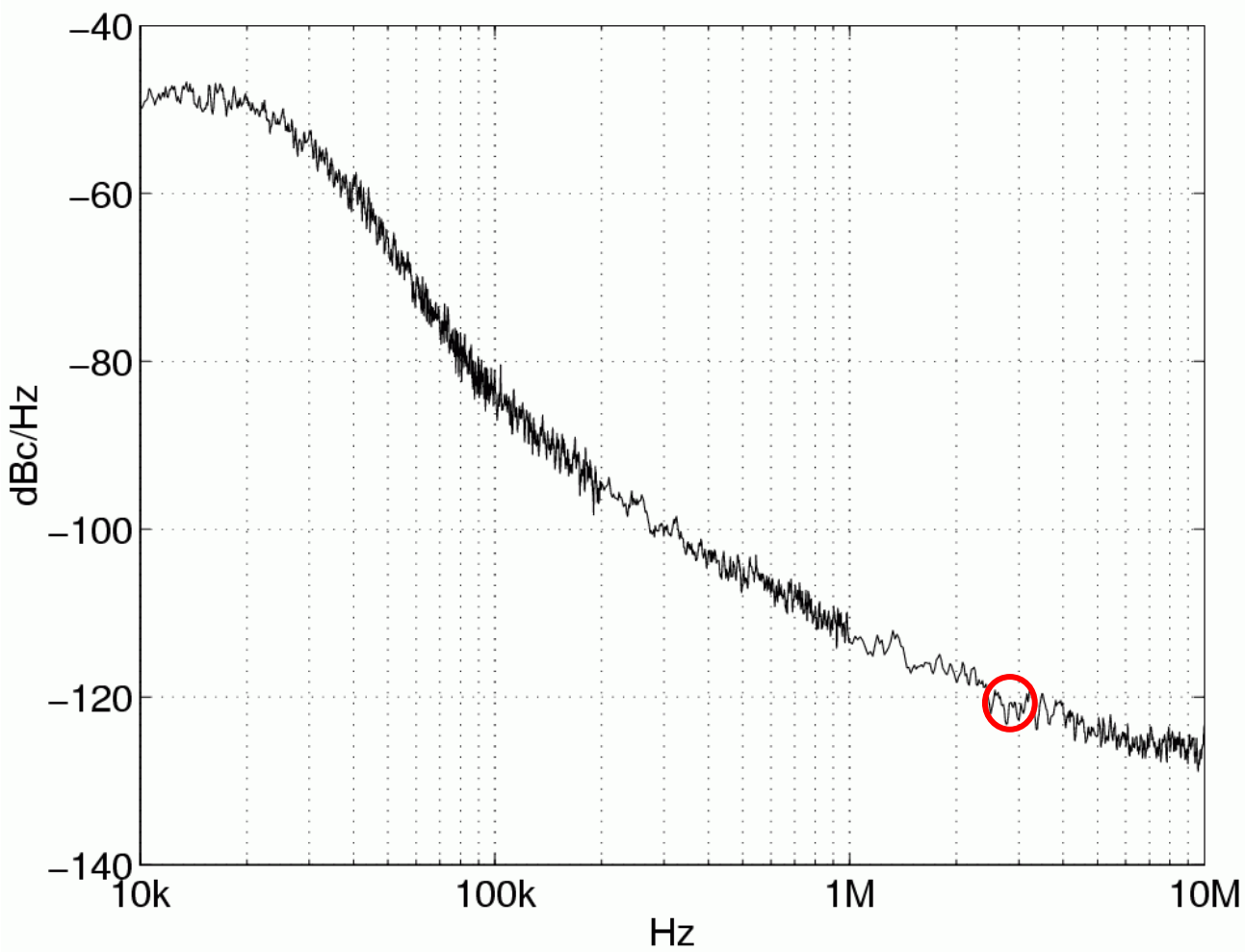
IIP2 = 10dBm



IIP3 = -13dBm

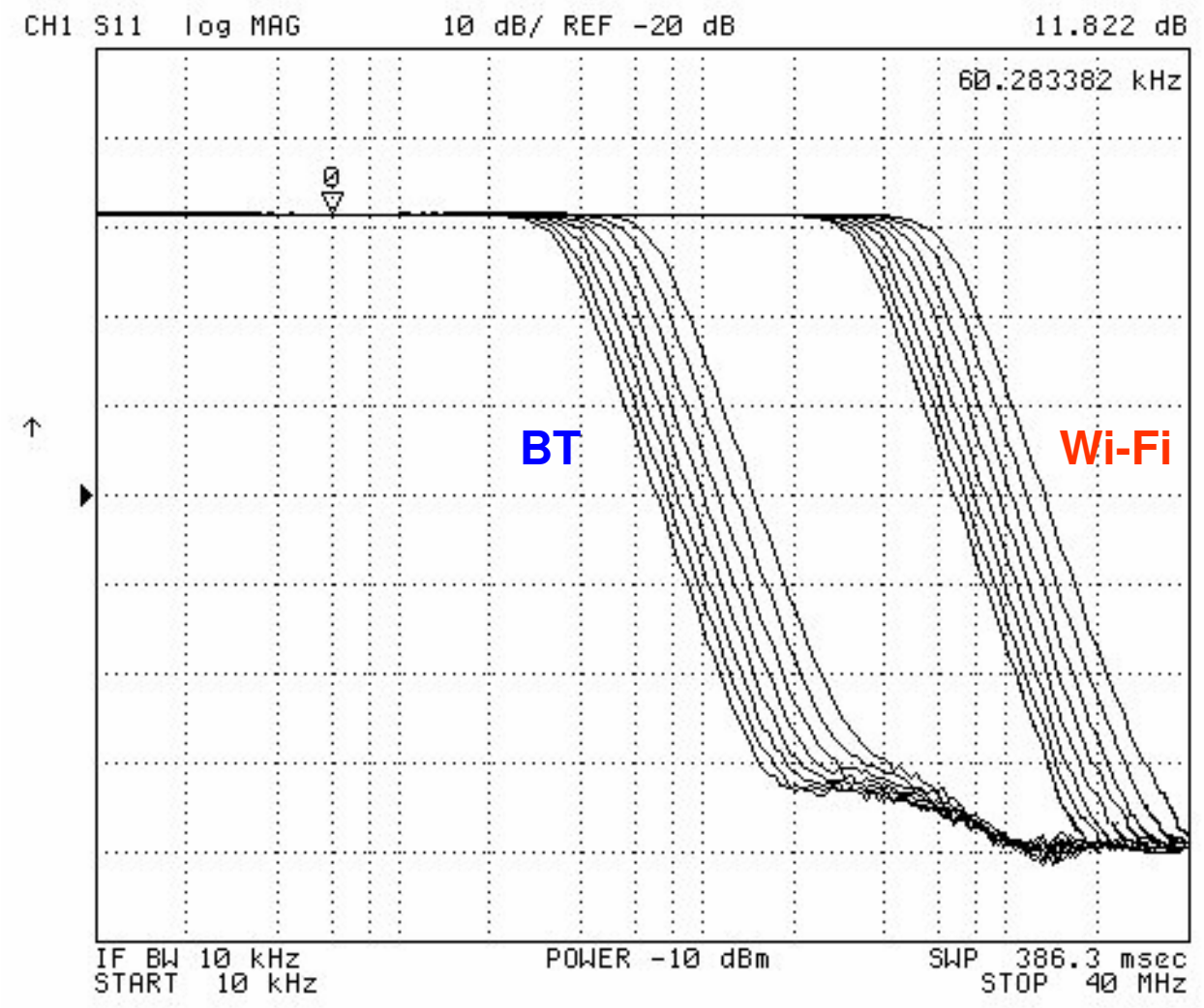


LO Phase Noise



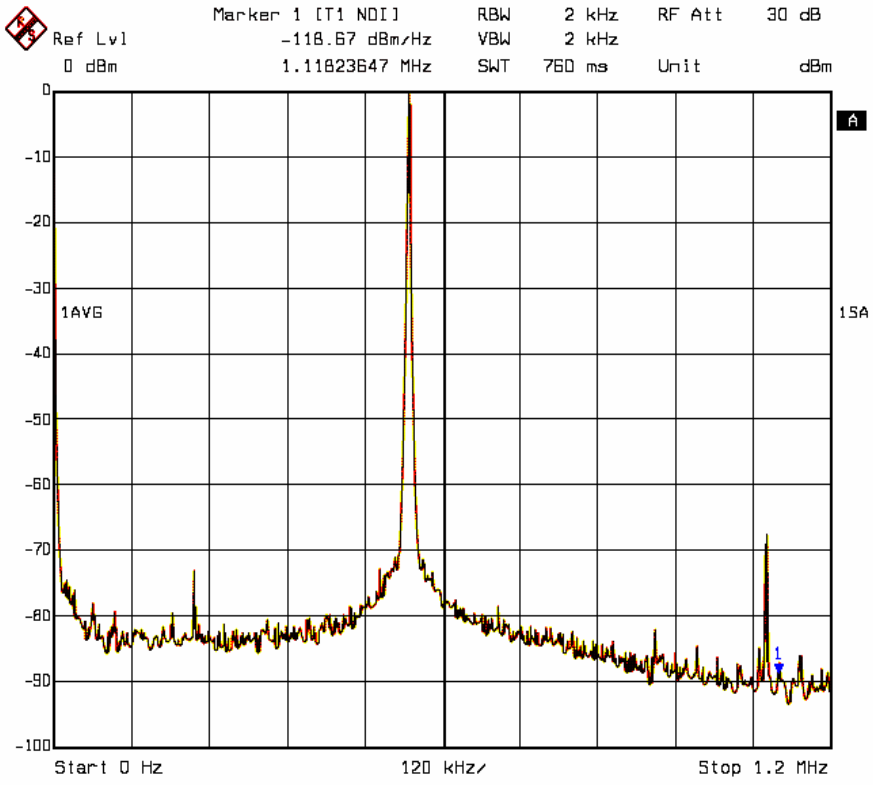
-124 dBc/Hz @ 3MHz

LPF Programmability

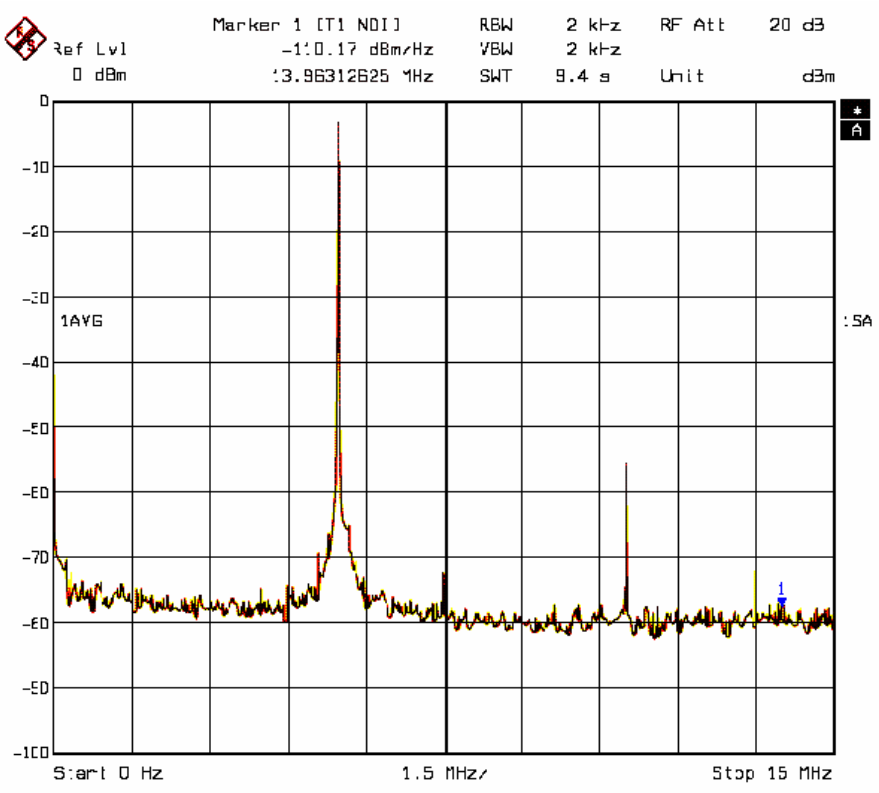


SNR Measurement for ADC

BT



Wi-Fi



64.2 dB at 11MSample/s for the 550 kHz BT signal

59.7 dB at 44MSample/s for the 5.5 MHz 802.11b signal

Comparison Table

	[1]		[2]		This design	
	BT	WiFi	BT	WiFi	BT	Wi-Fi
Receiver Architecture	Low-IF	DCR	Low-IF	DCR	DCR	DCR
Offset cancellation	Programmable loop		Injection at AGC input		AC coupling	
Channel select filter	separate		programmable		Programmable	
Baseband amplifier	separate		shared		Shared	
ADC	Not included		Not included		Included	
Filter bandwidth	1MHz (BPF)	7.5MHz (LPF)	1MHz (BPF)	7.5MHz (LPF)	600kHz (LPF)	6MHz (LPF)
Sensitivity	-82dbm	-88dBm	-80dBm	-92dBm (0dB SNR)	-91dBm	-86dBm
Technology	0.35 μm CMOS		0.18 μm CMOS		0.25μm BiCMOS	
Rx active current	46mA	65mA	60mA		27.9mA (w/o ADC)	30mA (w/o ADC)
ADC active current	-	-	-	-	13.4mA	15.6mA
IIP3	-7dBm	-8dBm	-12dBm		-13dBm	
IIP2	N/A	N/A	20dBm		10dBm	
Rx area (w/ pads)	N/A		16mm^2 (transceiver)		9mm^2 (w/o ADC)	
ADC area (w/ pads)	-	-	-	-	10mm^2	
Supply voltage	2.7V		1.8V		2.5V	

Summary

- Direct conversion architecture for BT / Wi-Fi allows maximum level of block sharing
- Lower consumption than previous dual-mode implementations (27.9 mA / 30mA)
- Shared RF front-end and programmable baseband components
- Programmable channel selection filter with constant linearity
- AC coupled VGA with constant output offset
- On-chip time interleaved pipeline ADC