

NBTI

A “New” Transistor Reliability Degradation Mechanism

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Agenda

- Introduction
- Mechanism/Kinetics
- Process Dependence
- CHC vs NBTI
- NBTI Impact on Digital Circuit Reliability
- Summary

Transistor Reliability Care-abouts

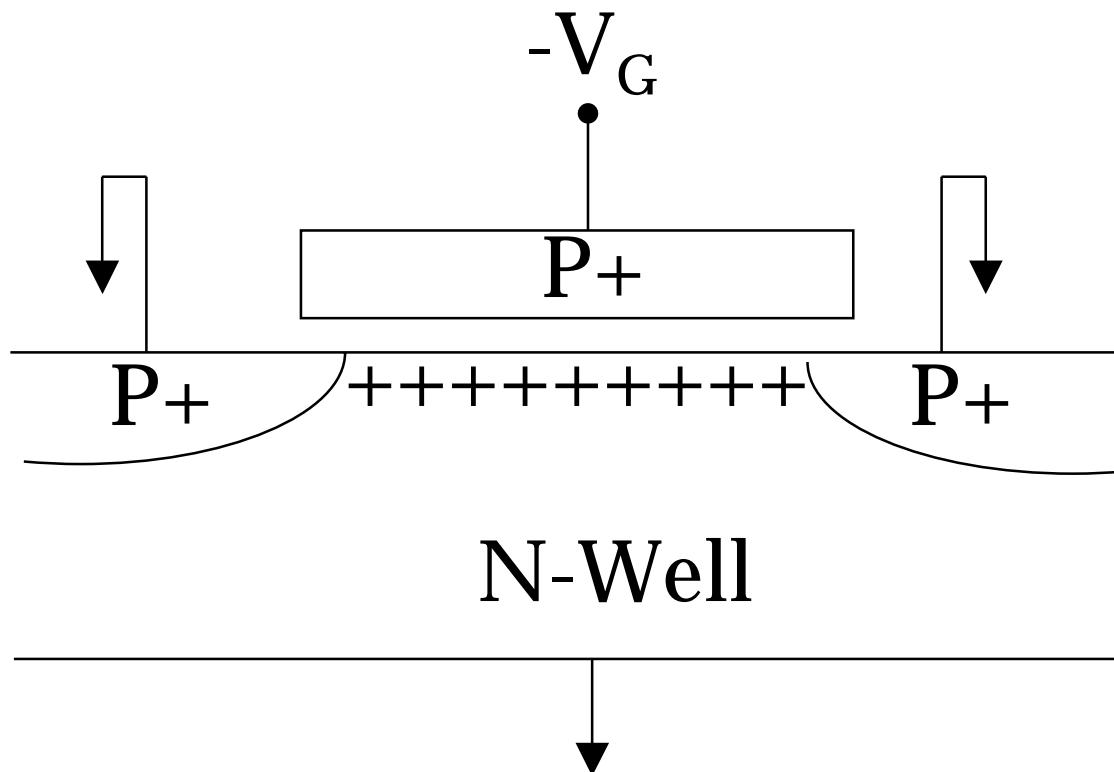
- Electrostatic Discharge (ESD)
 - Very high current induced damage
- Latchup
 - High current (overstress) causing functional or hard failure
- Channel Hot Carrier (CHC) Degradation
 - High-energy (“Hot”) carriers degrading Si/SiO₂ interface
 - Studied intensively during the 1980’s and 90’s
 - CHC degradation well-understood
 - Process: LDD, Drain Junction Engineering
 - Circuit: Design Guidelines
- **Negative Bias Temperature Instability (NBTI)**
 - **Gaining a lot of attention in the last few years...**

NBTI Background

- NBTI is not a “new” phenomenon
 - NBTI first studied in 1967 (B. Deal et. al.)
 - Intensively studied in the early 1970’s and eventually “solved” through gate oxide improvements
- The “instability” in NBTI refers to transistor parameter (I_{dsat} , V_{th} , etc.) shift observed in a transistor when a negative gate bias is applied.

NBTI Background

- NBTI Biasing Configuration
 - pMOS biased in inversion (holes at surface)



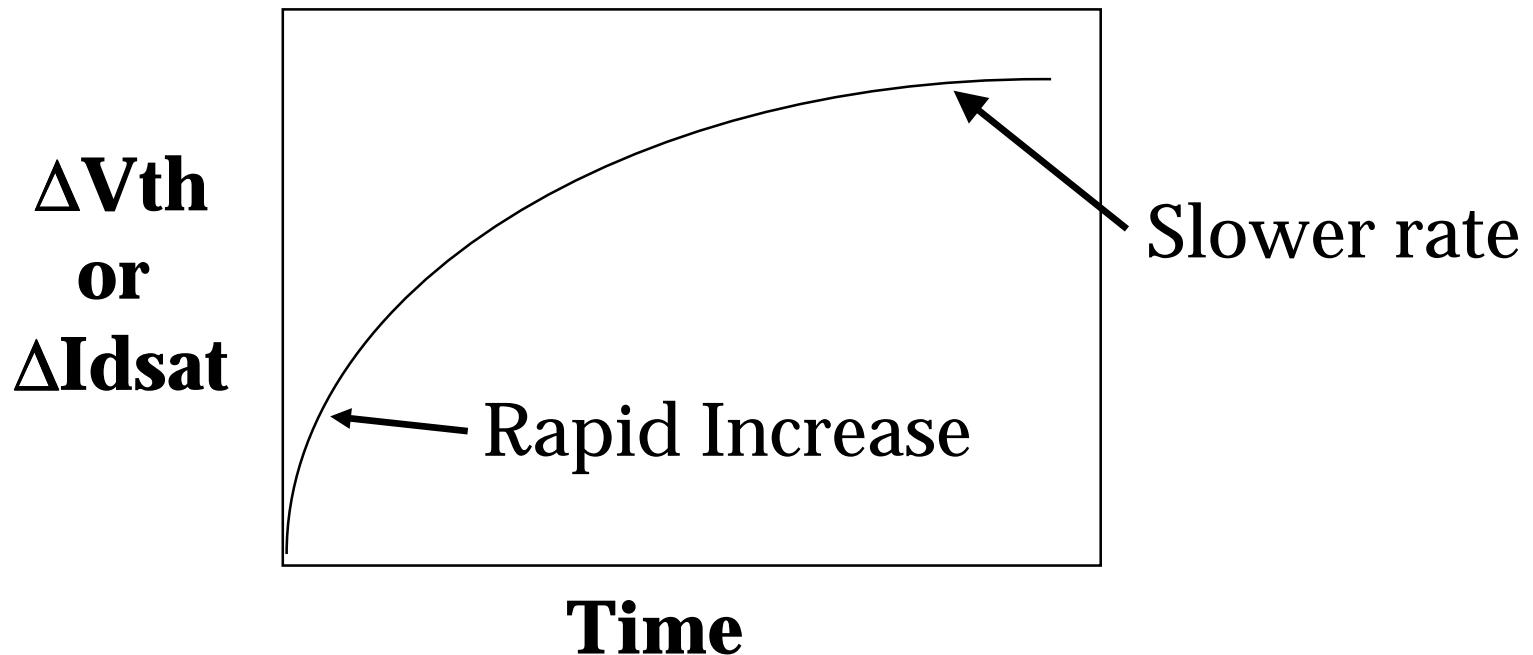
NBTI Background

Necessary ingredients for NBTI:

- Holes at Si/SiO₂ interface (pMOS in inversion)
 - Hydrogen species
 - Molecular or Atomic hydrogen
 - Moisture (i.e., Water)
 - High temperature (> 100C)
 - Oxide voltage/field
-
- Is an oxide degradation phenomenon
 - Similar to gate oxide wearout but degradation metric is transistor parametrics

NBTI Background

- Parametric manifestation of NBTI damage
 - Id_{sat} decrease
 - V_{th} increase
 - Transistor gets “colder”

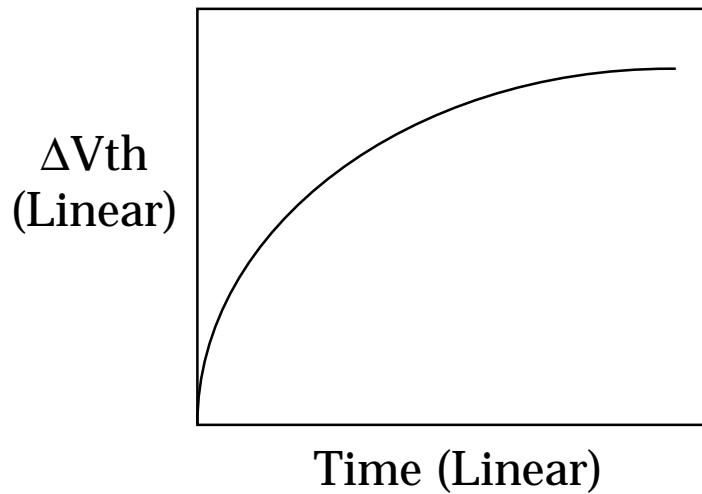


NBTI Time Dependence

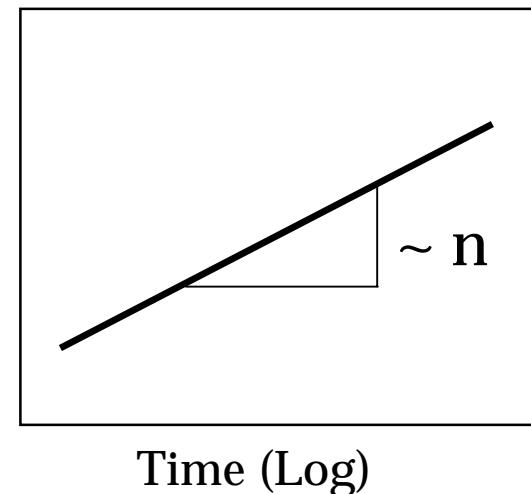
NBTI Drift tends to follow a power-law time dependence

- $\Delta V_{th} = A * t^n$ with $n \sim 0.2$ to 0.3

ΔV_{th} vs Time



ΔV_{th} vs Time

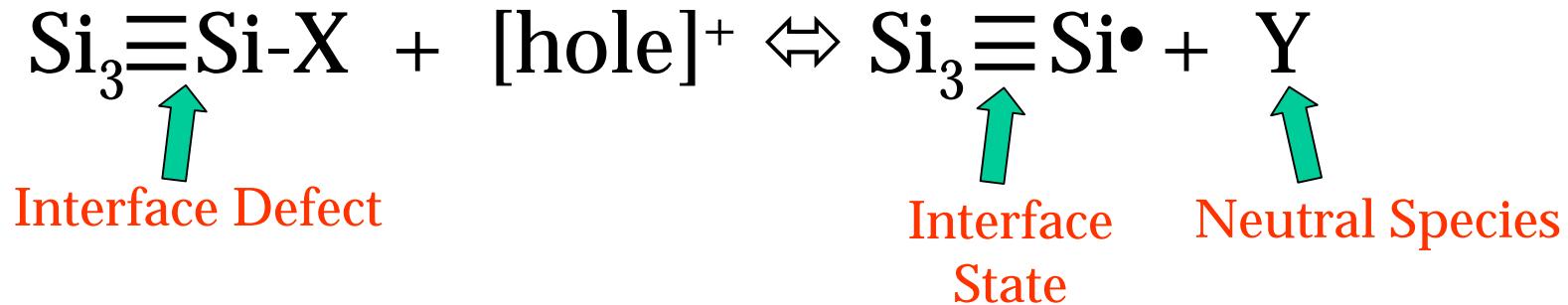


- Impact of $n \sim 0.25$
 - I.e., for $n = 0.23 \Rightarrow 2X \Delta V_{TH}$ requires $20X$ time increase
 - Low values of n give rise to “saturating” behavior

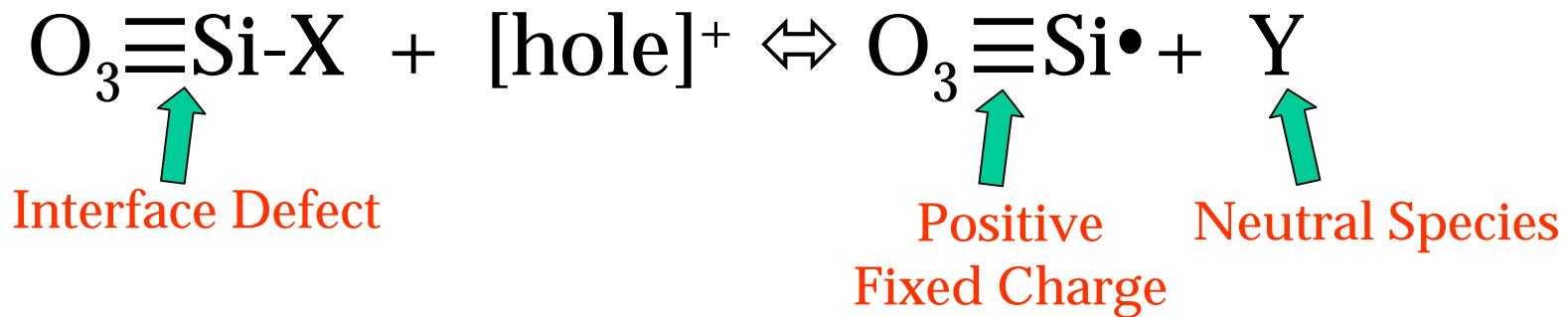
NBTI Mechanism

Electrochemical Reaction

1) Interface State Generation, N_{it}



2) Positive Oxide Fixed Charge Generation, N_f



(Yamamoto et. al. TED-46, 1999)

NBTI Kinetics

Several Models Exist in the Literature

1) Ogawa et. al (JAP-77, 1995)

$$\Delta V_{th} = \frac{q(\Delta N_{it} + \Delta N_f)}{C_{ox}}$$
$$\Delta N_{it}(E_{ox}, T_{ox}, T, t) = \frac{BE_{ox}^{3/2} t^{0.25} e^{-E_a/kT}}{T_{ox}}$$
$$\Delta N_f(E_{ox}, T, t) = CE_{ox}^{3/2} t^{0.14} e^{-E_a/kT}$$

2) LaRosa et. al. (IRPS-1997)

$$\Delta I_{ds} = A * e^{-E_a/kT} * e^{\gamma/V_g} * t^{0.2}$$

3) Liu et. al. (IRW-2000)

$$\Delta V_{th} = A * e^{-E_a 0.34/kT} * E_{ox}^3 * t^{0.37}$$

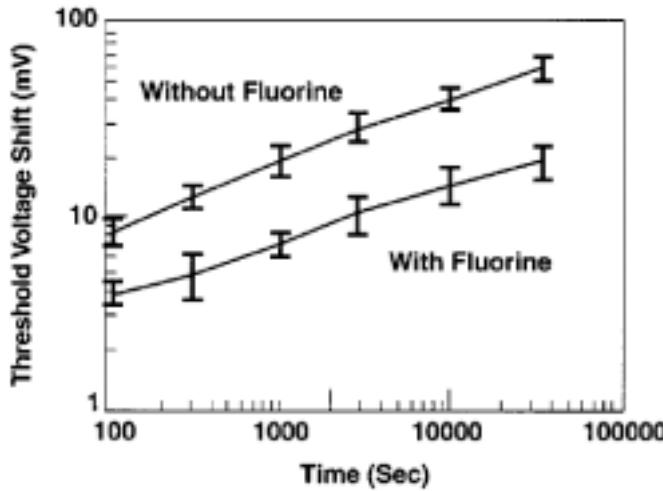
- Very different functional dependence!

NBTI Process Dependence

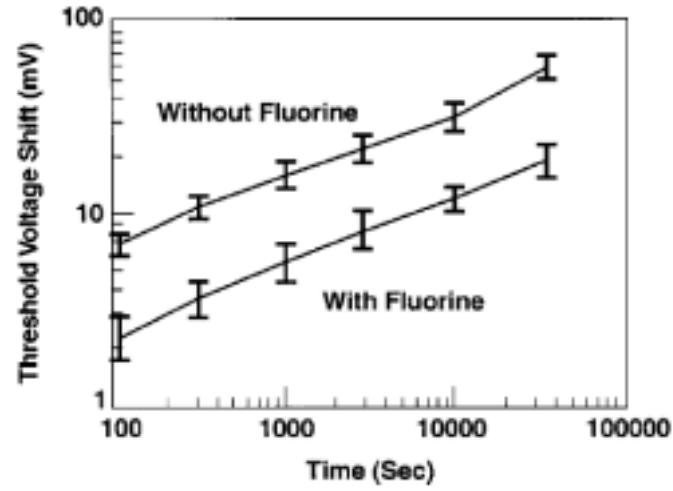
Process knobs known to affect NBTI performance

- Fluorine
 - Can improve NBTI performance
- Nitrided Oxides
 - Tend to degrade NBTI performance
- Deuterium
 - Improve NBTI performance
- Plasma Damage
 - Degrade NBTI performance
 - Most process steps are plasma based – Not a good trend

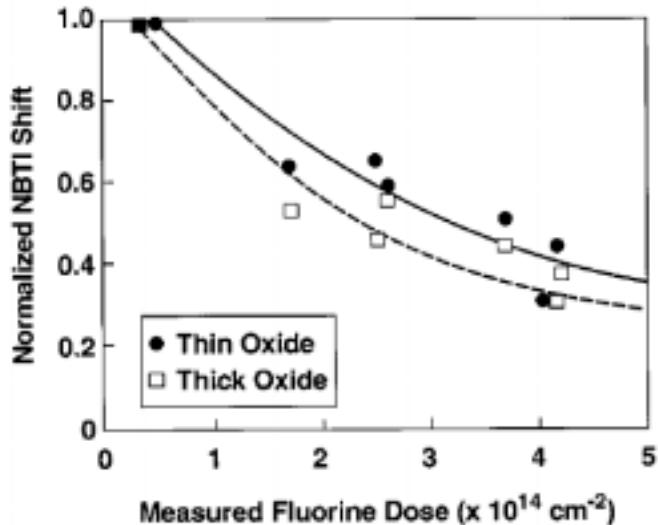
Impact of Fluorine



Thick Oxide $\sim 68\text{\AA}$



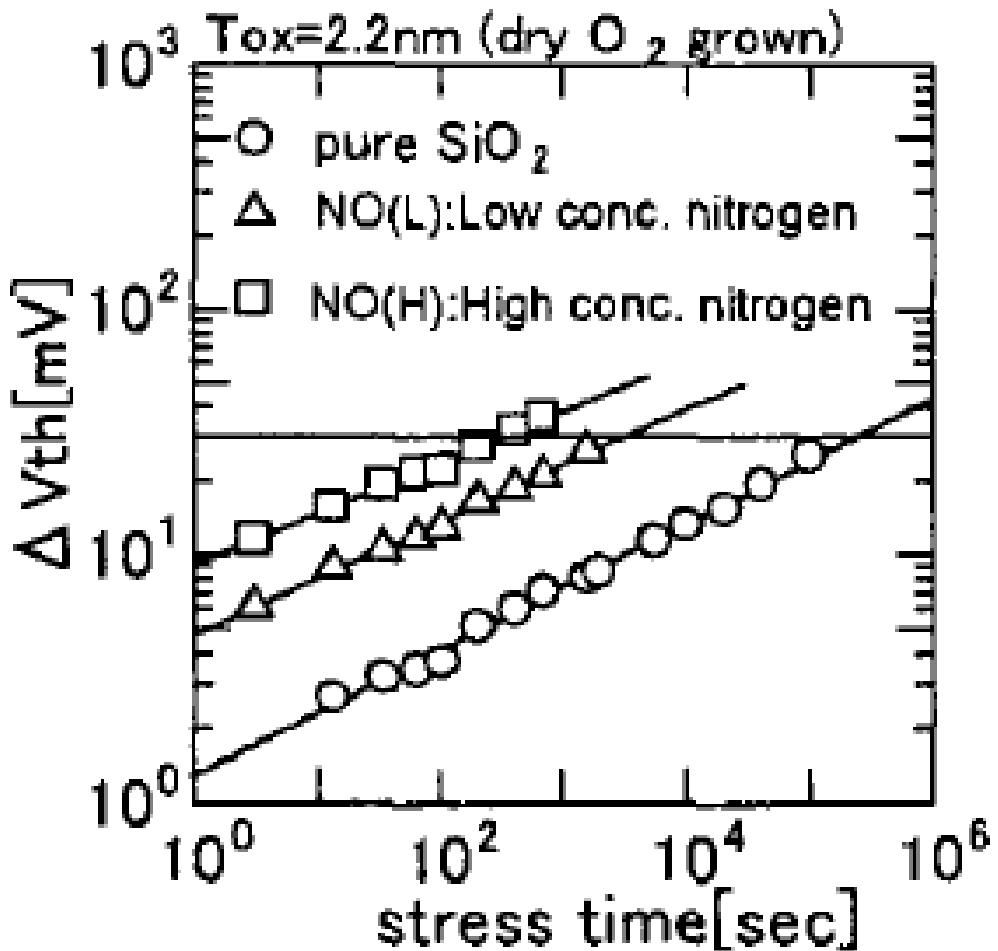
Thin Oxide $\sim 35\text{\AA}$



- BF_2 implant used to introduce fluorine
- Hypothesis for improvement is that fluorine replaces hydrogen related sites that are precursors to interface trap generation.

[T. Hook et. al (IBM), TED-48, 2001]

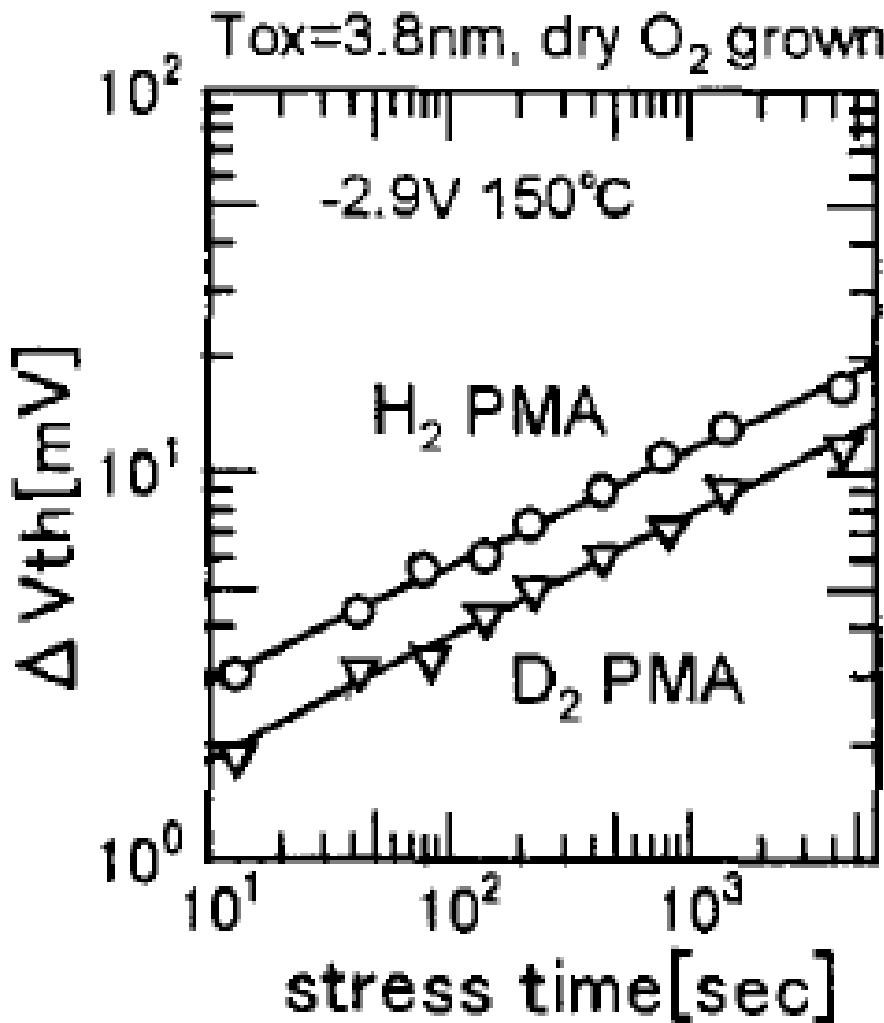
Impact of Nitrided Oxides



(Kimizuka et. al, VLSI Symp.2000)

- Incorporation of nitrogen can degrade NBTI performance

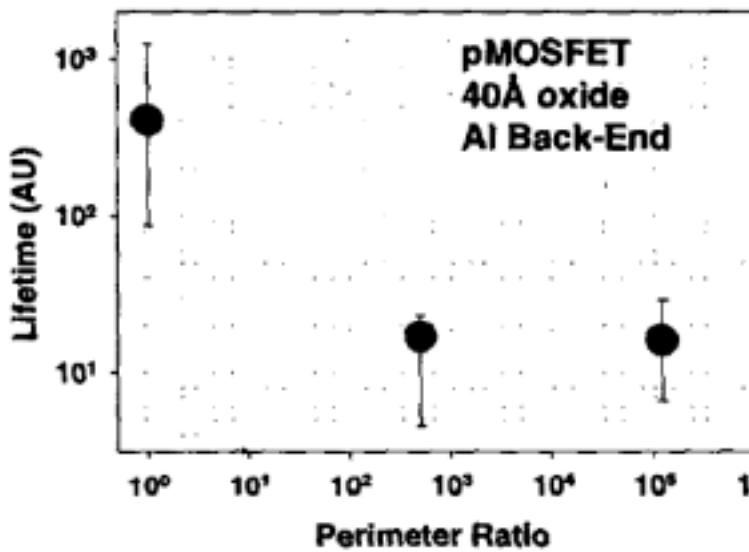
Impact of Deuterium



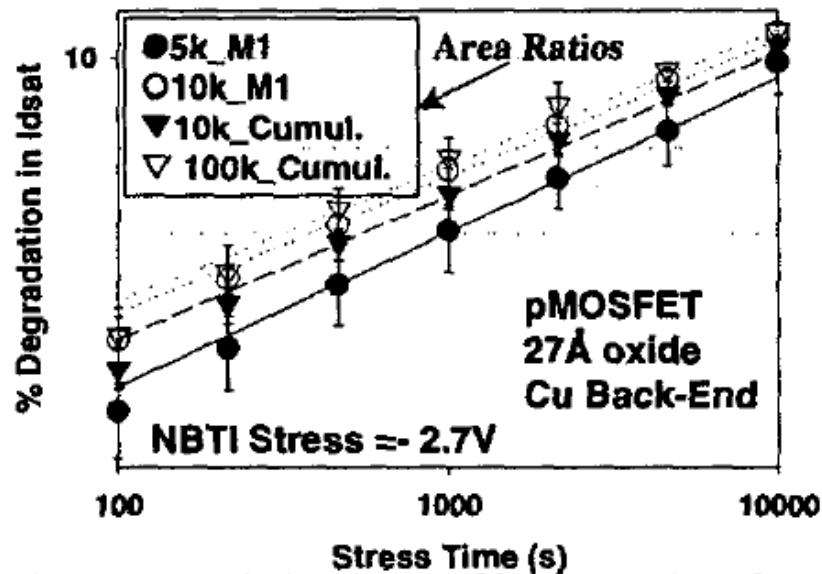
(Kimizuka et. al, VLSI Symp.2000)

- Incorporation of deuterium can improve NBTI performance
 - Harder to generate interface states

Impact of Plasma Damage (Antenna Charging)



Al BEOL

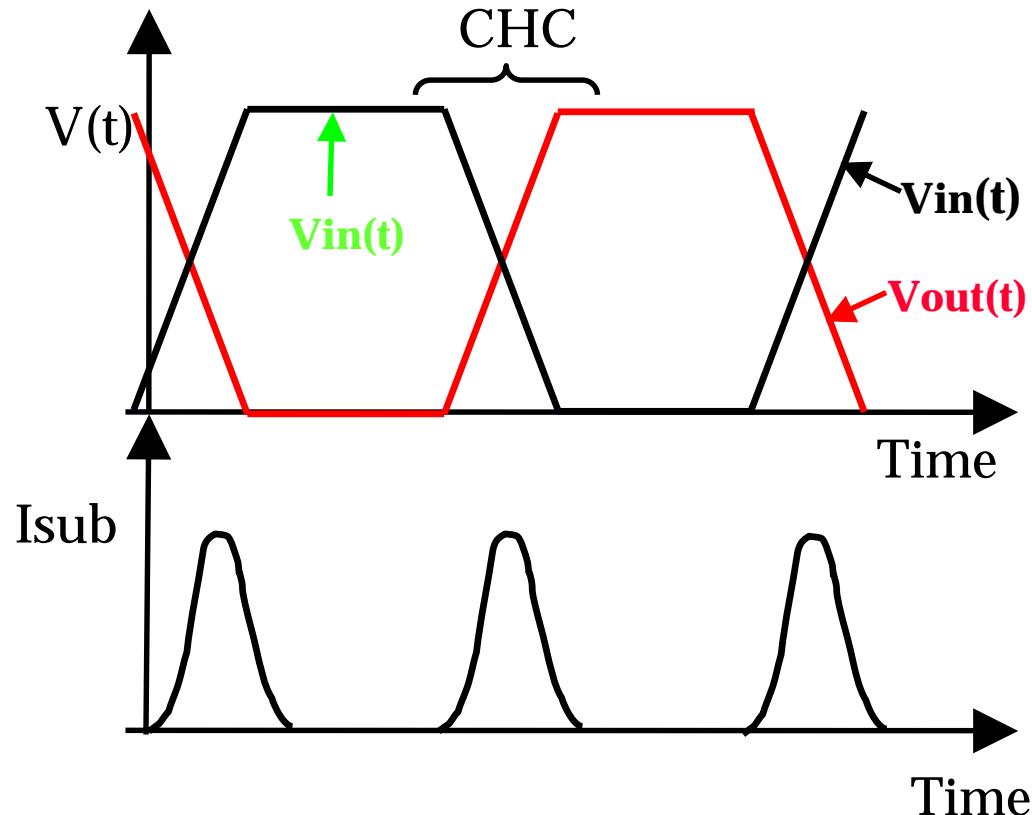
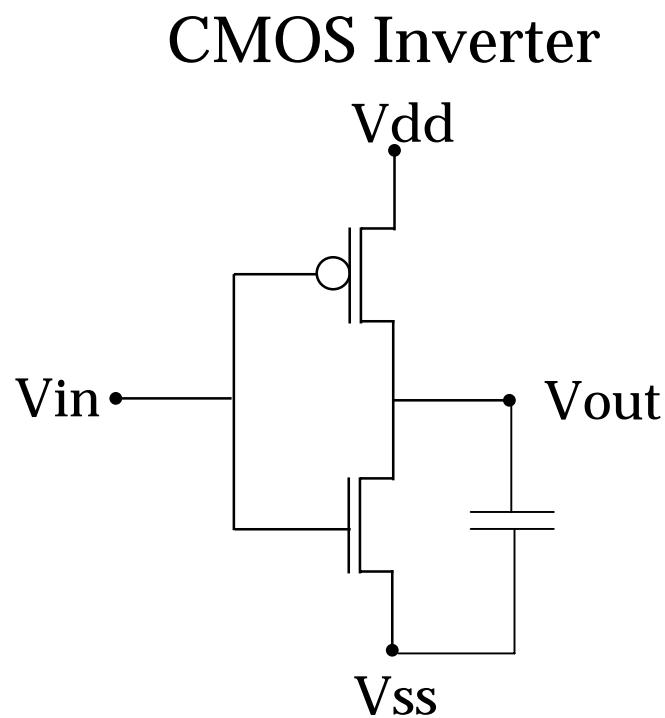


Cu BEOL

[Krishnan et. al (TI), IEDM.2001]

- Increasing antenna ratio increases NBTI degradation
- Plasma damage creates interface states during processing, which are then passivated during forming gas anneal
 - NBTI stress electrically re-activates these latent defects

CHC During Digital Circuit Operation



I_{sub} current is generated only during device switching. To minimize CHC,

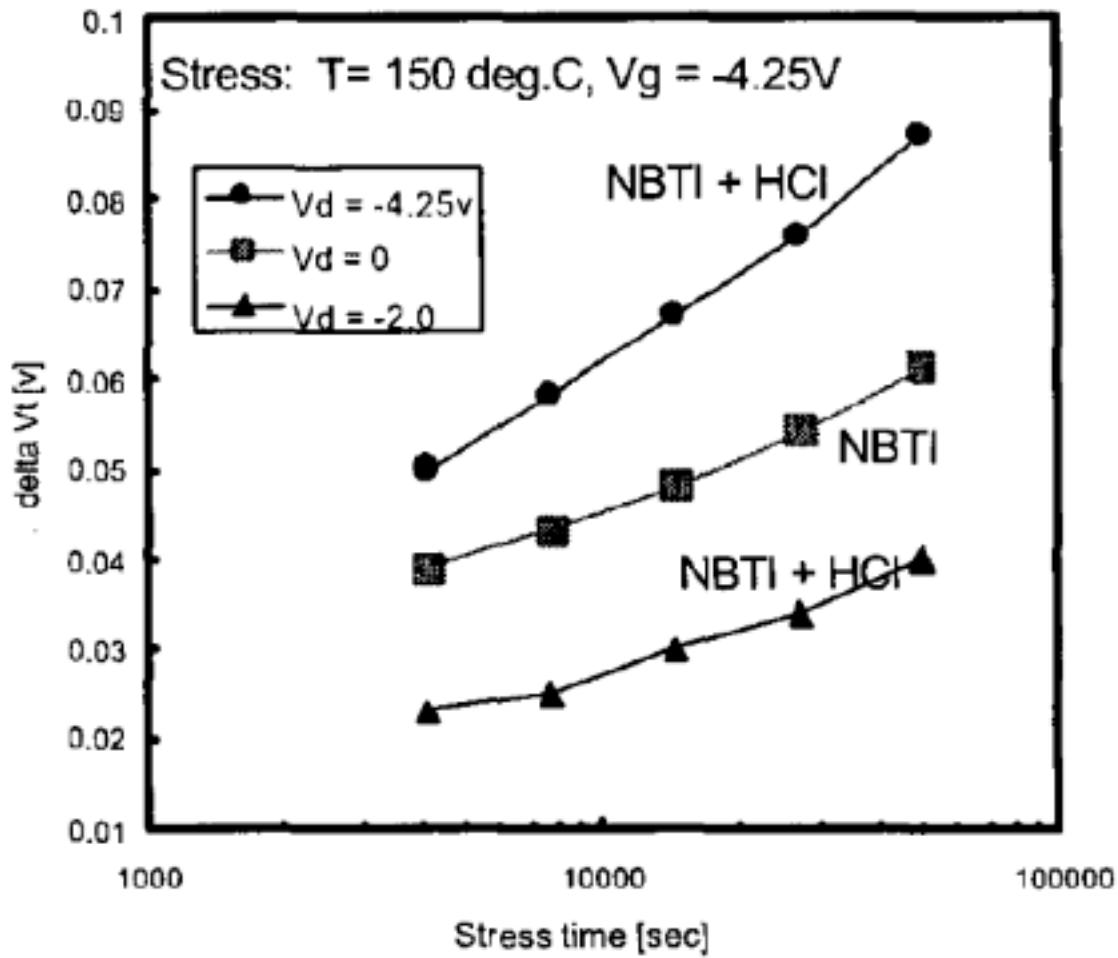
- (1) Reduce slew rate of waveform (larger transistors)
- (2) Reduce load capacitance

Comparison of CHC vs NBTI

Parameter	CHC	NBTI
Gate Length	Strong	Weak ^(*)
Voltage	Strong	Strong
Temperature	Weak	Strong
Duty Cycle	During Transitions	When pMOS is on

(*) – A few reports of strong L_G dependence in literature
• As $L_G \downarrow$, $\Delta V_{TH} \uparrow$

Comparison of CHC vs NBTI



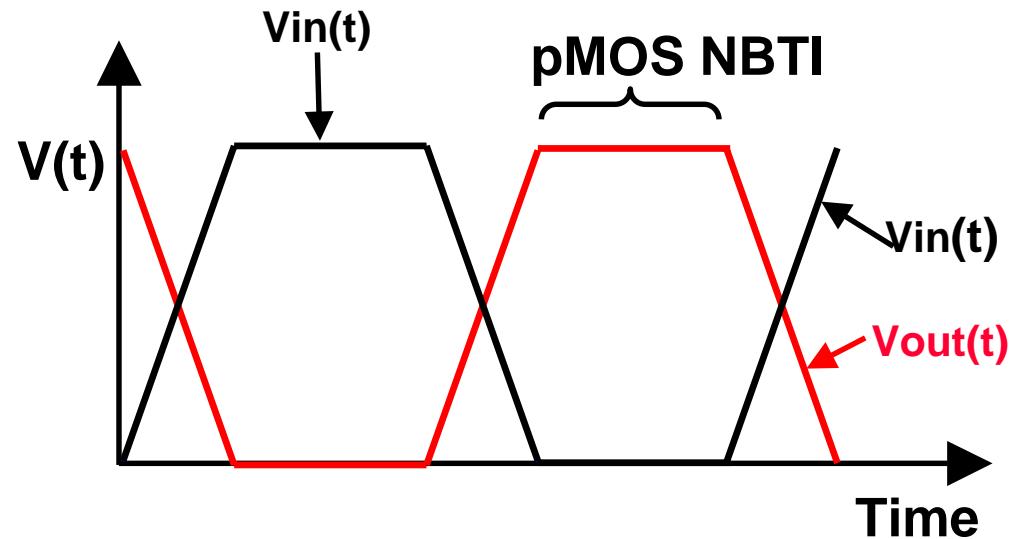
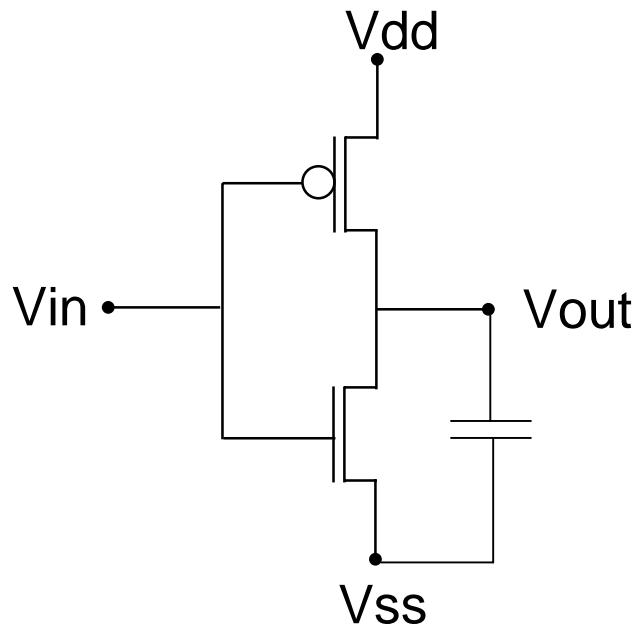
(Chaparala et. al., IRW 2000)

- NBTI + CHC(HCl) Degradation > NBTI Degradation Only

Impact of NBTI On Digital Circuit Reliability

NBTI During Digital Circuit Operation

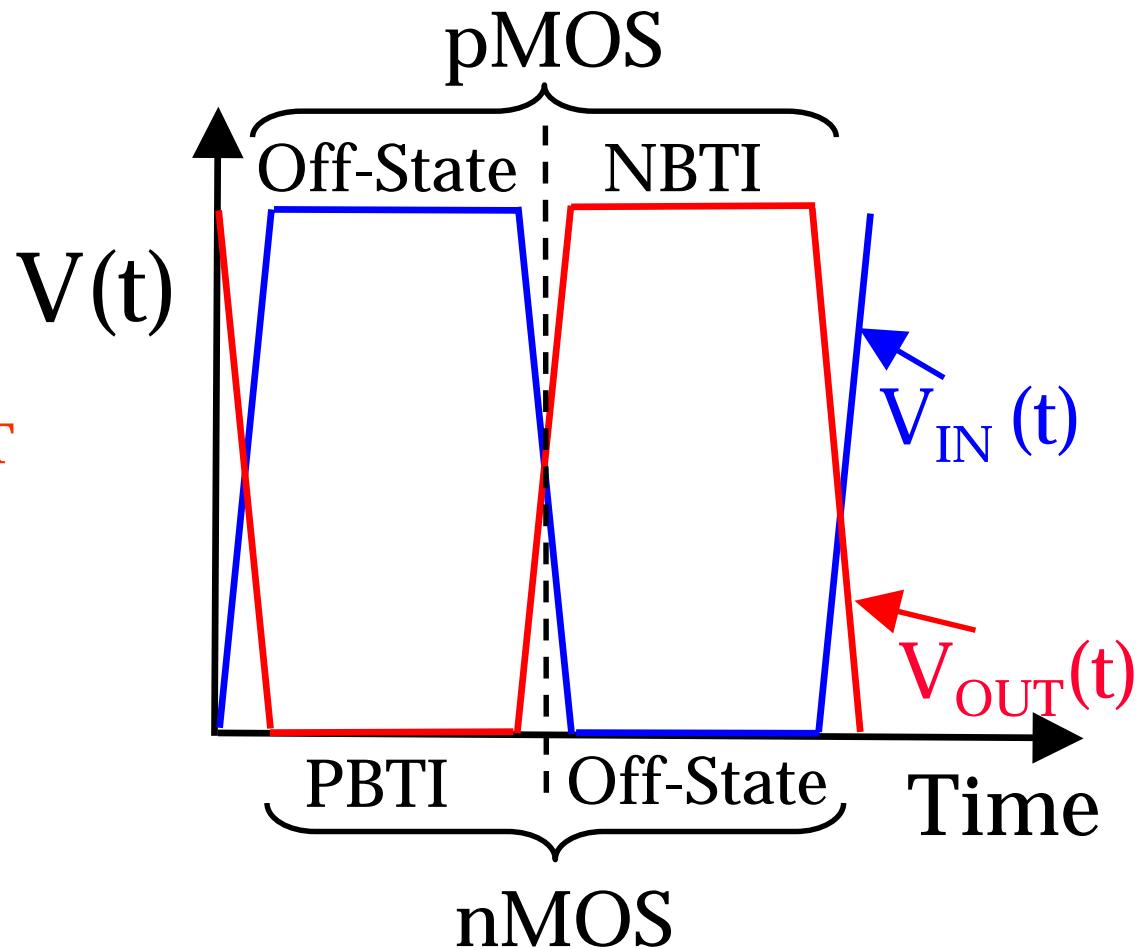
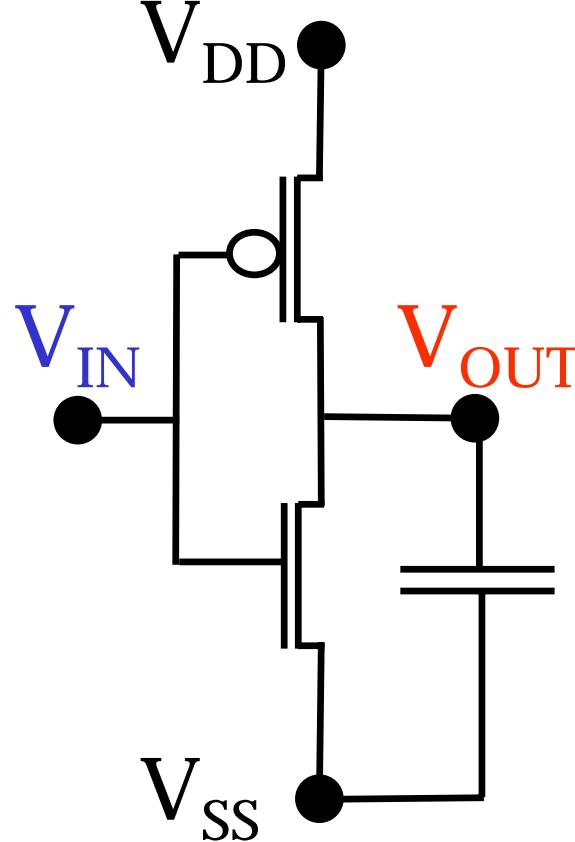
CMOS Inverter



pMOS NBTI occurs when the pMOS transistor fully charges up the inverter load

- $V_g=0V$, $V_d=V_s=V_{nwell}=V_{dd}$
or
- $V_g=-V_{dd}$, $V_d=V_s=V_{nwell}=0V$

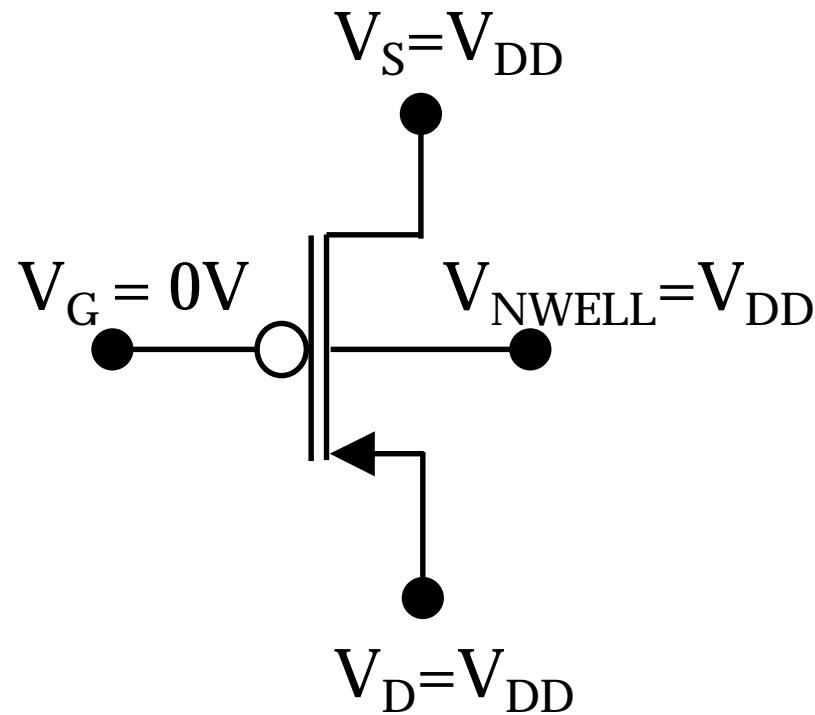
Static CMOS Inverter Degradation



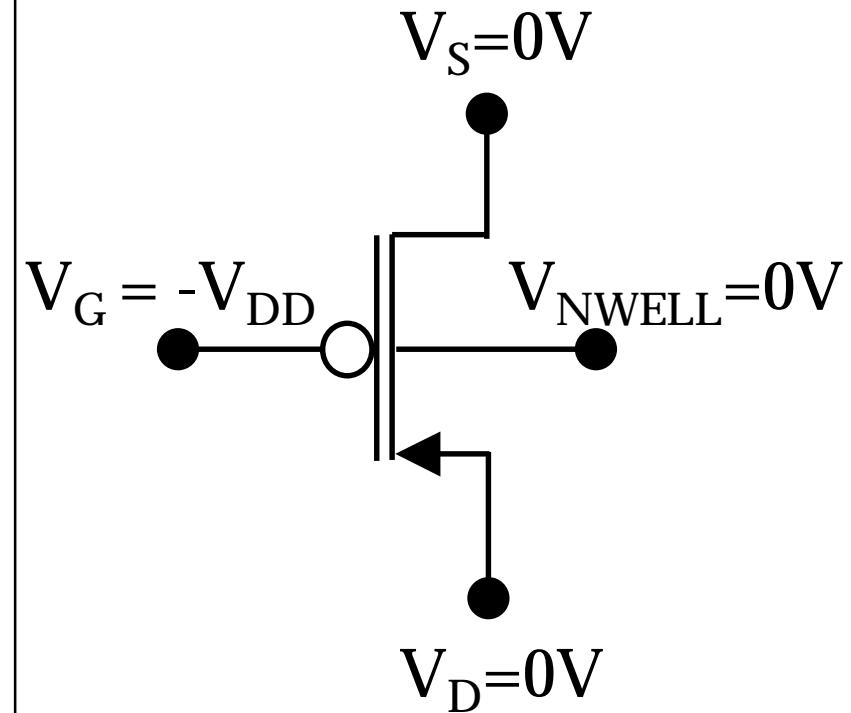
- Two possible degradation modes

pMOS NBTI Testing

Circuit Biasing

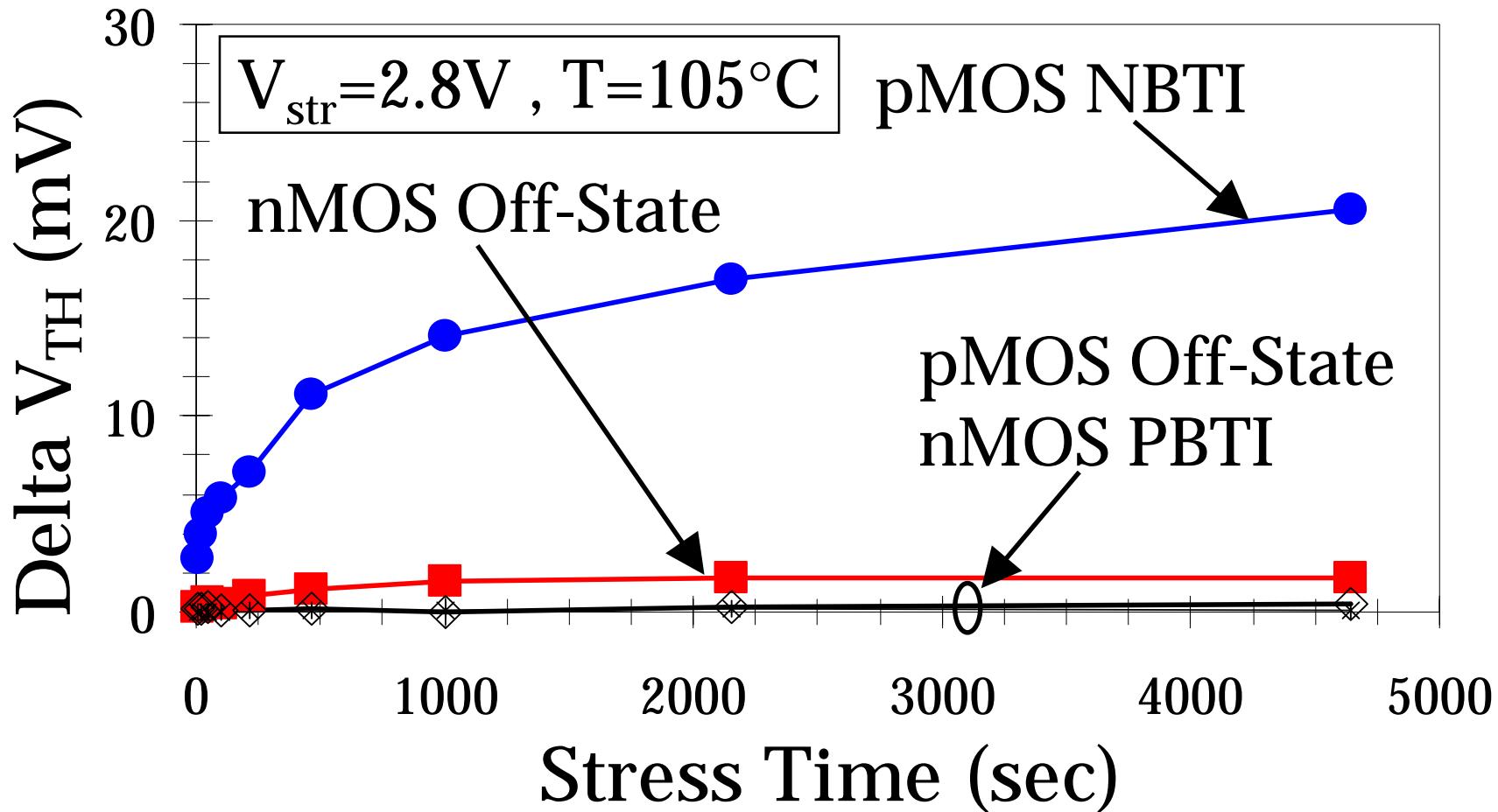


Discrete Transistor Biasing



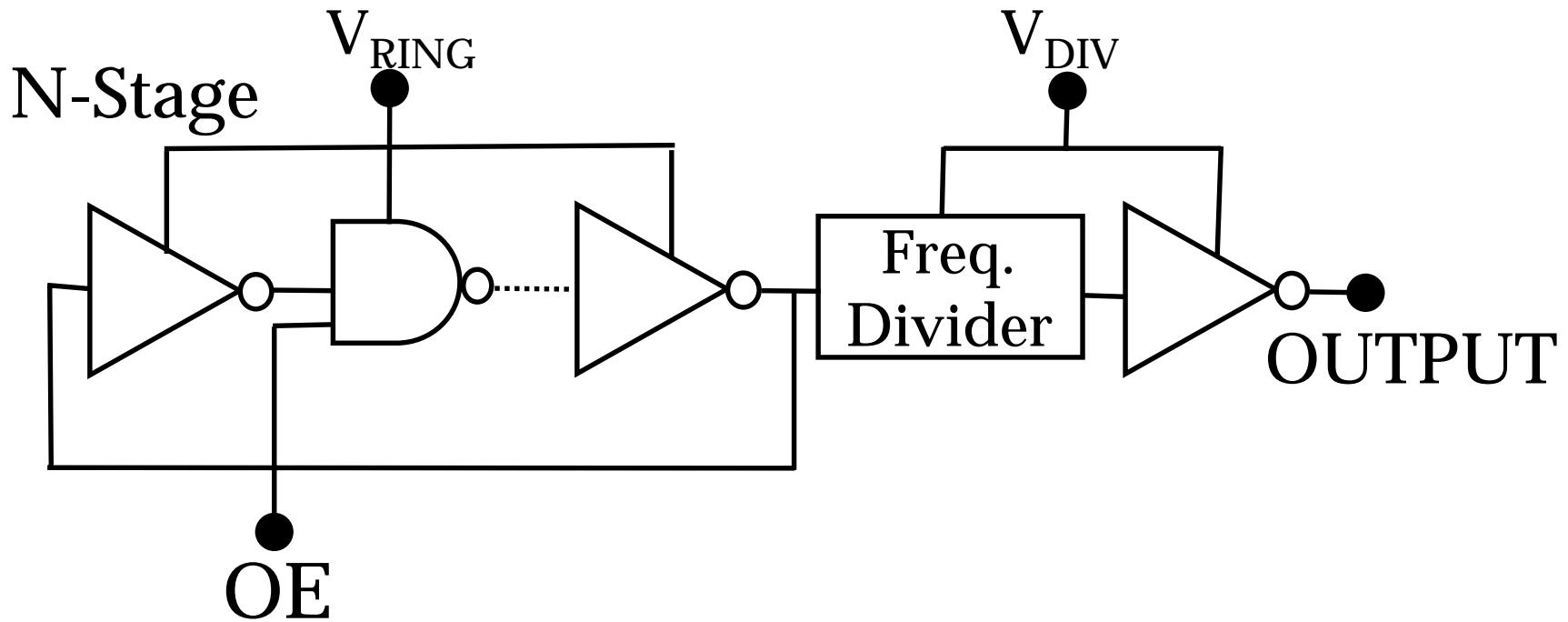
pMOS - Inverter \longleftrightarrow pMOS - Device

Inverter Static Stress: V_{TH} Drift



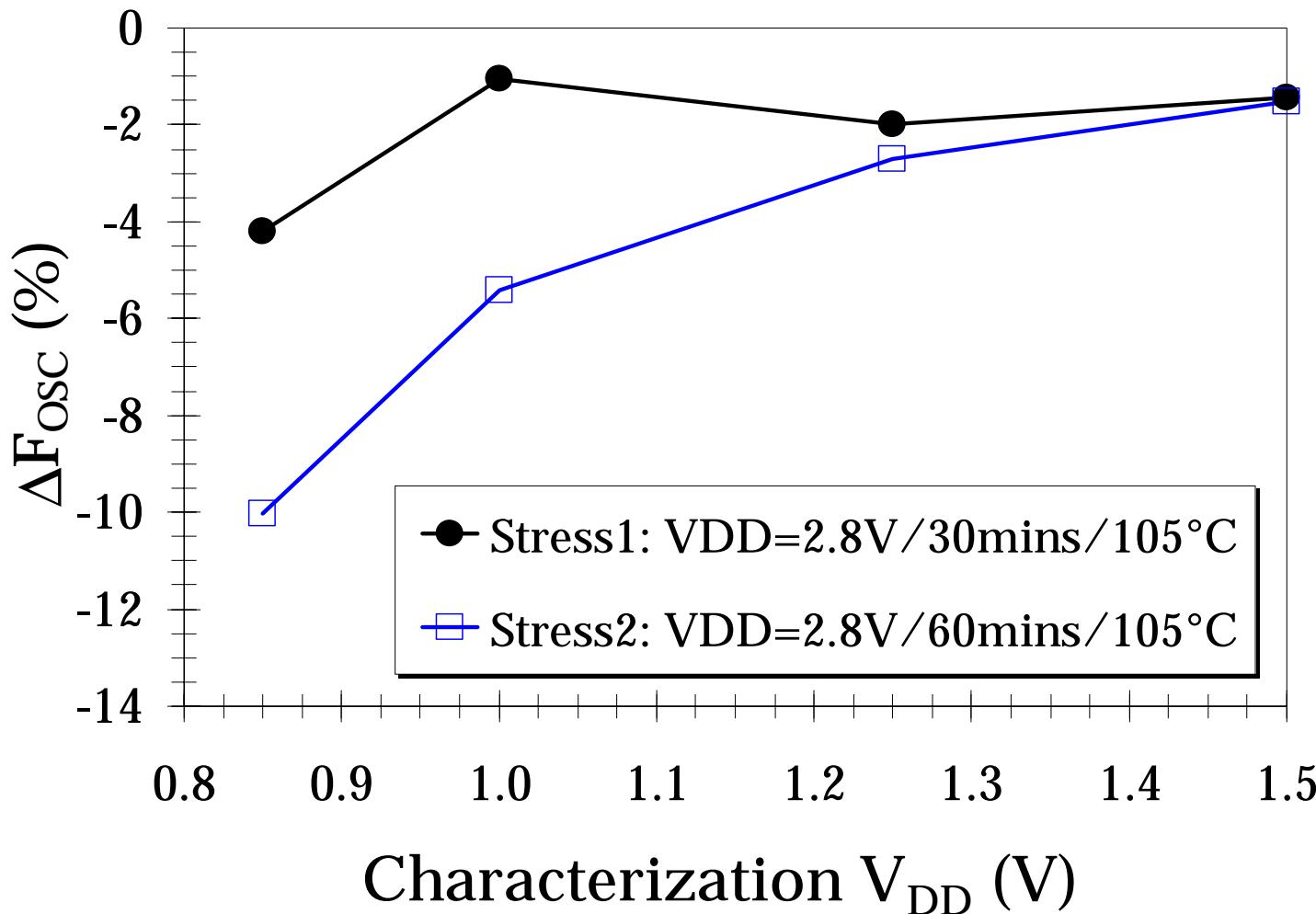
- pMOS NBTI degradation dominant

Ring Oscillator Schematic



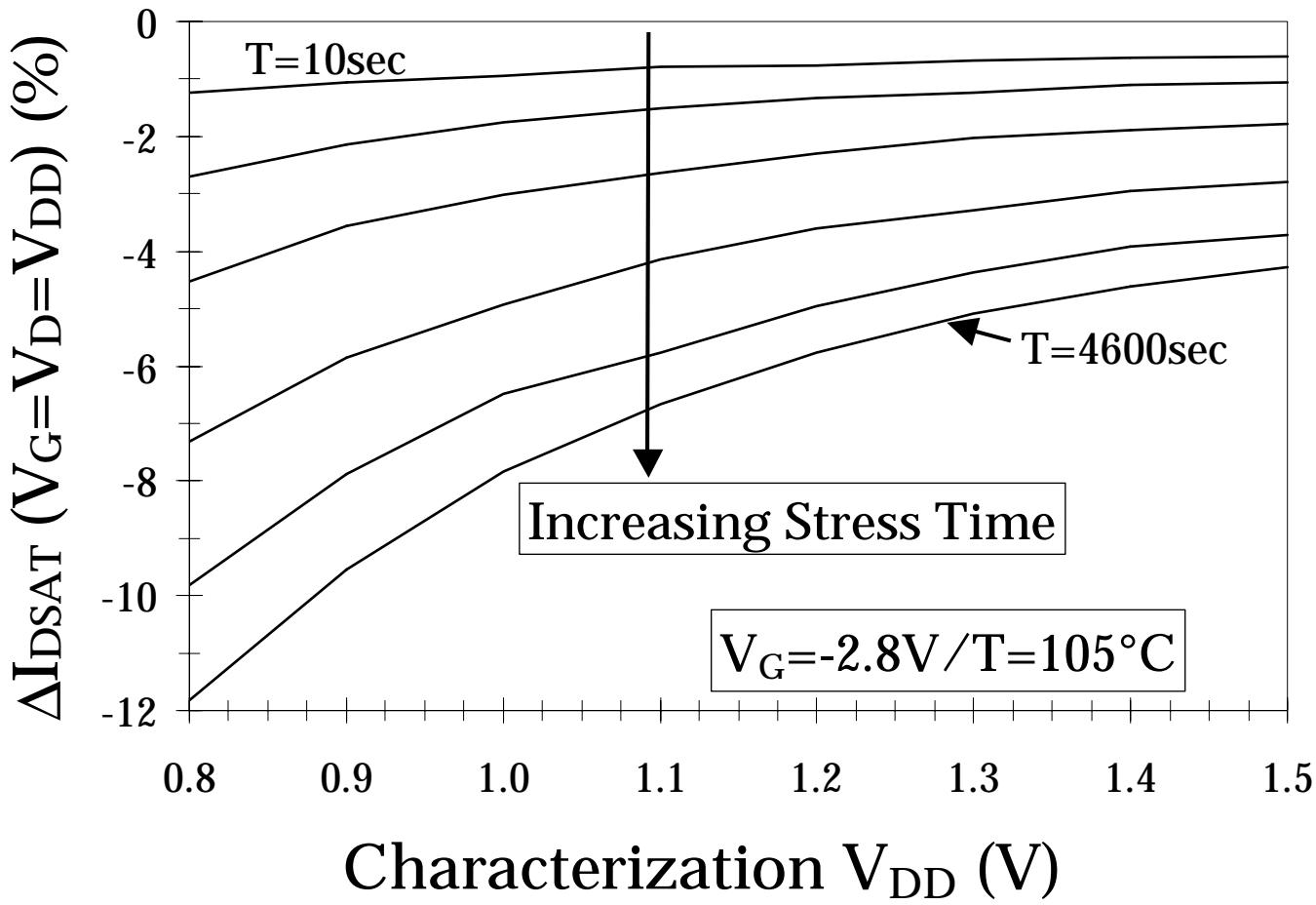
- $OE=0V$ enables static stress
→ Dominated by pMOS NBTI

NBTI Induced Frequency Drift



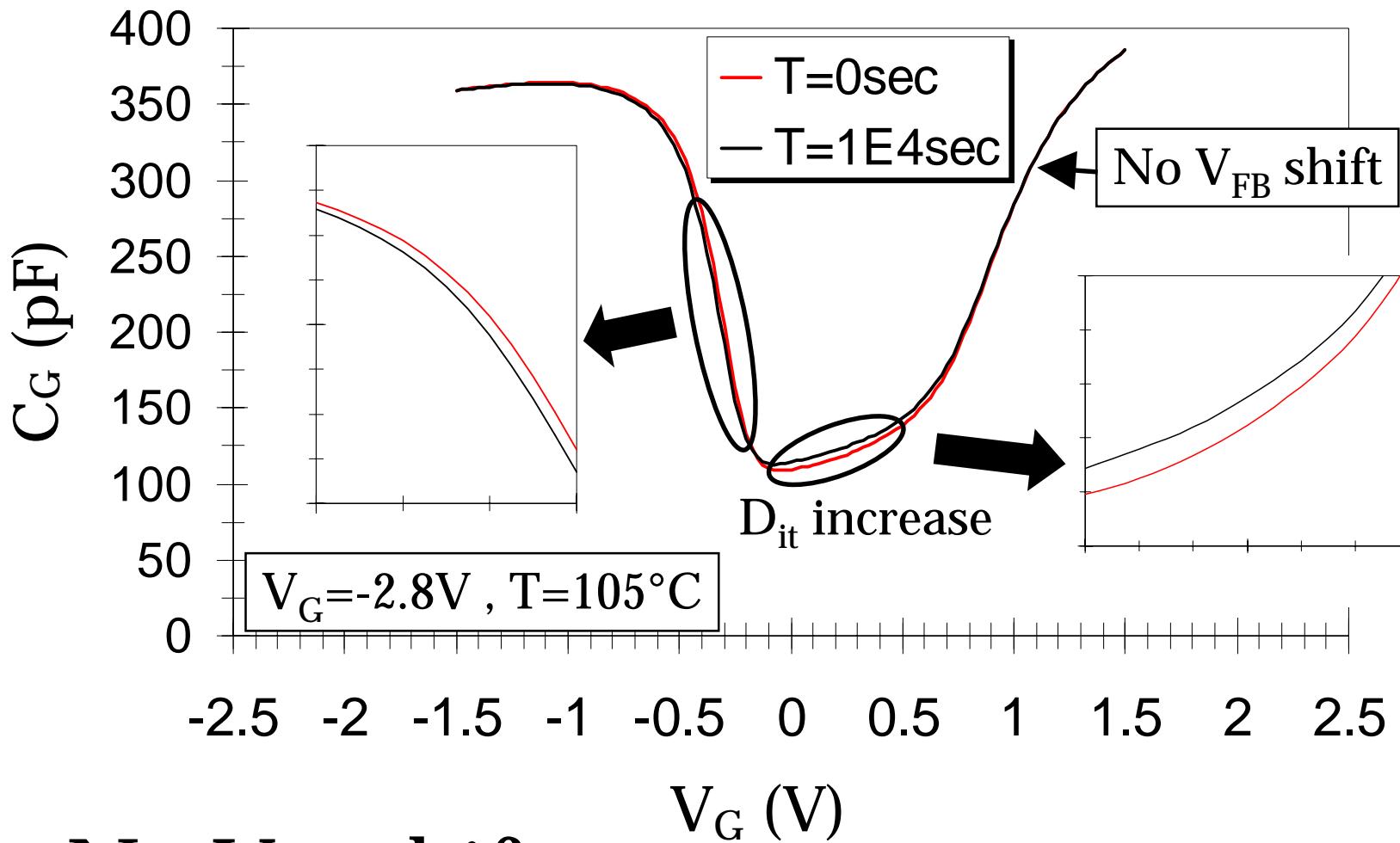
- $\Delta F_{OSC} \uparrow$ as $V_{DD} \downarrow$

NBTI Induced Transistor Drift



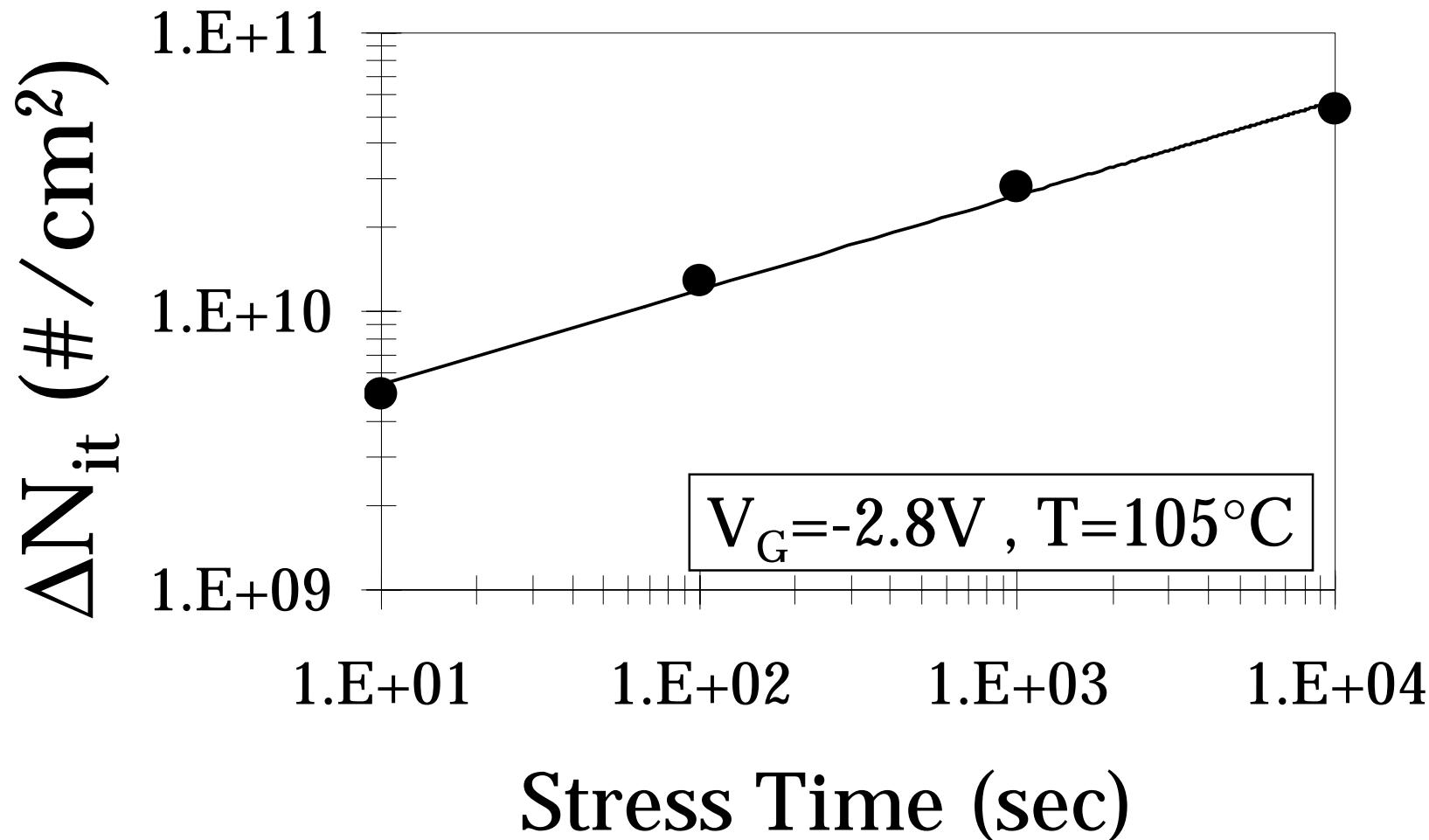
- $\Delta I_{DSAT} \uparrow$ as $V_{DD} \downarrow$
- Reduced Gate Overdrive ($V_G - V_{TH}$)

Capacitance – Voltage Characteristics



- No V_{FB} shift
- D_{it} increases with NBTI stress

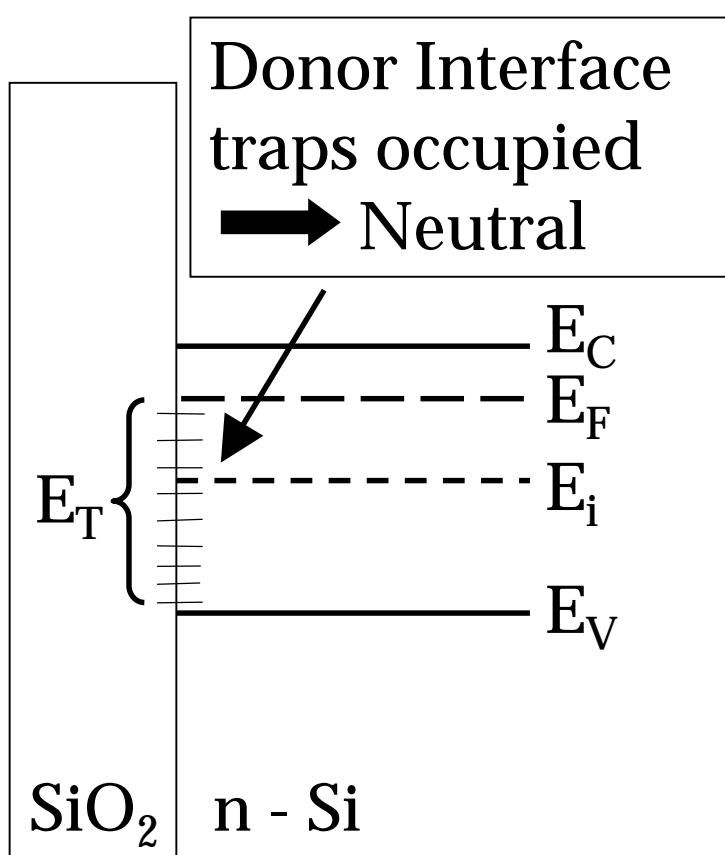
Interface State Density Increase with NBTI



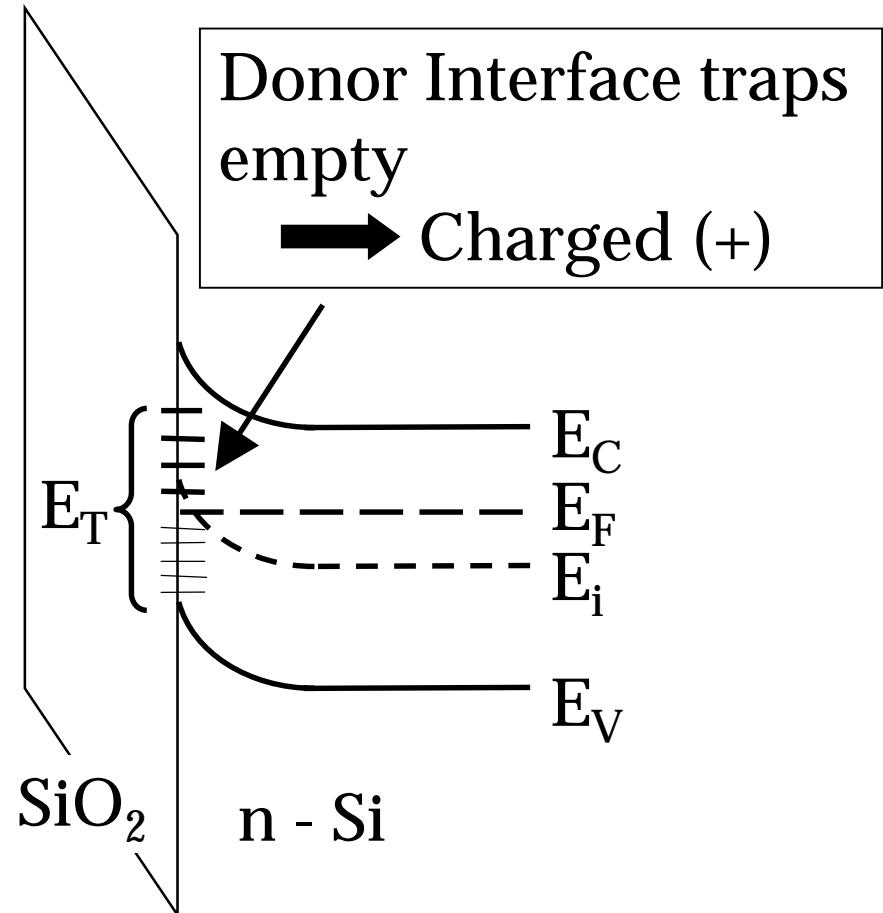
- D_{it} increase confirmed with Charge Pumping measurements

Impact of Donor Interface Traps

$V_G \sim V_{FB} > 0$ (Flatband)

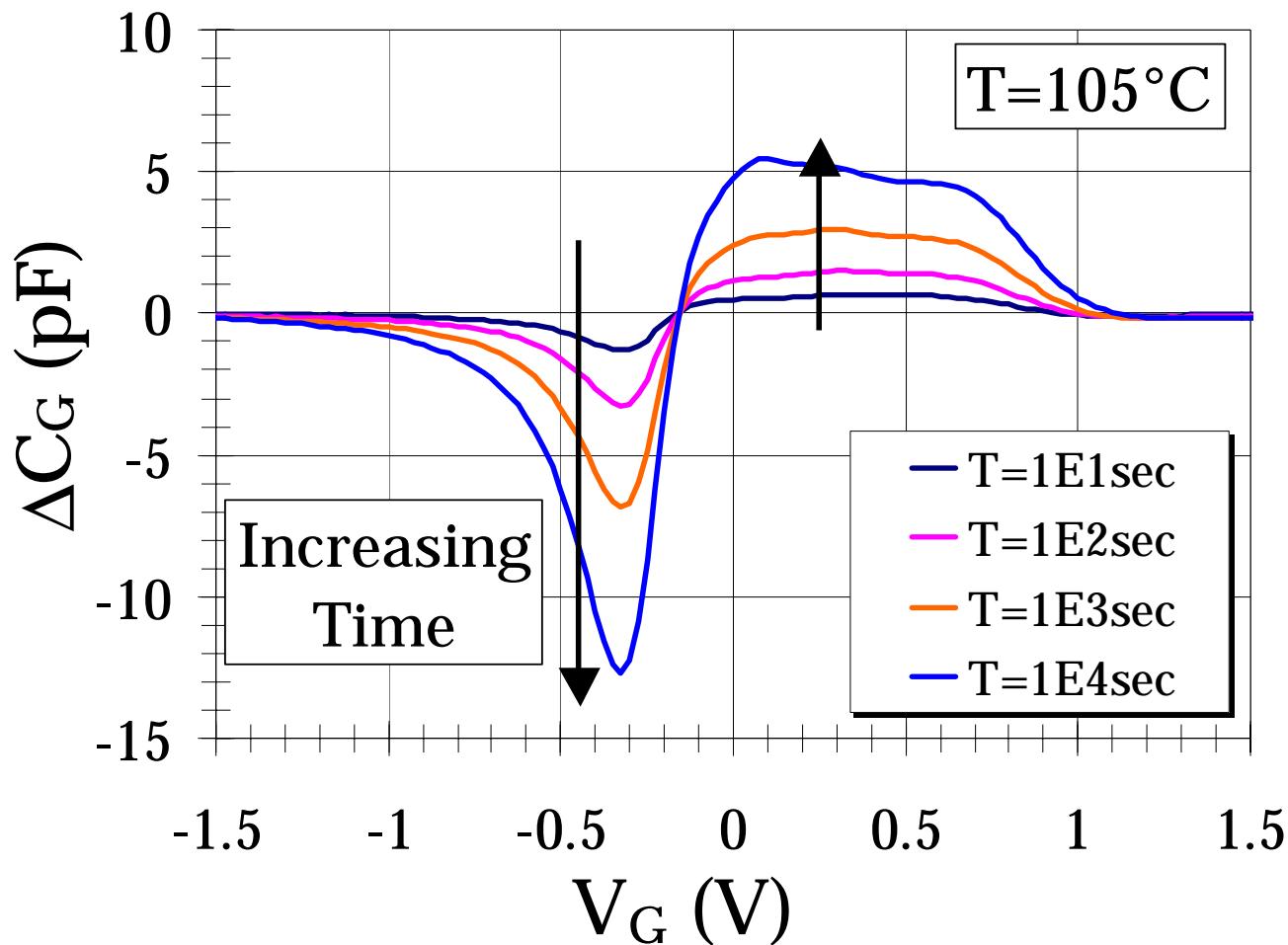


$V_G < V_{FB}$



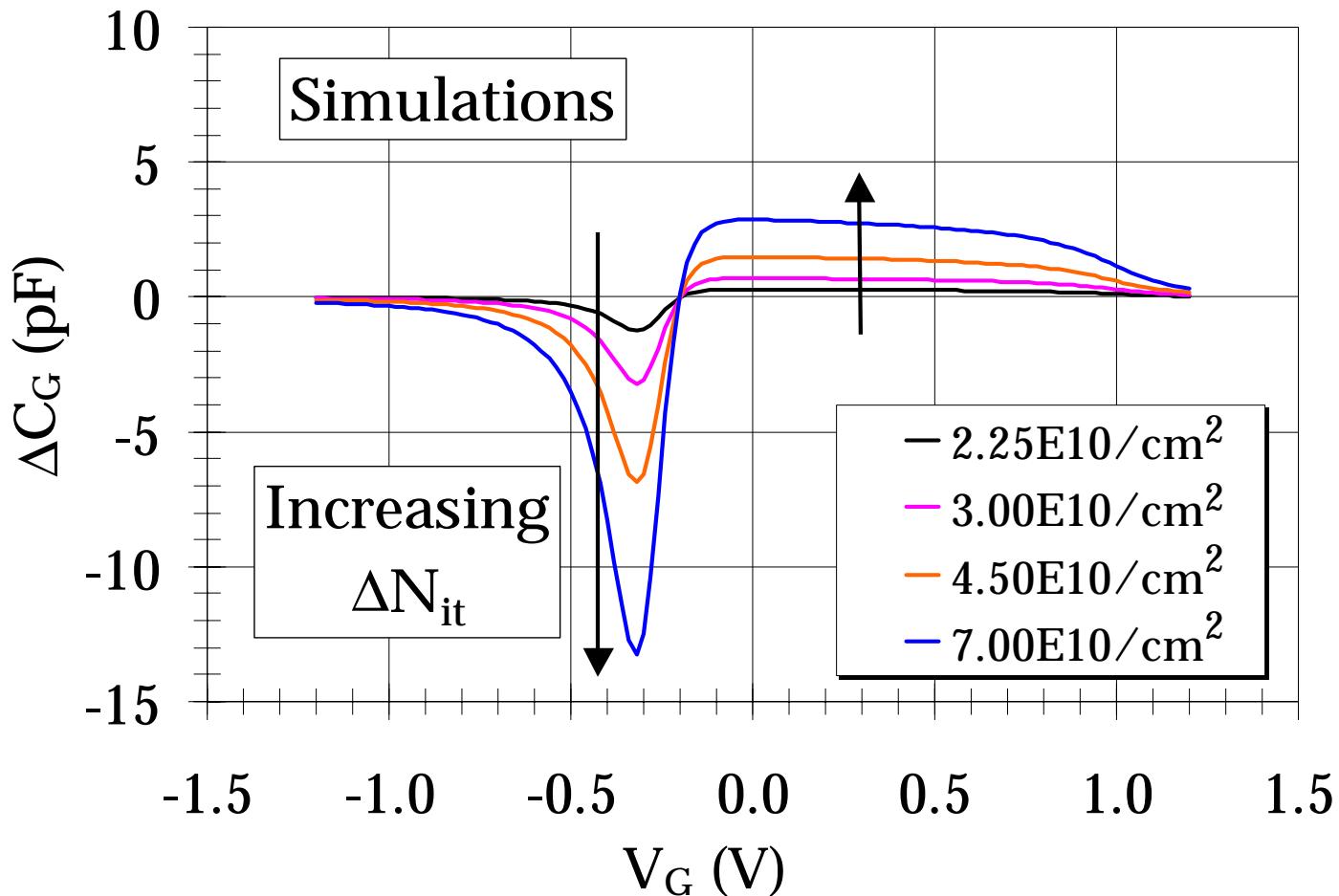
- Bias dependent trap occupancy

Experimental ΔC_G vs V_G Characteristics



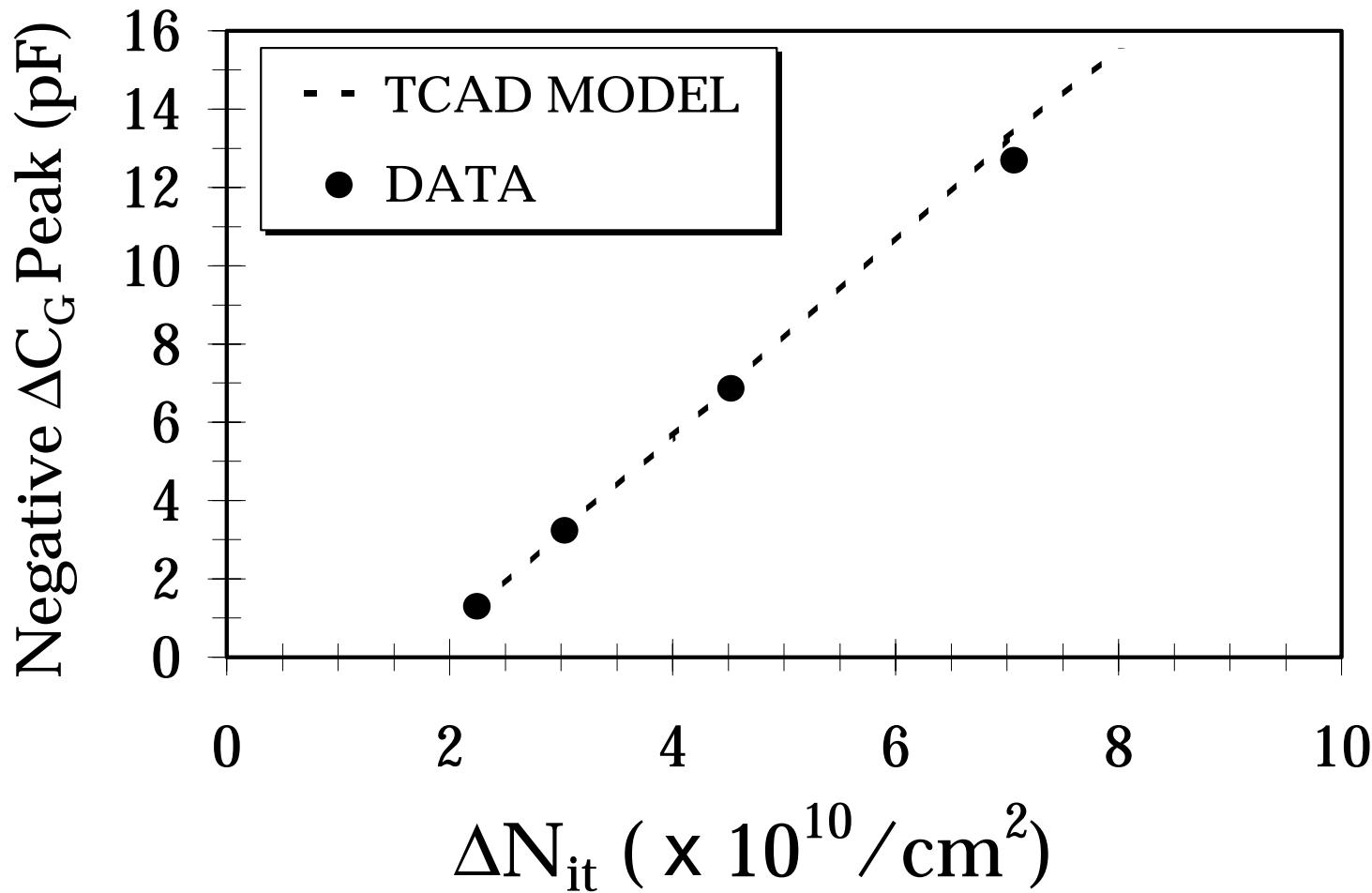
- $\Delta C_G > 0$: D_{it} contribution
- $\Delta C_G < 0$: Lateral shift from D_{it}

TCAD Simulated $\Delta C_G - V_G$ Characteristics



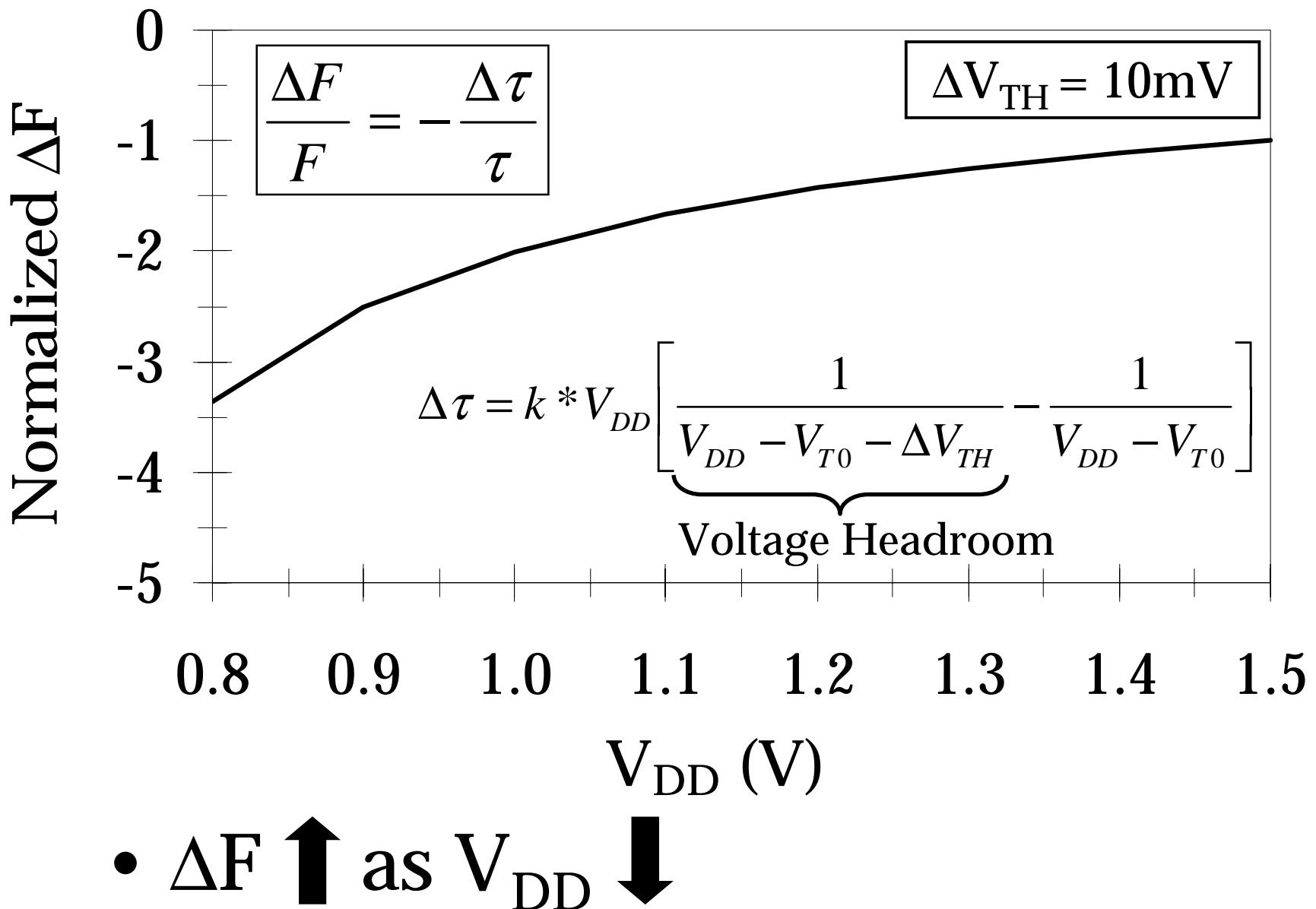
- TCAD with donor interface traps
→ Agreement with experiment

Experiment vs Simulation Comparison

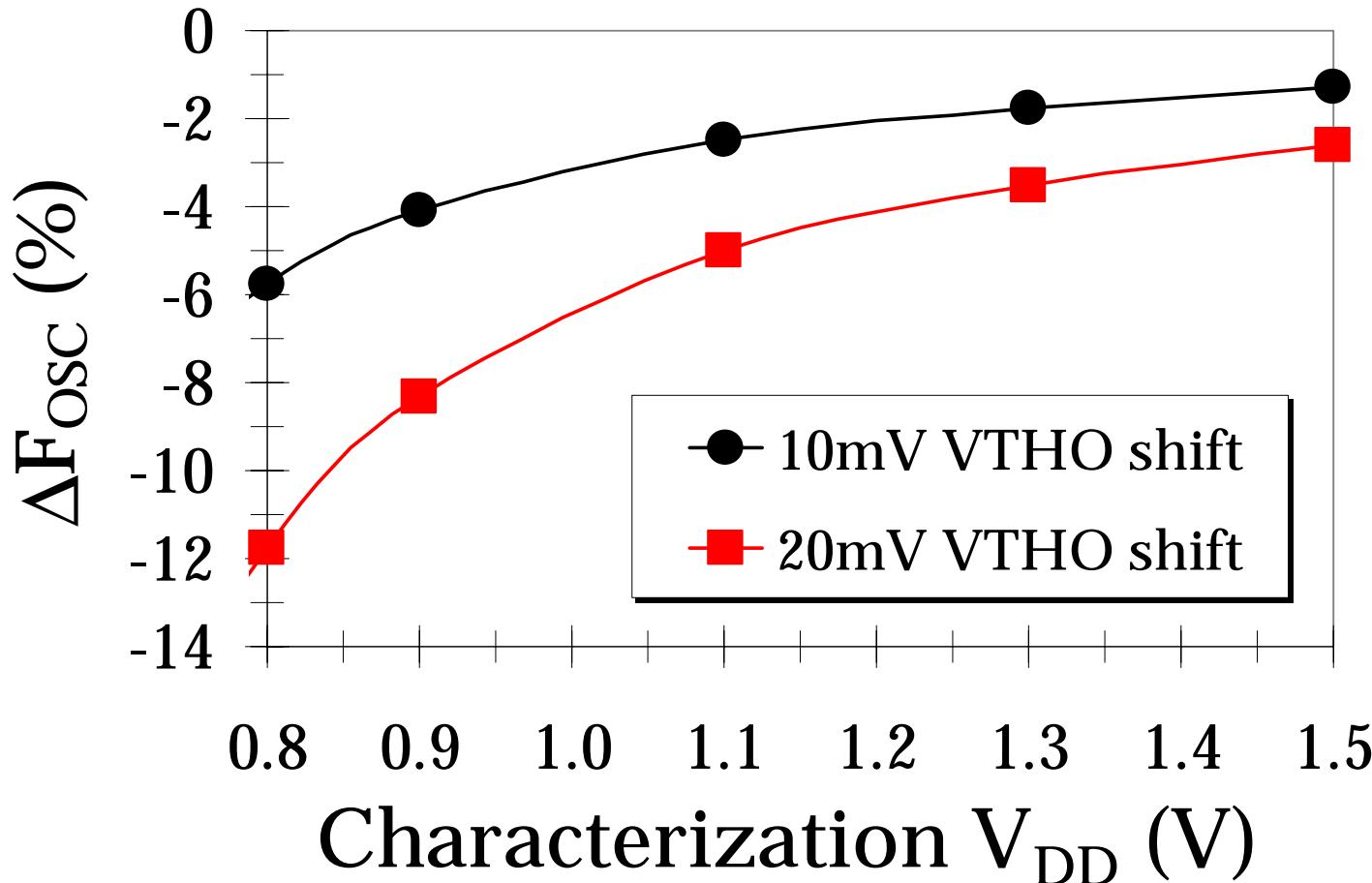


- Confirms donor trap model validity

Inverter Propagation Delay



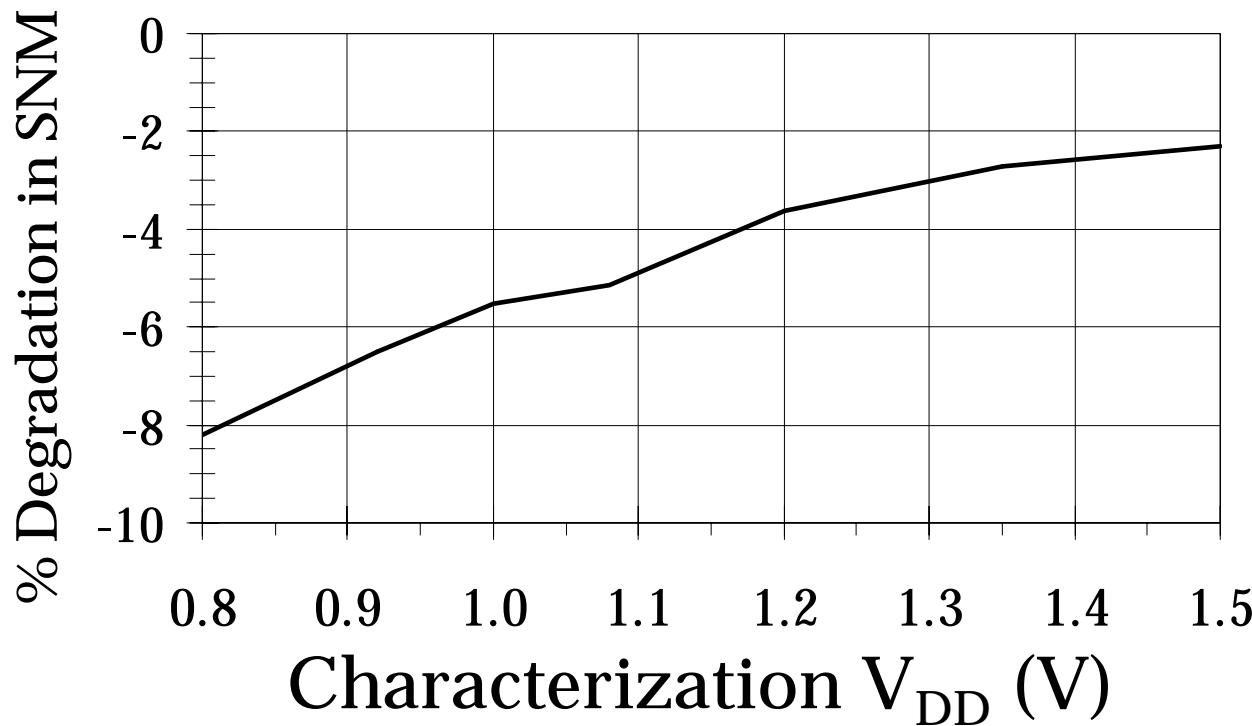
SPICE Simulated ΔF_{OSC}



- SPICE: $\Delta F_{\text{OSC}} \uparrow$ as $V_{\text{DD}} \downarrow$
- Reduced Voltage Headroom

NBTI Impact on SRAM Cell Stability

- Static Noise Margin (SNM): Ability to maintain data under noise and device mismatch
- NBTI impact modeled with degraded SPICE model in one of the pMOS load transistors



- SNM degrades as V_{DD} decreases

NBTI Impact on FPGA Propagation Delay

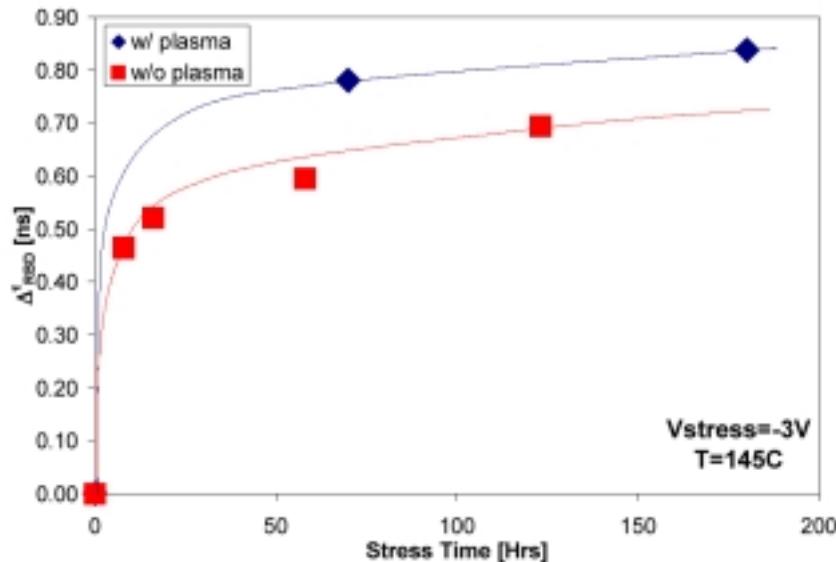


Figure 9. Performance degradation of an FPGA device under $-3V$, $145C$ stress condition

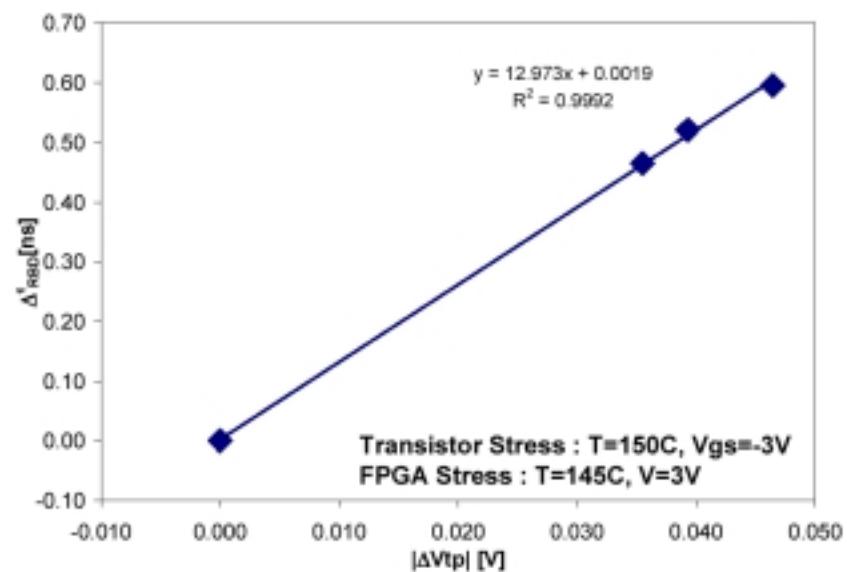


Figure 10. comparison of performance degradation of FPGA and V_t shift of a PMOS transistor.

(Pagaduan et. al, 2001 IRPS)

- Correlation between NBTI ΔV_{tp} and Product propagation delay
- Plasma damage increases NBTI degradation and results in increase propagation delay

Summary

- Provided a brief introduction to NBTI mechanism/kinetics
- Deep sub-micron processes can exacerbate NBTI
- Need to incorporate NBTI degradation into circuit simulation
- Impact of NBTI on digital circuits illustrated
 - Frequency degradation is worse at lower V_{DD}
 - Transistor: Reduced transistor gate overdrive
 - Circuit: Voltage headroom reduction
 - Simulations
 - Transistor: Donor interface state generation during NBTI stress results in degradation
 - Circuit: Experimental F_{osc} drift modeled through SPICE simulations
- NBTI stress results in SRAM SNM and Prop. Delay degradation
- Circuit impact of NBTI expected to worsen as V_{DD} scaling continues

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