

Circuit Design using a FinFET process

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DCAS – Jan 2006

Acknowledgements

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TEXAS INSTRUMENTS

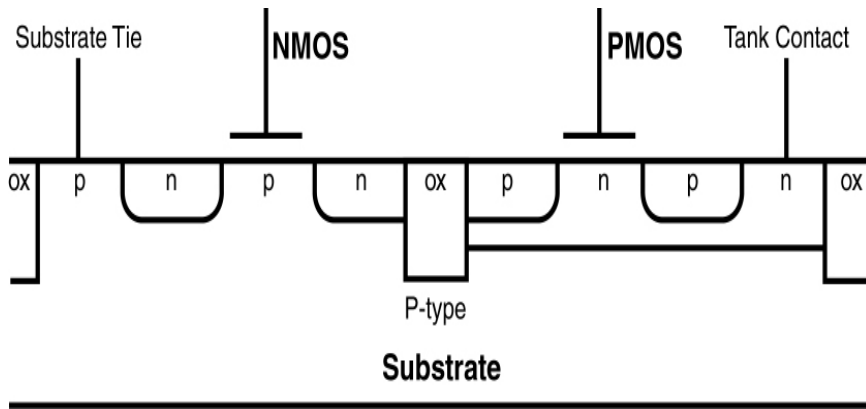


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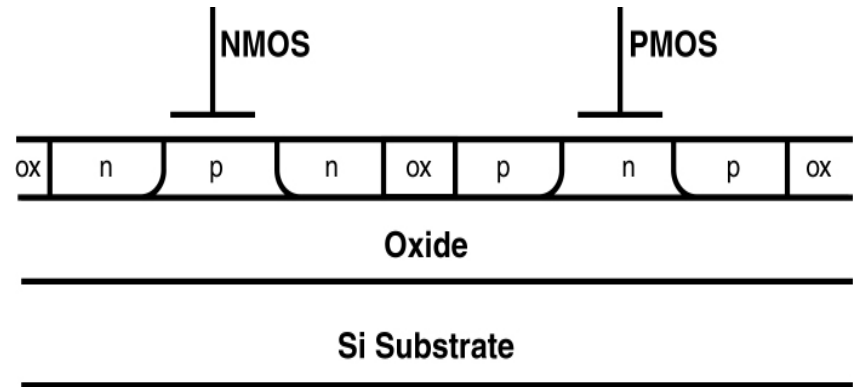


Soitec

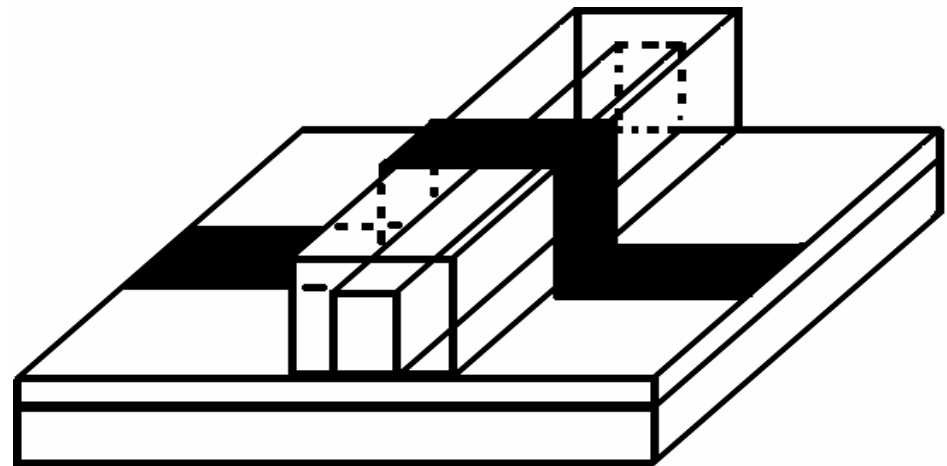
SOI and bulk transistor comparison



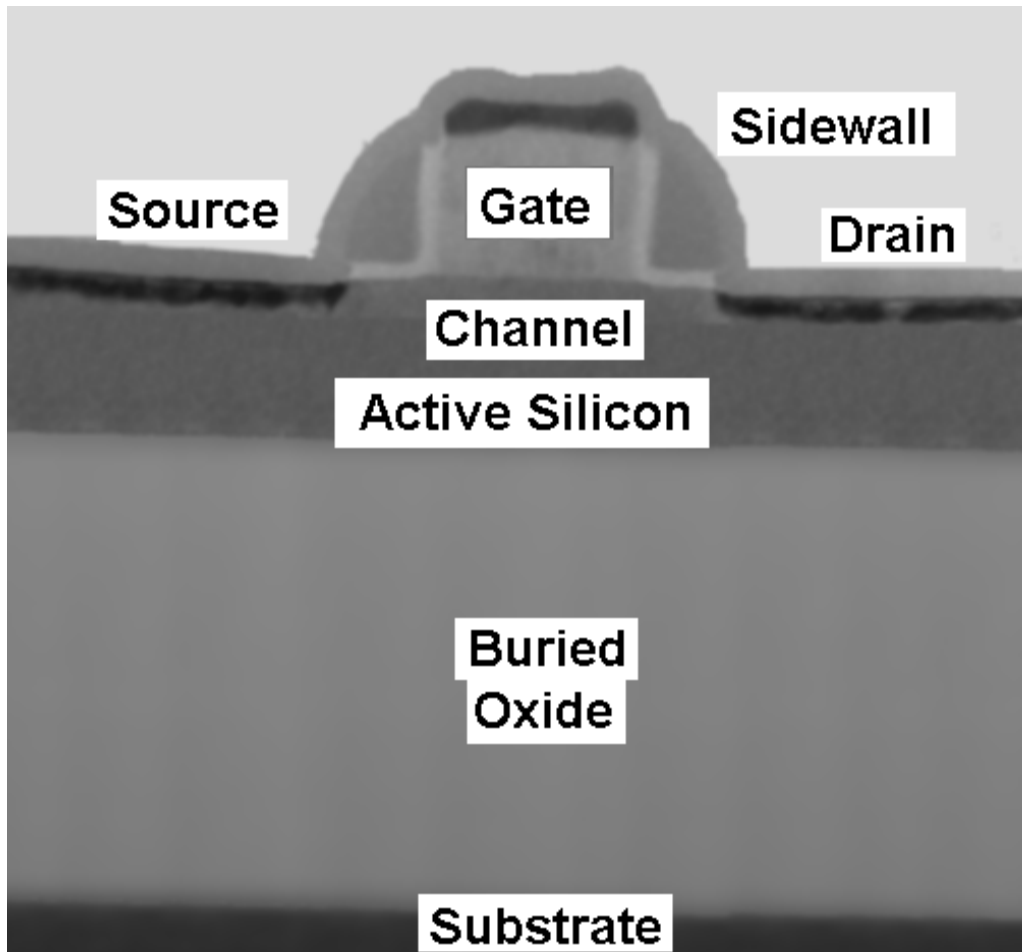
Simplified bulk dielectric isolated process



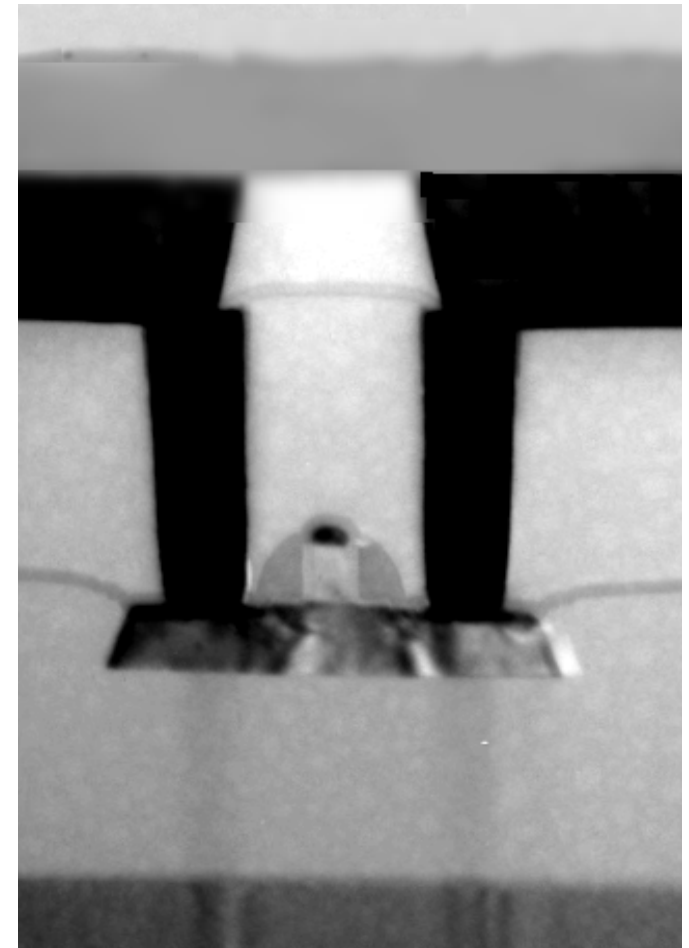
Simplified planar SOI CMOS cross-section



Simplified finfet process cross-section

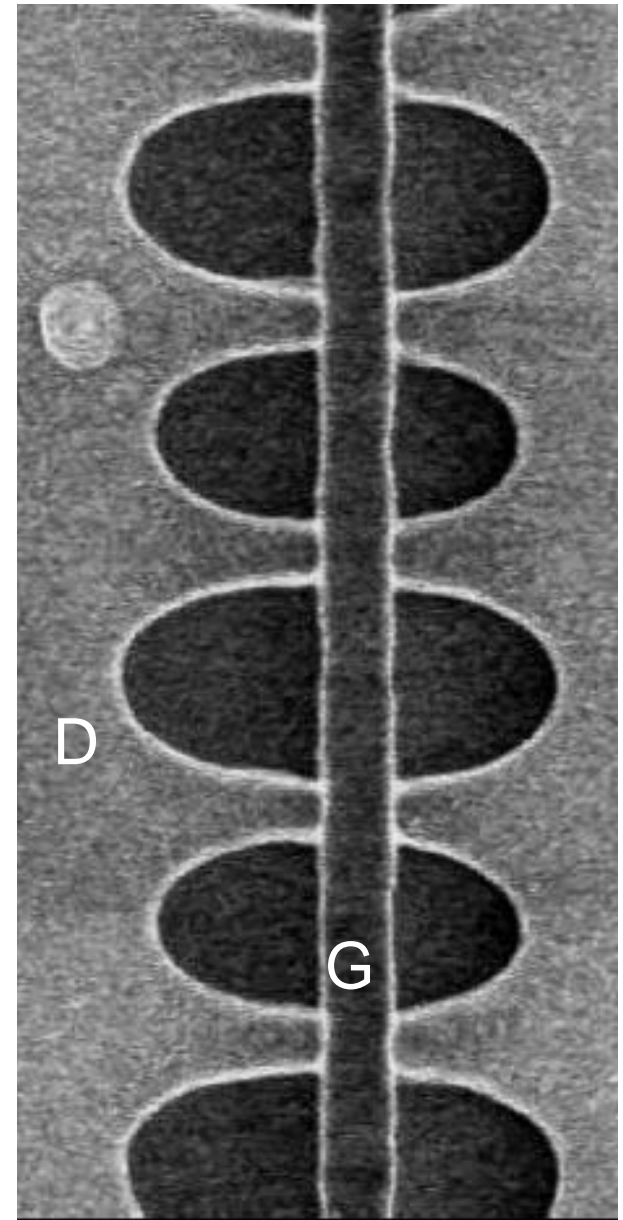
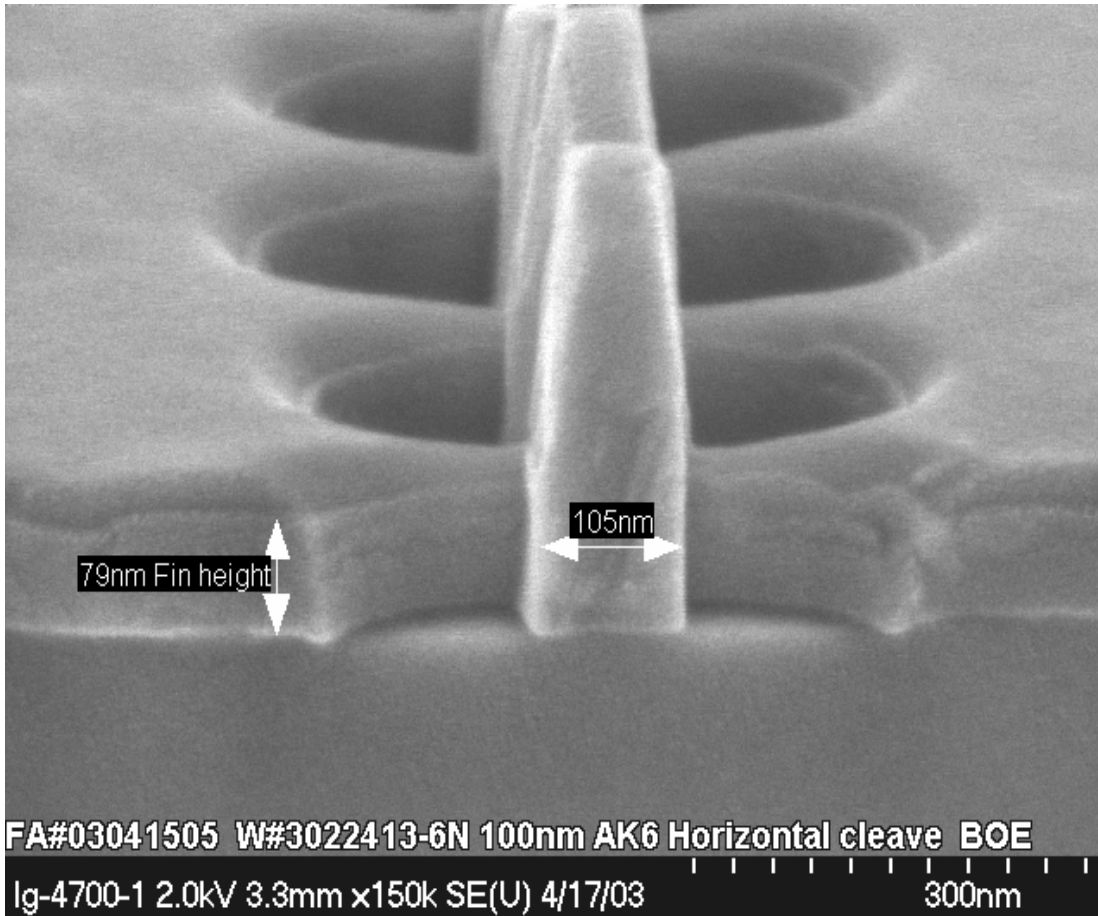


(a)



(b)

Cross sections of a planar-SOI NMOS transistor. (a) shows the basic MOS structure (b) shows the source/drain contacts, and silicon mesa

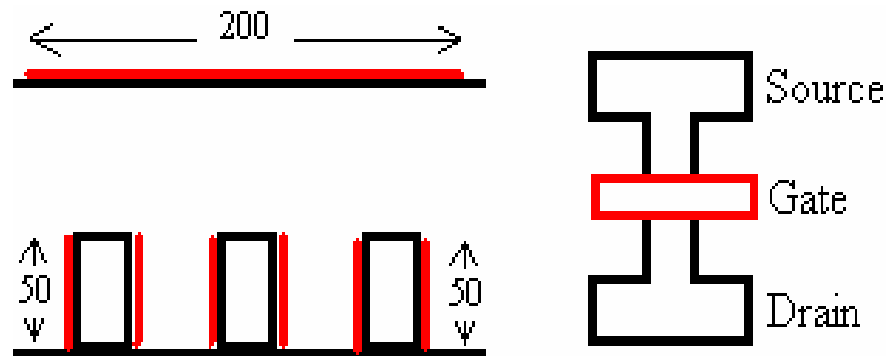


Views of FinFet, showing cross sectional and top down views.

FinFET / Multiple Gate (MUG) FET

Sidewalls (FinFET) and also tops (trigate) become active channel width/length, thus more than one surface of an active region of silicon has gate, eg: sides and top, vs one surface for planar structures.

- State of the art fin W is 20-60nm, fin/gate height 50-100nm, gate length ~30nm
- lower parasitic capacitances
- larger gate width / unit area
- With Fin height of 50nm, Fin width 20nm, pitch 80nm, 300nm of gate width can be squeezed into 200nm silicon width [1]
- Gate lengths of <20nm have been generated.
 - S/D resistance / channel modulation
- Multiple fins permit larger widths, but gate width is quantized by fins gate width



Advantages of SOI over Bulk

- Reduced D/S cap (oxide isolation vs junction isolation) – Lower power
- Reduction in the "MOS reverse body effect" in stacked transistor devices
- Improved latchup, noise and current immunity through the substrate
- Simpler high V component design
- Improved high temp performance (lower device and parasitic leakage)
- Improved passive components – Inductor Q, parasitic capacitance
- Reduced capacitance from substrate to metal interconnect (reduced power)
- Fewer process steps (Pwell / NBL)
- SOC, High Perf, RF, High Freq, Low Leakage, Low Power, High Temp, Smaller area

Disadvantages of SOI over Bulk

- Self heating, dissipation problems
- Reduced Vdd-GND capacitance for noise reduction on supply rail
- Floating body can cause higher drain-source leakage (transient and DC) *
- Cost, Engineering & Management Pushback, Extra Design time, Relatively new, Starting wafer cost.
- Quantization of width in Mugfet designs
- Some Power reduction techniques cannot be used

Scaling trends between Bulk, PD/FD-SOI and MuGFET

- Bulk requires increase in doping level with scaling, adversely affecting carrier mobility and junction capacitance.
 - May limit scaling to 20-35nm gate lengths
- SOI able to scale considerably further than this, but trend may be to metal gates, for V_t tuning, double and triple gate / finfet
 - PD-SOI thick SOI film (>150nm) – must consider floating body
 - FD-SOI thinner SOI film (<100nm) – more difficult manufacture (also untrathin-SOI)
- MuGFET (Multigate fet) is the general term for the class of devices that gain extra component width by allowing vertical active gates. Finfets and trigate are examples
 - Similar in function to FDSOI
 - AIM to increase area vs equivalent bulk/FDSOI
 - Adds extra dimension (height) for additional gate width

PD-SOI specific design issues

Floating Body makes PD-SOI design complex vs bulk:

History effect: Gate delay change as fn of switching history

Cap coupling perturbs steady-state V_{BS}

At MOS turn "ON" body capacitively couples to drain

- Pulled low, & converges to a DC value due to leakage

Delay varies if next switching event occurs before body returns to equilibrium and as the input period is changed

Kink effect: Observed once impact ionization begins

Result of abrupt saturation current increase due to body V increase

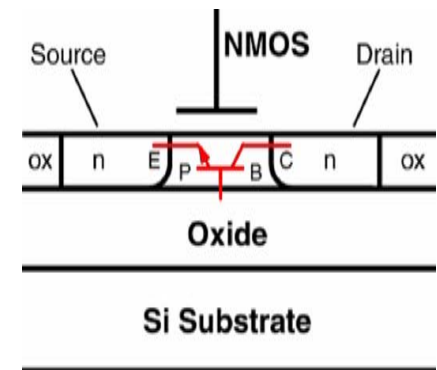
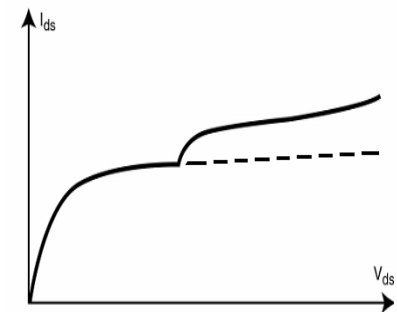
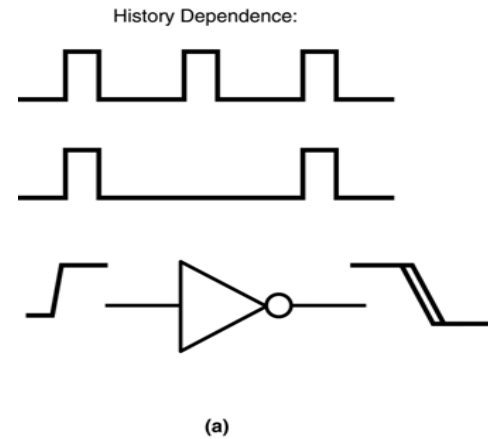
Detrimental to the design of most analog circuits

Bipolar effect: Parasitic bipolar base effects

NPN can turn-on when S & D high (e.g. Xmission gate).

Body drifts high until S,D & B are at same potential.

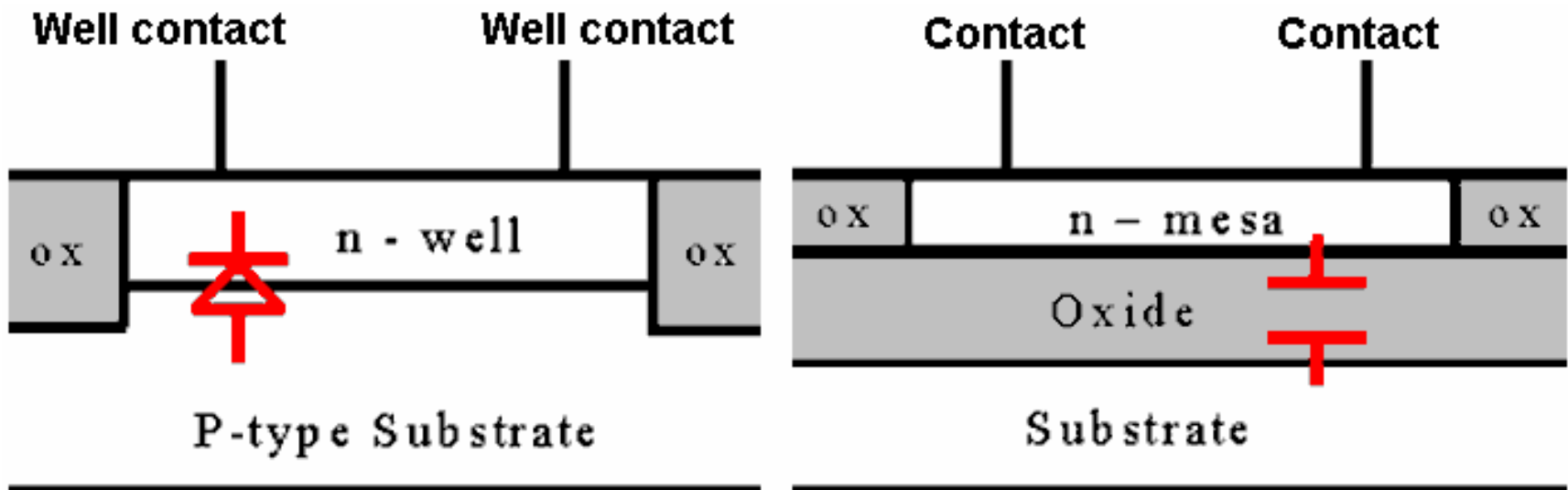
If gate is low and source then pulled low, base pulled down due to B-E diode turn on. Parasitic NPN turns on until carriers are swept from base.



Passive Components - Major passive components: R's C's, diodes and L's

Resistors in SOI - two forms

- Polysilicon resistors constructed on SOI in same way as on bulk
 - Reduced capacitance to substrate due to BOX region
- SOI Well resistors are different to their bulk counterparts.
 - In bulk n-type doping into p-type substrate, creates V dependent R/C
 - SOI mesa resistor has no parasitic diode to ground, low capacitance to ground, and R/C variation with respect to voltage is low



Cross sections of well resistors in (a) bulk silicon, and (b) SOI

Capacitors

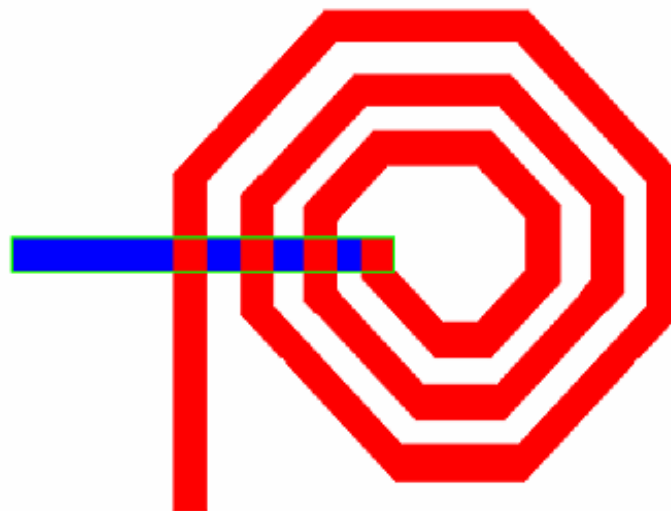
- Well capacitors not available in SOI
 - As circuit components they are not used much in modern devices
 - Supply to ground capacitance provided by Nwell is absent in SOI
 - Power advantages / noise disadvantages
- Gate caps usually have higher series resistance in SOI due to thinner silicon
 - Inferior resistance but lower parasitic capacitance to ground
 - Minimized with multiple-finger layout
- The metal capacitor is commonly used, formed with multiple interdigitated layers
 - Interdigitated for maximum capacitance.
 - Alike in bulk and SOI, but reduced parasitics in SOI

Inductors

Often constructed in the top level of metal

- Since SOI is used for RF circuitry influence of SOI on integrated inductors is important
- The Q-factor of inductors improved on SOI (esp. high res substrates)
- Inductors and transformers are constructed as a spiral using one or more levels of metal

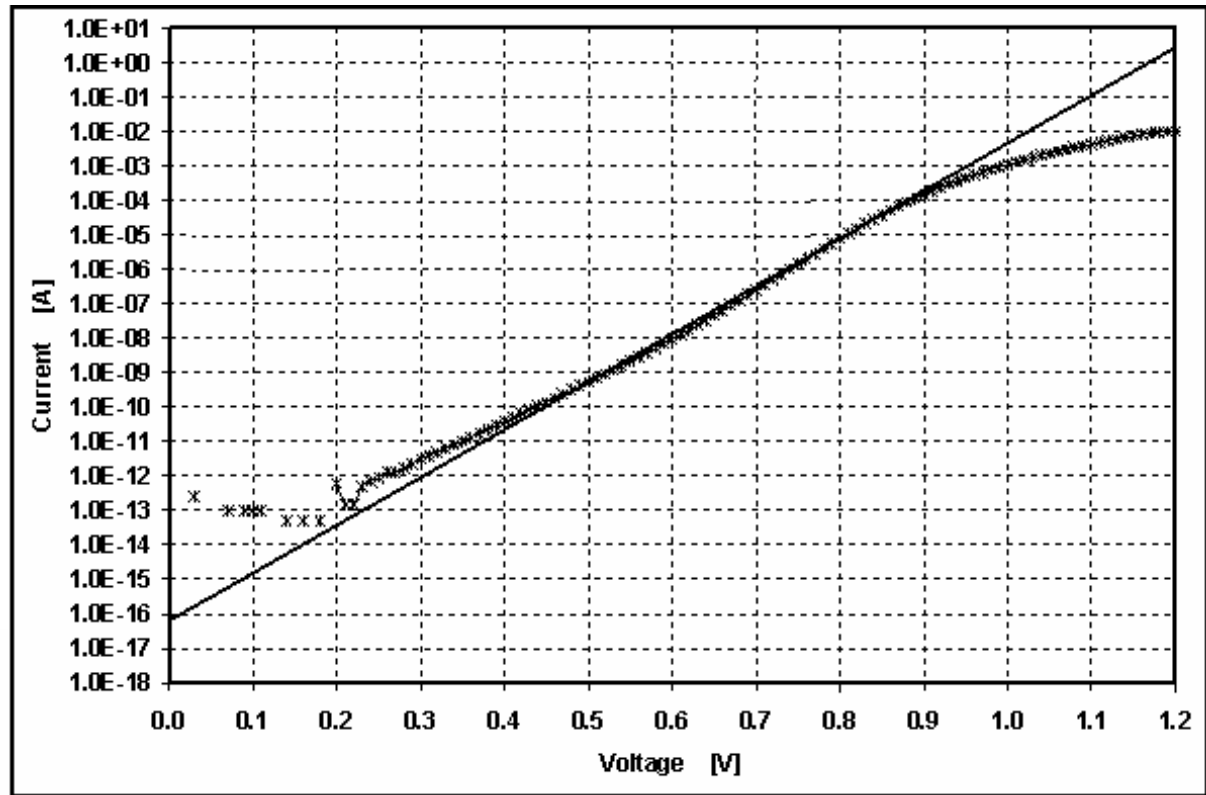
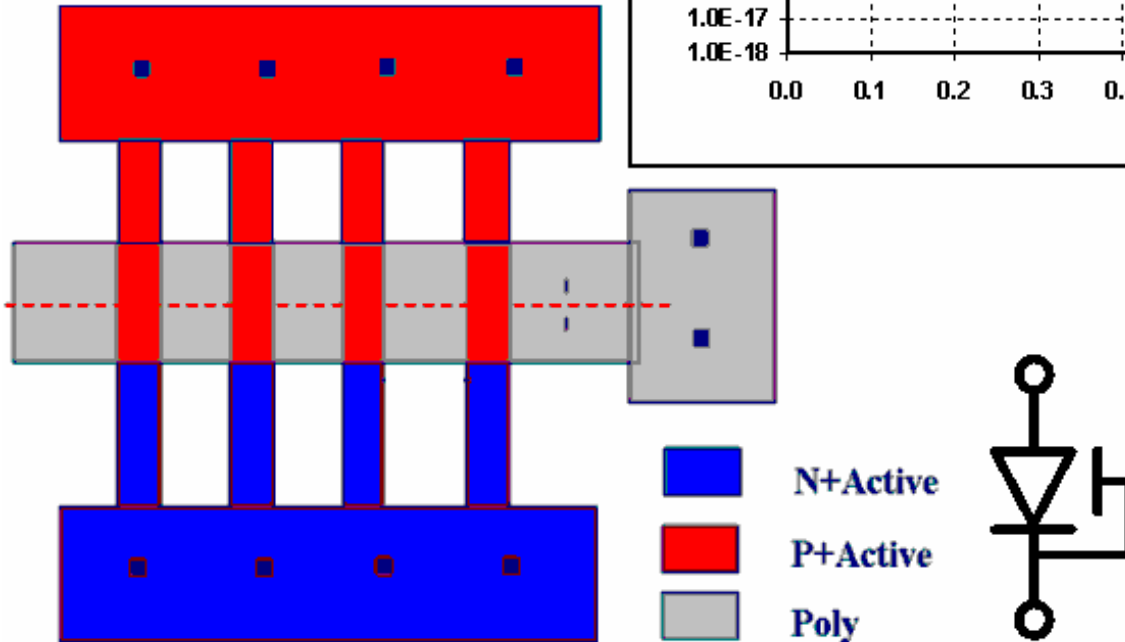
Monolithic inductor layout: Red trace represents one or more metal levels, center tap tunnels under the inductor



Diodes

Conventional bulk well diodes are not readily available in SOI

The gated diode is a diode based on a MOS device [2]

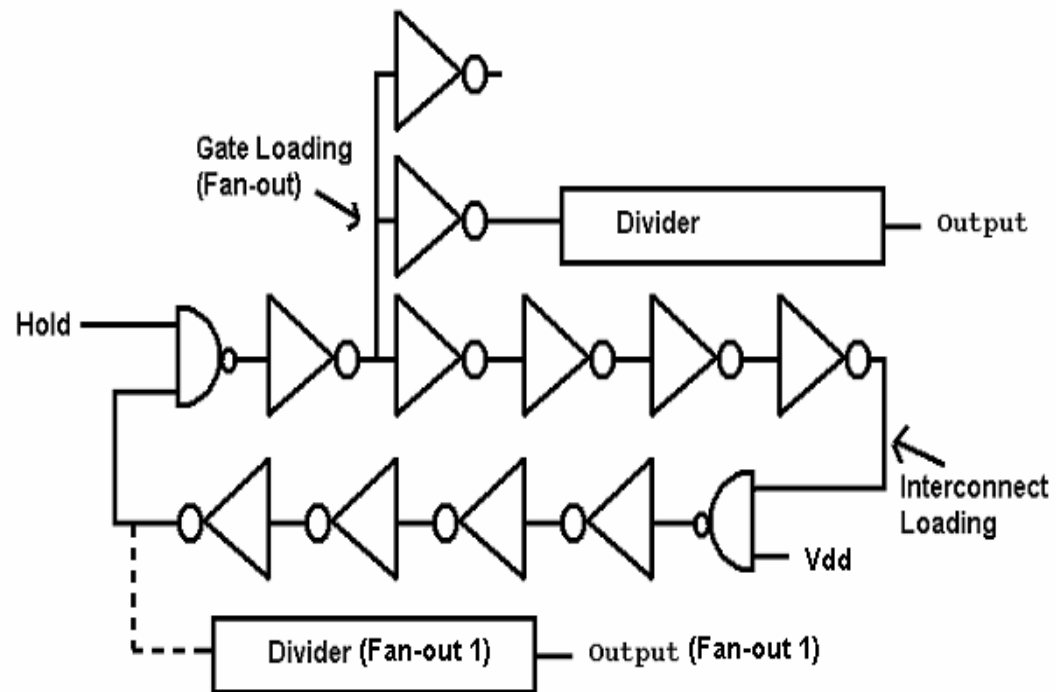


Ring Oscillator Performance [3-5]

- Ring oscillators have long been used as a guide to process performance
- Fastest ring oscillator is a minimally loaded fan-out of 1 inverter (even these need to take account of minimum interconnect R/C)
- More realistic circuit operation indicator are larger fan-out NAND ROs
- Interconnect loaded ROs good for monitoring capacitive & resistive effects
- Common to include:

'hold' to stop the ring
(leakage
measurements)

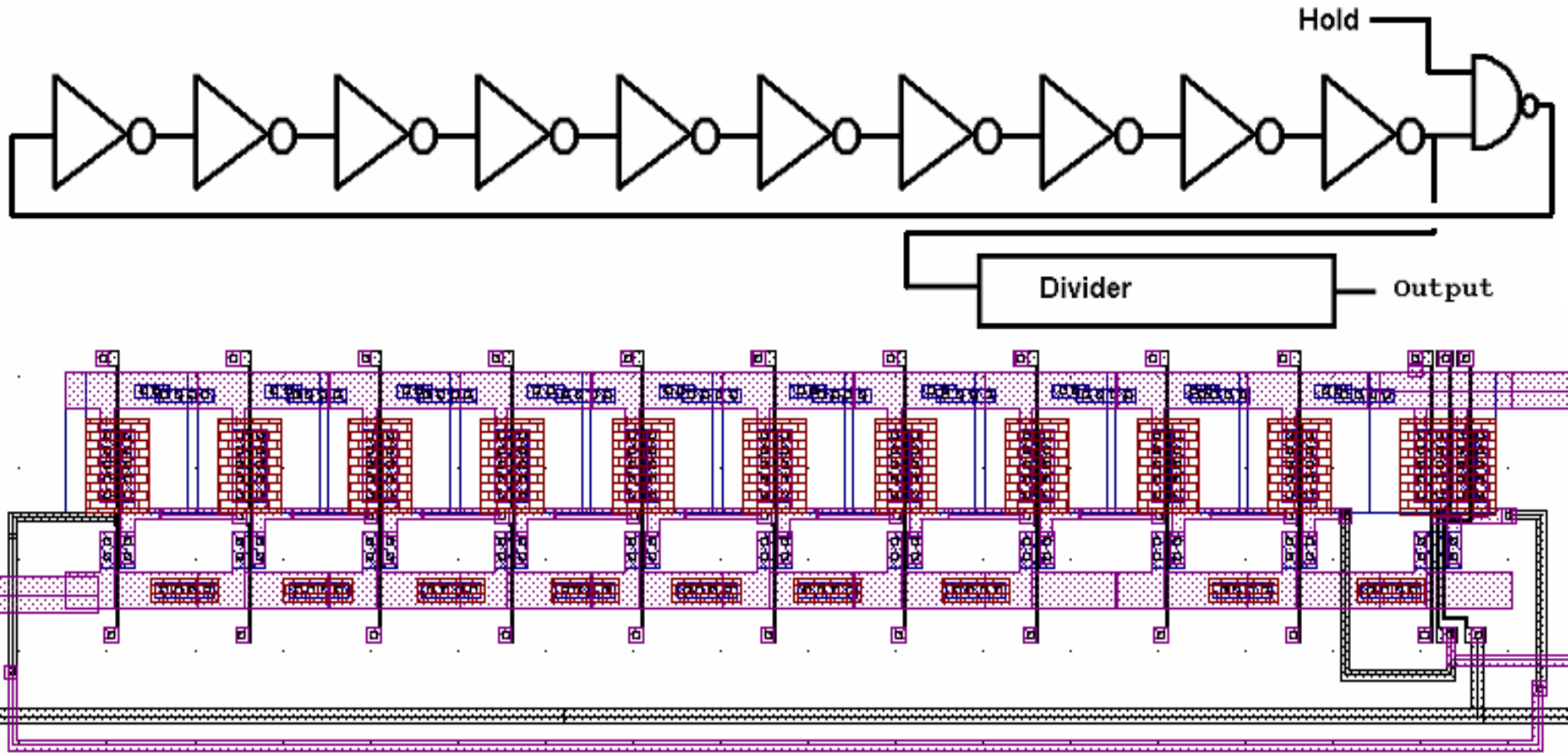
Frequency divider for
more convenient
frequency monitoring



Example ring-of-eleven oscillator circuit, showing some typical features

Ring Oscillators - Inverter/Nand/NOR Frequencies

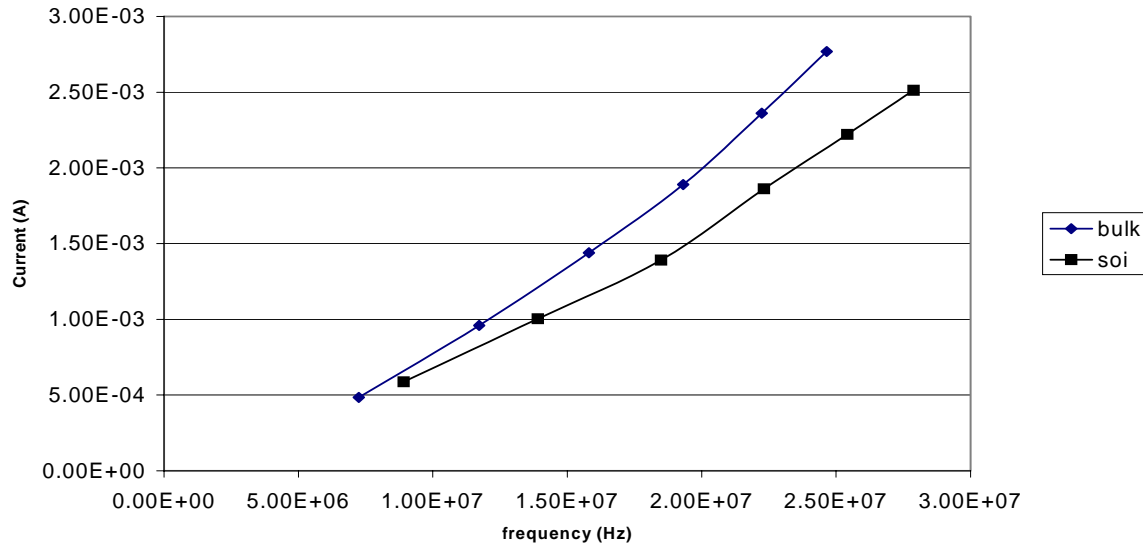
- Based on bulk ROs, ring of 11 or some other odd #
- indication of performance of logic circuits



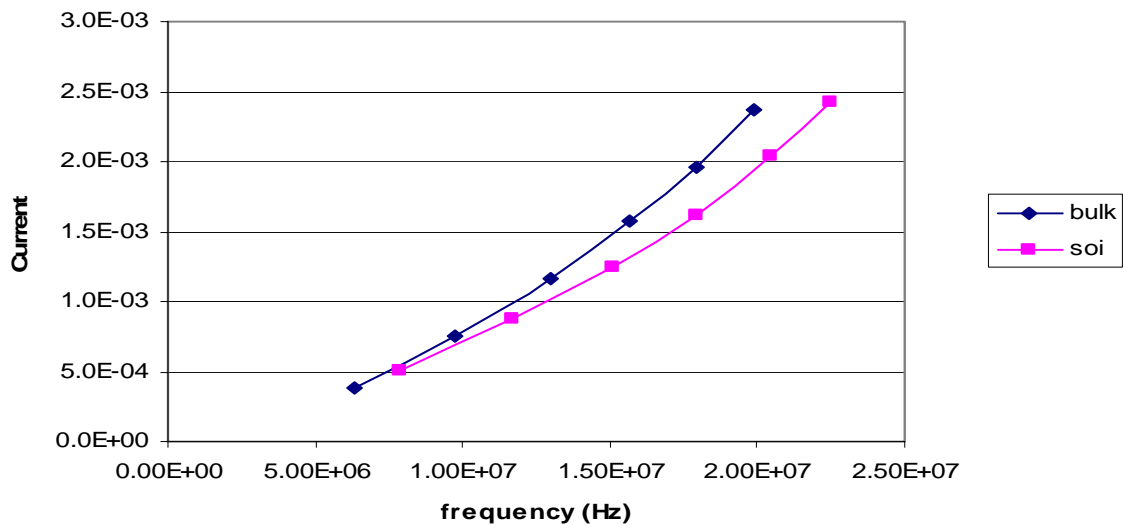
PDSOI vs bulk comparison

- PDSOI faster and lower current (130nm technology)
- SOI requires less current and power for a given frequency
- Performance gap Bulk to SOI is reduced at higher temperatures, but persists over all conditions

Fanout 3 NAND - 25 degrees



Fanout 3 NAND - 125 degrees



FinFET Ring Oscillator Circuits Performance

Approx 30 ROs on test chip with:

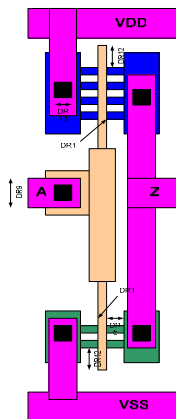
gate lengths 90-120nm

fin widths from 50 to 80nm

fin height ~ 80nm

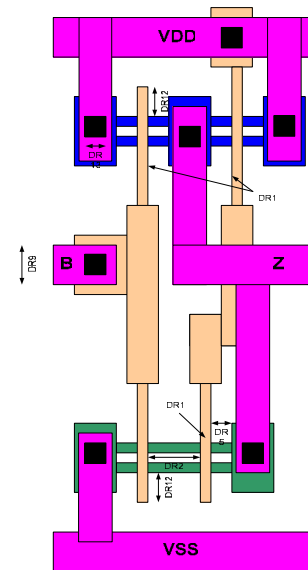
fin numbers: 2-12 (NMOS) 2-18 (PMOS)

Invertor, Nand, Nor



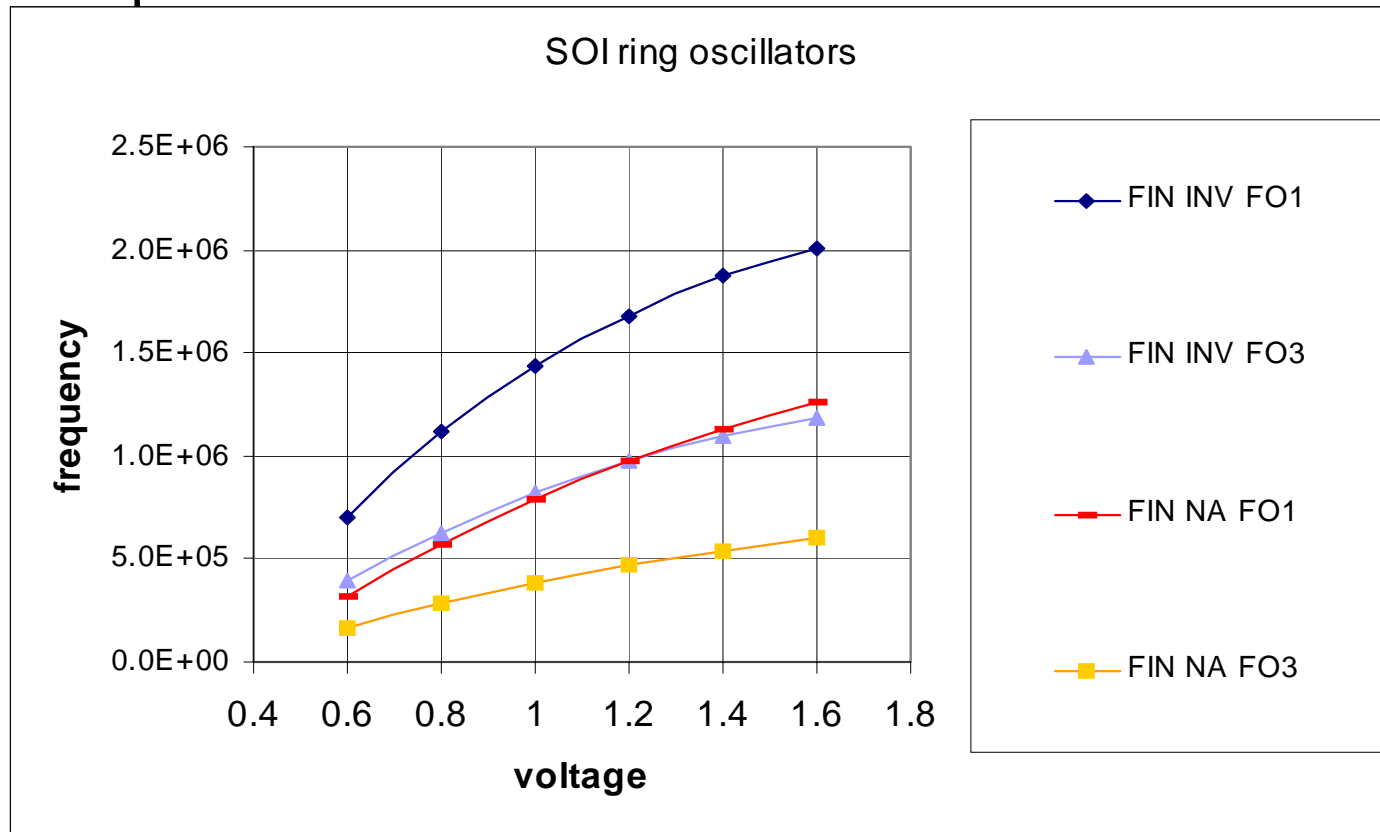
INV1

NAND2



RO's Inv/Nand freq vs supply

- Operate from $<0.6\text{v}$ to $>1.6\text{v}$
 - performance broadly in line with equivalent bulk would expect perf $\sim 25\%$ better than bulk when optimized



Analog Design using MuGFET - Overview

Advantages of SOI for Analog

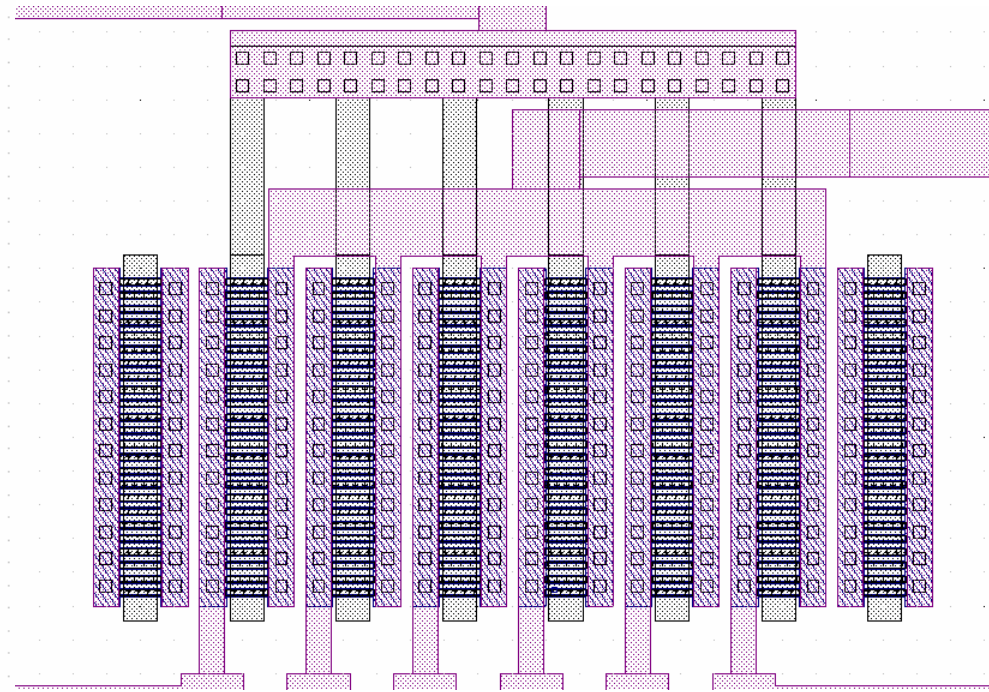
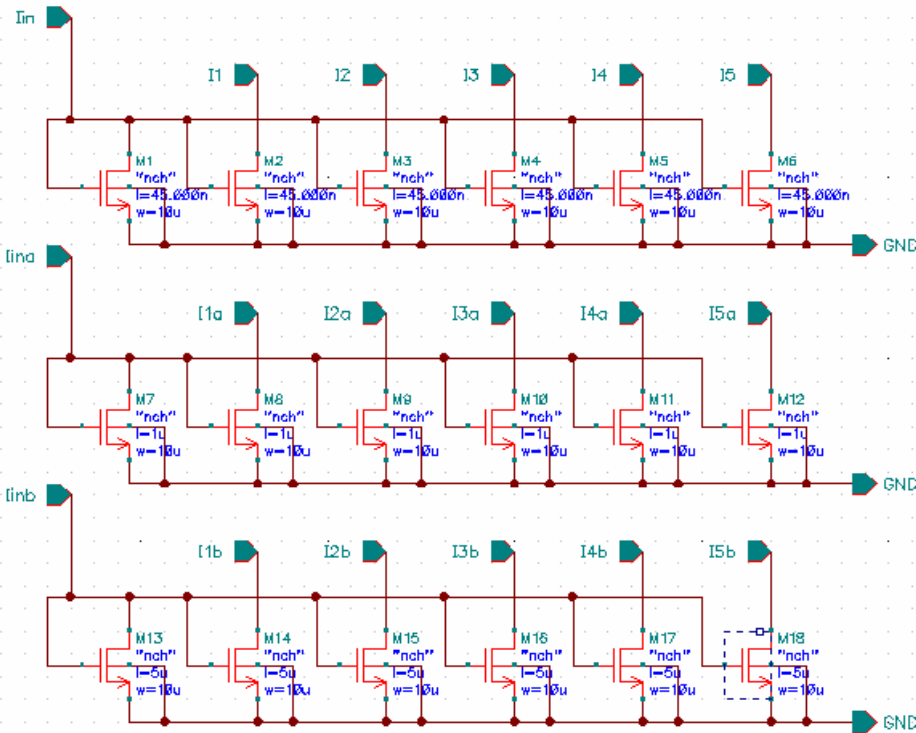
- Improved frequency performance
 - Reduced capacitance
 - Higher drive current
 - Reduction in interconnect length / reduced interconnect capacitance
- Noise and latchup are minimized through reduced substrate coupling
- Silicon resistors have improved linearity with respect to absolute voltage
 - Do not form reverse biased diodes to substrate
- Inductor Q can be enhanced through use of very high resistivity substrates

Drawbacks to SOI for Analog

- Floating body
- Poor thermal response due to buried oxide and trench isolation.
- Device noise is a potential issue Quantized widths

Current Mirrors - MuGFET

- Based on similar bulk current mirrors
- NMOS and PMOS mirrors, Input and 5 adjacent outputs
- Three gate lengths – 45nm, 1um, 5um
- Matching and leakage, in sat, lin and intermediate states

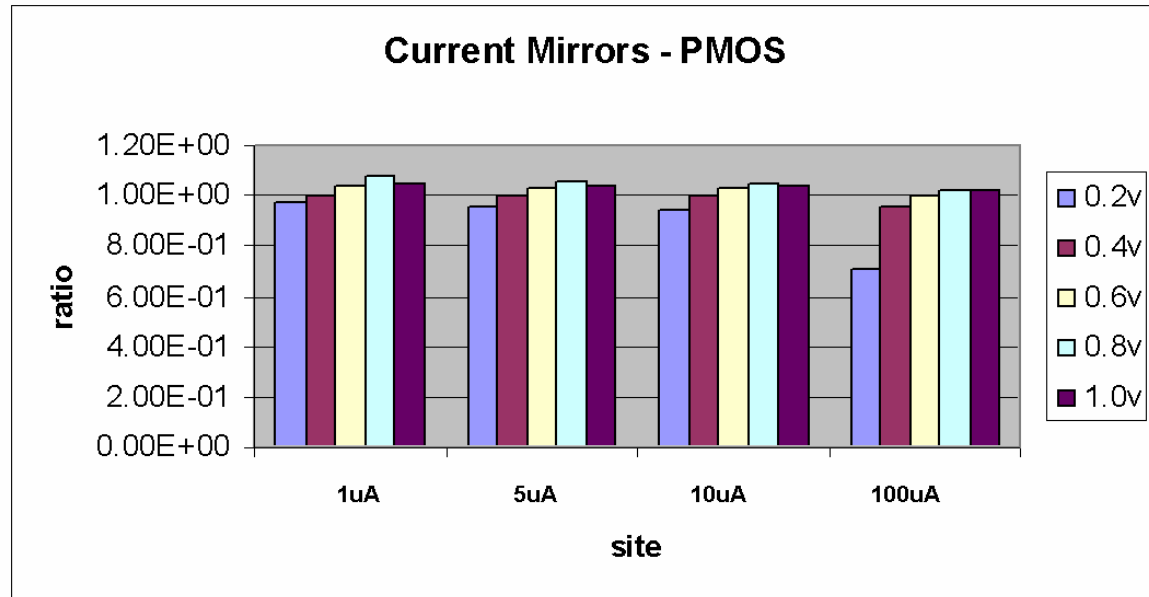
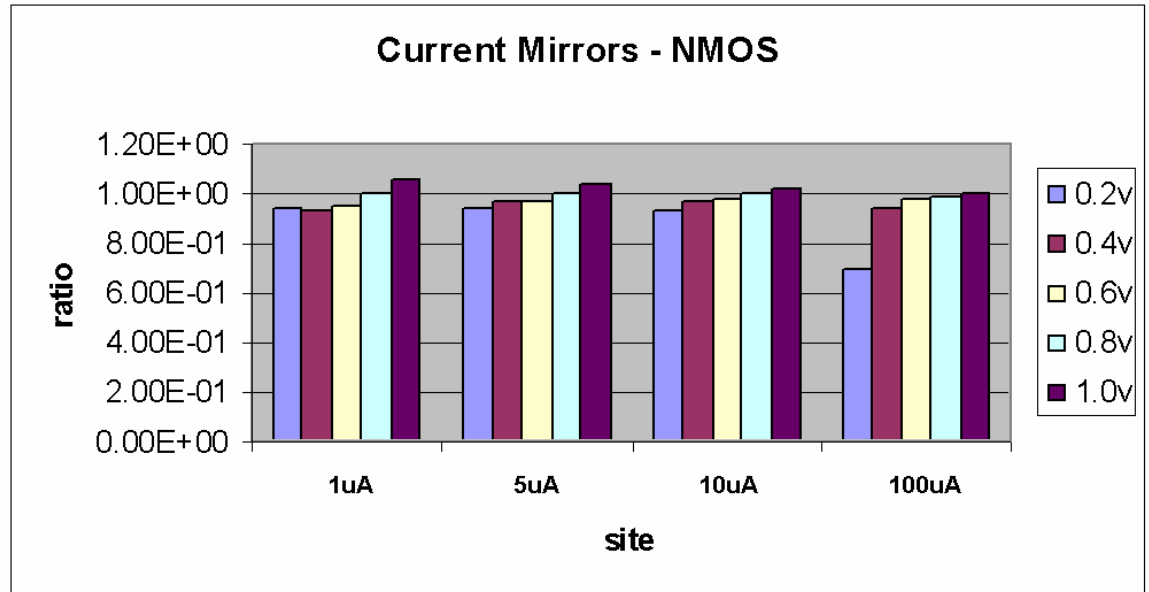


MuGFET Current Mirrors – (1 μ m LG)

- Good matching (better than 2.5%) for most of current range

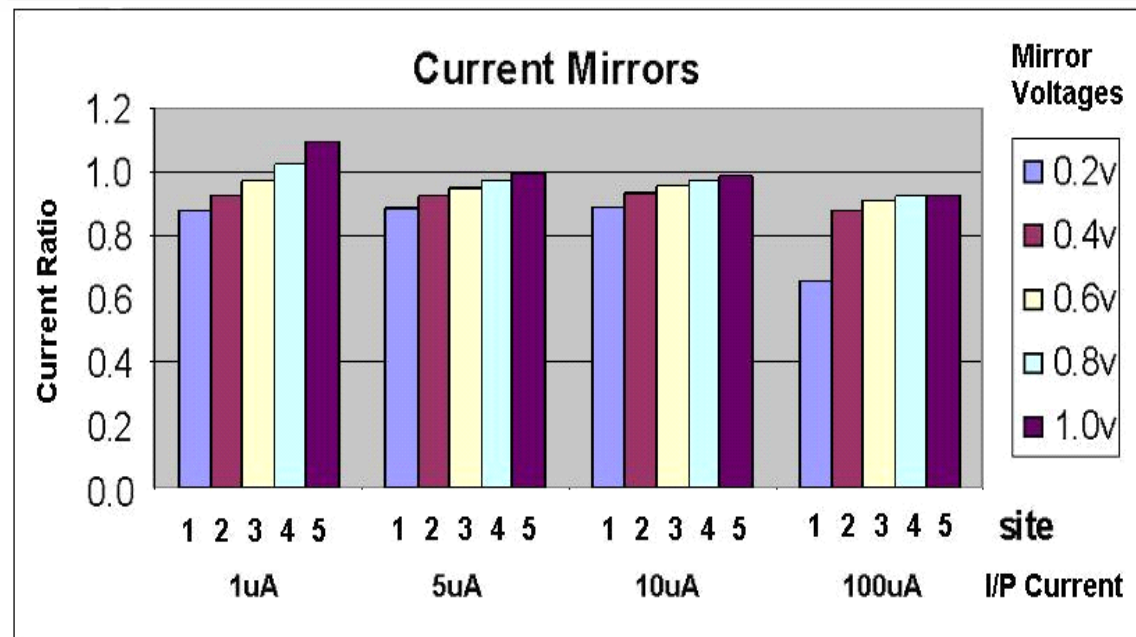
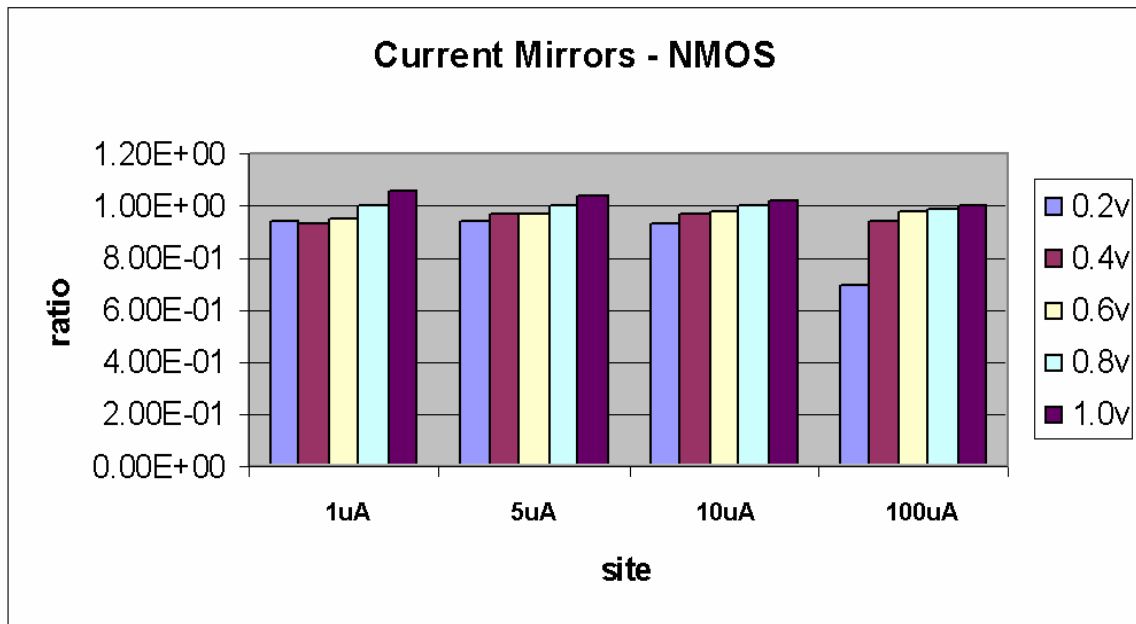
- Matching retained over supply voltages, except for higher currents

- Similar performance from NMOS and PMOS, though PMOS leakier

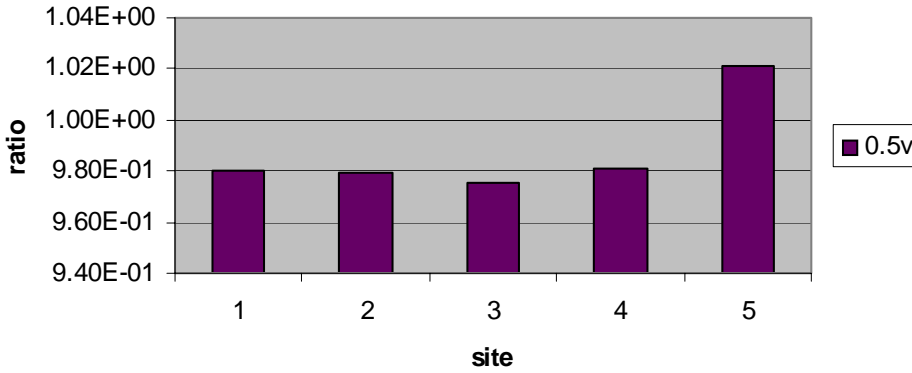


MuGFET Current Mirrors – correlation to simulation

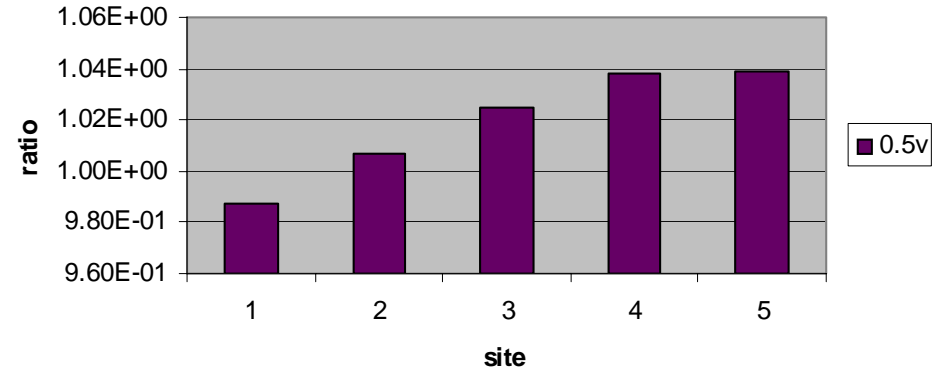
- Upper trace – silicon results, lower simulation
- Good matching (better than 3%) for most of current range, but some falloff at 100uA state (rd/rs modeling)
- Similar performance fo PMOS



Current Mirrors - matching - NMOS

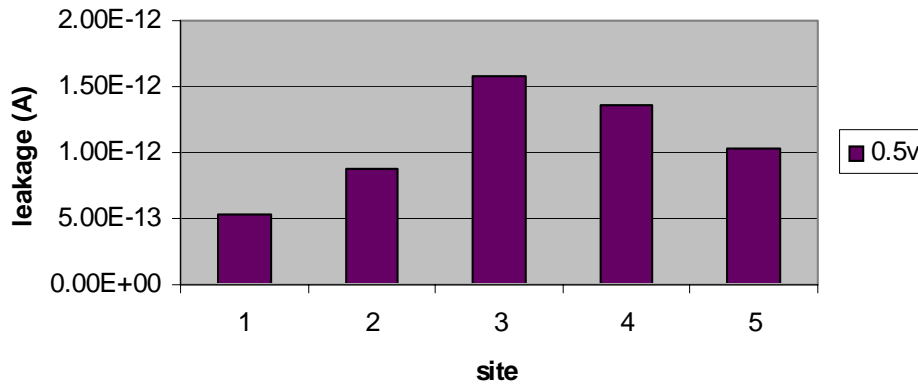


Current Mirrors - matching - PMOS

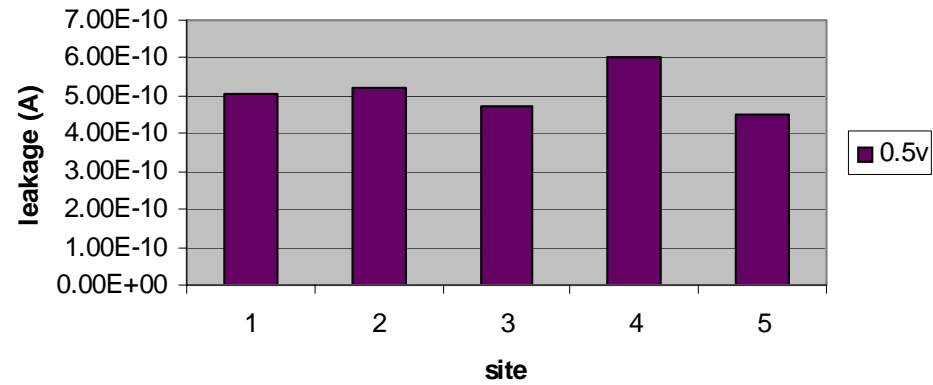


1um LG MuGFET Current Mirror performance

Current Mirrors - leakage - NMOS



Current Mirrors - leakage - PMOS



DC Thermal Coupling in Current Mirrors can cause mismatch

- Current mirrors rely on matched thermal and electrical conditions
 - Largest errors in bulk mirrors caused by electrical variation (drain voltage mismatch between reference and mirror)
 - Increased gate lengths reduce channel modulation, minimize mismatch, but with reduced bandwidth
 - Channel modulation also reduced with cascode but needs higher voltages
 - In SOI, combining devices within a mesa aids thermal matching
- Thermal mismatch can still occur within the subcircuit
 - When power dissipated in a current mirror differs between the input and output
 - E.g., 100 μ A mirror dissipates $\sim 100\mu\text{A} * V_t = 0.2\text{V}$ (20 μ W) on the input
 - The uncascoded mirror device may have a drain voltage of 1.5V, at 400 μ A current, dissipating 600 μ W at the output. A local thermal resistance of 25000 $^\circ\text{C/W}$ results in a local temperature rise of about 15 $^\circ\text{C}$ in SOI, compared to an insignificant rise in temperature in bulk material

Operational Amplifier [6]

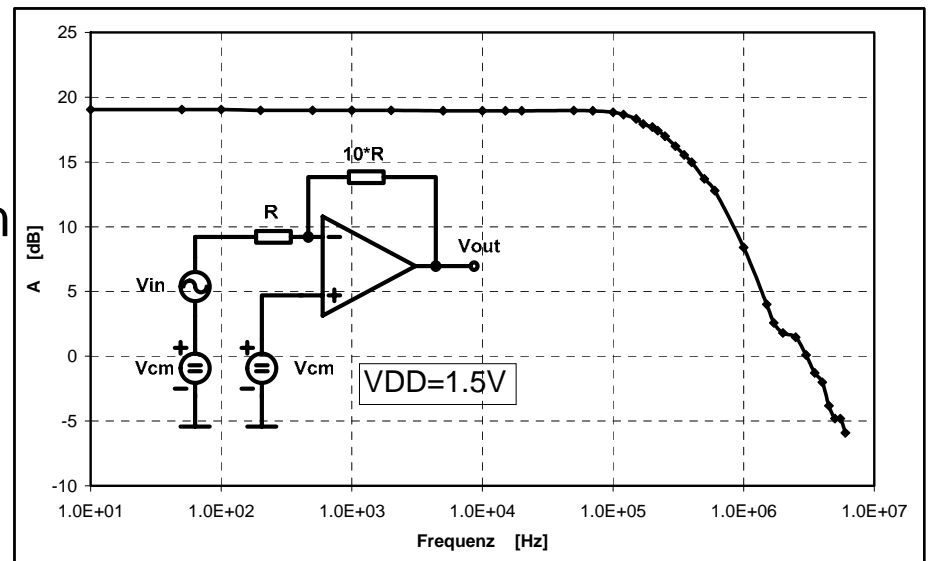
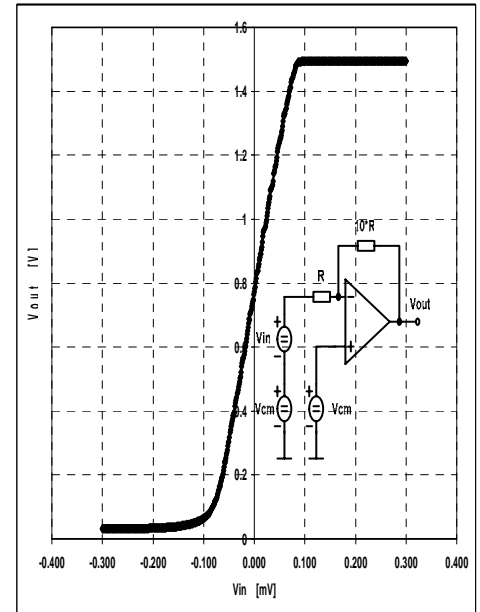
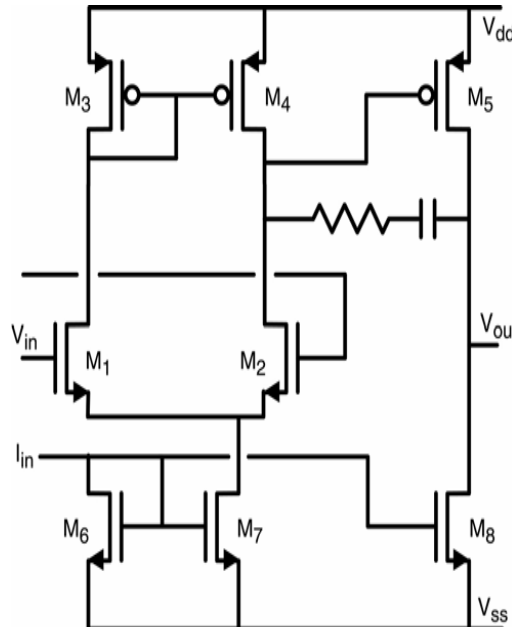
Basic CMOS op-amp requires a matched input pair

Same basic circuit design can be used for MuGFET

MuGFET don't normally suffer from body bias effect, so can be treated in the same way as bulk

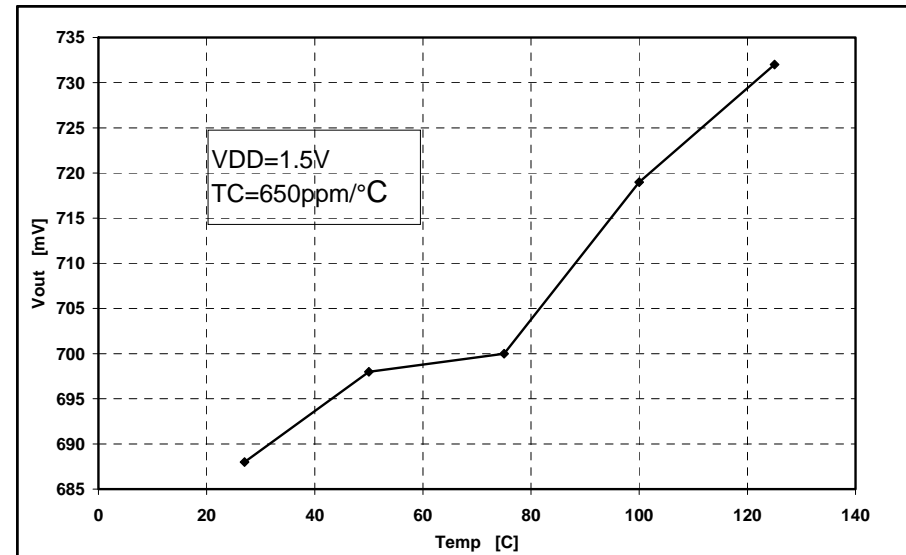
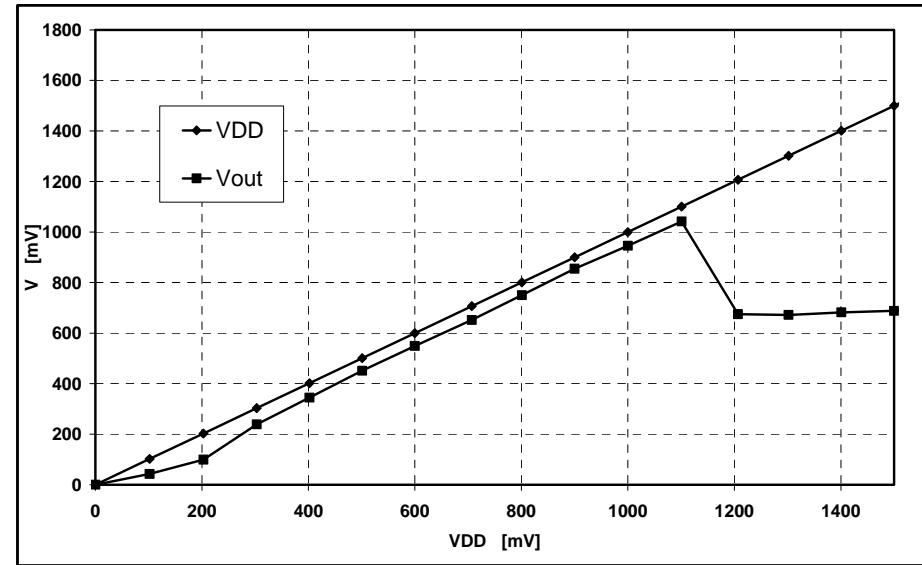
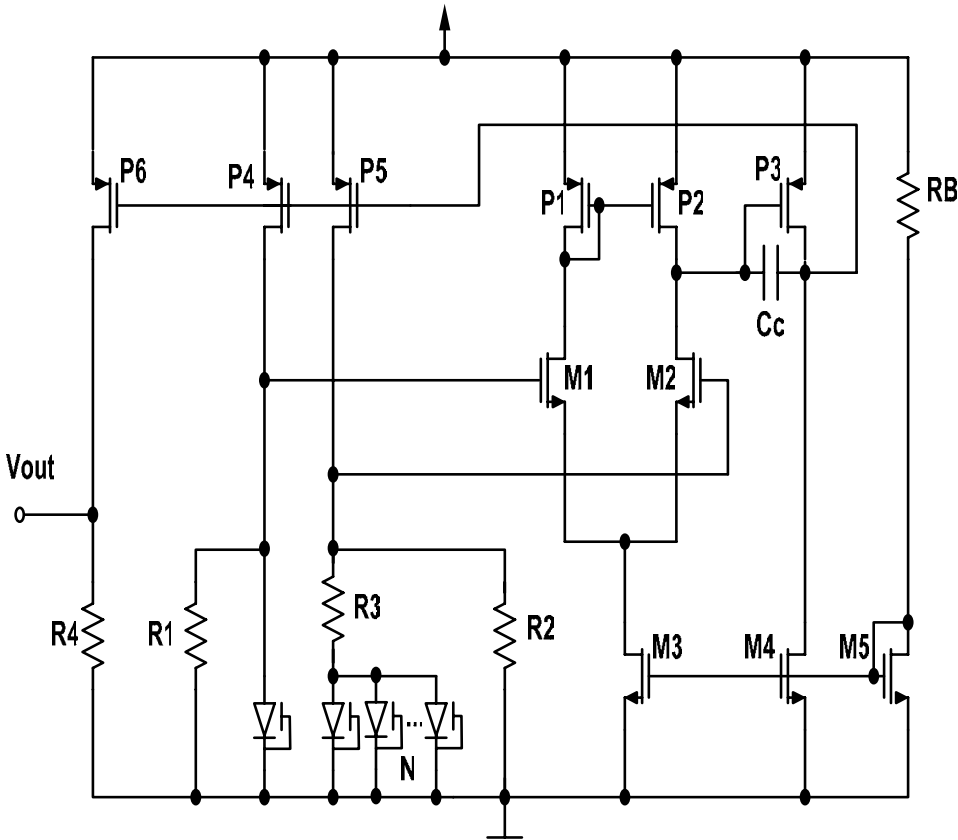
Quantization of transistor widths (approx 100nm) usually not a design issue

Bode plot (frequency vs gain) and bulk and DC transfer curves are similar to bulk



Bandgap [6]

Conventional circuit design, but using gated diode



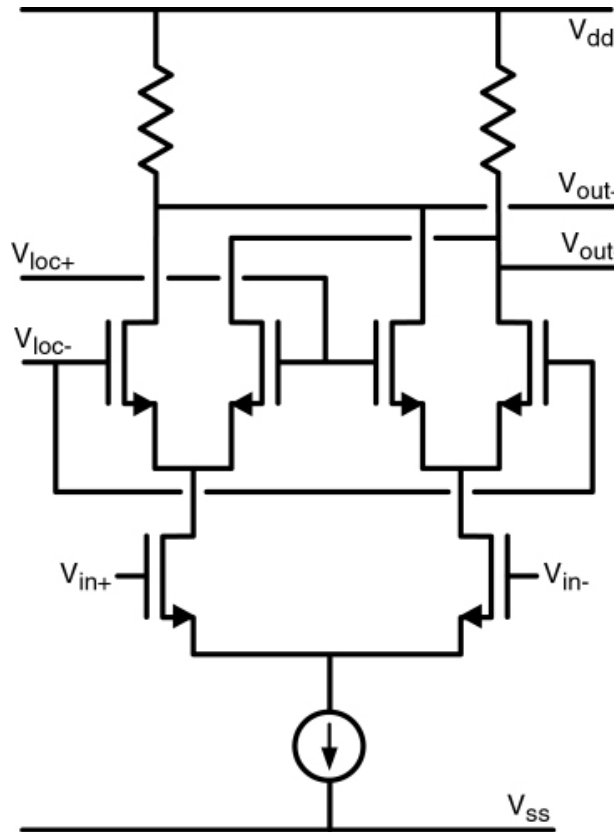
Mixers

• Important chars of mixers:

- high linearity
- low noise and low power
- high gain.

• SOI mixers benefit from reduced capacitance, aiding high frequency applications while reducing power and providing improvements in passive components

Gilbert Mixer



- Balanced signals
- Local Oscillator reference (V_{loc-} and V_{loc+}) and input signal (V_{in-} and V_{in+}) are inputs
- Differential output signal (V_{out+} and V_{out-}) is filtered to remove unwanted frequency components
- In PD-SOI Body ties are typically used at each of the input pairs

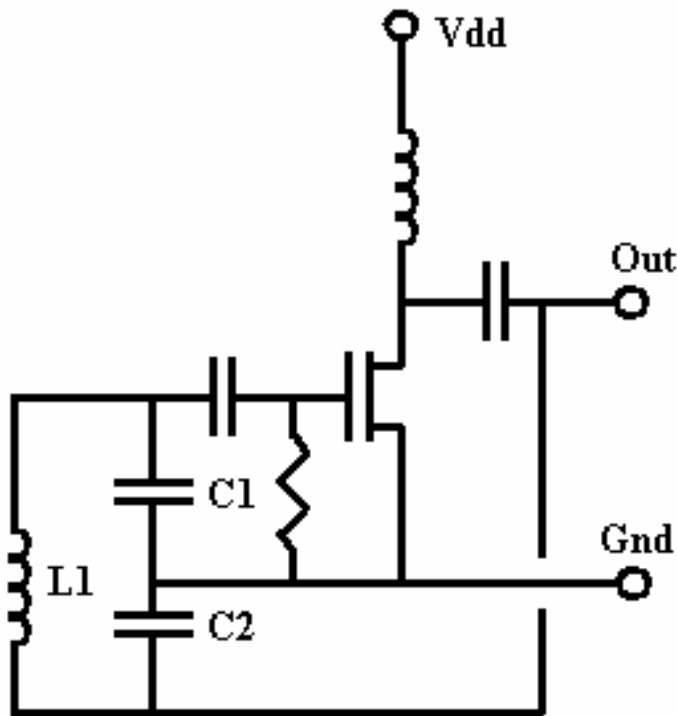
Oscillators (Fixed frequency and VCO)

- Three basic on chip oscillators
 - LC resonant circuit (for example the Colpitts oscillator)
 - Relaxation oscillators (based on capacitive charging/discharging)
 - Delay-based oscillators (such as the analog ring oscillator)

LC resonant oscillators

- Particularly stable frequency
 - Circuit operating point defined by LCR resonance
 - Difficult to integrate successfully in bulk
 - Limitations of integrated inductor design
- With some difficulty can be converted to VCO by replacing fixed capacitor with a varactor
 - However, most varactors have limited tuning range, unless several volts can be applied.
 - A method to circumvent tuning range limits, is to use several smaller tuning ranges with switchable varactors.

Typical Colpitts Oscillator



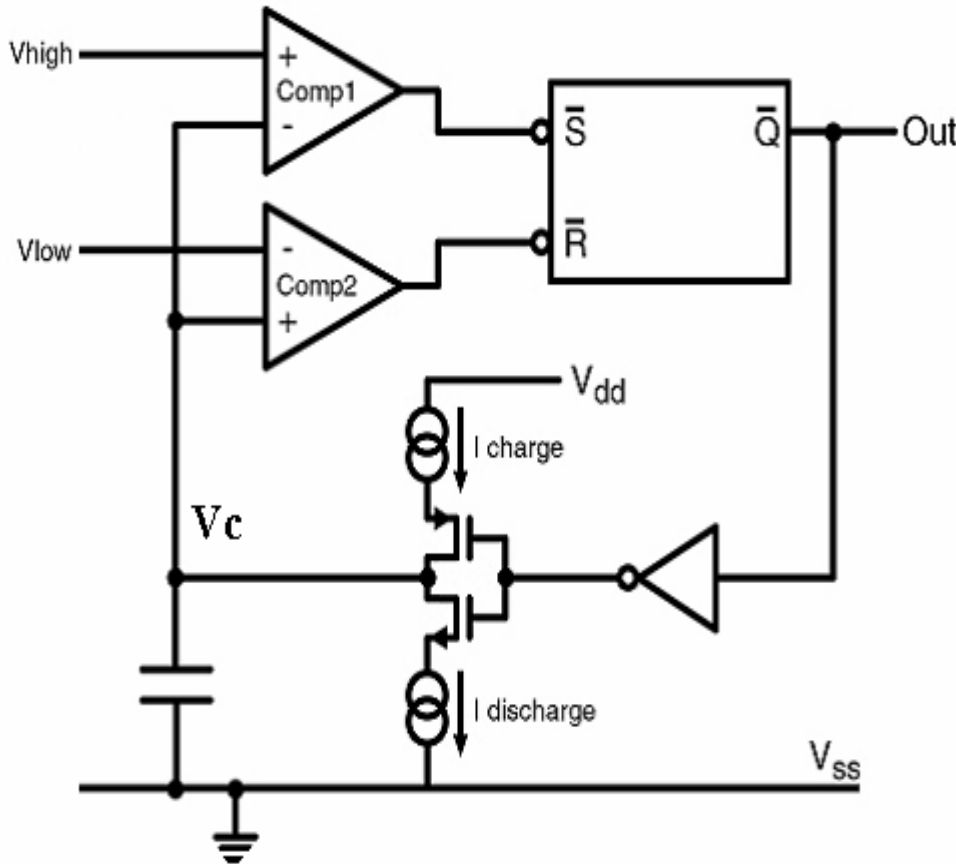
$$C_t = \frac{C_1 * C_2}{C_1 + C_2}$$

$$f_0 = \frac{1}{2\pi\sqrt{L_1 * C_t}}$$

This type of oscillator is more stable than ring or relaxation oscillators, a requirement in some wireless systems [7]

- Feedback loop C1, C2, L1 defines operating frequency
- SOI has reduced Capacitance parasitics to ground
- SOI has Inductors with improved 'Q', for improved stability

Relaxation oscillator (multivibrator)



Relaxation oscillator

- Operates by charging/discharging of capacitance between two voltages
- Controllable with V-controlled current source as charging / discharging current
- But is sensitive to thermal effects, supply voltage variation, and phase noise
- However, temperature stabilized current supplies, controlled voltage thresholds minimize these effects.
- Requires same precautions in comparator design as op-amp

SOI (in general FinFET in particular) and low power applications

SOI is generally good for Low Power:

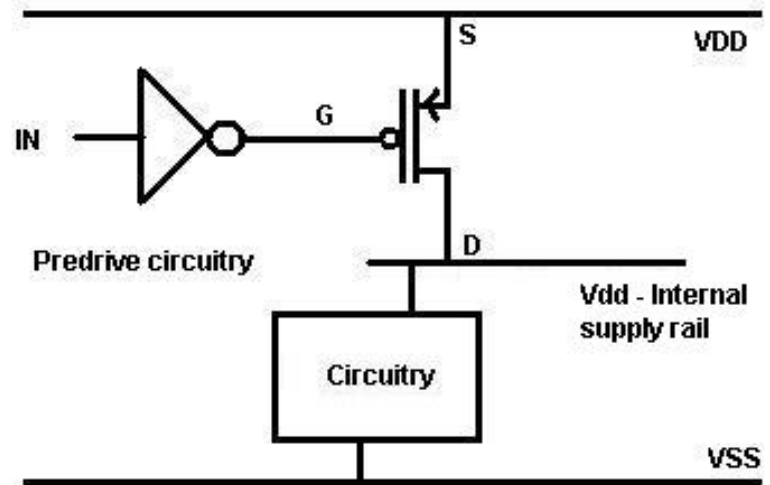
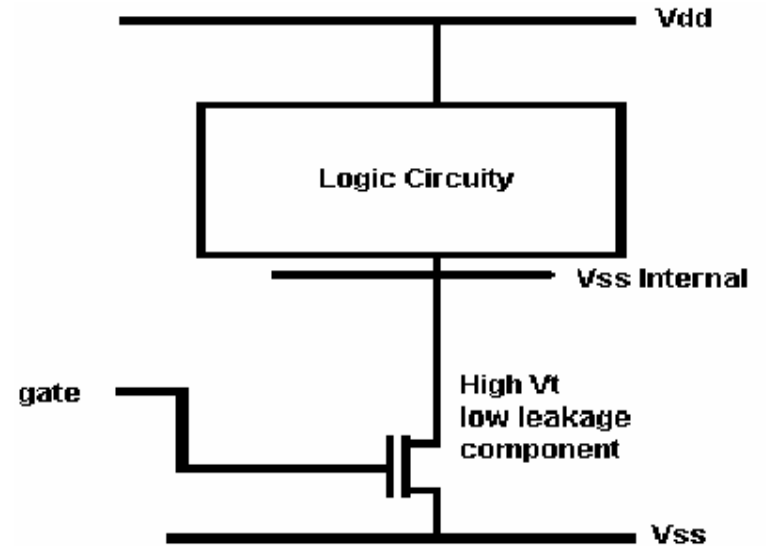
- Reduced parasitic capacitances reducing switching losses
- No leakage to substrate
- Flatter leakage profile with temperature
- Gate coupling – enhanced transient performance (PD-SOI)
- Biasable gate – lower off-state leakage, enhanced on-state performance (PD-SOI)
- Reduced noise coupling through substrate
- Fewer parasitics to cause leakage in standby operation modes.

But, SOI problems with low power:

- Lost ability to simple backbias (though other tr leakages reduced)
- MuGFET quantization possibly detrimental to SRAM power

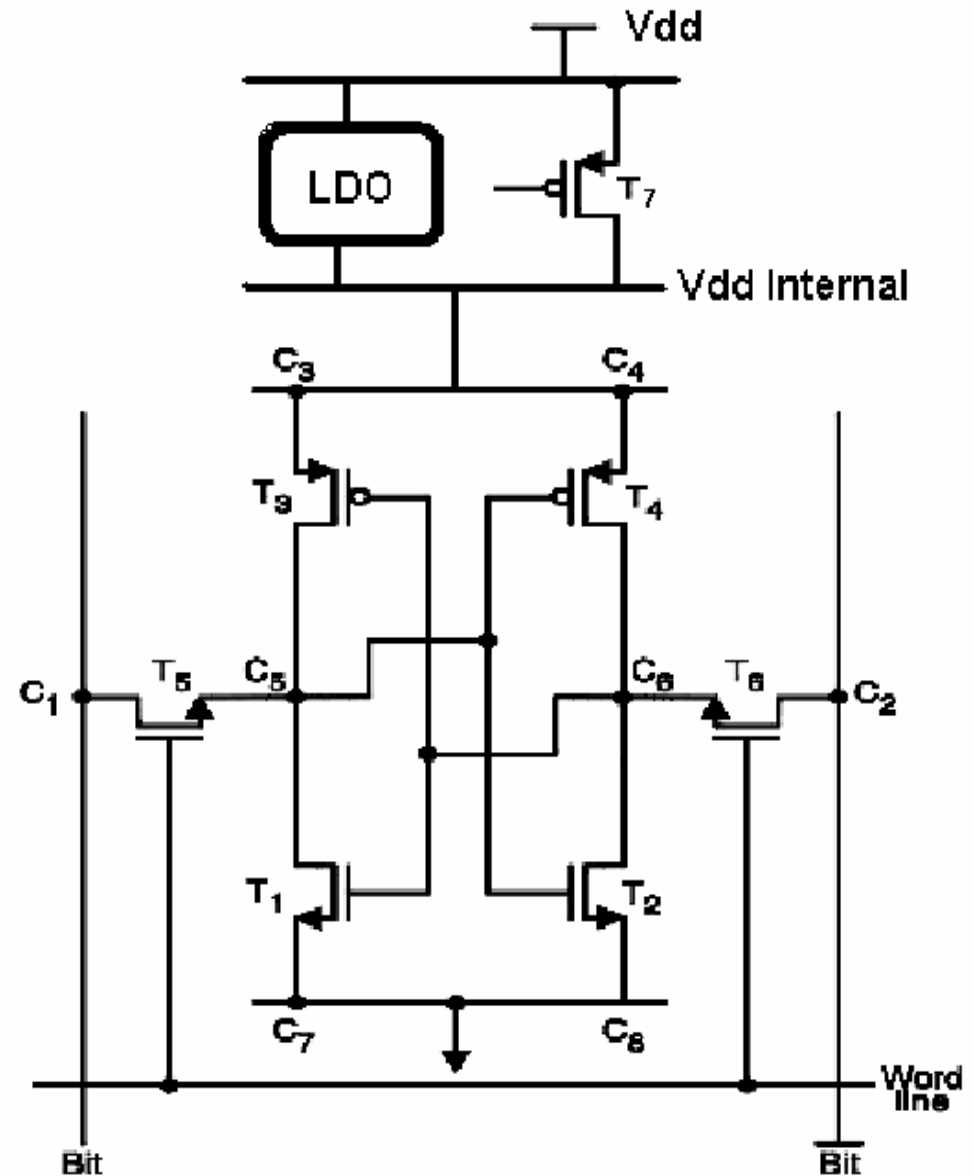
Standby Current Reduction Methods

- Footer switch
 - SOI universal substrate contact vs bulk, so fewer sneak paths
 - Chargepumped switch
 - Reduced breakdown concerns
- Header switch
 - Reduced area overhead for distributed Header (no guard rings)
 - Chargepumped switch
 - Easier to create a negative voltage CP
- SOI vs bulk
 - reduced circuitry capacitance (reduced losses between modes)
 - Reduced switching capacitance (smaller standby transistor)
 - Distributed transistors easier



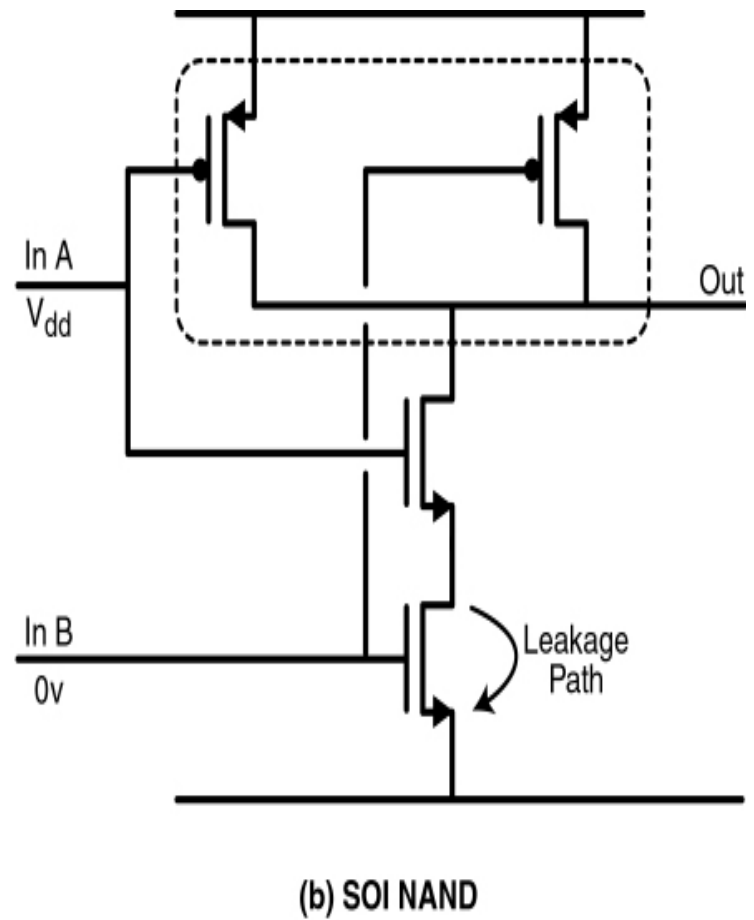
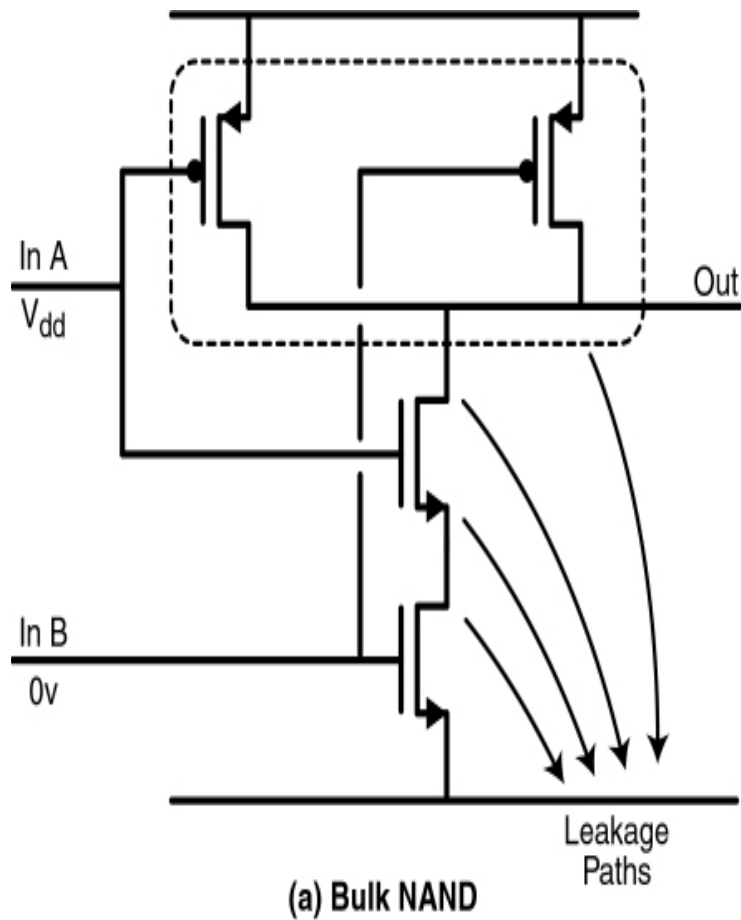
Standby Current Reduction Techniques (cont)

- SRAM power saving
 - must maintain data in standby
 - Noise margin
 - Retention only
 - by supply switching
 - Reduce supply voltage
 - Increase source voltage
 - Additional techniques
 - body bias (PDSOI)
 - float bit line



High Temperature Operation

- Circuits can operate at much higher temperatures using SOI material than possible using bulk material
- SOI general, and FD-SOI in particular has leakage 2-3 orders of magnitude lower than bulk at elevated temperatures
- Leakage is due to lower forward voltage drop of diodes at high temperatures, typical bulk processes display reduced immunity to noise, and an increased tendency to latch-up
- SOI circuit design avoids leakage to substrate
- In SOI overall leakage is defined by the lowest leakage component
- For most applications PD-SOI can operate to about 250°C [8]
- Bulk is marginal even at 200°C [9]
- Very high temperature systems often benefit from the use of fully-depleted silicon, when operation is possible up to 300°C or higher



Junction leakage paths associated with a NAND (a) in bulk and (b) in SOI material, showing leakage path through the off-state SOI device, reverse biased diodes, and the PMOS well in bulk material

System on a Chip (SOC)

- Combination of Analog and Digital design for SOCs
 - Look for SOC SOI in the next five years
 - SOI, probably Mugfet, with optional planar FD-SOI/PD-SOI
 - In general power supply voltages 1-1.2v
 - falling to 0.7-1.0v by 2010
 - Benefits of SOI for SOC are:
 - Noise Isolation
 - power output to input
 - digital to sensitive analog
 - Low power
 - Will require all techniques currently used and more
 - gate leakage (integrators, ADC)
 - power management (dynamic voltage scaling)

Summary

- A Brief discussion of the differences between MuGFET, FD/PDSOI and bulk with details of the active and passive components
- Circuit design for FinFET SOI material shares strong similarities to circuit design for bulk – based silicon, though optimization is required between the two process types.
- Basic digital and analog circuits have been described, and verification of silicon performance shown
- Correlation of simulation to silicon has been demonstrated using BSIM4 and TiSPICE
- Thank you for your attention

References

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