IEEE Dallas CAS Chapter

Frequency Synthesizers in Nanometer CMOS

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TEXAS INSTRUMENTS

Outline

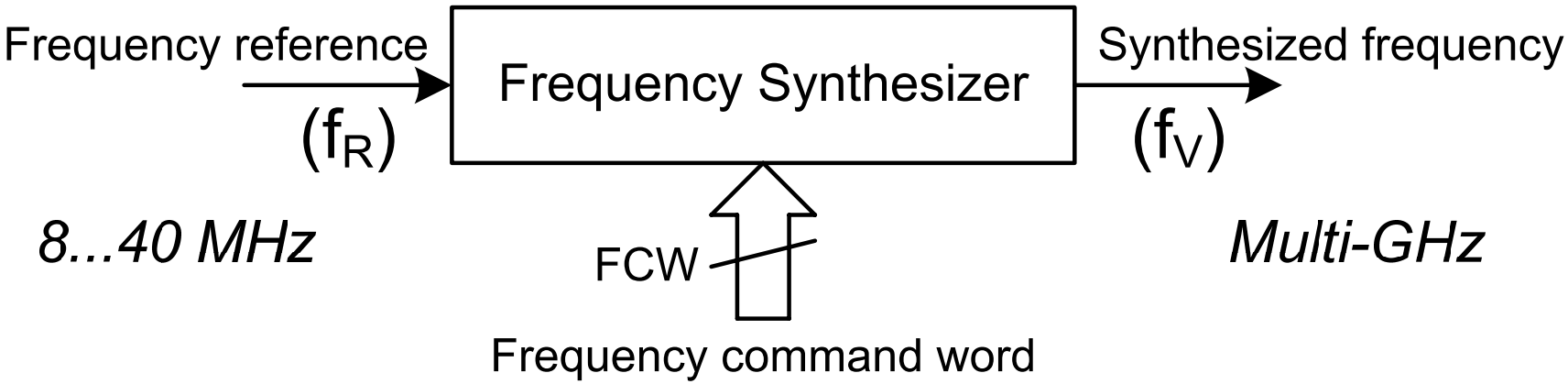
- RF frequency synthesis fundamentals
  - Motivation for digitally-intensive PLL
- New paradigm in nanometer-scale CMOS
- All-digital phase-locked loop (ADPLL)
- ADPLL wideband frequency modulation
- Conclusion

Frequency Synthesis in Radio Transceivers

Local Oscillator in a Radio Transceiver

- Local oscillator (LO) is needed in every radio TX and RX
  - Irrespective of the architecture
- Needed to translate RF frequency down to IF or baseband (in RX) and vice versa (in TX)
- LO has to be tunable across the RF wanted frequency band and the frequency resolution has to be at least equal to the channel spacing
- **Frequency synthesizer** is used as LO
- RF frequency synthesizers remain one of the most challenging blocks in mobile wireless communication systems

Local Oscillator



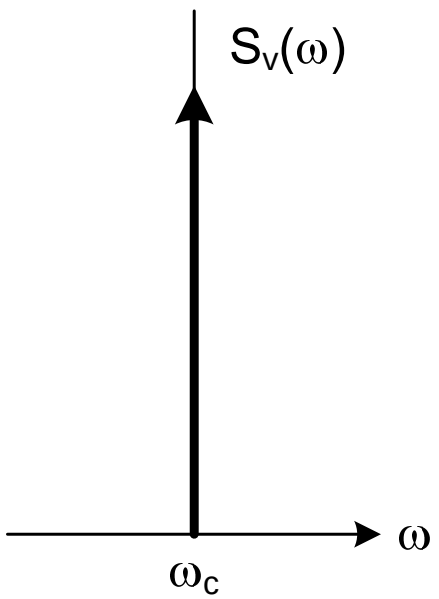
- Frequency reference (FREF) source usually built as tunable crystal oscillator (XO)
  - Voltage-controlled temperature-compensated XO (VCTCXO)
    - External module; expensive (~$1)
  - Digitally-controlled XO (DCXO)
    - Requires external XTAL (~$0.2)
  - MEMS resonators
    - Emerging technology
- Three major frequency synthesis techniques:
  - Direct-analog (error correction process is avoided)
  - Direct-digital
  - Indirect or phase-locked loop

Phase Noise in Oscillators

- Ideal oscillator: power concentrated at ω_c
  - Dirac pulse in frequency domain
- Real oscillator: phase is time-varying
  - Spectrum will exhibit “skirt” around the carrier frequency

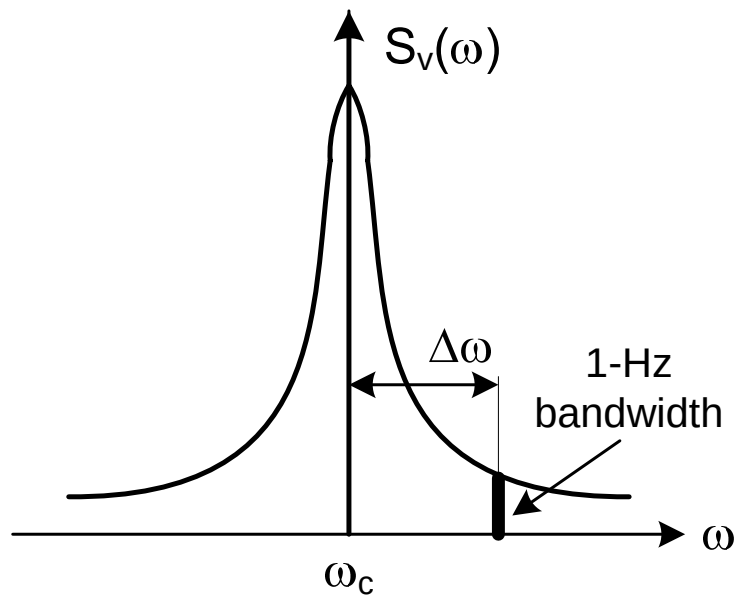
$$v(t) = A \cdot \cos(\omega_c t + \phi)$$

Ideal Oscillator



$$v(t) = A \cdot \cos(\omega_c t + \phi(t))$$
$$v(t) \approx A \cdot \cos \omega_c t - A \cdot \phi(t) \cdot \sin \omega_c t$$

Practical Oscillator



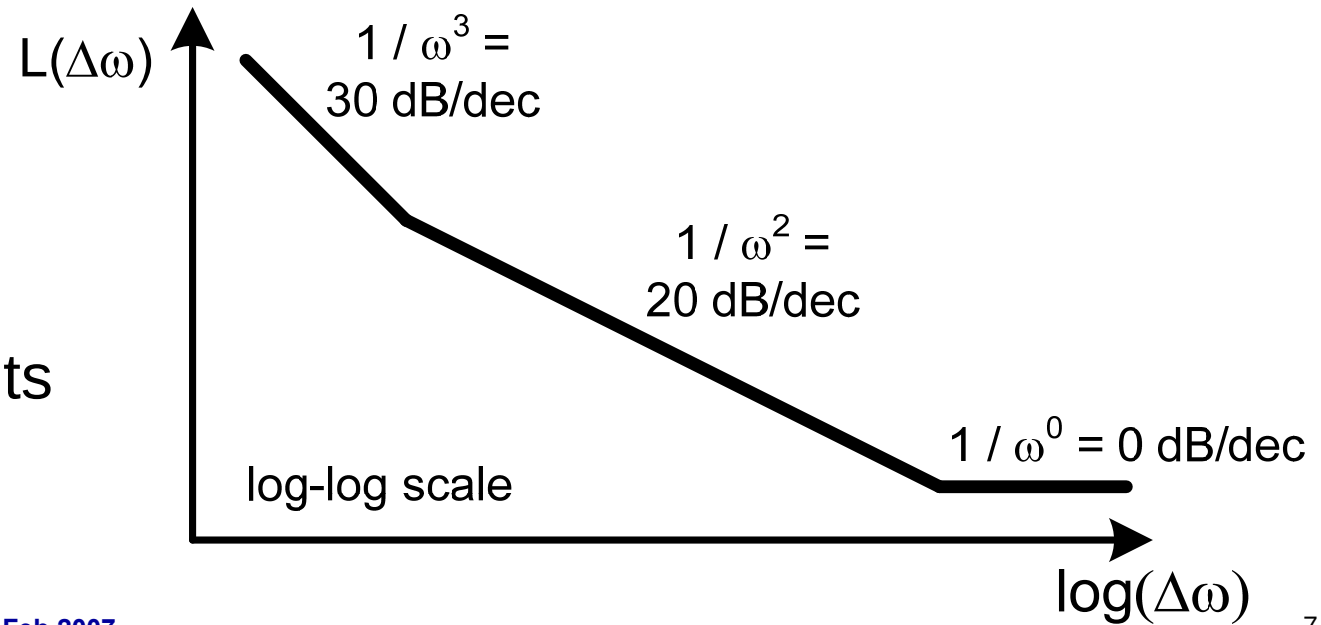
Single side band noise

$$L(\Delta\omega) = \frac{S_\phi(\Delta\omega)}{2}$$

Phase Noise Profile

- $1/\omega^0$: thermal noise added to the clock outside of the oscillator proper; does not affect the oscillation time base
- $1/\omega^2$: upconverted thermal (AWGN) noise; caused by uncorrelated timing fluctuations in the period of oscillation; modeled as random walk
- $1/\omega^3$: upconverted flicker (1/f) noise; significant in thin-oxide MOS transistors

- RF oscillator phase noise spectrum exhibits three regions



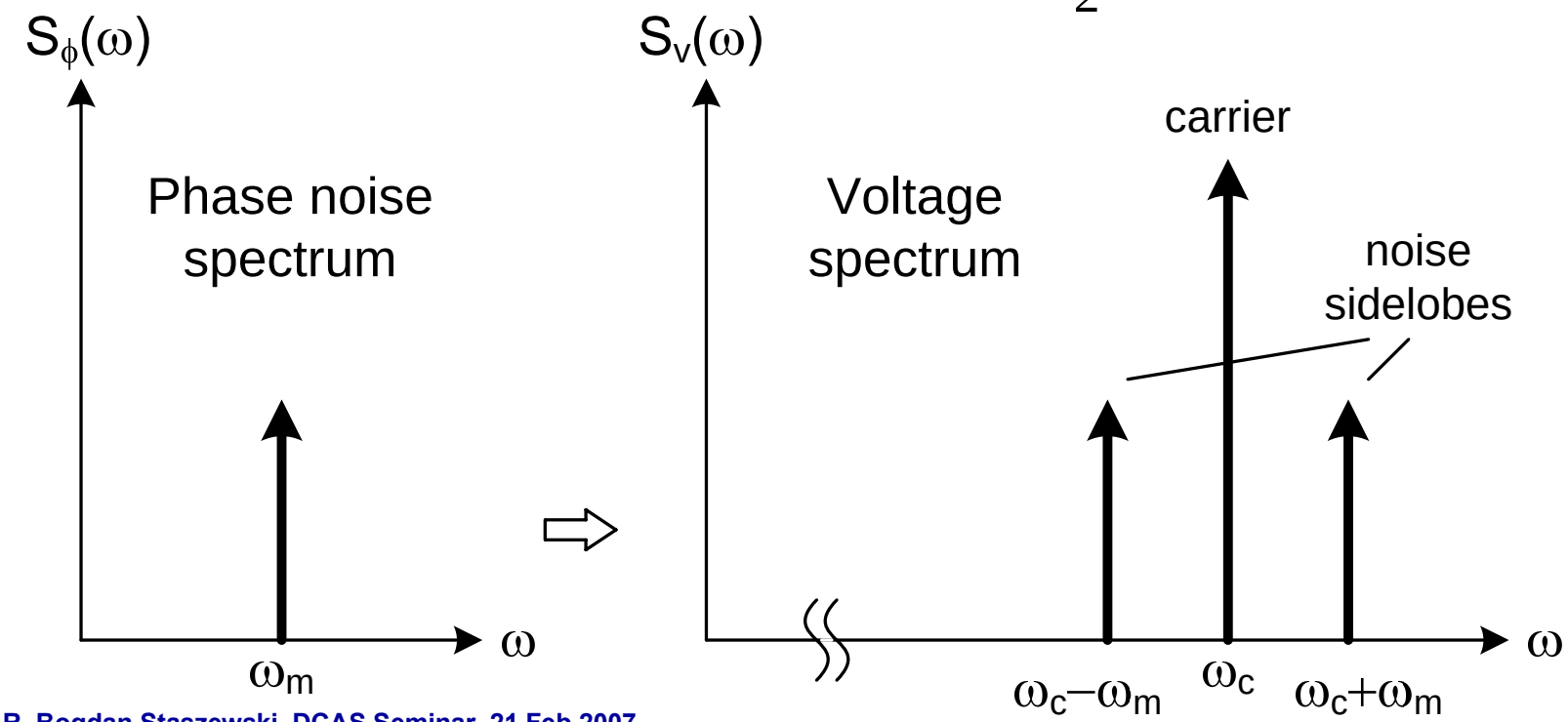
Oscillator Spurious Tones

- Periodic (systematic) content in the phase noise will exhibit itself as undesired spurious tone sidelobes upconverted around the carrier

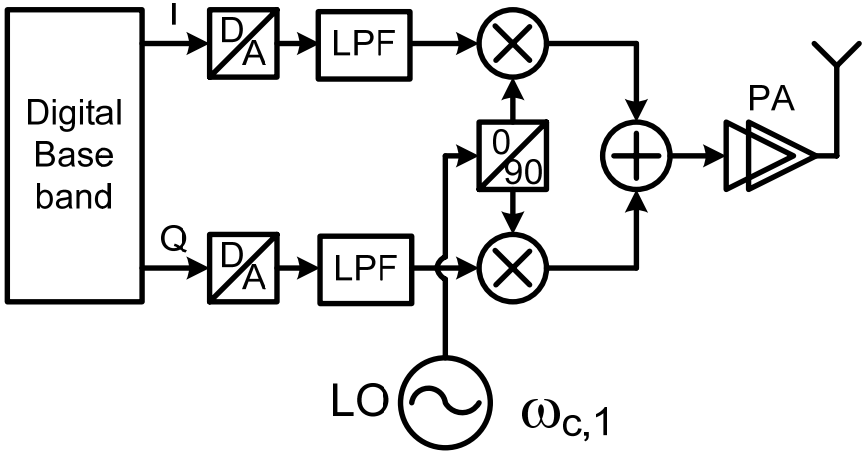
$$\phi(t) = \phi_p \cdot \sin(\omega_m t)$$

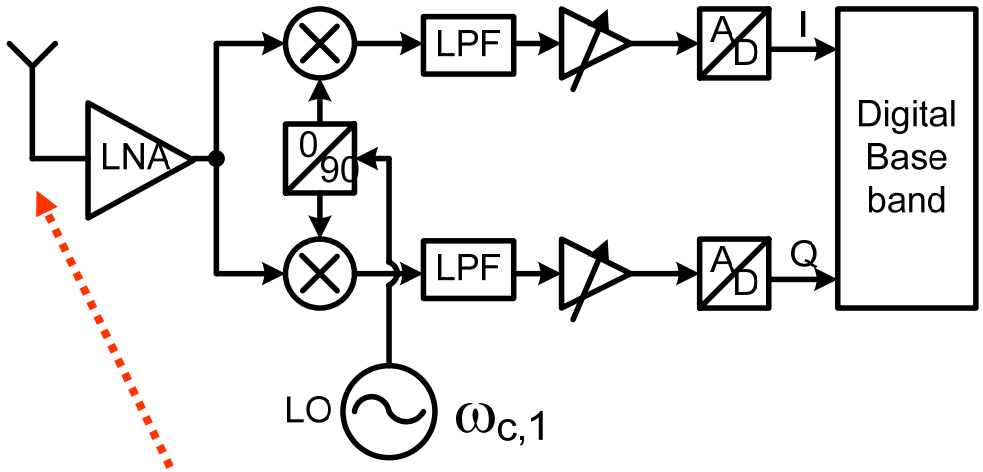
$$v(t) = A \cdot \cos(\omega_c t + \phi(t))$$

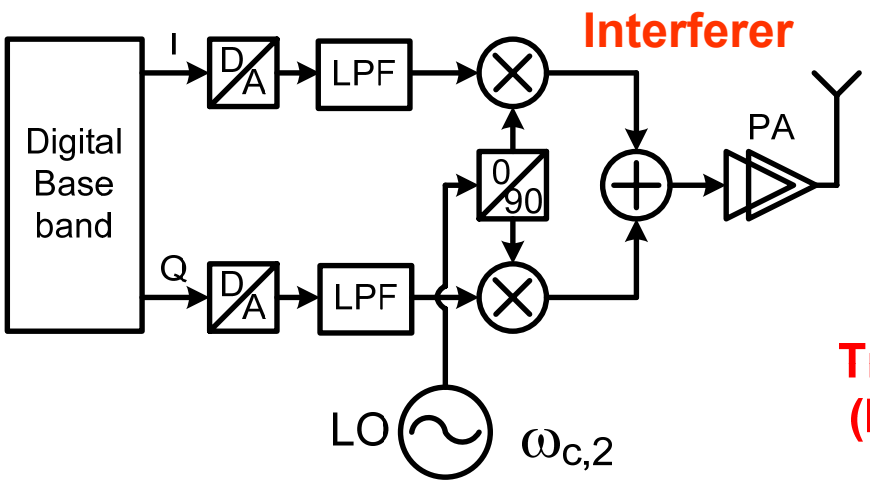
$$v(t) \approx A \cdot \cos \omega_c t + \frac{A \cdot \phi_p}{2} \cdot [\cos(\omega_c + \omega_m)t - \cos(\omega_c + \omega_m)t]$$

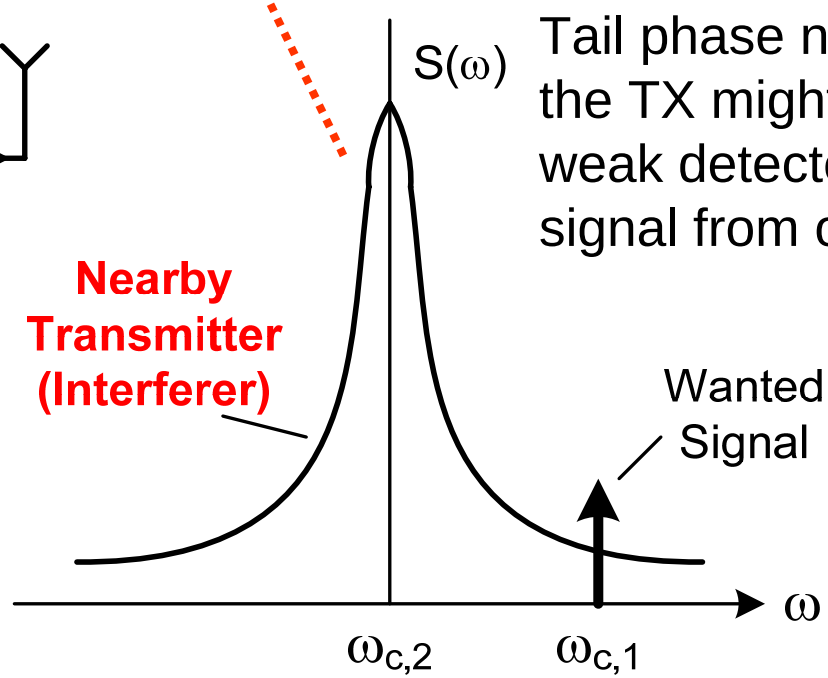


LO in Transmitter



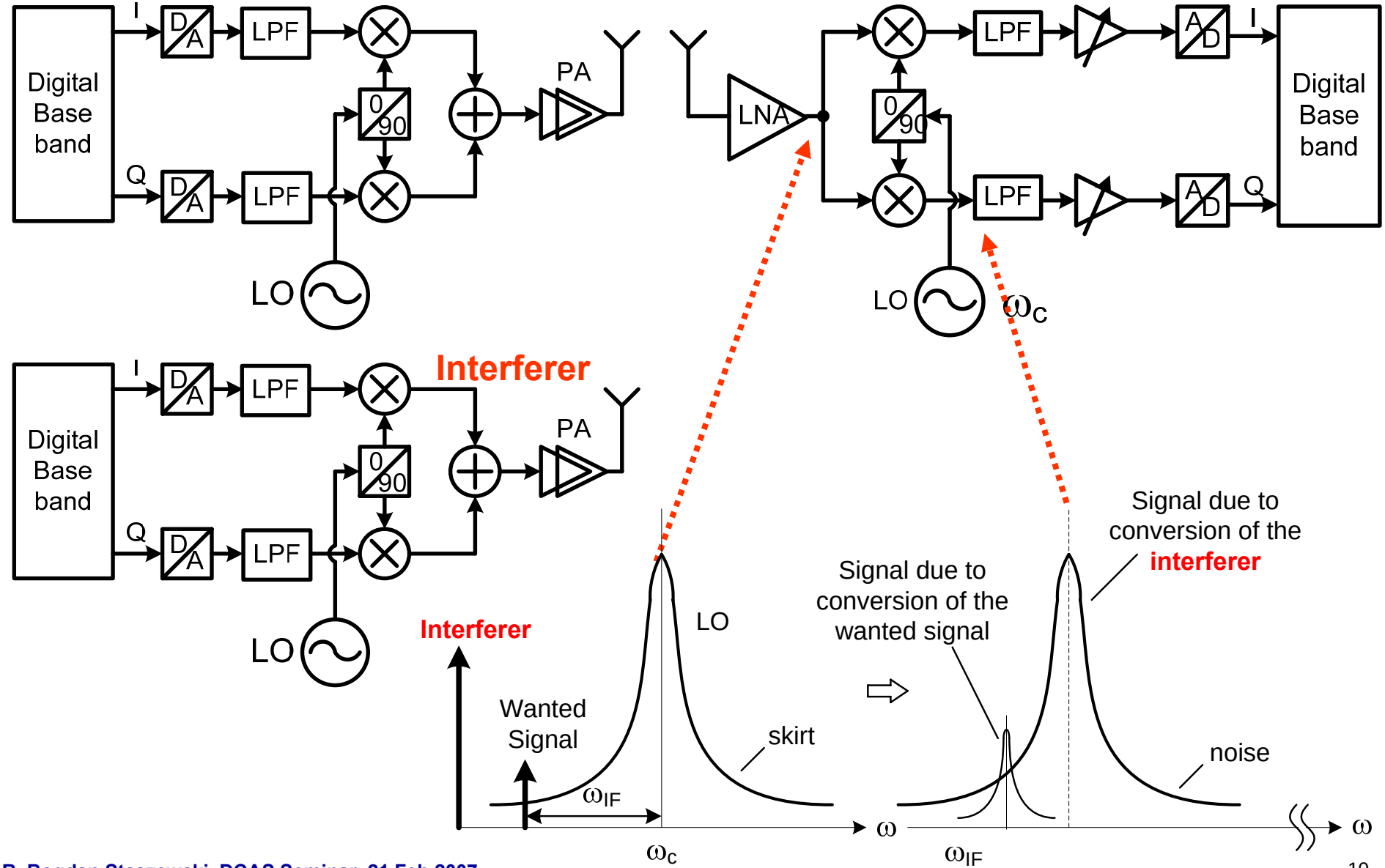






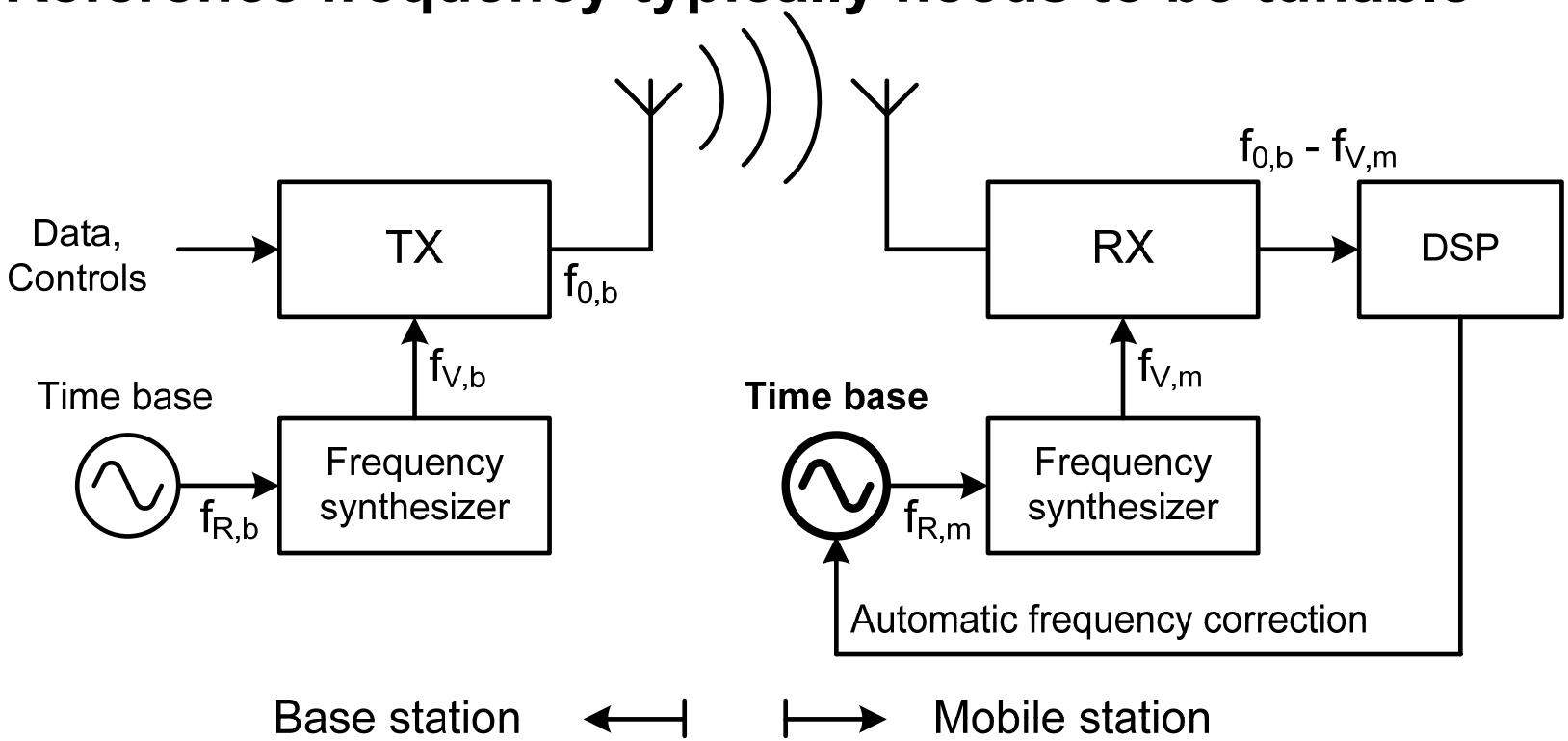
Tail phase noise of the TX might corrupt weak detected signal from other TX

LO in Receiver

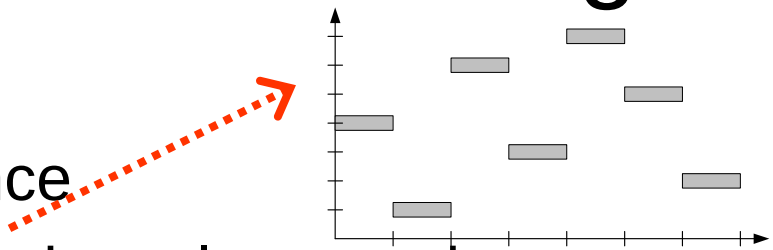


Synchronization of a Mobile Station

- LO needs to be accurate and stable to 0.1 ppm
  - i.e., 200 Hz at 2 GHz
- Crystal's inaccuracy more than 10 ppm
- Mobile station uses base station for synchronization
  - Automatic frequency control (AFC)
- => **Reference frequency typically needs to be tunable**



Frequency Synthesizer Ranking

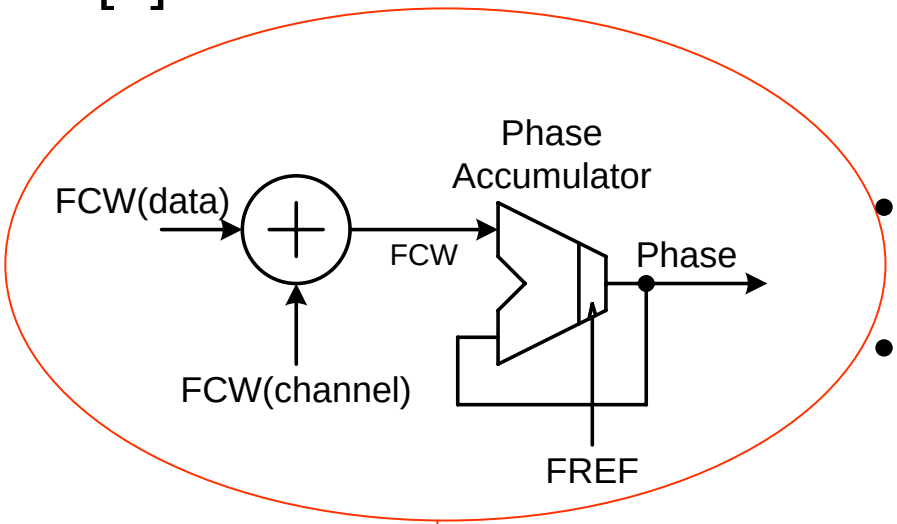


- Phase noise performance
- Discrete spurious noise performance
- Switching speed – for channel hopping, sleep modes
- Frequency and tuning range – operational band plus PVT margin
- Power consumption – battery operated mobile devices
- Size – mass production deployment
- Integrateability – integrate with digital logic and memory
- Cost – no extra cost added to the process; minimal count of external components
- Testability – low testing costs; built-in self test (BIST)
- Portability – ability to transfer the design from one application to another and from one process to another

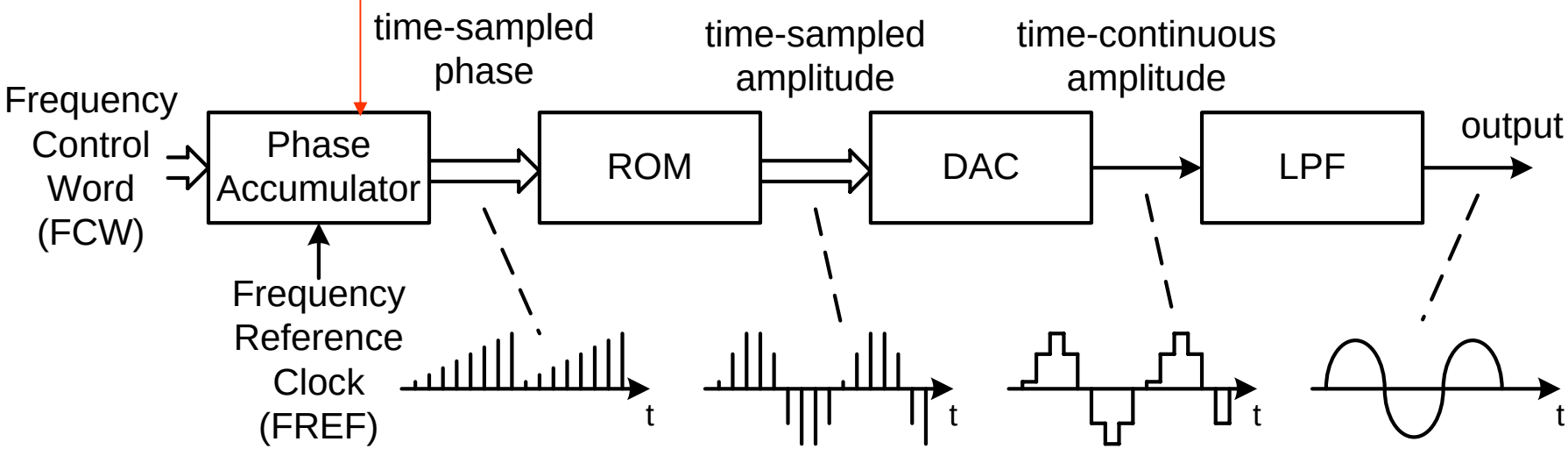
Frequency Synthesis Types

Direct Digital Synthesis (DDS)

- Developed by Tierney [1] in 1970s



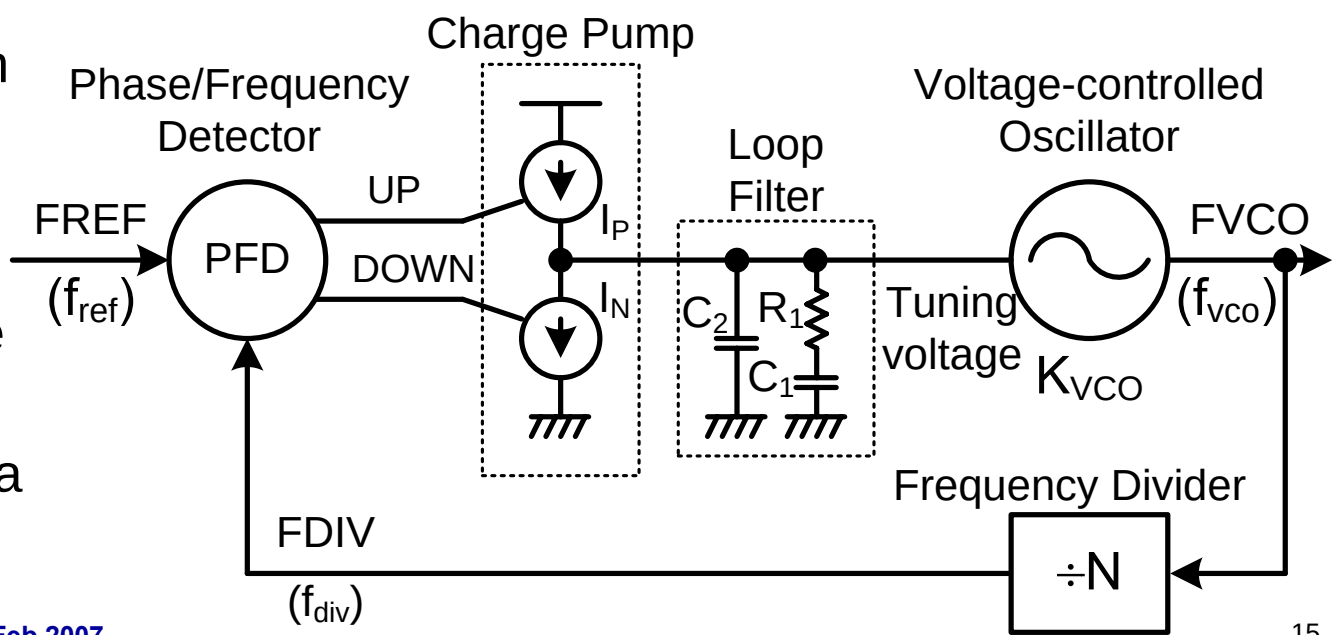
- Digitally constructs the desired signal
  - Amplitude, frequency and phase are known and controlled at all times
- Not entirely digital
  - Requires DAC and LPF
- Not feasible at GHz frequencies
  - Clock has to be at least 3x of the output frequency



Indirect Synthesis: Charge-pump PLL

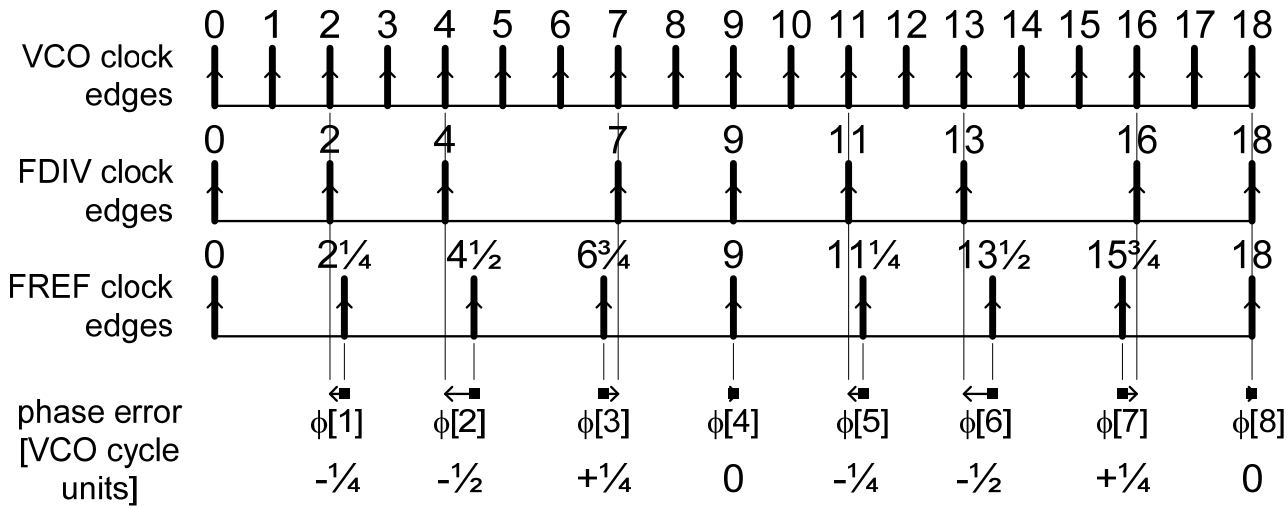
- Phase difference estimated in PFD by measuring time difference between f_{ref} and f_{div} closest edges, hence fundamentally slow acquisition
- Frequency acquisition time is proportional to the initial $\Delta f / f_{BW}$
- Disadvantage: slow acquisition and difficult to integrate
  - Difficult to integrate: VCO and large charge-pump caps
- Conflict in frequency switching time and suppression of spurs
- Only suitable for narrowband transmit modulation

- PFD produces current pulse I_p with prop. duty cycle
- Loop filter converts the current into a VCO tuning voltage
- C_2 is an integrating capacitor and puts a pole at dc



Fractional-N Synthesizer

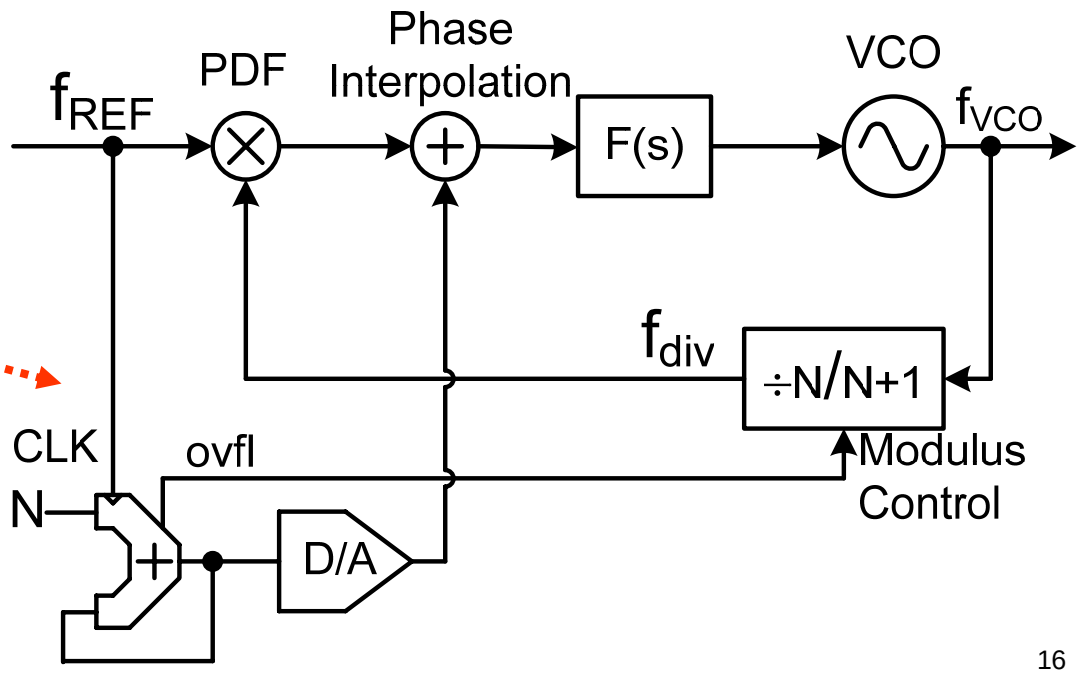
- Frequency tones (spurs) due to repetitive phase shift
- Easy to predict in a digital manner -- accumulator



Kingsford-Smith
US patent 3,928,813
1974 (filing date)

Spur reduction techniques:

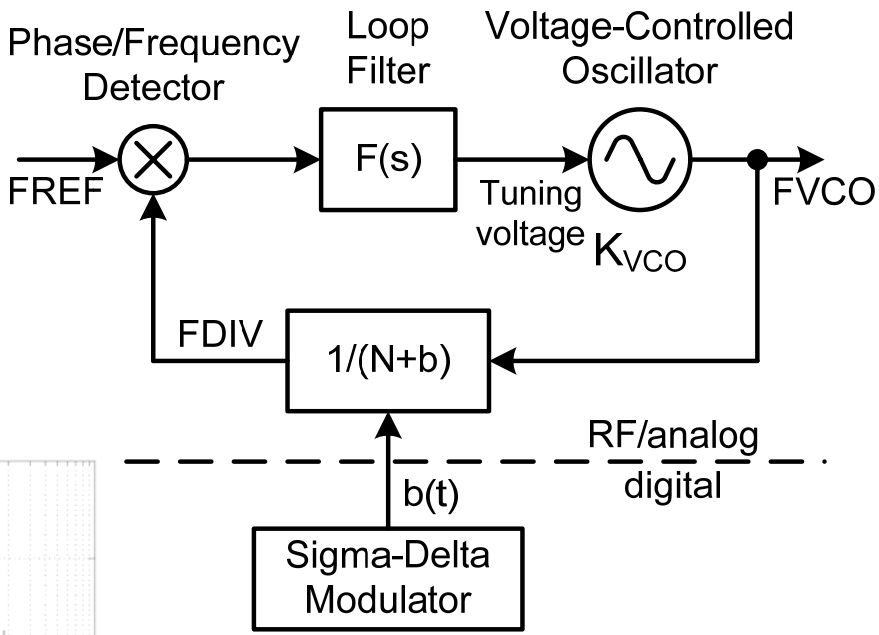
- Analog compensation schemes – phase interpolation
- Sigma-Delta modulator

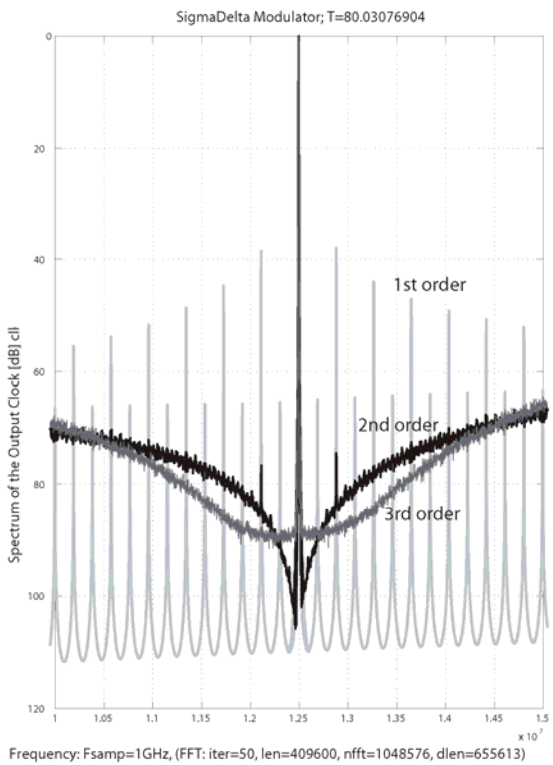


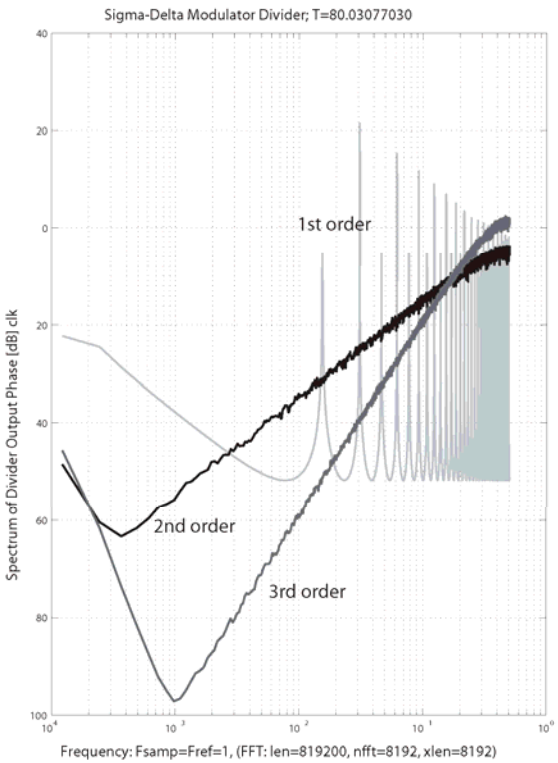
Sigma-Delta Fractional-N Divider

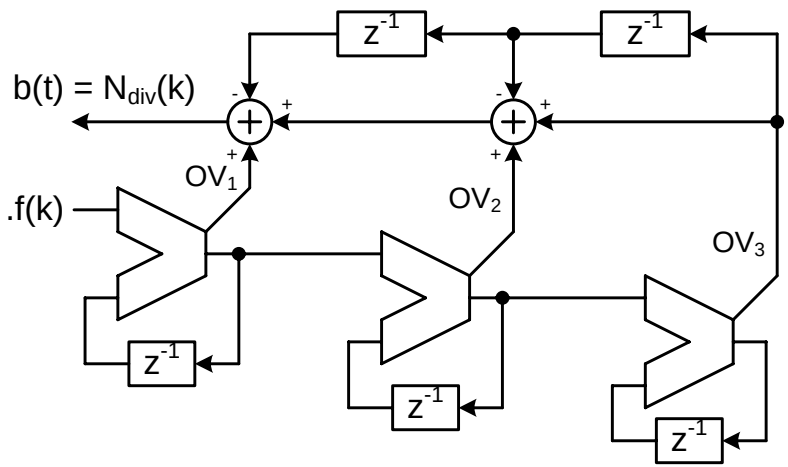
Riley	Wells
US patent 4,965,531	US patent 4,609,881
1989 (filing date)	1984 (filing date)

ΣΔ modulator shapes the quantization error energy into higher frequencies which are then easy to filter out



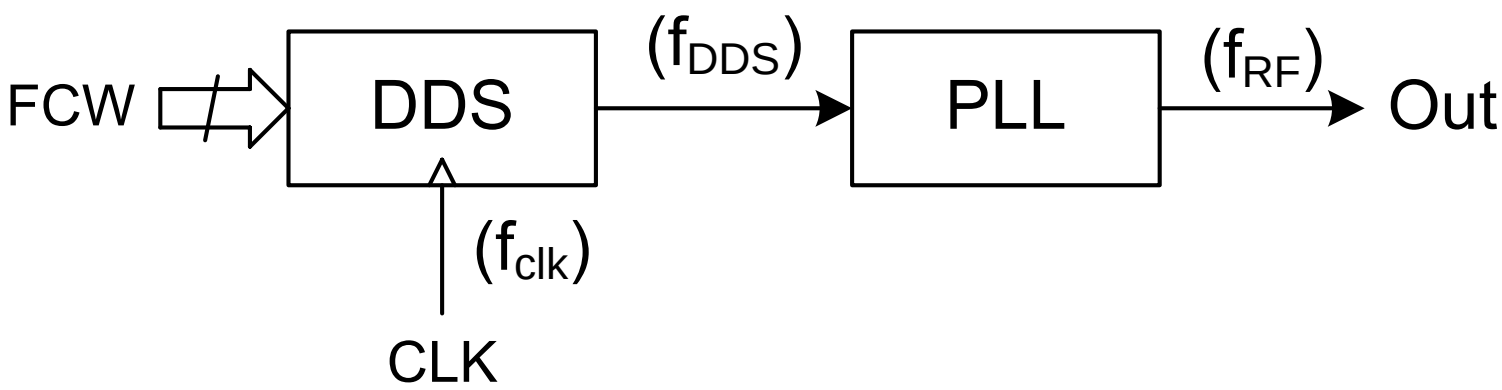






Hybrid of DDS and PLL

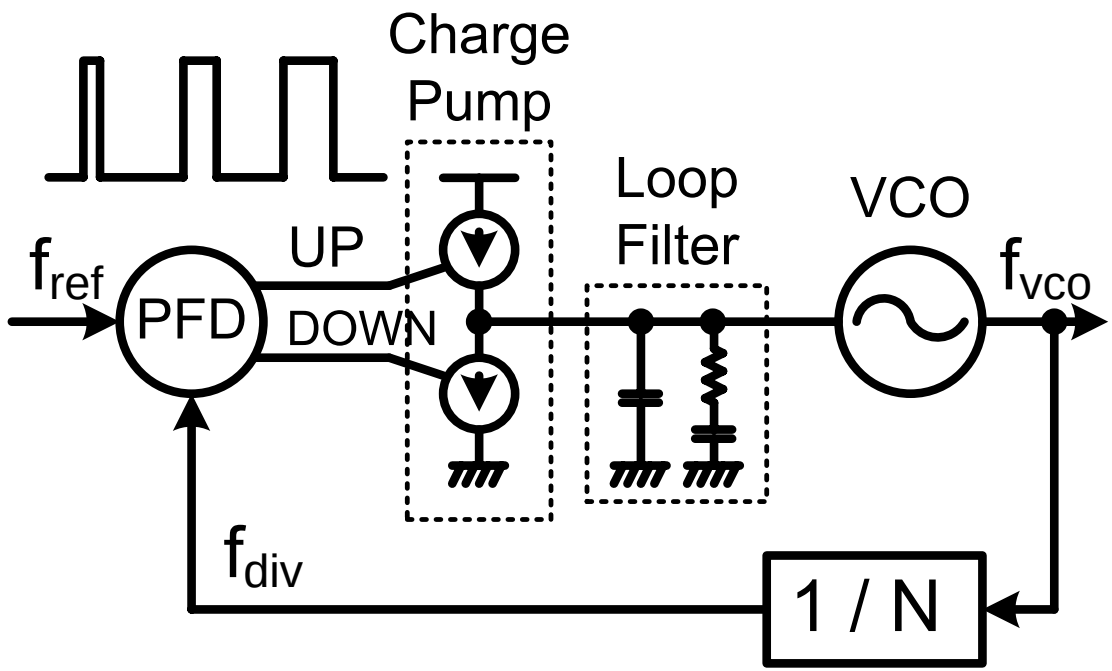
- DDS combined with PLL
- DDS operates at lower frequency: wideband modulation and fast channel hopping capability
- PLL used as frequency multiplier to up-convert the DDS output to RF band
- Used in basestations
  - Fast settling time



Motivation for (All?)-Digital PLL

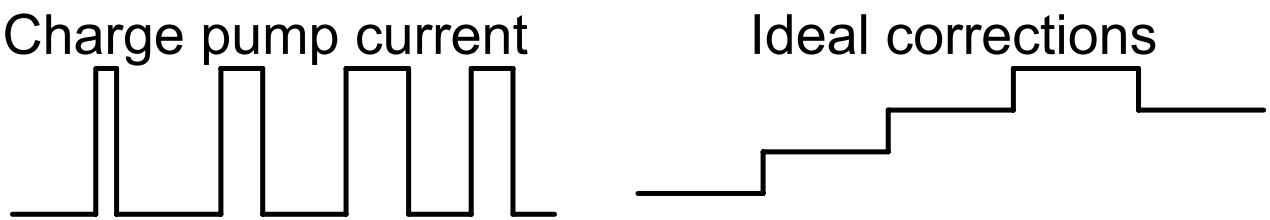
- Frequency synthesizers in commercial wireless applications traditionally use charge-pump PLL's
- No prior reports on successful low-cost synthesizer architectures for mass-market mobile communications employing *all-digital* approach
- Design flow and circuit techniques are analog intensive

- Technology incompatible with modern digital baseband processors
  - Use low-voltage nanoscale CMOS



Phase Domain Operation

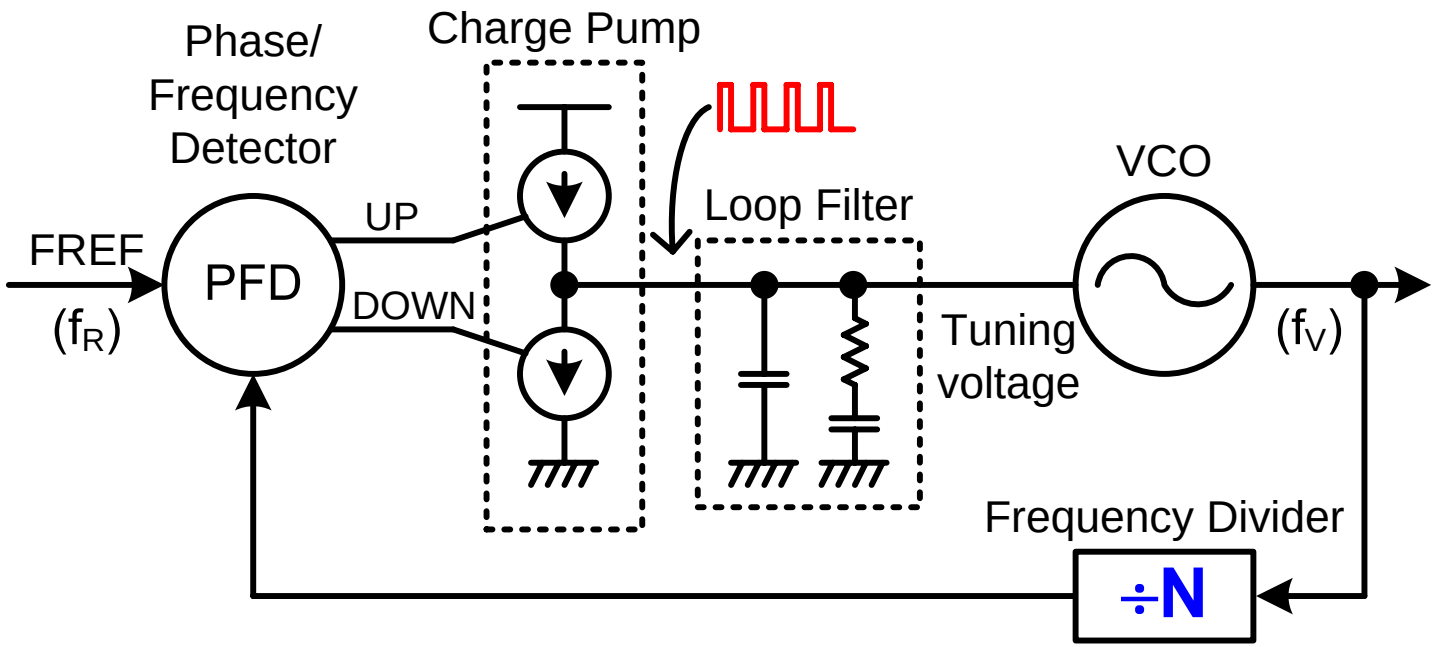
- Charge-pump PLL does not truly operate in the phase domain: only approximation under lock
  - [2: Gardner'80] describes: "converting the timed logic levels into analog quantities"
  - Generates reference spurs that require filter



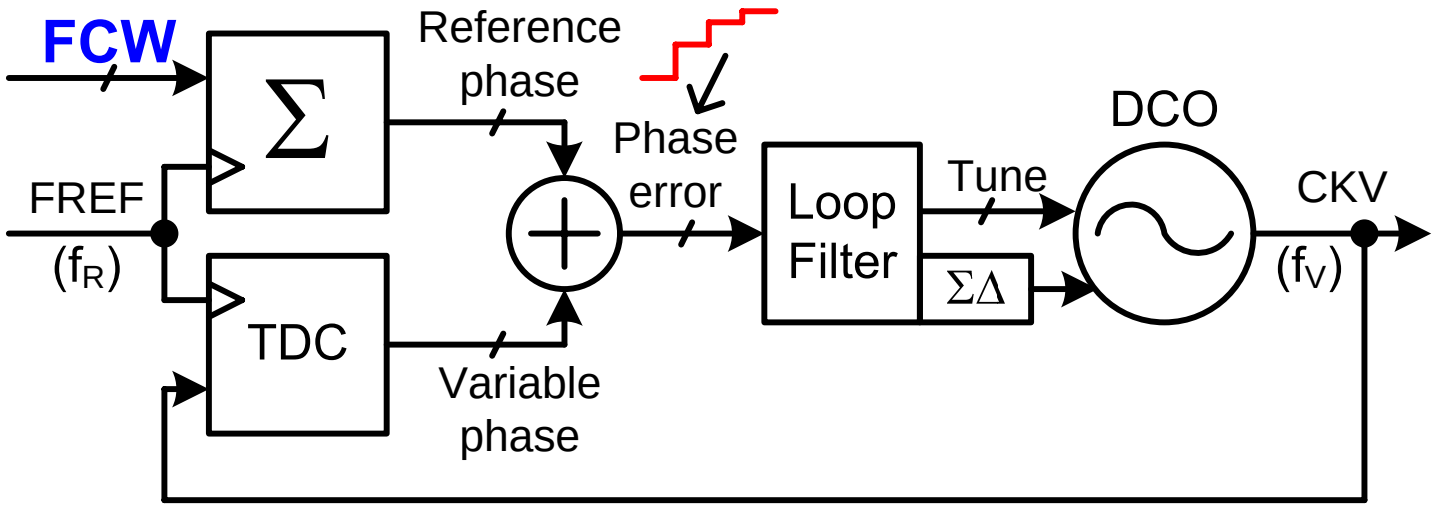
- Consequence: tradeoff between the reference spur level and settling time
- No such tradeoff with true phase-domain operation
  - See [3: Kajiwara'92]

Preview: All-Digital PLL

- Charge-pump PLL:
- Suffers from reference spurs
- Tradeoff: bandwidth against spur level

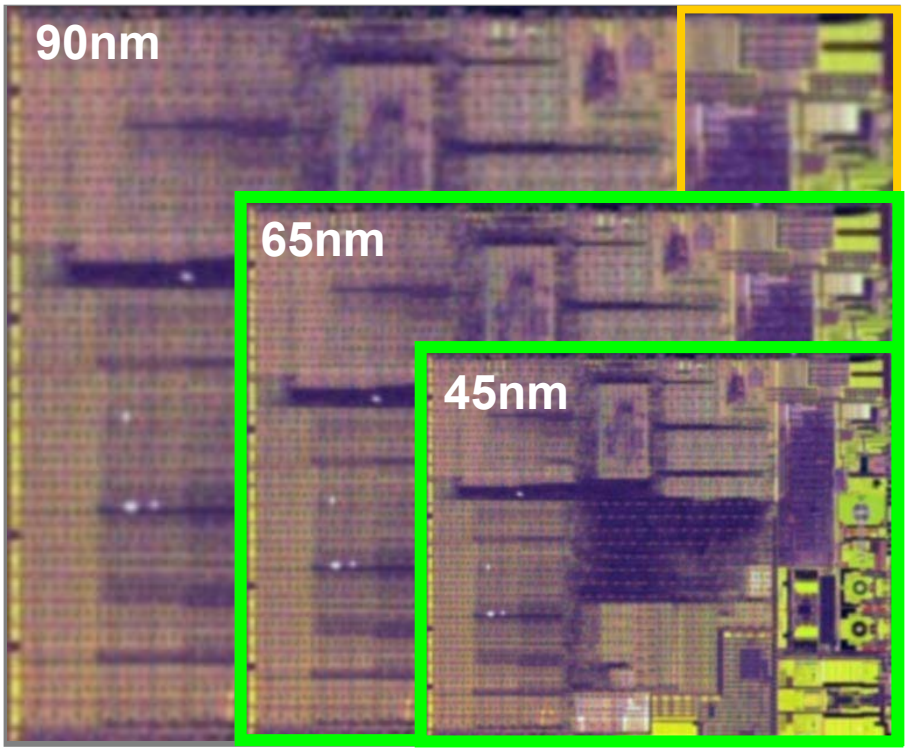


- All-digital PLL:
- True phase domain operation
- (Details to come…)



Nanoscale CMOS

SoC Drives Cost Reduction



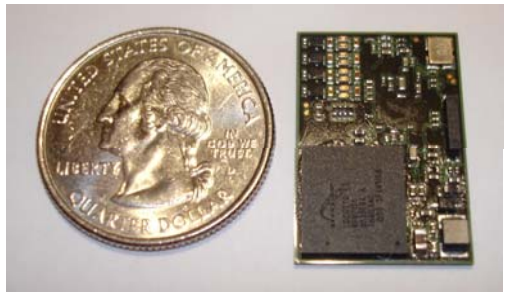
- 2x area reduction each process technology node
- RF/analog is 20-30% of SoC

- SoC Integration Includes:
  - RF
  - Analog
  - Power management
  - Digital baseband
  - SRAM
  - Processors
  - Software

- Most advanced process technology used to maximize integration while minimizing cost
  - 90nm (shipping)
  - 65nm (mature design)
  - 45nm and beyond (preliminary)

Why Single-Chip Radio?

- "Integration is like gravity"
  - Already happened in hard-disk drives, ADSL, etc
  - Not a single example of reversal
- "$20 phones"
- Large untapped market in India and China
- More "real estate" space for advanced features
- Better reliability
  - Today, more than half of the total components on a board are analog RF components
- Longer talk time



Old Platform

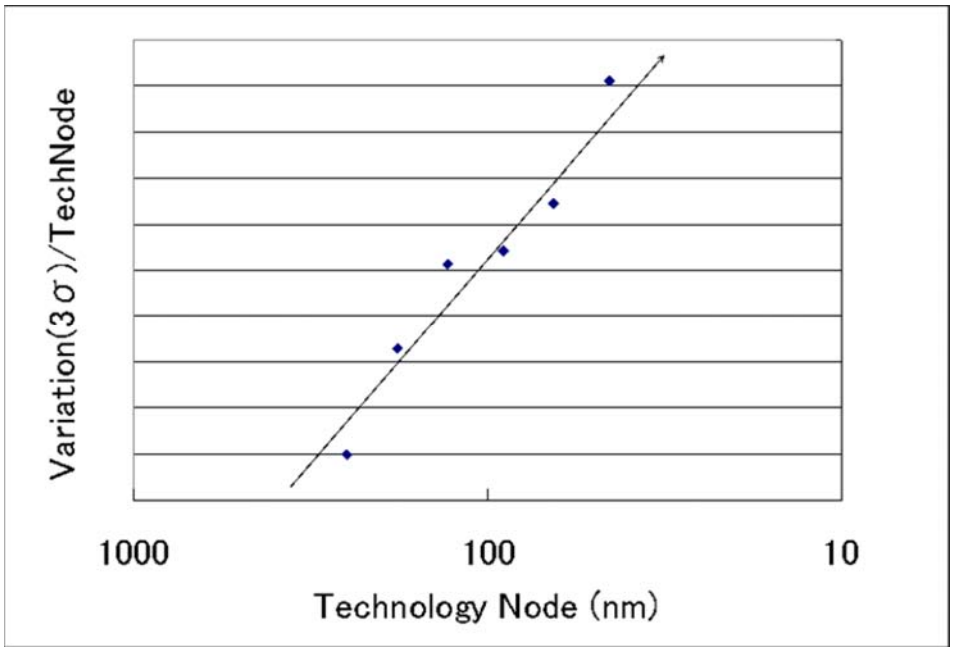
Technology Trends for 45 nm CMOS

- 45 nm doubles transistor density over 65 nm and quadruples over 90 nm technology
  - To support more standards, radios and multimedia in mobile phones
- Smaller transistor capacitances hence lower power dissipation
- Nominal supply voltage of 1.1 V; ranging from 0.9 V to 1.2 V
- SRAM size of 0.24 um^2 optimized for size
- Conventional gate stack of nitrided silicon dioxide and polysilicon gate
  - Metal gate only for high-performance process (SUN Sparc)
- No high-k dielectric
  - Very little performance gain compared with higher complexity and cost
- New package technology
  - Stacked die for embedding of large memories
  - Dies embedded in a board to maximize space and performance

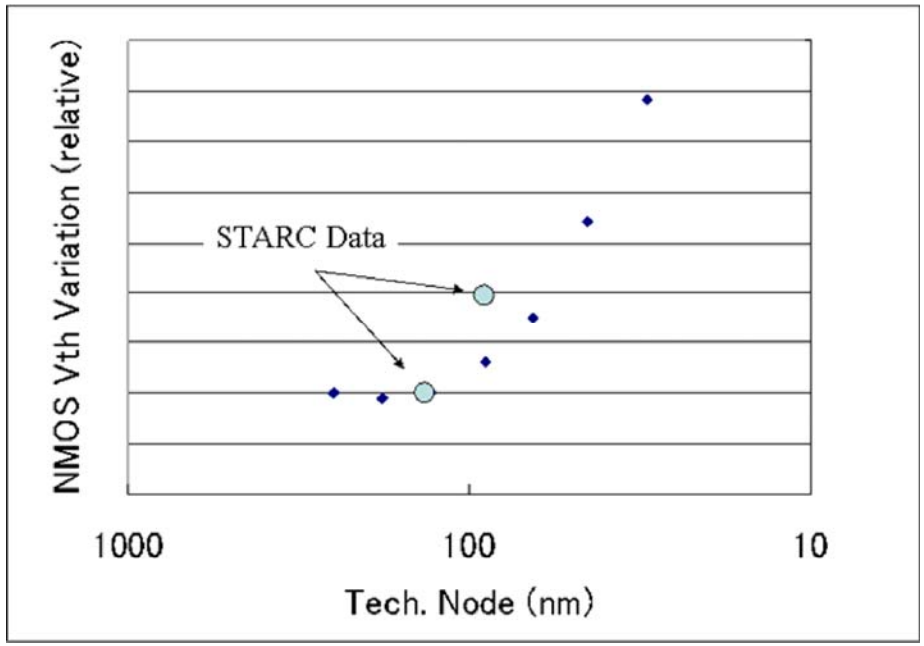
Nanoscale CMOS Technology Trends

- Variability of minimum size devices gets worse with each process node
- Source: ISSCC 04, Microprocessor Forum, p29

Relative Gate Length (CD) Variation



Relative NMOS Vth Variation



New Paradigm

In a highly-scaled CMOS technology, time-domain resolution of a digital signal edge transition is superior to voltage resolution of analog signals

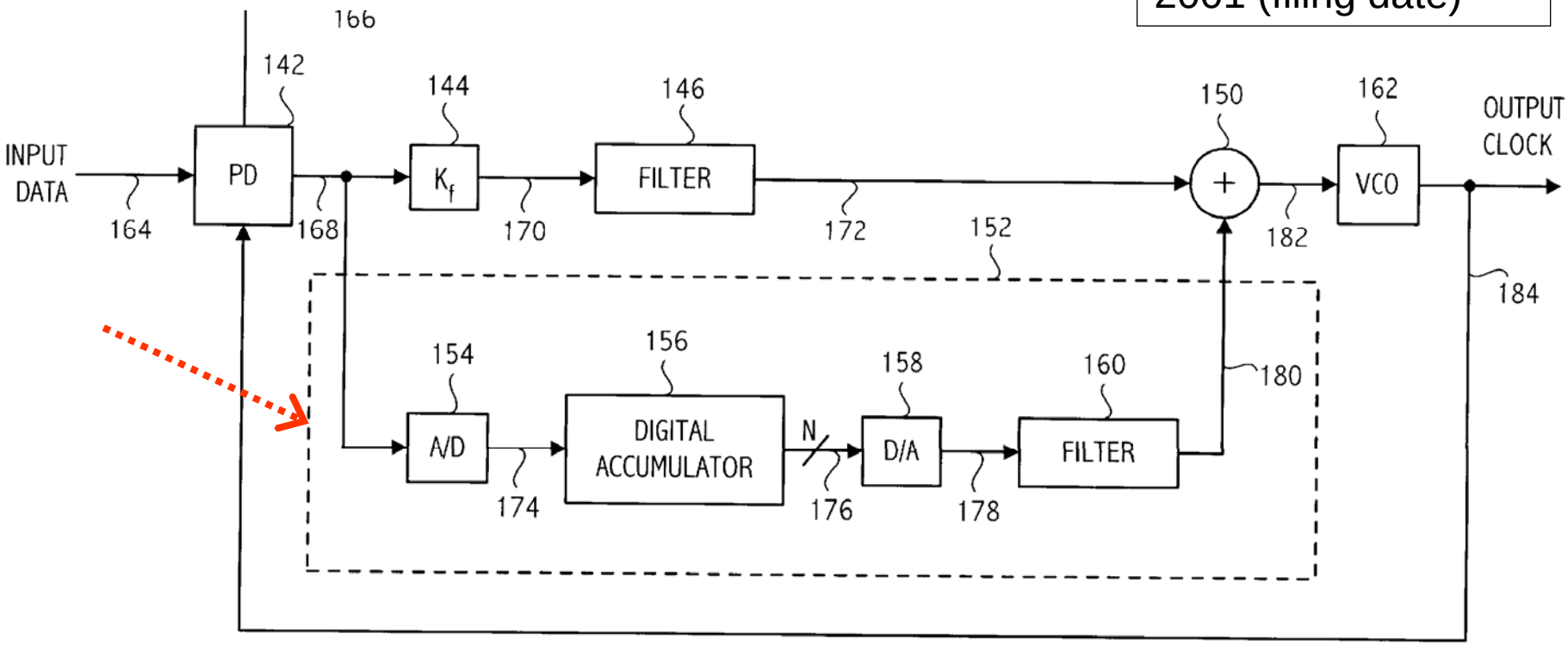
Rules of nm-Scale CMOS

- **Exploit:**
  - Fast switching characteristics of MOS transistors
    - 20 ps transition and f_T of 250 GHz in 45-nm CMOS
    - Improves 20% per process node (18—24 months)
  - Small device geometries and precise device matching
  - High density of digital logic: 1 Mgates/mm^2 in 45-nm CMOS
    - 2x scaling at each process node (18—24 months)
  - High density of SRAM memory: 4 Mbits/mm^2 in 45-nm CMOS
- **Avoid:**
  - Biasing currents for analog circuits
  - Reliance on voltage resolution
  - Nonstandard devices not needed for memory and logic

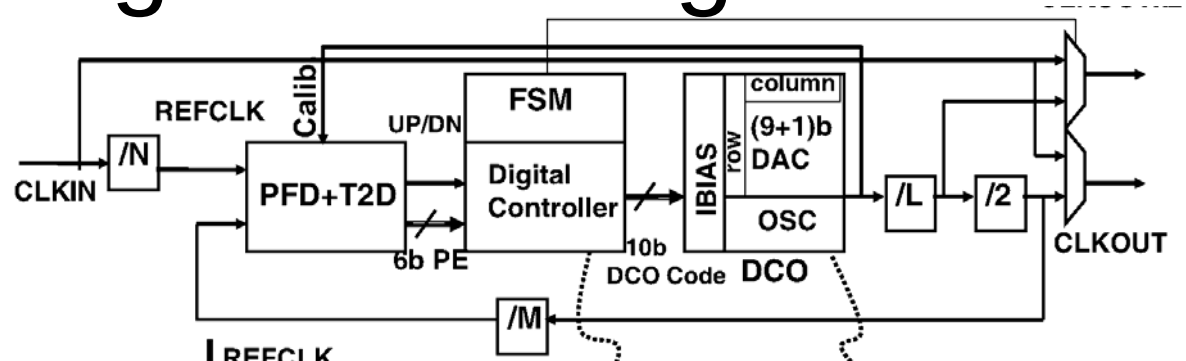
Trend towards Digitization (e.g.#1)

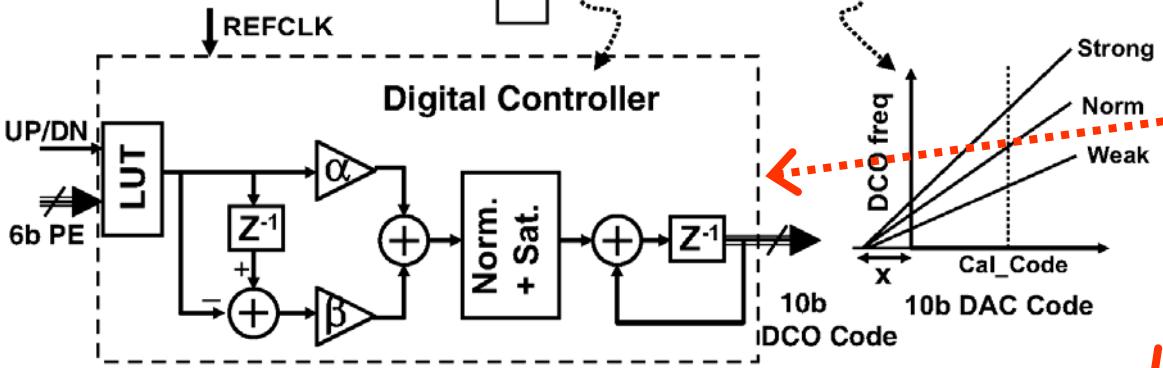
- **(Example)**
- A/D => **ACCUM** => D/A
- Gets rid of the large leaky integrating capacitor
  - Leakage acts like an additional resistor
- Integrating pole stays at zero

Perrott et al
US patent 6,630,868
2001 (filing date)



Mitigation through Architecture (e.g.#1)



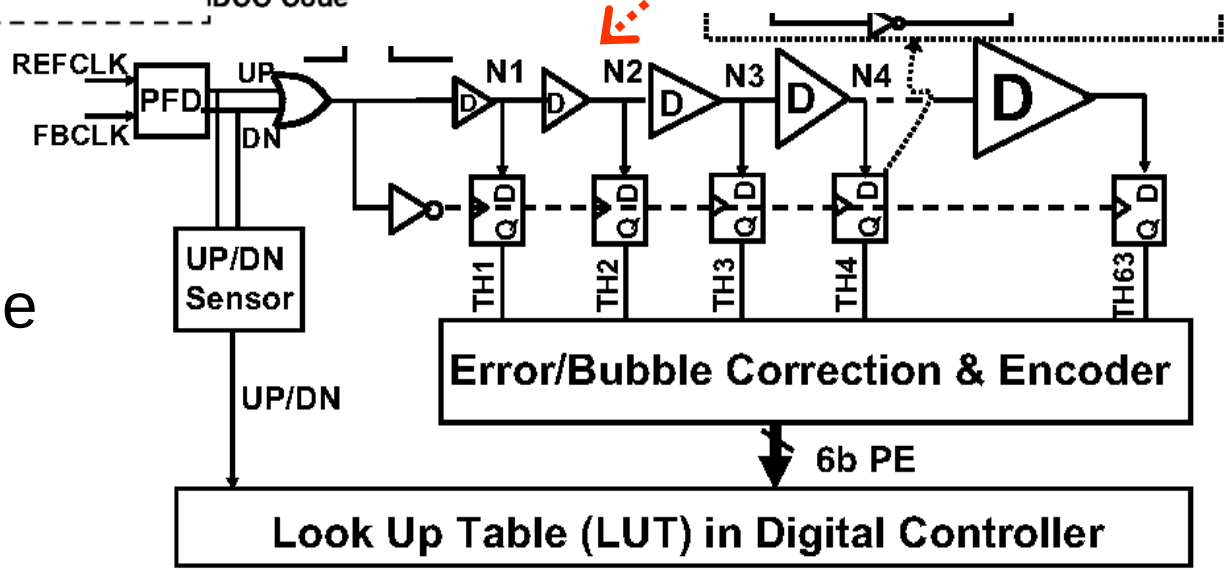


- [8: Lin'04]
- Also see
  - [5: Dunning'95]

Digital loop filter

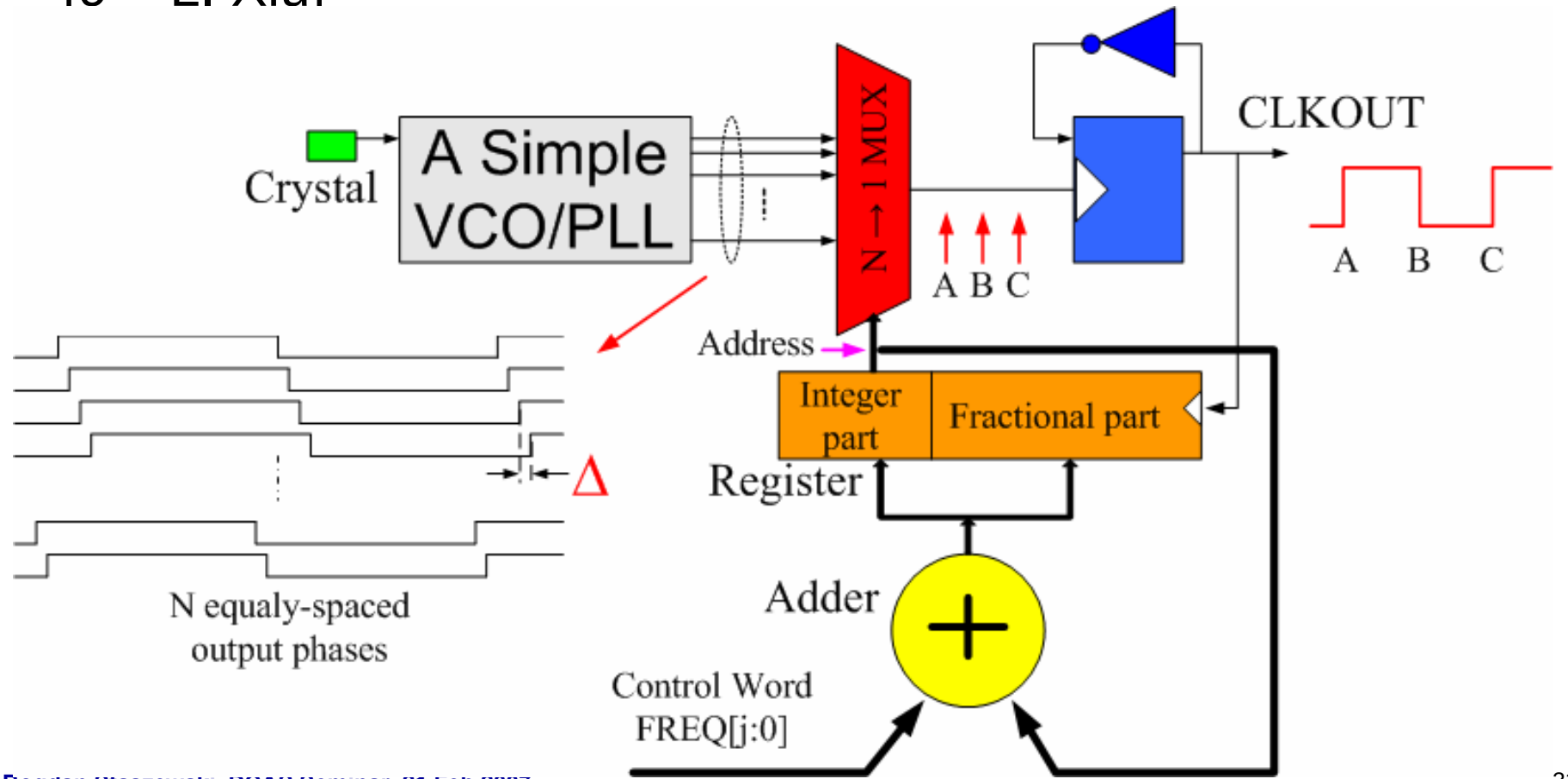
TDC

- **(Example)**
- DPLL in 90-nm
- Uses TDC for phase detection
- Digital loop filter



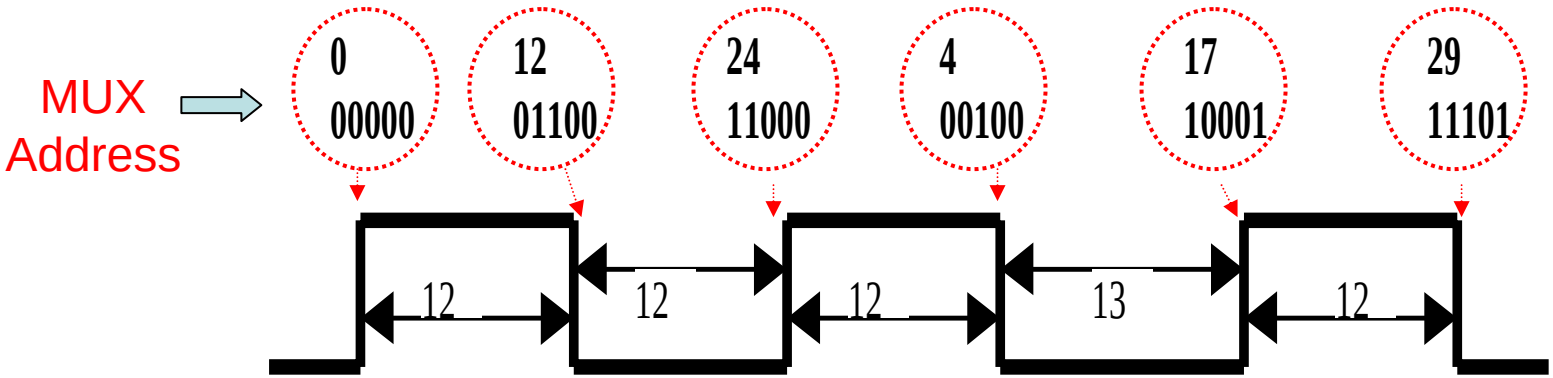
Flying-Adder Frequency/Phase Synthesis

- Using multiple equally-spaced phases generated from a VCO to synthesis various *frequency* and *phase*, by triggering the flip-flops at predestined time
- Principle idea: see diagram below (just the principle).
- [9 – L. Xiu]



Flying-Adder Frequency/Phase Synthesis

- **An example:**
  - **VCO at 156.25 MHz (6.4 ns) →Δ = 6.4/32 = 0.2 ns (assume N=32)**
  - **Wanted: 204.08 MHz, or T = 4.9 ns →FREQ[9:0] = T/(2Δ) = 4.9/0.4 = 12.25 = 01100.01000b**
  - **Integer portion is used for selecting tick, fractional portion is for accumulation.**



00000.00000 + 01100.01000 = **01100**.01000

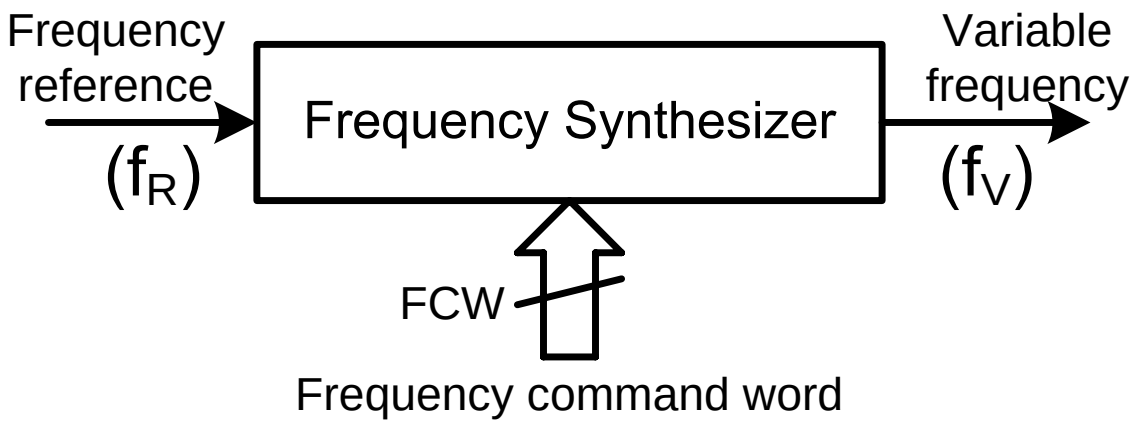
01100.01000 + 01100.01000 = **11000**.10000

11000.10000 + 01100.01000 = **00100**.11000

00100.11000 + 01100.01000 = **10001**.00000

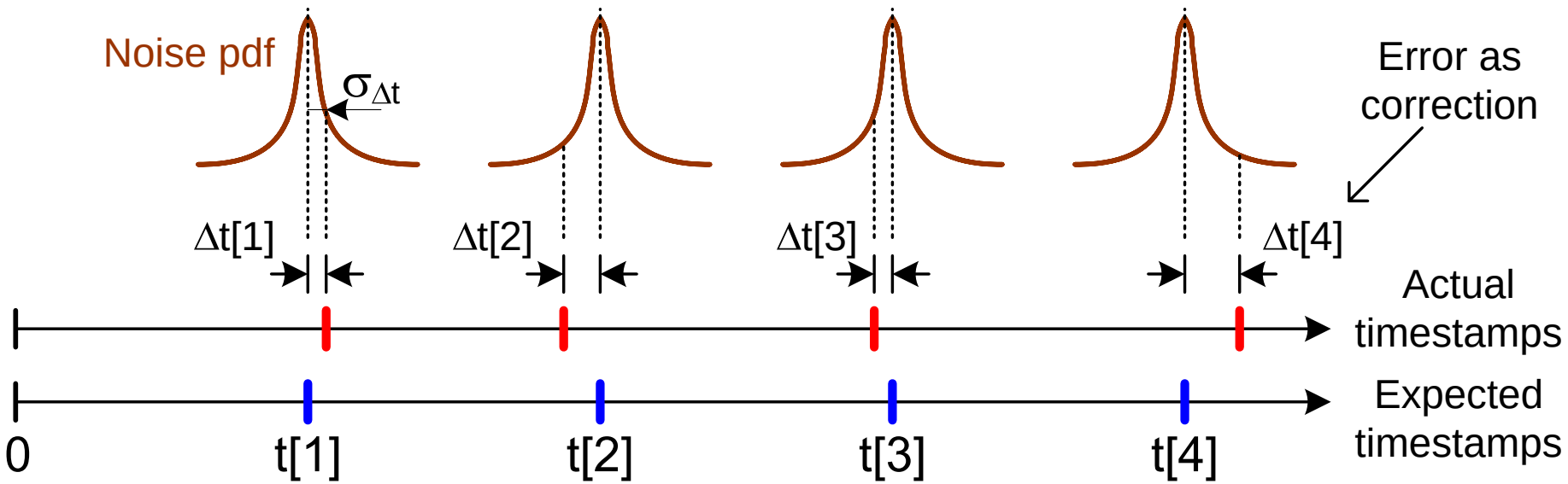
10001.00000 + 01100.01000 = **11101**.01000

All-Digital Phase-Locked Loop



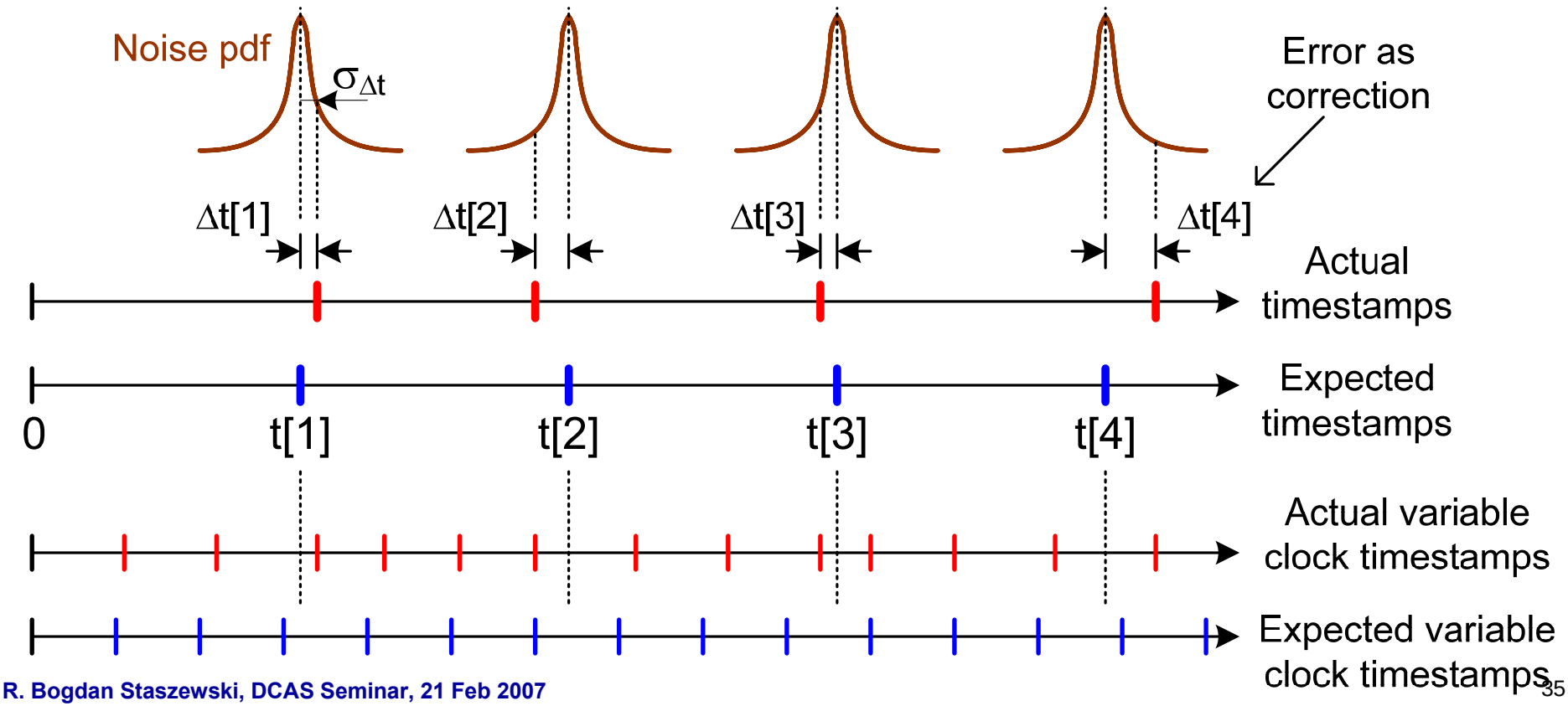
Simple Idea of Phase Domain

- Construct expected or ideal timestamps
  - "Reference phase"
- Measure the actual timestamps
  - "Variable phase"
- Their difference is the time error
  - Used for future timing corrections as negative feedback



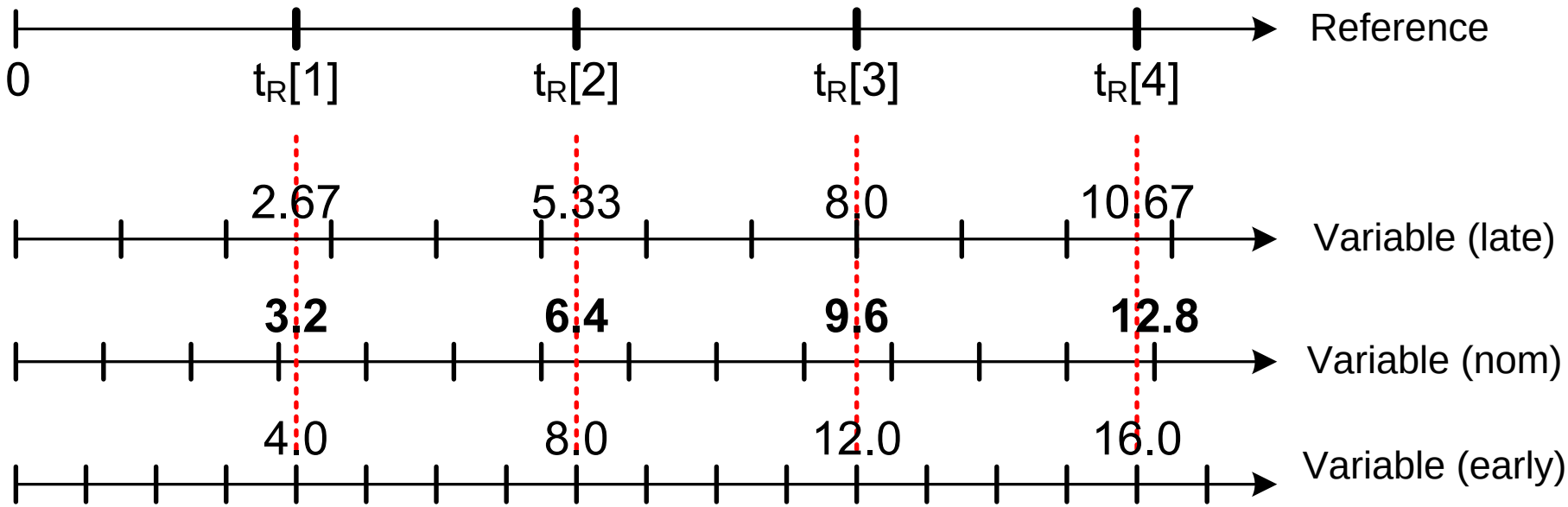
Issues with the Simple Idea

- Synthesized (variable) frequency is typically much higher than the reference frequency
- Non-integer relationship
- How to truly operate in time domain, i.e., “timestamps”?



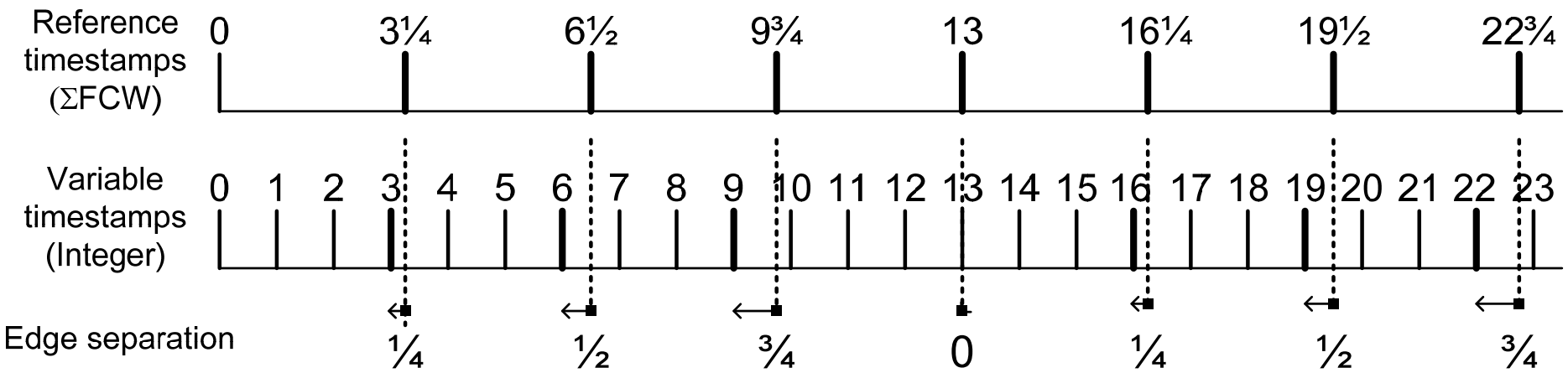
Proposed Solution

- Reference and variable signals are digital clocks
  - Use only their (rising) edges
- Phase error calculation to be performed on reference edges
- Turn the phase detection problem around
  - Measure the reference timestamps with the variable clock
  - Sample the count of variable clock cycles with each reference edge
  - If variable phase drifts, their sampled count will get affected



Hardware Needed for Digital Operation

- Accumulator of FCW
- Interpolator or normalize estimator of edge separation
  - Time-to-digital converter (TDC)
- RF oscillator needs to be numerically controlled:
  - Digitally-controlled oscillator (DCO)
- Digital phase detector and loop filter



Digitally-Controlled Oscillator (DCO)

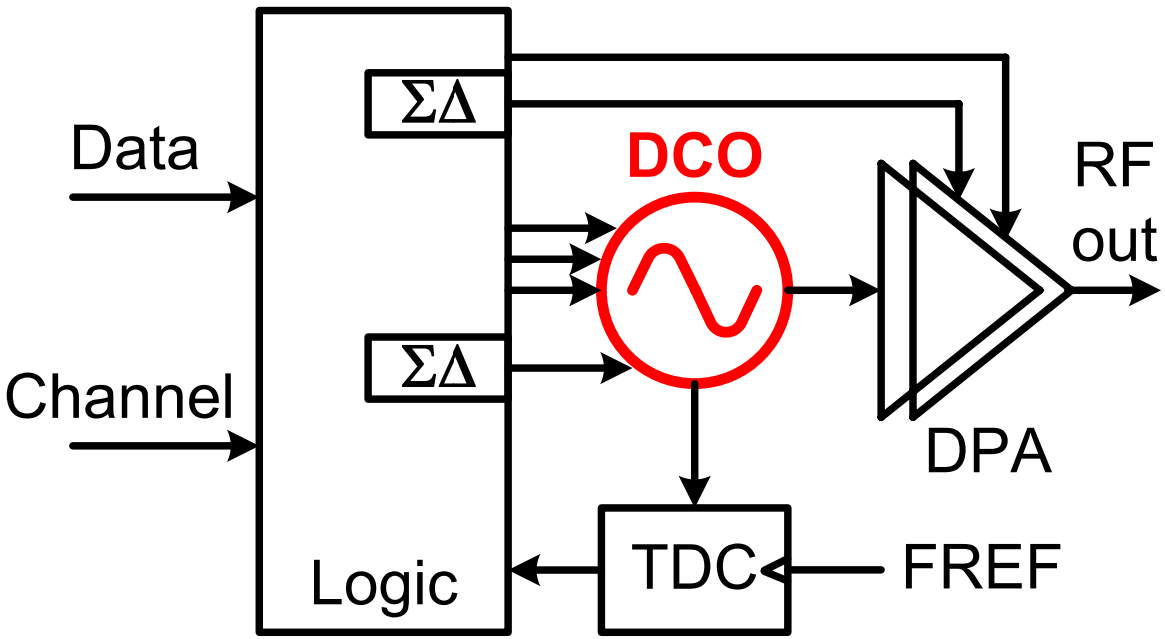
ΣΔ Modulator and DCO Interface

Time-to-Digital Converter (TDC)

Digital Loop Filter (LF)

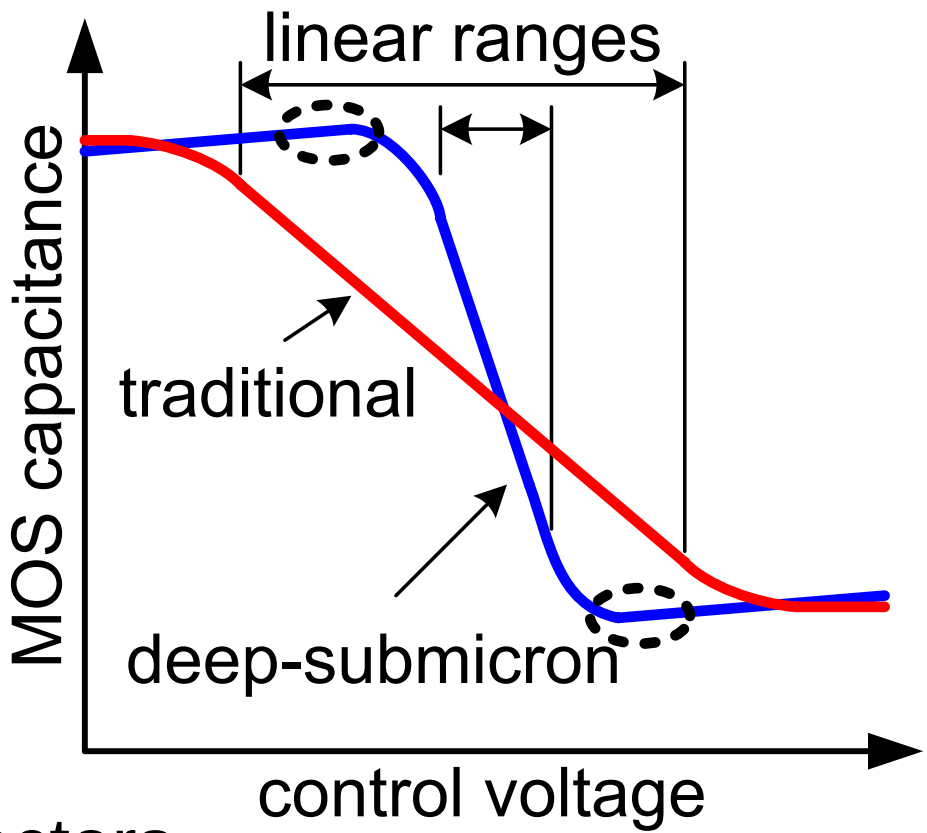
All-Digital PLL (ADPLL)

ADPLL Wideband Frequency Modulation



MOS Varactor

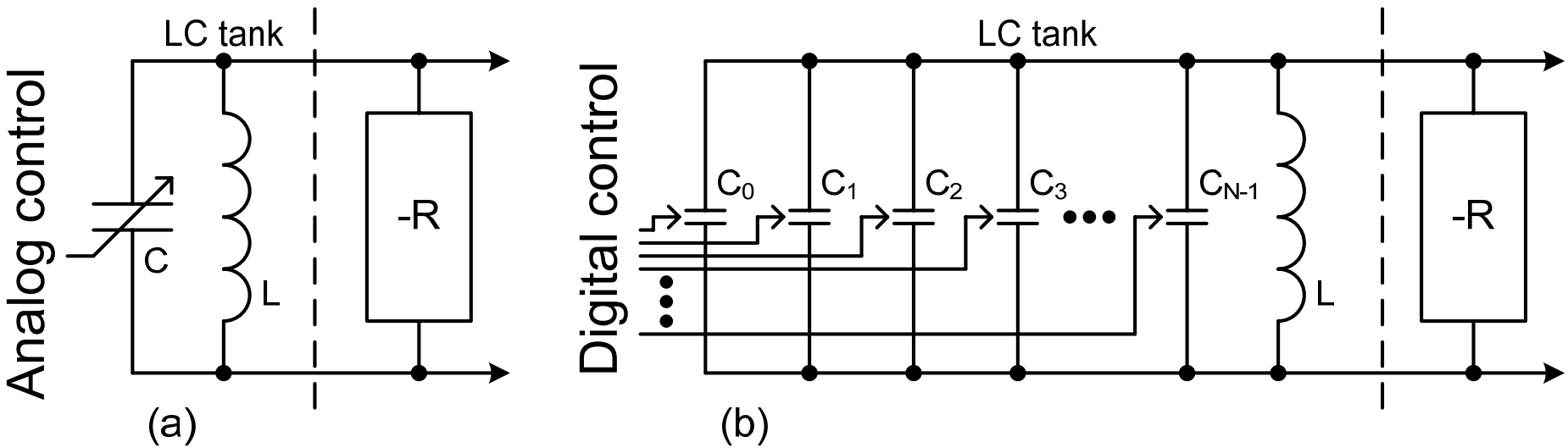
- Only simplest varactors in the digital CMOS
- Perceived poor quality of varactors in a nanoscale CMOS for conventional VCO's



- Conventional CMOS varactors
  - Large linear range for precise and wide frequency control
- Nanometer CMOS varactor
  - Linear range is compressed with high noise sensitivity

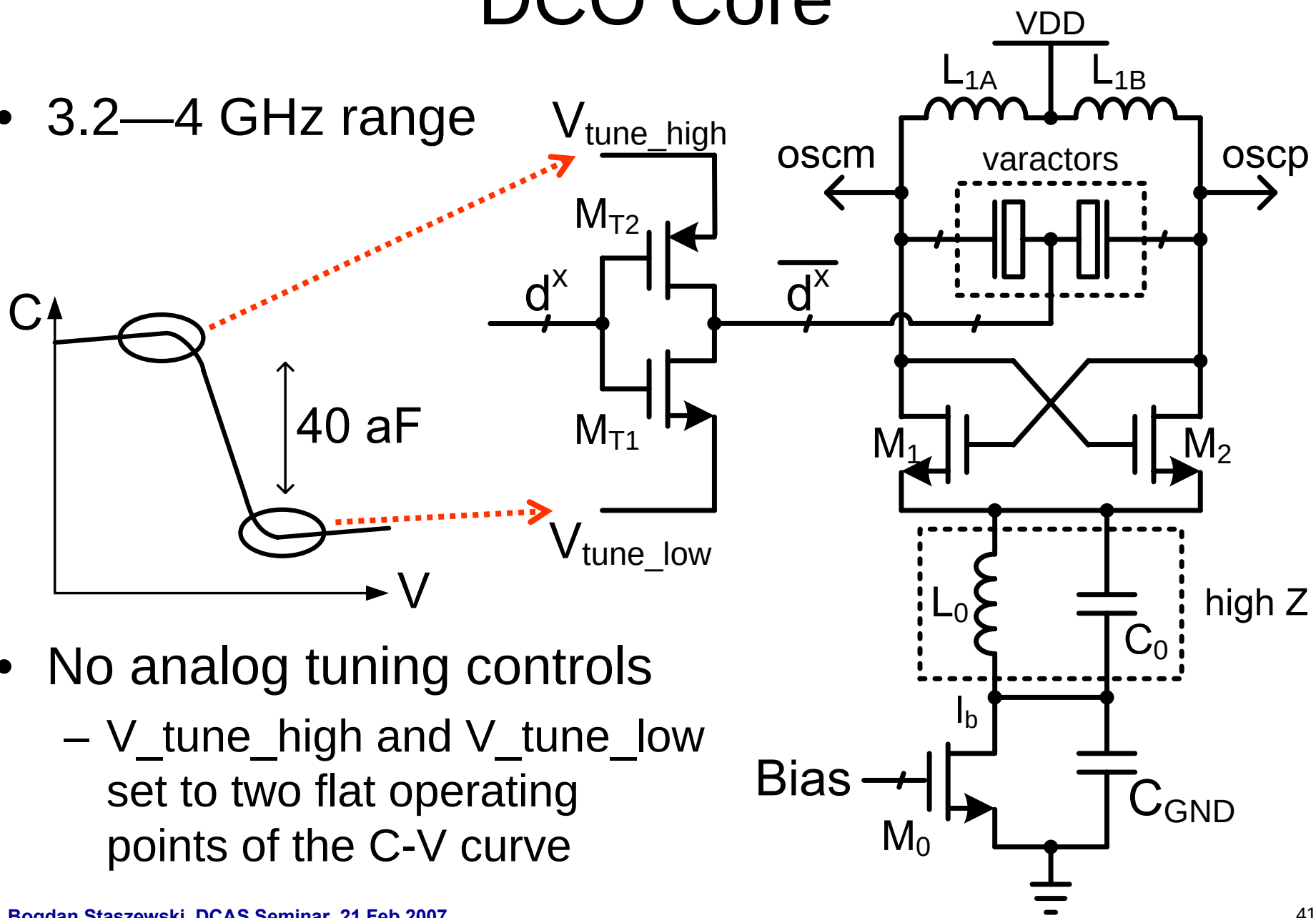
Digital Tuning of DCO

- A large linear varactor in conventional VCO replaced with a large number of tiny binary-controlled varactors in a digitally-controlled oscillator (DCO)
  - Smallest varactor size: tens of atto-farad
- Deliberate avoidance of any analog tuning
- The feedback loop could now be fully digital



DCO Core

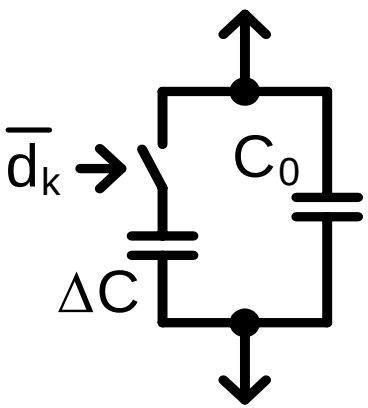
- 3.2—4 GHz range
- No analog tuning controls
  - V_tune_high and V_tune_low set to two flat operating points of the C-V curve

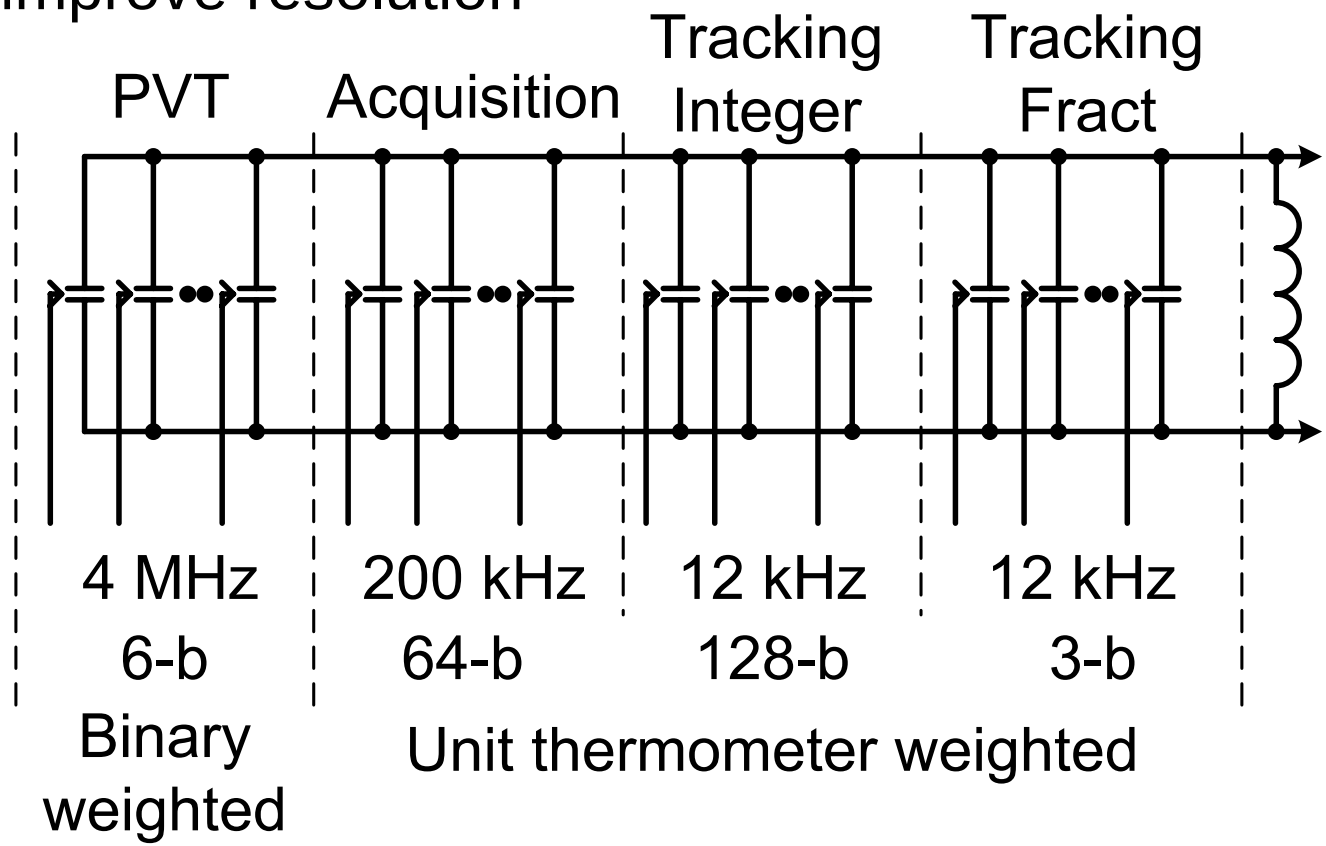


DCO Varactor Functional Banks

- Process/voltage/temperature (PVT) calibration mode
- Acquisition mode (during channel select)
- Tracking mode (during the actual TX and RX)
  - Dithering to improve resolution

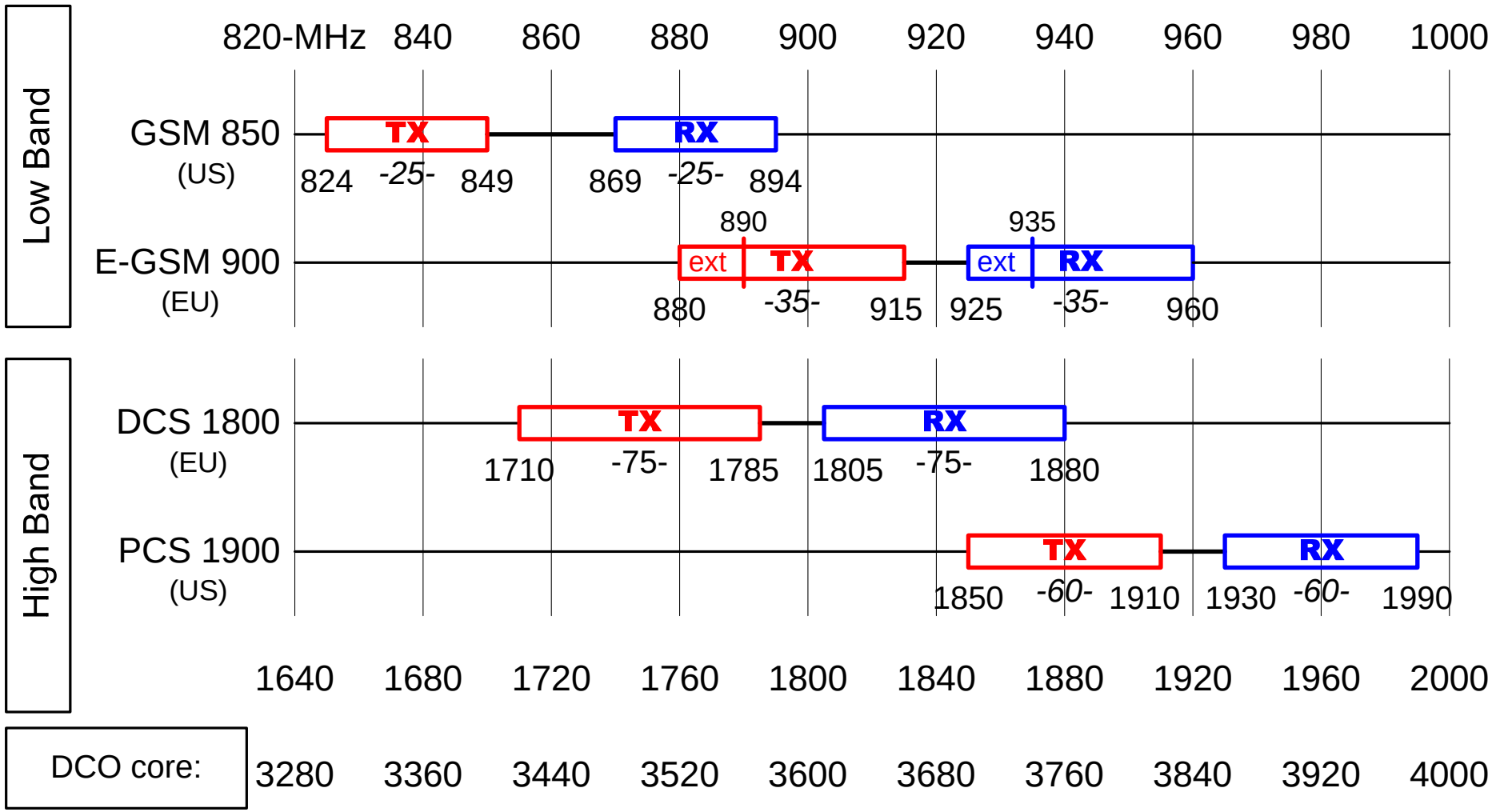
Varactor model:



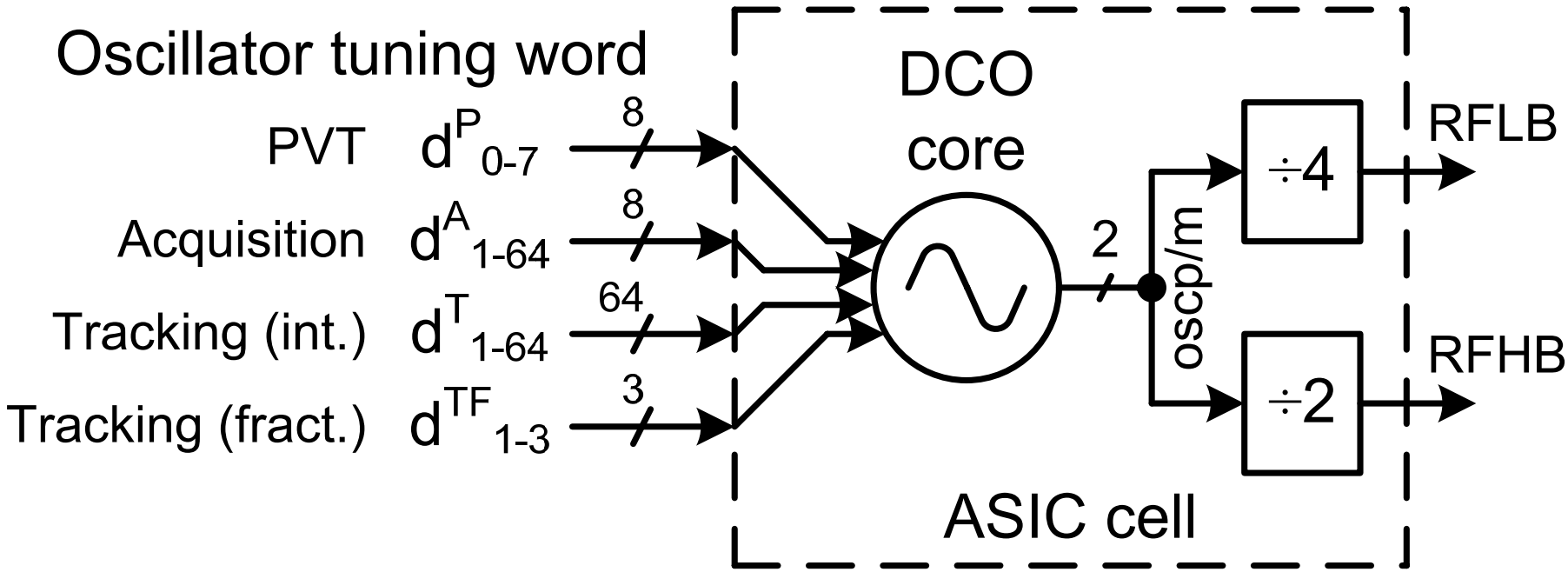


GSM Bands

- Single oscillator covers four GSM bands
  - ÷2/÷4 clock division



DCO ASIC Cell



- Truly digital I/O's even at 1.8 GHz output – t_r<50 ps
- DCO built as a digital ASIC cell despite analog underlying internals
- DCO analog nature does not propagate
- Circuitry around it can be digital

Digitally-Controlled Oscillator (DCO)

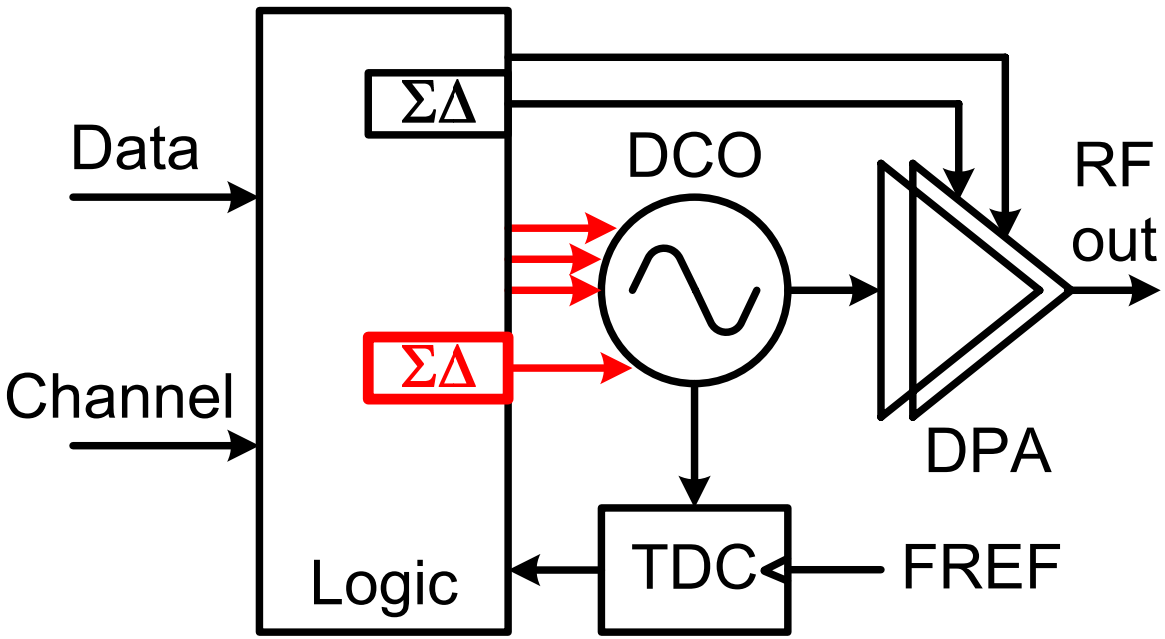
ΣΔ Modulator and DCO Interface

Time-to-Digital Converter (TDC)

Digital Loop Filter (LF)

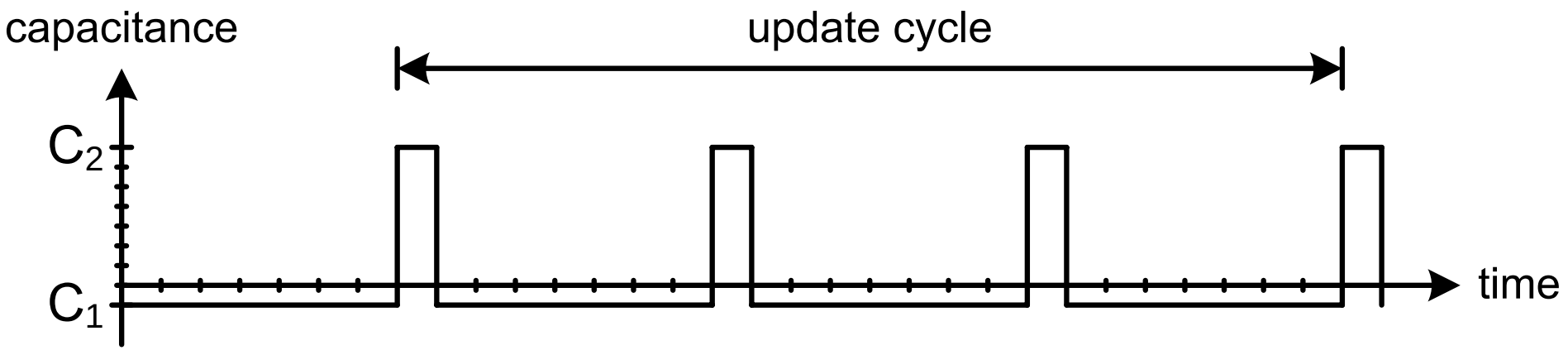
All-Digital PLL (ADPLL)

ADPLL Wideband Frequency Modulation



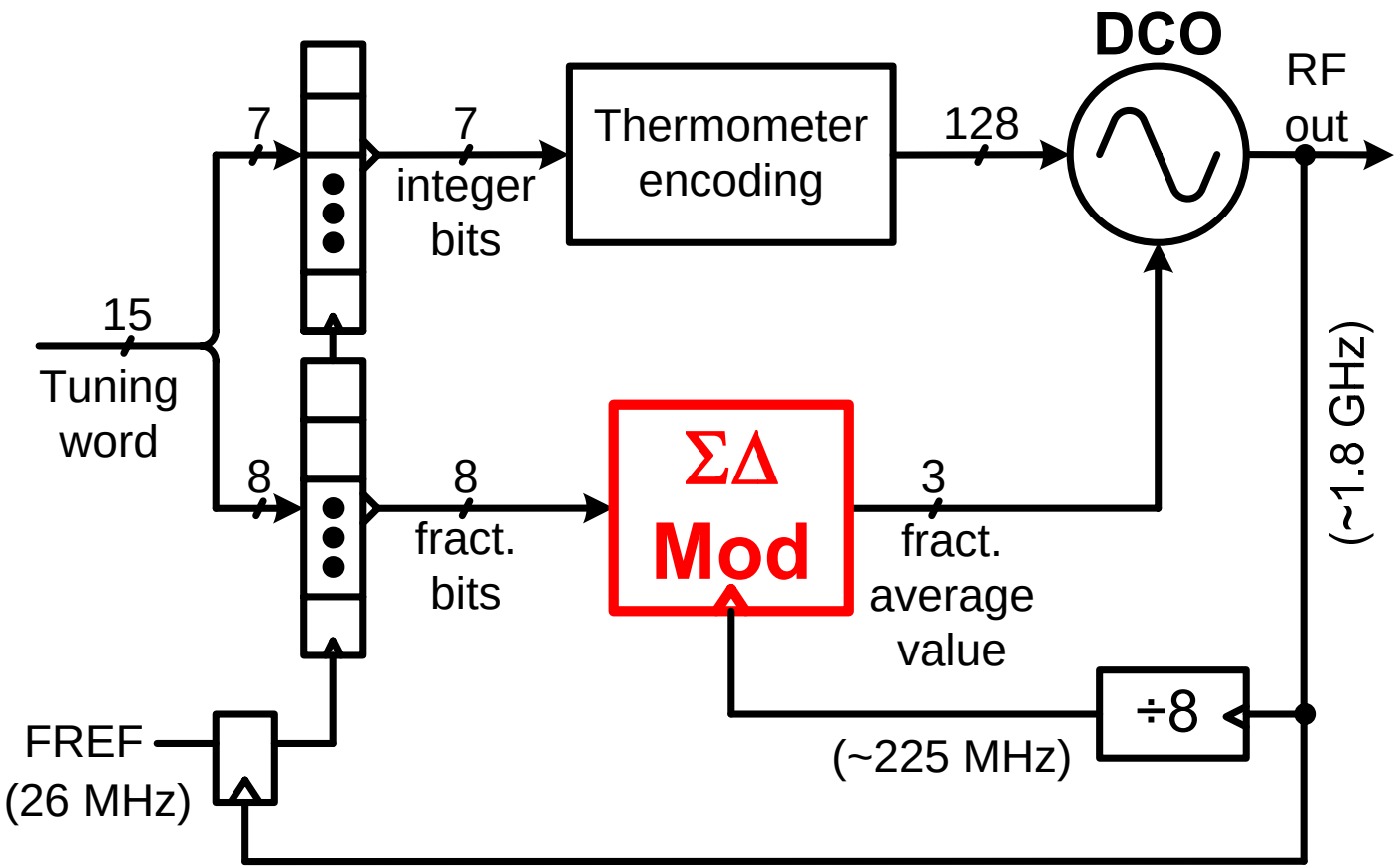
DCO Varactor Dithering Principle

- Frequency resolution enhanced by high-speed dithering of the finest varactors
- Produces spurious tone at the oscillator output with power inversely proportional to the dithering speed
  - Spur power = -20 log(β/2) [dBc], where β is a dimensionless ratio of the peak frequency deviation (low) to the modulating frequency (high)
  - e.g., β = 12 kHz / 225 MHz => -91 dBc spur



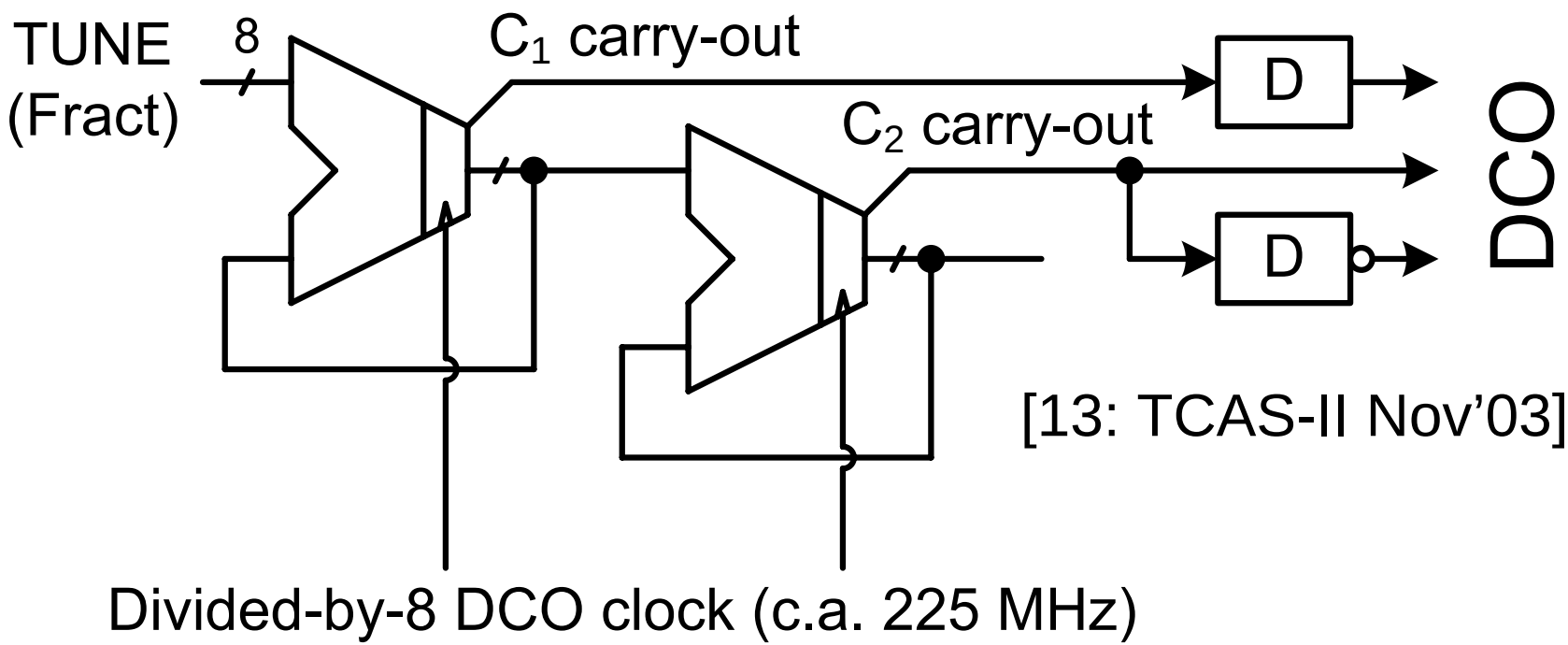
Sigma-Delta DCO Dither

- Improves time-averaged DCO frequency resolution over the basic $\Delta f = 12$ kHz
  - New resolution: 12 kHz / 2^8 = 47 Hz



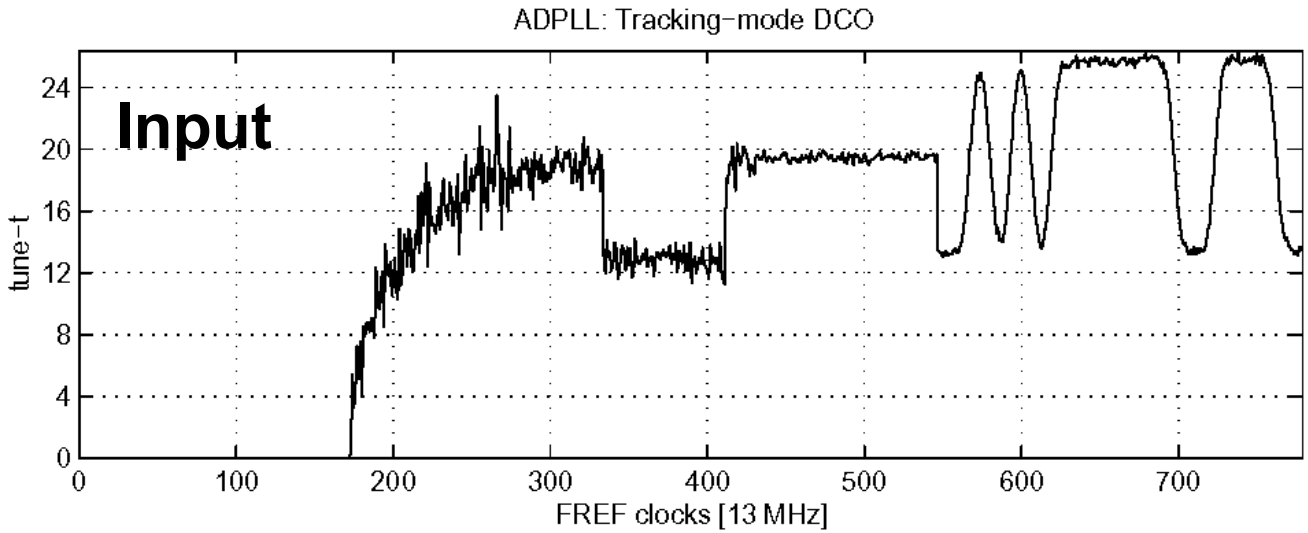
ΣΔ Modulator

- 2nd order MASH structure
- Inspired by [4] (Riley'93)
  - Critical path retimed for high-speed operation
- Addition of ΣΔ polynomial inside the DCO

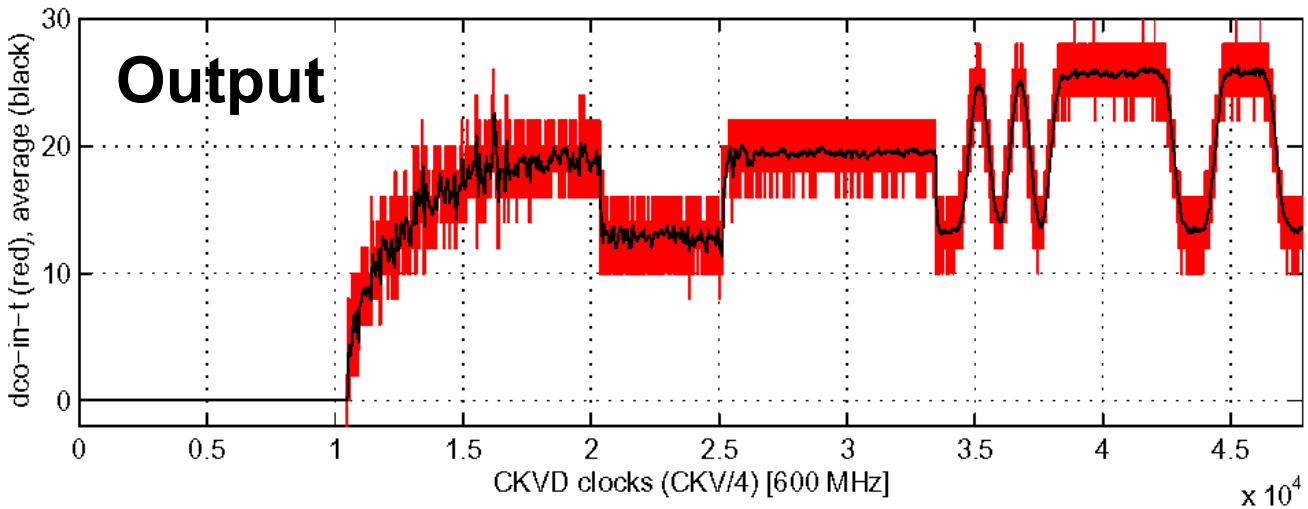


Simulation Example of ΣΔ DCO Dither

- 2nd order MASH ΣΔ Modulator
- Fixed-point DCO tuning word



- **Red**: Integer DCO input word
- **Black**: running average
  - Faithful reproduction of the input!



DCO Quantization Noise Derivation

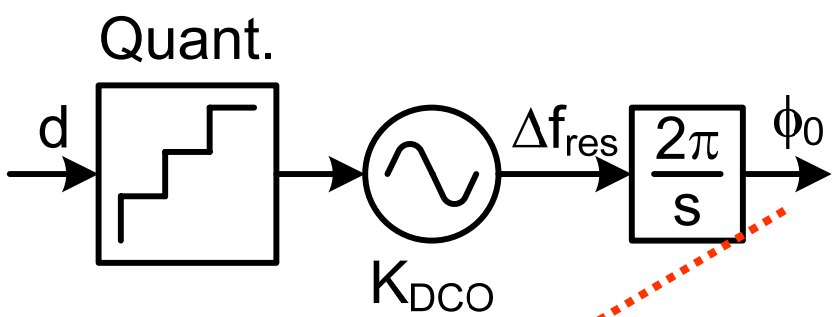
Total Q-noise power:

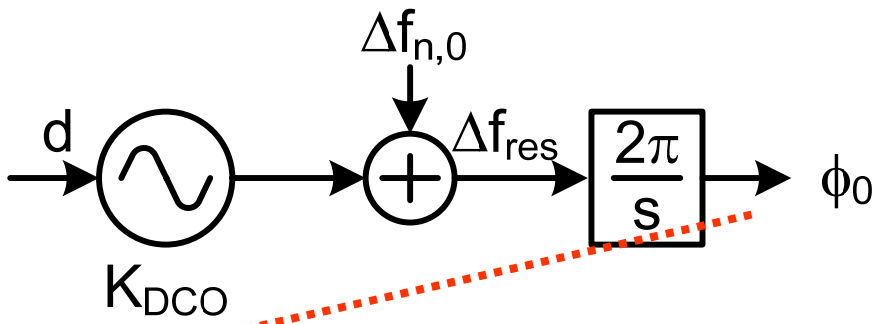
$$\sigma_{\Delta f}^{\ 2} = \frac{\Delta f_{res}^{\ 2}}{12}$$

Q-noise spectrum:

$$\frac{S_{\Delta f}}{2} = \frac{\sigma_{\Delta f}^{\ 2}}{f_{dith}} = \frac{\Delta f_{res}^{\ 2}}{12 \cdot f_{dith}}$$

[17: JSSC Nov'05]





Phase noise (PN) due to white dither:

$$L(\Delta f) = \frac{1}{12}\left(\frac{\Delta f_{res}}{\Delta f}\right)^2 \frac{1}{f_{dith}}\left(\operatorname{sinc}\frac{\Delta f}{f_{dith}}\right)^2$$

PN due to ΣΔ:

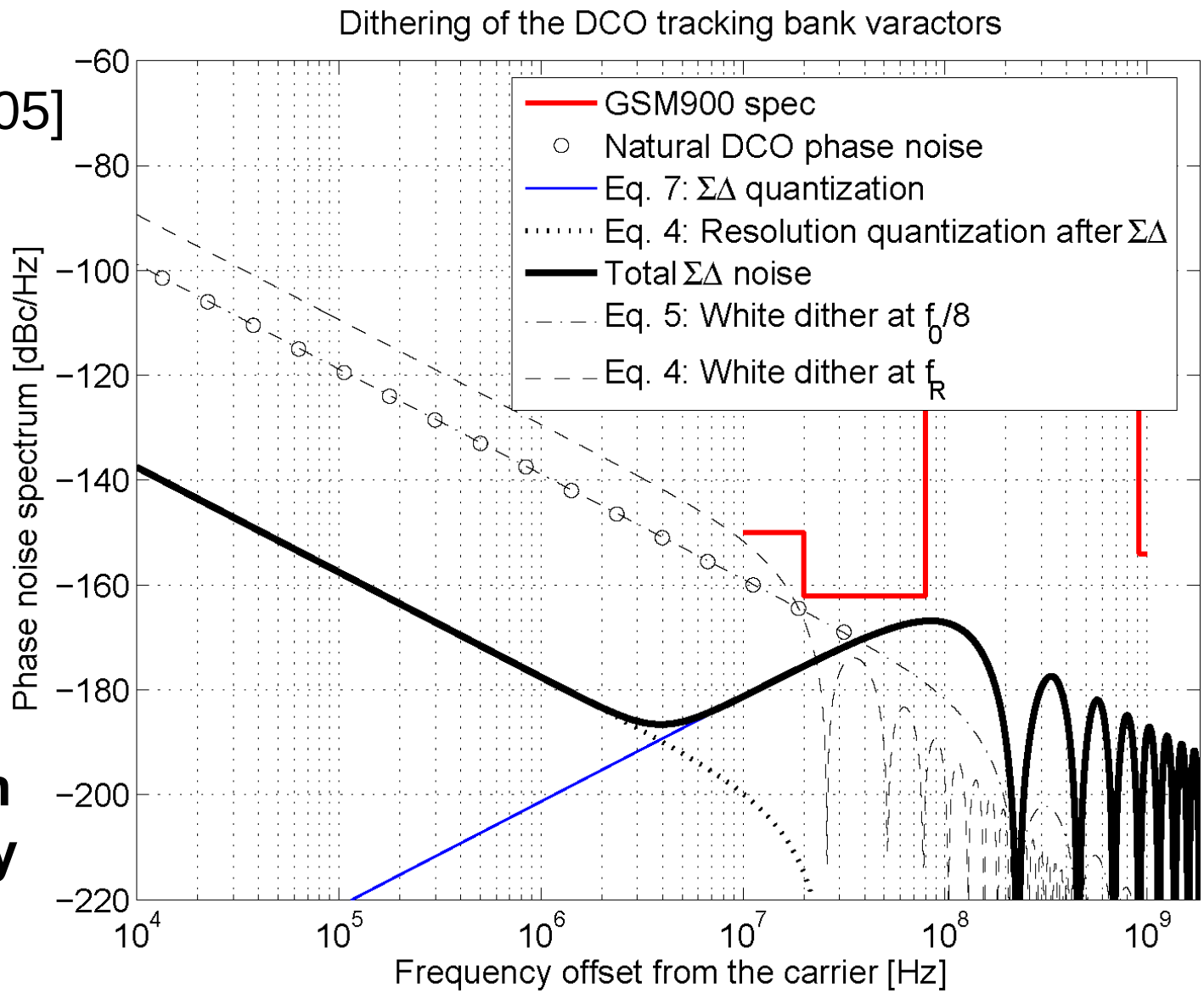
$$L(\Delta f) = \frac{1}{12}\left(\frac{\Delta f_{res}}{\Delta f}\right)^2 \frac{1}{f_{dith}}\left(2\sin\frac{\pi\Delta f}{f_{dith}}\right)^{2n}$$

PN is frequency shaped!

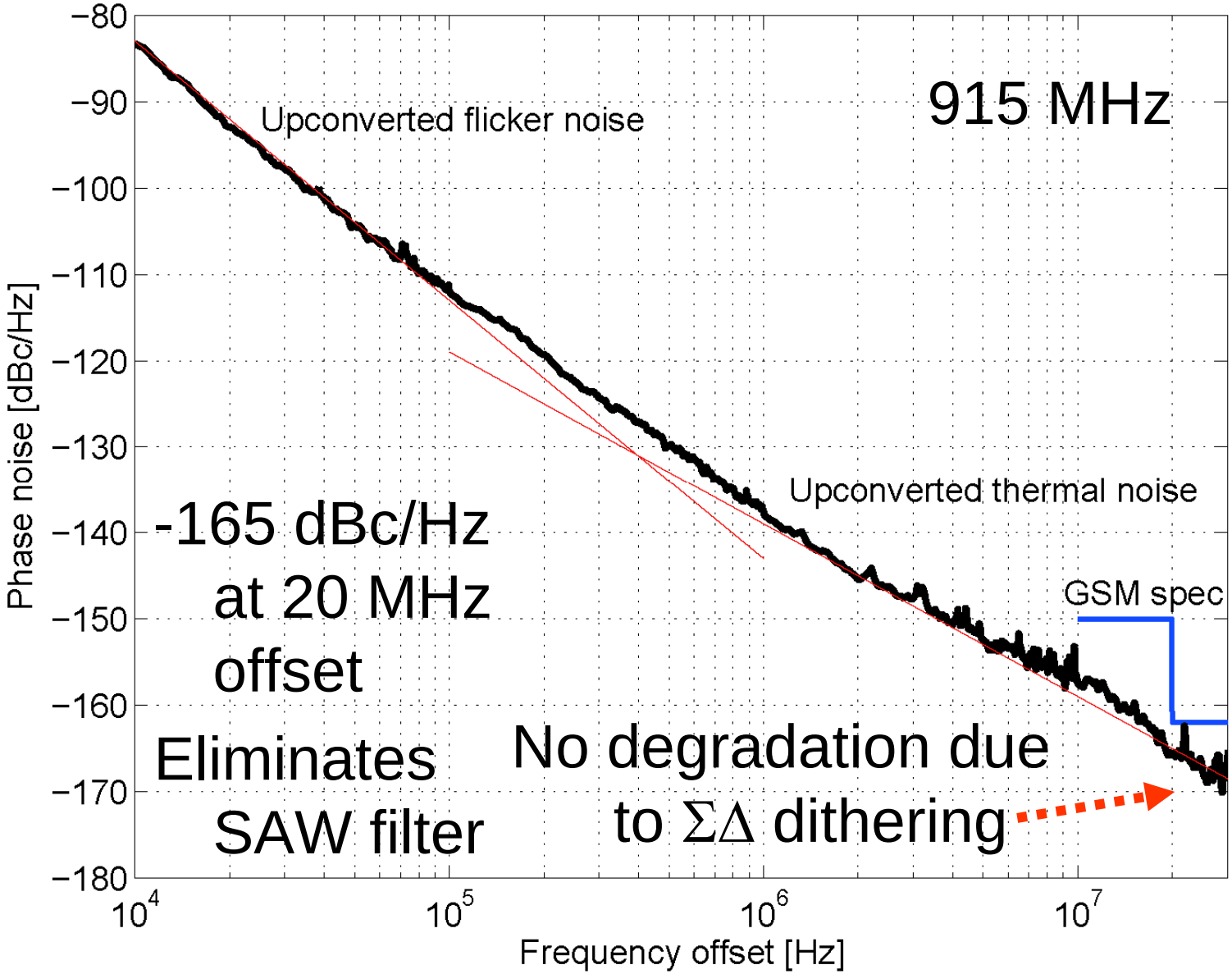
Theoretical Phase Noise Spectra

[17: JSSC Nov'05]

- Δf = 12 kHz
- f_R = 26 MHz
- f_{dith} = 225 MHz
- 2nd order $\Sigma\Delta$
- **Quantization noise energy at high-freq.**

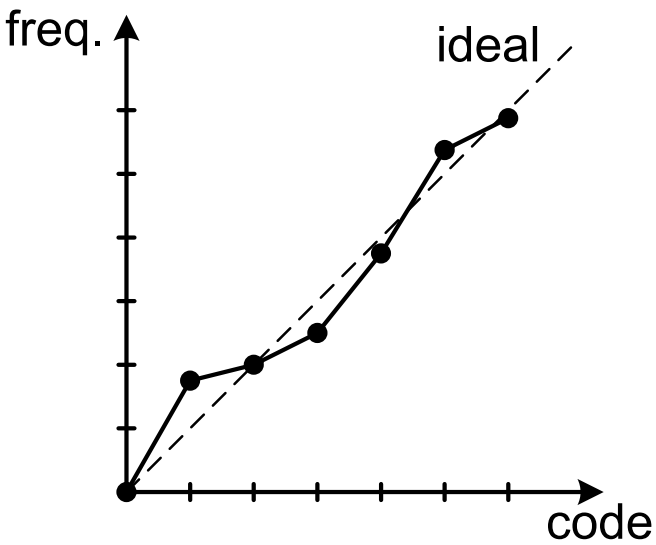


Measured DCO Phase Noise

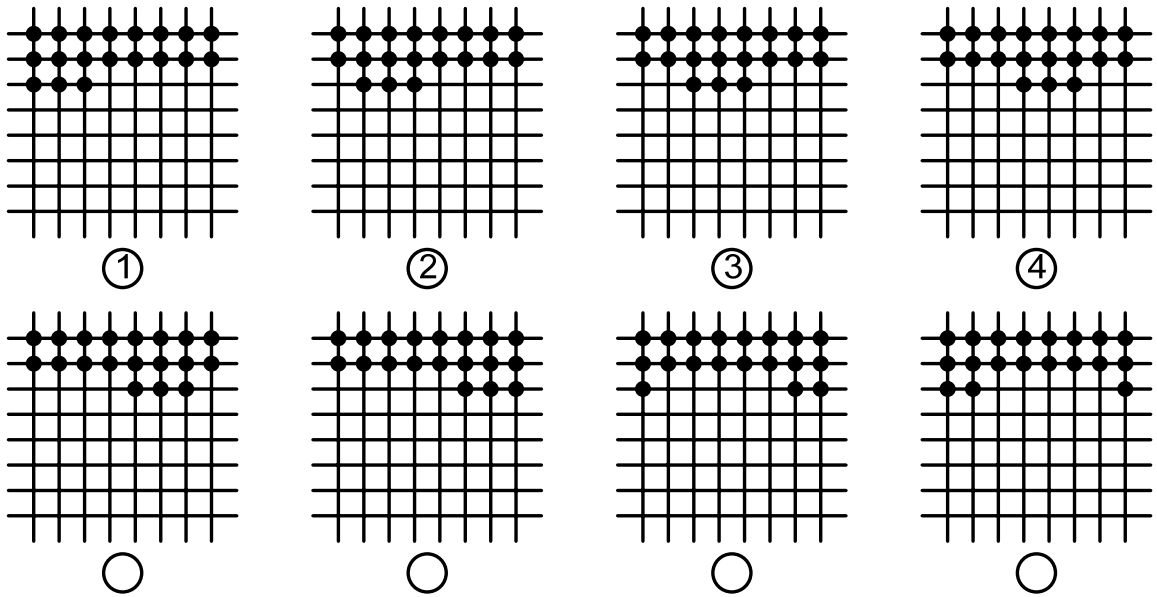


Dynamic Element Matching

- Unit-weighted varactors have slightly different capacitative values
- As capacitors are turned on and off, non-linearities will be evident in the output
- Dynamic element matching (DEM) to improve digital-to-frequency conversion linearity

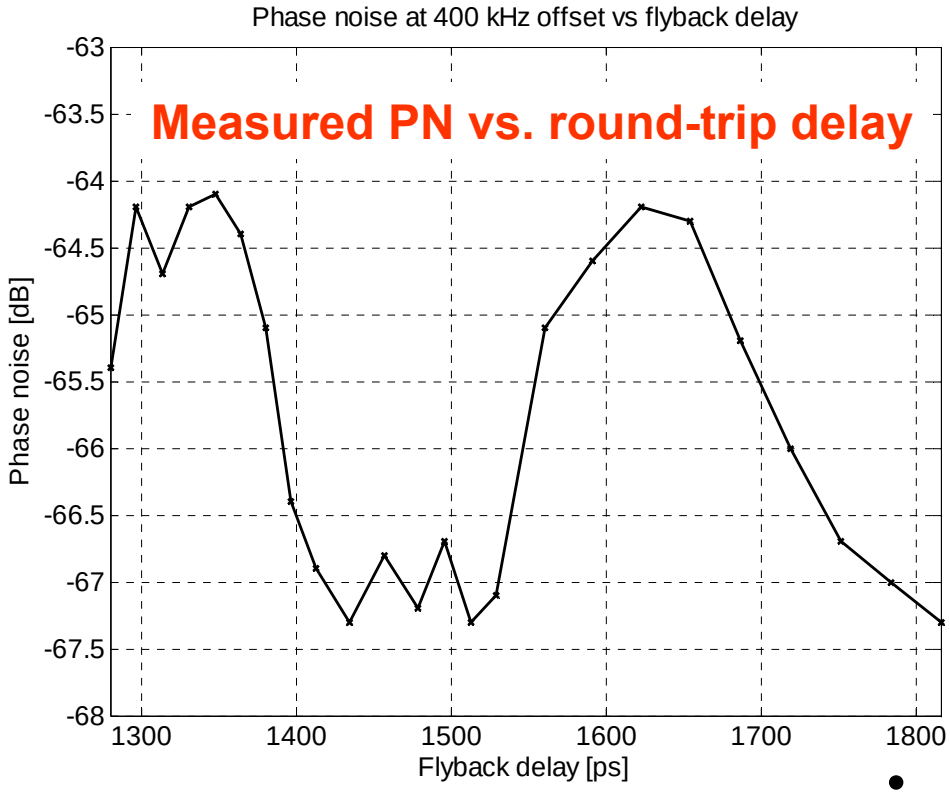


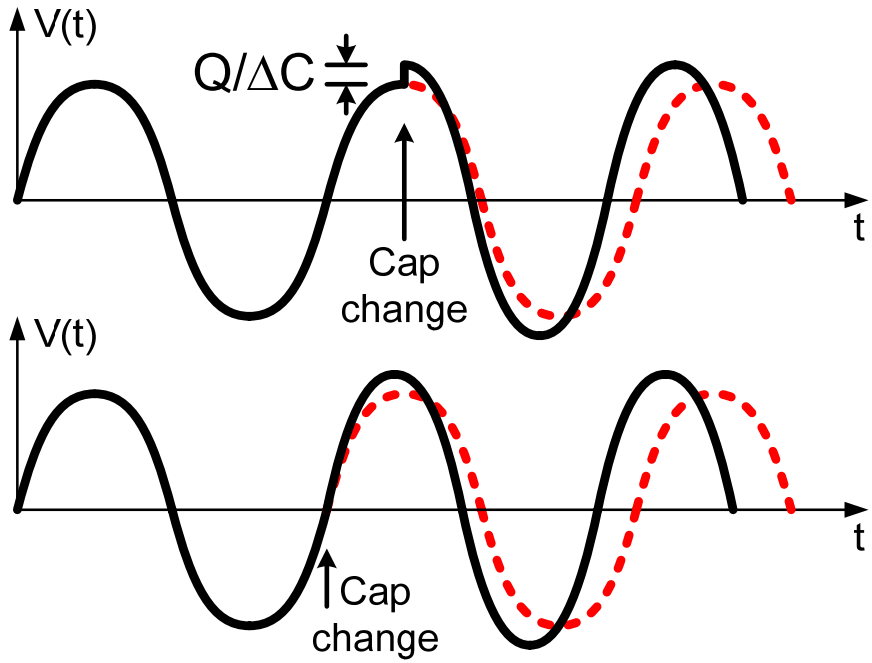
8x8 varactor encoding matrix:

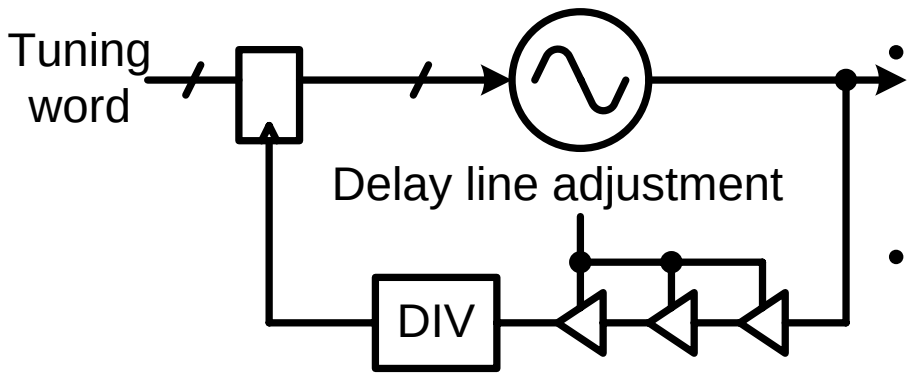


Progression of time (shown 8 cycles)

Synchronously-Optimal Sampling

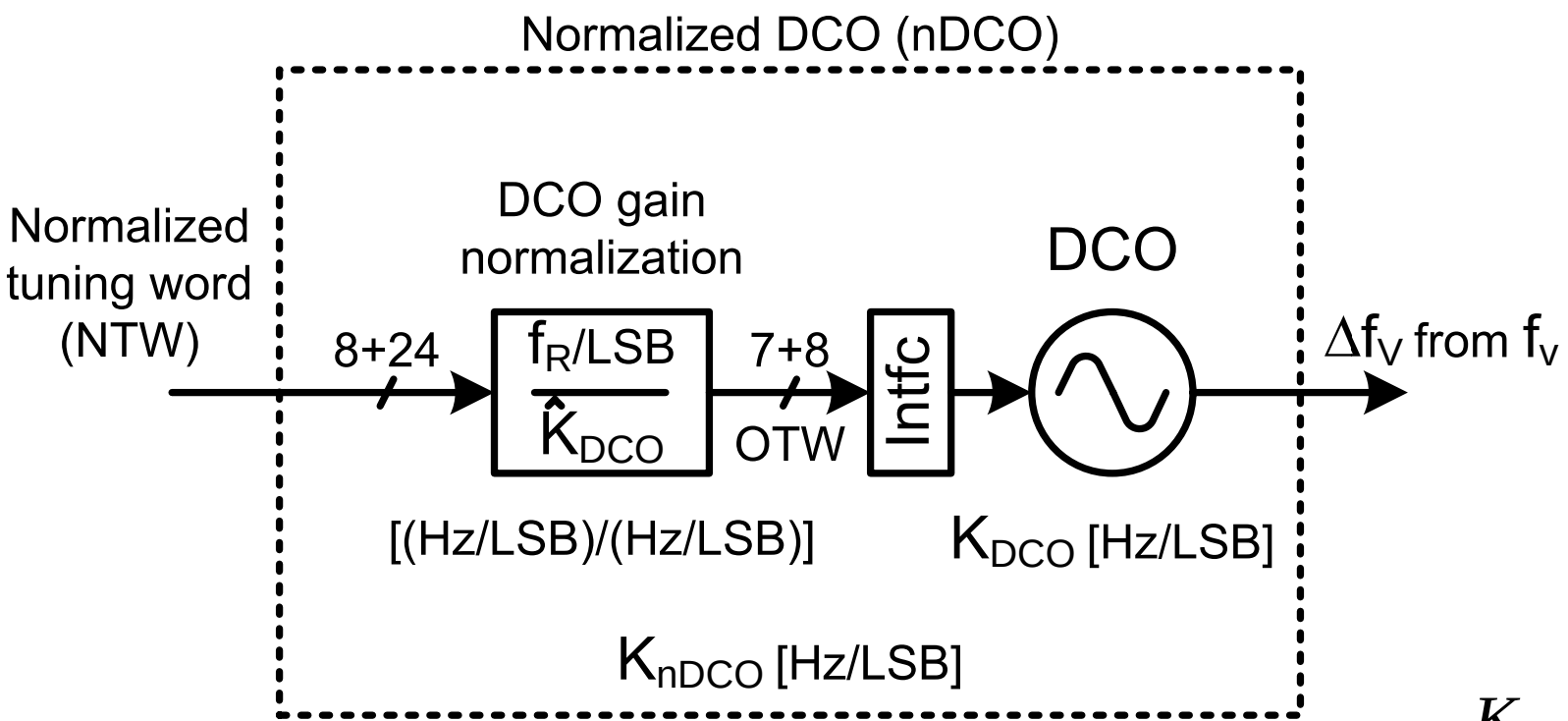






- DCO is a time-variant system
- Digital input controls the oscillating frequency by modifying the total capacitance
- Oscillator input word changes only at precise DCO state where it causes least amount of perturbations

Normalized DCO



$$K_{nDCO}(f) = f_R \frac{K_{DCO}}{\hat{K}_{DCO}} = f_R \cdot r$$

- K_{DCO} is dependent upon PVT
- K_{DCO} therefore is tracked and normalized
- Decouples the phase and frequency info from process, voltage and temperature

Digitally-Controlled Oscillator (DCO)

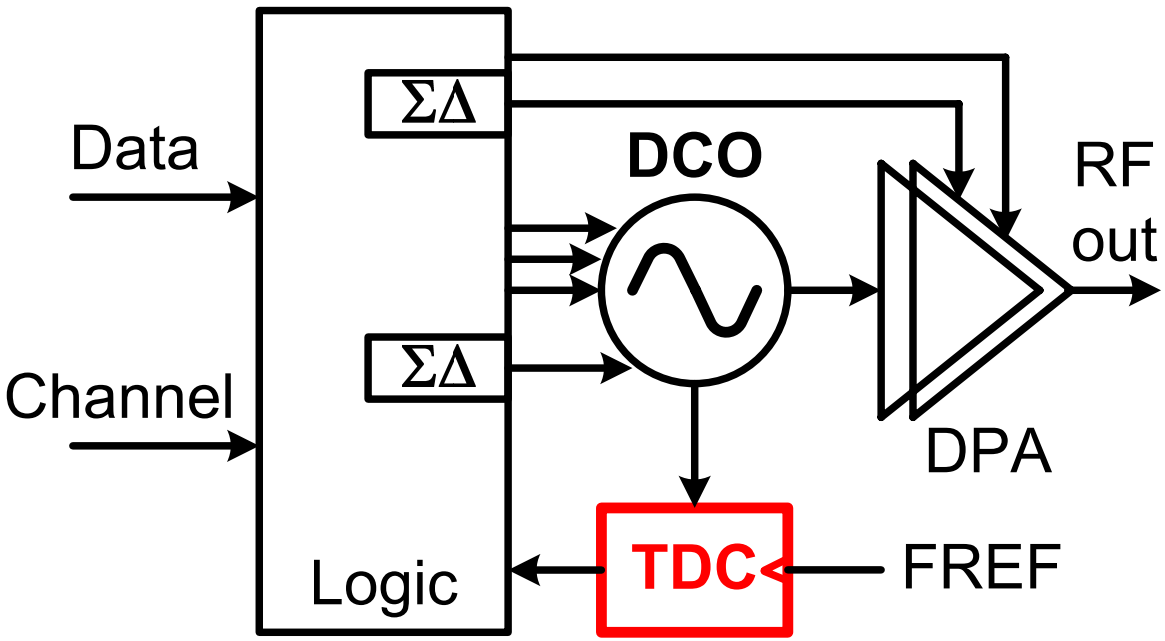
ΣΔ Modulator and DCO Interface

Time-to-Digital Converter (TDC)

Digital Loop Filter (LF)

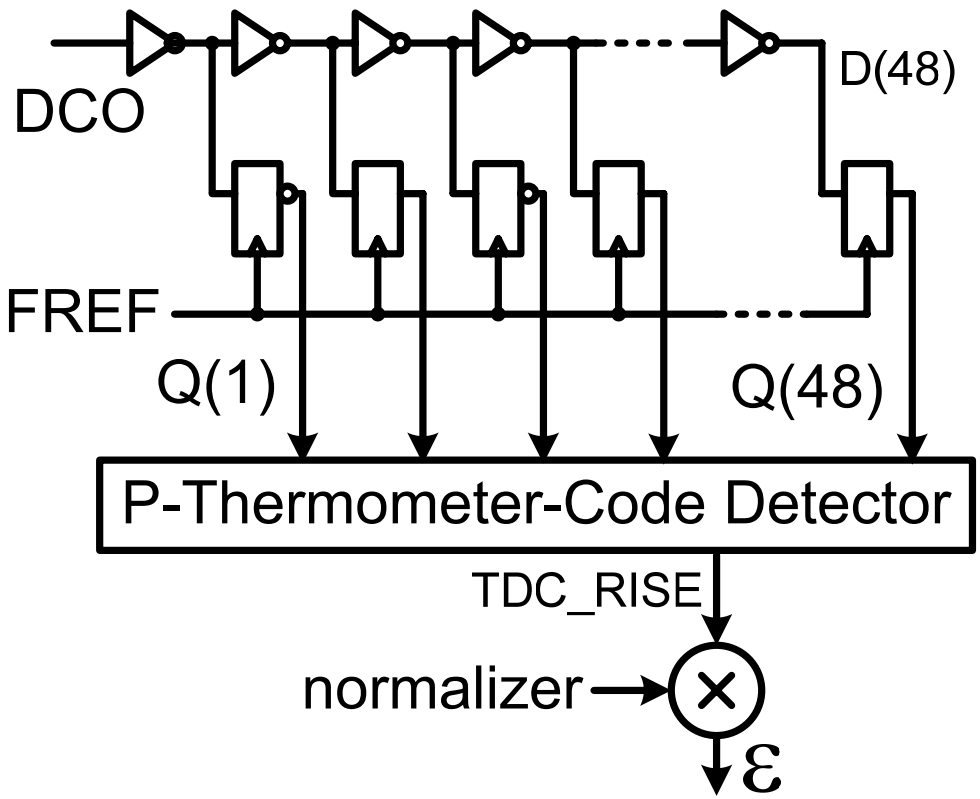
All-Digital PLL (ADPLL)

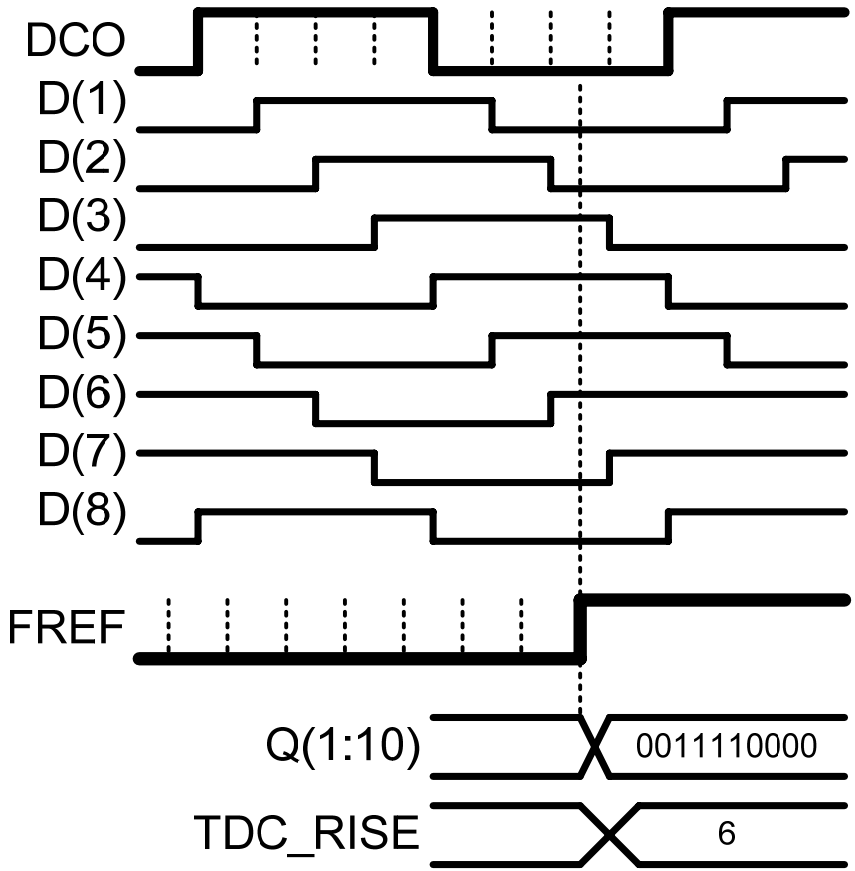
ADPLL Wideband Frequency Modulation



Time-to-digital Converter (TDC)

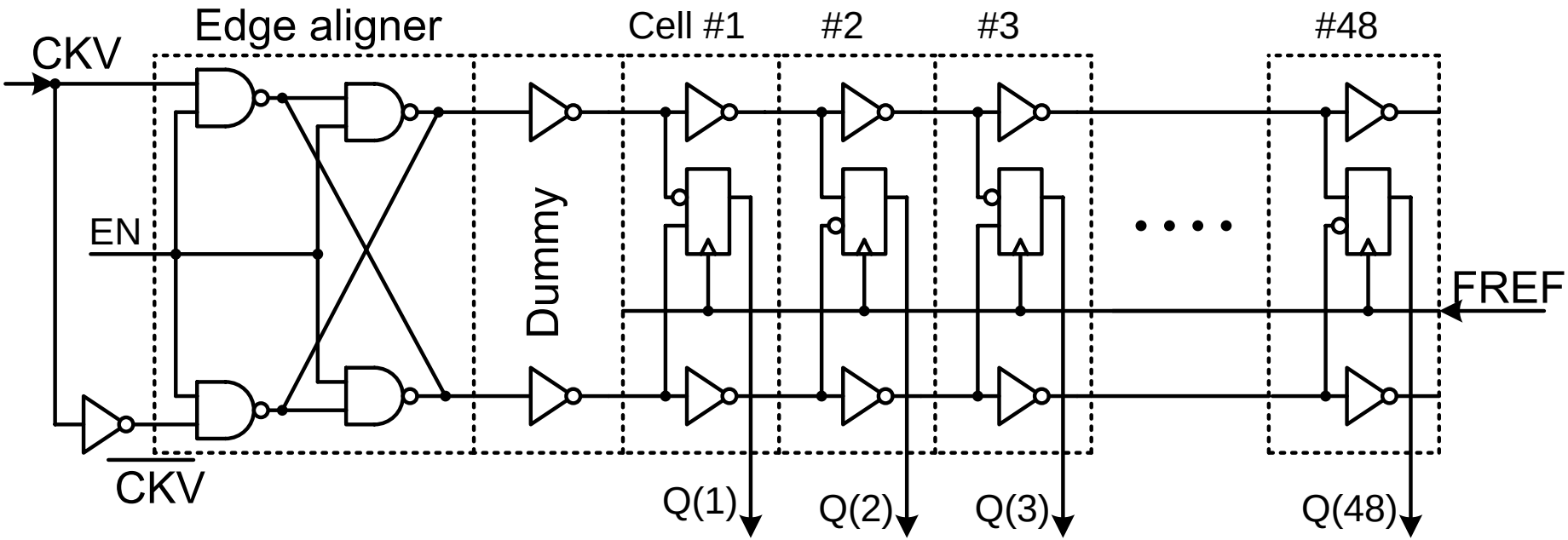
- Quantized phase detector with resolution of about 20 ps
- DCO clock passes through the inverter chain
- Delayed outputs are sampled by FREF





TDC Core Implementation

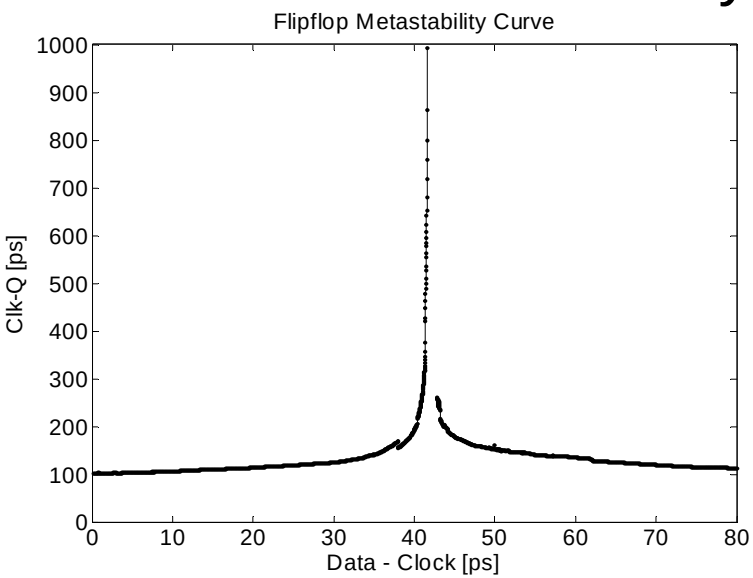
- Novel pseudo-differential architecture
- Insensitive to NMOS and PMOS mismatches
- TDC resolution close to an inverter delay
  - 15 – 20 ps
  - Fastest logic-level regenerative delay in CMOS

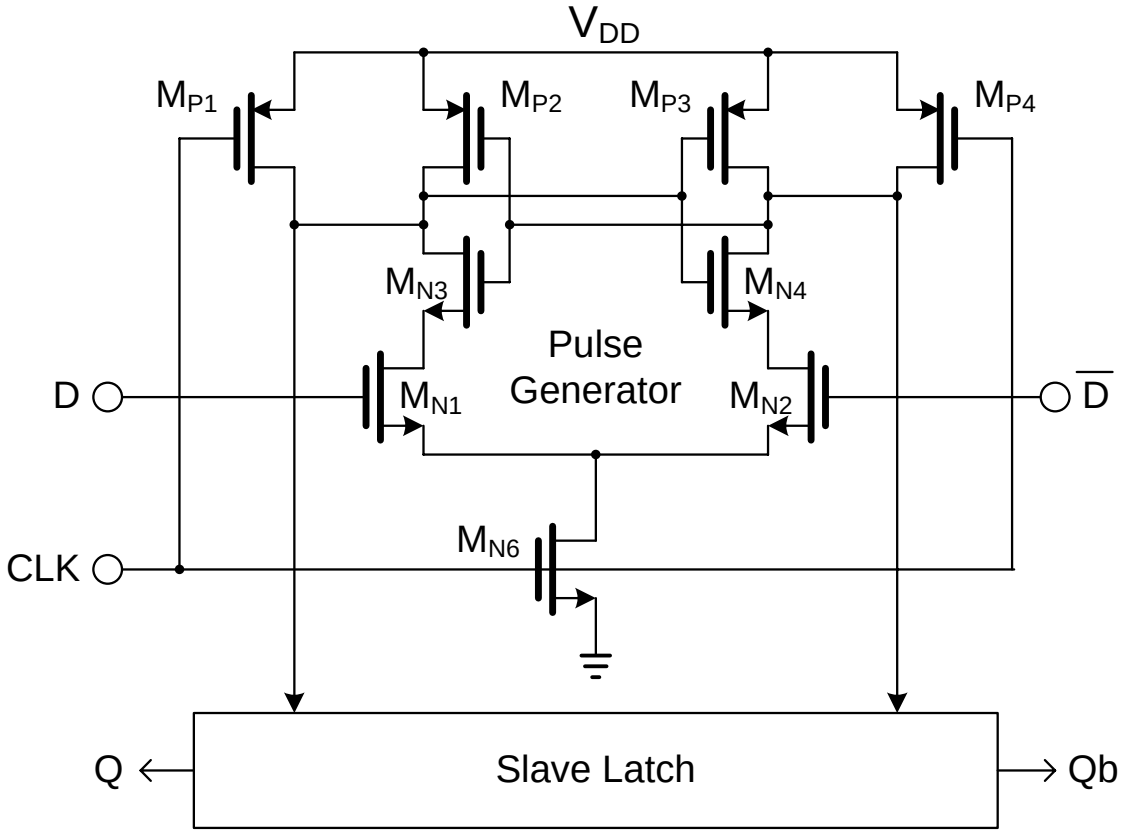


High-Resolution Flip-Flop

- Adapted from [Nikolic, JSSC'00]
- Symmetric along the vertical axis
- Identical resolution of rising and falling edges
- Light input loading

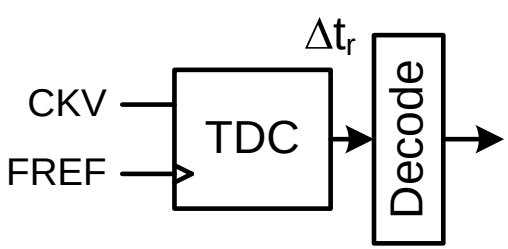
- Simulated metastability

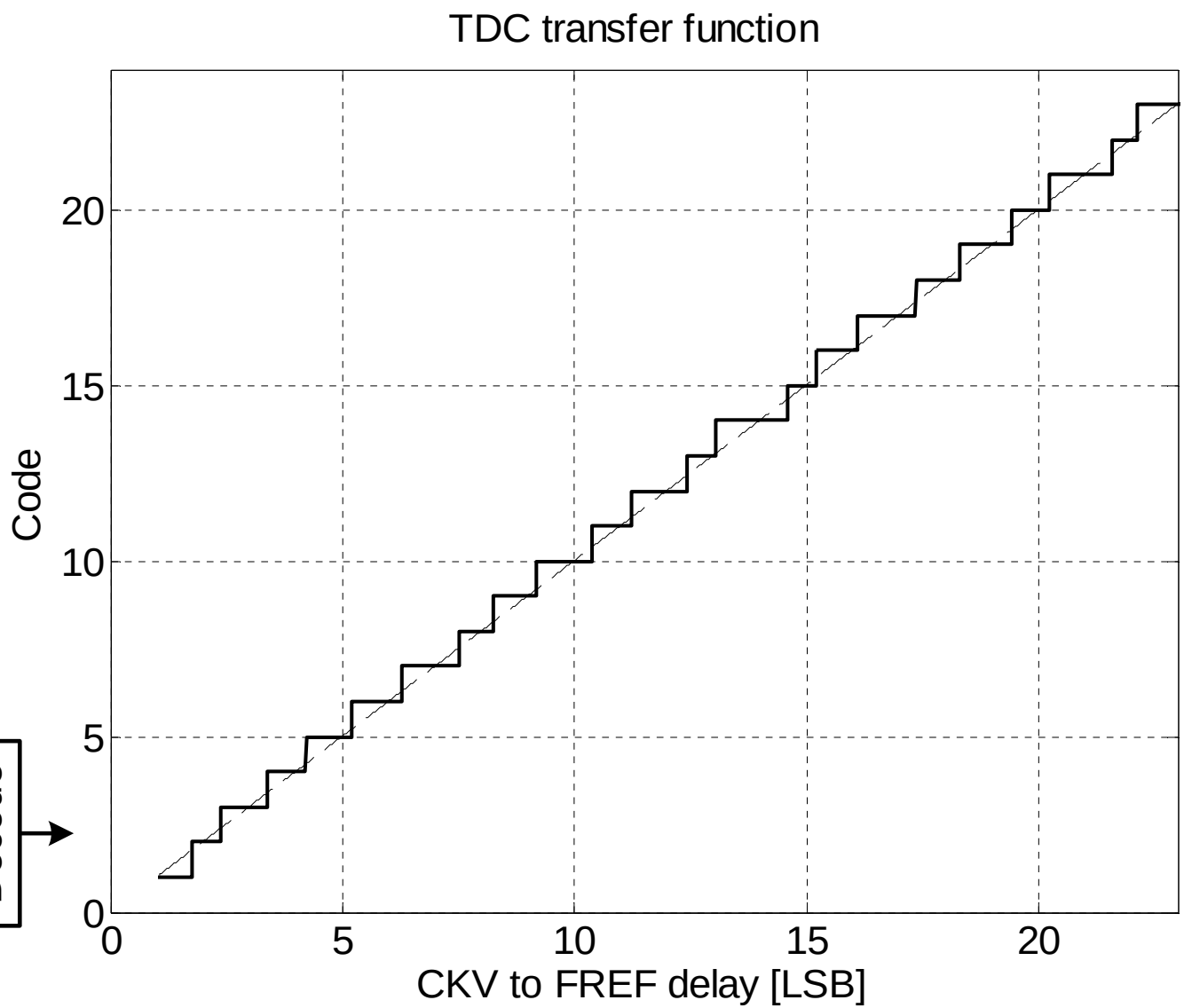




Measured TDC Transfer Function

- Only even-odd nonlienarity

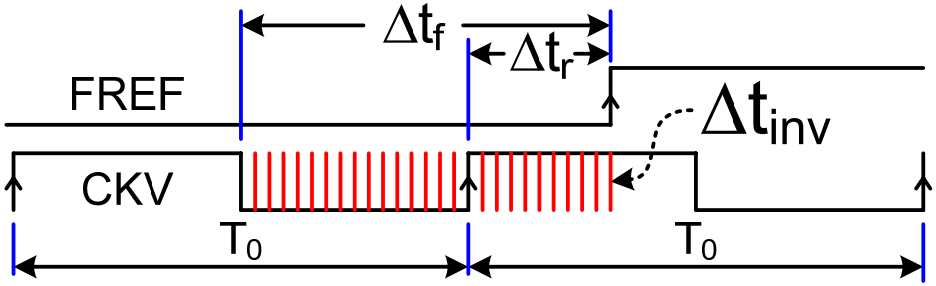




TDC Normalization

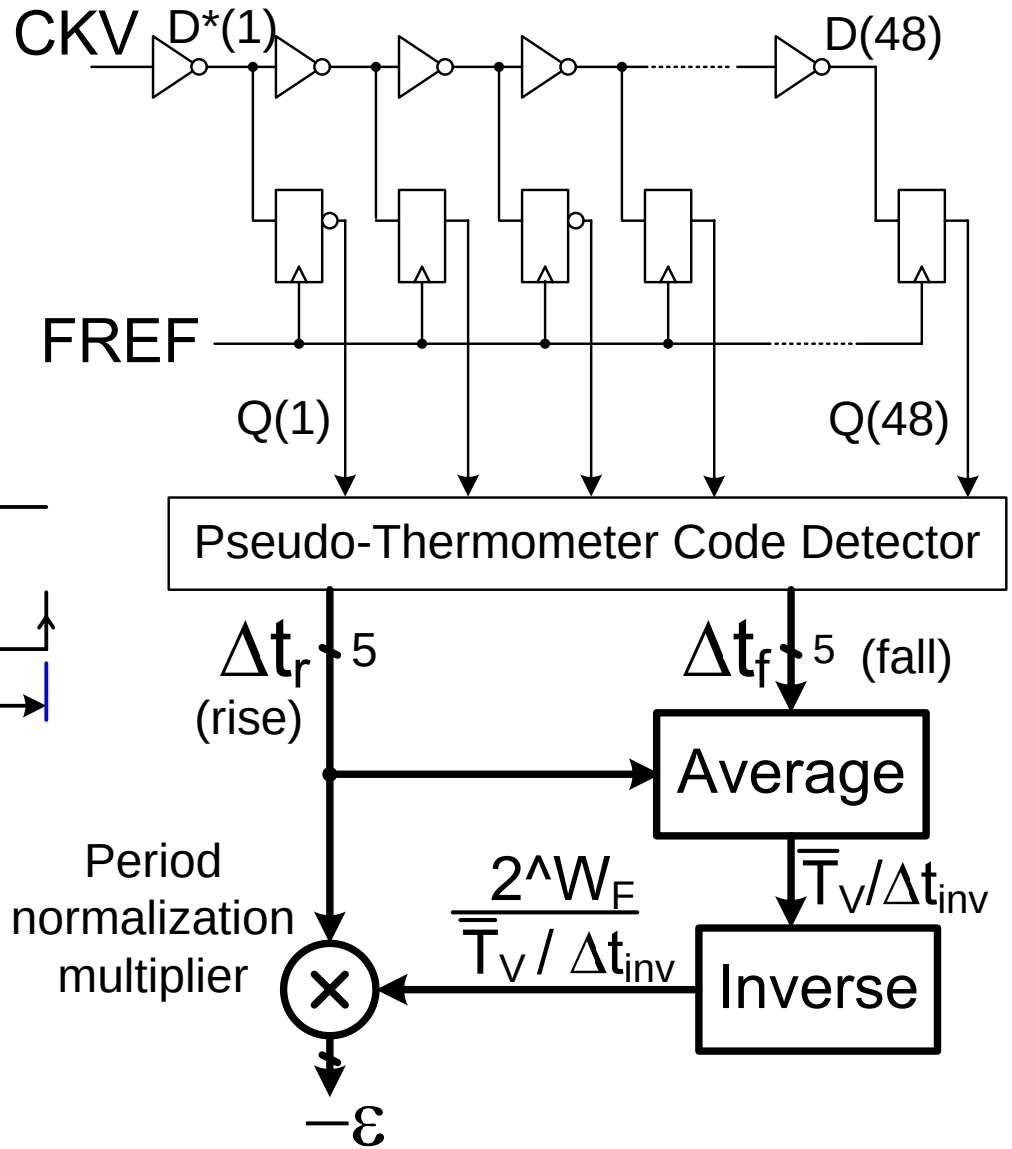
- Expected output between 0.0 – 1.0 UI

$$-\varepsilon = \frac{2^{W_F}}{\overline{T}_V / \Delta t_{inv}}$$



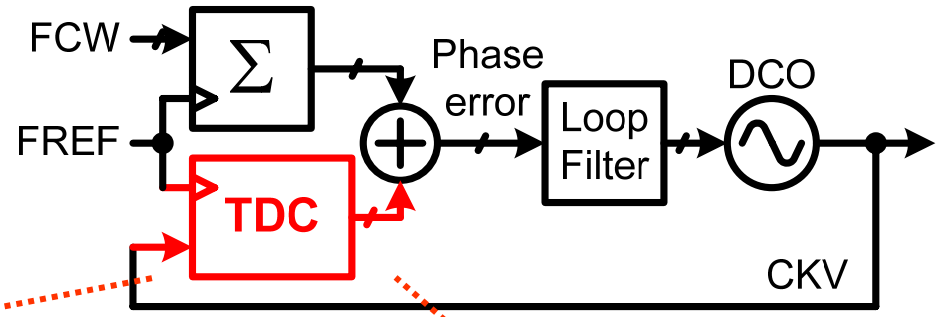
- Accurate calibration of the inverter delay

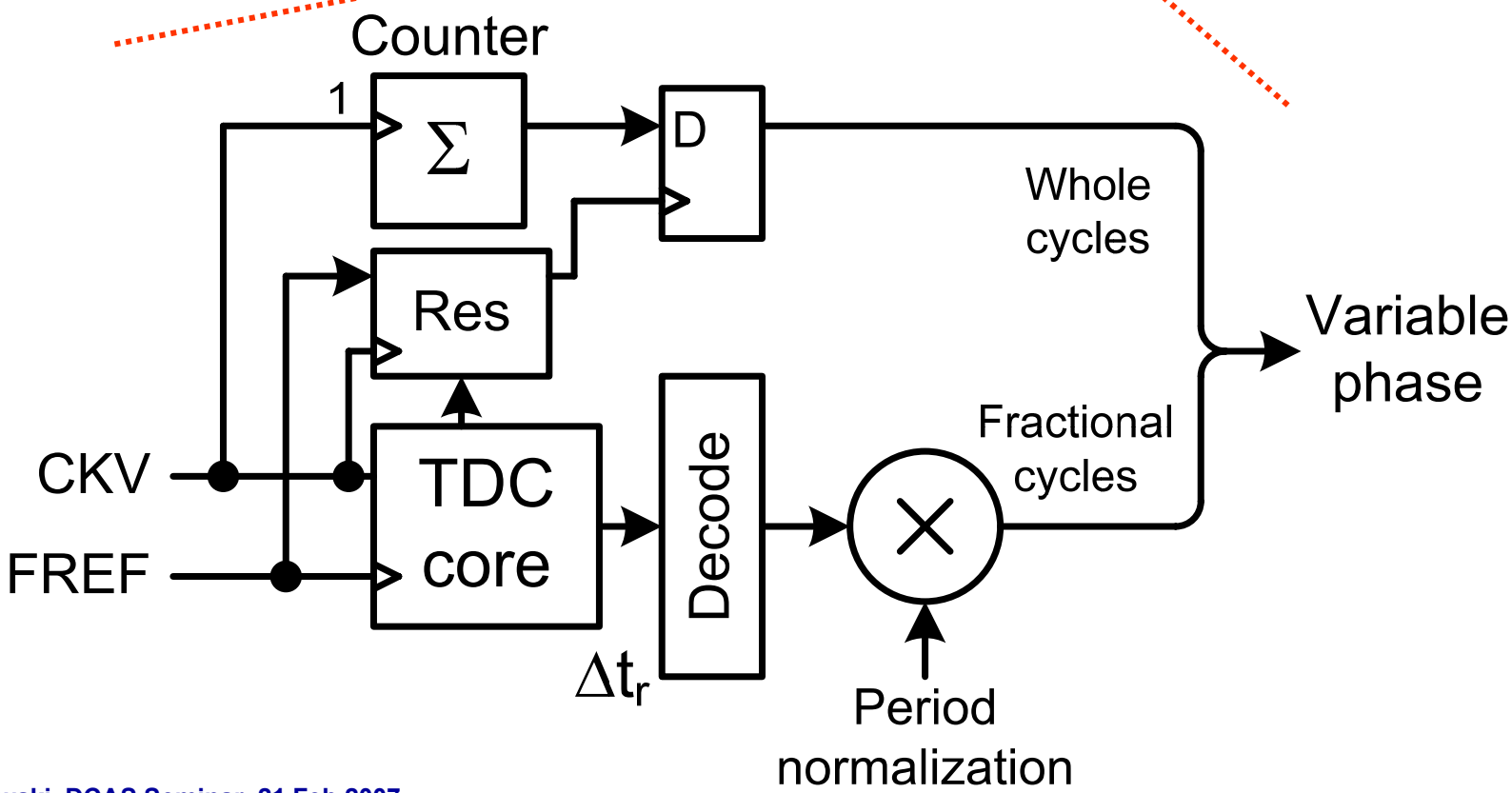
$$\overline{T}_V = \frac{1}{N_{avg}} \sum_{k=1}^{N_{avg}} T_V[k]$$



TDC System

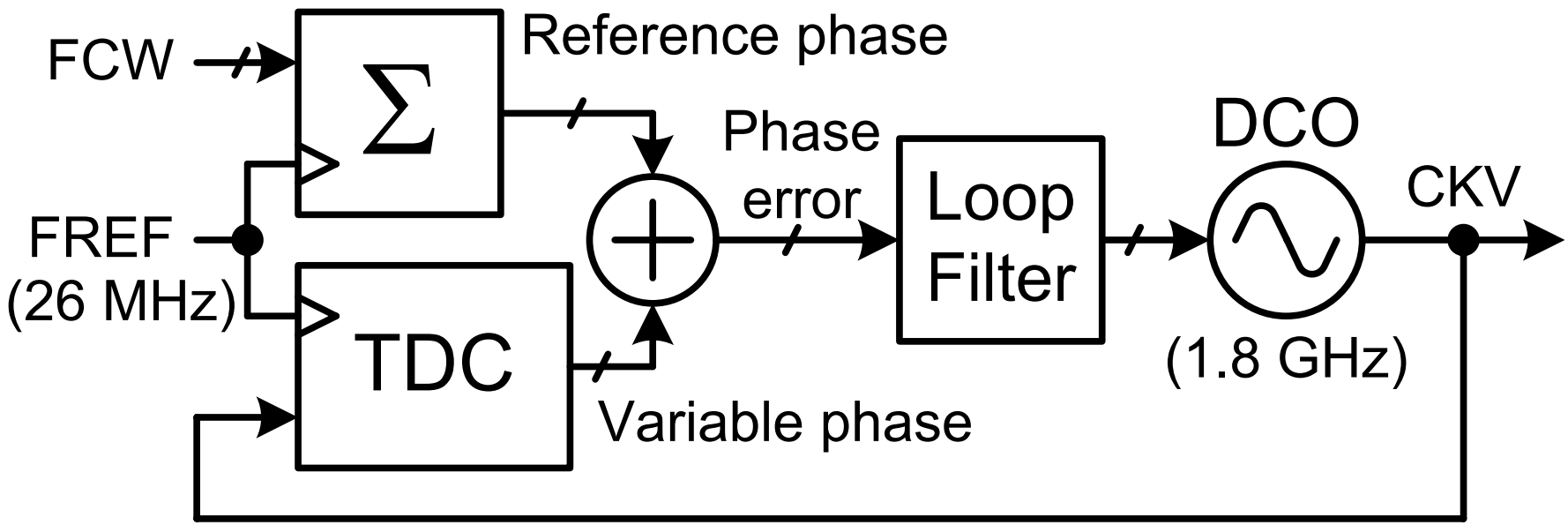
- Extended dynamic range
- Resampler needed to avoid metastability



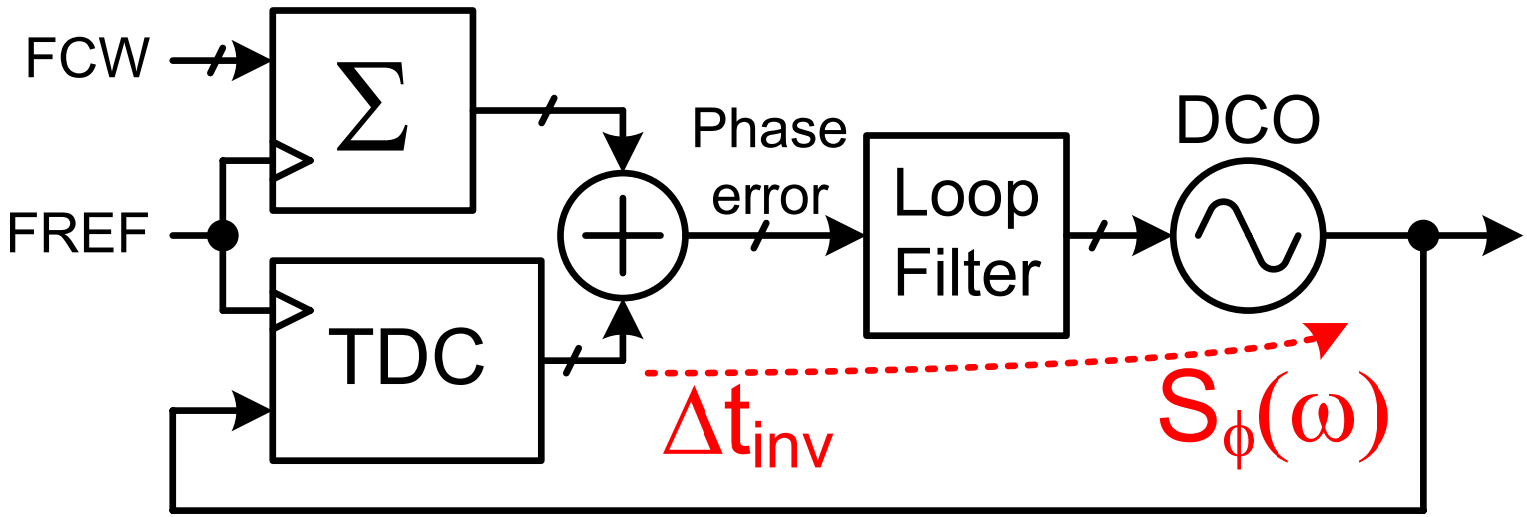


TDC-Based All-Digital PLL

- TDC replaces the conventional PFD and charge pump
- TDC measures the actual FREF timestamps
- FCW is a fixed-point frequency multiplication ratio
- FREF timestamps compared with accumulated FCW



Phase Noise Due to TDC



- In-band phase noise at RF output [TCAS-II'06]

$$L = \frac{(2\pi)^2}{12}\left(\frac{\Delta t_{inv}}{T_V}\right)^2 \cdot \frac{1}{f_R}$$

  - E.g., Δt_{inv}=20ps, f_v=1.8GHz, f_R=26MHz, **L = -97.8dBc/Hz**
  - Good enough for GSM: can get only better

Digitally-Controlled Oscillator (DCO)

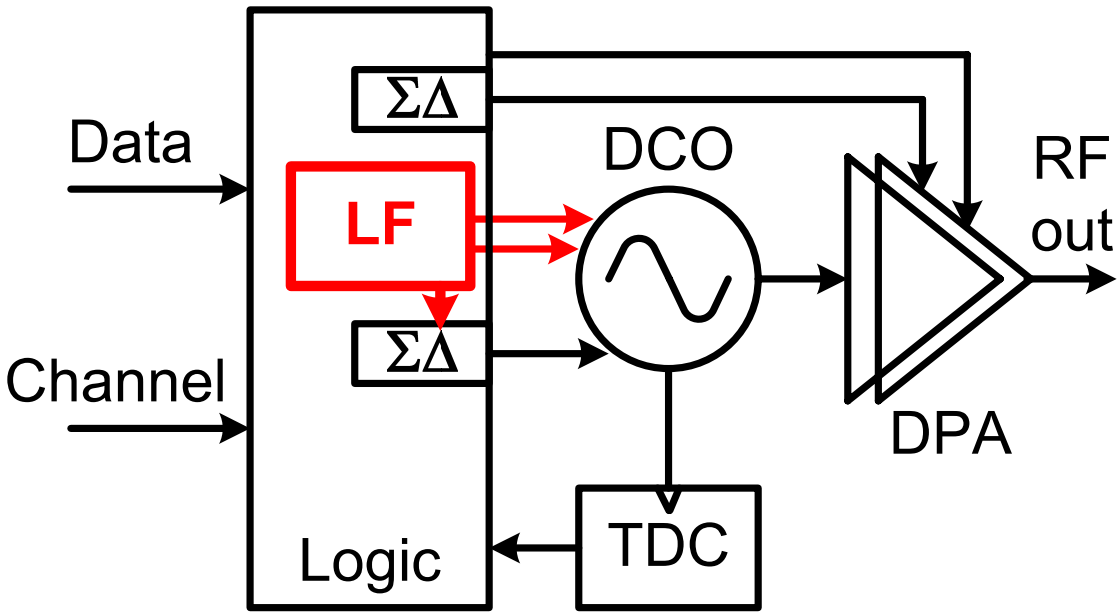
ΣΔ Modulator and DCO Interface

Time-to-Digital Converter (TDC)

Digital Loop Filter (LF)

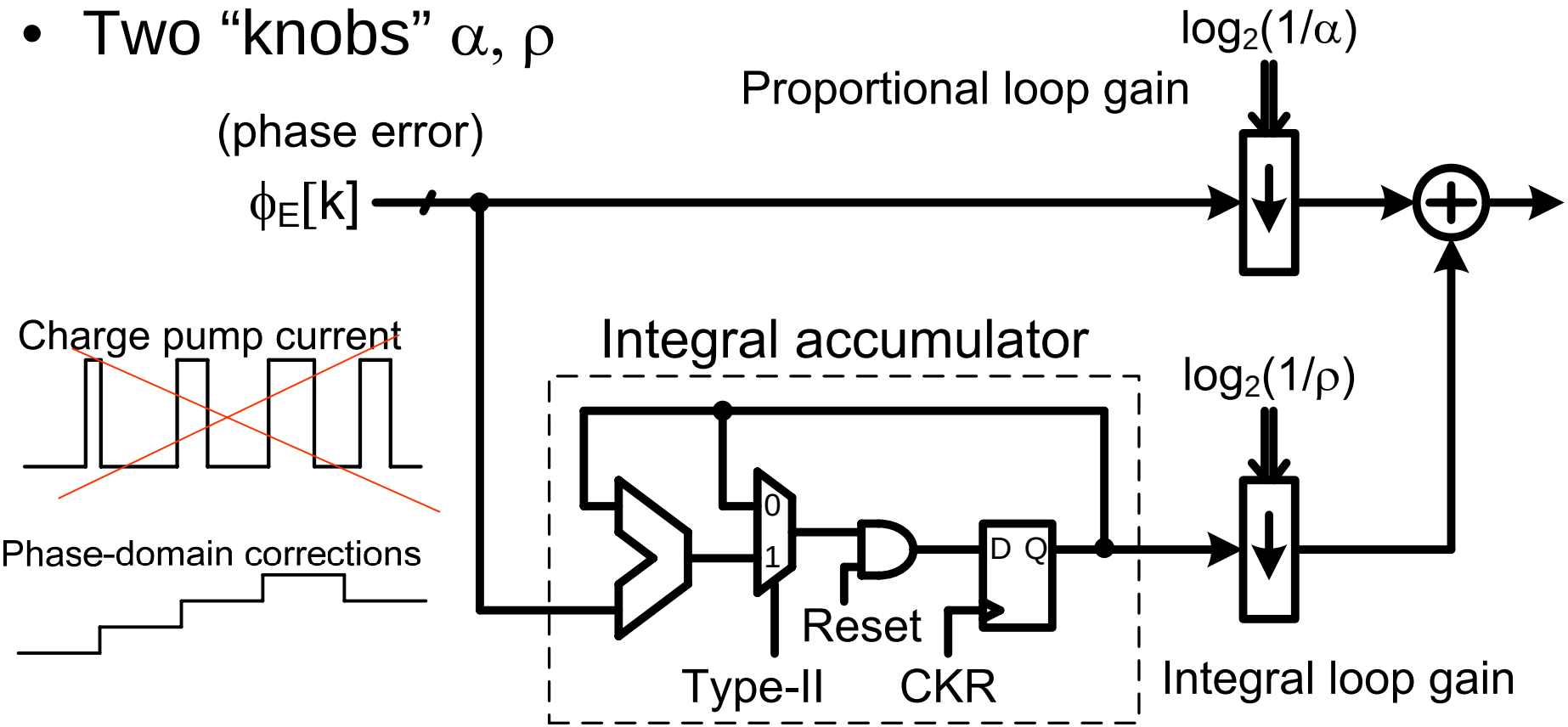
All-Digital PLL (ADPLL)

ADPLL Wideband Frequency Modulation



Type-II Loop Filter

- No correlative detection spurs
- Software programmed PLL loop:
  - Gentle transition of type-I to type-II
- Two "knobs" α, ρ

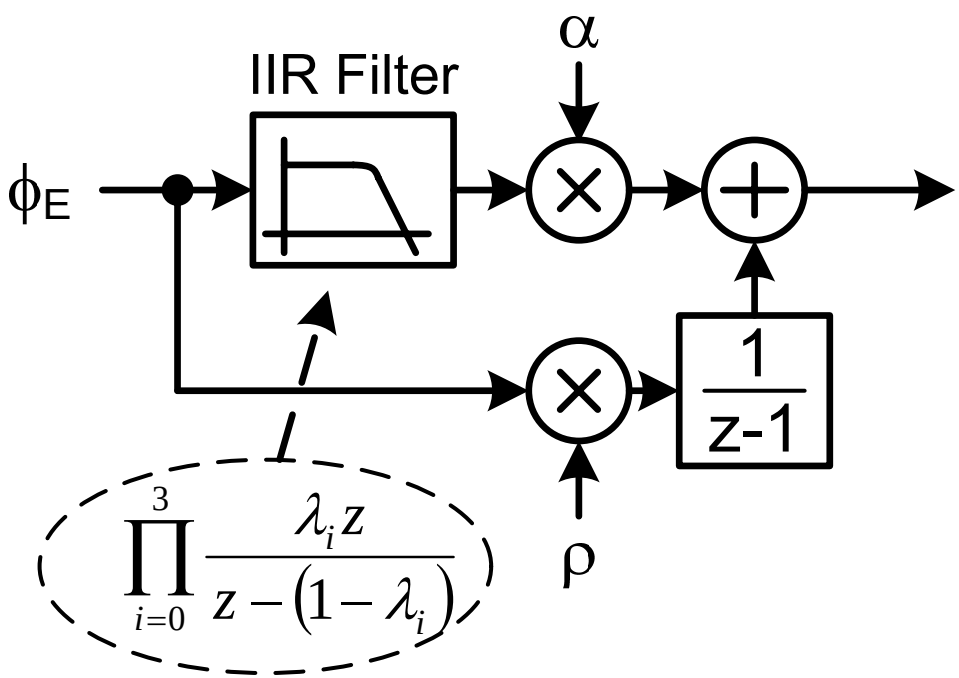


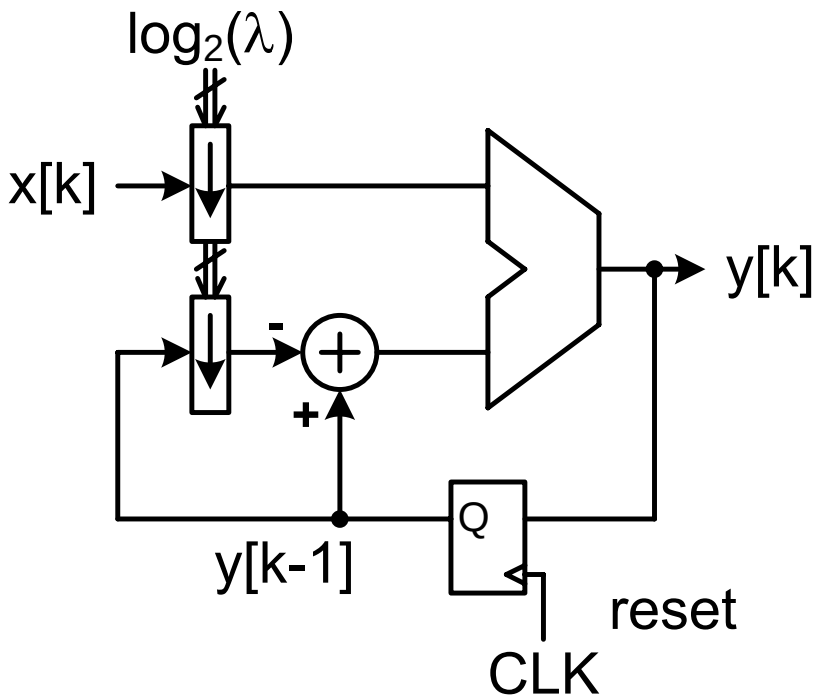
Loop filter with IIR Filtering

- 4th order digital IIR loop filter to suppress the frequency reference and TDC quantization noise
- Unconditionally stable IIR filter

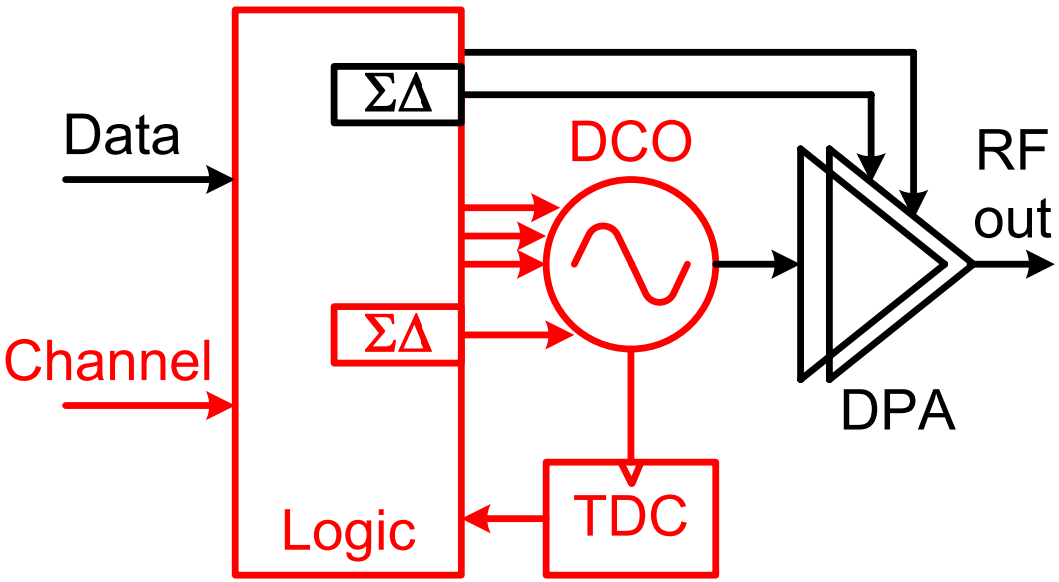
Single-pole IIR stage:

$$y[k] = (1-\lambda)\cdot y[k-1] + \lambda \cdot x[k]$$





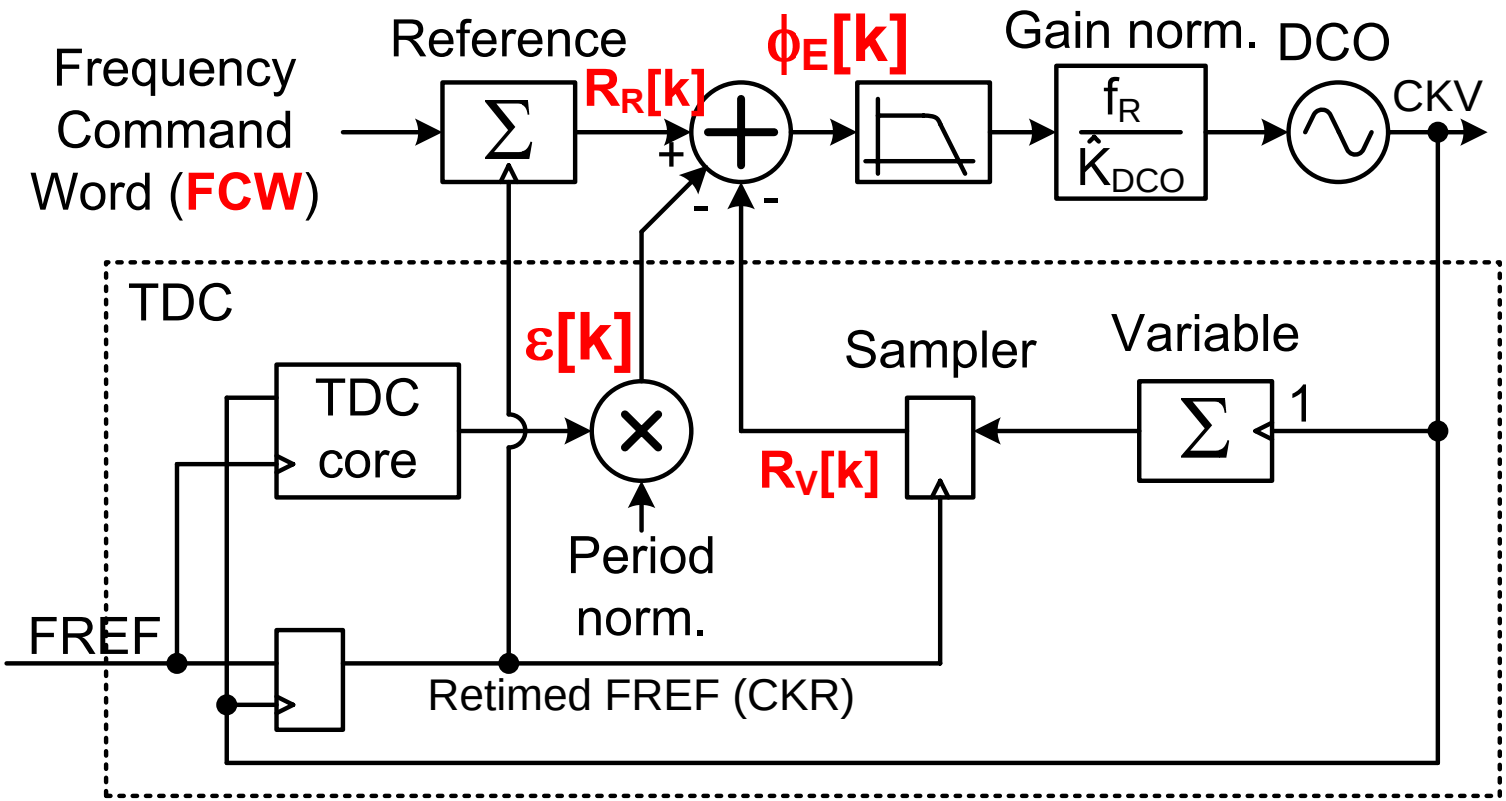
Digitally-Controlled Oscillator (DCO)
ΣΔ Modulator and DCO Interface
Time-to-Digital Converter (TDC)
Digital Loop Filter (LF)
All-Digital PLL (ADPLL)
ADPLL Wideband Frequency Modulation



All-Digital PLL (ADPLL)

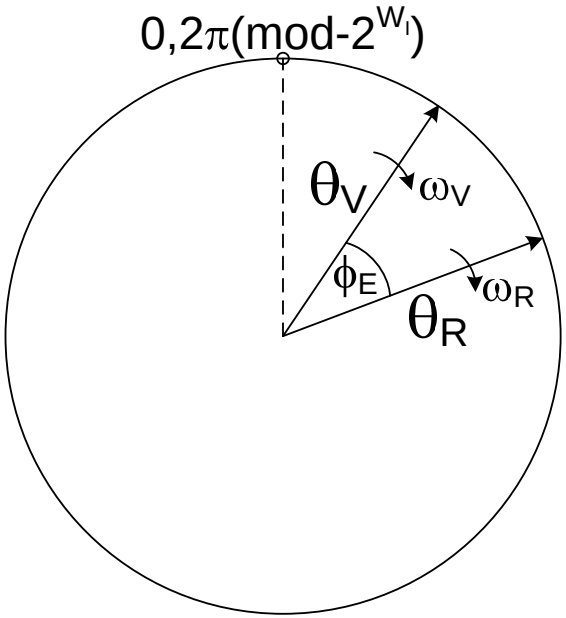
- Phase domain operation
- Digitally synchronous fixed-point arithmetic
- Phase signals cannot be corrupted by noise

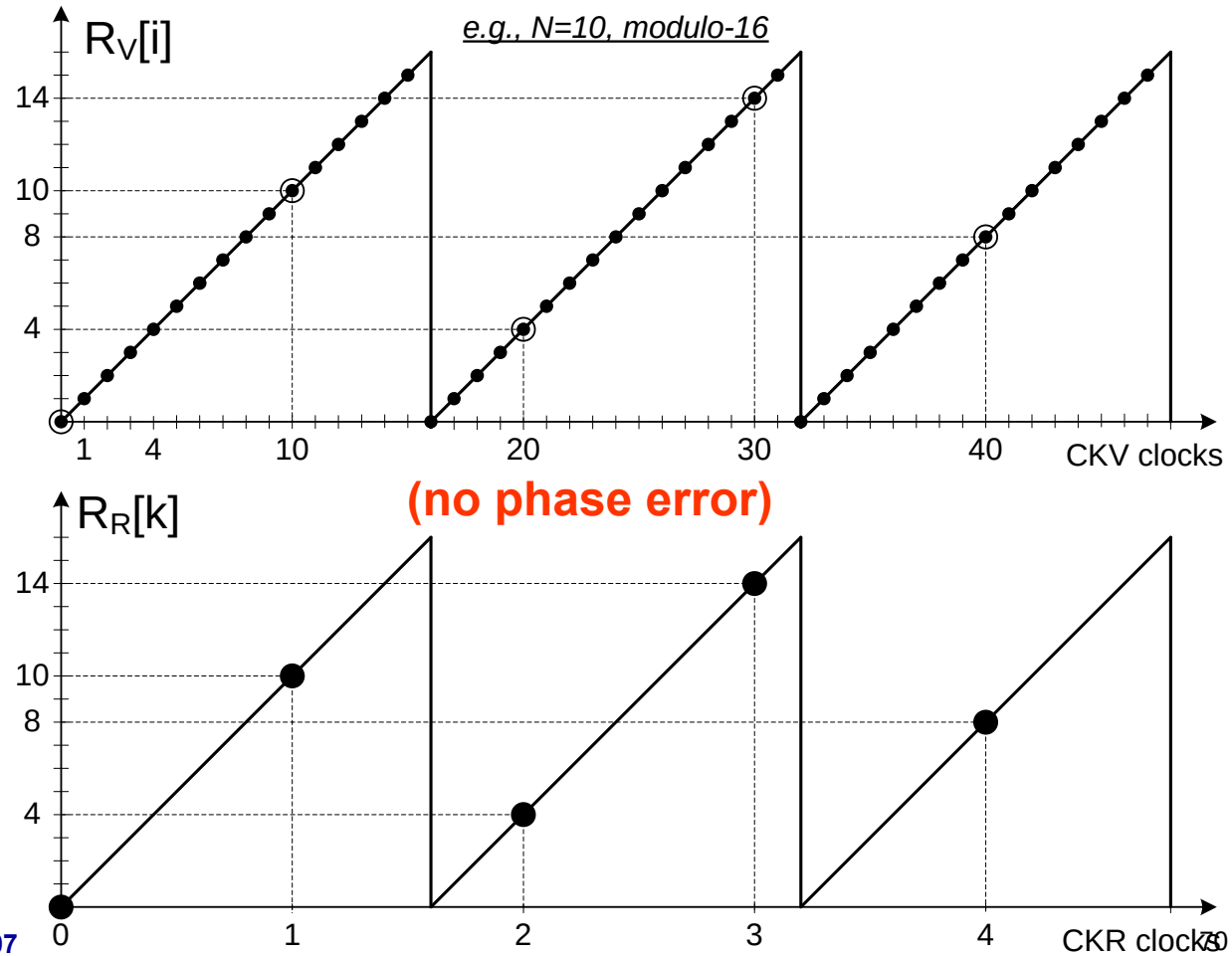
$$\varphi_E = R_R[k] - (R_V[k] + \varepsilon[k])$$



Modulo Arithmetic

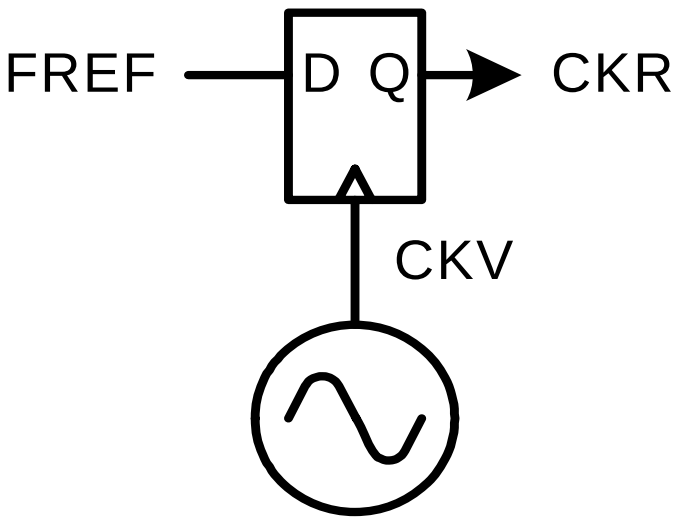
- Theoretically, reference θ_R and variable θ_V phases grow without bound
- θ_R and θ_V implemented in modulo arithmetic to limit wordlength: $W_I = 8$, $W_F = 15$

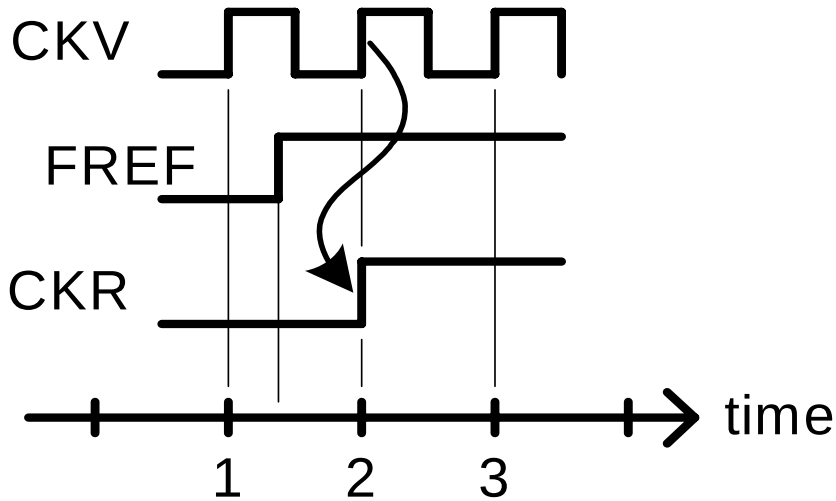




Reference Phase Retiming

- DCO clock and FREF domains are not entirely synchronous despite being in phase lock
- Variable and reference phases cannot be compared in hardware: metastability!
- Solution: Oversampling FREF by CKV and using the resulting CKR

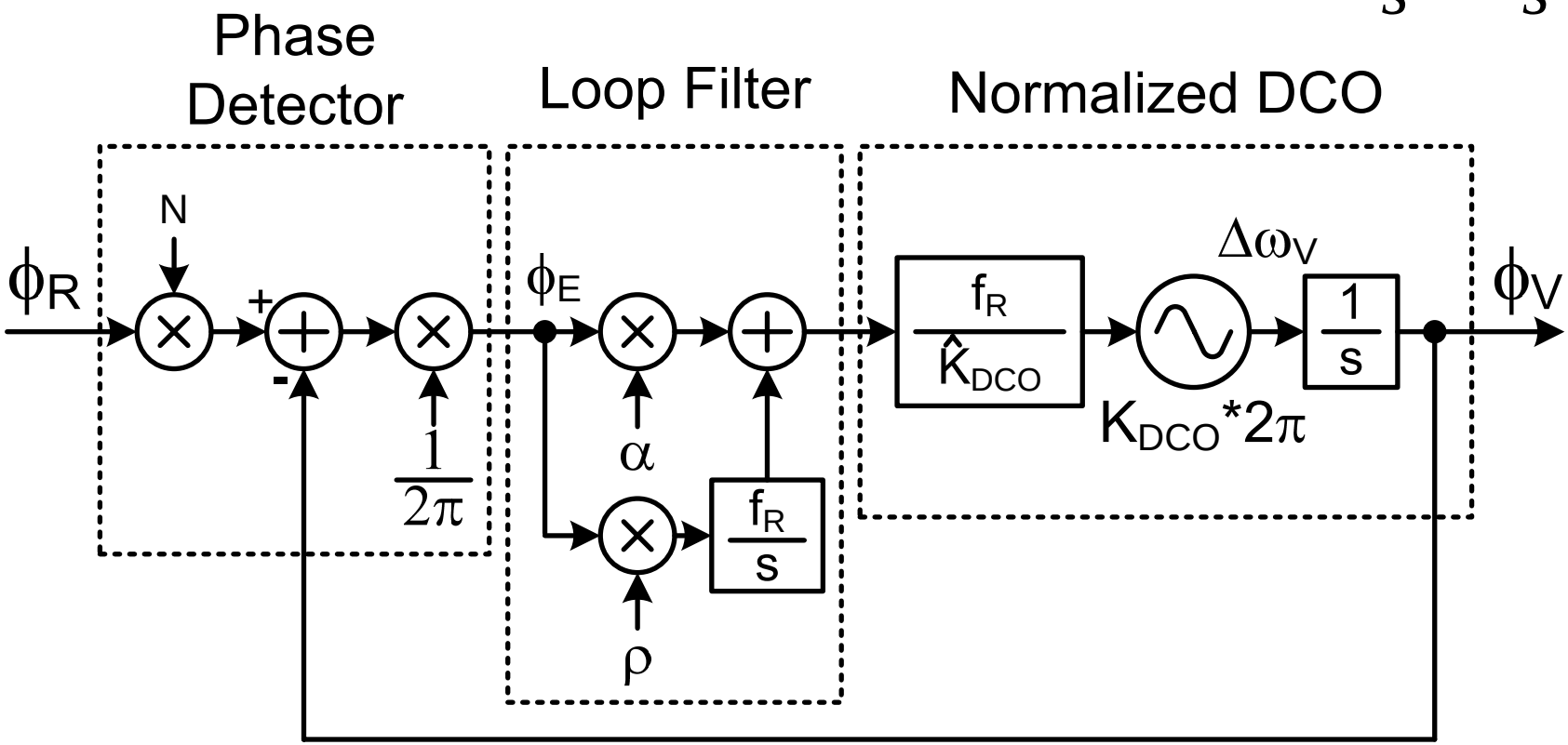




Frequency Response of 2nd-order PLL

- IIR filter turned off
- Type-II second-order PLL loop
- "knobs" α, ρ

$$H_{ol}(s) = (\alpha + \frac{\rho f_R}{s}) \frac{f_R}{s}$$



2nd-order PLL: Closed-Loop Response

- Closed-loop transfer function

$$H_{cl}(s) = N\frac{\alpha f_R s + \rho f_R^2}{s^2 + \alpha f_R s + \rho f_R^2}$$

- Canonical two-pole control system

$$H_{cl}(s) = N\frac{2\xi\omega_n s + \omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2}$$

Natural frequency

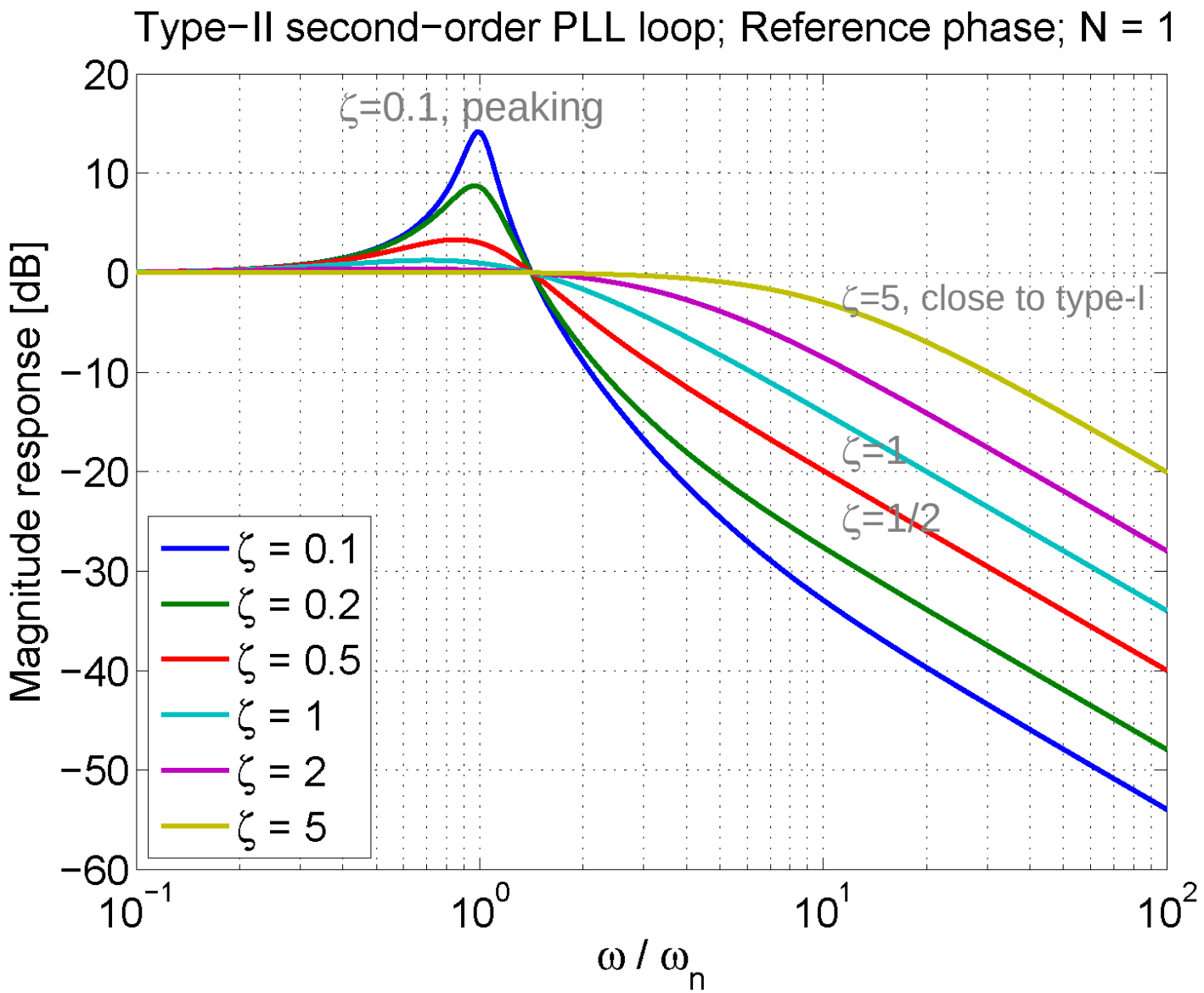
$$\omega_n = \sqrt{\rho}\, f_R$$

Damping factor

$$\xi = \frac{1}{2}\frac{\alpha}{\sqrt{\rho}}$$

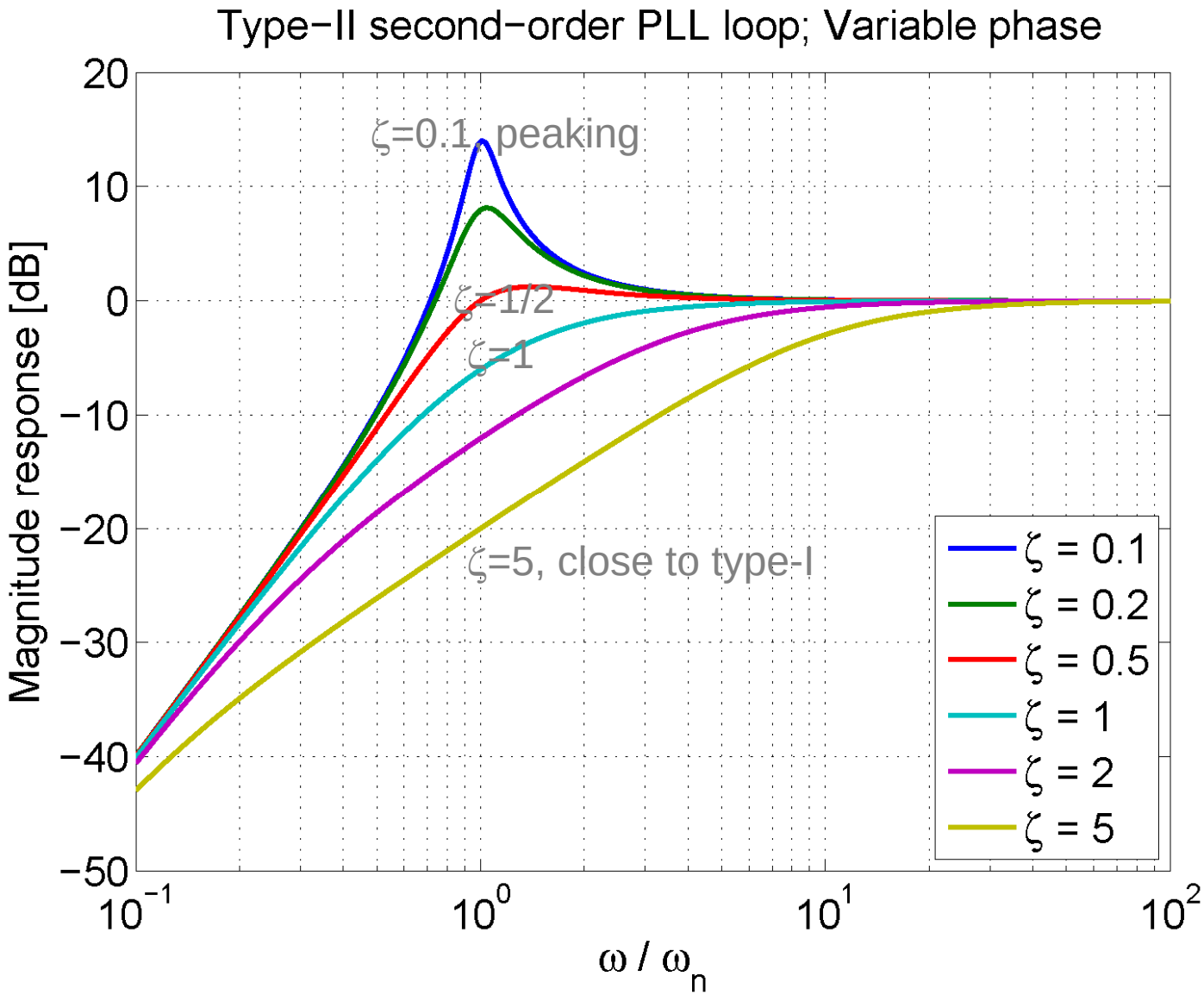
FREF/TDC Transfer Function

- Type-II 2nd order PLL
- Weak filtering



DCO Transfer Function

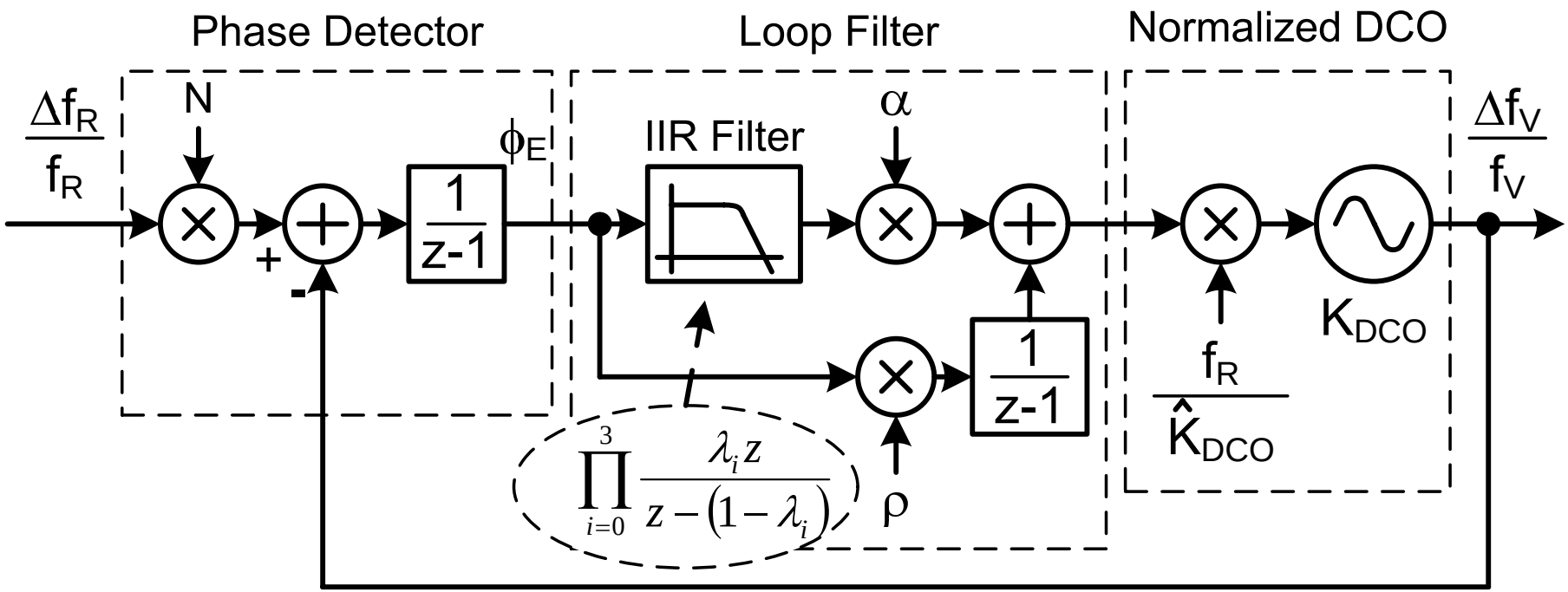
- Type-II 2nd order PLL
- 20 dB/dec
  - Type-I
- 40 dB/dec
  - Type-II
- 1/f noise attenuation



z-Domain Model of the ADPLL

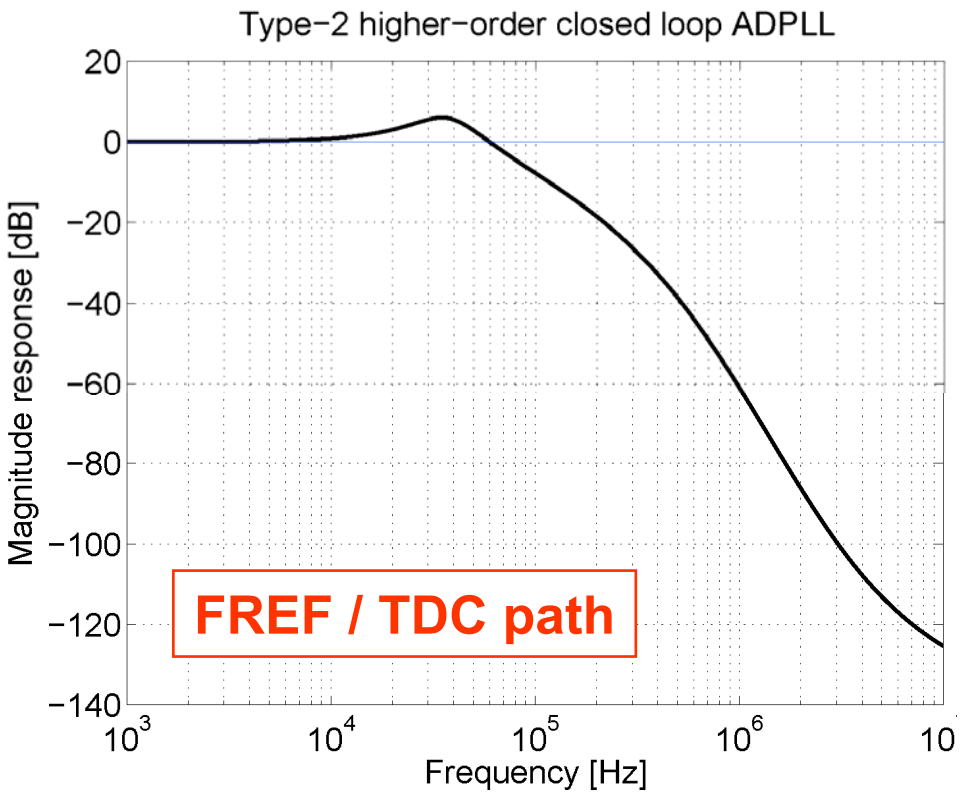
- "knobs" α, ρ, $\lambda_{1\text{-}4}$
- Type-I or Type-II PLL loop
- 1st through 6th order

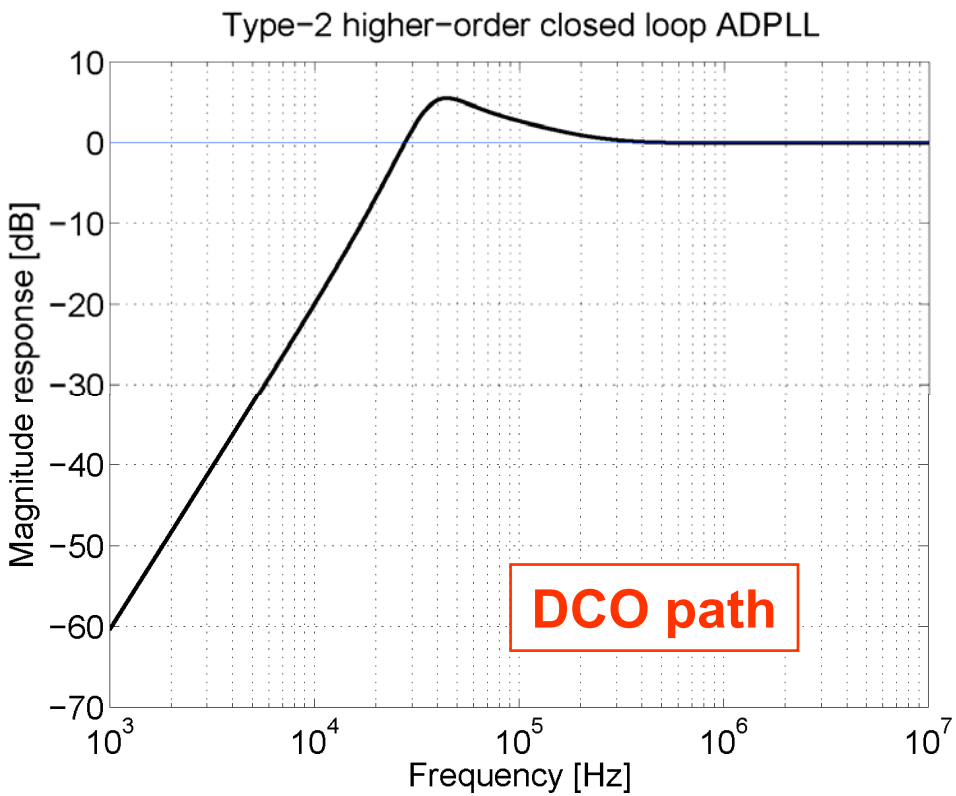
$$H_{ol}(s) = \left[\alpha \cdot H_{iir}(s) + \frac{\rho \cdot f_R}{s} \right] \frac{f_R}{s}$$



ADPLL Transfer Function

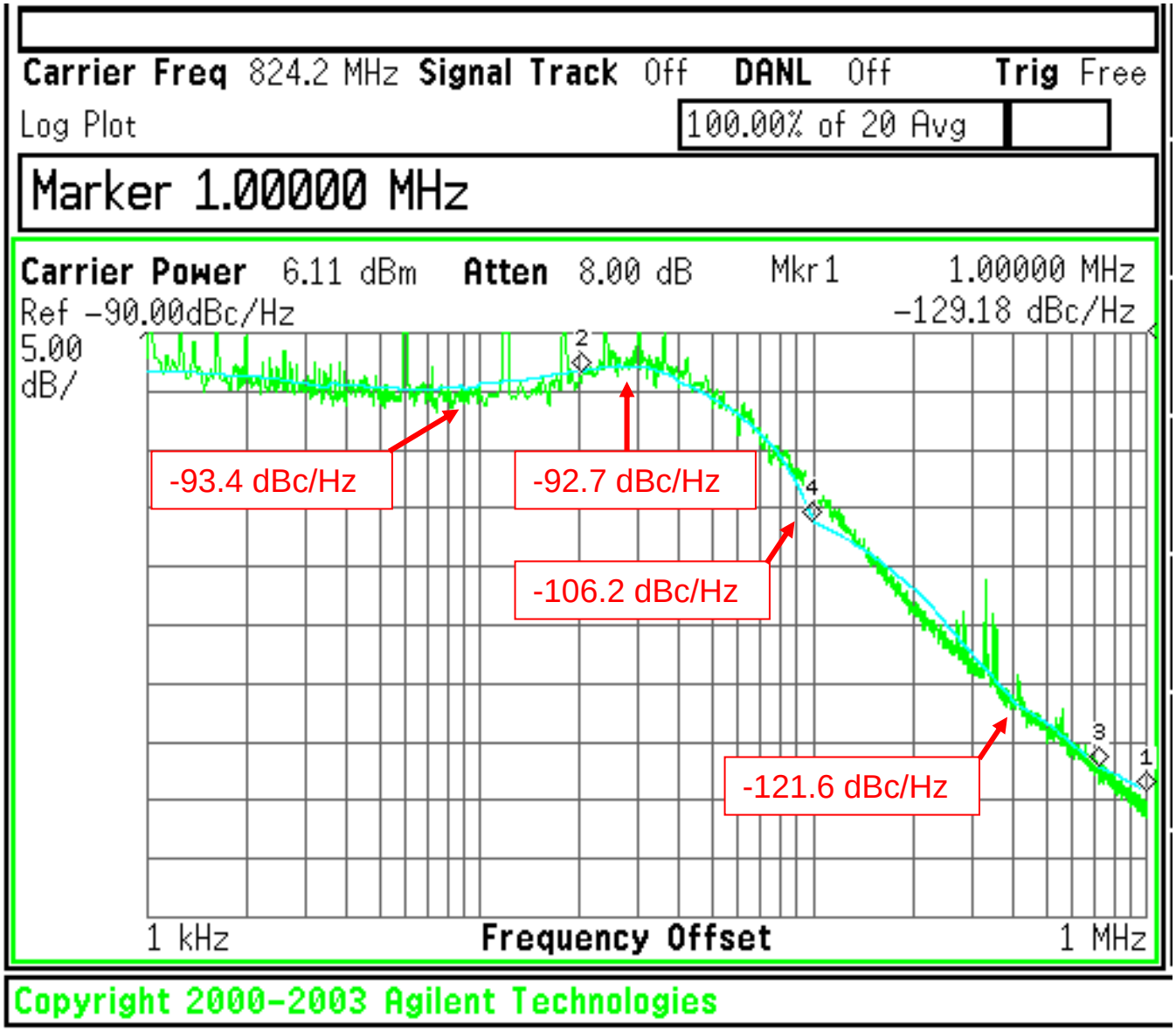
- Type-II 6^{th}-order PLL
- Settings: $\alpha = 2^{-7}$, $\rho = 2^{-15}$, $\lambda = 2^{-[3\ 3\ 3\ 4]}$
- Provides 33 dB of attenuation at 400 kHz
- Provides 40 dB/dec filtering of 1/f DCO noise



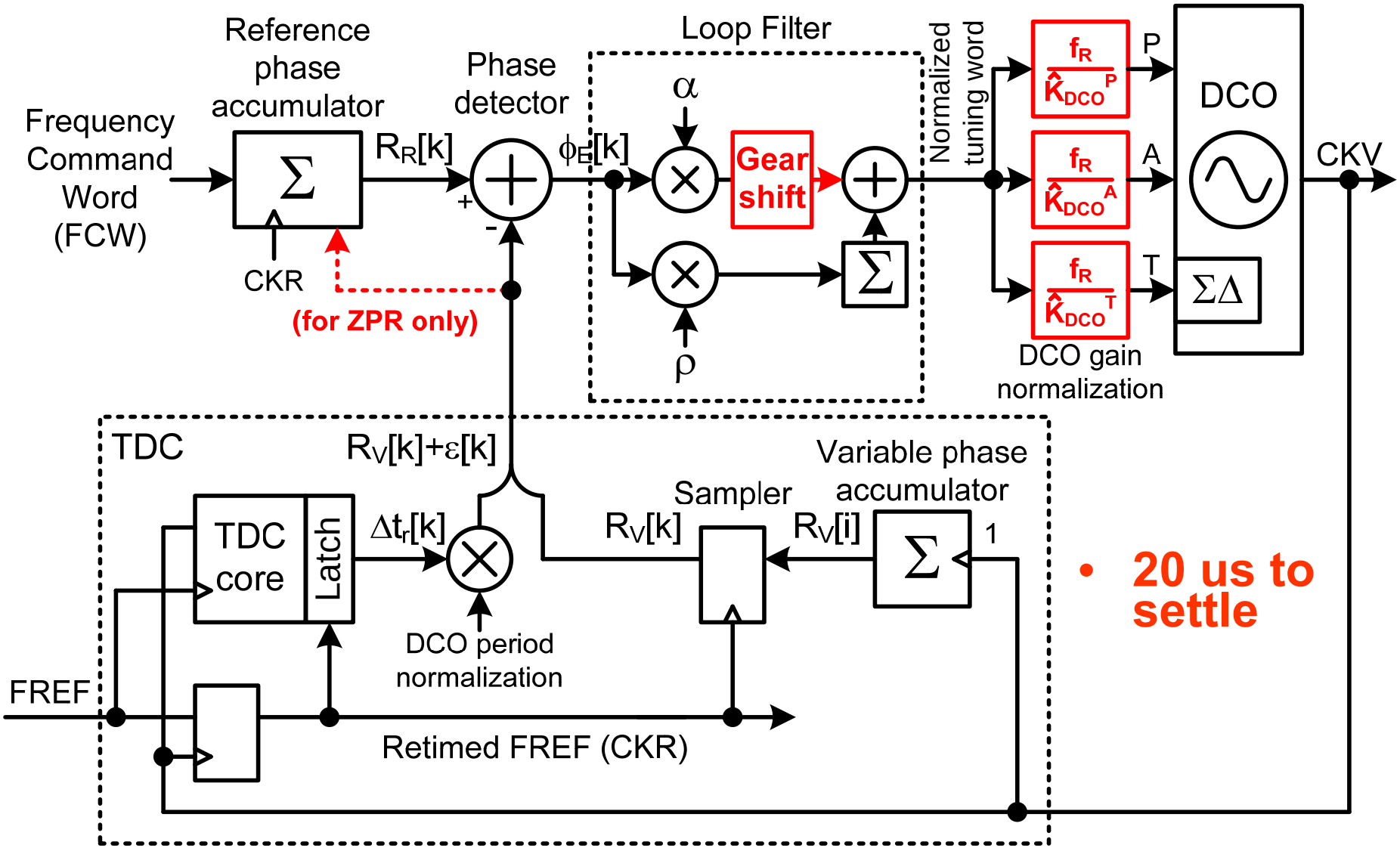


Measured Carrier Phase Noise

- 824.2 MHz carrier
- 26 MHz FREF
- -92…-95 dBc/Hz in-band phase noise
- 0.5 deg rms phase noise
  - Spec: 5 deg
- -122 dBc/Hz @ 400 kHz



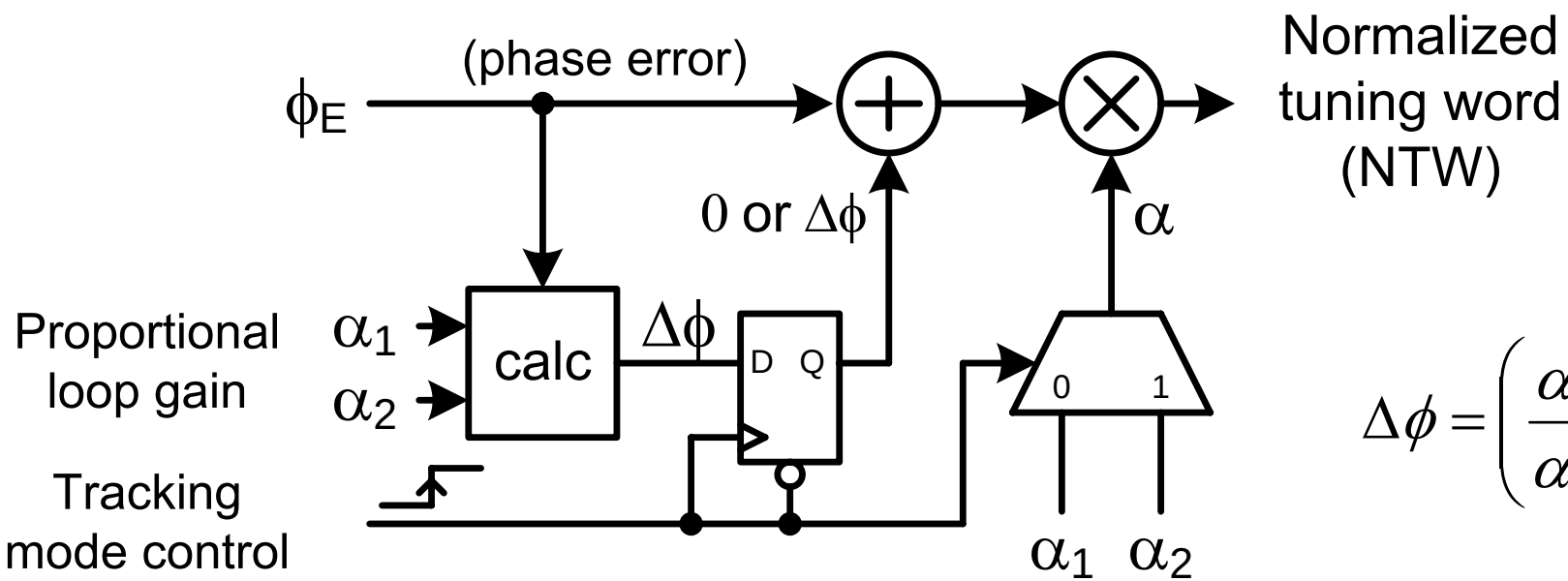
ADPLL with Zero Phase Restart



Gear Shifting of PLL Bandwidth

- Executed in tracking mode after the acquisition is completed
- Normalized tuning word continuity before and after the event
- Guarantees no frequency perturbation of the oscillator

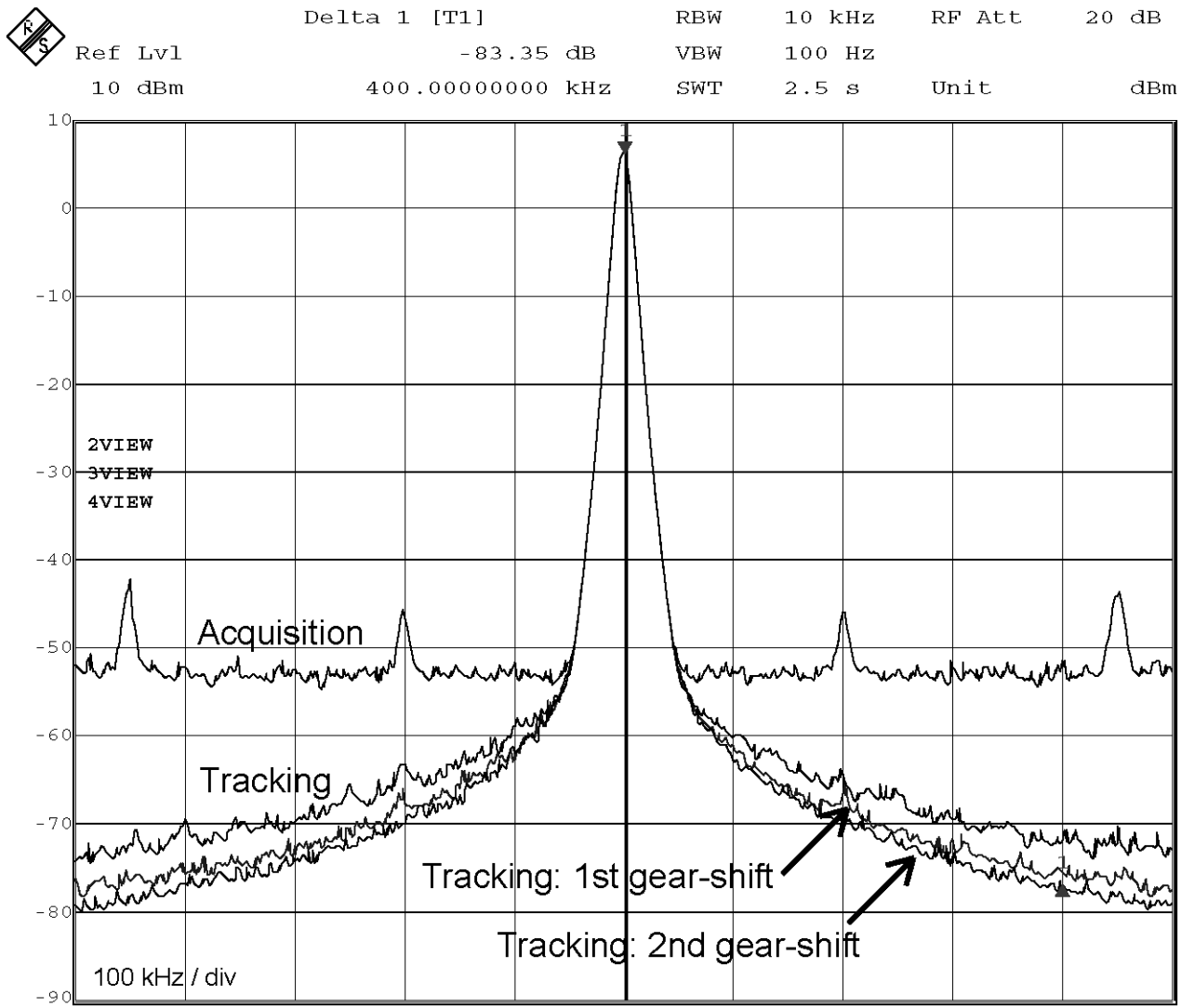
$$\alpha_1 \cdot \phi_1 = \alpha_2 \cdot (\phi_1 + \Delta\phi)$$



$$\Delta\phi = \left(\frac{\alpha_1}{\alpha_2} - 1\right)\phi_1$$

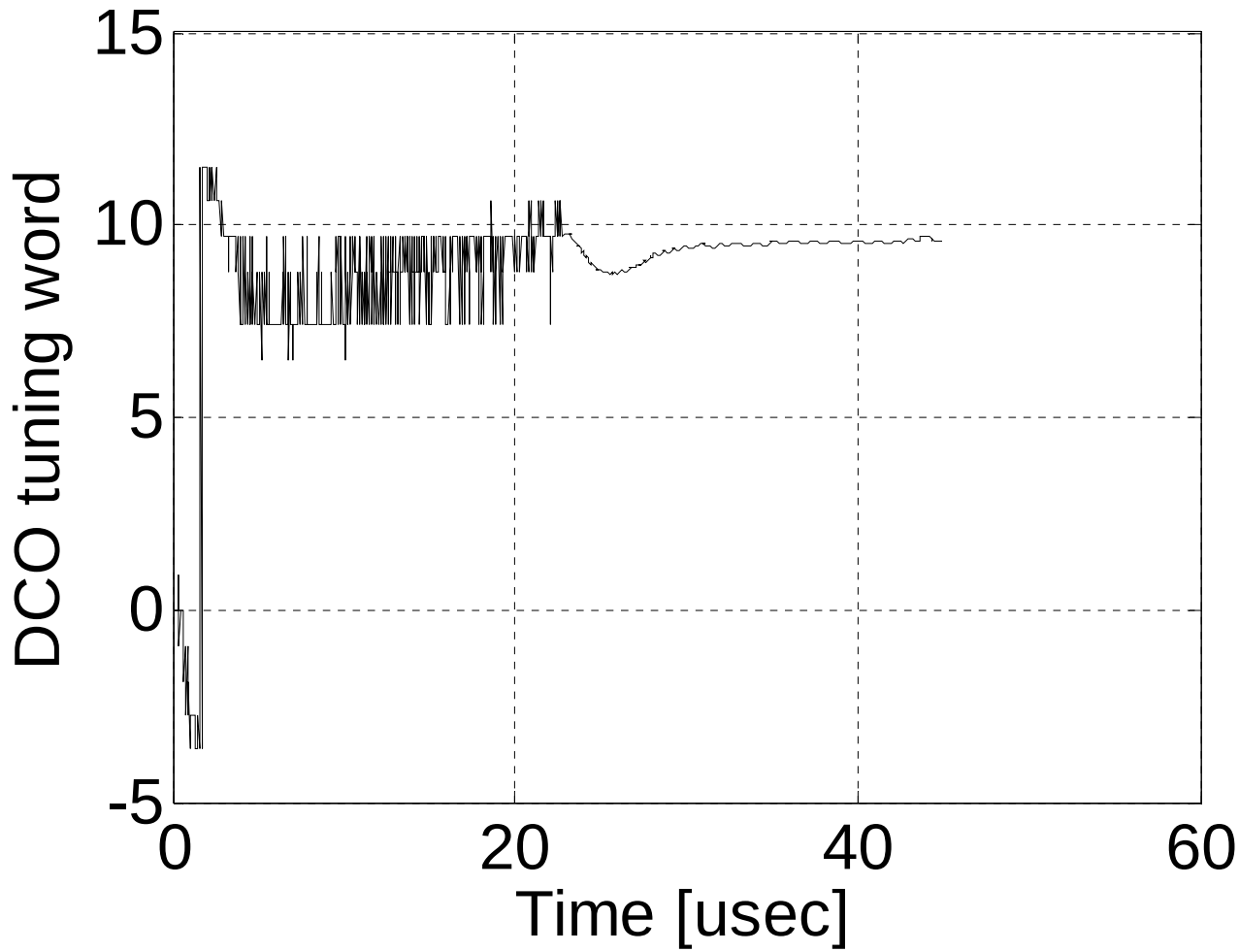
PLL Modes: Close-In Phase Noise

- Gradual phase noise improvement with narrowing down the loop bandwidth
- Little improvement after second gear shift when the DCO noise predominates



Measured Trajectory during Settling

- Gear shift at 23 us



Digitally-Controlled Oscillator (DCO)

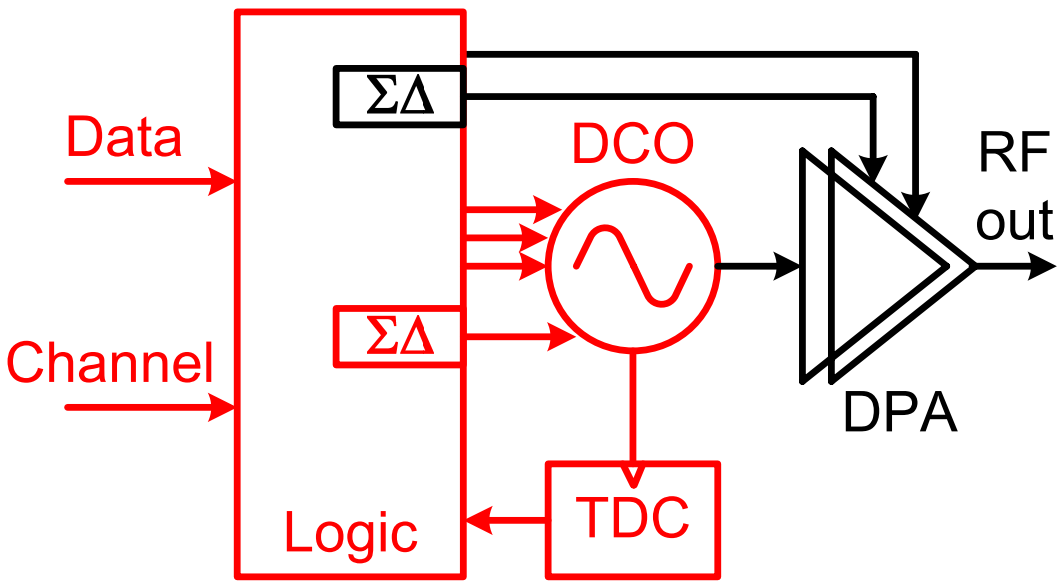
ΣΔ Modulator

Time-to-Digital Converter (TDC)

Digital Loop Filter (LF)

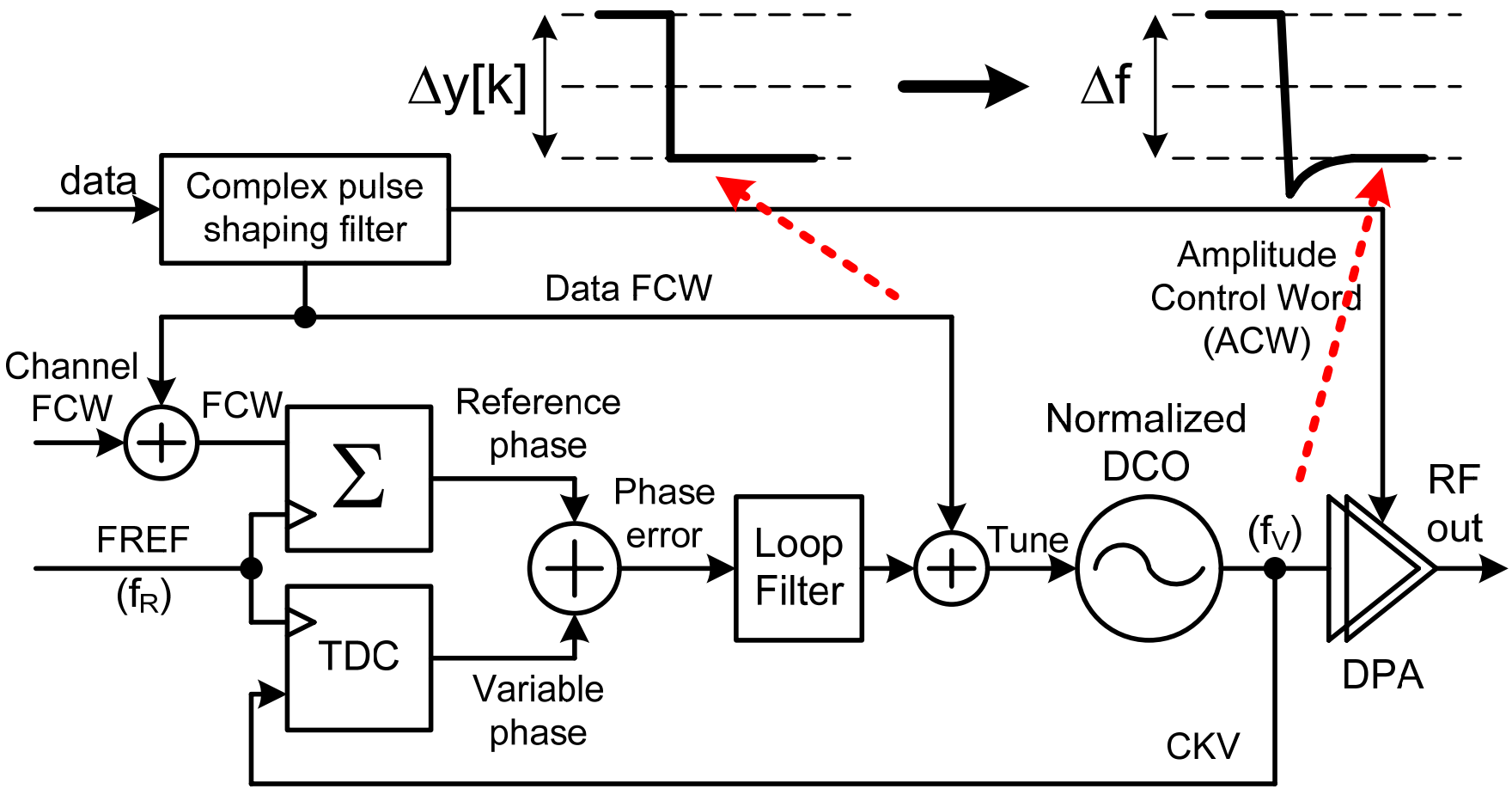
All-Digital PLL (ADPLL)

ADPLL Wideband Frequency Modulation

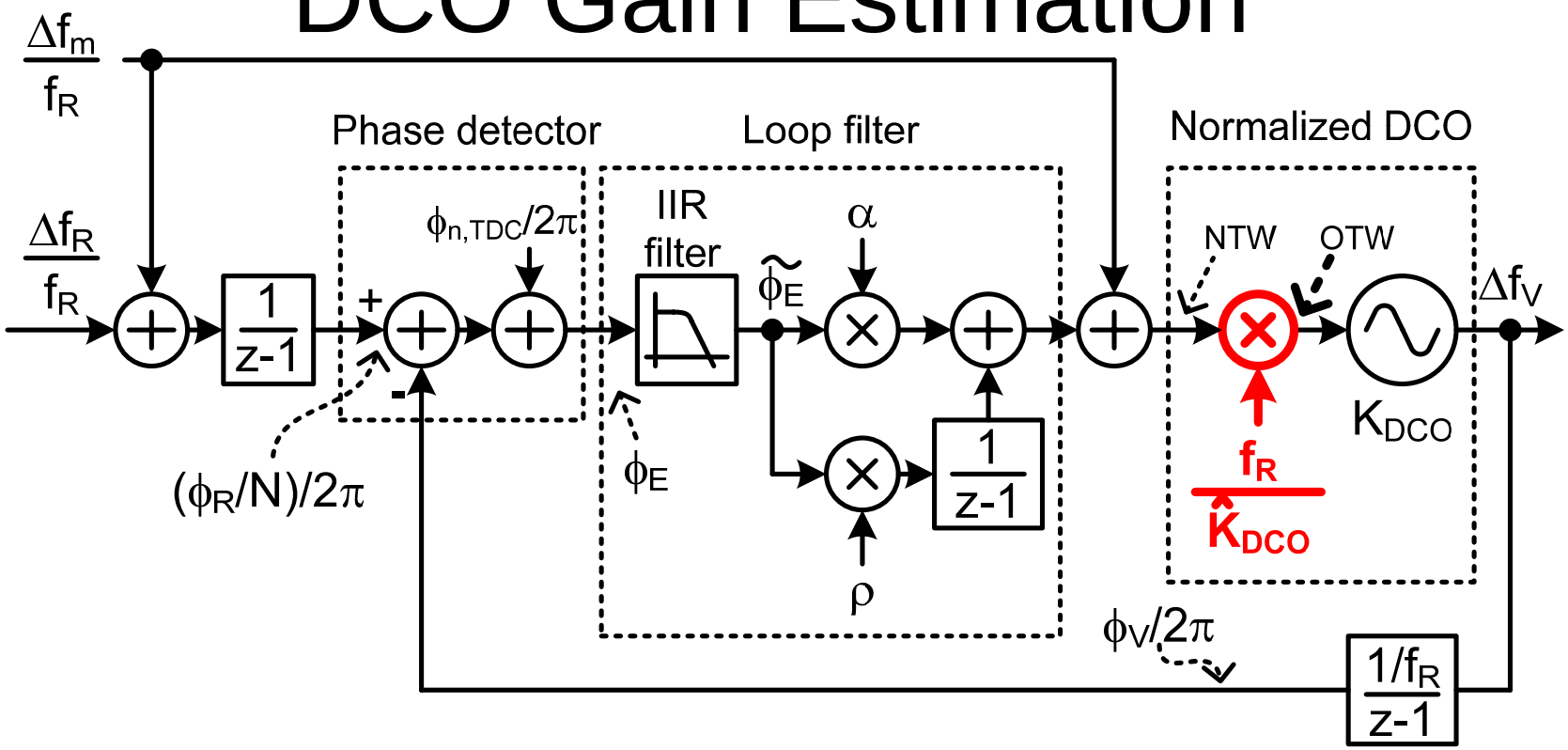


ADPLL with Wideband Modulation

- Two-point frequency modulation
  - Direct feedforward path – y[k] directly drives the DCO
  - Compensating path – y[k] added to the channel FCW



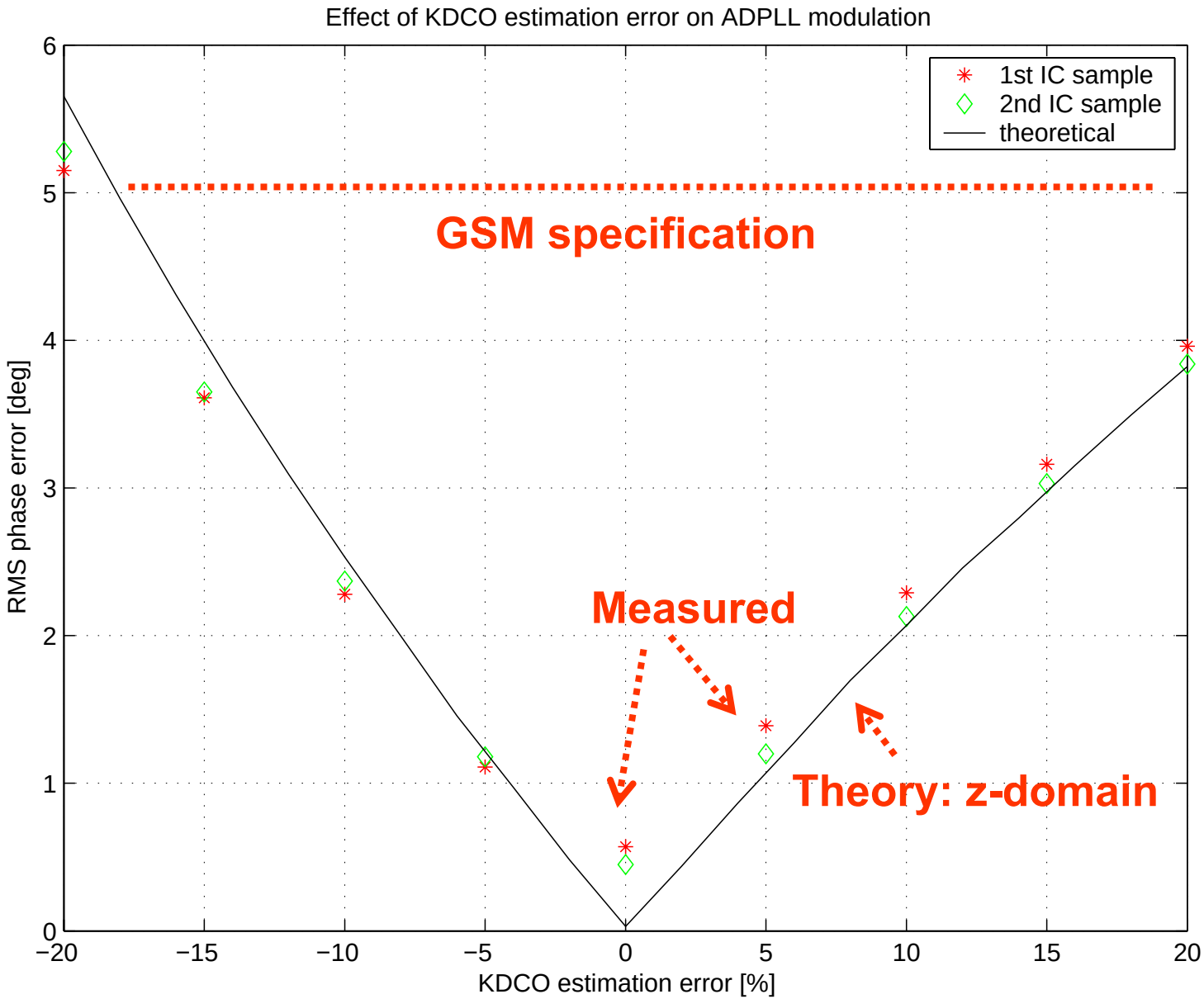
DCO Gain Estimation



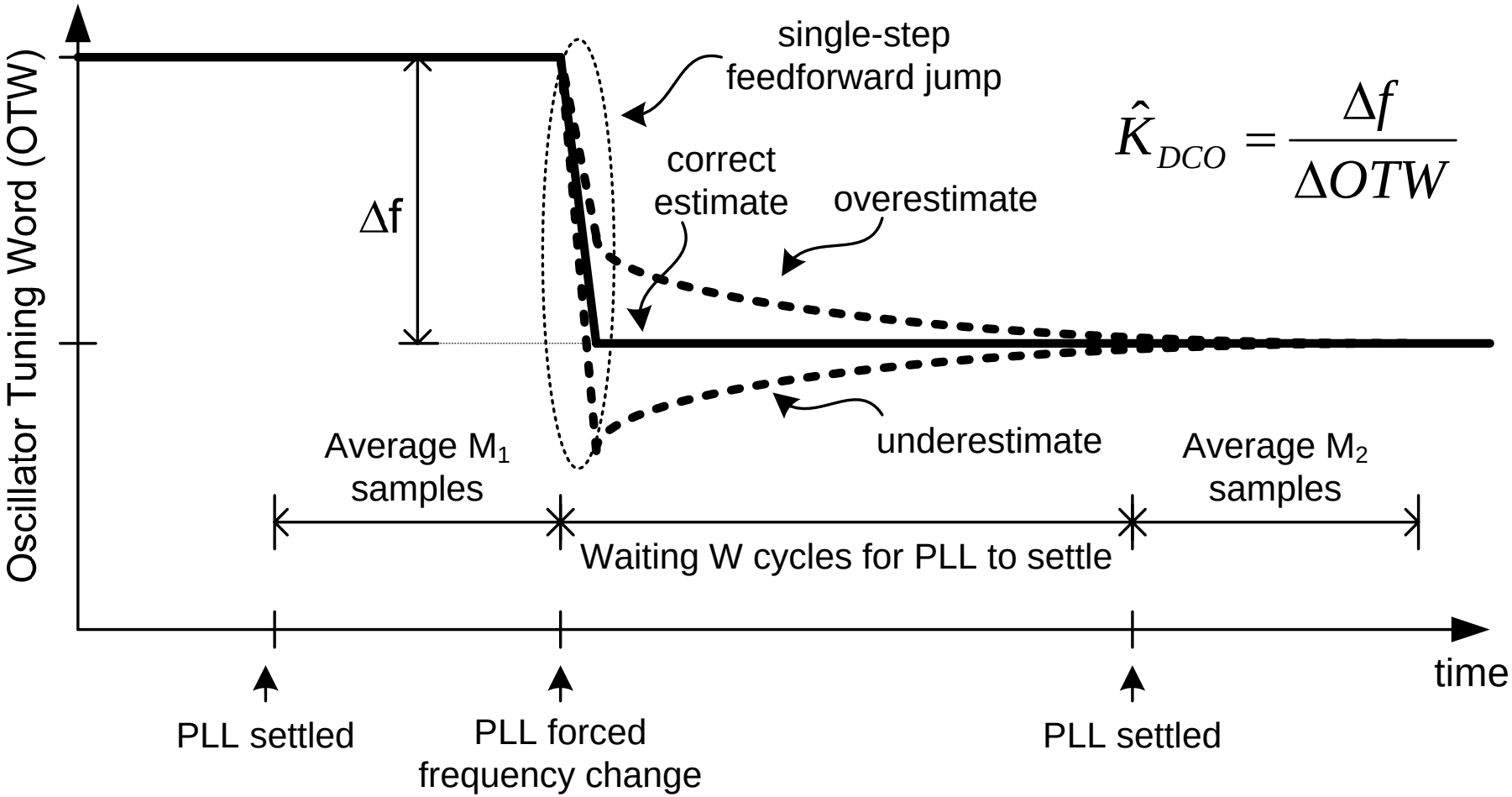
- Estimation of RF oscillator gain is critical in low-cost high-volume transceivers
  - RX: sets the loop bandwidth
  - TX: sets transfer function of the direct frequency modulation path
  - Tolerated gain estimation error from less than 1% (CDMA) to several % (GSM, Bluetooth)

K_{DCO} Error Effect on GSM Modulation

- Y-axis: RMS phase error [deg]
- X-axis: KDCO estimation error [%]
- KDCO estimation error of several % allowed



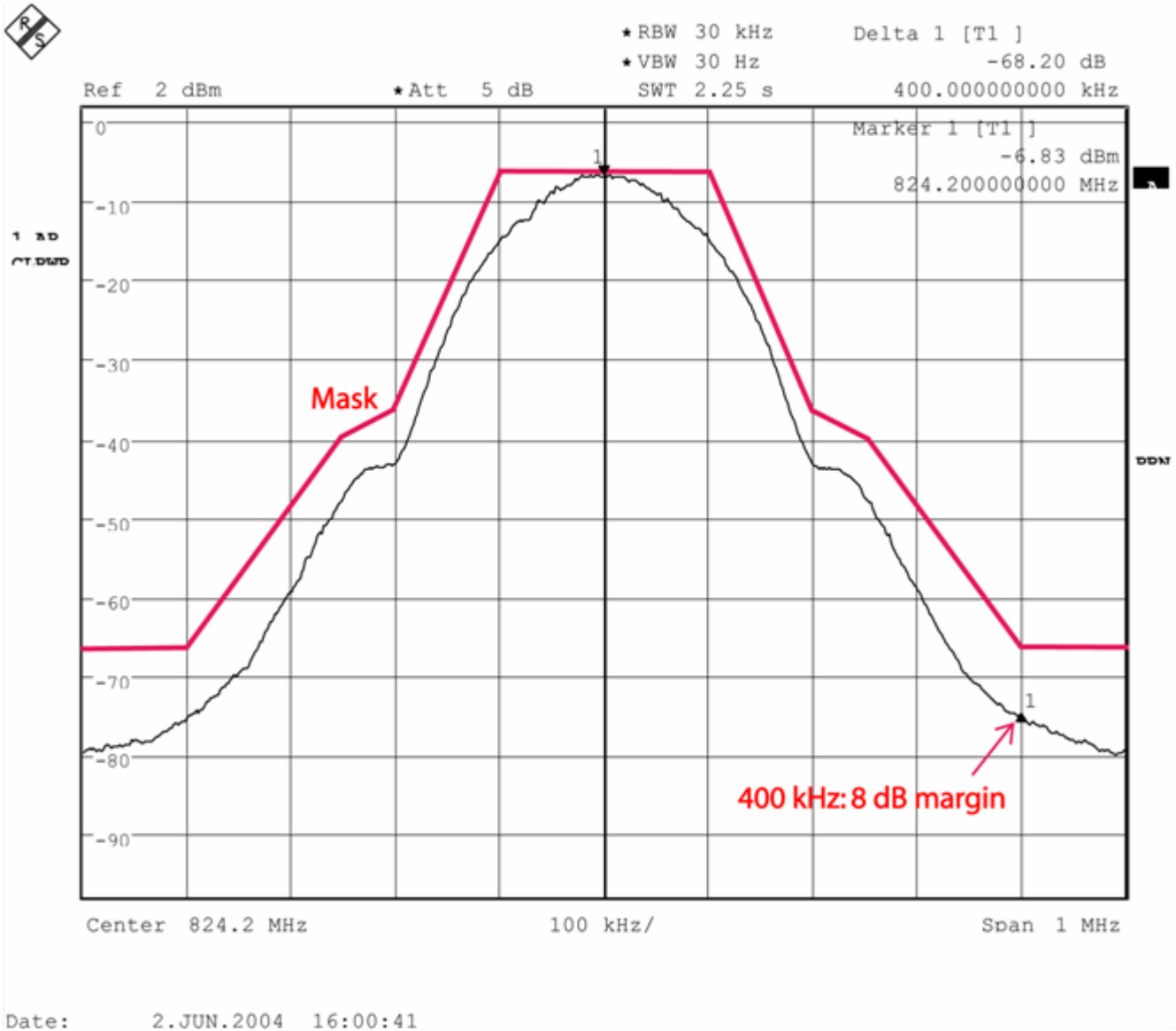
Just-in-time DCO Gain Estimation



- Forces Δf through the PLL
- Measures steady-state ΔOTW
- Could be repeated a few times for better estimation

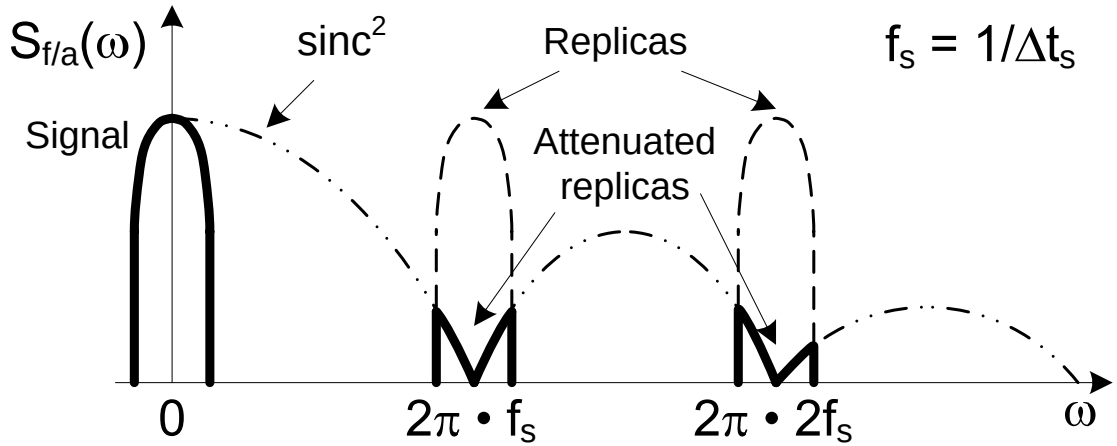
Measured GSM Output Spectrum

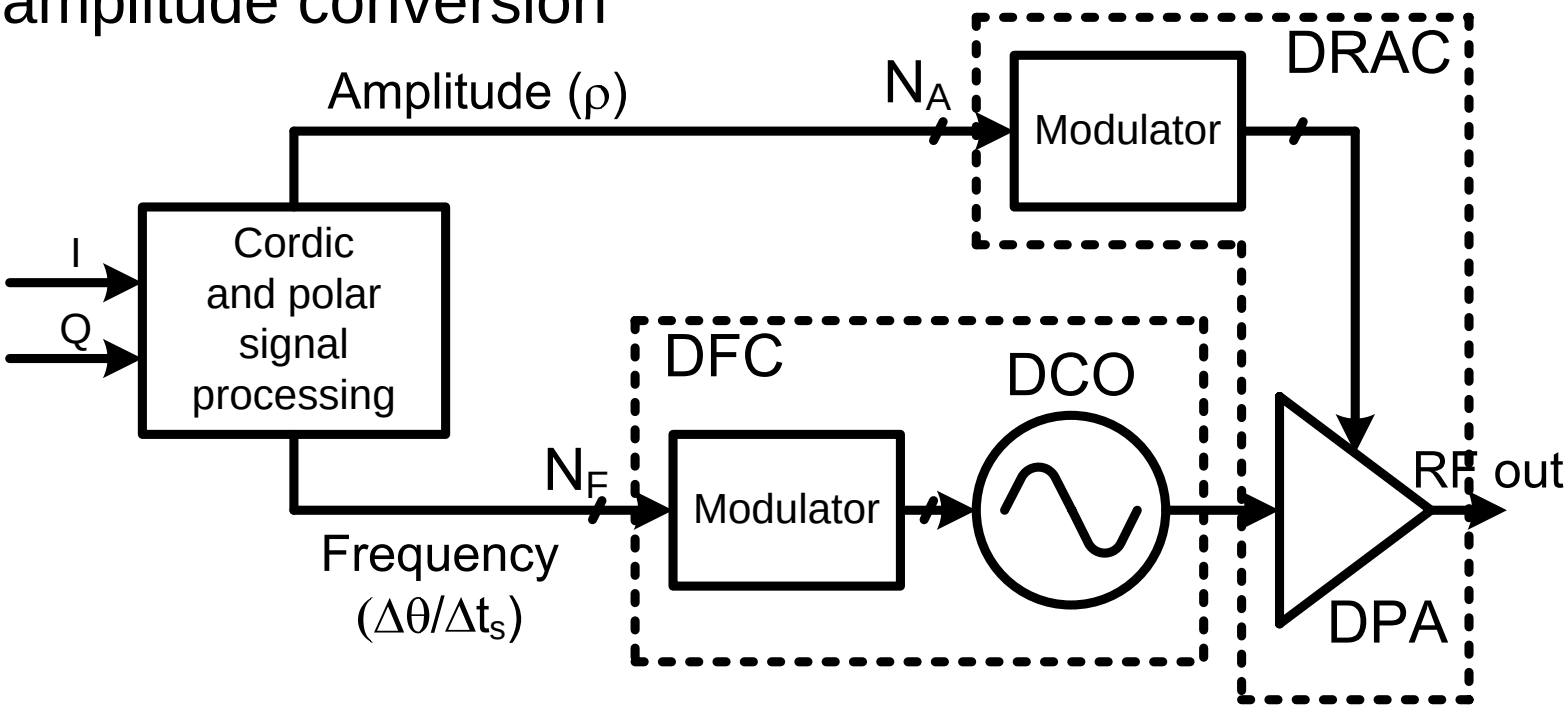
- Meets GSM spec
  - 8 dB margin @ 400 kHz
- Phase error
  - 1º rms (5º spec)
  - 3º peak (20º spec)



All-Digital Polar TX Architecture

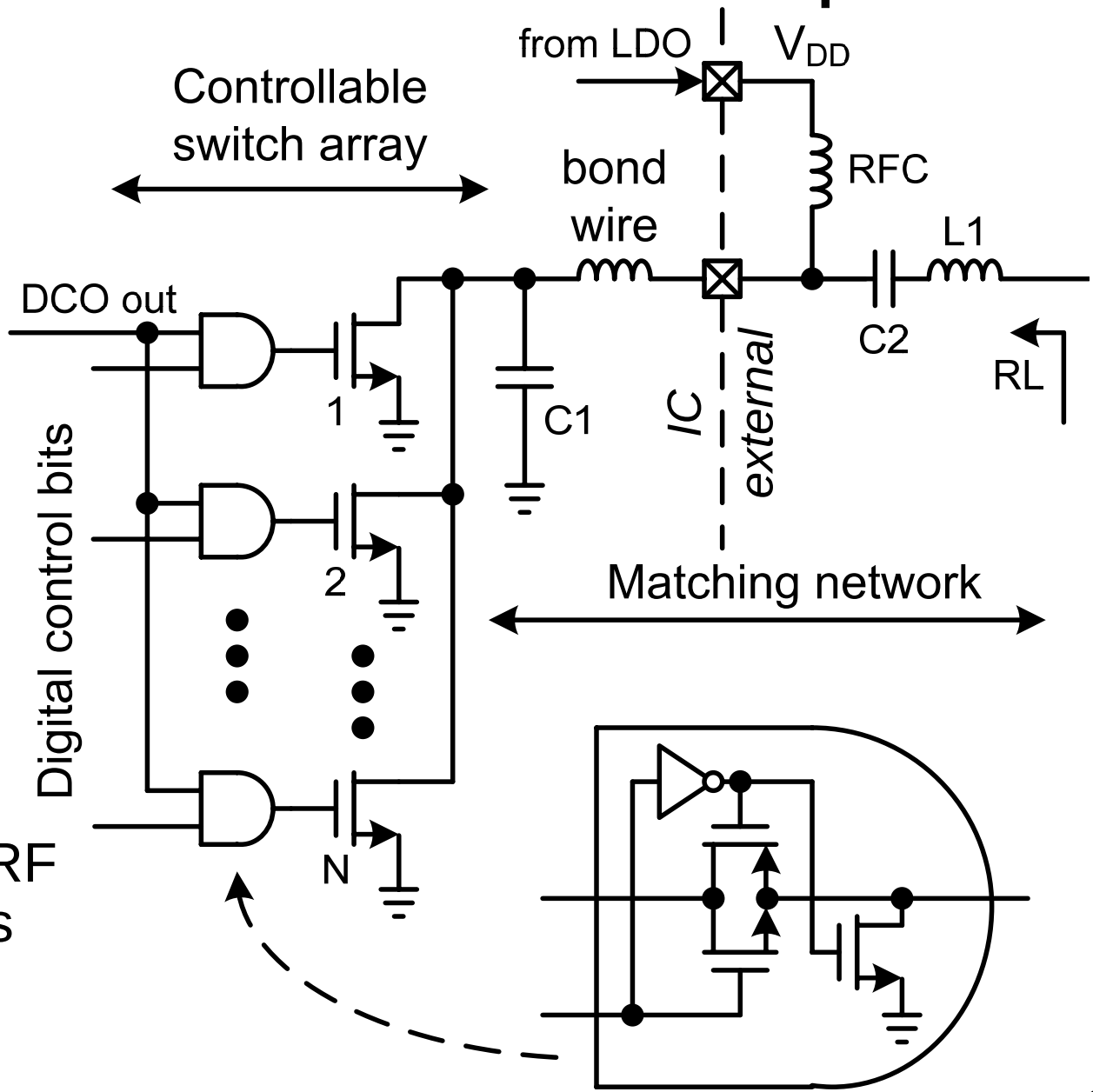
- Dense logic for digital signal processing
- DCO for digital-to-frequency conversion
- DPA for digital-to-RF-amplitude conversion



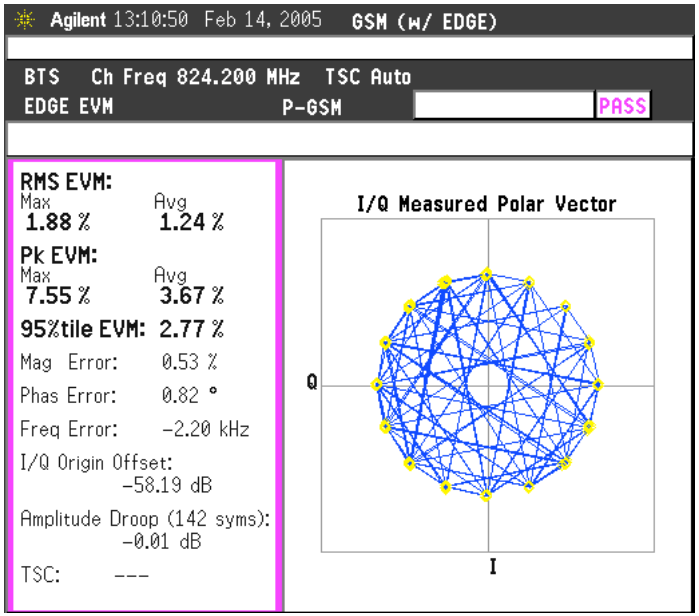


Digitally-Controlled Power Amplifier

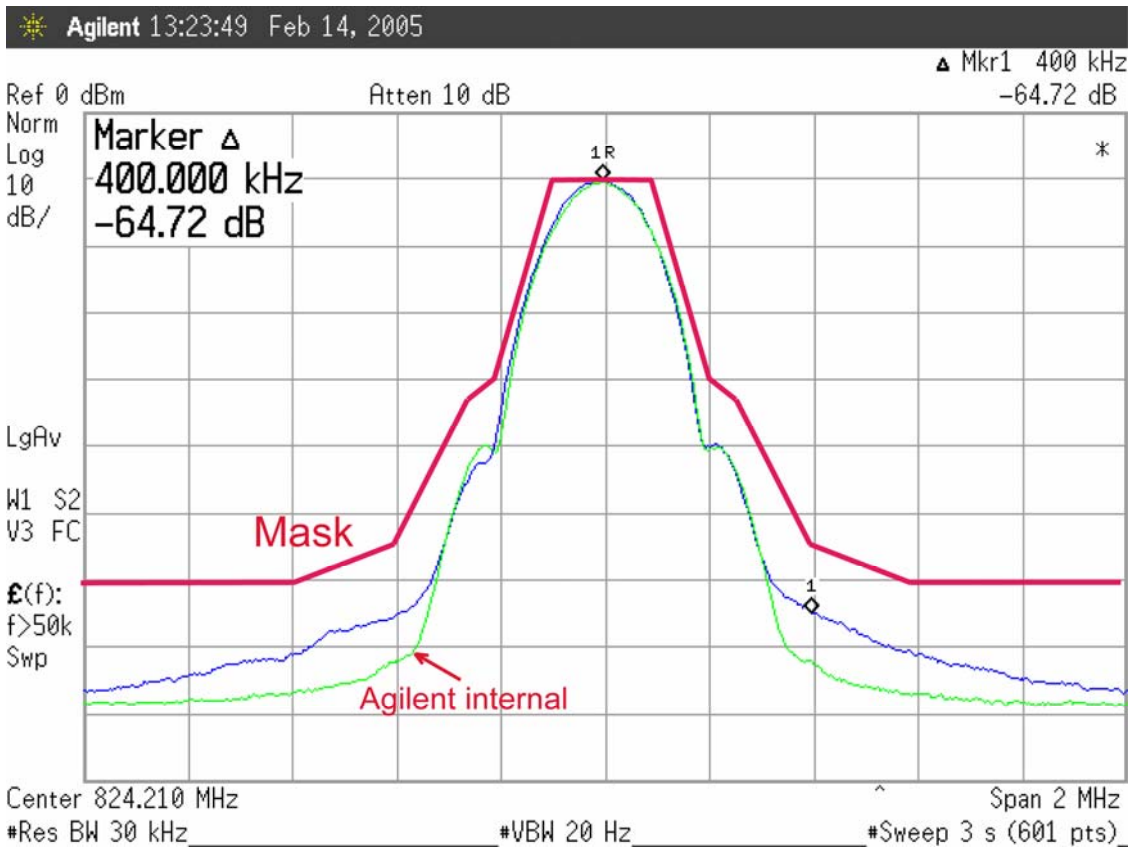
- Array of unit-weighted MOS switches
- Each switch contributes a conductance
- Near class-E operation
- Fine amplitude through ΣΔ modulation
- The DPA can be thought of as an RF DAC, where “A” is RF “amplitude”



Measured EDGE Modulation



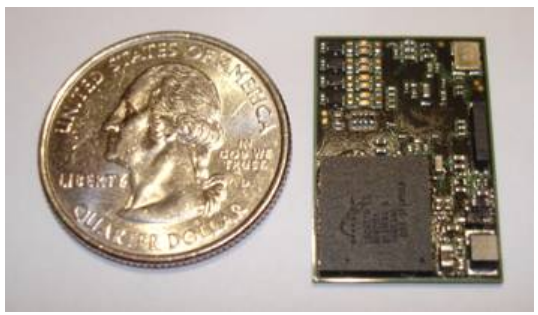
- Meets the spectral mask with 10 dB margin



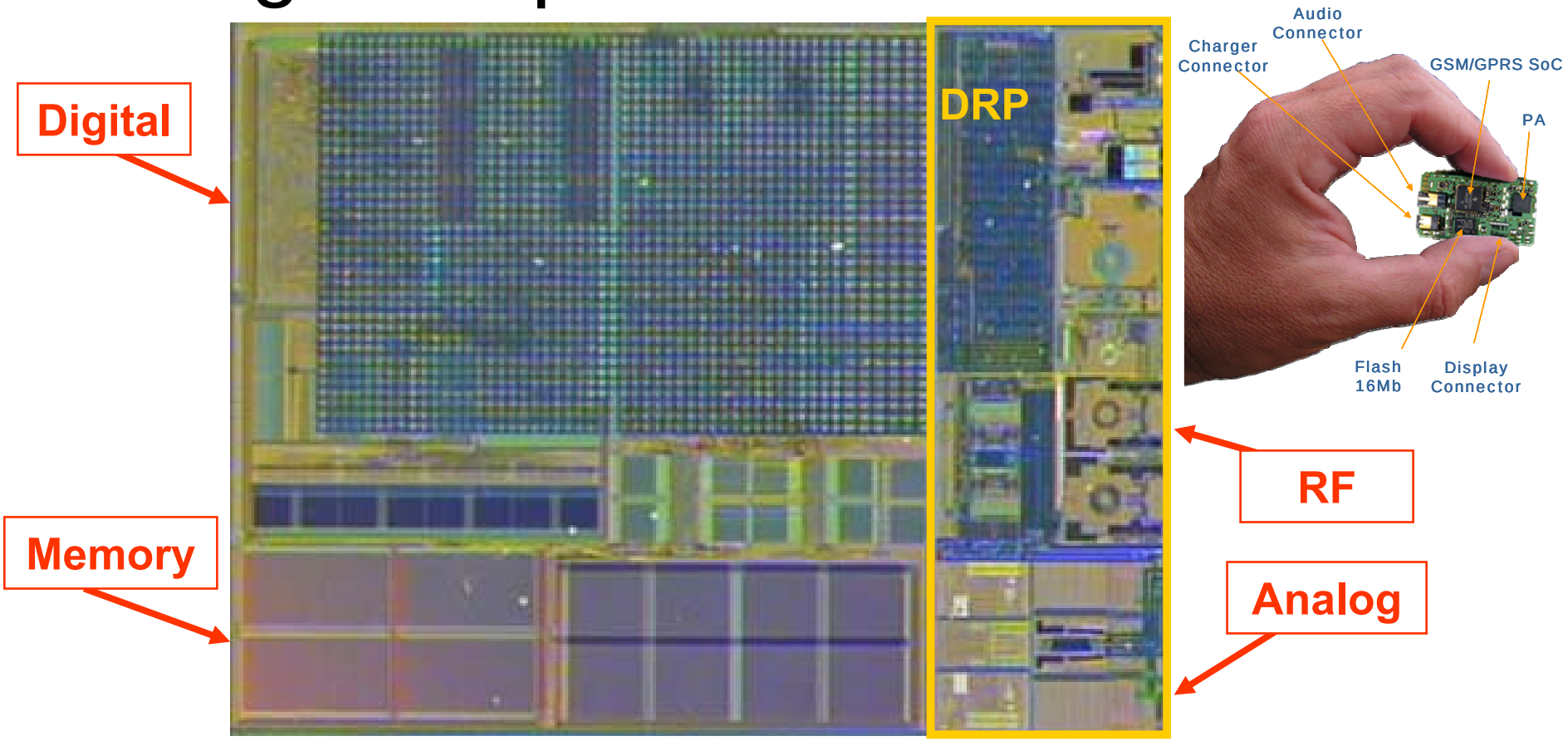
- 1.24% meets the rms EVM spec of 9%
- 3.67% meets the peak EVM spec of 30%

Single-Chip GSM Radio in 90 nm

- 90 nm CMOS
- All-digital PLL
- All-digital TX
- Digitally-intensive RX
- w/o
  - 2-W PA
  - Battery management



Single-Chip GSM Radio in 90 nm



- First single-chip GSM radio
- In volume production
- Logic density of 250 kgates/mm^2
- SRAM density of 1 Mbits/mm^2

Conclusions

- Survey of RF wireless frequency synthesizers
- Highly-scaled CMOS is extremely unfriendly for RF and analog designs
- Radio architecture must transform voltage-domain circuits into time-domain operation and high-speed digital logic
- All-digital PLL (ADPLL)
  - ADPLL features wideband frequency modulation
- All-digital and digitally-intensive architecture in nanometer CMOS can replace traditional RF circuits
- Performance demonstrated in a commercial single-chip GSM radio

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