Dallas IEEE CAS Seminar:

# Digital RF Processor (DRP™) for Cellular Phones

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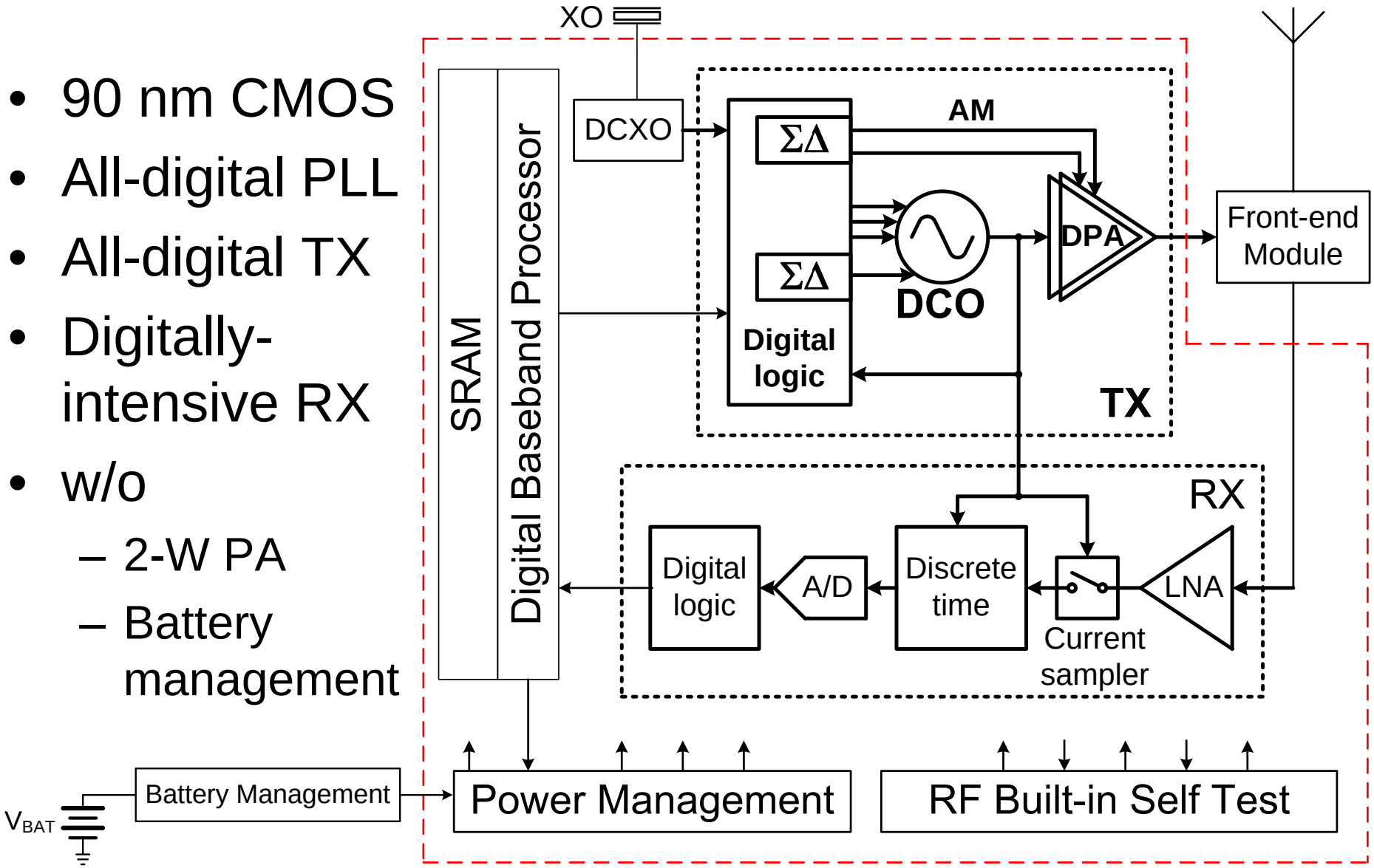
Texas Instruments

# “Big Picture”: Single-Chip Cell Phone

- 90 nm CMOS
- All-digital PLL
- All-digital TX
- Digitally-intensive RX
- w/o
  - 2-W PA
  - Battery management

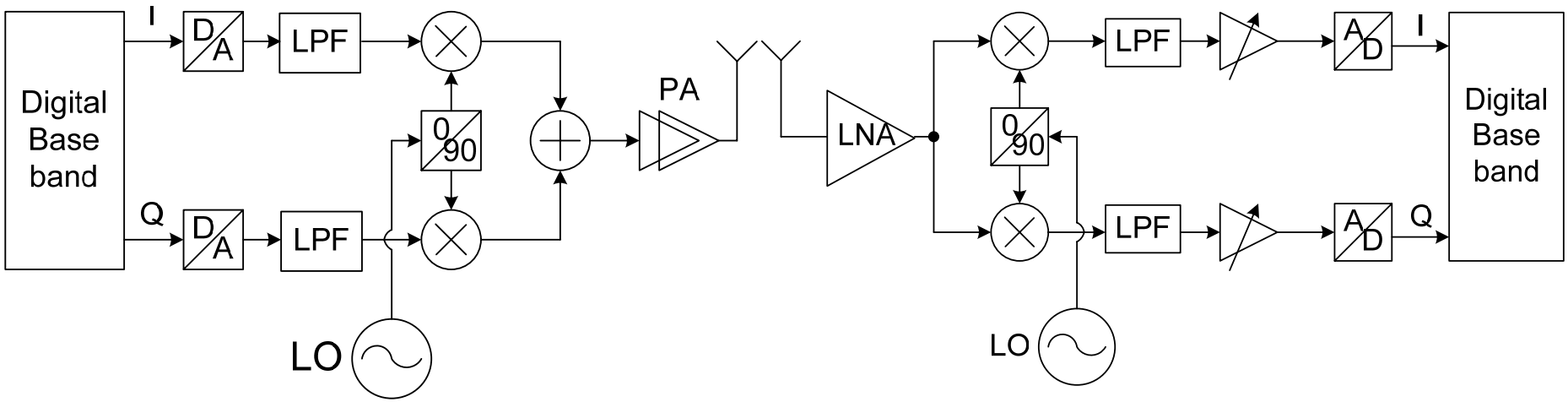


# Outline

- Motivation
- New paradigm in deep-submicron CMOS
- All-digital PLL (ADPLL)-based transmitter
- Direct sampling receiver
- VHDL top-level modeling and simulation
- Implementation
- Conclusion

# Motivation

- RF transmitters in commercial wireless applications are traditionally based on charge-pump PLL's and IQ upconversion mixers
- RF receivers use continuous-time mixing, filtering and amplification
- Design flow and circuit techniques are analog intensive
- Technology incompatible with modern digital processors
  - Low-voltage deep-submicron CMOS

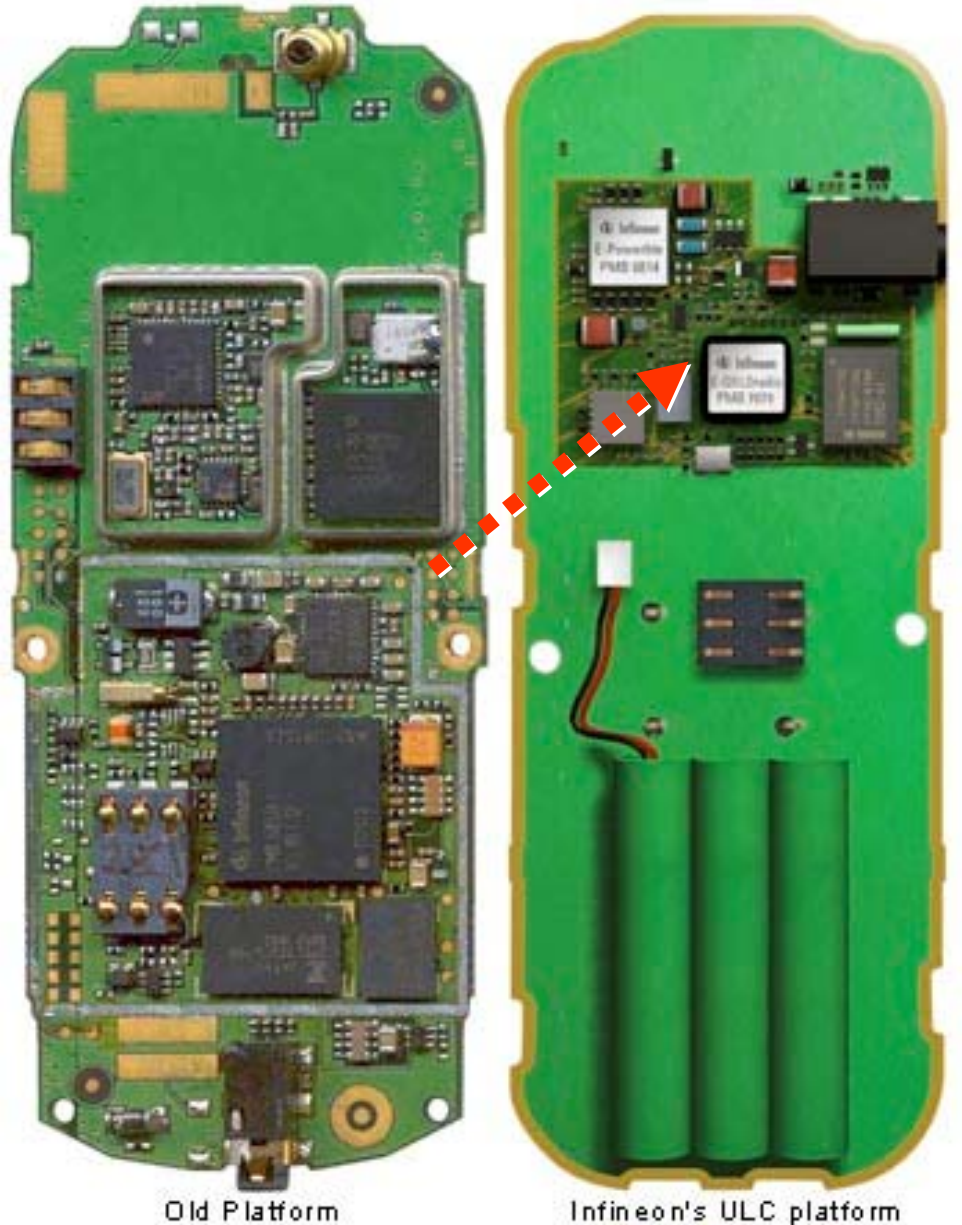


# Motivation

- Aggressive cost and power reductions of mass-produced mobile wireless terminals require the highest level (i.e., single chip) of integration
  - Digitally-intensive approach to conventional RF and analog functions
- RF/analog is typically 20% of SoC area
  - Rest is digital logic and memory
- Migration to the most aggressive CMOS is a must for digital baseband and application processor
- Area or cost of digital logic in 90-nm CMOS is almost half of that in 130-nm CMOS

# Why Single-Chip Radio?

- Not a fad
  - First TI, then Infineon, then SiLab
- <$20 phones
- Large untapped market in India and China
- More “real estate” space for advanced features
- Better reliability
  - Today, more than half of the total components on a board are analog RF components
- Longer talk time



# New Paradigm

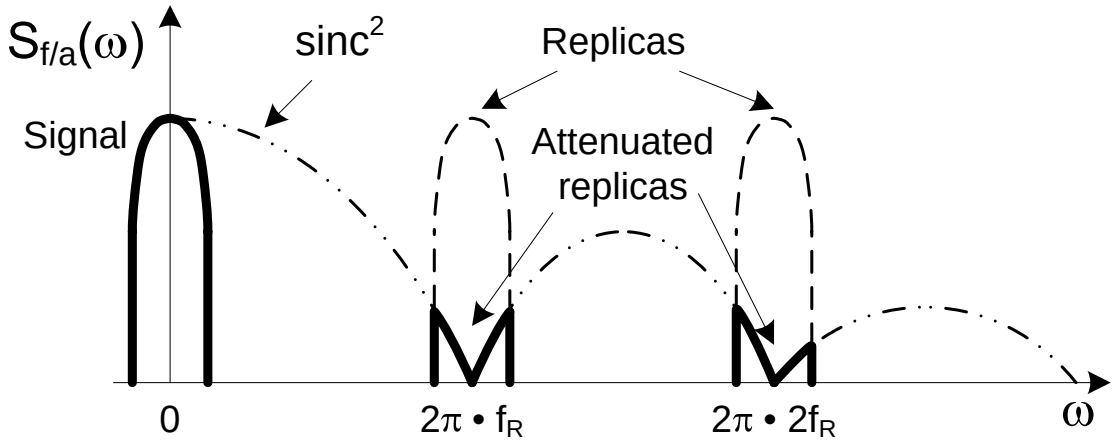
In a deep-submicron CMOS process, time-domain resolution of a digital signal edge transition is superior to voltage resolution of an analog signal

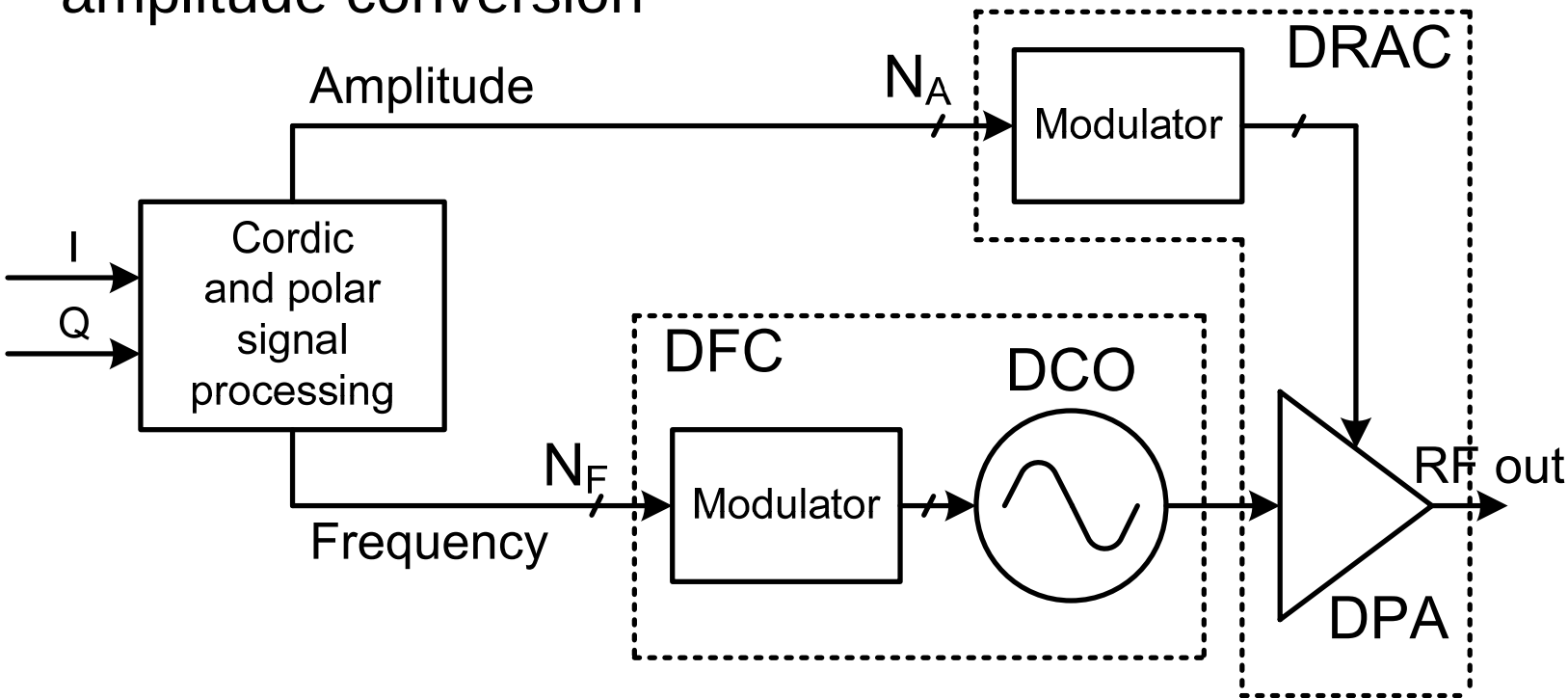
# Deep-Submicron CMOS Rules

- Exploit:
  - Fast switching characteristics of MOS transistors
  - Small device geometries and precise device matching
  - High density of digital logic: 250 kgates/mm$^2$ in 90-nm CMOS
  - High density of SRAM memory: 1 Mbits / mm$^2$ in 90-nm CMOS
- Avoid:
  - Biasing currents for analog circuits
  - Reliance on voltage resolution
  - Nonstandard devices not needed for memory and digital logic

# All-Digital Polar TX Architecture

- Logic for digital signal processing
- DCO for digital-to-frequency conversion
- DPA for digital-to-RF-amplitude conversion



# Digitally-Controlled Oscillator (DCO)

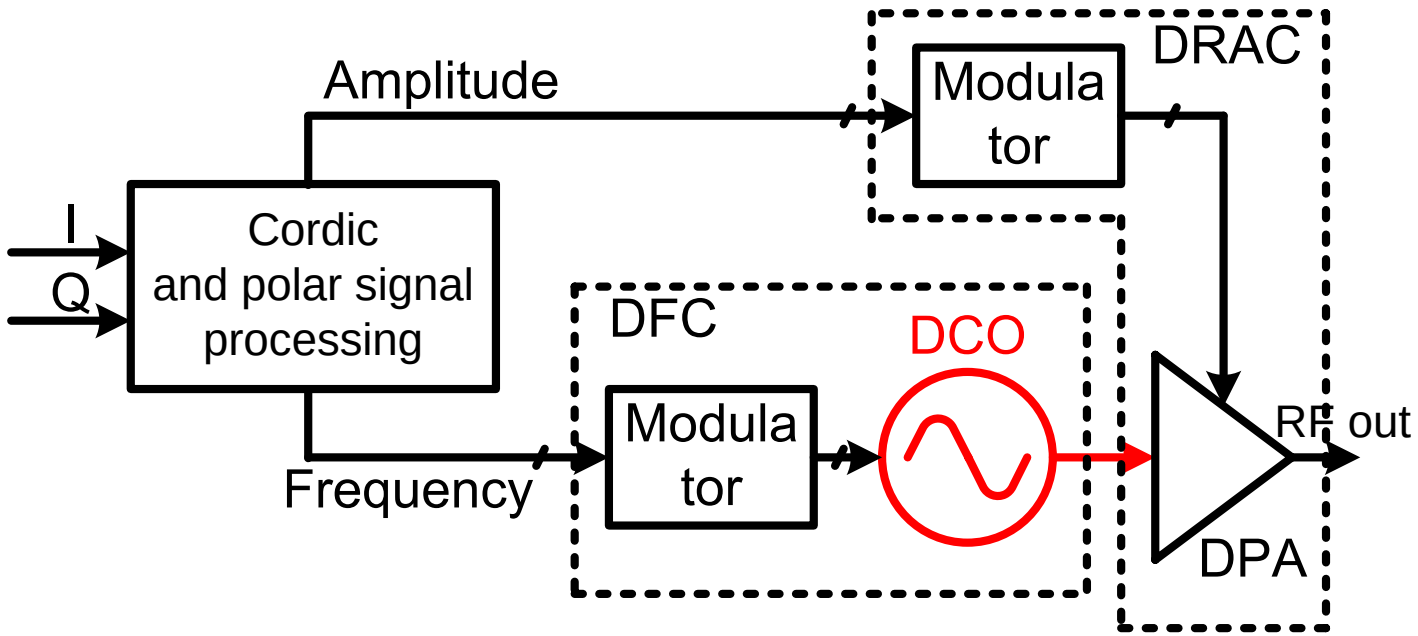
Digitally-Controlled Pre Power Amplifier (DPA)

Generic Modulator

Digital-to-Frequency Converter (DFC)

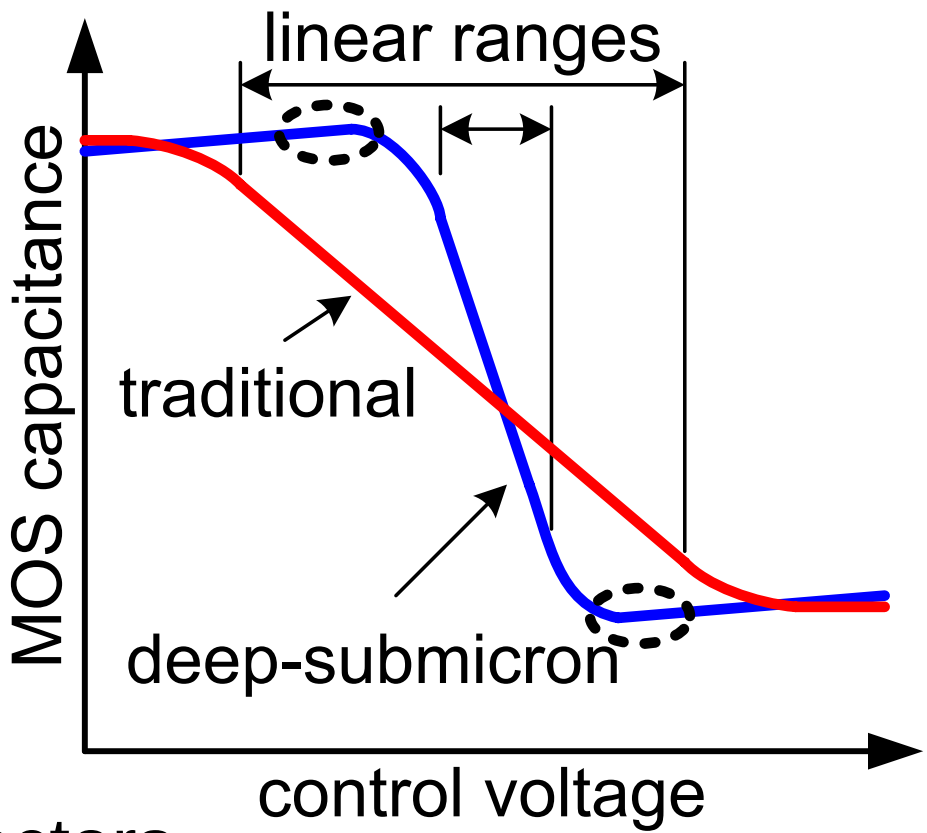
Digital-to-RF-Amplitude Converter (DRAC)

Polar Transmitter



# MOS Varactor

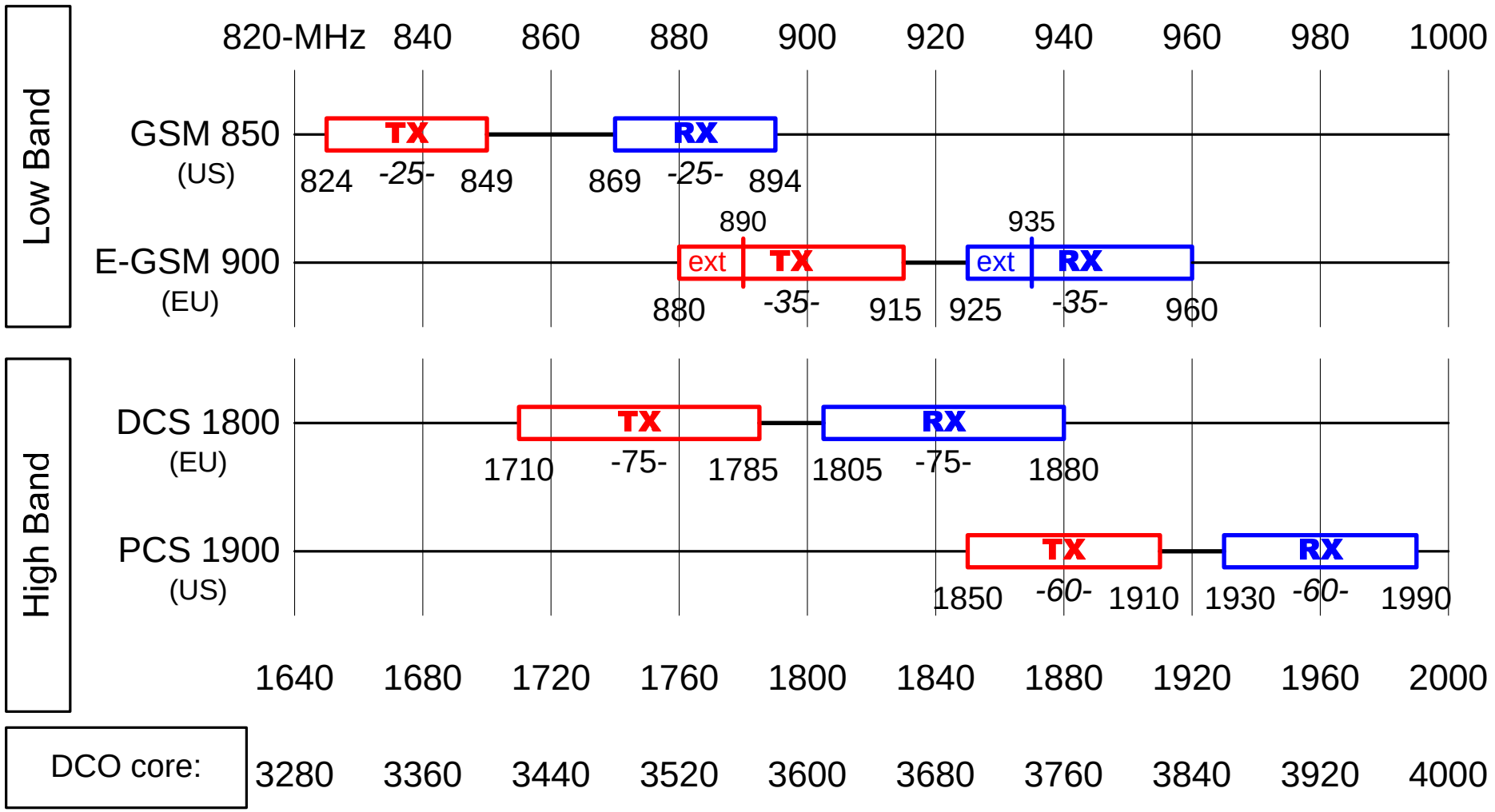
- Only simplest varactors in the digital CMOS
- Perceived poor quality of varactors in a deep-submicron CMOS for conventional VCO's




- Conventional CMOS varactors
  - Large linear range for precise and wide frequency control
- Deep-submicron CMOS varactor
  - Linear range is compressed with high noise sensitivity

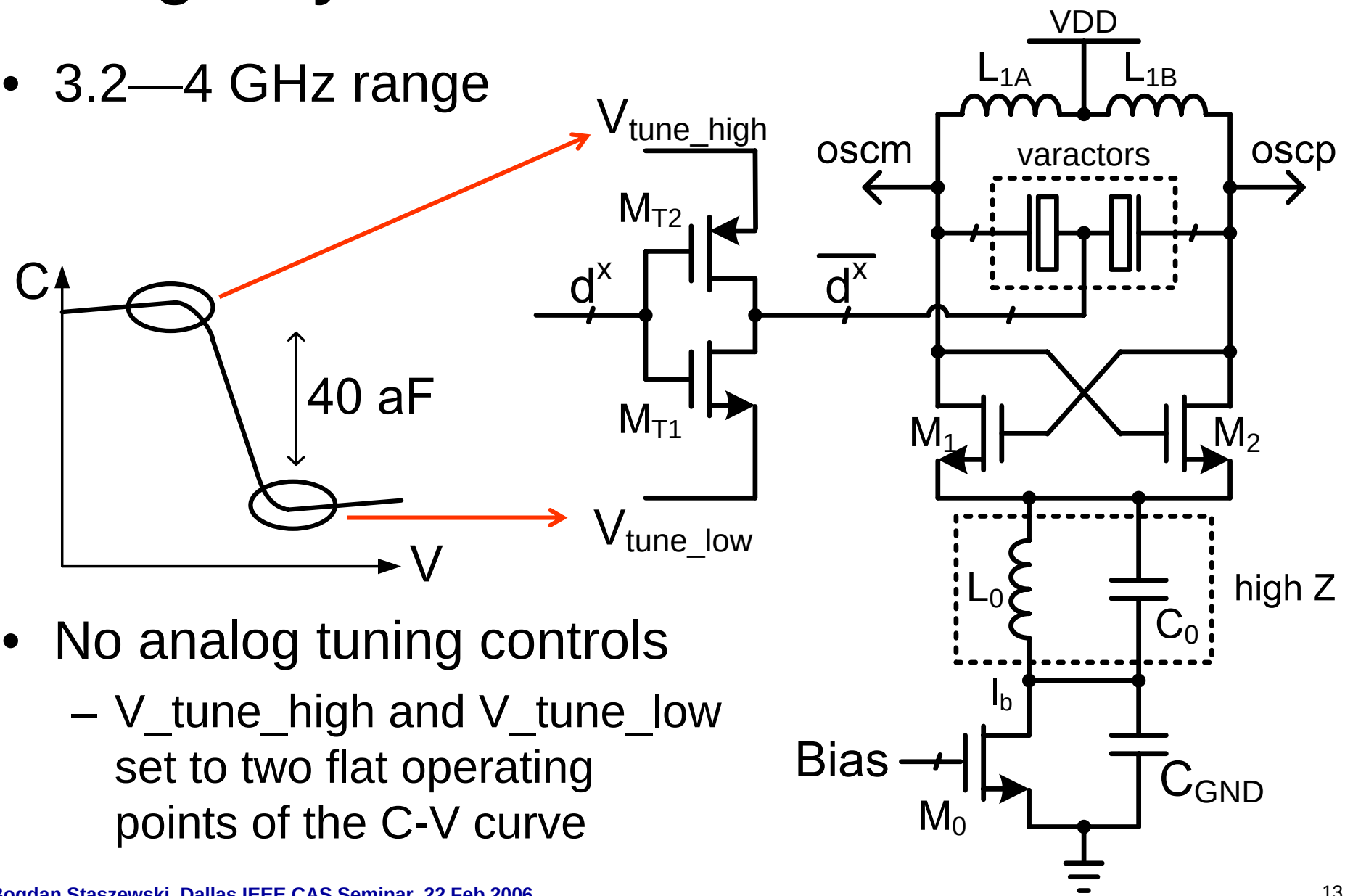
# GSM Bands

- Single oscillator covers all four bands



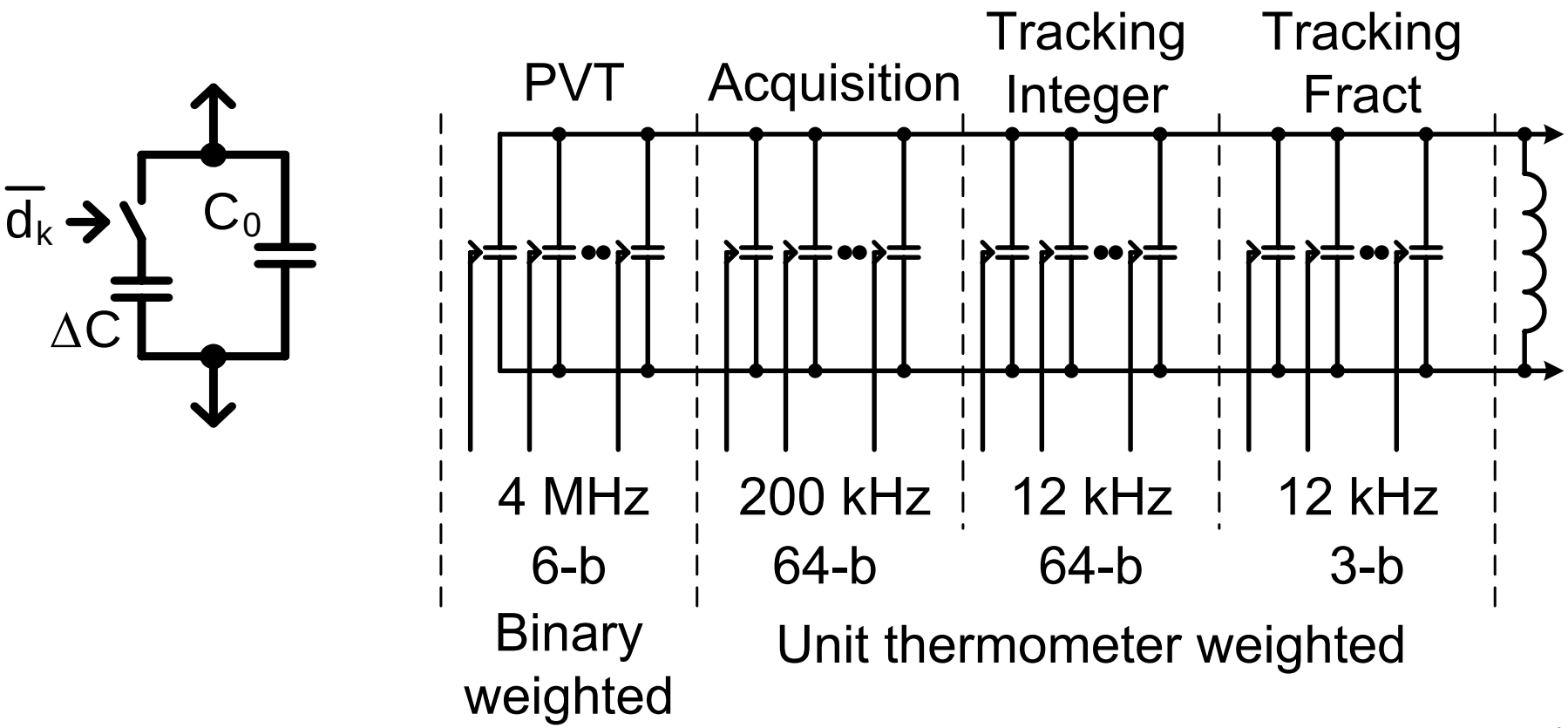
# Digitally-Controlled Oscillator Core

- 3.2—4 GHz range
- No analog tuning controls
  - V_tune_high and V_tune_low set to two flat operating points of the C-V curve

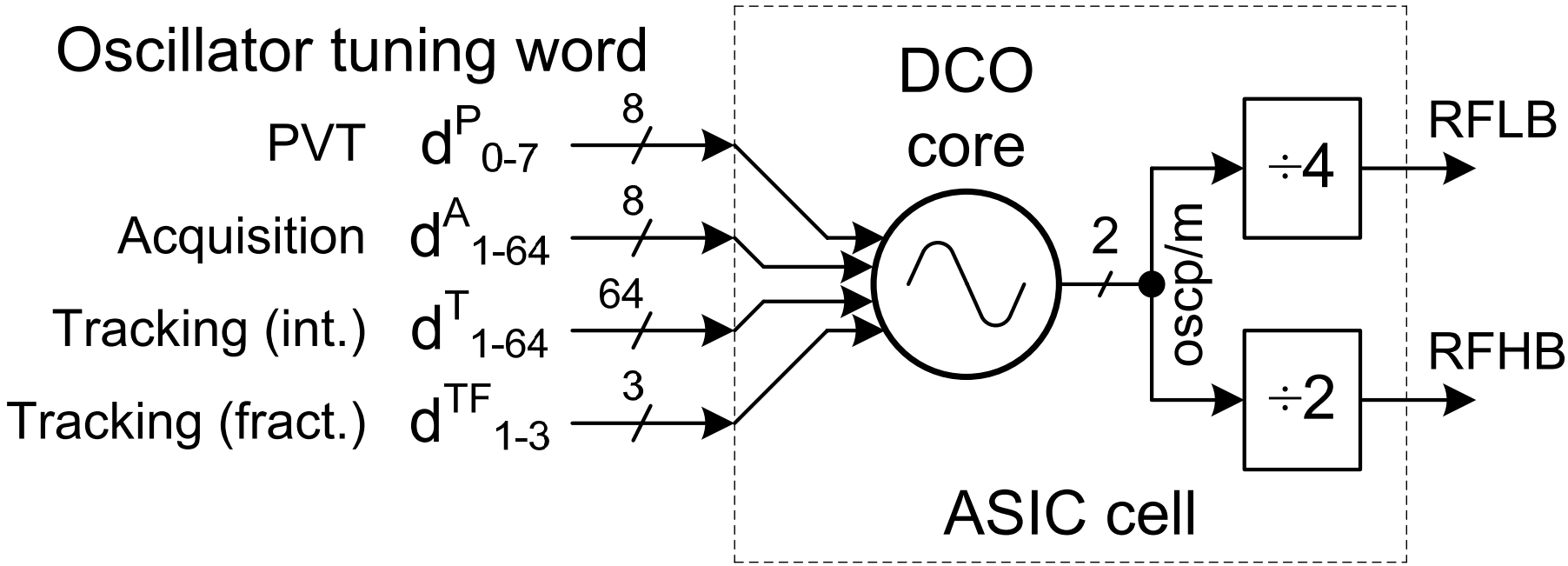


# DCO Varactor Functional Banks

- Process/voltage/temperature (PVT) calibration mode
- Acquisition mode (during channel select)
- Tracking mode (during the actual TX and RX)
  - Dithering to improve resolution



# DCO ASIC Cell




- Truly digital I/O's even at 1.8 GHz output – $t_r$<50 ps
- DCO built as a digital ASIC cell despite analog underlying internals
- DCO analog nature does not propagate
- Circuitry around it can be digital

Digitally-Controlled Oscillator (DCO)

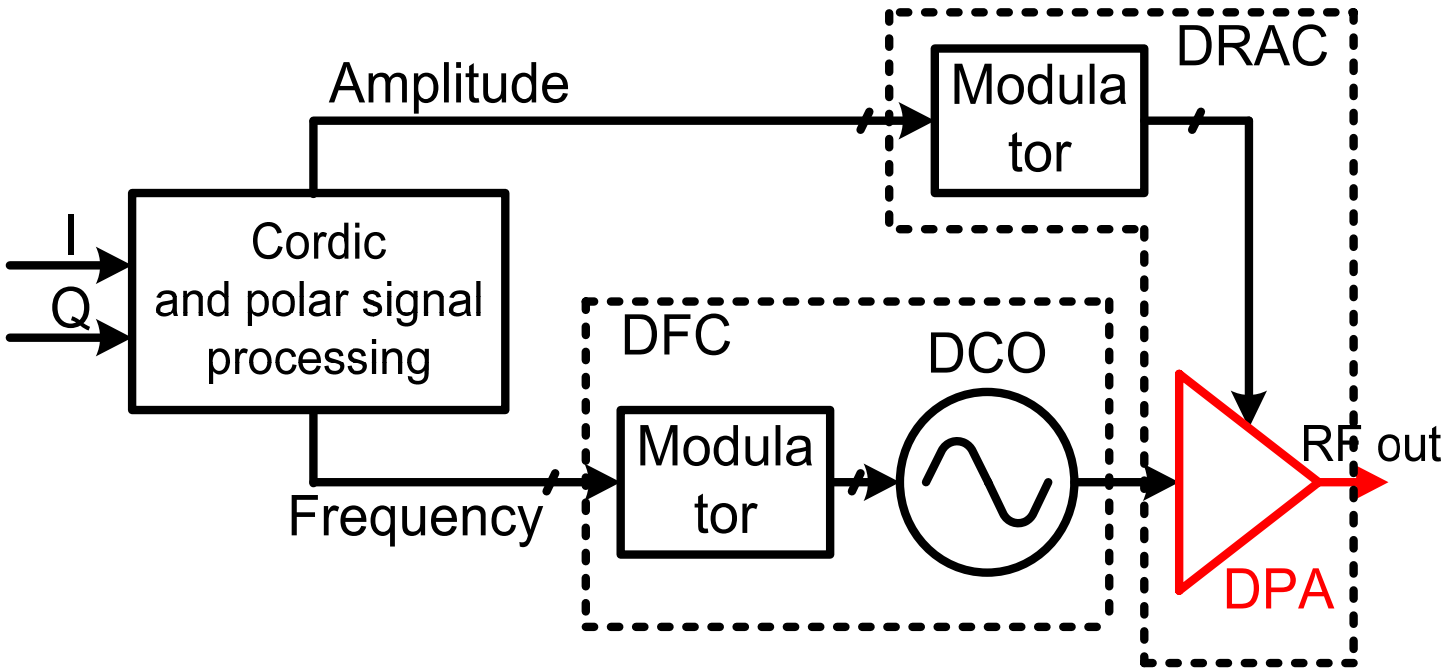
**Digitally-Controlled Pre-PA (DPA)**

Generic Modulator

Digital-to-Frequency Converter (DFC)

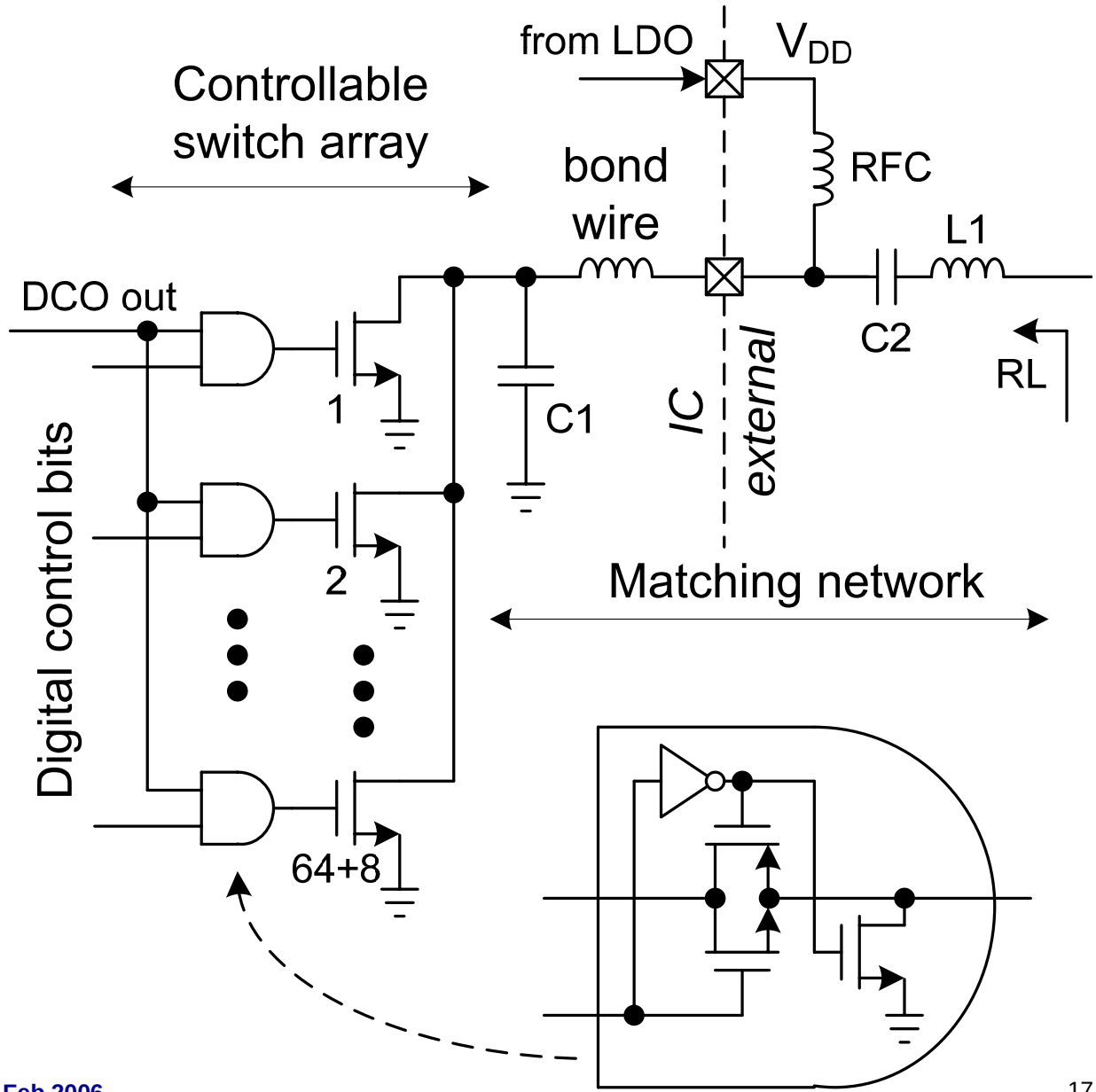
Digital-to-RF-Amplitude Converter (DRAC)

Polar Transmitter



# Digitally-Controlled Pre Power Amplifier

- Array of unit-weighted MOS switches
  - 64 transistors: 6-bit raw resolution
  - 8 transistors: high-speed ΣΔ dithering



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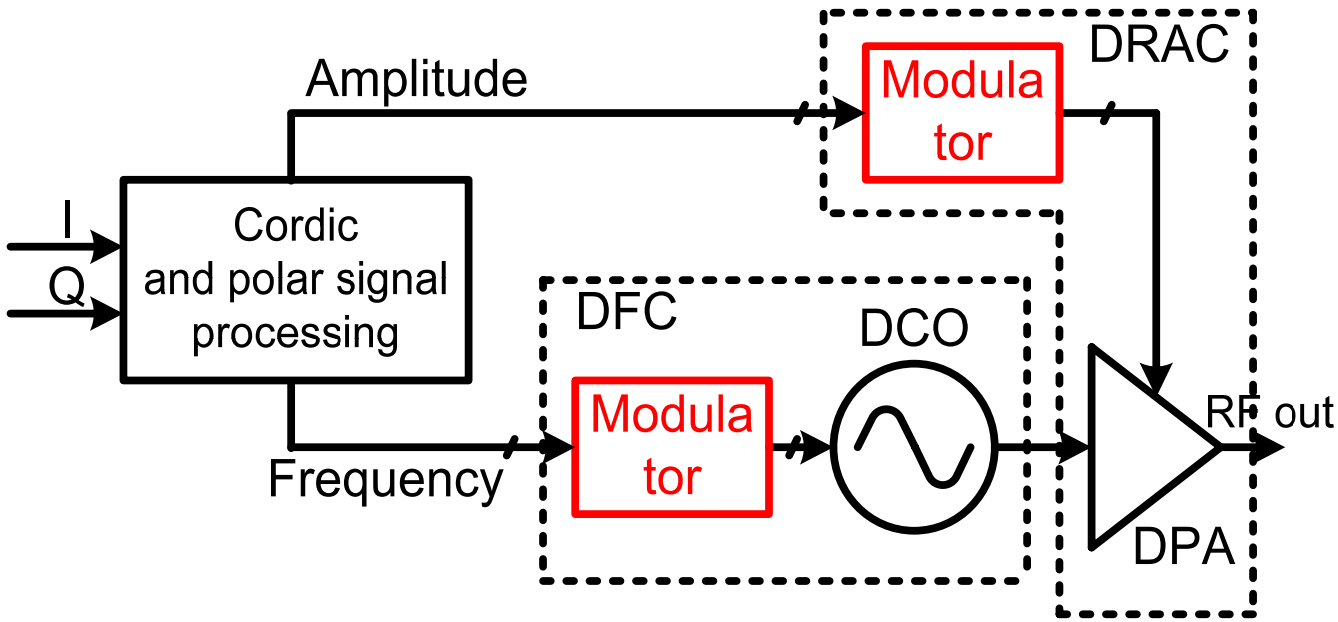
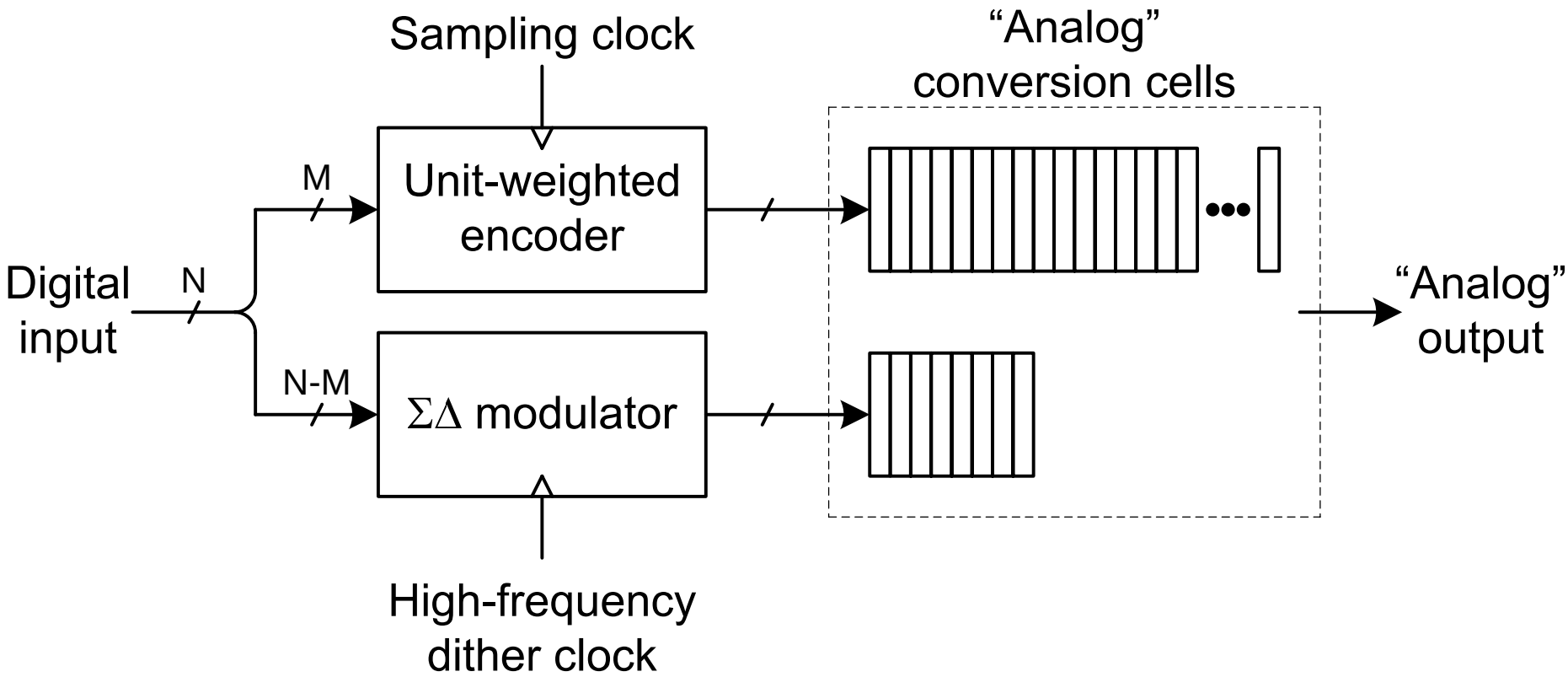


# Generic Digital Modulator

- Generic DAC: either DFC or DRAC
- Unit-weighted conversion cells
- Integer and fractional arrays



Digitally-Controlled Oscillator (DCO)
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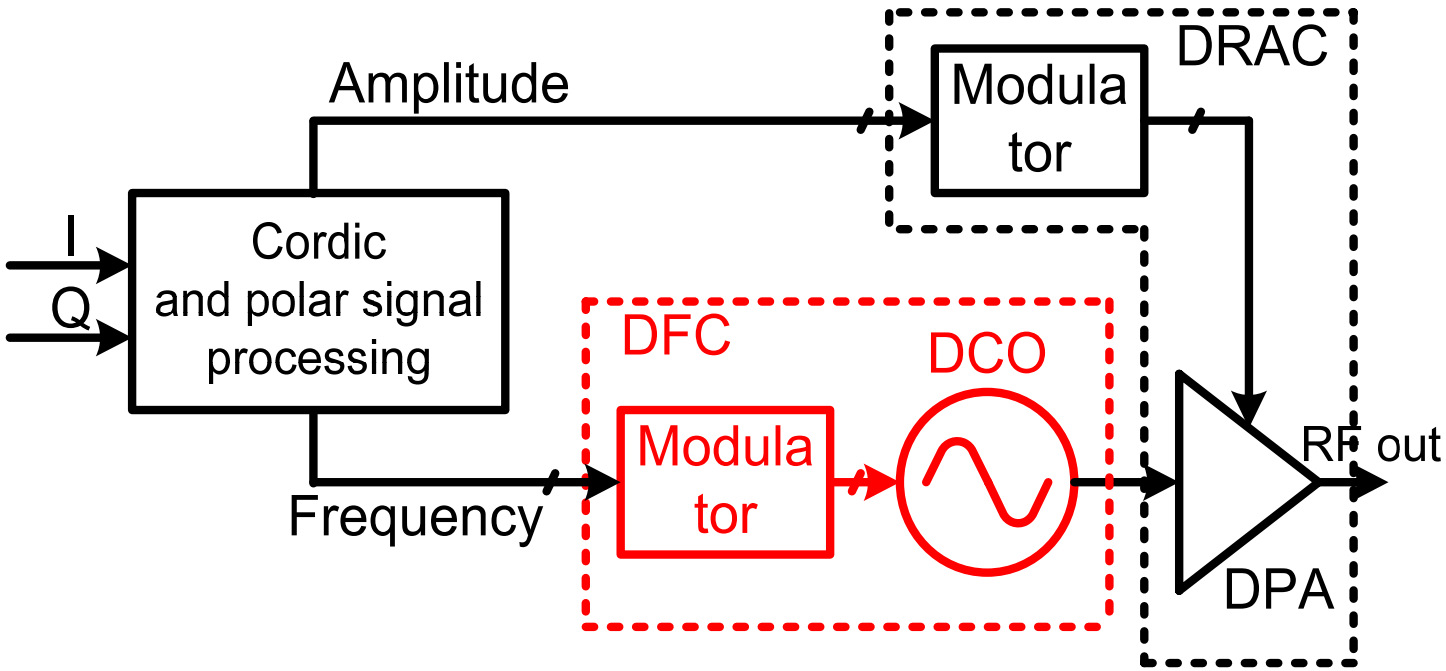
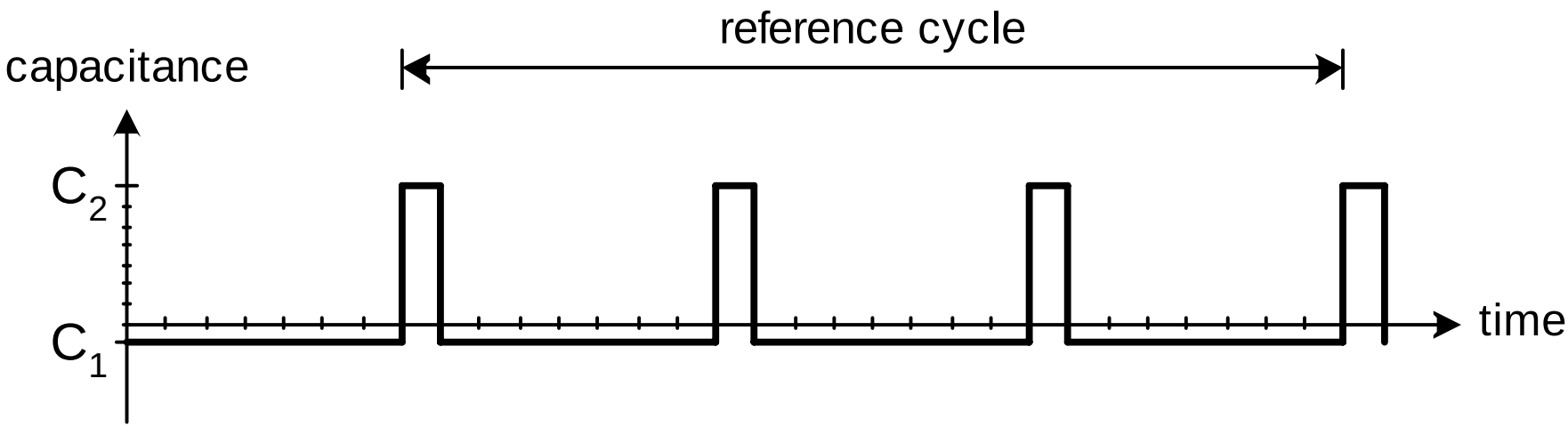


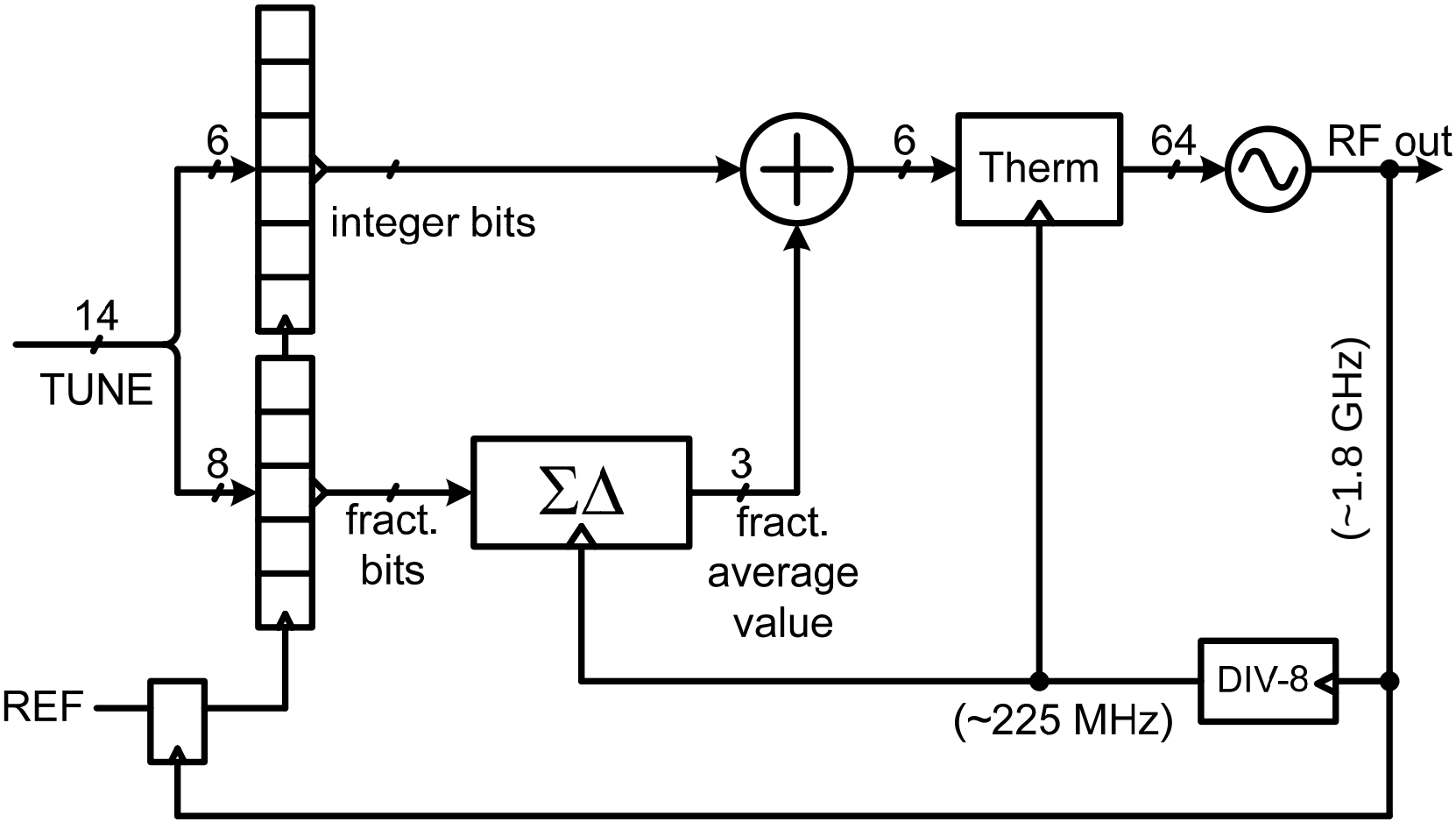
# Varactor Dithering

- Frequency resolution enhanced by high-speed dithering of the finest varactors
- Produces spurious tone at the oscillator output with power inversely proportional to the dithering speed
  - Spur power = -20 log($\beta$/2) [dBc], where $\beta$ is a dimensionless ratio of the peak frequency deviation to the modulating frequency



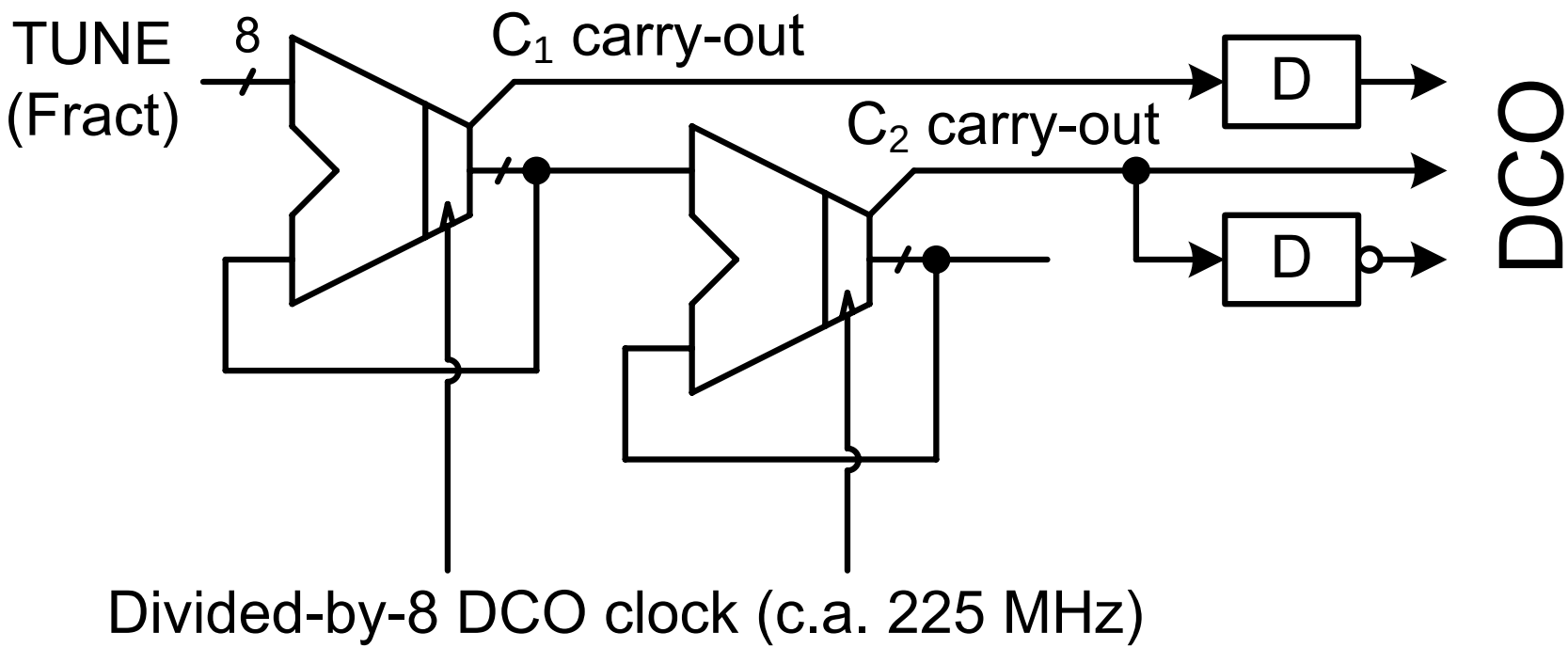
# Sigma-Delta DCO Dither

- Improves time-averaged DCO frequency resolution over the basic 12 kHz / LSB



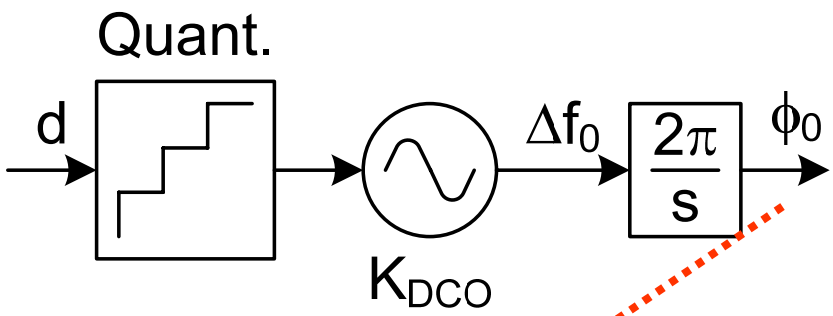
# Sigma-Delta Modulator

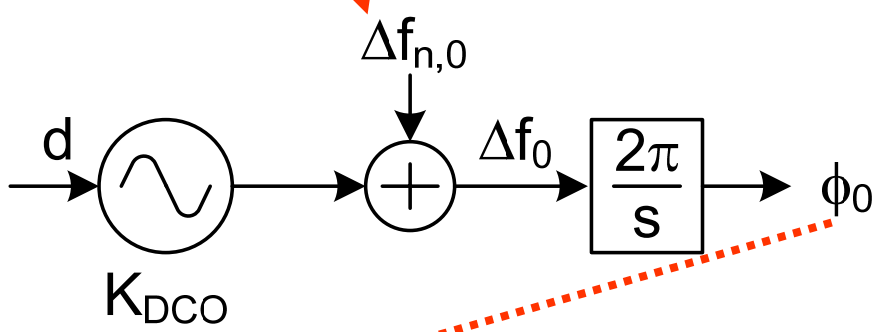
- 2nd order MASH structure
- Critical path retimed
- Addition of $\Sigma\Delta$ polynomial inside the DCO



# DCO Quantization Noise

$$\sigma_{\Delta f_0}^{\ 2} = \frac{\Delta f_{res}^{\ 2}}{12} \quad \Rightarrow \quad \frac{S_{\Delta f}}{2} = \frac{\sigma_{\Delta f_0}^{\ 2}}{f_R} = \frac{\Delta f_{res}^{\ 2}}{12 \cdot f_R}$$




- PN due to white dither

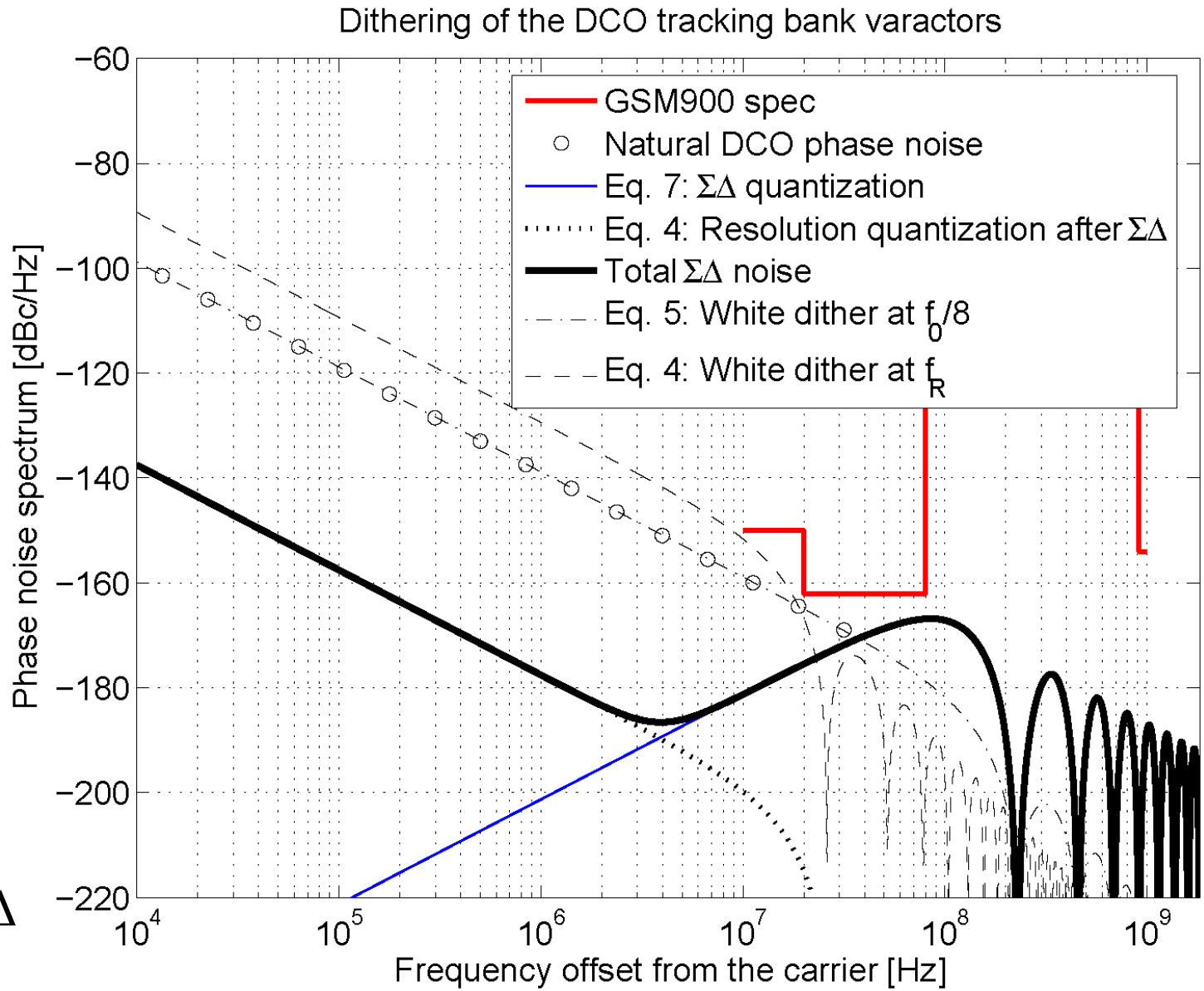
$$L(\Delta f) = \frac{1}{12}\left(\frac{\Delta f_{res}}{\Delta f}\right)^2 \frac{1}{f_{dith}}\left(\operatorname{sinc}\frac{\Delta f}{f_{dith}}\right)^2$$

- PN due to ΣΔ

$$L(\Delta f) = \frac{1}{12}\left(\frac{\Delta f_{res}}{\Delta f}\right)^2 \frac{1}{f_{dith}}\left(2\sin\frac{\pi\Delta f}{f_{dith}}\right)^{2n}$$

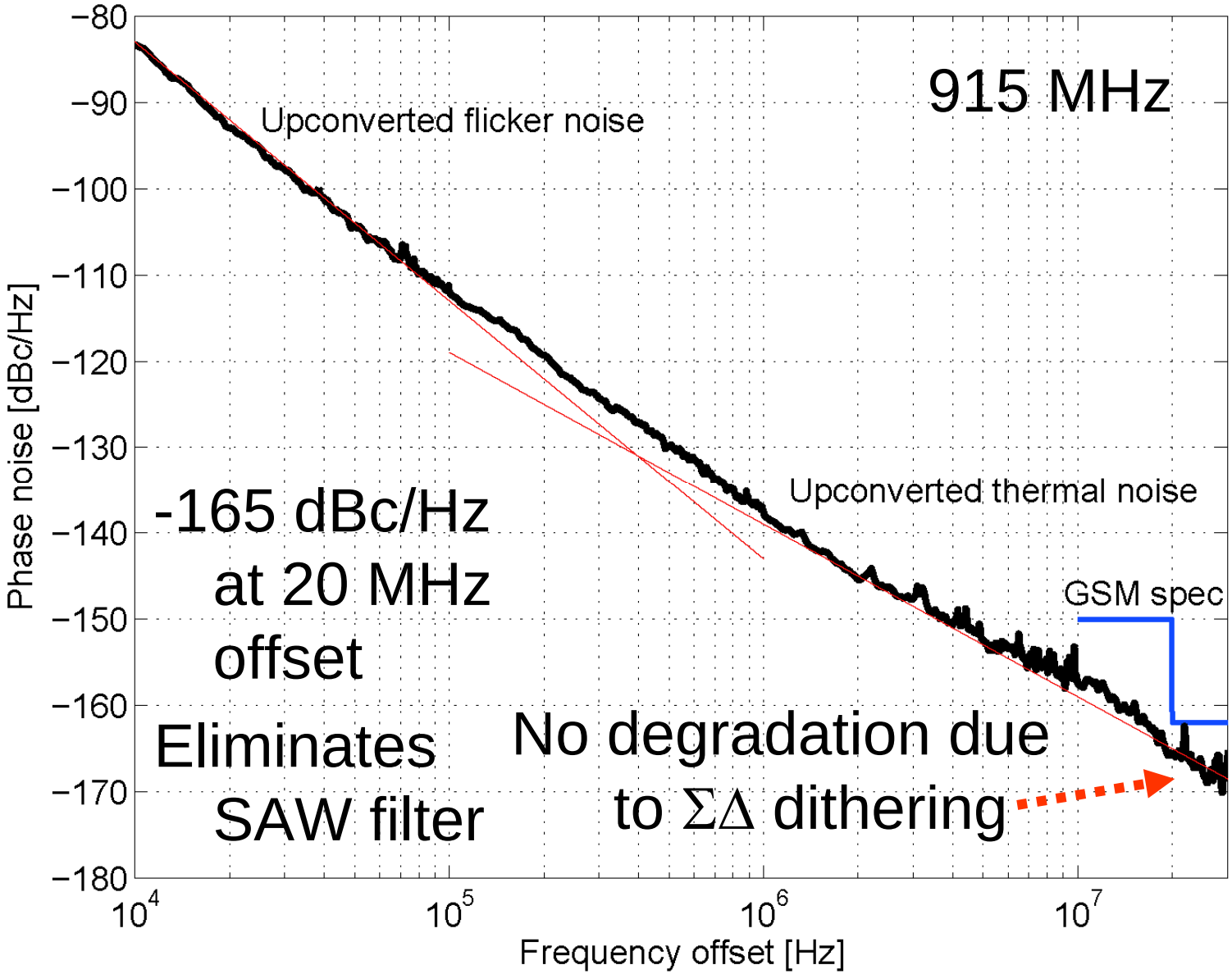
# Theoretical Phase Noise Spectra

[RFIC'05]



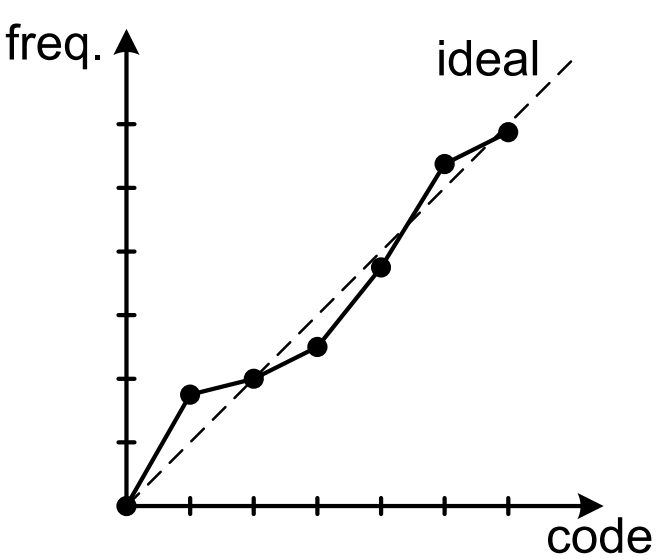

- $\Delta f$ = 12 kHz
- $f_{dith}$ = 225 MHz
- 2nd order ΣΔ

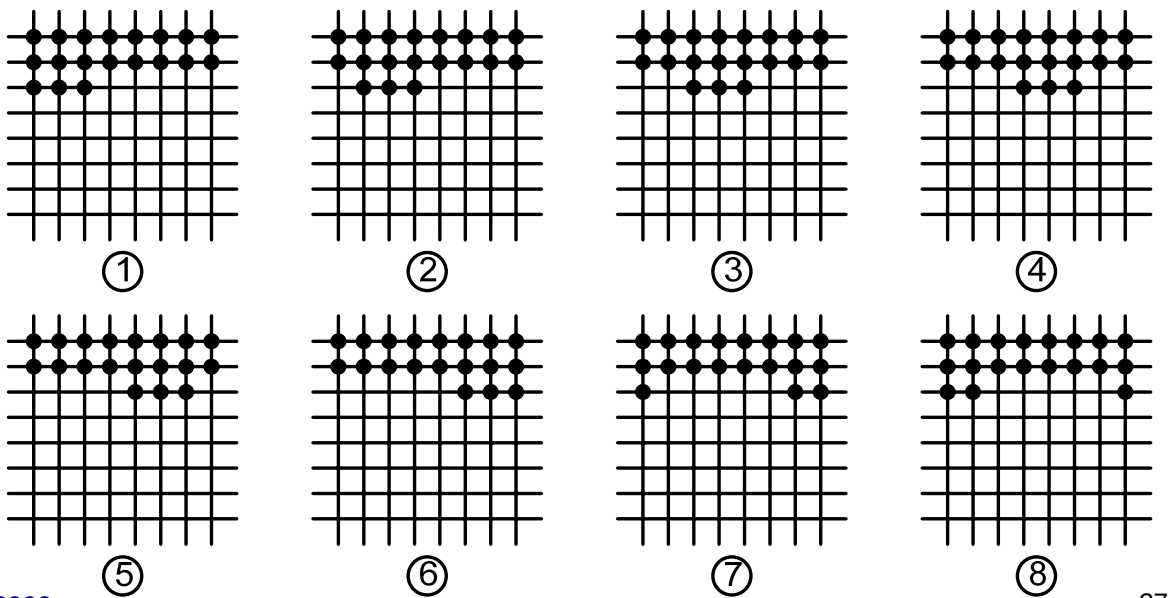
# Measured DCO Phase Noise



# Dynamic Element Matching

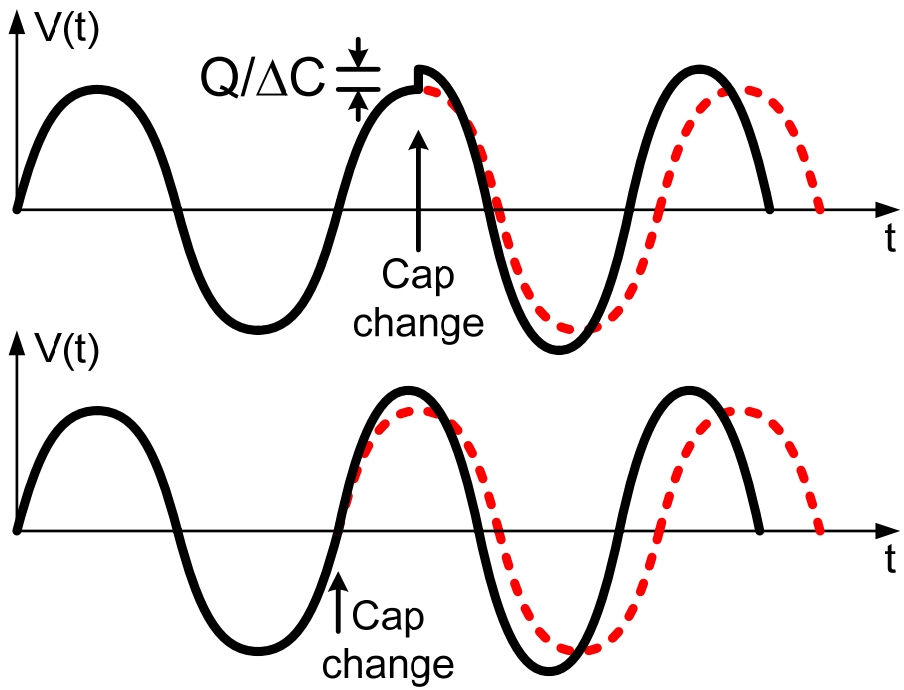
- Unit-weighted varactors have slightly different capacitative values
- As capacitors are turned on and off, non-linearities will be evident in the output
- Dynamic element matching (DEM) to improve digital-to-frequency conversion linearity



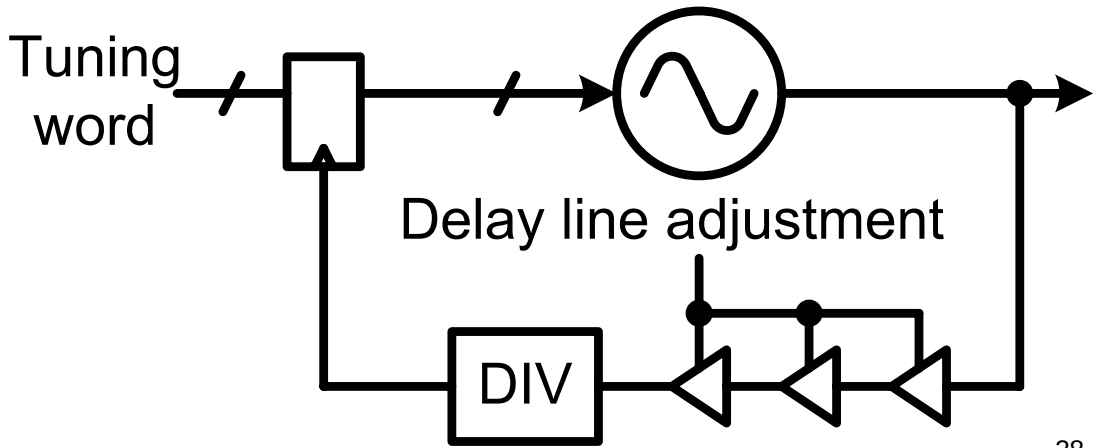



# Synchronously-Optimal Sampling

- DCO is a time-variant system
- Digital input controls the oscillating frequency by modifying the total capacitance




- Oscillator input word changes only at precise DCO state where it causes least amount of perturbations



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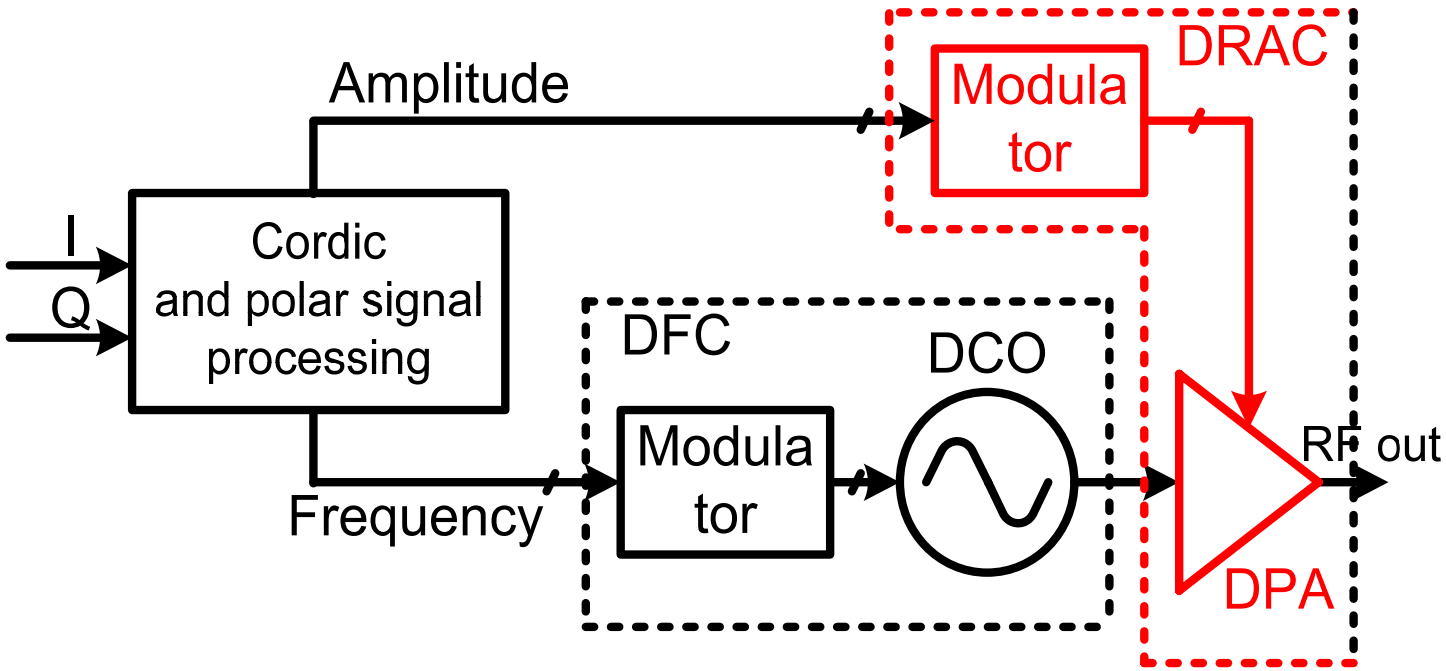
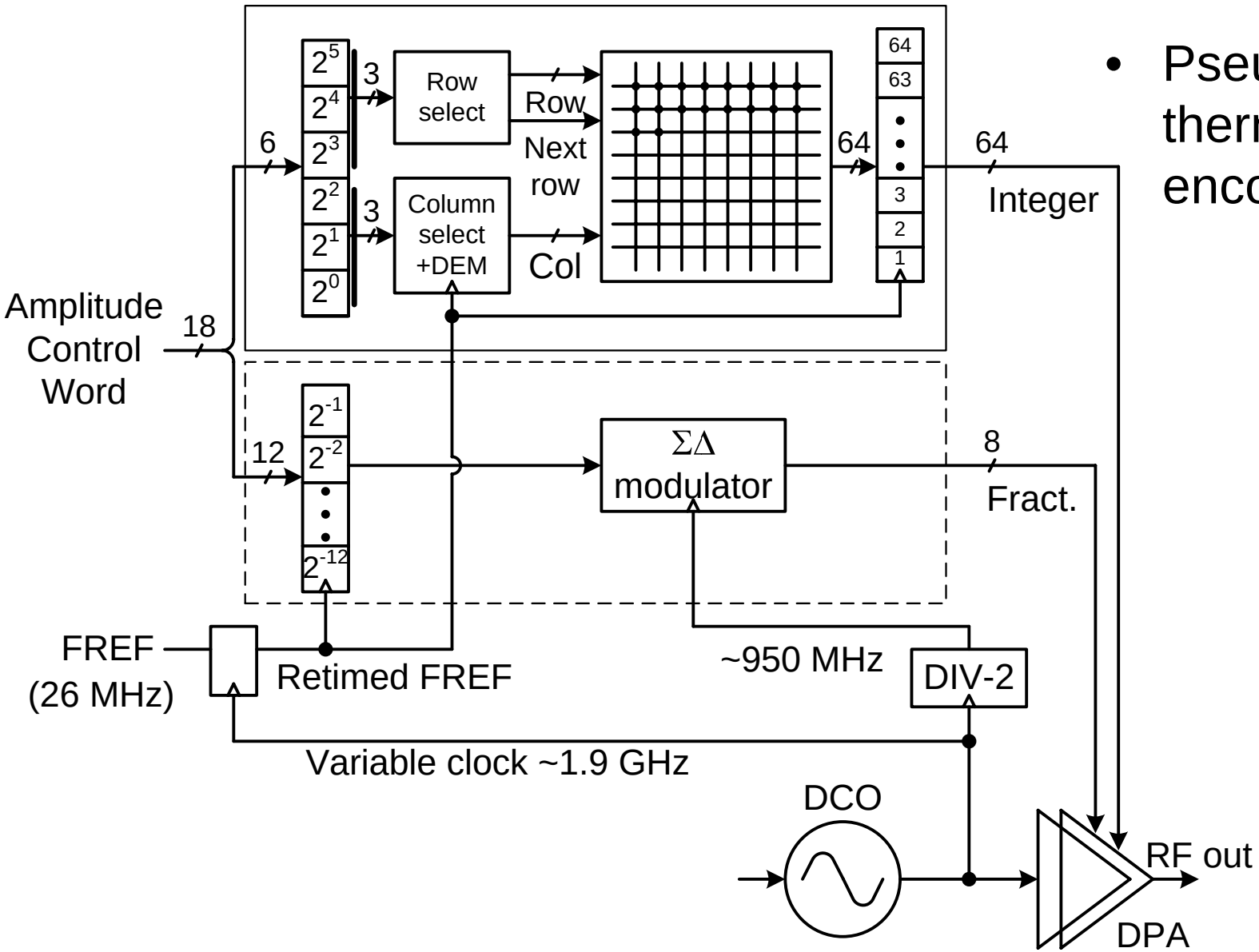
Generic Modulator
Digital-to-Frequency Converter (DFC)
**Digital-to-RF-Amplitude Converter (DRAC)**
Polar Transmitter



# Digital Amplitude Modulation Circuit




- Pseudo-thermometer encoding

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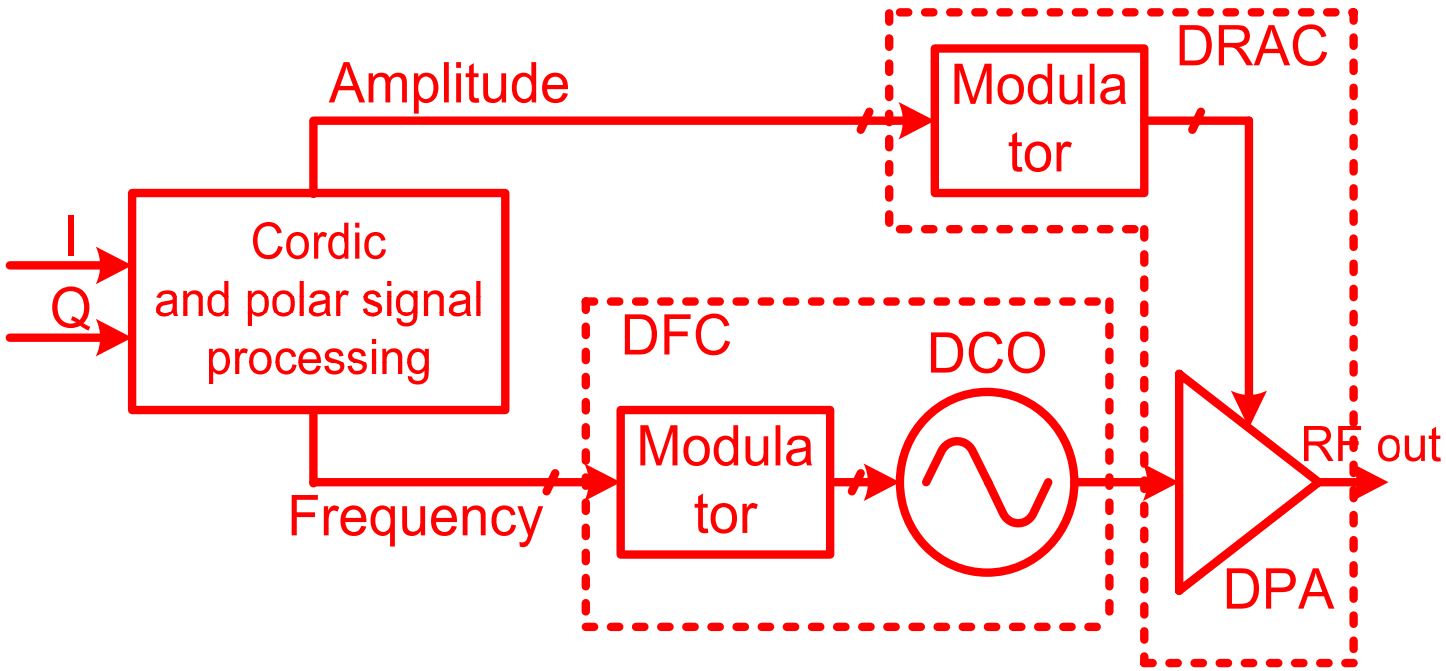
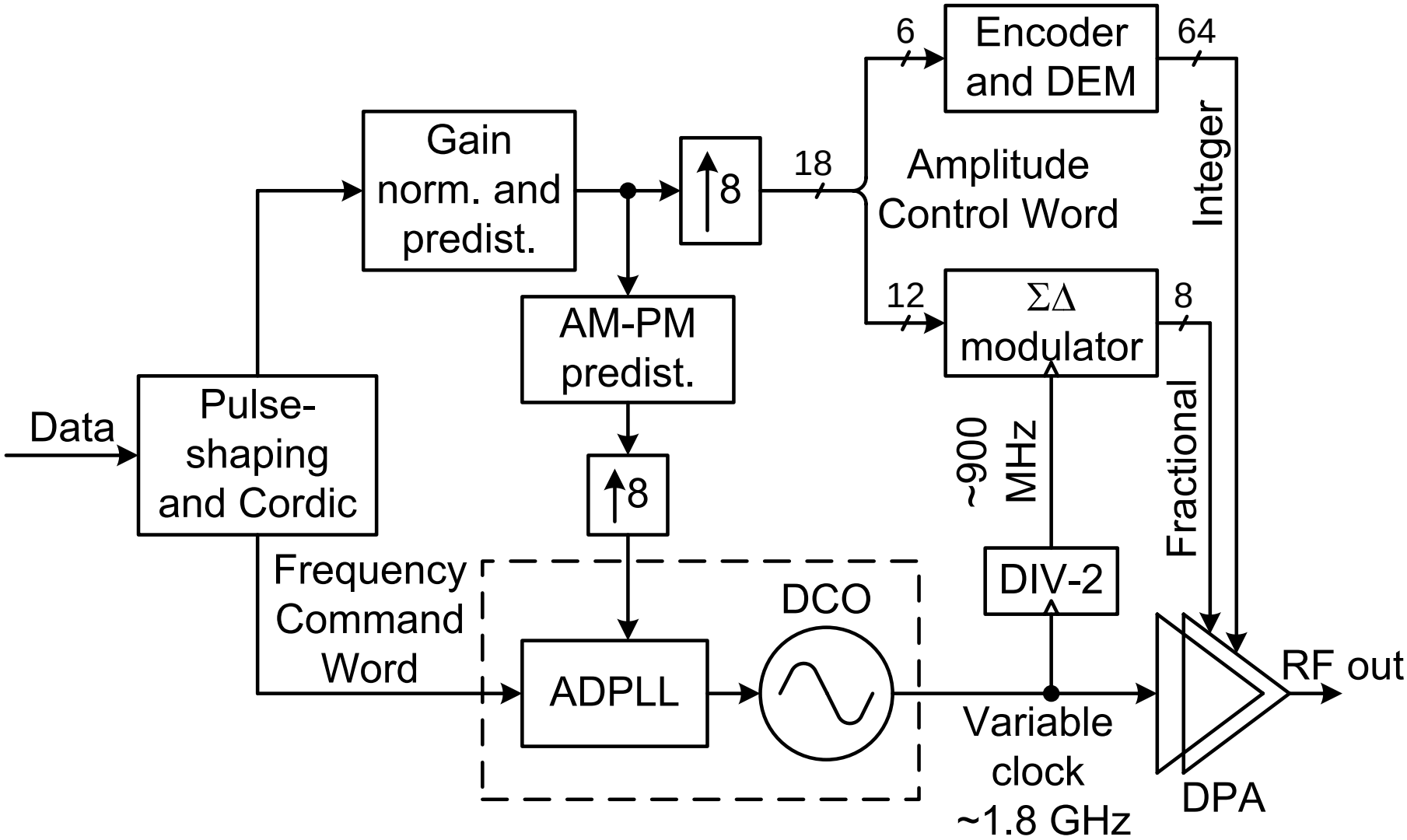
# Polar Transmitter



# AM Path of the Polar TX

- DPA combines PM and AM paths

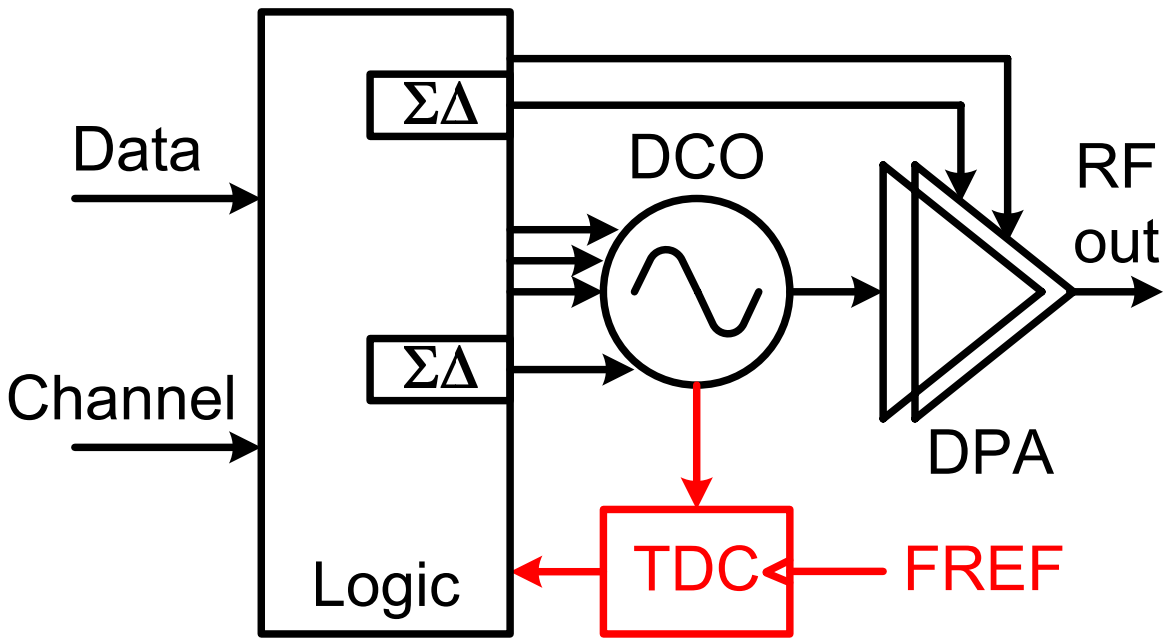


# Time-to-Digital Converter (TDC)

## Digital Loop Filter (LF)

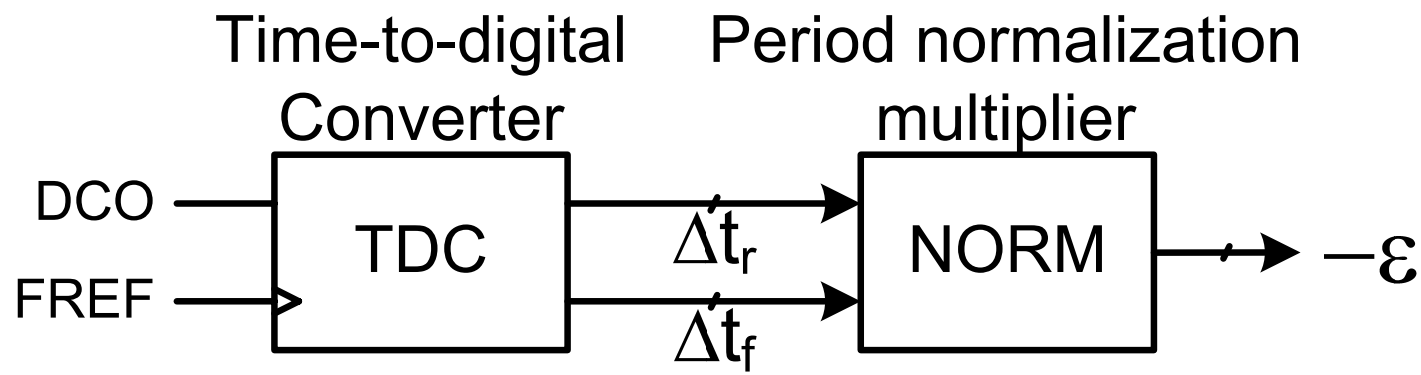
## All-Digital PLL (ADPLL)

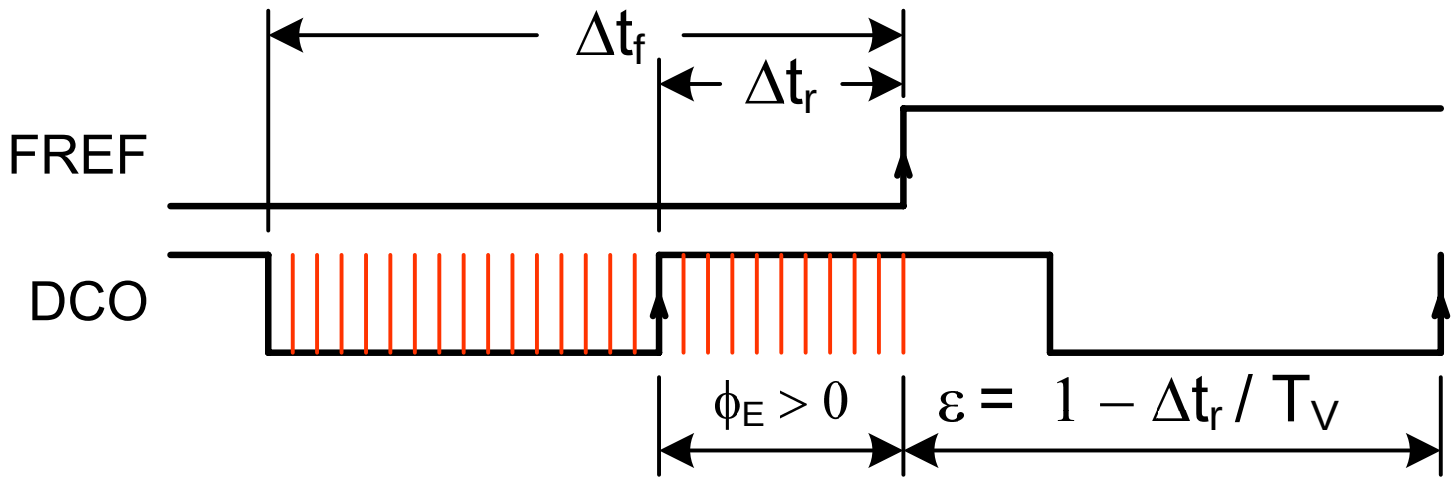
## ADPLL Wideband Frequency Modulation



# Fractional Phase Error Estimation

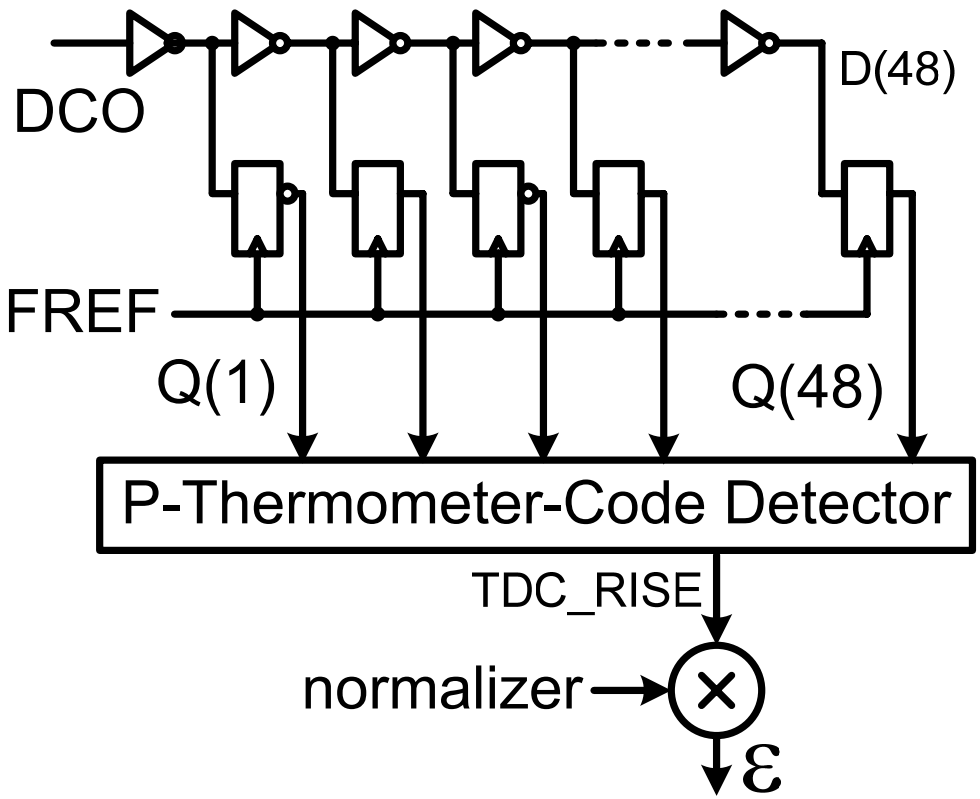
- Quantized phase detector with resolution of <20 ps

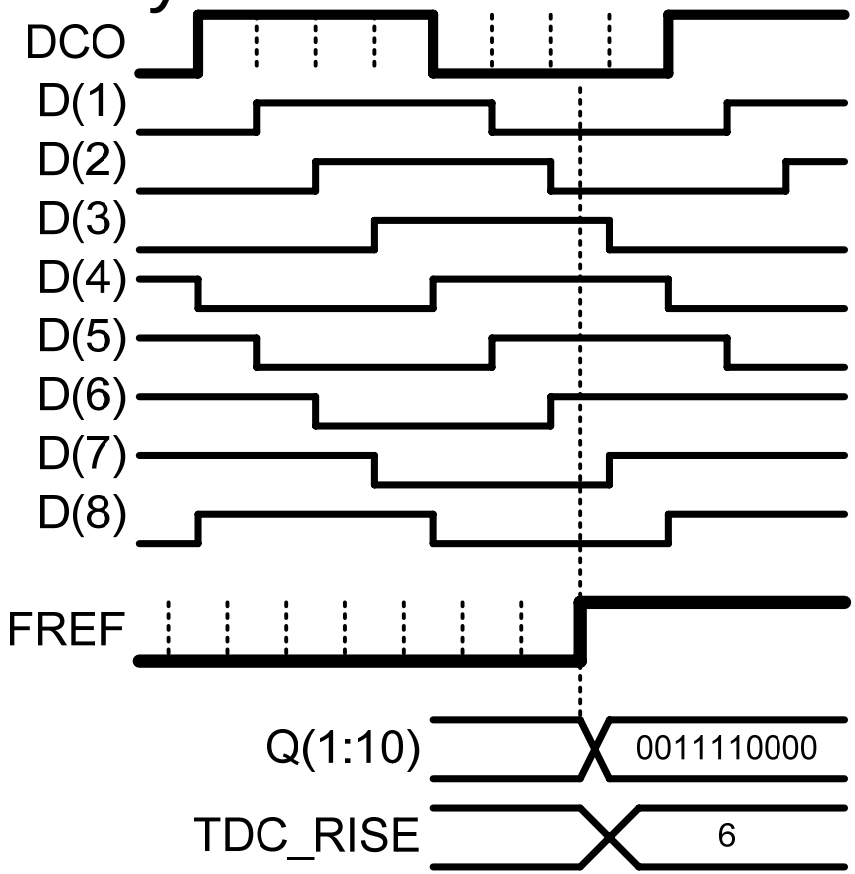


# Time-to-digital Converter (TDC)

- Quantized phase detector with resolution of 20 ps
- DCO clock passes through the inverter chain
- Delayed outputs are sampled by FREF

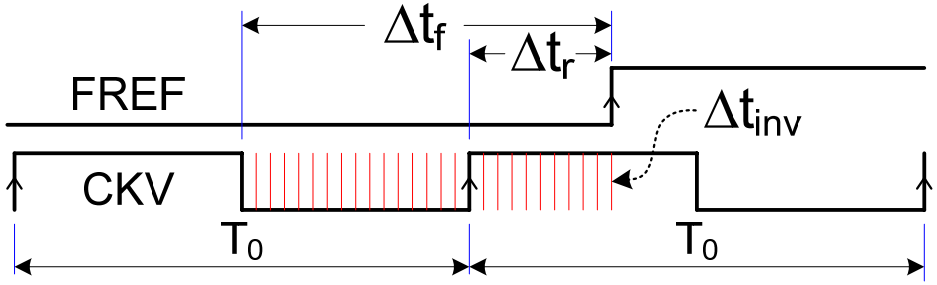


# Period Normalization

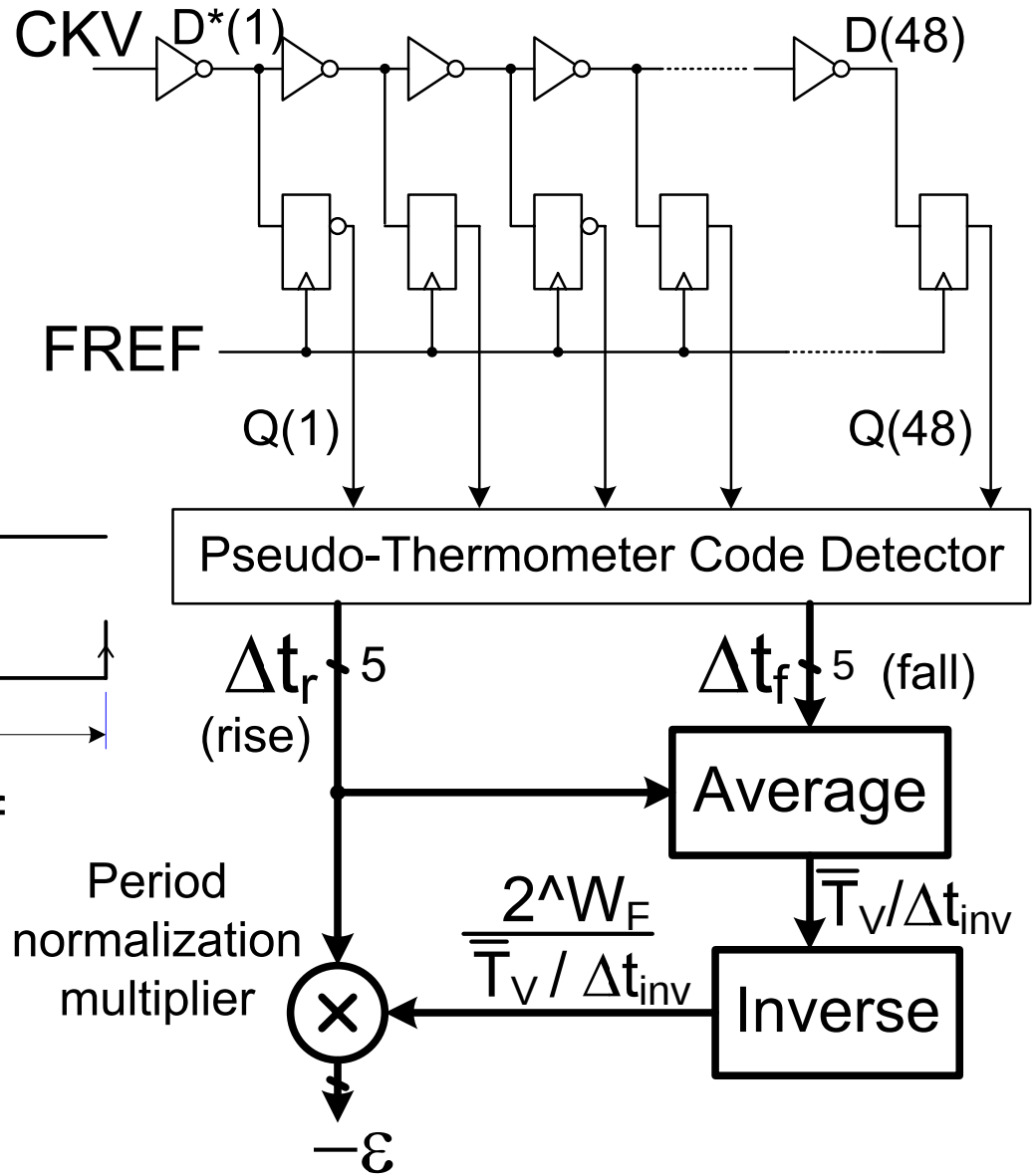
- Expected output between 0.0 – 1.0 UI

$$-\varepsilon = \frac{2^{W_F}}{\overline{T}_V / \Delta t_{inv}}$$

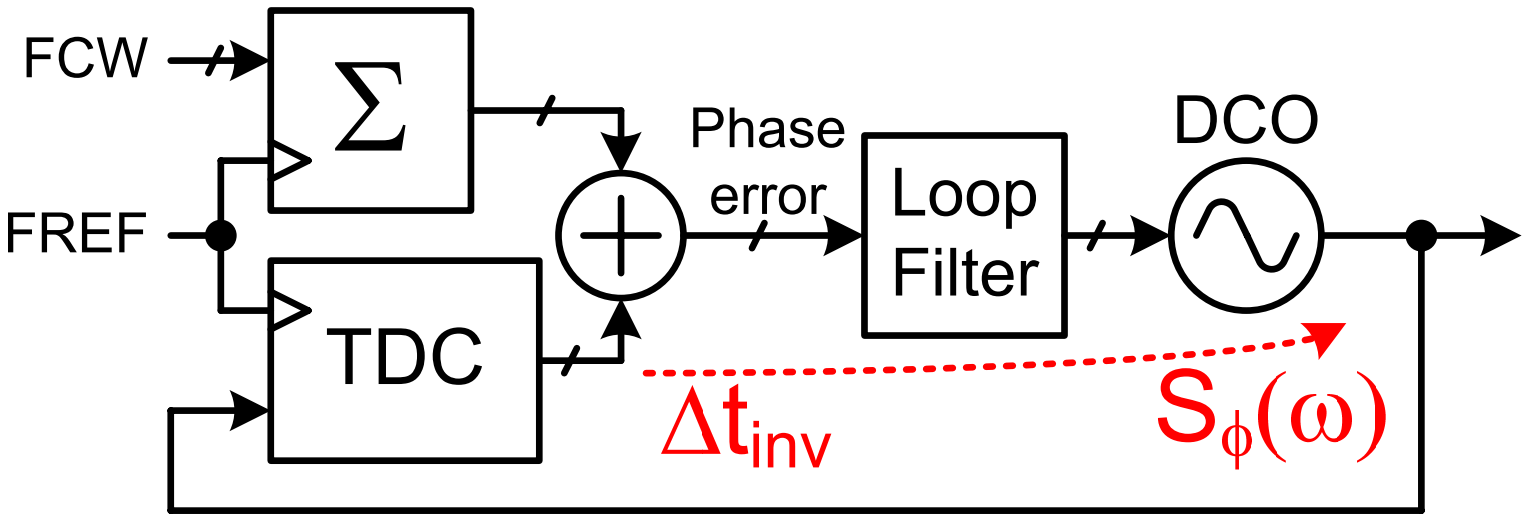



- Accurate calibration of the inverter delay

$$\overline{T}_V = \frac{1}{N_{avg}} \sum_{k=1}^{N_{avg}} T_V[k]$$



# Phase Noise Due to TDC



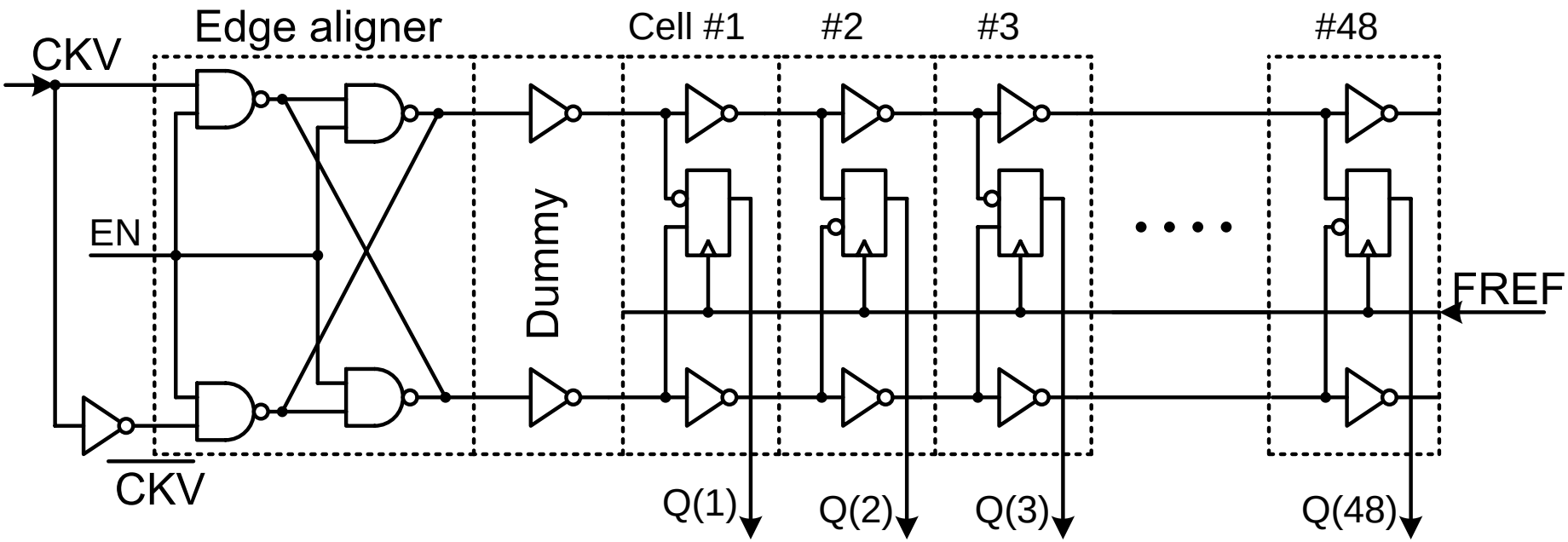

- In-band phase noise at RF output [RFIC'04]

$$L = \frac{(2\pi)^2}{12}\left(\frac{\Delta t_{inv}}{T_V}\right)^2 \cdot \frac{1}{f_R}$$

  - E.g., $\Delta t_{inv}$=20ps, $f_v$=1.8GHz, $f_R$=26MHz, **L = -97.8dBc/Hz**
  - Good enough for GSM: can get only better

# TDC Core Implementation

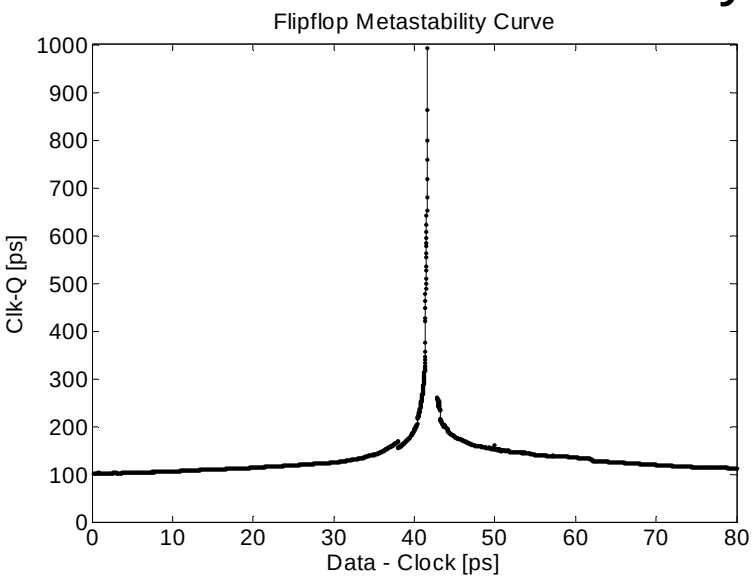
- Novel pseudo-differential architecture
- Insensitive to NMOS and PMOS mismatches
- TDC resolution close to an inverter delay
  - 15 – 20 ps
  - Fastest logic-level regenerative delay in CMOS

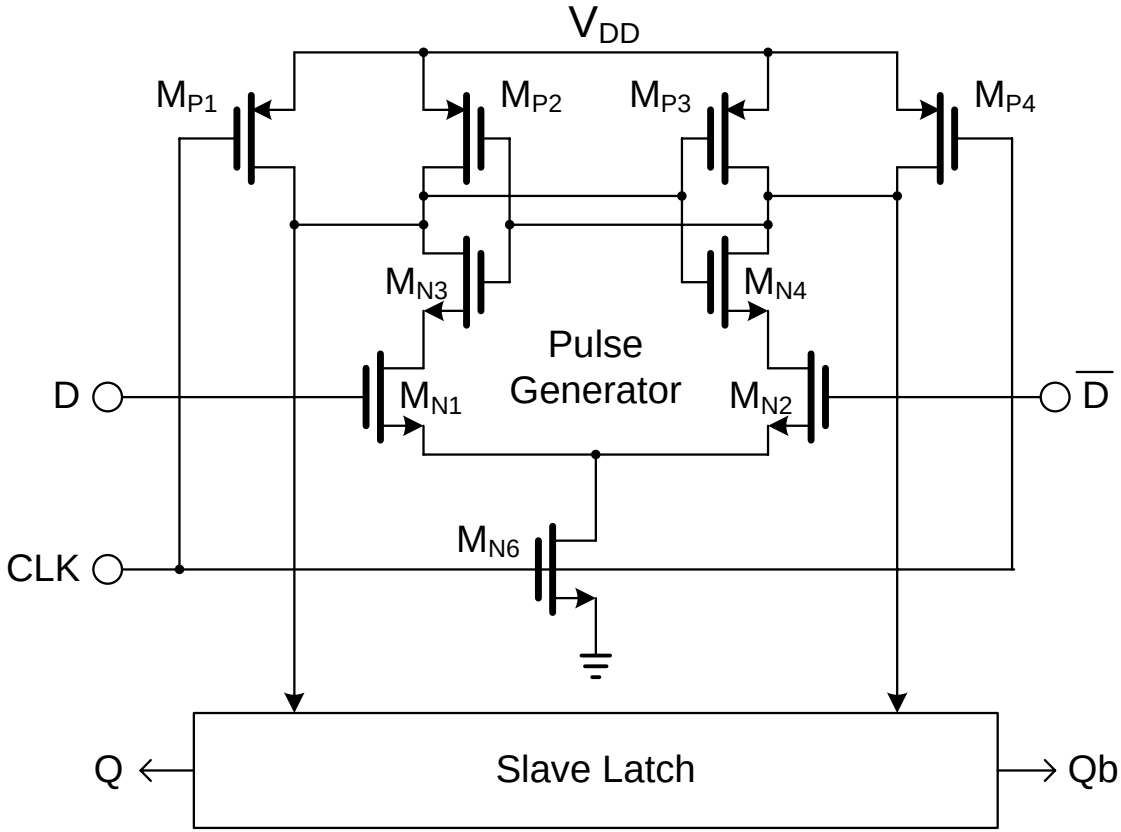


# High-Resolution Flip-Flop

- Adapted from [Nikolic, JSSC'00]
- Symmetric along the vertical axis
- Identical resolution of rising and falling edges
- Light input loading

- Simulated metastability



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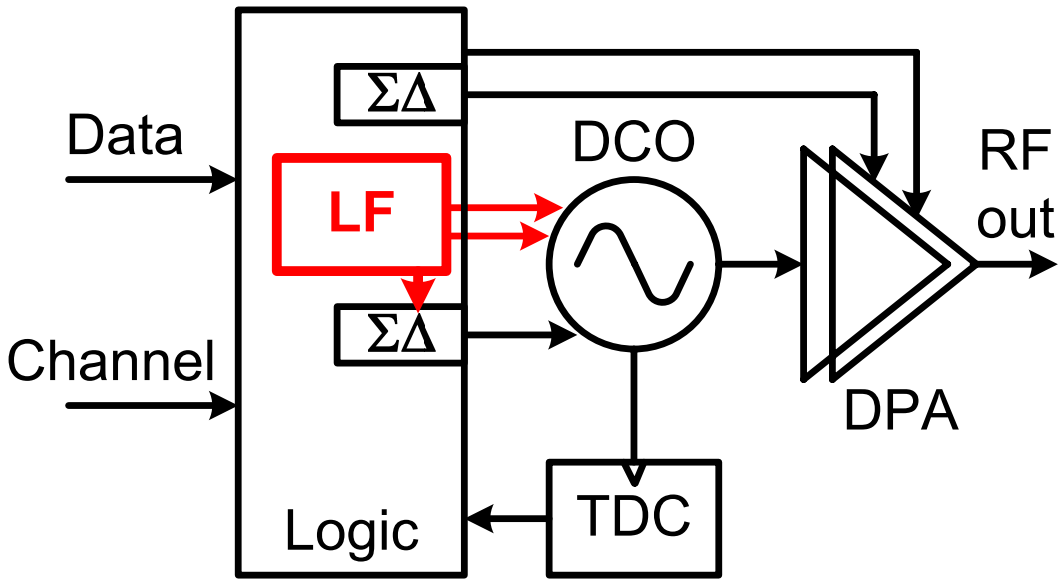
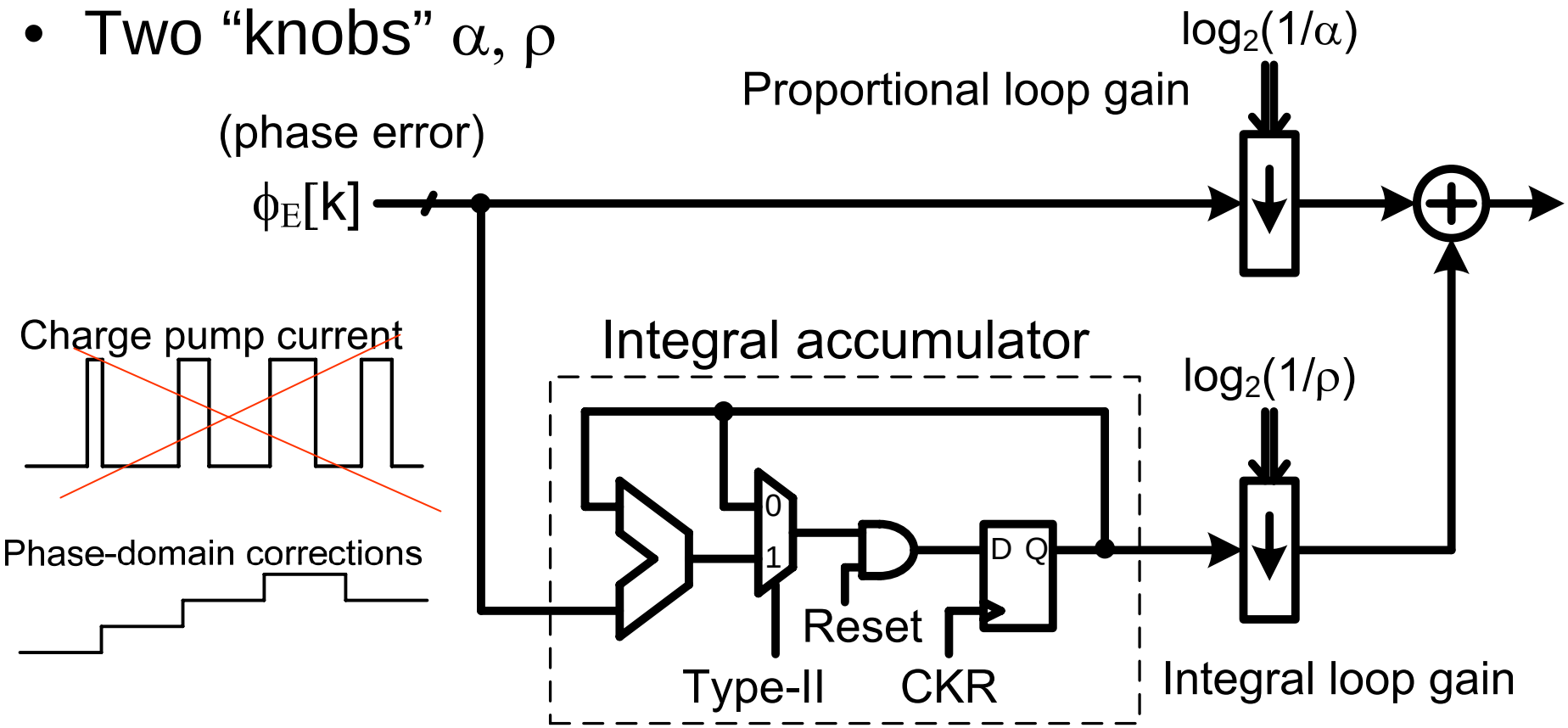
# **Digital Loop Filter (LF)**
# All-Digital PLL (ADPLL)
# ADPLL Wideband Frequency Modulation



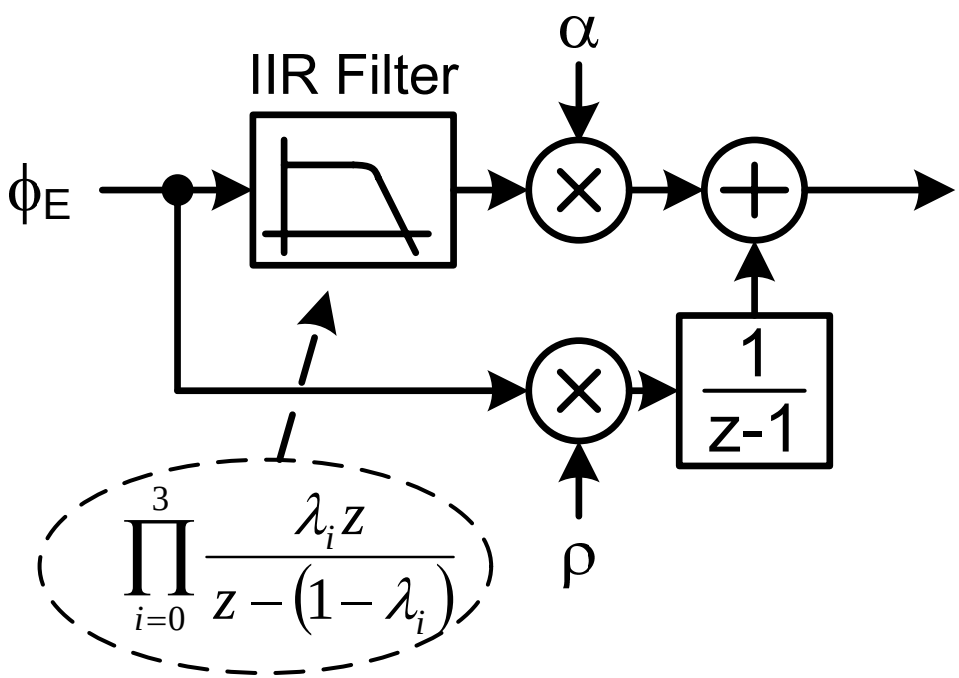
# Type-II Loop Filter

- No correlative detection spurs
- Software programmed PLL loop:
  - Gentle transition of type-I to type-II
- Two "knobs" $\alpha$, $\rho$



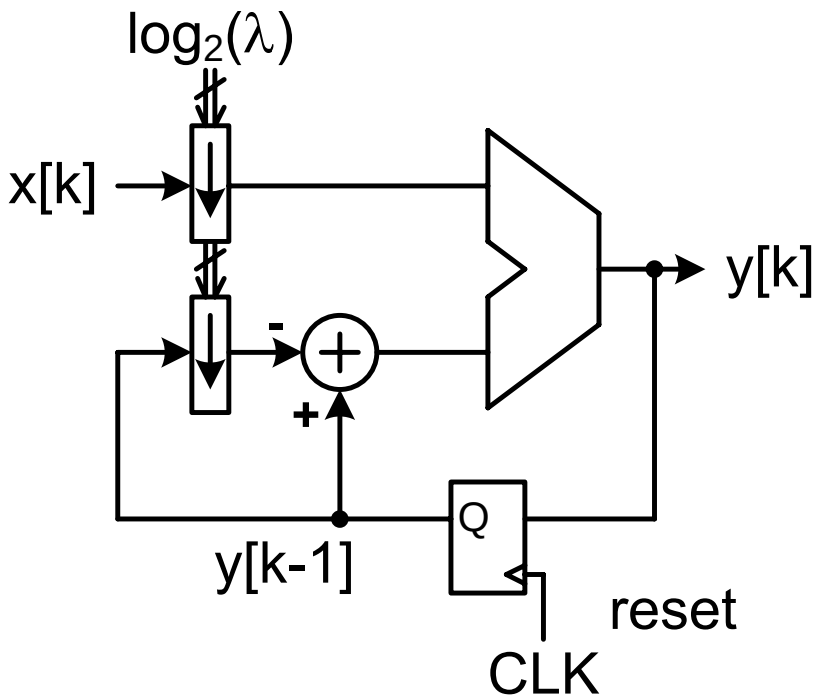
# Loop filter with IIR Filtering

- 4th order digital IIR loop filter to suppress the frequency reference and TDC quantization noise
- Unconditionally stable IIR filter

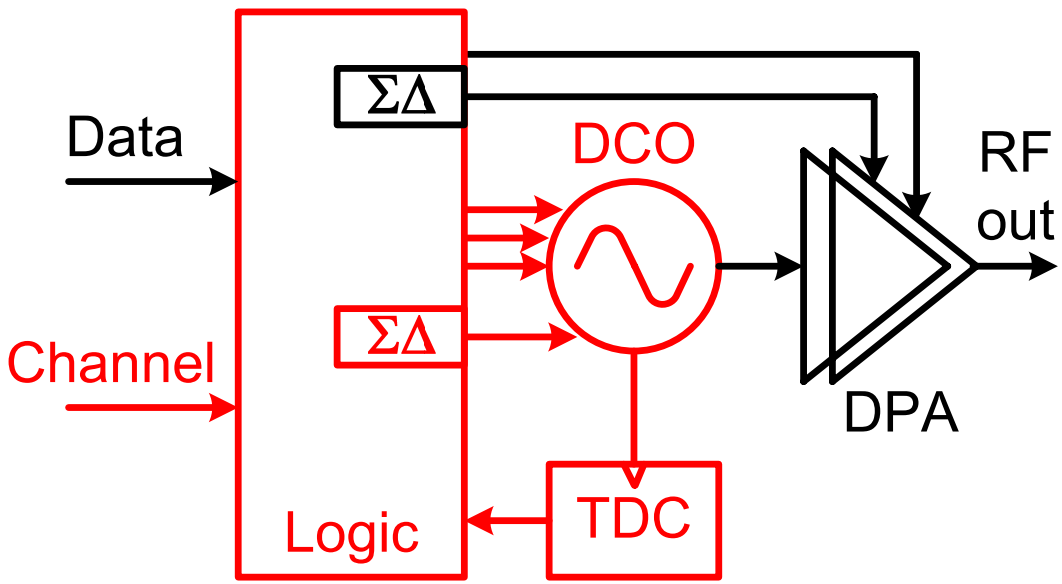



Single-pole IIR stage:

$$y[k] = (1-\lambda)\cdot y[k-1] + \lambda \cdot x[k]$$

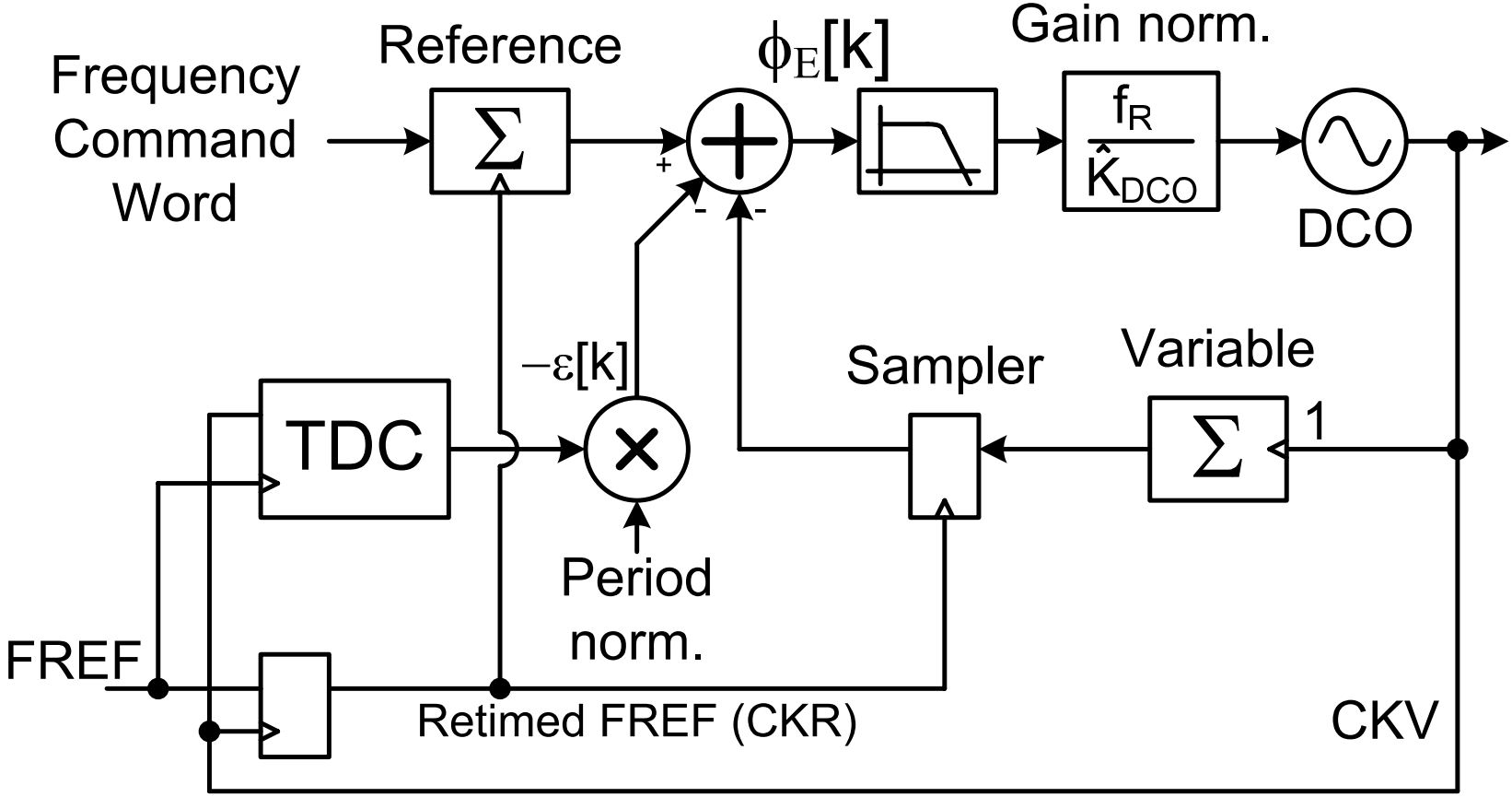


# Time-to-Digital Converter (TDC)
# Digital Loop Filter (LF)
# **All-Digital PLL (ADPLL)**
# ADPLL Wideband Frequency Modulation



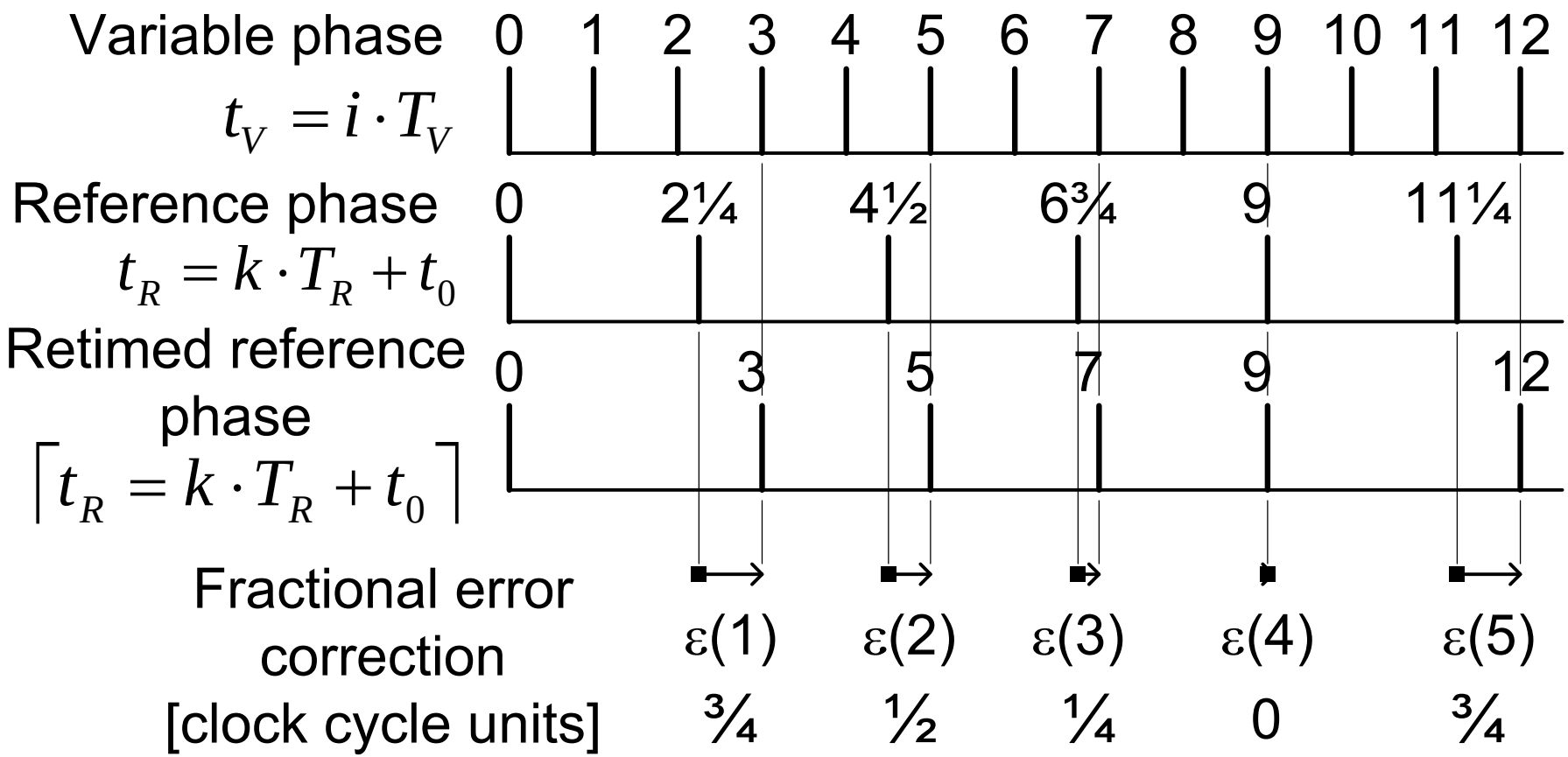
# All-Digital PLL (ADPLL)

- Phase domain operation
- Digitally synchronous fixed-point arithmetic
- Phase signals cannot be corrupted by noise



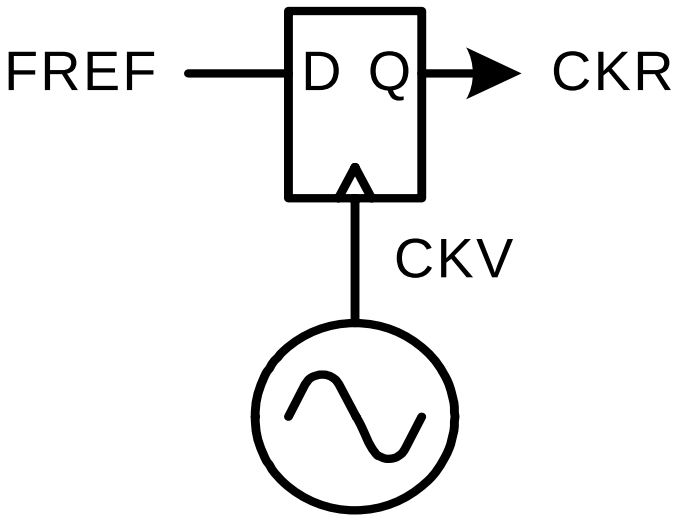
# Phase Domain Operation

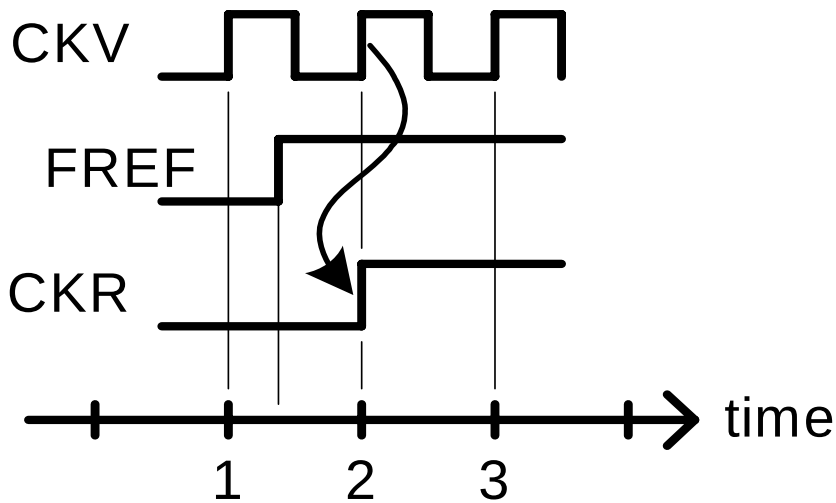
*e.g., N=2.25*



# Reference Phase Retiming

- DCO clock and FREF domains are not entirely synchronous despite being in phase lock
- Variable and reference phases cannot be compared in hardware: metastability!
- Solution: Oversampling FREF by CKV and using the resulting CKR

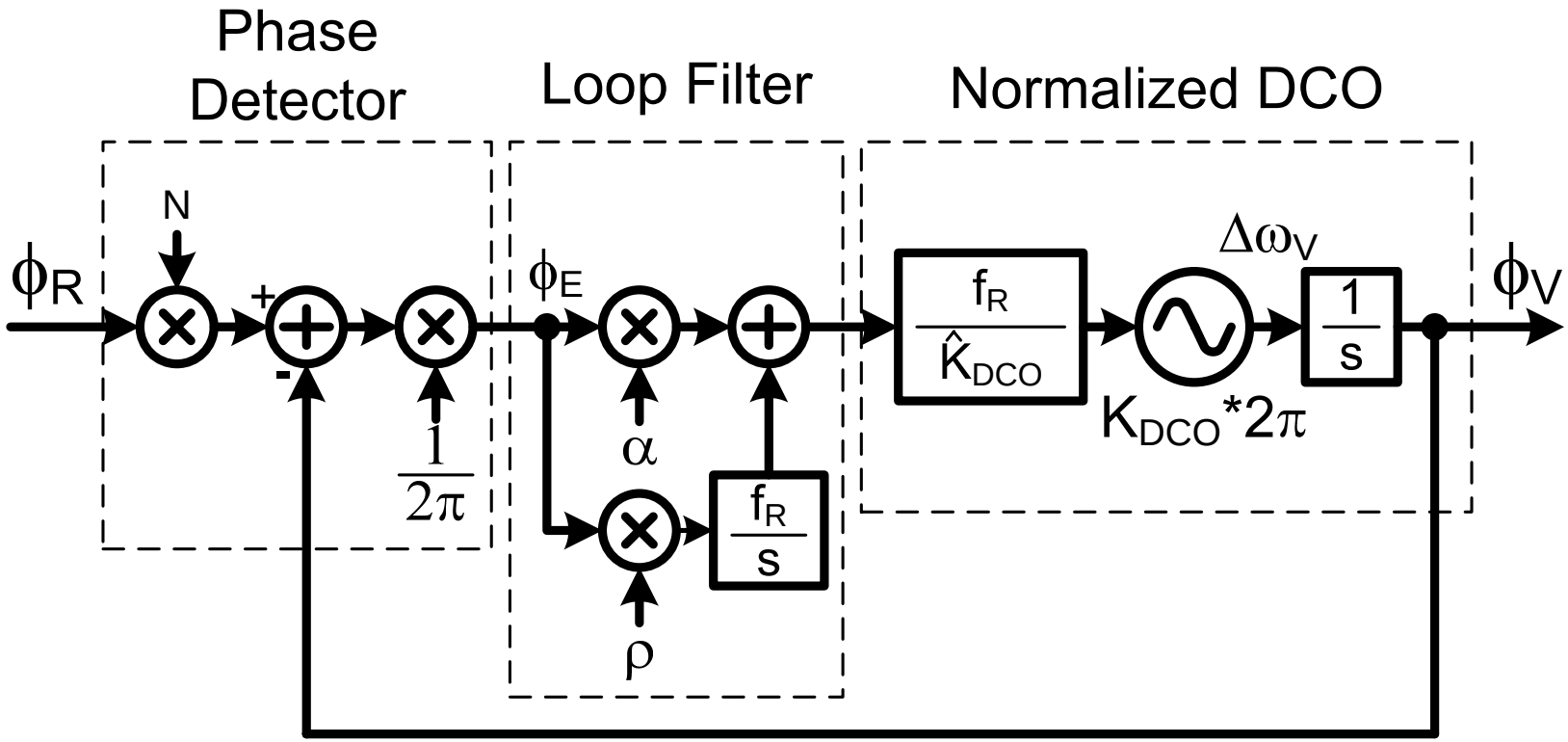


# Frequency Response of 2nd-order PLL

- IIR filter turned off
- Type-II second-order PLL loop
- "knobs" $\alpha$, $\rho$

$$H_{ol}(s) = (\alpha + \frac{\rho f_R}{s}) \frac{f_R}{s}$$



# 2nd-order PLL: Closed-Loop Response

- Closed-loop transfer function

$$H_{cl}(s) = N\frac{\alpha f_R s + \rho f_R^2}{s^2 + \alpha f_R s + \rho f_R^2}$$

- Canonical two-pole control system

$$H_{cl}(s) = N\frac{2\xi\omega_n s + \omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2}$$

Natural frequency

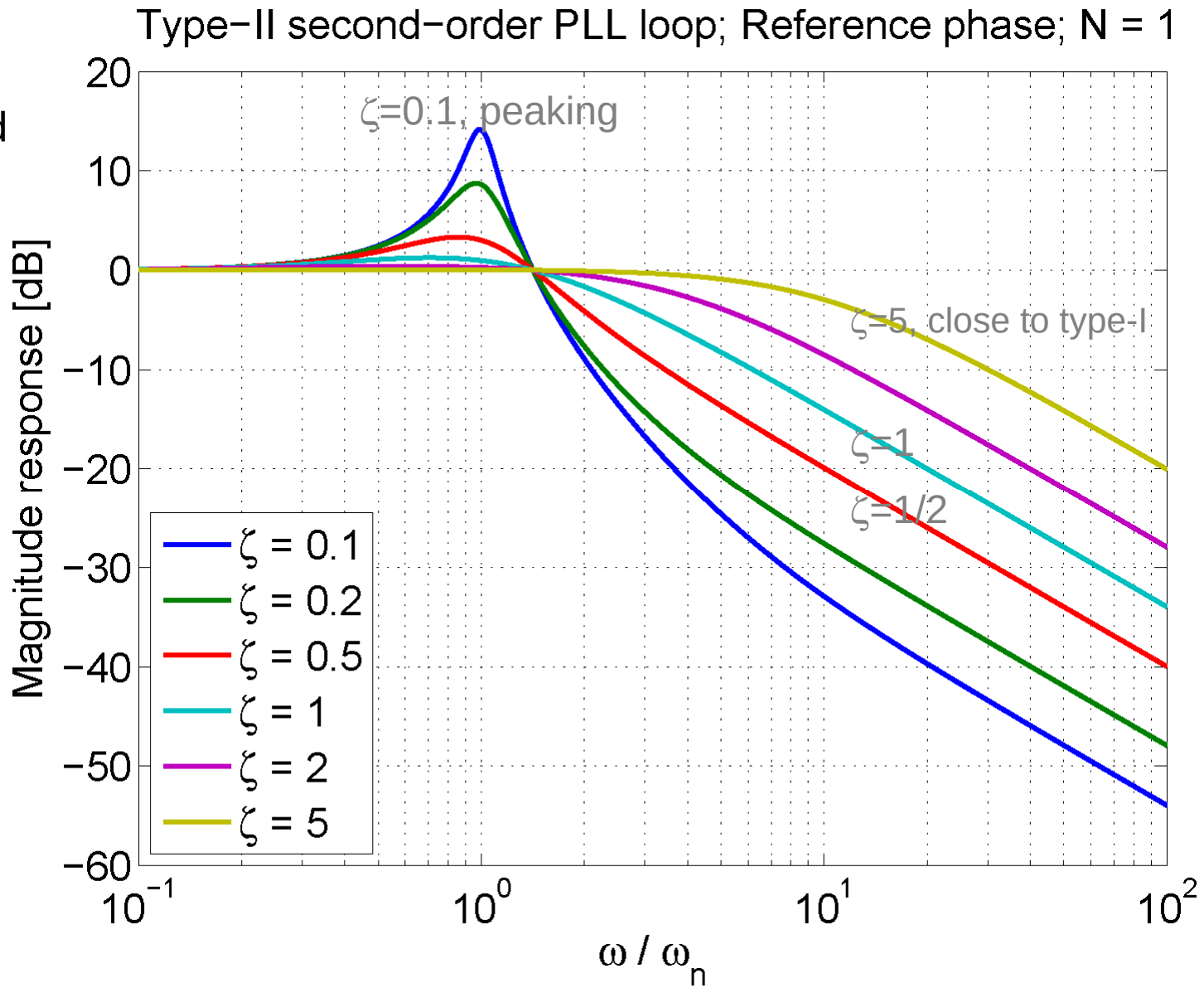
$$\omega_n = \sqrt{\rho}\, f_R$$

Damping factor

$$\xi = \frac{1}{2}\frac{\alpha}{\sqrt{\rho}}$$

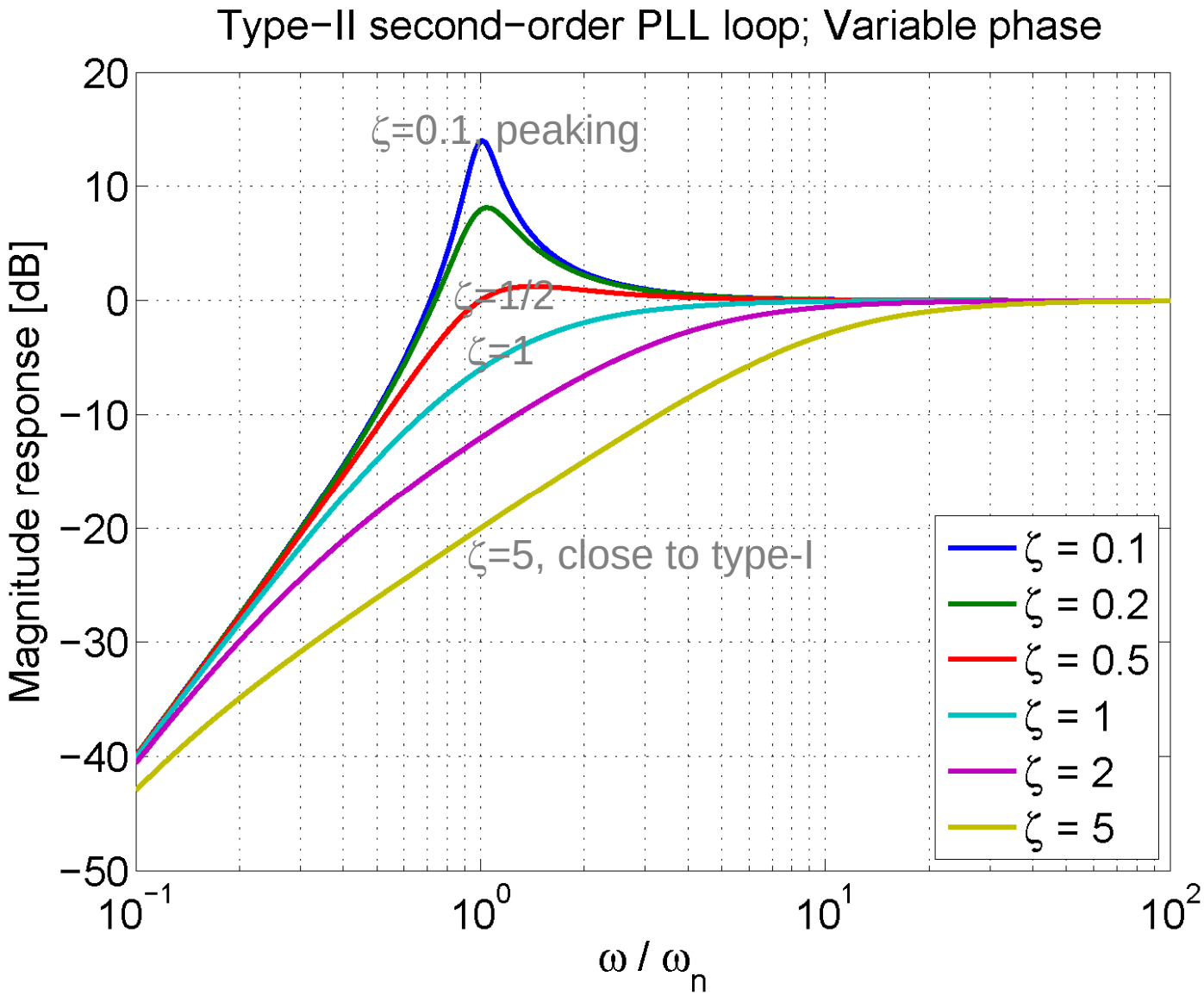
# FREF/TDC Transfer Function

- Type-II 2nd order PLL
- Weak filtering



# DCO Transfer Function

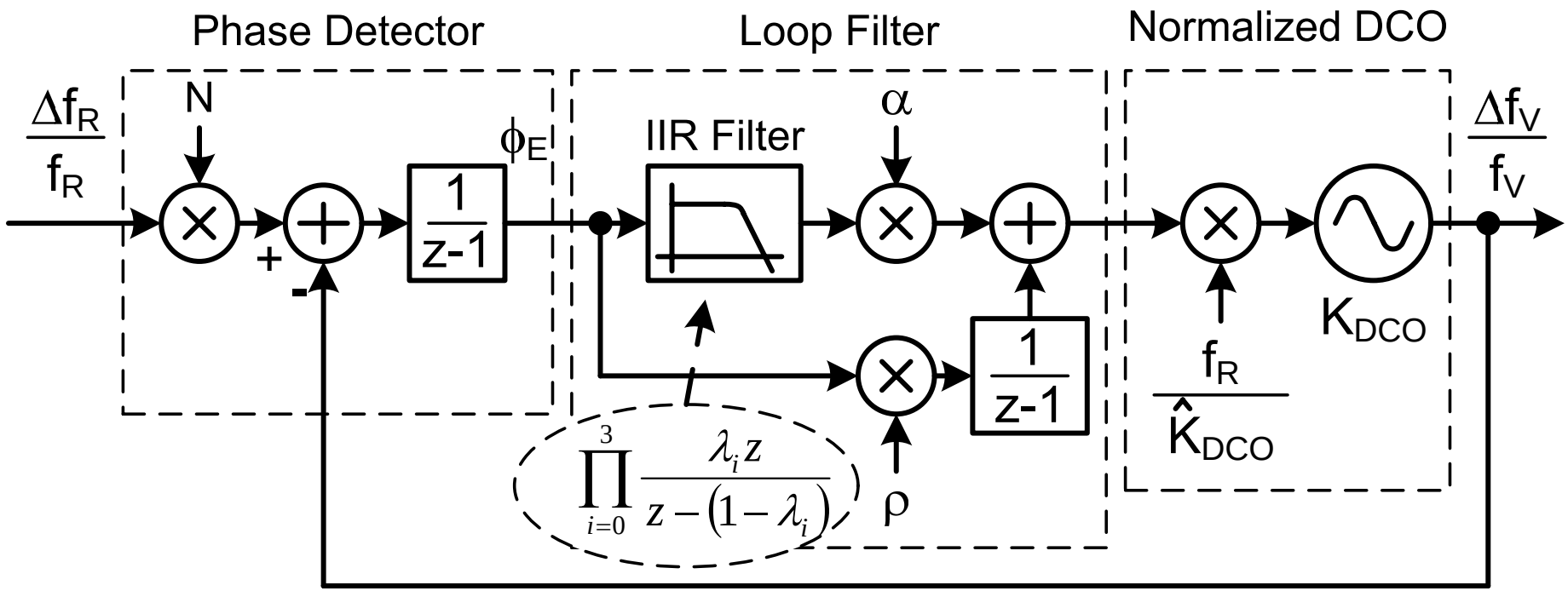
- Type-II 2nd order PLL
- 20 dB/dec
  - Type-I
- 40 dB/dec
  - Type-II
- 1/f noise attenuation



# z-Domain Model of the ADPLL

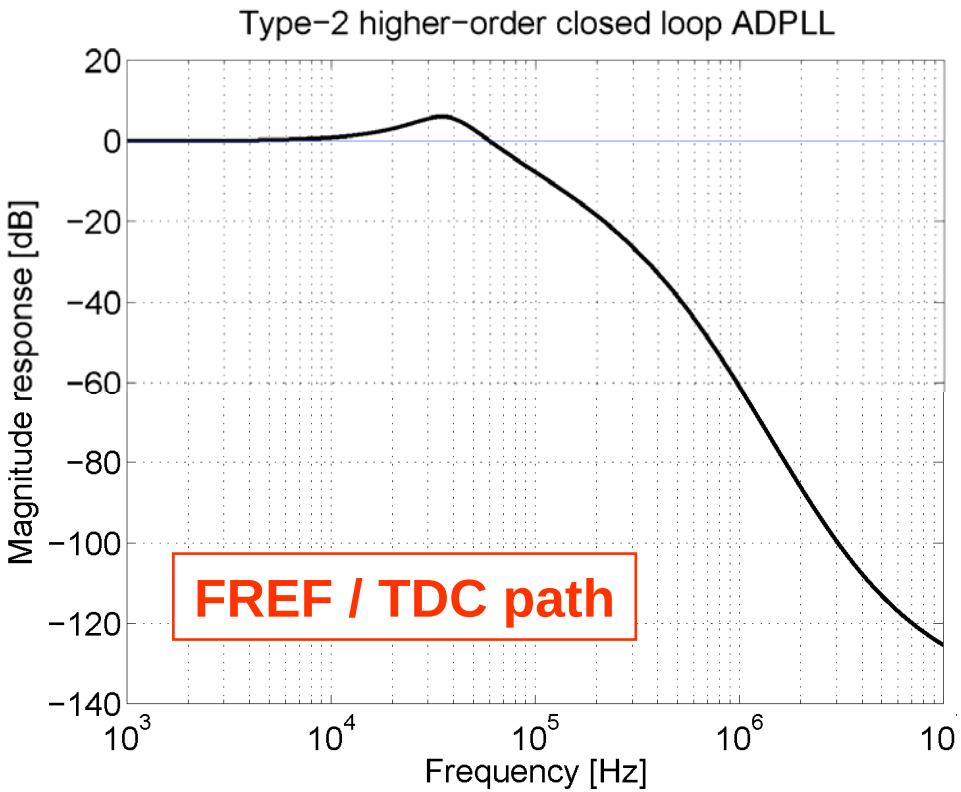
- "knobs" $\alpha$, $\rho$, $\lambda_{1\text{-}4}$
- Type-I or Type-II PLL loop
- 1st through 6th order

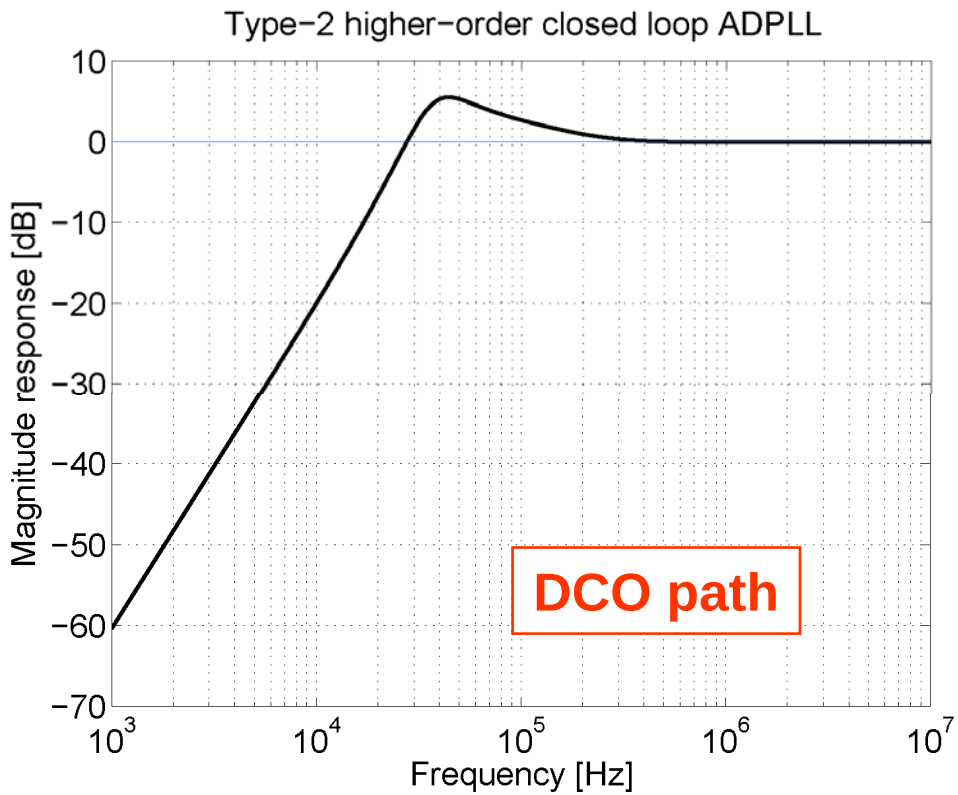
$$H_{ol}(s) = \left[ \alpha \cdot H_{iir}(s) + \frac{\rho \cdot f_R}{s} \right] \frac{f_R}{s}$$



# PLL Transfer Function

- Type-II 6th-order PLL
- Settings: $\alpha = 2^{-7}$, $\rho = 2^{-15}$, $\lambda = 2^{-[3\ 3\ 3\ 4]}$
- Provides 33 dB of attenuation at 400 kHz
- Provides 40 dB/dec filtering of 1/f DCO noise

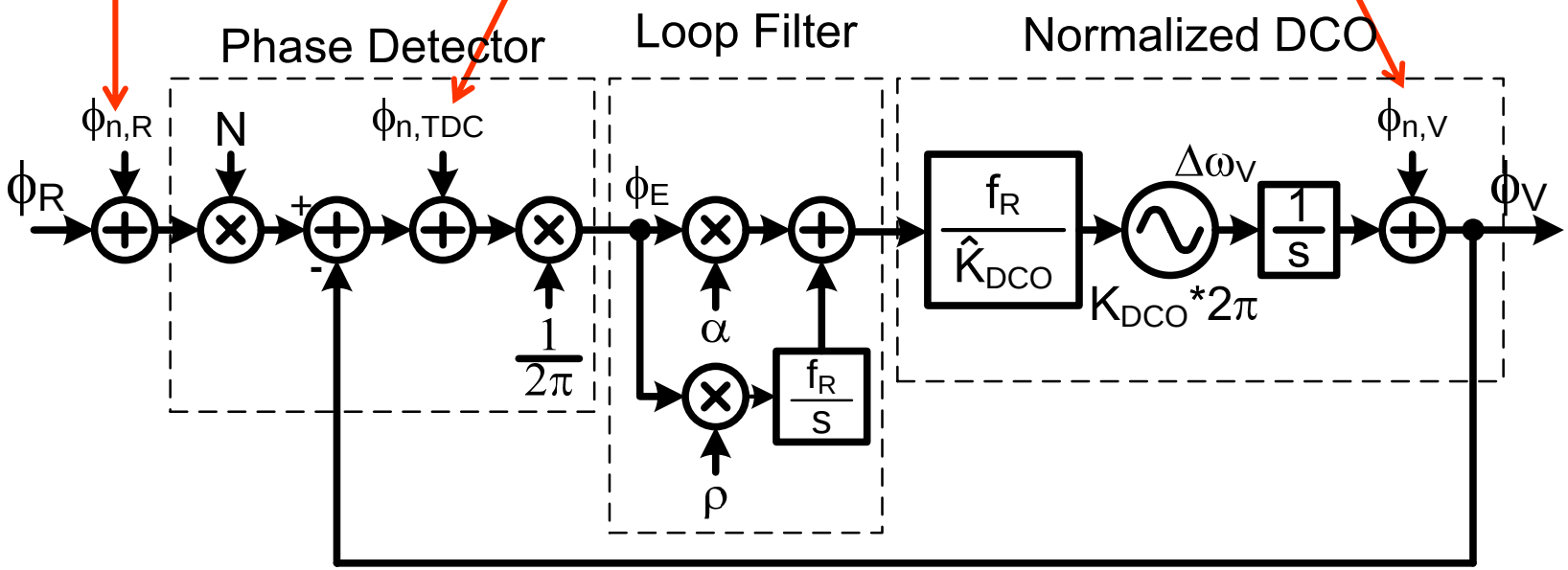


# Noise and Error Sources

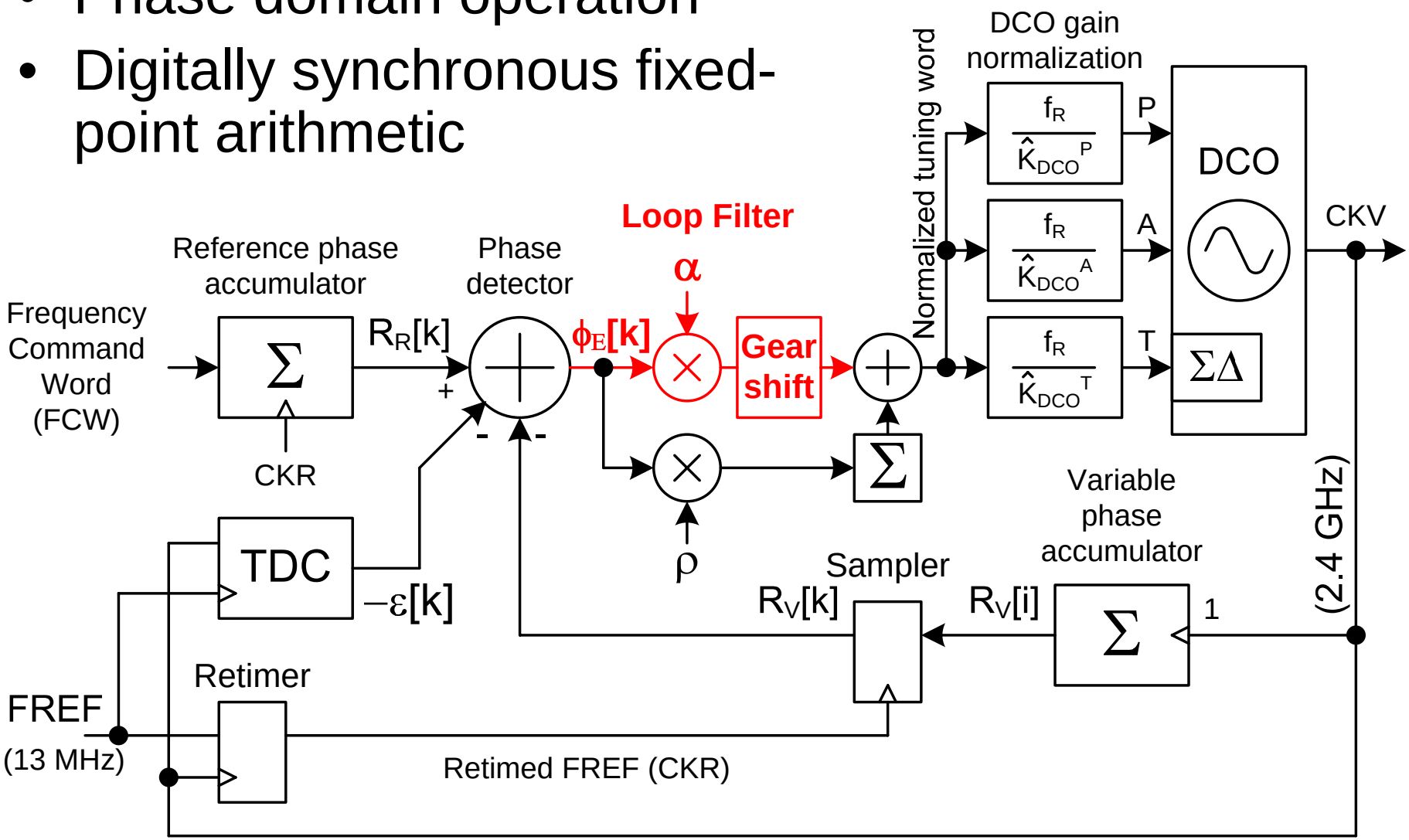
- Only three noise sources
  - Frequency reference (external to ADPLL) – low pass
  - TDC quantization – low pass
  - DCO oscillator – high pass

$$H_{cl,R}(s) = N\frac{H_{ol}}{1+H_{ol}} \qquad H_{cl,TDC}(s) = \frac{H_{ol}}{1+H_{ol}} \qquad H_{cl,V}(s) = \frac{1}{1+H_{ol}}$$



# All-Digital PLL (ADPLL)

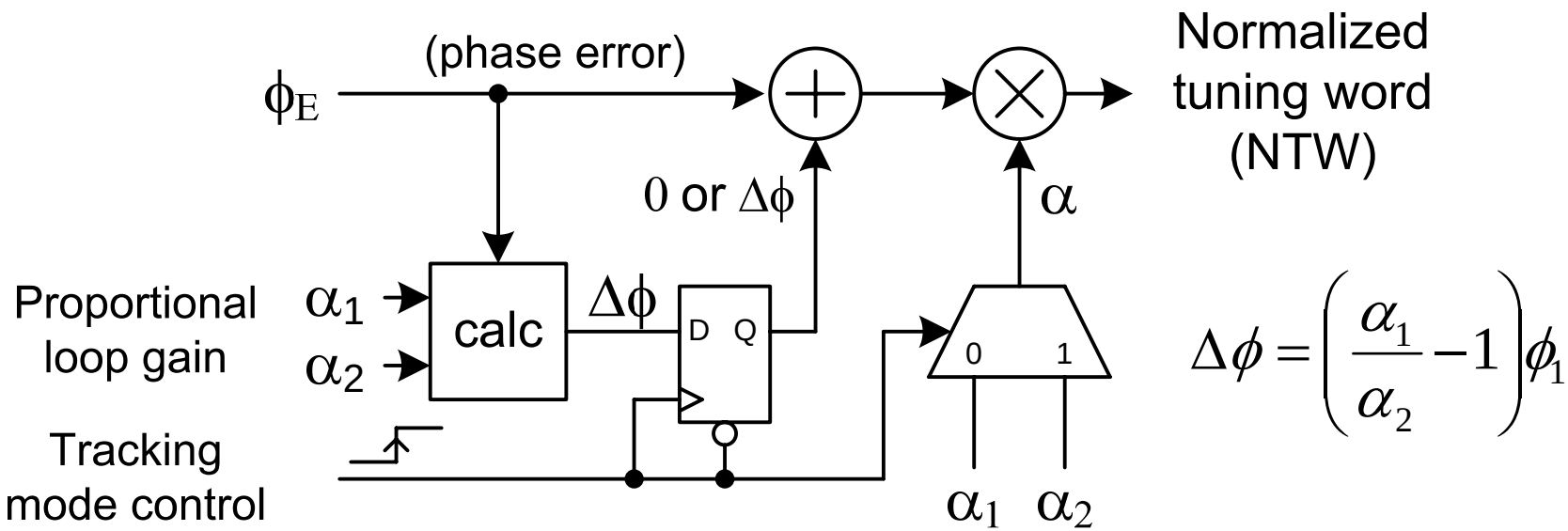
- Phase domain operation
- Digitally synchronous fixed-point arithmetic



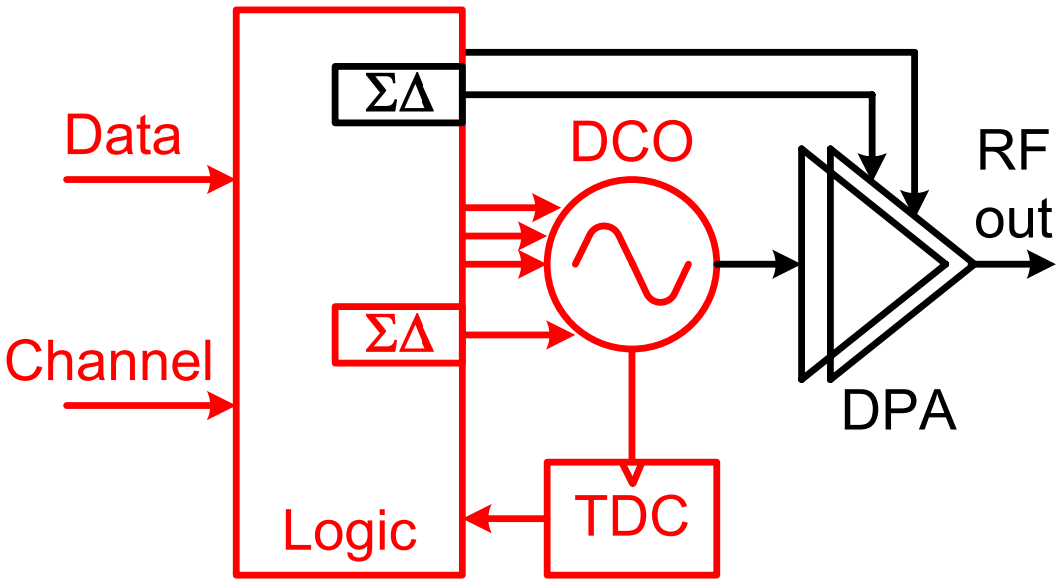
# Gear Shifting of PLL Bandwidth

- Executed in tracking mode after the acquisition is completed
- Normalized tuning word continuity before and after the event
- Guarantees no frequency perturbation of the oscillator

$$\alpha_1 \cdot \phi_1 = \alpha_2 \cdot (\phi_1 + \Delta\phi)$$

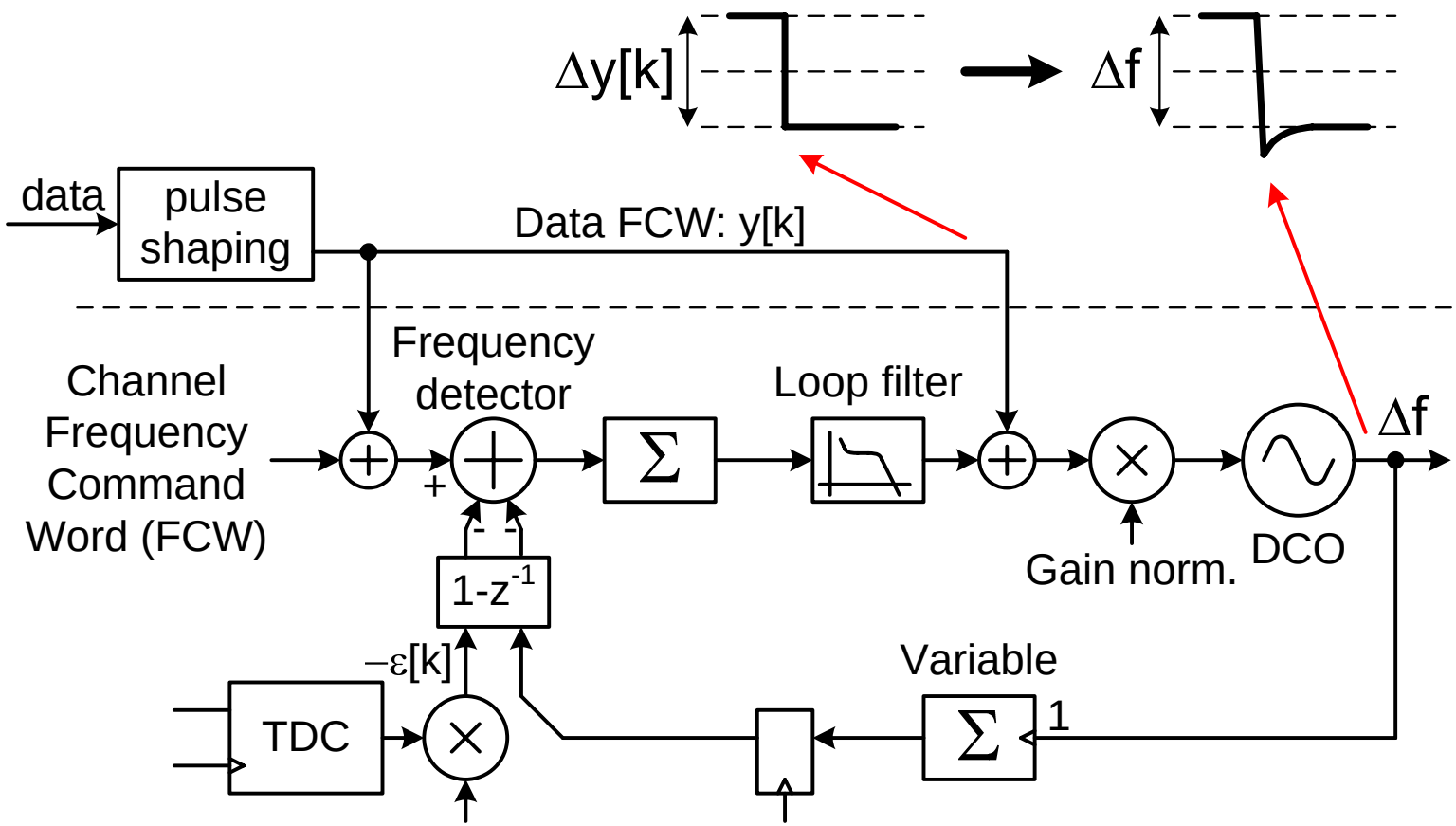


# Time-to-Digital Converter (TDC)
# Digital Loop Filter (LF)
# All-Digital PLL (ADPLL)
# ADPLL Wideband Frequency Modulation

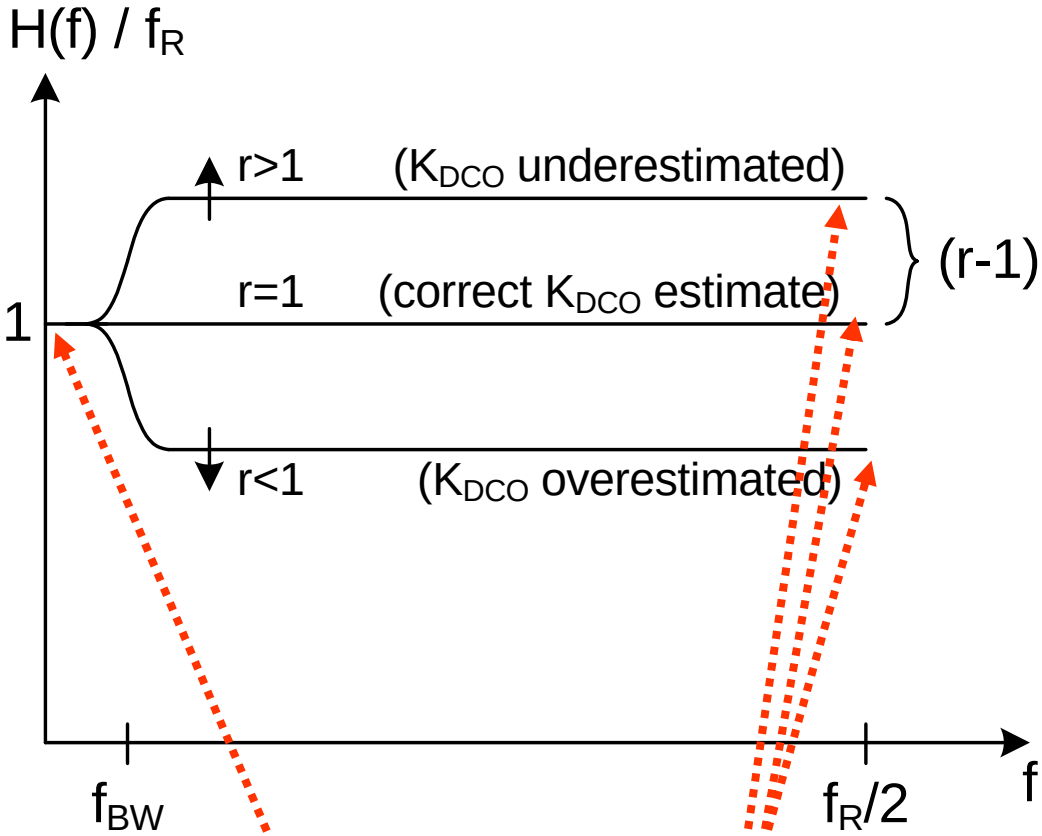


# ADPLL with Wideband Modulation

- Two-point modulation
  - Direct feedforward path – y[k] directly drives the DCO
  - Compensating path – y[k] added to the channel FCW



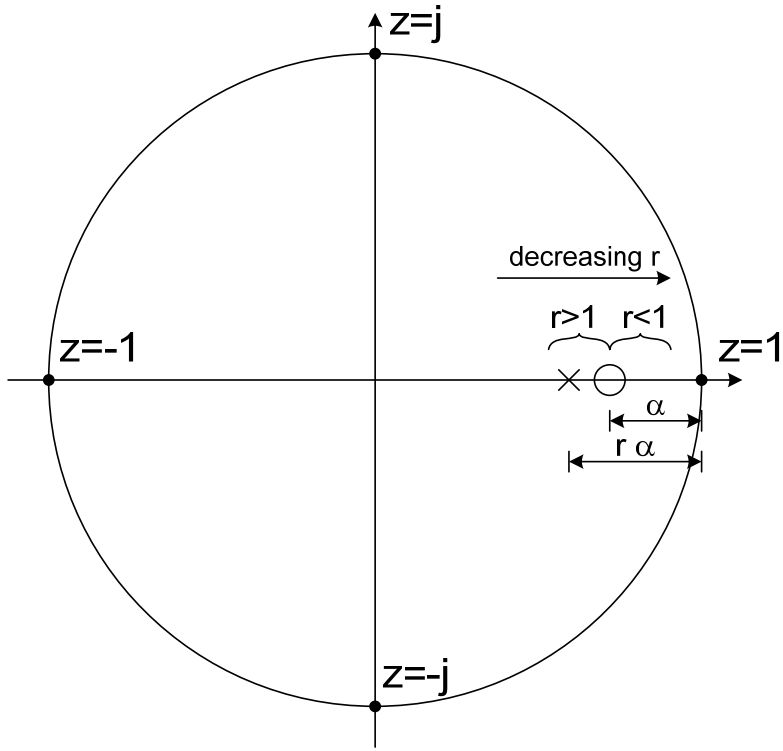
# Error in DCO Gain Estimation




$$H(z) \cong f_R (r-1)\left[1+\frac{\alpha r}{2}\right]$$

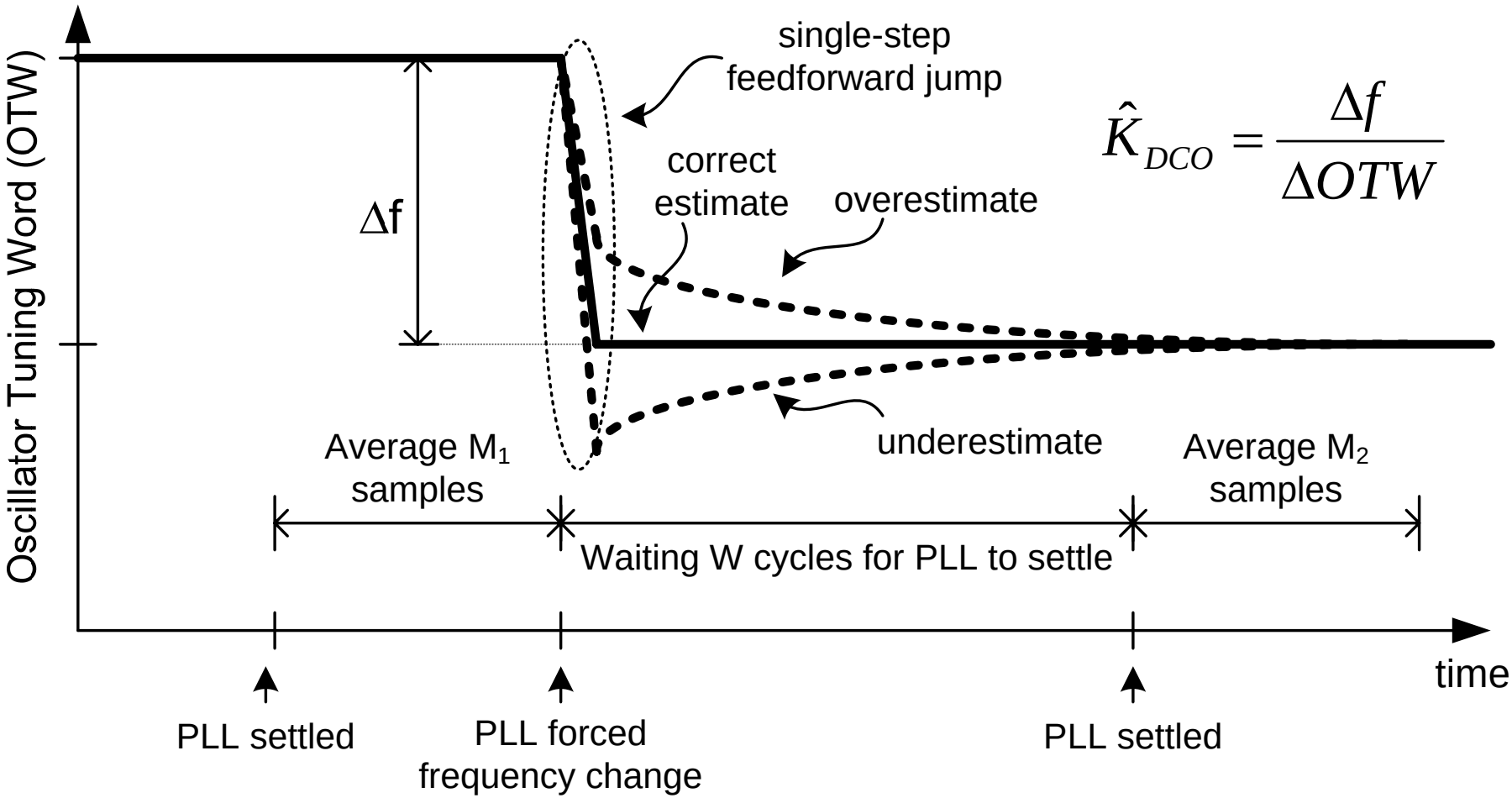
$$H(z) = f_R \cdot r \frac{z-(1-\alpha)}{z-(1-r\alpha)}$$

$$H(z)\big|_{z=1} = f_R \qquad H(z)\big|_{z=-1} = f_R \cdot r \frac{-2+\alpha}{-2+\alpha r}$$




- Transfer function somewhat high-pass or low-pass

# Just-in-time DCO Gain Estimation



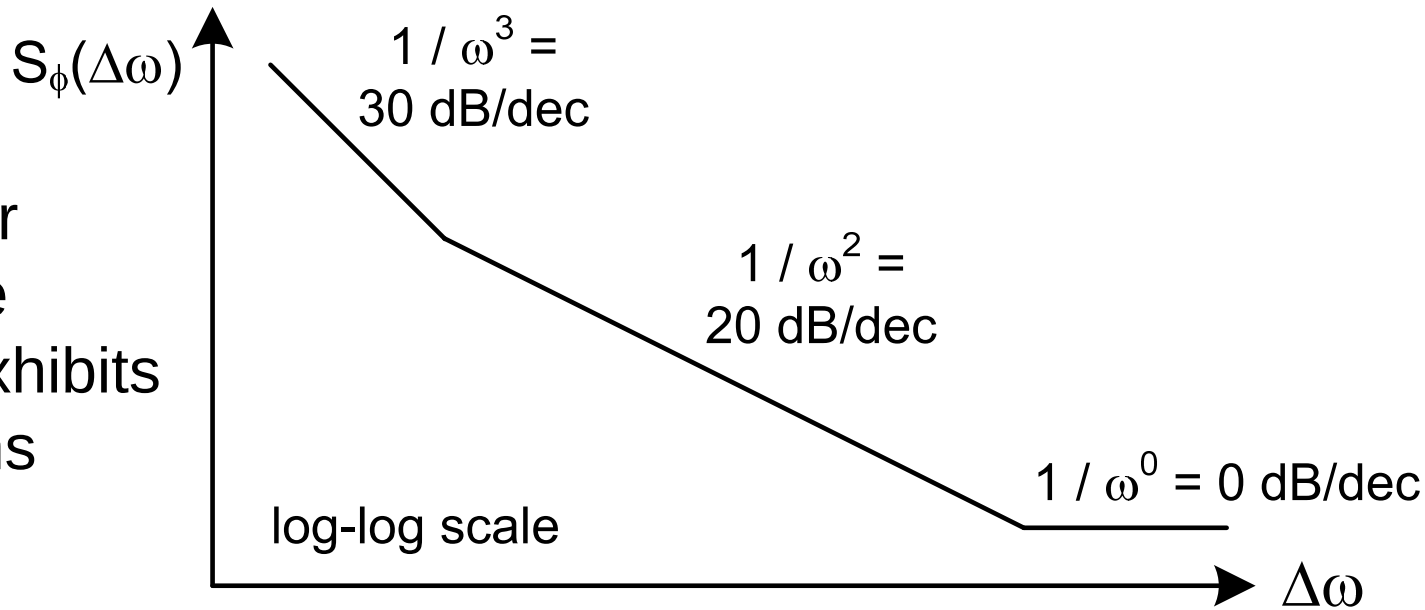

- Forces Δf through the PLL
- Measures steady-state ΔOTW

# Behavioral Simulation and Modeling

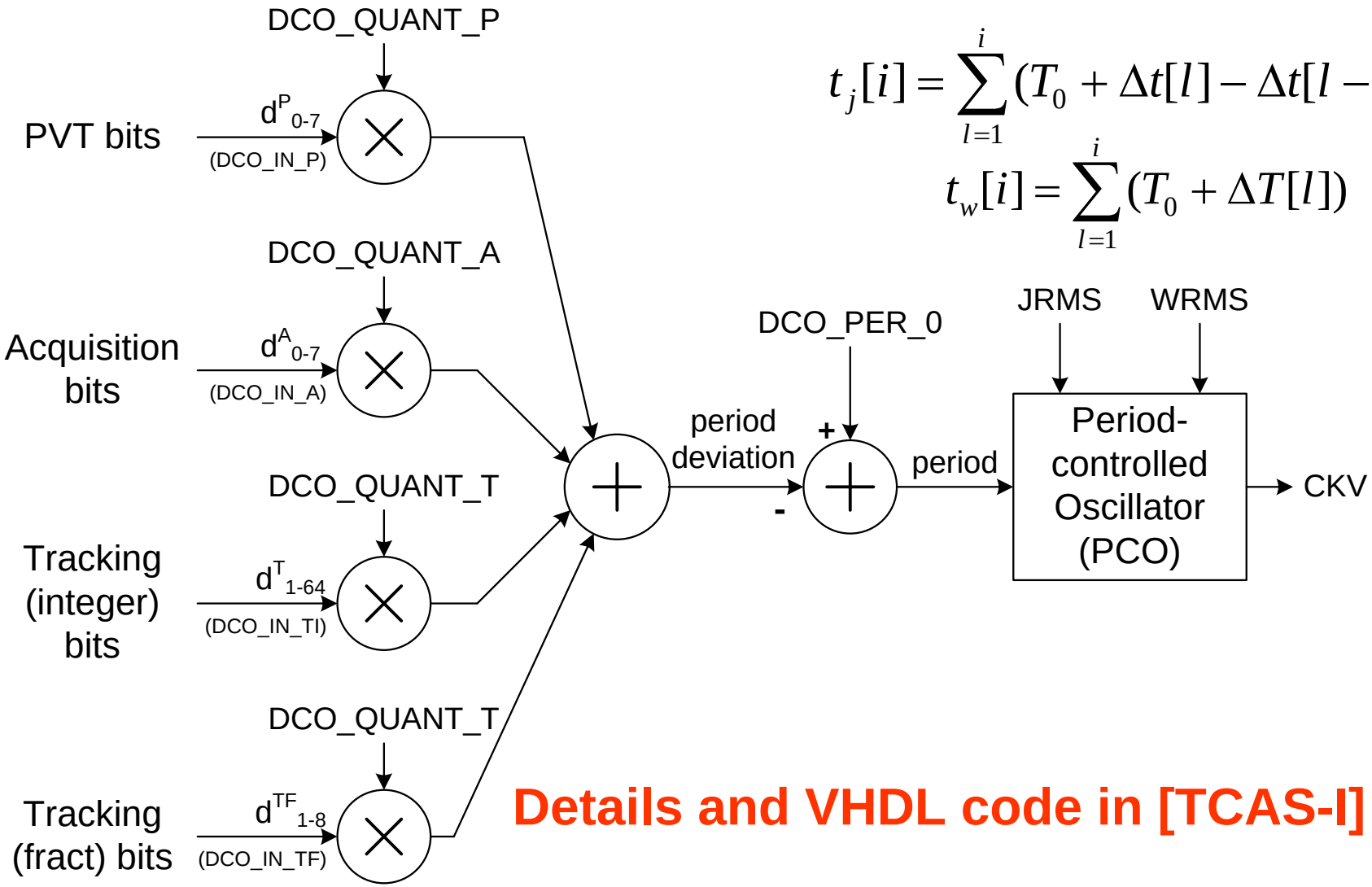
# VHDL Example: Phase Noise Model

- $1/\omega^0$: thermal noise added to the clock outside of the oscillator proper; does not affect the oscillation time base
- $1/\omega^2$: upconverted thermal (AWGN) noise; caused by uncorrelated timing fluctuations in the period of oscillation; modeled as random walk
- $1/\omega^3$: upconverted flicker (1/f) noise; significant in thin-oxide MOS transistors

- RF oscillator phase noise spectrum exhibits three regions



# DCO Time-domain VHDL Model



# SPICE and RF Tools Can't Handle…

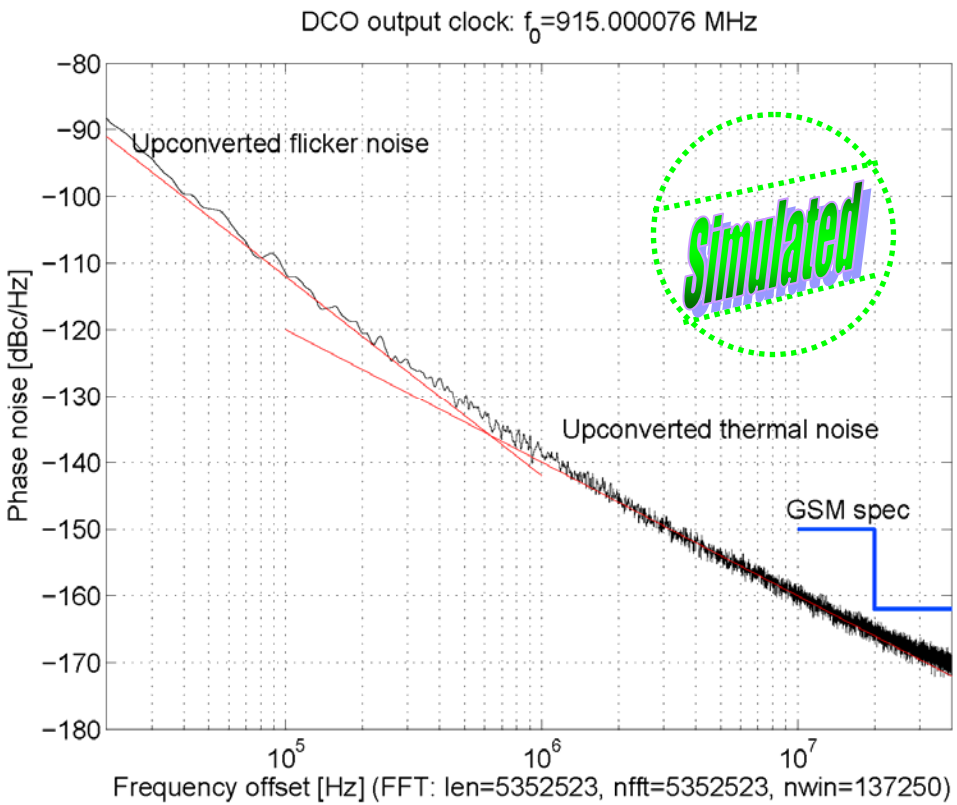
- "Laundry list" from [TCAS-I]
- Effect of the DCO phase noise on the PLL phase noise performance and generated spurs, especially when the PLL contains a higher-order digital loop filter and operates in fractional-*N* mode
- Effect of the DCO frequency resolution on the close-in phase noise of the PLL
- Effect of the SD DCO dithering on the far-out phase noise
- Effect of the varactor mismatches on the modulated spectrum
- Effect of the TDC resolution and nonlinearity on the close-in PLL phase noise performance and generated spurs
- Effect of the DPA resolution and nonlinearity on the RF output
- Effect of the DCO phase noise on the degradation of the signal-to-noise ratio in the direct RF sampling RX

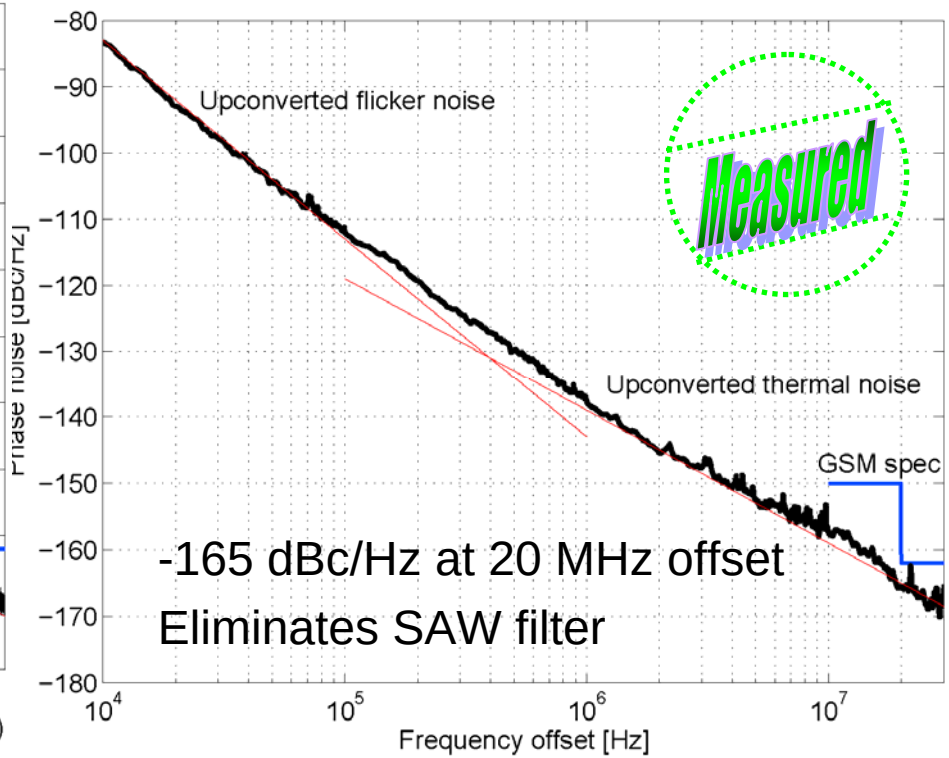
# CAD Challenges & Opportunities

- Unified modeling and simulation engine is a must
  - DRP uses an event-driven engine (standard VHDL) for RF, analog, digital, system, software (microcode)
  - SPICE and “analog/RF” simulation tools not useful at SoC level
  - Computation and disk space are inexpensive
  - VHDL RF/analog models include: amplitude noise, phase noise nonlinearities, distortion, charge-domain RX
  - Full SoC-level system validation
  - $1M for the 90nm mask set
- Reduce analog requirements by digital signal processing
- Include package and PCB models in simulations
  - Spurs, coupling, etc.

# Measured vs. Simulated Phase Noise

- Shows DCO upconverted 1/f and thermal noise
- Simulation matches the measurements!

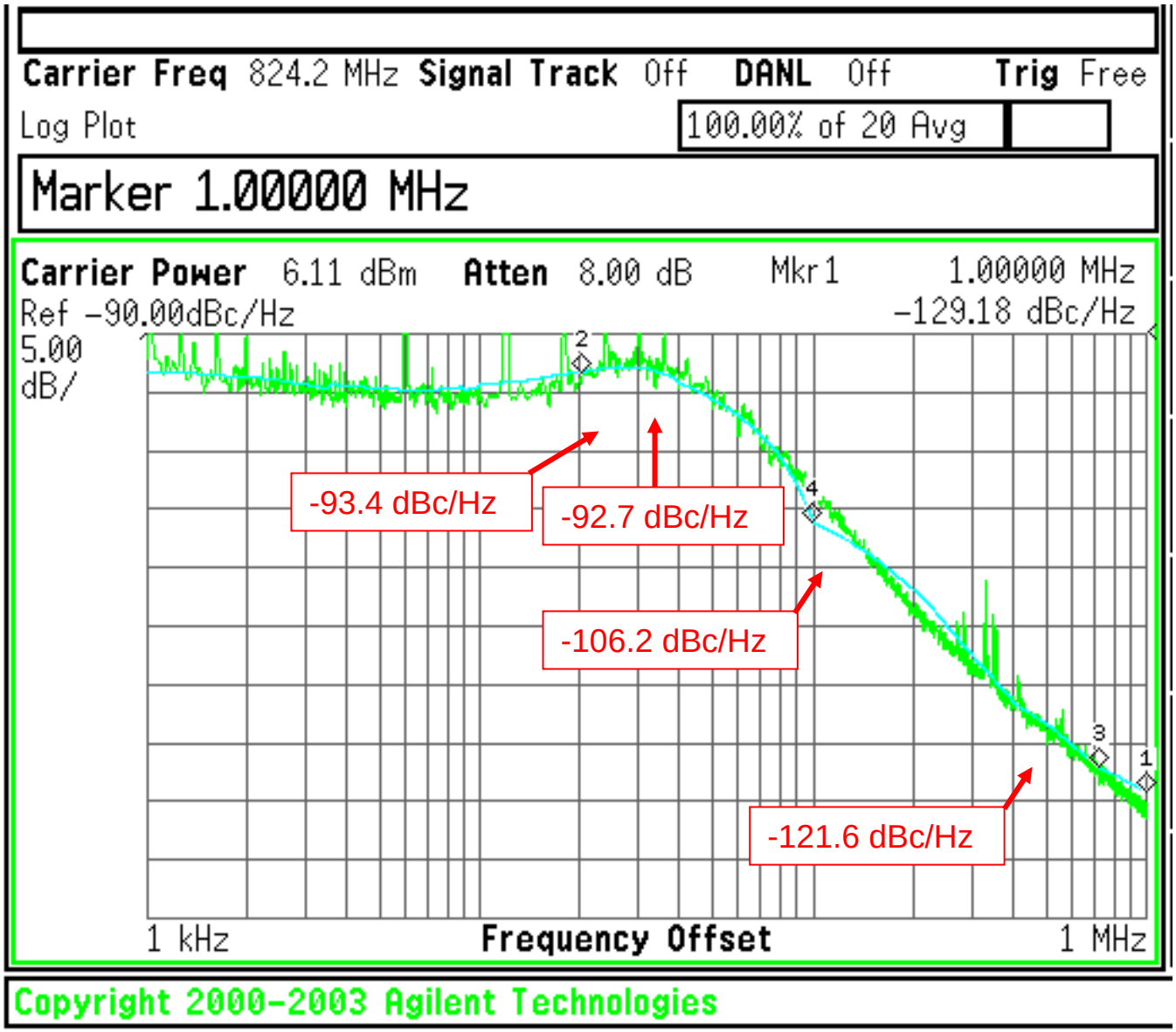


# Measured Results

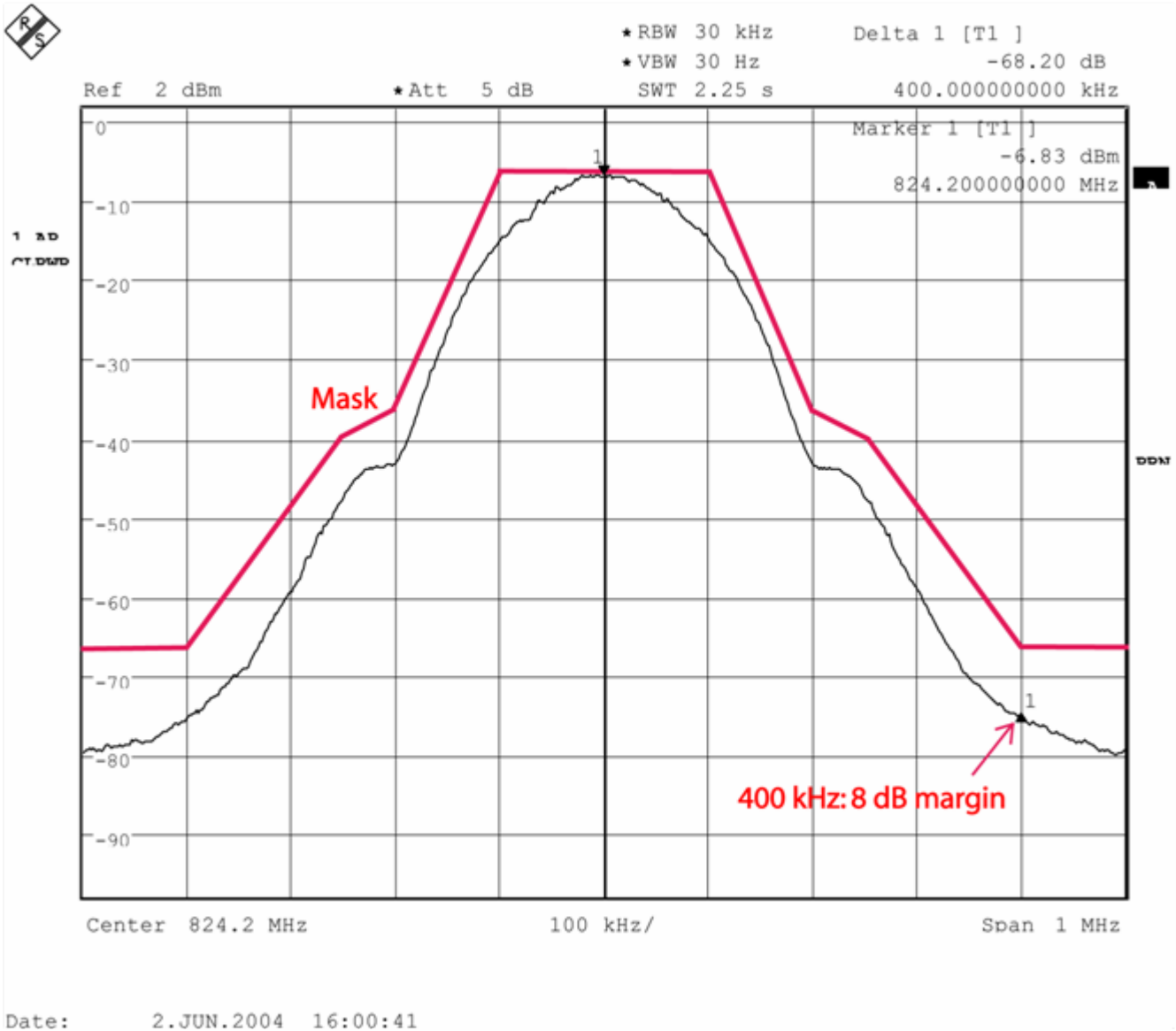
# Unmodulated Carrier Phase Noise

- 824.2 MHz carrier
- 26 MHz FREF
- -92…-95 dBc/Hz in-band phase noise
- 0.5 deg rms phase noise
  - Spec: 5 deg
- -122 dBc/Hz @ 400 kHz

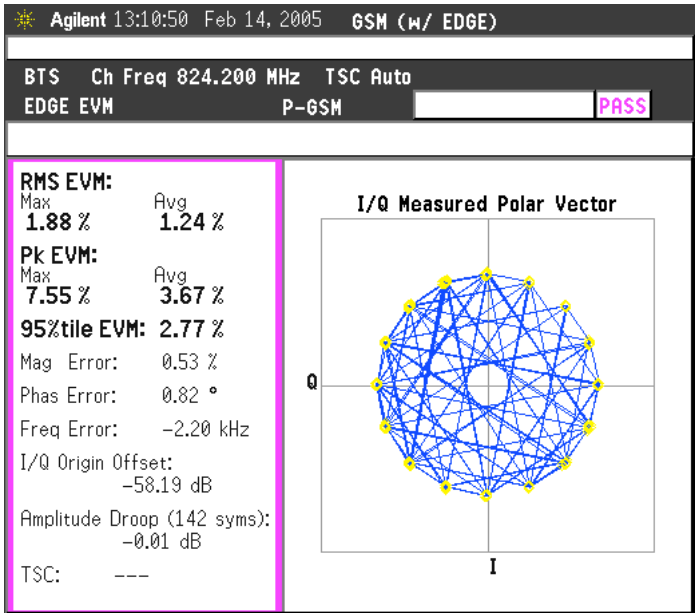


# Measured GSM Output Spectrum

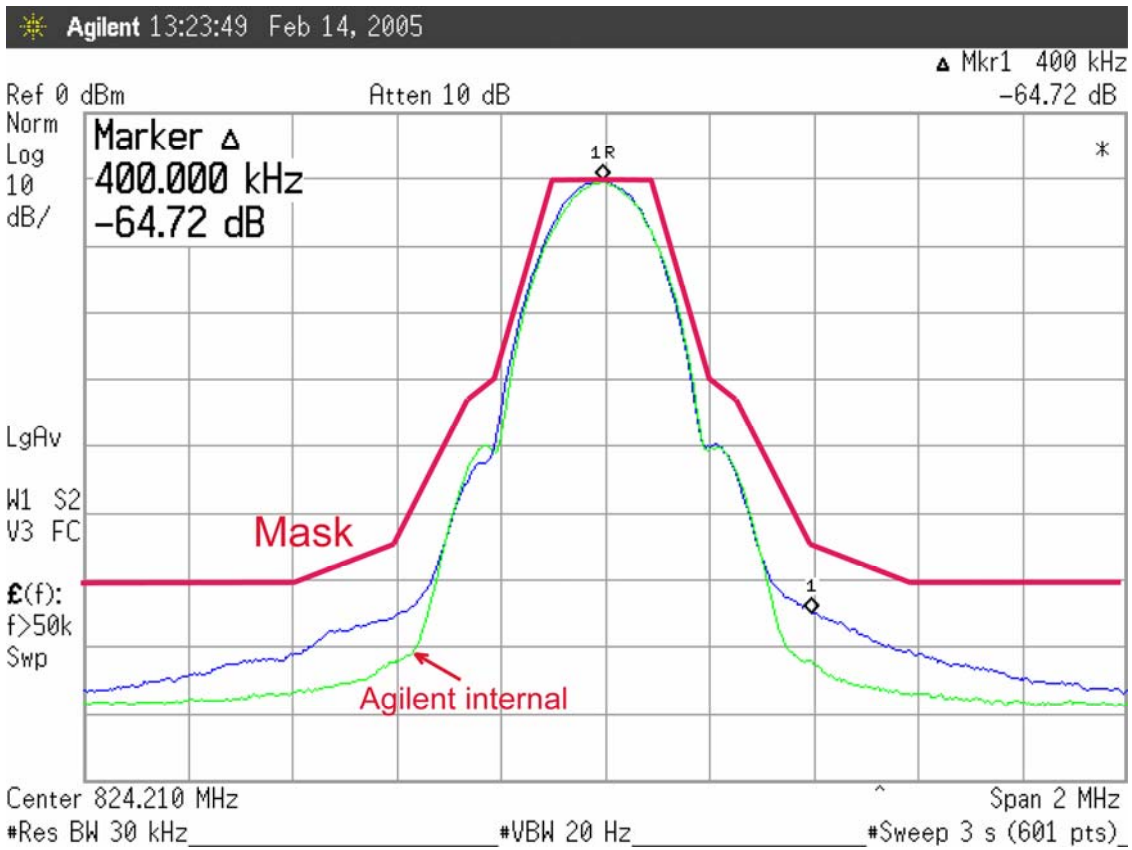
- Meets GSM spec
  - 8 dB margin @ 400 kHz
- Phase error
  - 1º rms (5º spec)
  - 3º peak (20º spec)



# Measured EDGE Modulation



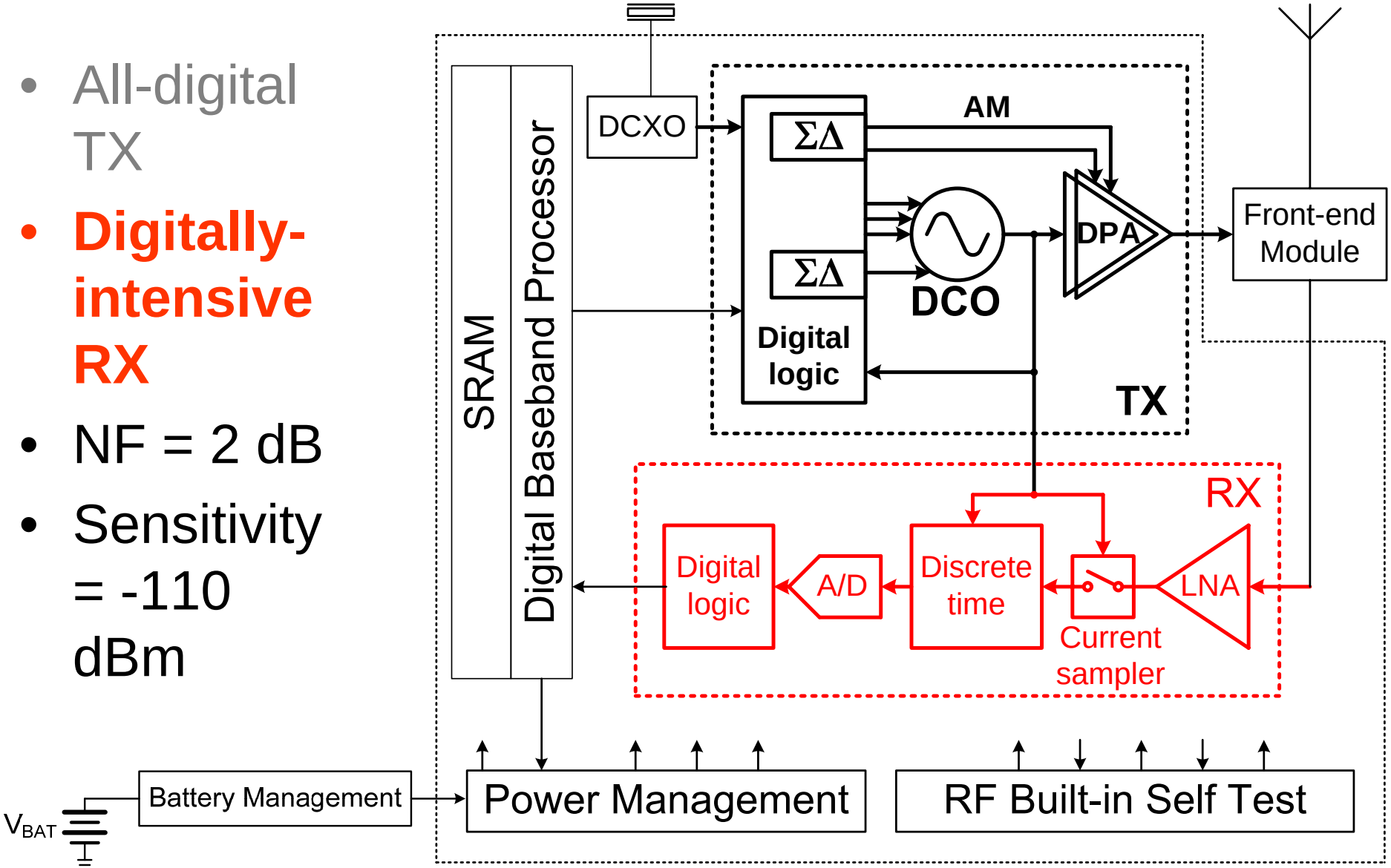

- Meets the spectral mask with 10 dB margin




- 1.24% meets the rms EVM spec of 9%
- 3.67% meets the peak EVM spec of 30%

# “Big Picture”: Single-Chip Cell Phone

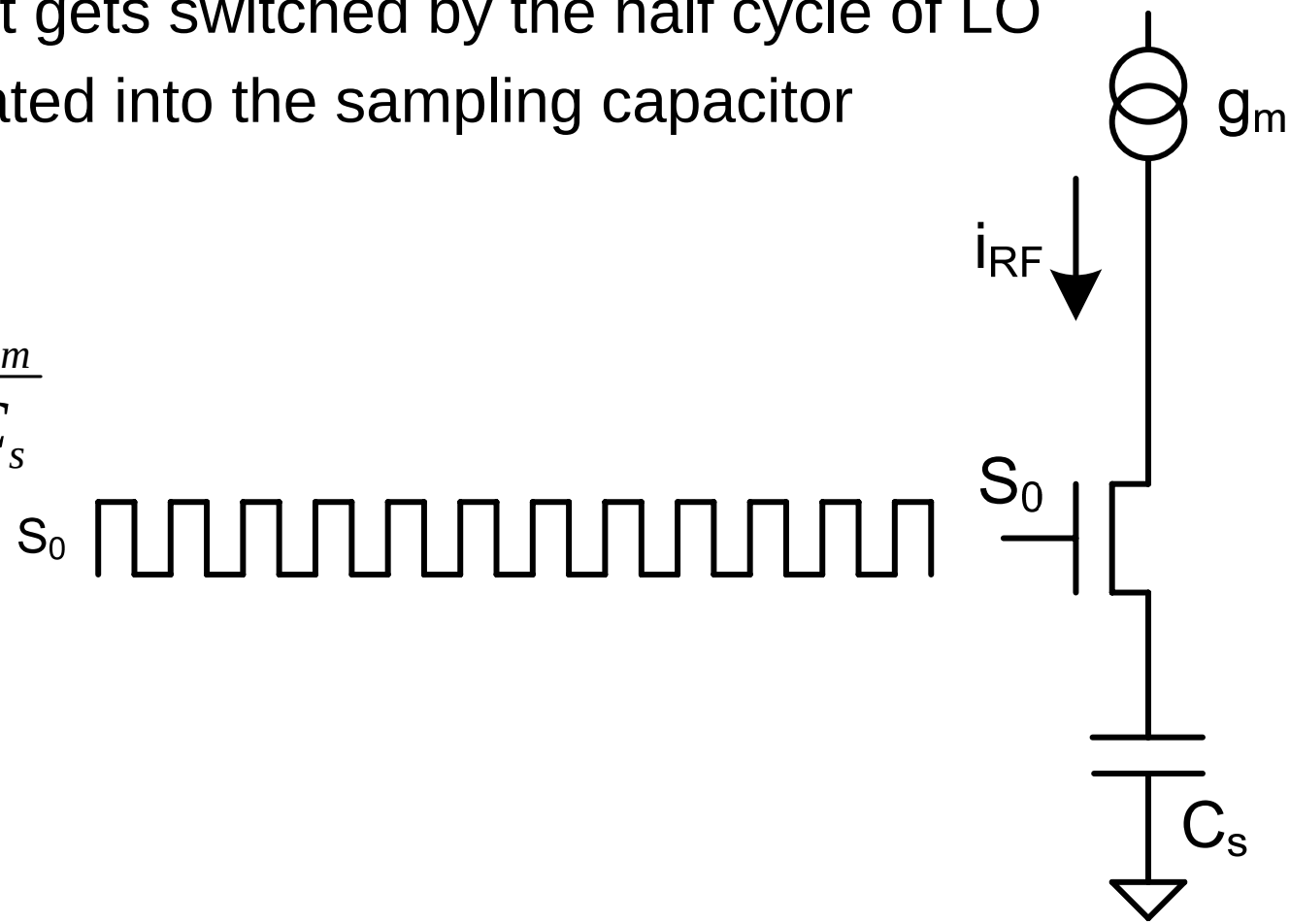
- All-digital TX
- **Digitally-intensive RX**
- NF = 2 dB
- Sensitivity = -110 dBm



# Direct Sampling Mixer

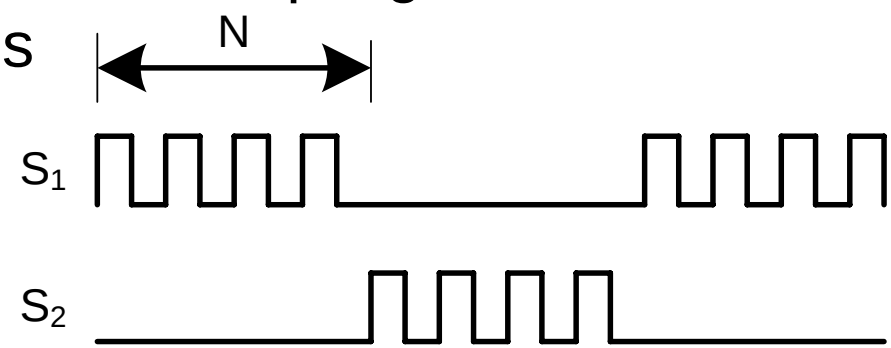
- Low-noise transconductance amplifier $g_m$ converts the RF voltage into RF current
- The RF current gets switched by the half cycle of LO
- Charge integrated into the sampling capacitor
- Voltage gain:

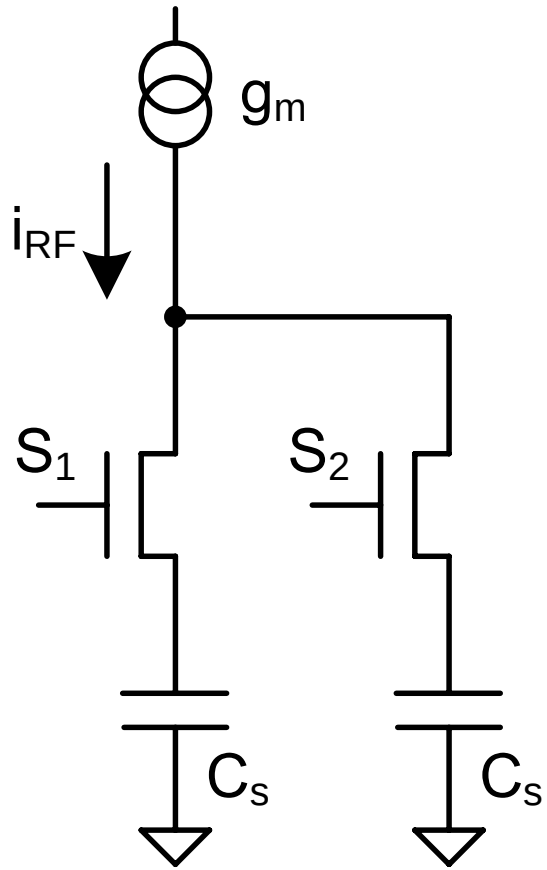
$$G_{v,RF} = \frac{1}{\pi} \cdot \frac{1}{f_0} \frac{g_m}{C_s}$$



# Temporal Moving Average

- Continuous accumulation of charge is not practical
  - Cannot read it out
  - Must prevent an overflow
- Integration window fixed
- Charge readout and discharge
- Rotation of RF sampling and readout operations



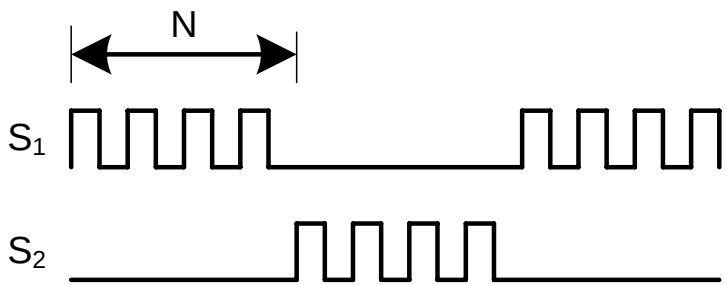



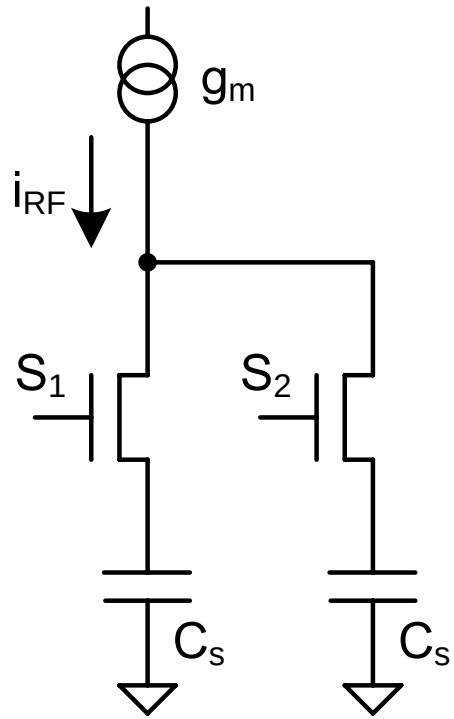
# Temporal Moving Average

- Temporal integration of N half-rectified RF samples
- FIR filter with all-ones coefficients
- Sinc transfer function in the frequency domain
- Charge accumulation done on the same capacitor
  - Very exact transfer function

$$w_i = \sum_{0}^{N-1} u_{i-l}$$

$$R_{eq} = \frac{1}{f_0 / N \cdot C_R}$$



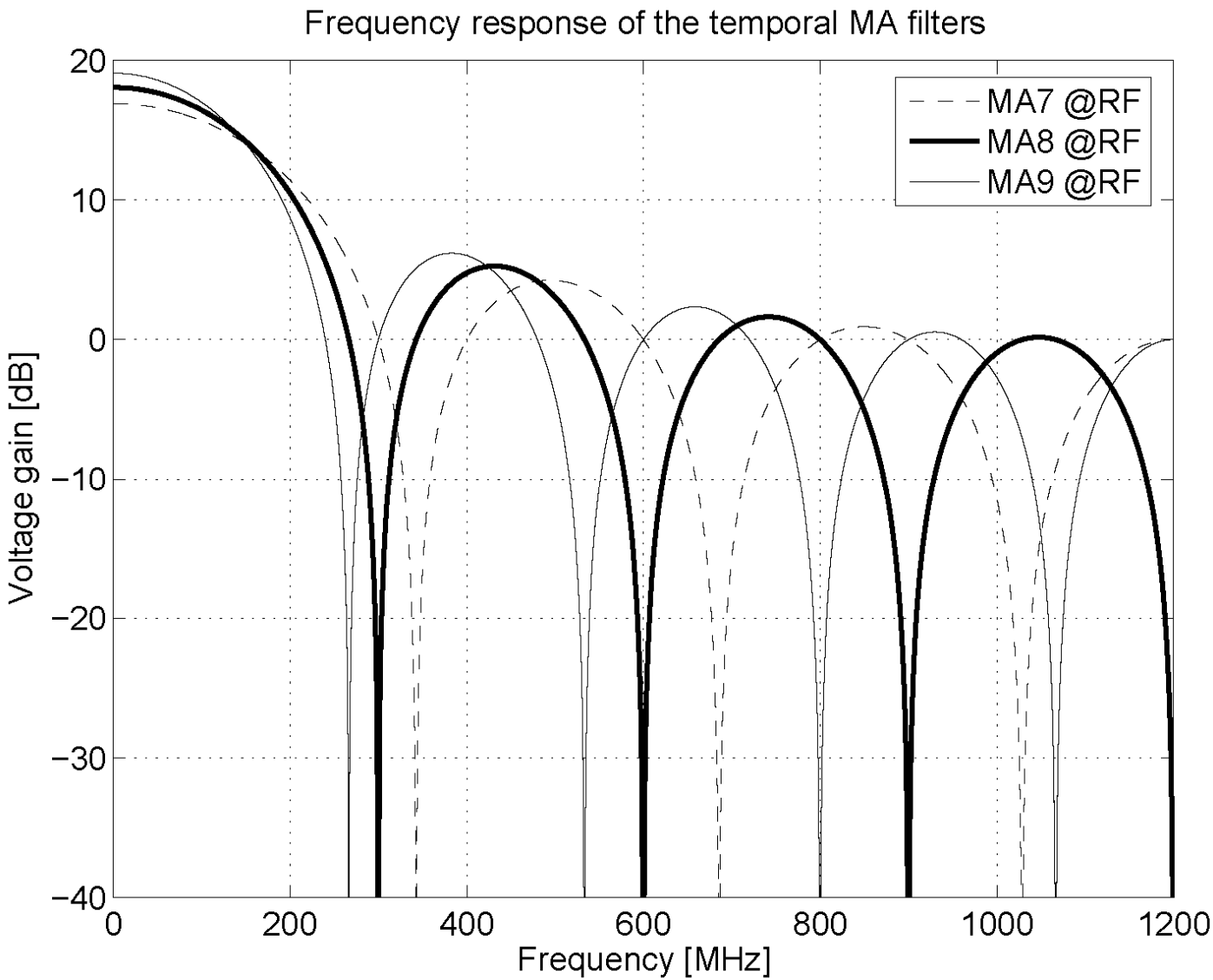




- Charge and voltage gains

$$G_{q,tma} = G_{v,tma} = N$$

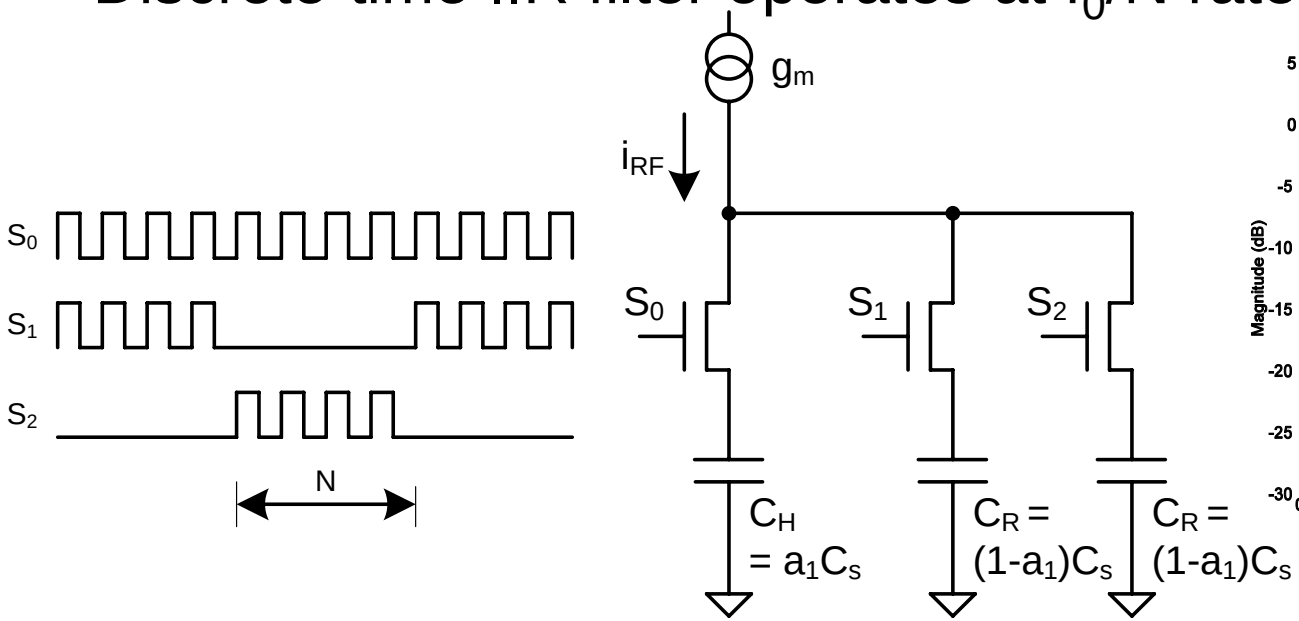
# Transfer Function of TMA

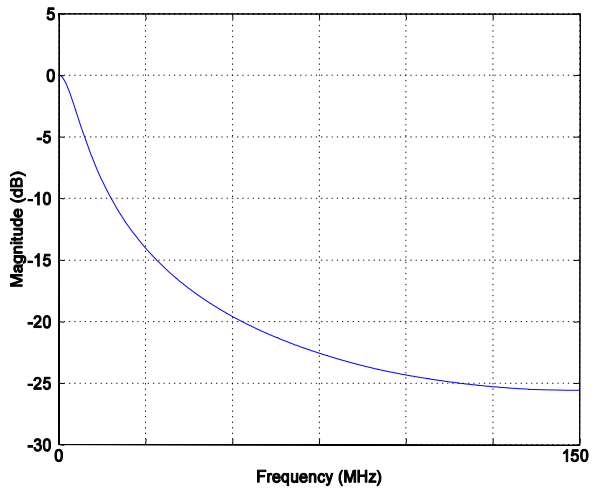
- Example N: 7,8,9
- TMA output read out at a lower rate
- Aliasing with foldover at $f_0/2N$



# IIR Filtering

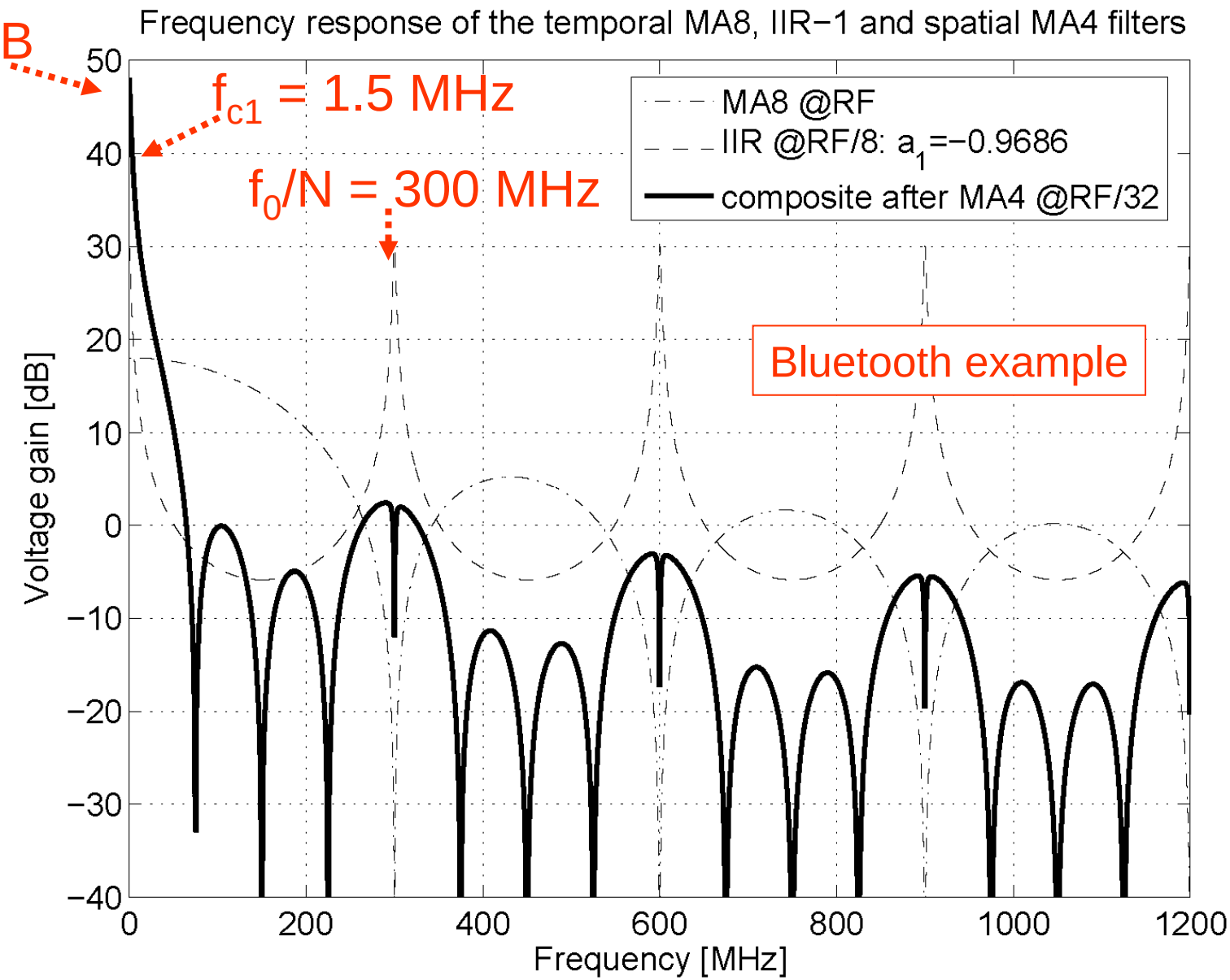
- Splitting of $C_s$ into $C_H$ and $C_R$ creates first order IIR filter
- IIR filtering much stronger than FIR
- $C_s = C_H + C_R$
- One $C_R$ is used for RF integration
- The other $C_R$ is used for readout
- Discrete-time IIR filter operates at $f_0/N$ rate



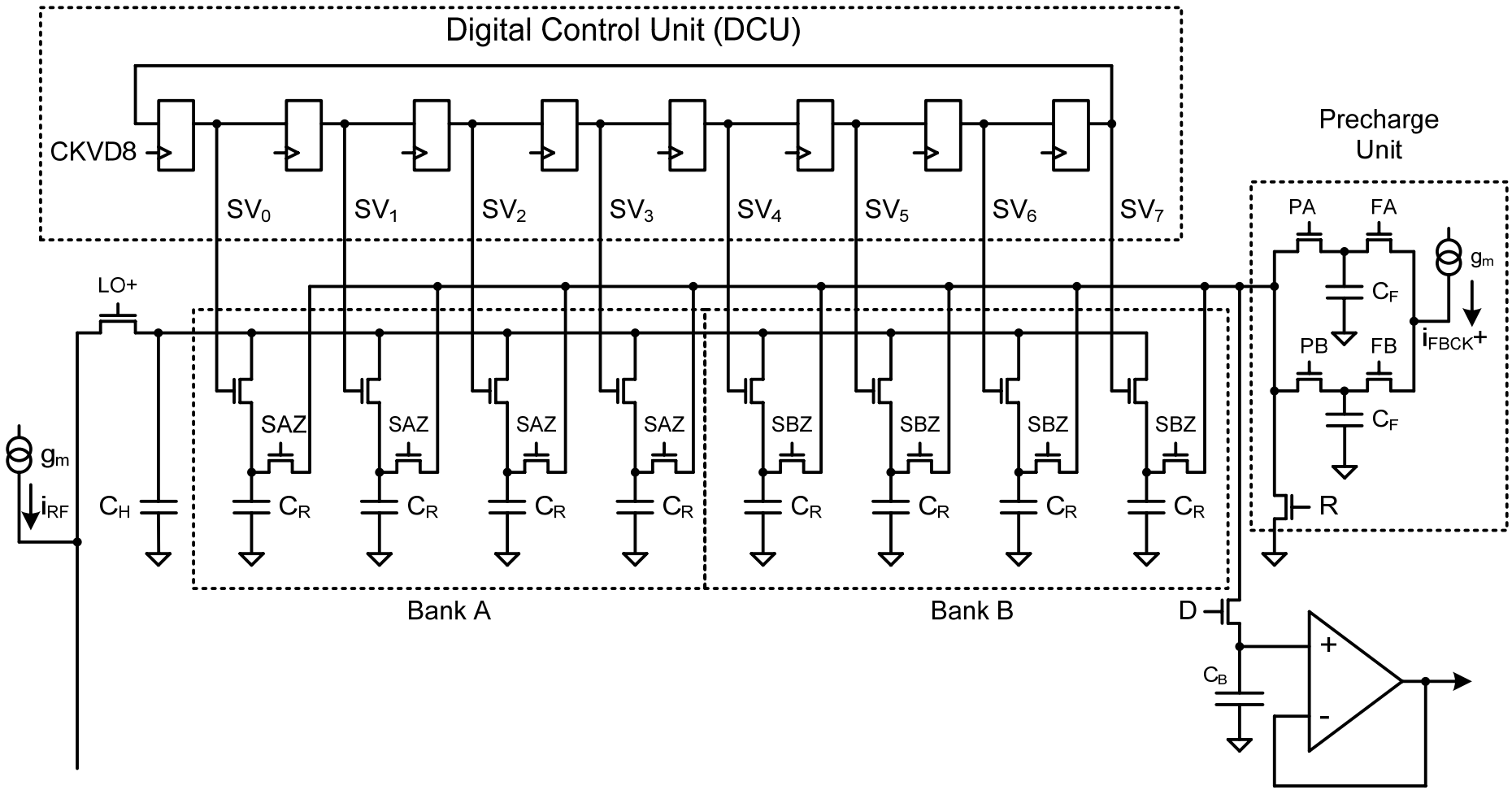



# Composite Filter Response

$G_{V,tot}$ = 48 dB

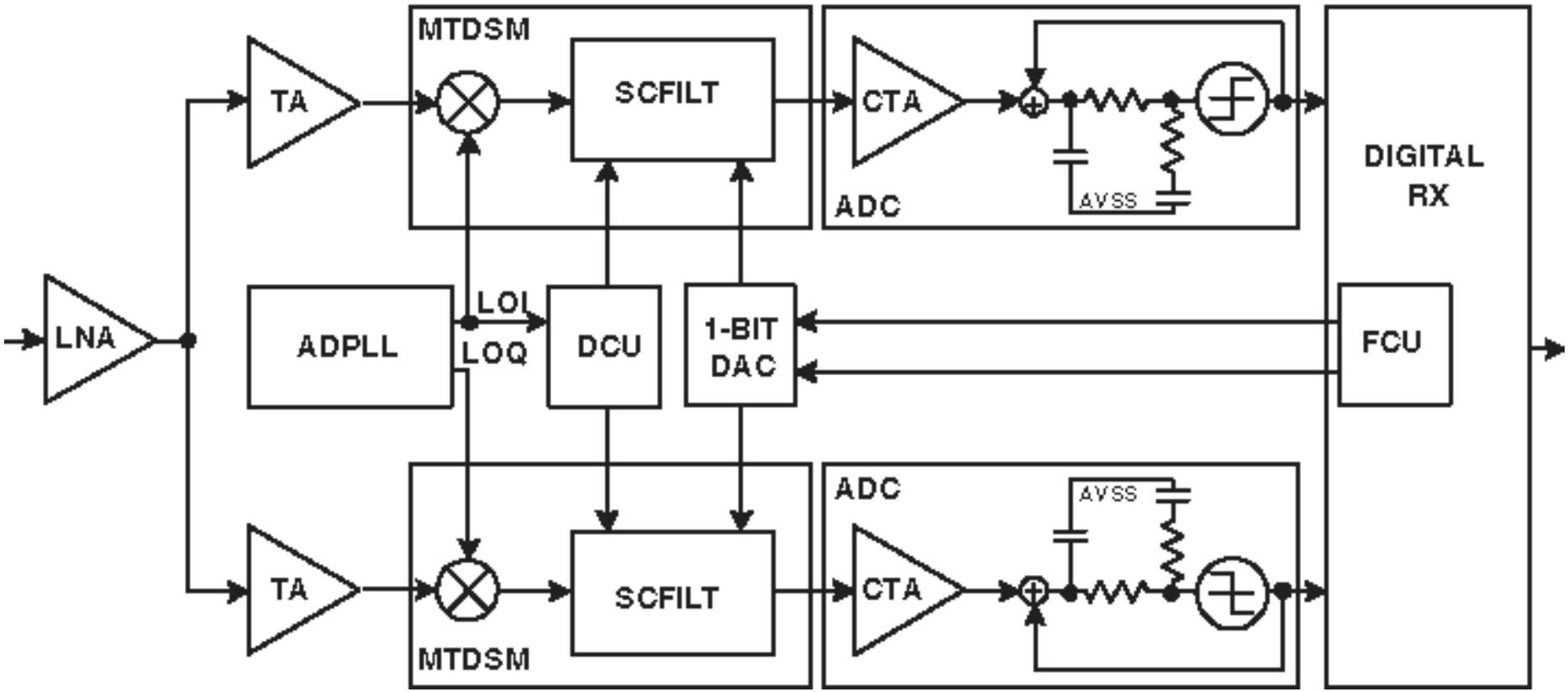


# Multi-tap Direct Sampling Mixer



# GSM Receiver Front-End

- RF front-end: LNA, MTDSM, ADC
- Feedback system
- Digital back-end

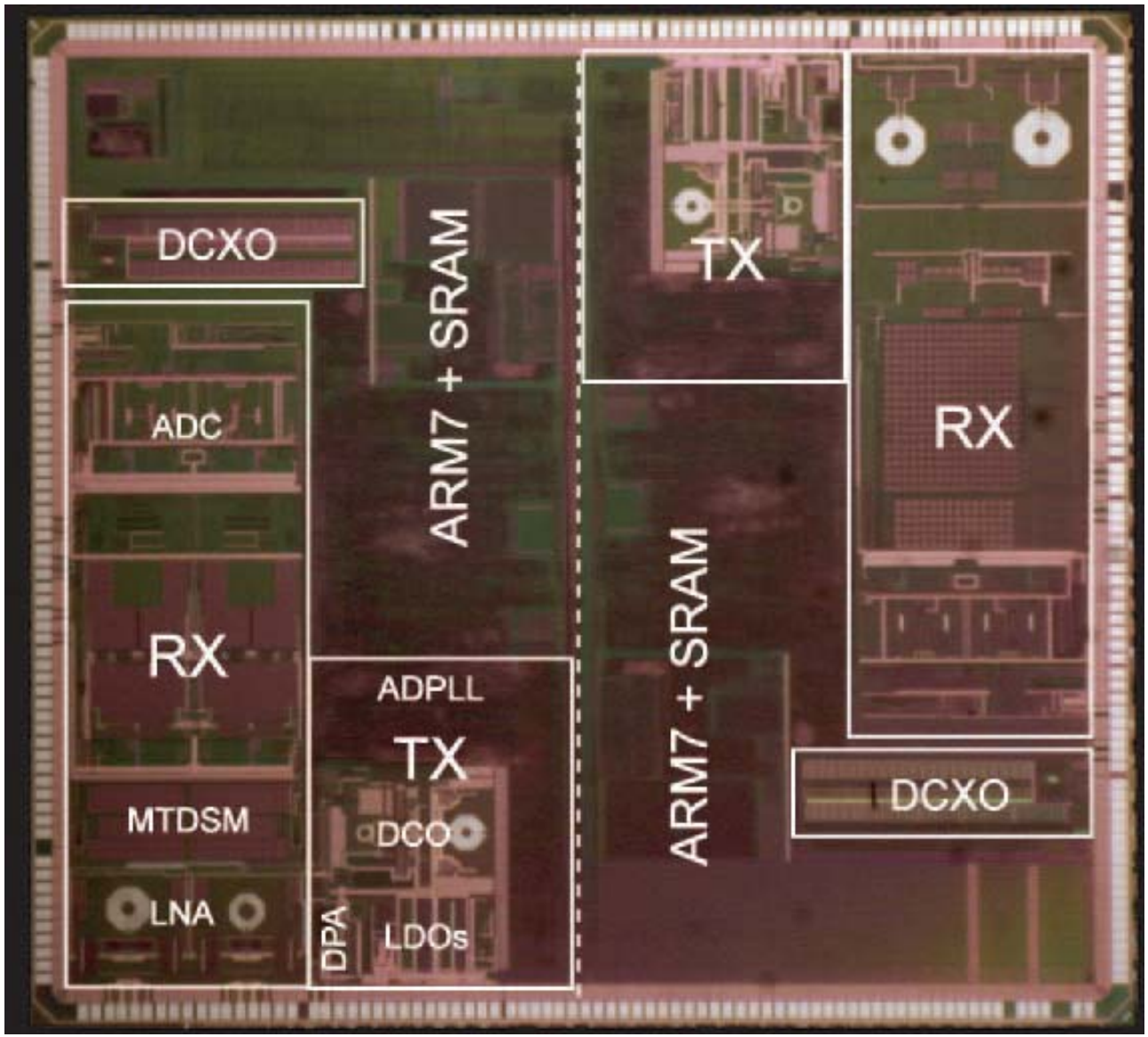


# Implementation

- Digital deep-submicron 90-nm CMOS process with no analog extensions
- RF, analog, mixed-signal integrated with digital and memory

| | |
|---|---|
| Interconnect material | copper |
| Minimum metal pitch | 0.27 um |
| Metal levels | 5 |
| Core transistor nom. voltage | 1.2 V |
| Gate oxide | 2.6 nm |
| Logic gate density | 240 kgates / $mm^2$ |
| 6-transistor SRAM cell | 1 Mbits / $mm^2$ |

# Single-chip GSM Transceiver




- 90 nm CMOS
- Preproduction version of the single-chip GSM radio
- Two pairs of TX & RX
  - Investigation of noise coupling for WCDMA
- Transceiver: ~7 $mm^2$
- January 2004: 1st cellular phone call

# For More Info on TX…

[1] R. B. Staszewski, C.-M. Hung, D. Leipold, et al., “A first multigigahertz digitally controlled oscillator for wireless applications,” *IEEE Trans. on Microwave Theory and Techniques*, vol. 51, no. 11, pp. 2154–2164, Nov. 2003.
[2] R. B. Staszewski, D. Leipold, K Muhammad, et al., “Digitally controlled oscillator (DCO)-based architecture for RF frequency synthesis in a deep-submicrometer CMOS process,” *IEEE Trans. on Circuits and Systems II*, vol. 50, no. 11, pp. 815–828, Nov. 2003.
[3] R. B. Staszewski, K. Muhammad, D. Leipold, et al., “All-digital TX frequency synthesizer and discrete-time receiver for Bluetooth radio in 130-nm CMOS,” *IEEE Journal of Solid-State Circuits*, vol. 39, iss. 12, pp. 2278–2291, Dec. 2004.
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[5] R. B. Staszewski and P. T. Balsara, “Phase-domain all-digital phase-locked loop,” *IEEE Trans. on Circuits and Systems II*, vol. 52, no. 3, pp. 159–163, Mar. 2005.
[6] R. B. Staszewski, J. Wallberg, S. Rezeq, et al., “All-digital PLL and transmitter for mobile phones,” *IEEE Journal of Solid-State Circuits*, vol. 40, iss. 12, pp. 2469–2482, Dec. 2005.

# For More Info on RX…

[1] K. Muhammad, D. Leipold, B. Staszewski, et al., “A discrete-time Bluetooth receiver in a 0.13mm digital CMOS process,” *Proc. of IEEE Solid-State Circuits Conf.*, pp. 268–269, 527, Feb. 2004.
[2] K. Muhammad and R. B. Staszewski, “Direct RF sampling mixer with recursive filtering in charge domain,” *Proc. of 2004 IEEE Intl. Symp. on Circuits and Systems*, pp. I-577—I-580, May 2004.
[3] K. Muhammad, R. B. Staszewski, and C.-M. Hung, “Joint common mode voltage and differential offset voltage control scheme in a low-IF receiver,” *Proc. of 2004 IEEE Radio Frequency Integrated Circuits (RFIC) Symp.*, pp. 405–408, June 2004.
[4] R. B. Staszewski, K. Muhammad, D. Leipold, et al., “All-digital TX frequency synthesizer and discrete-time receiver for Bluetooth radio in 130-nm CMOS,” *IEEE Journal of Solid-State Circuits*, vol. 39, iss. 12, pp. 2278–2291, Dec. 2004.
[5] K. Muhammad, Y.-C. Ho, T. Mayhugh, et al., “A discrete time quad-band GSM/GPRS receiver in a 90nm digital CMOS process,” *Proc. of 2005 IEEE Custom Integrated Circuits Conf.*, sec. 28-5, pp. 809–812, Sept. 2005.
[6] K. Muhammad, R. B. Staszewski, and D. Leipold, “Digital RF processing: toward low-cost reconfigurable radios,” *IEEE Communications Magazine*, vol. 43, no. 8, pp. 105–113, Aug. 2005.

# Conclusions

- Presented Digital RF Processor (DRP)
- Part I: All-digital TX
  - Based on all-digital PLL (ADPLL)
  - ADPLL features wideband frequency modulation
  - Two modulators: DFC and DRAC
- Part II: Direct sampling discrete-time RX
- All-digital and digitally-intensive architecture in deep-submicron CMOS can replace traditional RF circuits
- Performance demonstrated in a commercial single-chip GSM radio