Research on Extending and Surpassing the Limits of CMOS

IEEE Circuits and Systems Society

DFW Chapter 3/07 Seminar

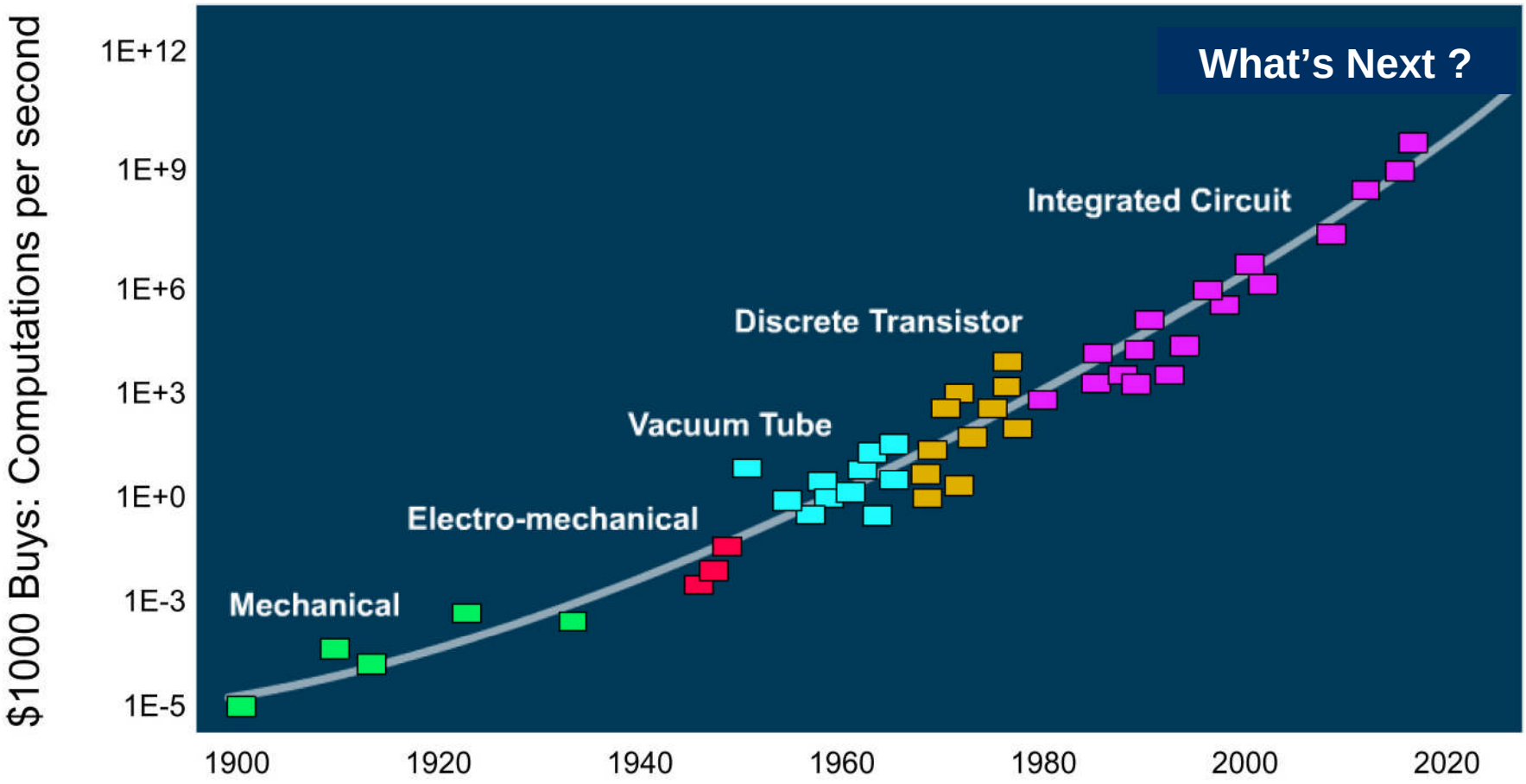
Dallas, Texas

March 21, 2007

Dr. Robert Doering

Texas Instruments

Miniaturization ("Scaling" today) has driven multiple eras of information technology



Smaller Components → Cheaper, Faster, More Energy-Efficient Systems

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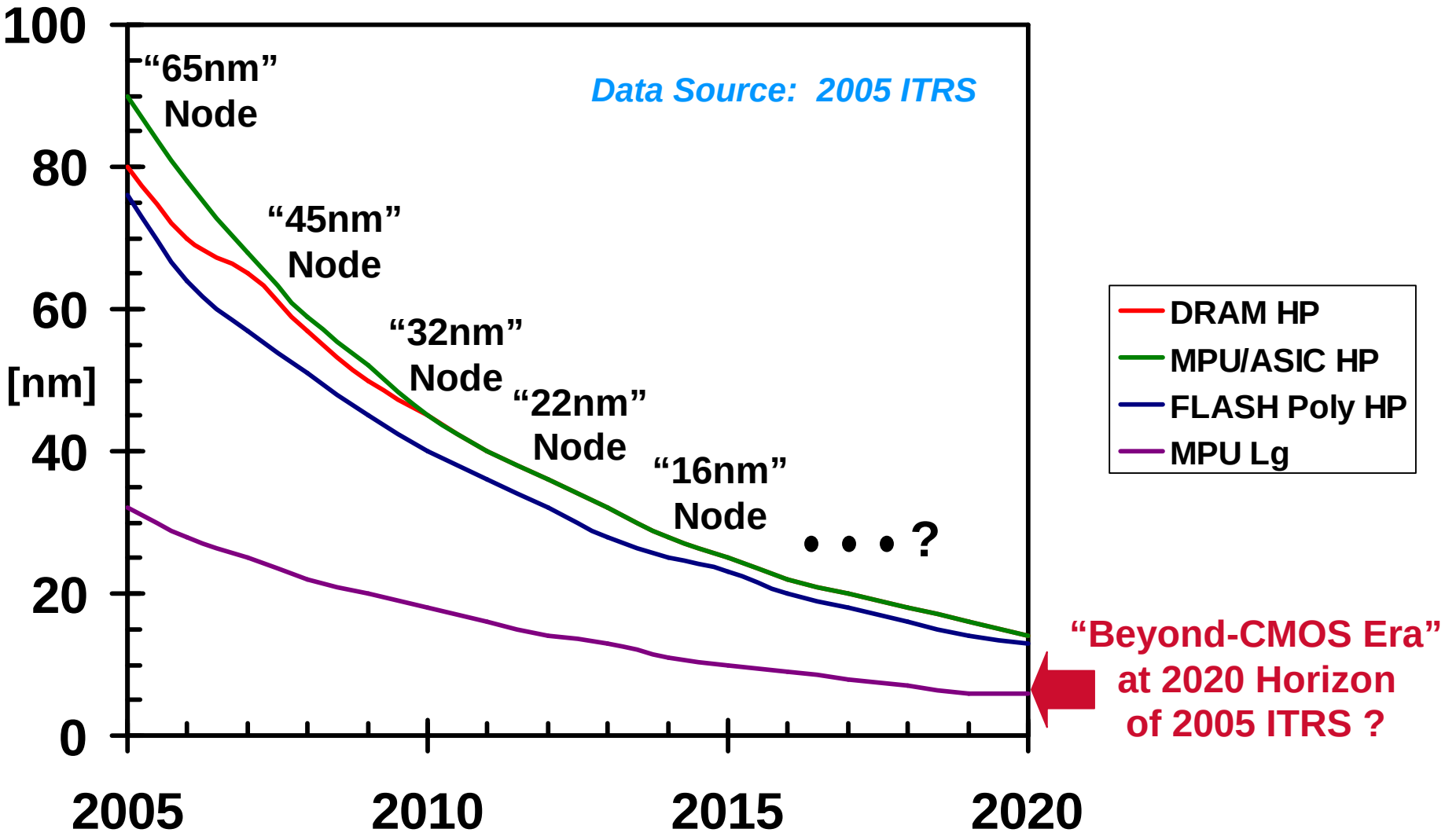
Source: Ray Kurzweil

CMOS Scaling as "Technology Nodes"



How long can we continue to scale CMOS ?

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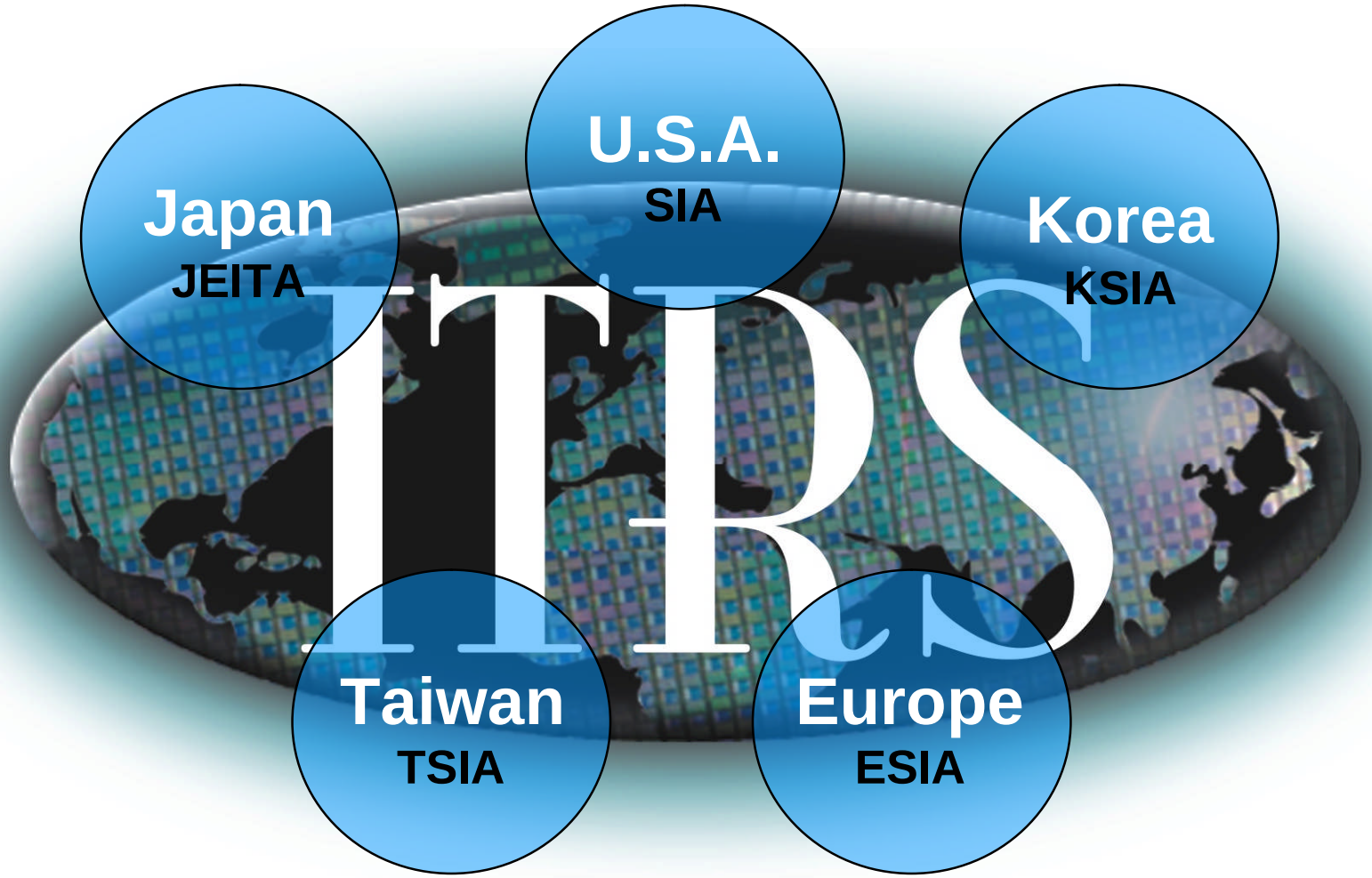
International Consensus Building on Future IC Technology Challenges



First – identify and categorize the R&D needs

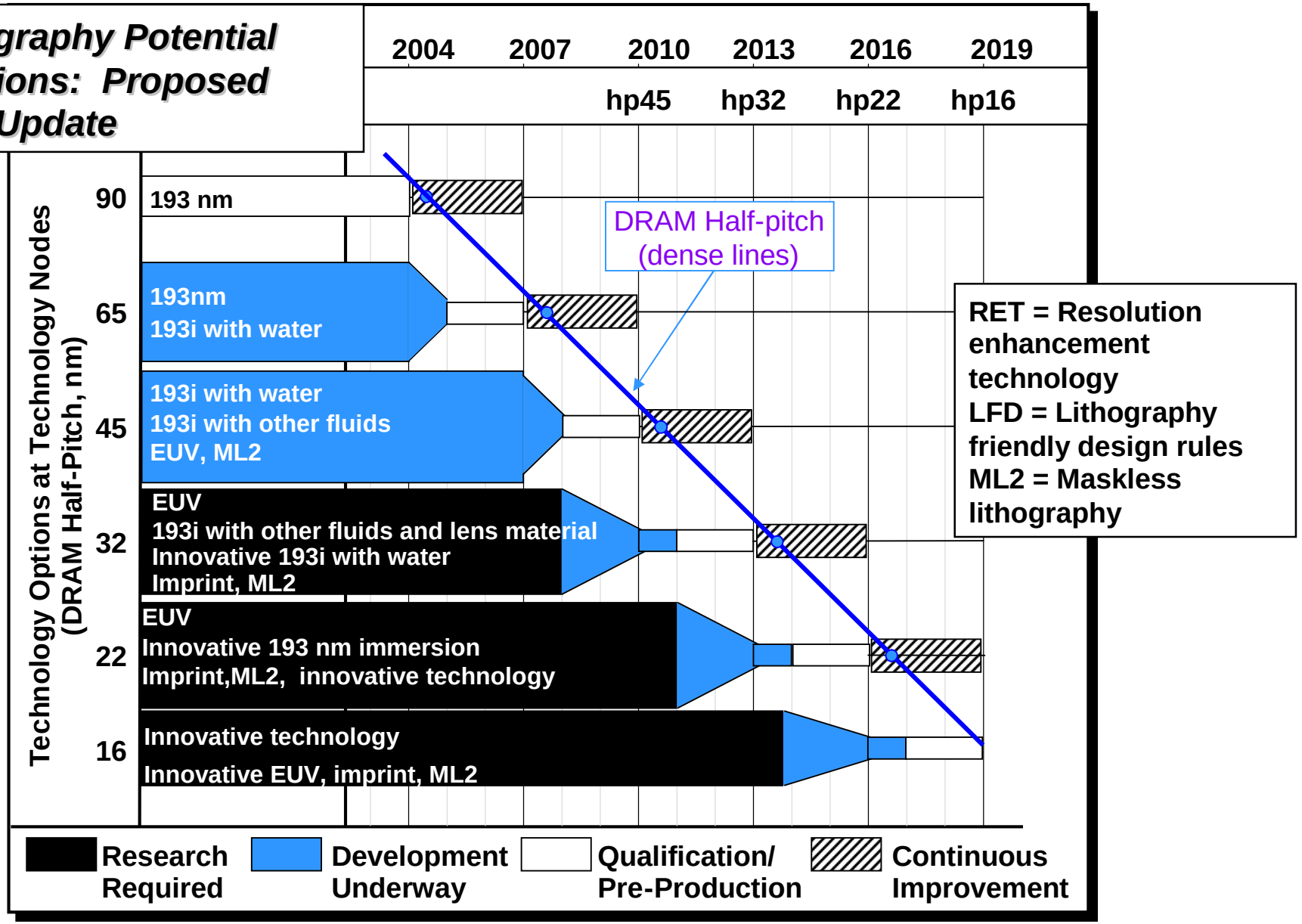
ITRS Methodology

for highlighting challenges/opportunities

Production Year:	2001	2004	2007	2010	2013	2016 …
DRAM Half-Pitch [nm]:	130	90	65	45	32	22
Overlay Control [nm]:	45	32	16	11	8	5.5
Gate Length [nm]:	65	37	25	18	13	9
CD Control [nm]:	6.3	3.3	2.6	1.9	1.3	0.9
T_{OX} (equivalent) [nm]:	1.3-1.6	1.2	1.1	0.65	0.5 (UTB)	0.5 (MUG)
I_{ON} (NMOS) [µA/µm]:	900	1110	1200	2050	2198	2713
I_{OFF} (NMOS) [µA/µm]:	0.01	0.05	0.2	0.28	0.29	0.11
Interconnect K_{EFF}:	-	3.1-3.6	2.7-3.0	2.5-2.8	2.1-2.4	1.9-2.2

values from the 2001, 2004, and 2005 editions of the ITRS

Lithography Potential Solutions: Proposed 2005 Update



Notes: RET and lithography friendly design rules will be used with all photon projection lithography solutions, including with immersion; therefore, it is not explicitly noted.

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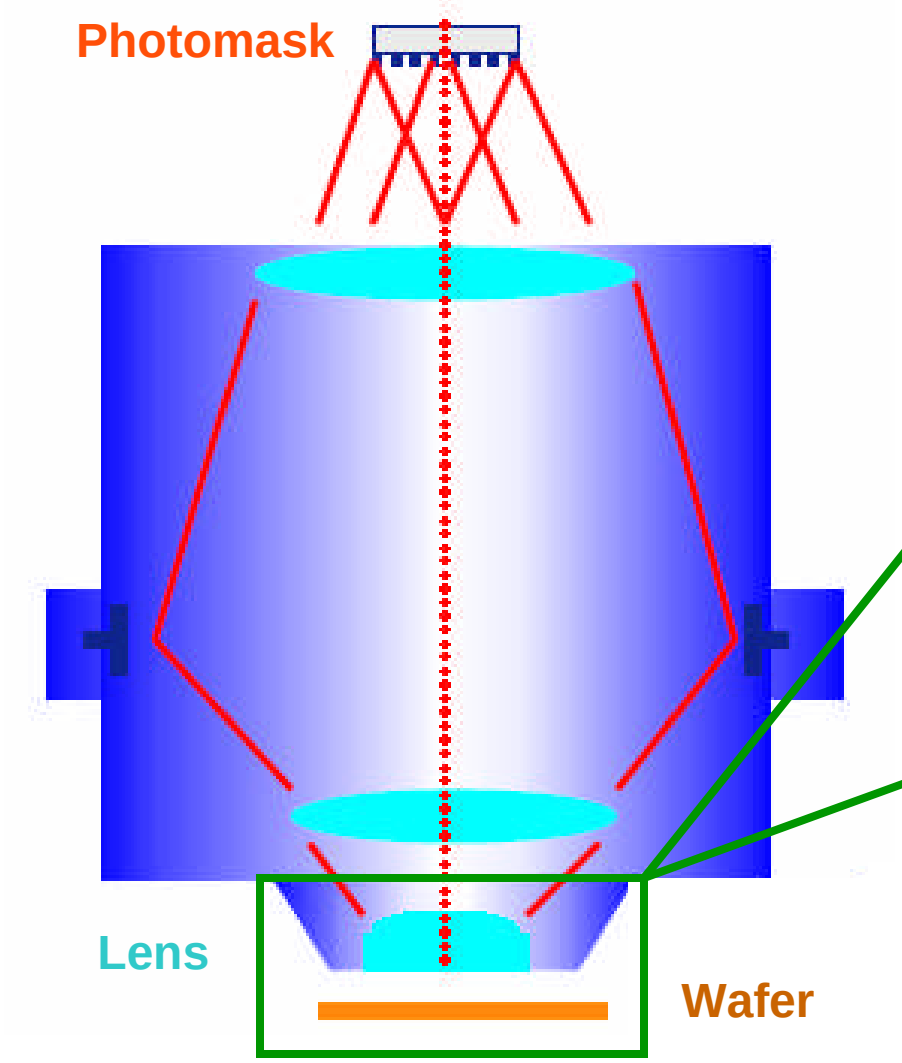
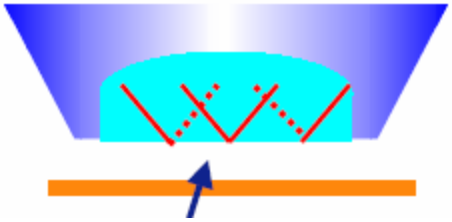
Source: 2005 ITRS

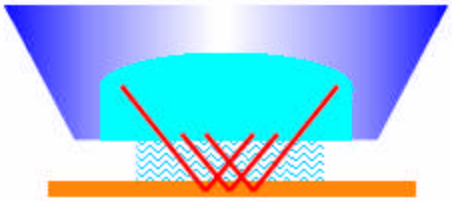
"Immersion Lithography"

A Solution for Patterning at 45, 32 and 22nm Nodes





DRY: High-angle light rays are internally reflected. Image information is lost.



IMMERSION: Water inserted btw lens and wafer. Image quality is improved.

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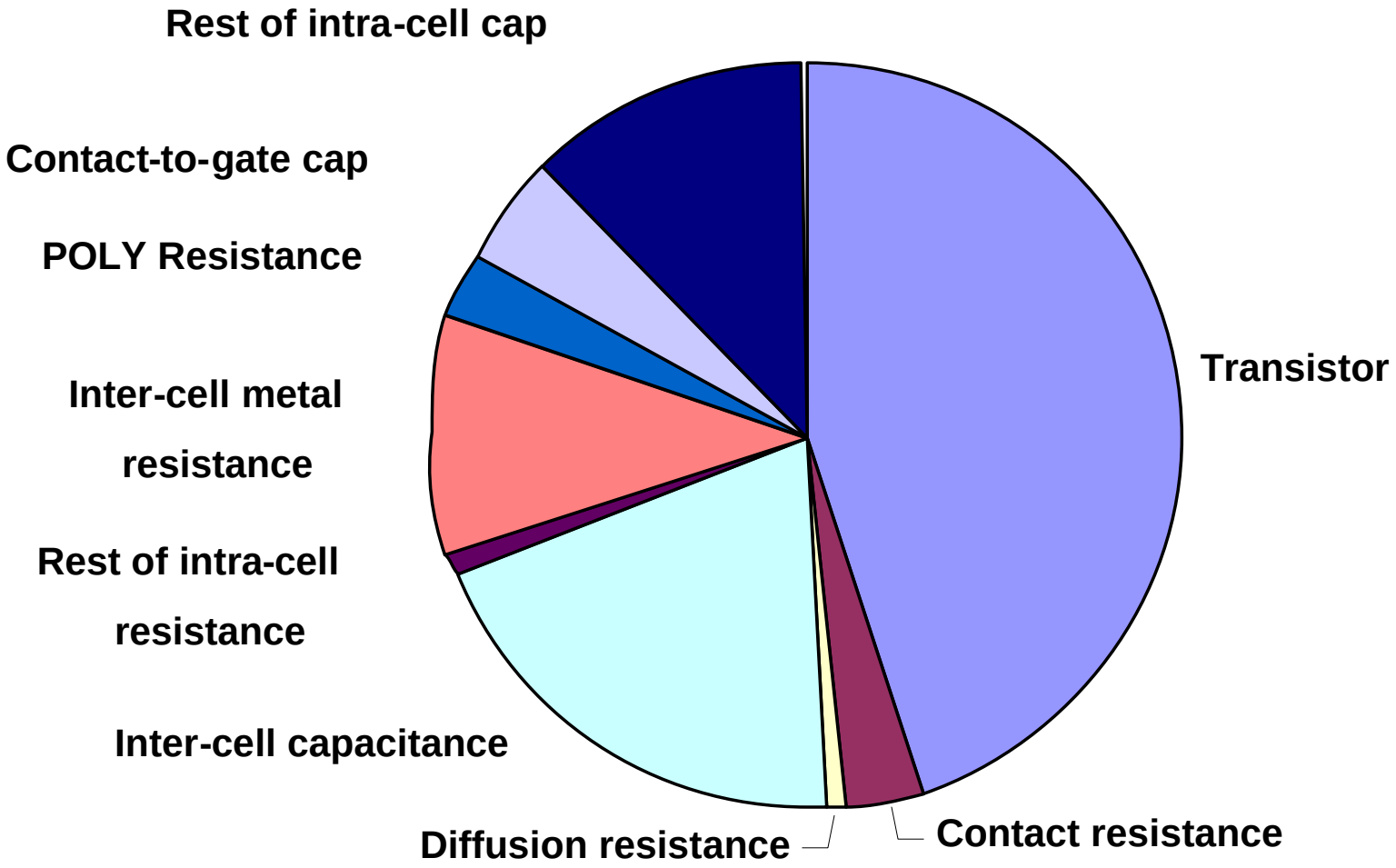
Scaling is limited by more than just lithography !

- **Growing Significance of Non-Ideal Device-Scaling Effects:**
  - **I_{ON} vs. I_{OFF} tradeoff**
  - **unfavorable ρ and length scaling for interconnects**
- **Approaching Limits of Materials Properties**
  - **Heat removal and temperature tolerance**
  - **C_{MAX} vs. leakage tradeoff for gate dielectric**
  - **C_{MIN} vs. mechanical-integrity tradeoff for inter-metal dielectric**
- **Increases in Manufacturing Complexity/Control Requirements**
  - **cost and yield of increasingly complex process flows**
  - **metrology and control of L_{GATE}, T_{OX}, doping, etc.**
- **Affordability of R&D Costs**
  - **development of more complex and "near cliff" technologies**
  - **design of more complex circuits with "less ideal" elements**

IC Performance: Transistors & Wires

At 65-nm, the speed of typical dense logic is about equally limited by transistor and wire performance



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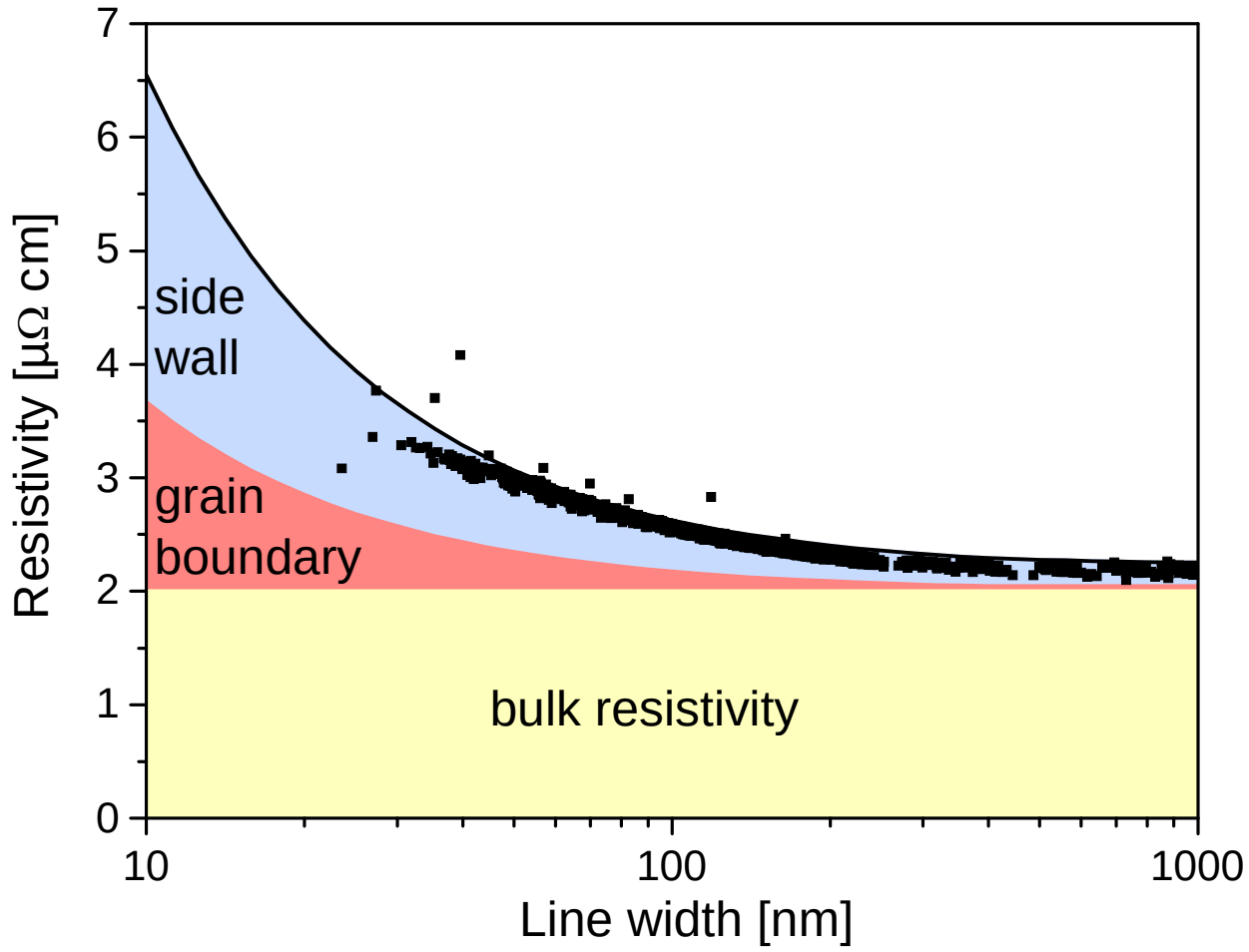
2005 Interconnect Update

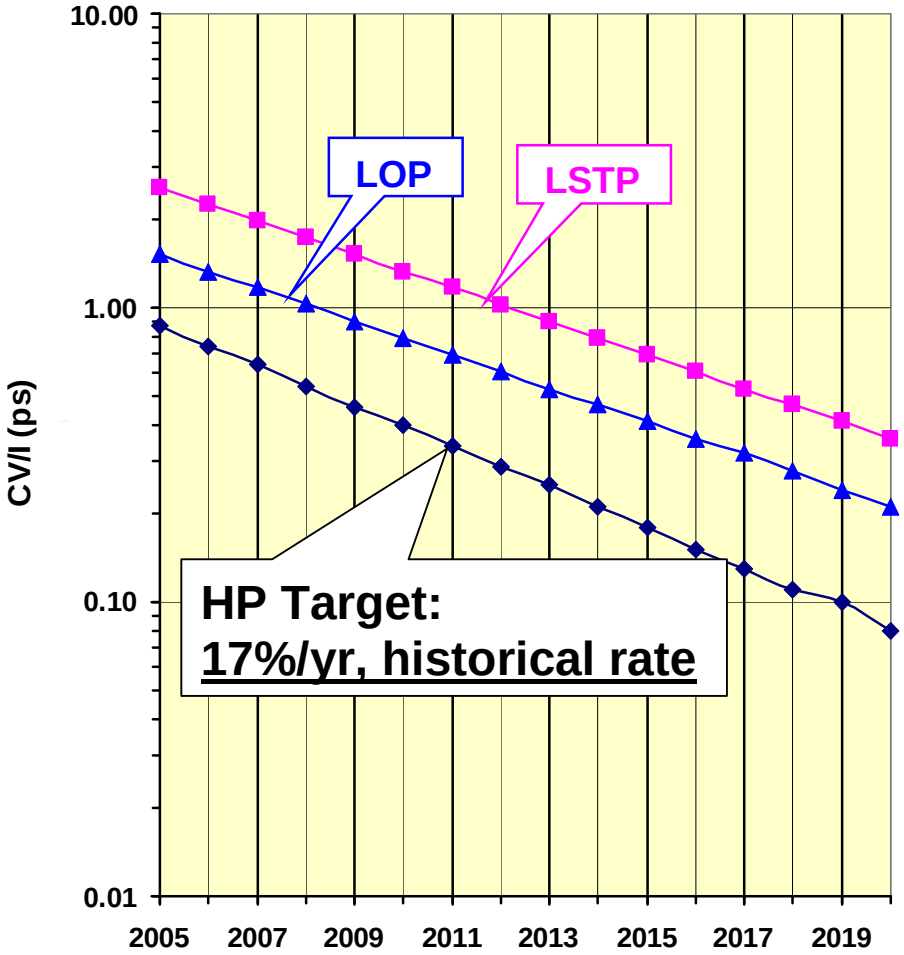
New Data and Models of Cu Resistivity Scaling



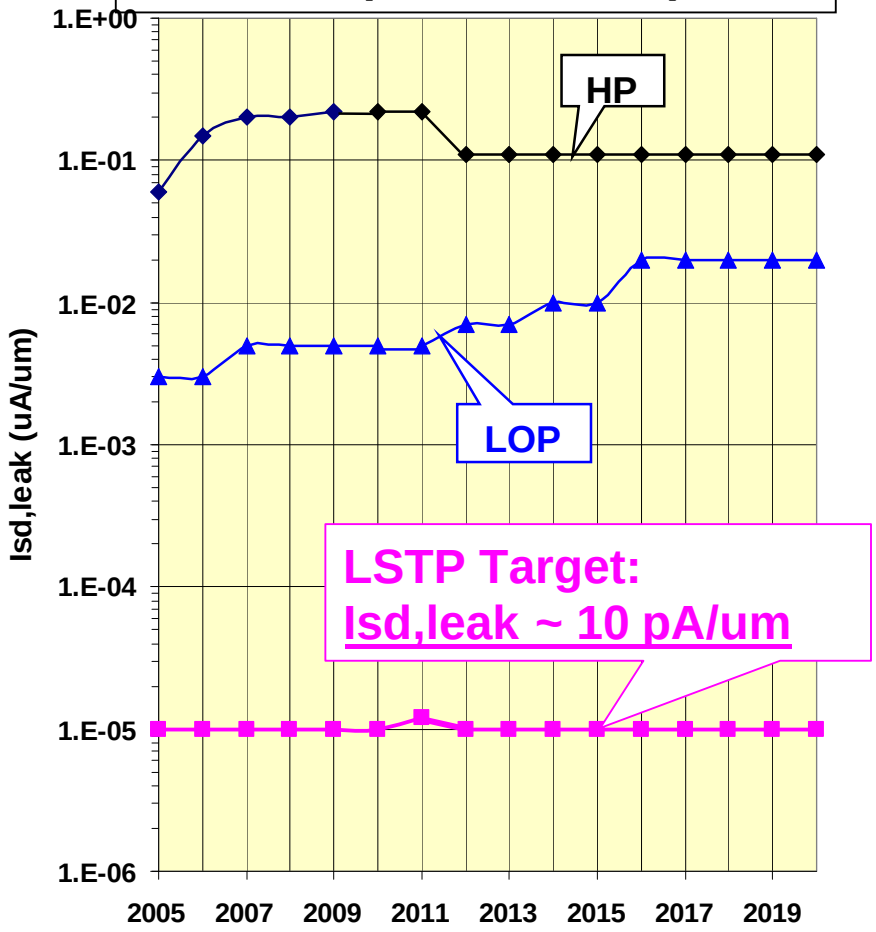
Courtesy: Infineon Technologies

Transistor Speed vs. Leakage Tradeoff

Intrinsic Transistor Delay,
$\tau = CV/I$
(lower delay = higher speed)



Leakage Current
(HP: standby power dissipation issues)



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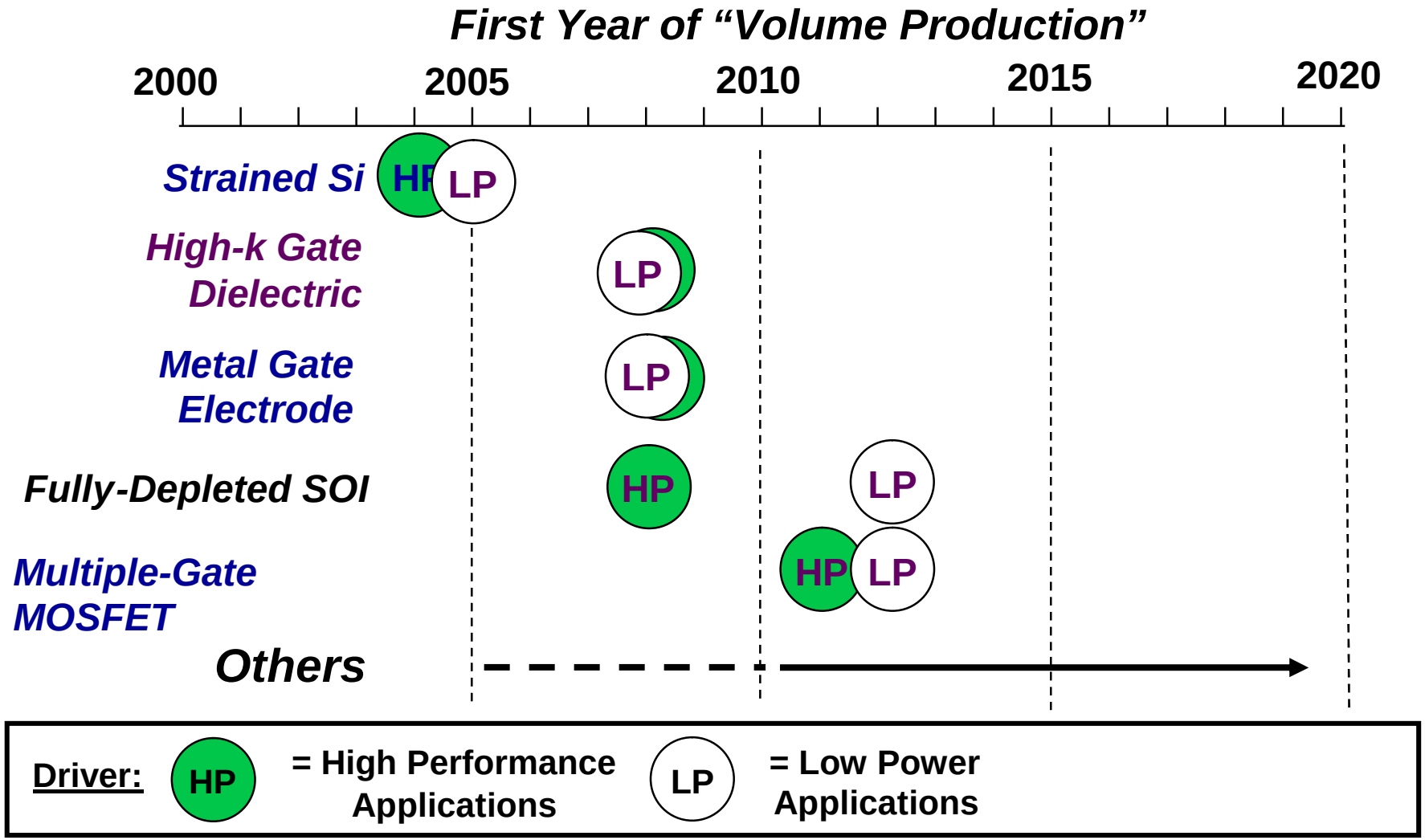
Source: 2005 ITRS

PIDS: The "CMOS Change Crunch"
Multiple, Big Changes Over ~7 Years



Source: 2005 ITRS

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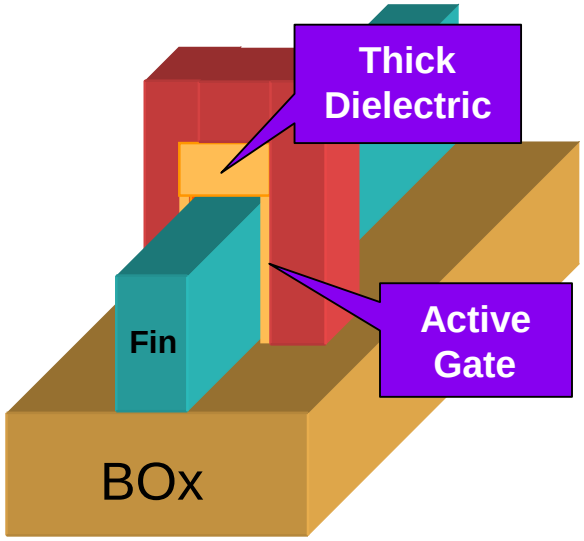
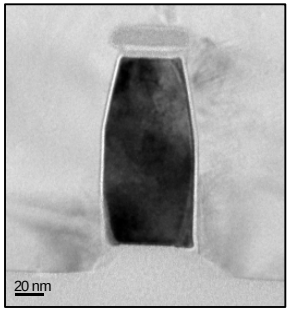
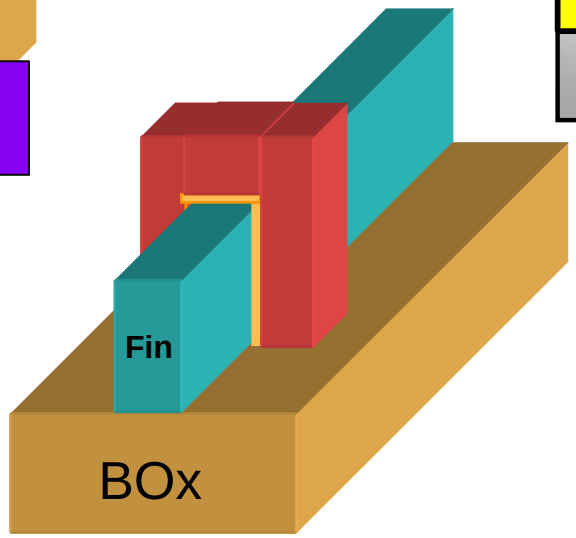
Potential path to "better electrostatics"…

(unfortunately, with I_{OFF} still limited by kT/q)

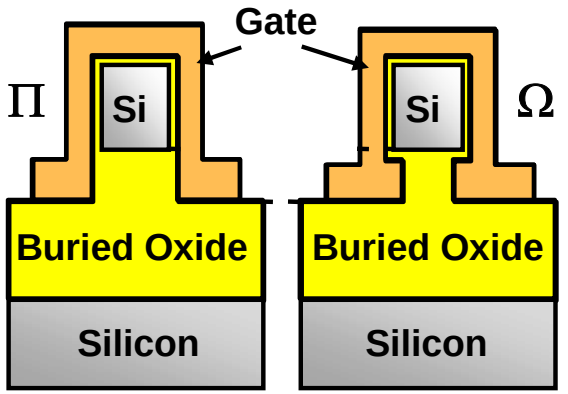


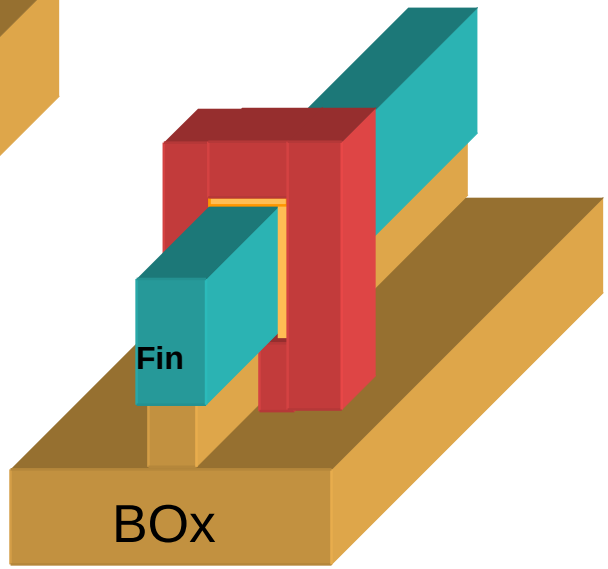
FinFET





Tri-Gate FET
3 Gates





Π / Ω Gate FET
3+ Gates

Steps toward ideal "coax gate" →

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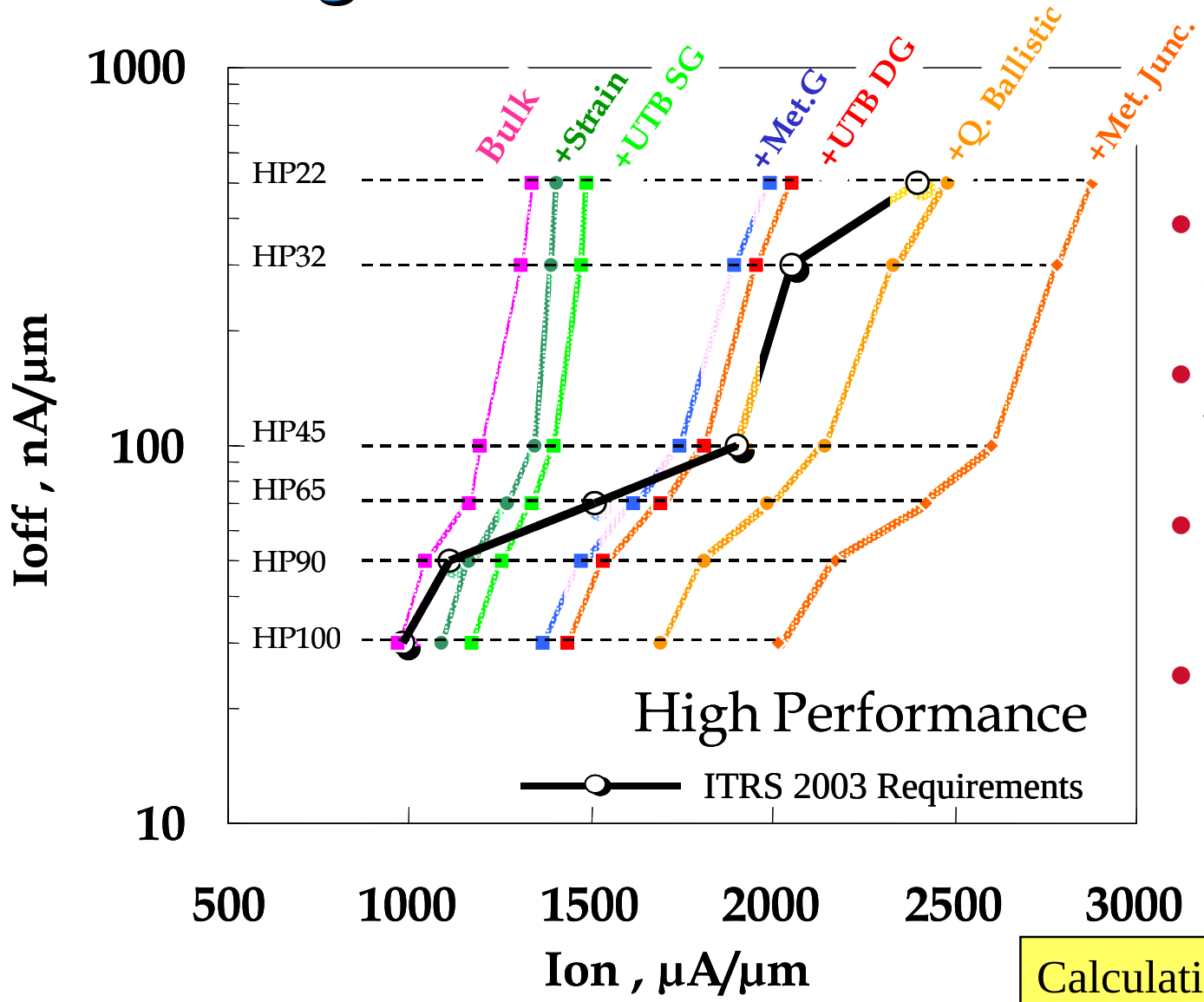
Modeling "Practical Limits" of Si FETs



- Modeling accuracy ?
- Assumption validity ?
- Integration issues ?
- Implementation cost ?

Calculations by T. Skotnicki

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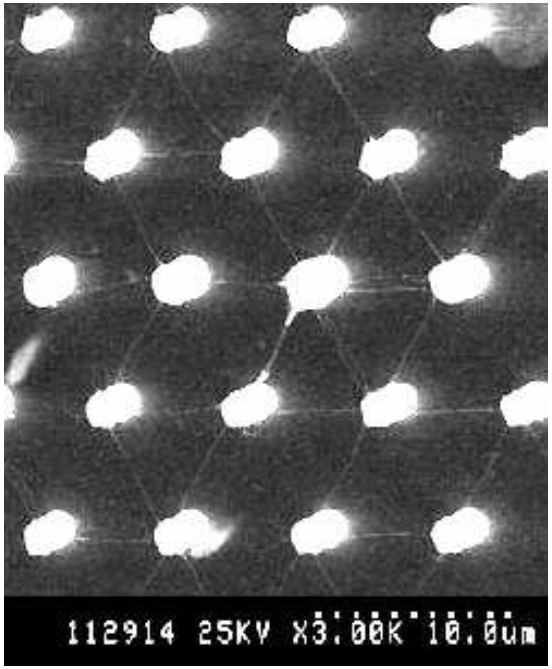
Source: 2003 ITRS

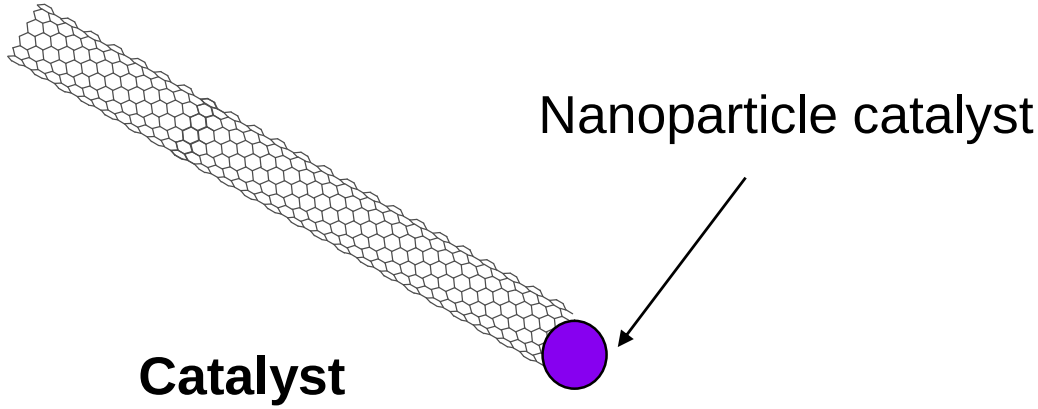
Carbon Nanotube FETs ?

Some carbon nanotubes have very good device characteristics, but:

- **Can we consistently make nanotubes with the desired properties ?**
- **Can we connect nanotubes to form complex electronic circuits ?**



Substrate Patterning



Catalyst engineering

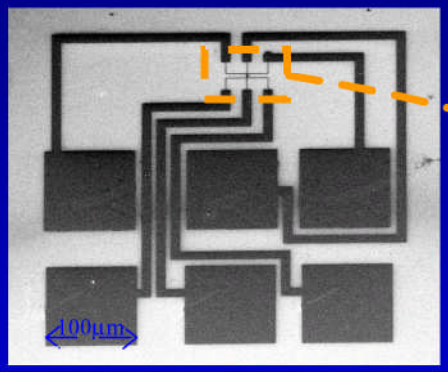
H. Dai, Stanford
P. McEuen, Cornell

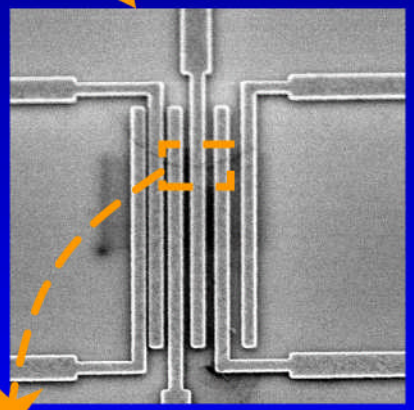
Nanotube Technology ?

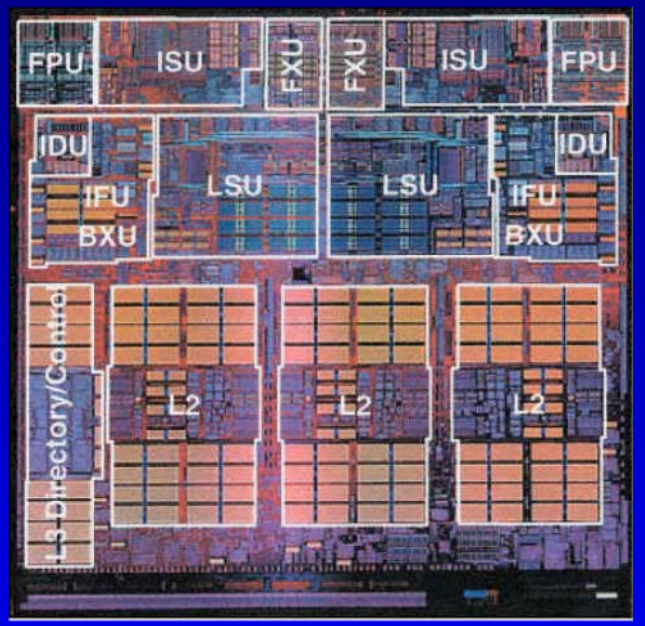
Plenty of room for improvement !

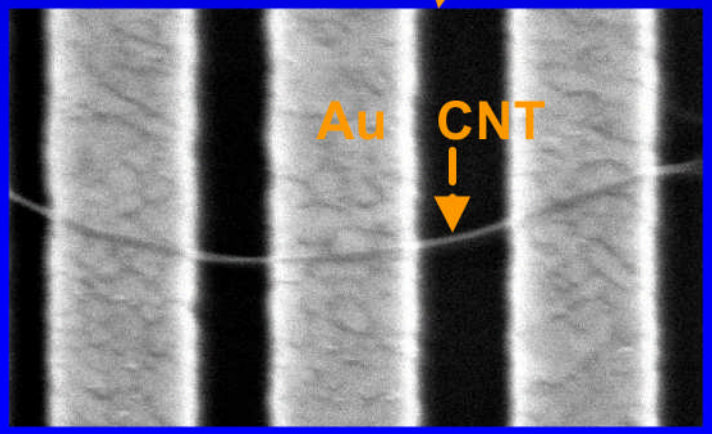
No new architecture !

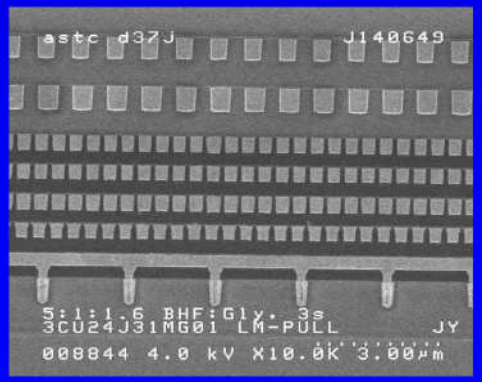
How do you get from here to there?

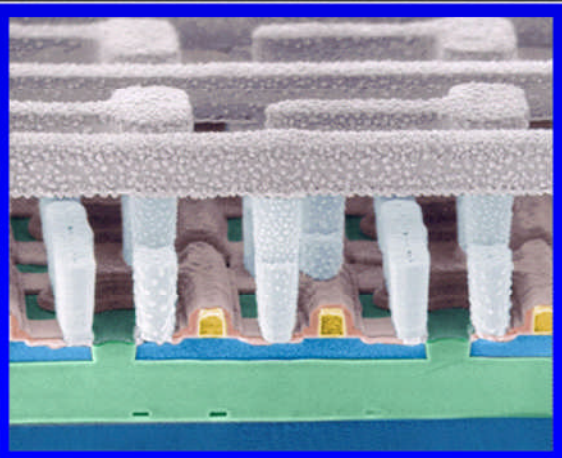












How close is today's volume technology to fundamental transistor limits ?

Fundamental FET Limits

$$E_S\big|_{\min} = \ln(2)\, k_B T$$

$$L_{\min} \approx \hbar \Big/ \sqrt{2mE_{\min}} = 1.5\text{nm}(300\text{K})$$

$$\tau_{\min} \approx \hbar \Big/ E_S\big|_{\min} = 0.04\ \text{ps} \quad (300\text{K})$$

$$n_{\max}(\text{at } 100\text{W/cm}^2) = 1.5\ \text{B/cm}^2$$

90nm technology
(from ITRS)

$$E_S \approx 35{,}000 \times E_S\big|_{\min}$$

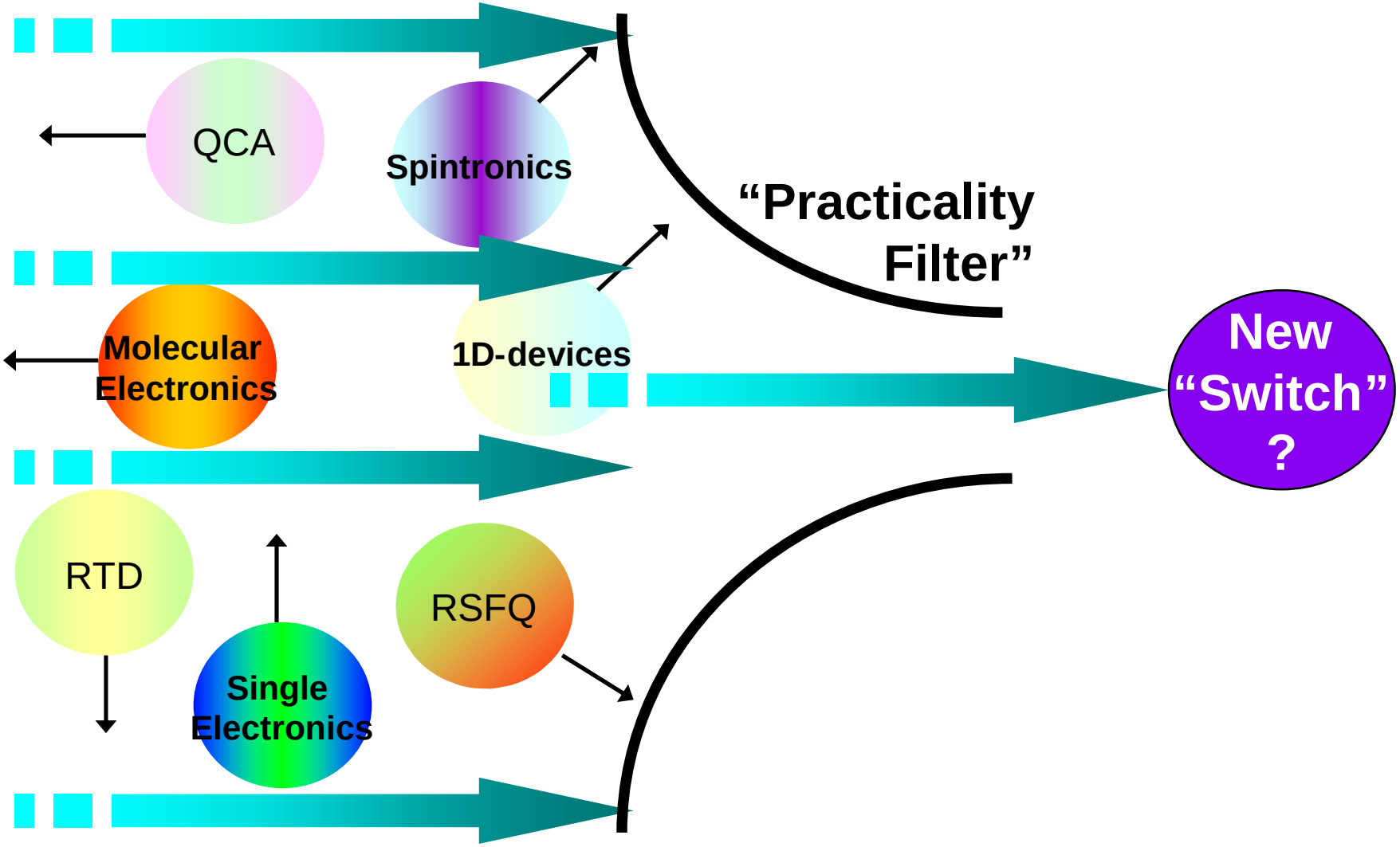
$$L \approx 25 \times L_{\min}$$

$$\tau \approx 24 \times \tau_{\min}$$

$$n \approx 0.13 \times n_{\max}$$

Source: Prof. Mark Lundstrom

Can anything replace the FET ?



2005 ITRS Risk Assessment of Potential Future Logic Devices

Logic Device Technologies (Potential)	*Scalability [A]*	*Performance [B]*	*Energy Efficiency [C]*	*Gain [D2]*	*Operational Reliability [E]*	*Room Temp Operation [F] ****	*CMOS Technological Compatibility [G]***	*CMOS Architectural Compatibility [H]**
1D Structures (CNTs & NWs)	**2.4**	**2.5**	**2.3**	**2.3**	**2.1**	**2.8**	**2.3**	**2.8**
Resonant Tunneling Devices	**1.5**	**2.2**	**2.1**	**1.7**	**1.7**	**2.5**	**2.0**	**2.0**
SETs	**1.9**	**1.5**	**2.6**	**1.4**	**1.2**	**1.9**	**2.1**	**2.1**
Molecular Devices	**1.6**	**1.8**	**2.2**	**1.5**	**1.6**	**2.3**	**1.7**	**1.8**
Ferromagnetic Devices	**1.4**	**1.3**	**1.9**	**1.5**	**2.0**	**2.5**	**1.7**	**1.7**
Spin Transistor	**2.2**	**1.3**	**2.4**	**1.2**	**1.2**	**2.4**	**1.5**	**1.7**

> 20	**>16 - 18**
>18 - 20	**≤ 16**

For each Technology Entry (e.g. 1D Structures, sum horizontally over the 8 Criteria
Max Sum = 24
Min Sum = 8

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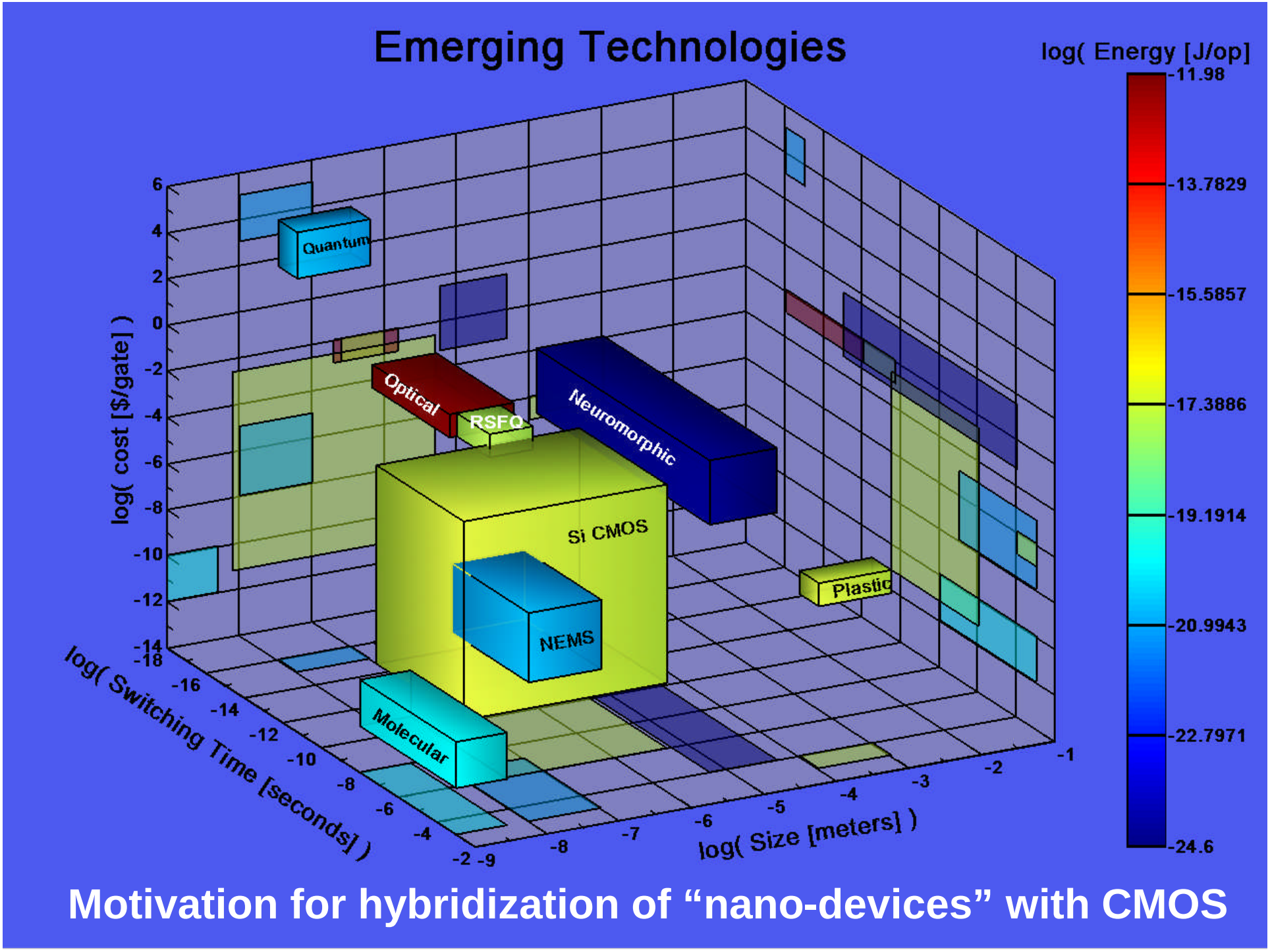
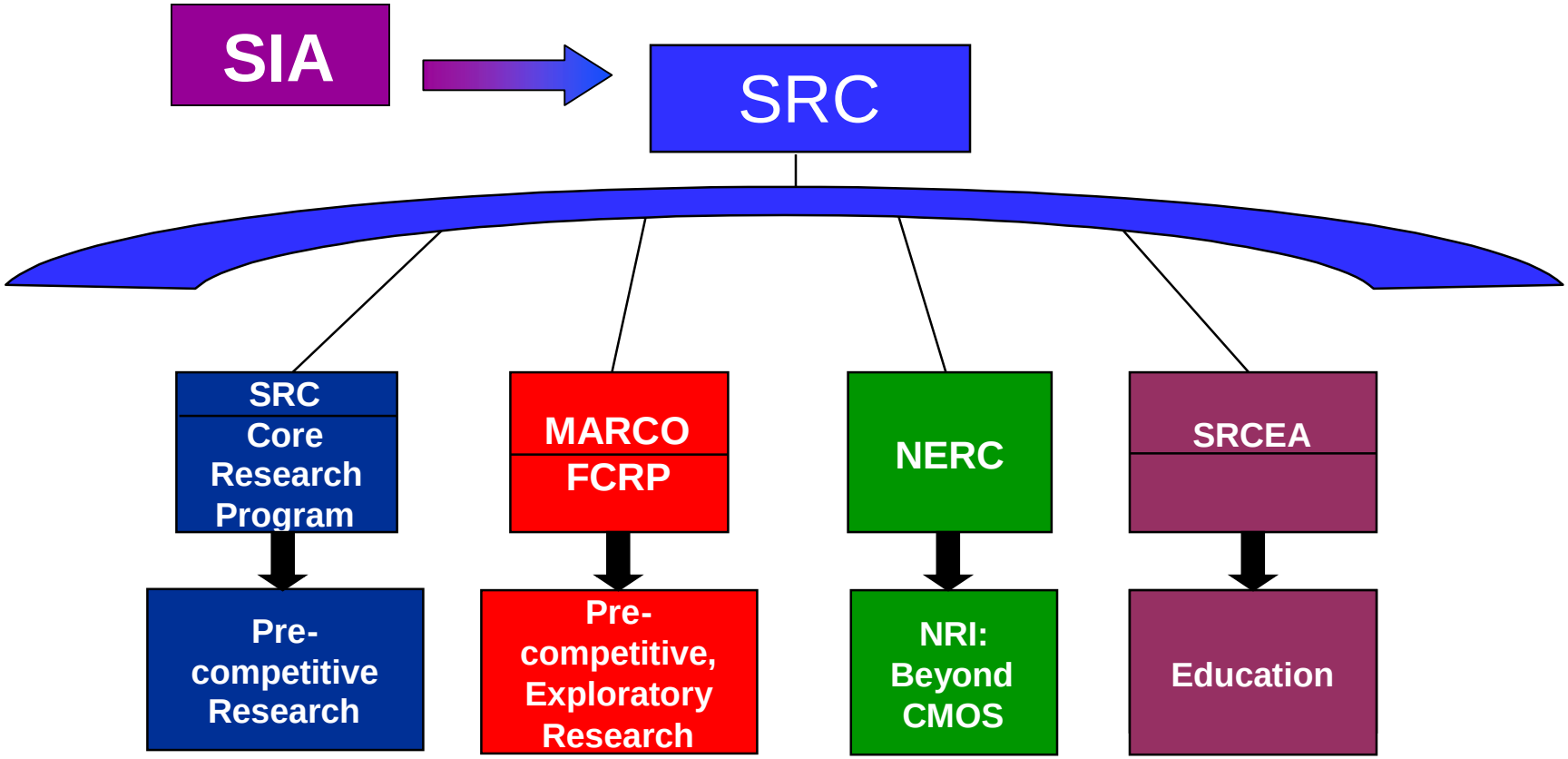
Source: 2005 ITRS



Motivation for hybridization of "nano-devices" with CMOS

The SIA-SRC "Umbrella"



- MARCO and NERC use SRC infrastructure and support staff
- Science Area Directors provide linkage to SRC Core Programs

MARCO FCRP: SIA-DoD Partnership
to Extend CMOS to Its Ultimate Limits

Members

SIA — Semiconductor Industry Association

AMD	LSI Logic
Analog Devices	Micron
Conexant	Motorola
Cypress	National
IBM	TI
Intel	Xilinx

semi

Air Products
Applied Materials
Cadence
Novellus
Teradyne

Dept. of Defense

DUSD(LABS)

DARPA

GSRC – System Design & Test Focus Cntr
Director: Prof. Jan Rabaey – **UC Berkeley**
- Design, verification, and test of heterogeneous SoC
- Covers spectrum from system specification to implementation.

UC Berkeley	Princeton
UCLA	Purdue
UCSB	Stanford
UC SC	U T Austin
UCSD	MIT
CMU	UIUC
Michigan	Georgia Tech
Penn State	Caltech

C2S2 – Circuit Design & Test Focus Cntr
Director: Prof. Rob Rutenbar - **Carnegie Mellon**
- Circuit techniques & system concepts for heterogeneous devices
- Design of end-of-roadmap and post-CMOS devices for robust performance

CMU	UC Berkeley
Columbia	UCLA
Cornell	UCSD
Ga Tech	U. Florida
MIT	UIUC
Stanford	U. Wash

IFC – Interconnect & Optoelectr Focus Cntr
Director: Prof. James Meindl – **GeorgiaTech**
- Nanoscale electrical and optical interconnects
- Novel thermal management solutions
- Interconnect-driven circuit & system design

Georgia Tech	UCSB
Stanford	RPI
MIT	UT Austin
SUNY Albany	CMU
U Central Fl	NC State U
Cornell	UC Berkeley

NST – NanoScale Devices Focus Cntr
Director: Prof. Dimitri Antoniadis - **MIT**
- CMOS scaling to ultimate limit
- Advanced FETs incorporating novel materials
- Nanotubes, molecular devices & spin-based FETs

MIT	SUNY Albany
Caltech	UT Austin
Cornell	Univ Virginia
NC State	UC Berkeley
Penn State	UCLA
Princeton	UC SB
Purdue	Univ Florida
Stanford	Univ Maryland

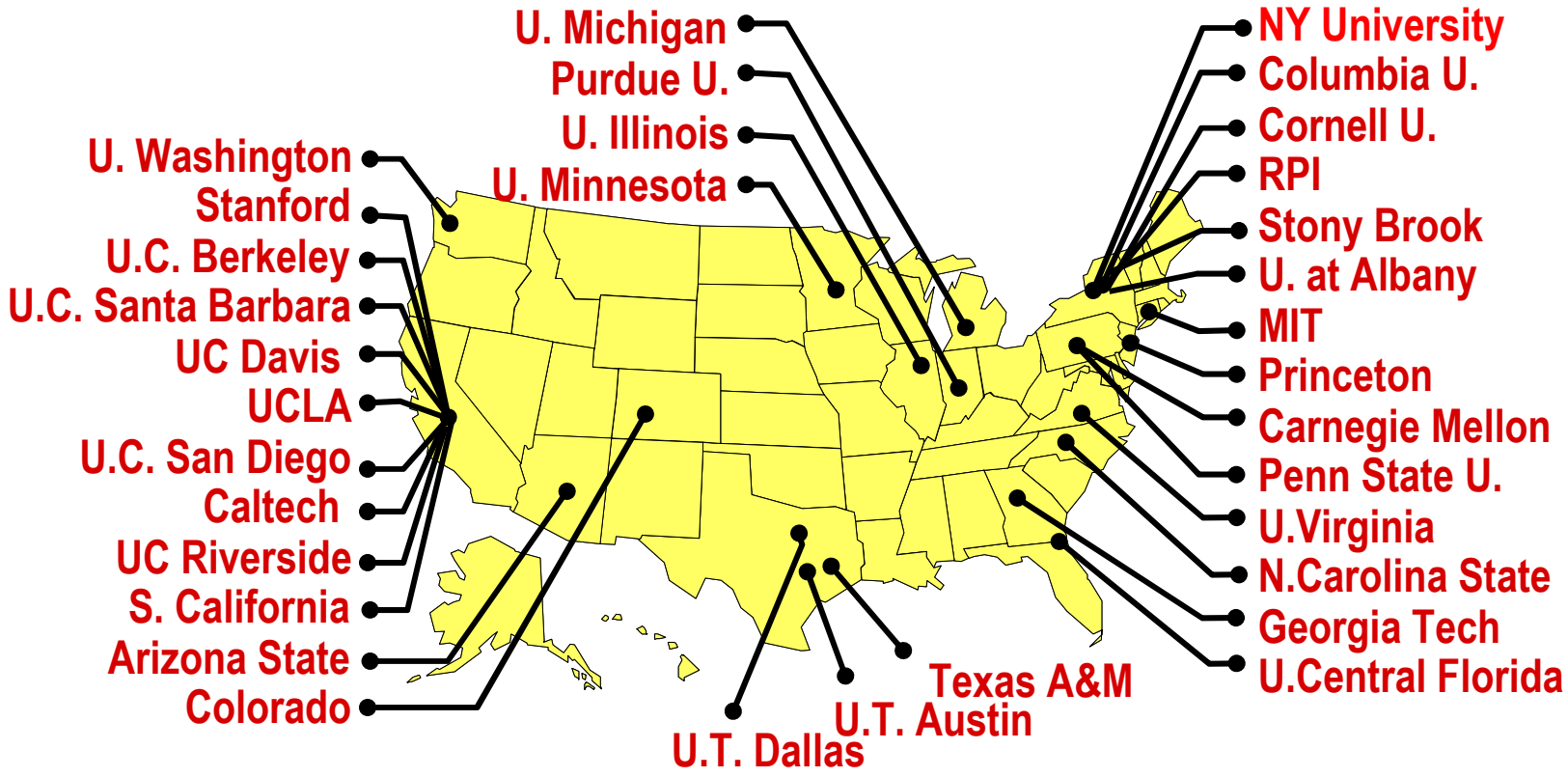
FENA – NanoScale Mat'rl Synth Focus Cntr
Director: Prof. Kang Wang – **UCLA**
- Novel nanoscale devices, materials and structures

UCLA	USC	U Minnesota
UC Berkeley	Caltech	SUNY Stony Br
UCSB	NC State	Ariz State
UC Riverside	MIT	

Source: MARCO, 2004

Top U.S. Universities in the FCRP

- Many of country's top universities and faculty are *already* part of at least one Focus Center
  - 33 Universities and ~200 research faculty



12/03 SIA Recommendations to PCAST

- **In the long term, the SIA feels that we face two grand challenges worthy of >$200M/year in new federal funding:**

(1) Scaling limits of "evolutionary lithography/thin-film manufacturing"

(2) Scaling limits of "charge-transport devices/interconnect"

- **We suggest that these might be overcome through new and synergistic research in the under-funded *broad areas* of:**

(1) "Directed self-assembly" of complex structures with "nanoelectronics-functionality" (computation, comm., etc.)

(2) "Beyond (classical) charge transport" signal-processing/ computational technology (e.g., based on quantum-states)

"Nanoelectronics Research Initiative"

The Search for a "New Switch":

The NERC Consortium NRI Program

- NERC members: AMD, Intel, IBM , Freescale, Micron, TI
- Started in March, 2005
- First project: partnership with NSF on supplemental funding for selected N/MR-SECs on nanoelectronics
- NERC-NSF award announcements at SNB-III, 12/05
- Latest program: formation of three regional NRI Centers in partnership with state governments, et al.

Promising Directions

in the search for a new switch

→ NRI "Research Vectors"

- "Bits" represented by variables other than charge (e.g., spin)
- Non-equilibrium systems → lower power, less heat
- Novel energy-transfer mechanisms → overcome RC limits
- Nanoscale thermal management → cooler operation
- Directed self-assembly → less variability, higher density, more reliable, lower cost

What about Quantum Computing ?

Big Challenges !

We require:

Difficult at room temp

- precise control of quantum phenomena
- low noise = long decoherence time T
- fast coherent switching time t

Figure of merit D

$$D = \left(\frac{T}{t} \right)$$

We want D as big as possible + quantum error correction

Source: A. Ekert, Oxford University

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Rationale for Non-Electric-Charge-Based Signal-Processing/Computation

Break the "electrical scaling tyranny," e.g.:

(1) Voltage (limiting speed/power/error-rate tradeoff)

(2) Resistance (limiting speed and low power)

(3) Capacitance (limiting speed and low active power)

(4) Charge-Transport (e.g., mobility -- limiting speed)

(5) Charge-Leakage Mechanisms (limiting standby power)

Some Potential *State Variables* Alternative to Electric Charge

- Molecular/atomic state
- Magnetic-dipole magnitude/orientation (e.g., electron/nuclear spin)
- Electric-dipole magnitude/orientation
- Photon number
- Photon polarization
- Quantum phase
- Mechanical state

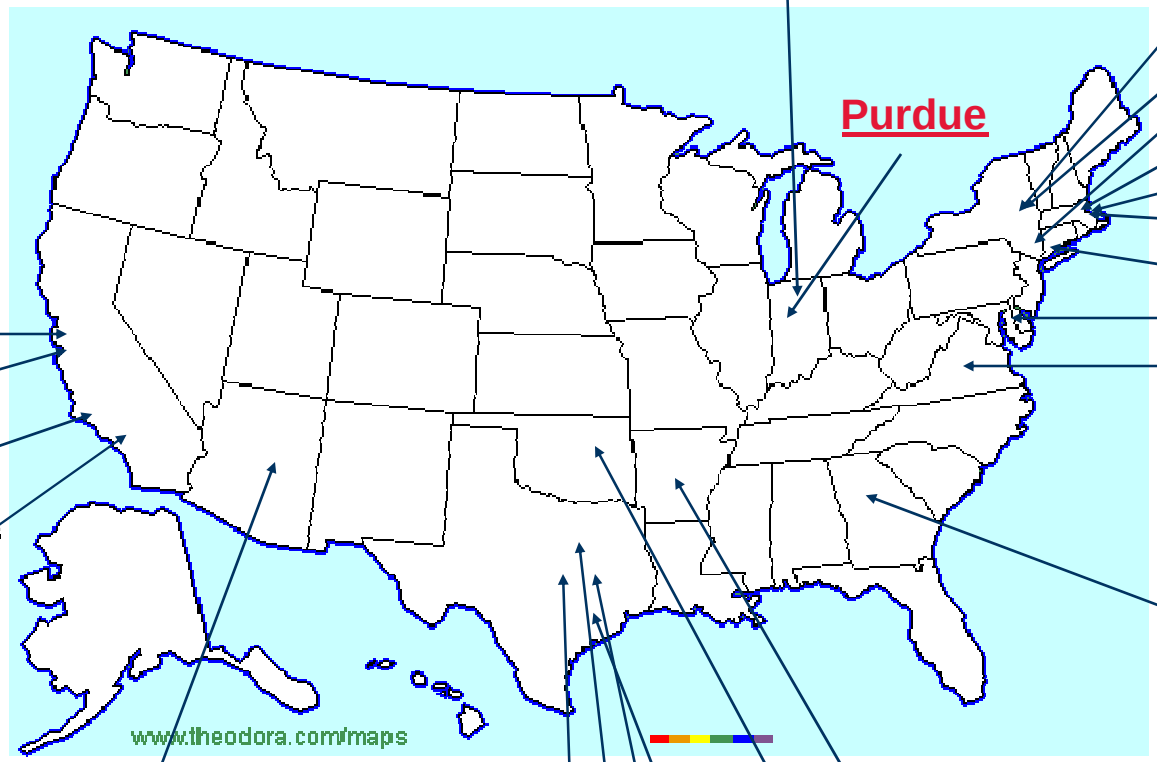
NRI Funded Universities

INDEX INSTITUTE FOR NANOELECTRONICS DISCOVERY AND EXPLORATION

WIN Western Institute of Nanoelectronics

SWAN

NRI



Notre Dame

SUNY Albany

RPI

Columbia

U Mass

MIT

Harvard

Yale

U of MD

U of Virginia

Purdue

UC Berkeley

Stanford

UC Santa Barbara

UC Los Angeles

GIT

Rice

U of Arkansas

Arizona State

TX A&M

U of Oklahoma

UT Dallas

UT Austin

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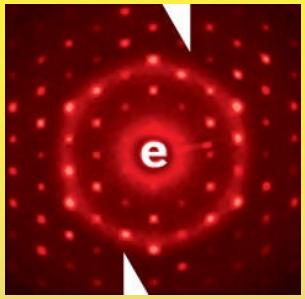
SWAN

WIN

NSF-NRI

Initial WIN Programs



the UC Discovery Grant

intel

Five Research Vectors for information processing beyond scaled CMOS.

1st Phase Focus:

- ✓ Spintronics Materials & Devices
- ✓ Plasmonics

Spintronics for Information Processing

- Spintronics Devices
- Spin Device-Device Interaction

WiN Western Institute of Nanoelectronics

UCLA, UCSB, UCB, & Stanford

To explore and develop advanced research devices, circuits and nanosystems with performance beyond conventional scaled CMOS.

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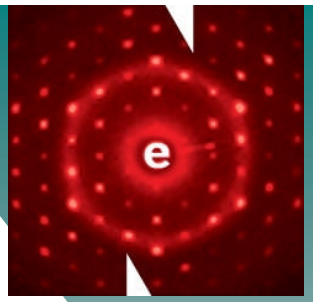
Initial INDEX Programs



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To discover and demonstrate nanodevice innovations that surmount CMOS scaling limits that will impede the historical rate of progress of US Semiconductor Industry

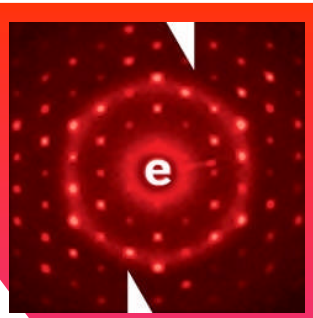
Five fully-integrated and synergistic research tasks for magnetic and molecular device paradigms

First Phase Focus: Task I (Novel Computing Devices) and Task II (Self-Assembly and Fabrication)

UAlbany, MIT, Yale, Harvard, Georgia Tech, RPI, and Purdue

RRD 3/21/07

Initial SWAN Programs



Five Research Tasks addressing all NRI Research Vectors

1st Phase Focus:

- ✓ Spin Hall Effect
- ✓ Pseudospintronics
- ✓ Phasetronics
- ✓ Quantum Point Contacts

The Search for Beyond-CMOS Logic-State Variables

- Modeling and simulation of devices based on alternative computational-state variables

SWAN

SouthWest Academy of Nanoelectronics

UT Austin, UTD, Texas A&M, Rice, ASU, U. MD, Notre Dame

RRD 3/21/07

SWAN Tasks and Investigators

- **Task 1: Logic Devices based on new computational state variables**
  (UT: Banerjee, Gilbert, MacDonald, Register; Maryland: Das Sarma, TAMU: Sinova, ASU: Shumway)

- **Task 2: Novel materials and structures**
  (TAMU: Sinova; Notre Dame: Porod, , Bernstein; UT: Gilbert, Banerjee, Maryland: Das Sarma)

- **Task 3: Directed Self-assembly and nanoscale thermal management**
  (UT: Gilbert, Register, Banerjee; Maryland: Das Sarma)

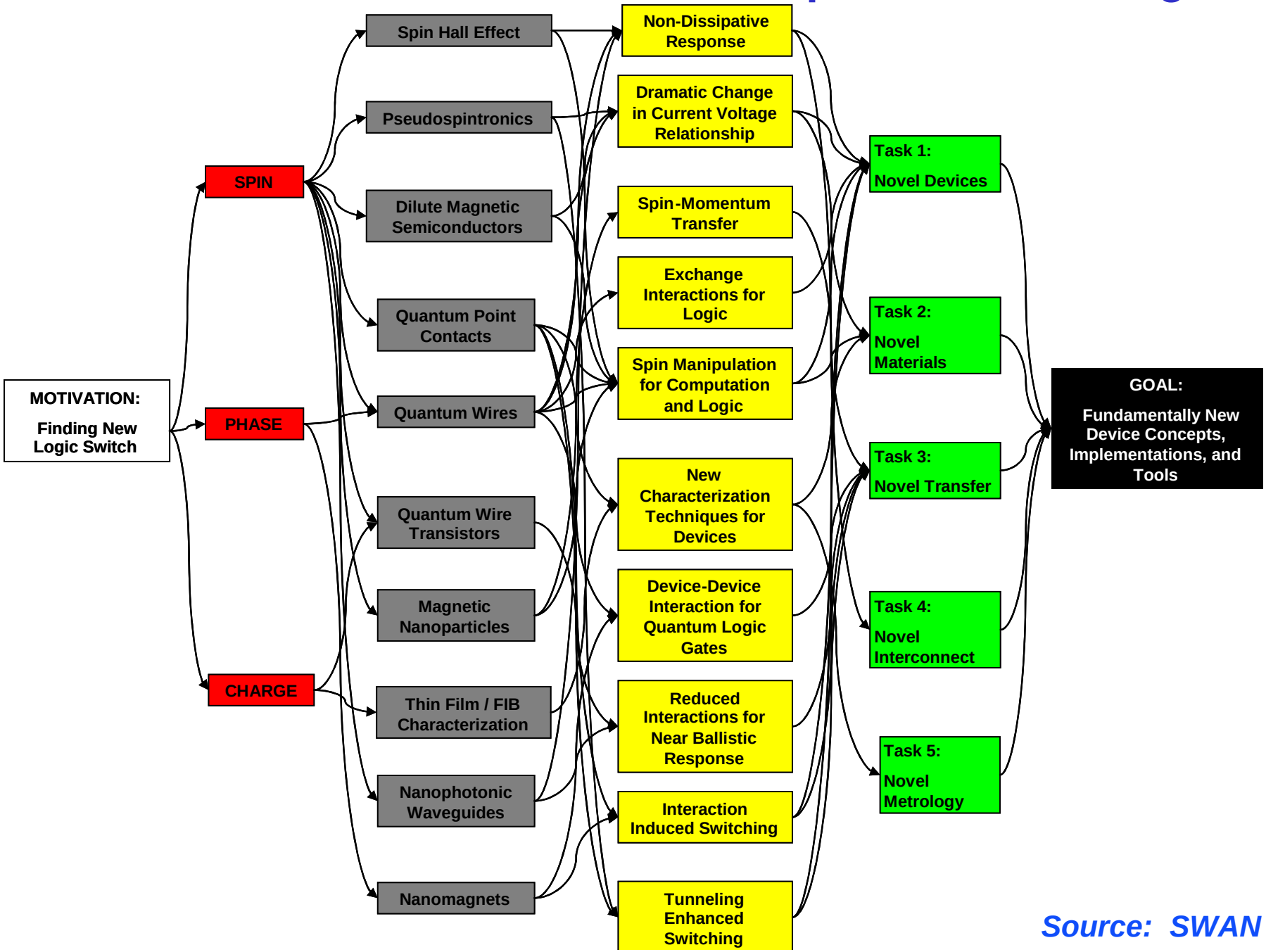
- **Task 4: Novel interconnect, and architectures**
  (Rice: Massoud, Nordlander, Halas)

- **Task 5: Nanoscale Characterization**
  (UT Dallas: Gnade/Kim)

Source: SWAN

Novel Transistors Based on Electron Spin, Phase, Charge

SWAN



Source: SWAN

Task 1,3: Spin Degree of Freedom in Quantum Point Contacts (QPC) and Quantum Wires (QW)

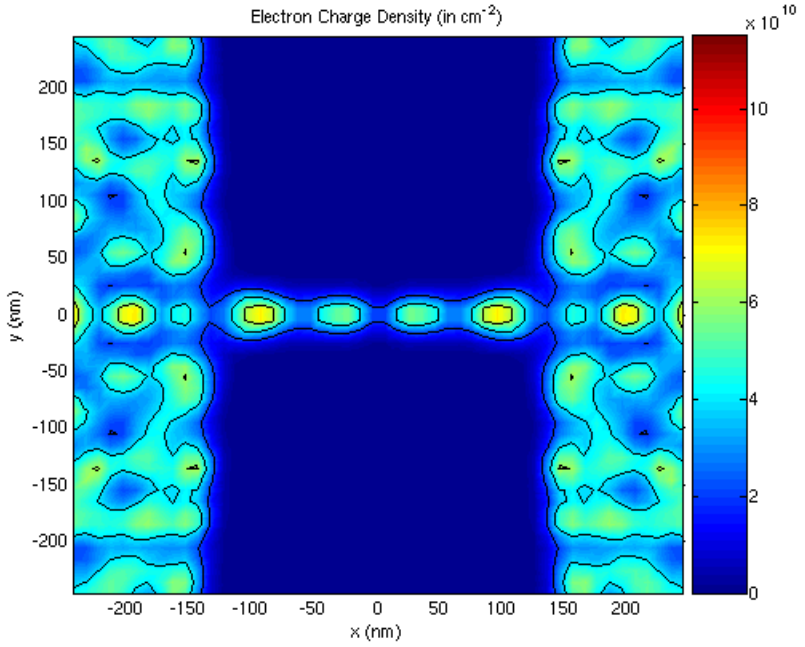
SWAN

Investigators: Shumway, Gilbert

Use many body Path Integral Monte Carlo to determine spin-charge separation in strongly correlated, low density quantum point contacts and quantum wires for novel switches.

In the figure:

- Spin down correlation function assuming a spin up electron at the center of the channel of a 100 electron quantum point contact.
- The length of the QPC is 200 nm
- The gate voltage is V_g = -0.30 V.
- Clear antiferromagnetic ordering associated with a Heisenberg spin chain is shown.
- This is a system which may exhibit spin-charge separation.

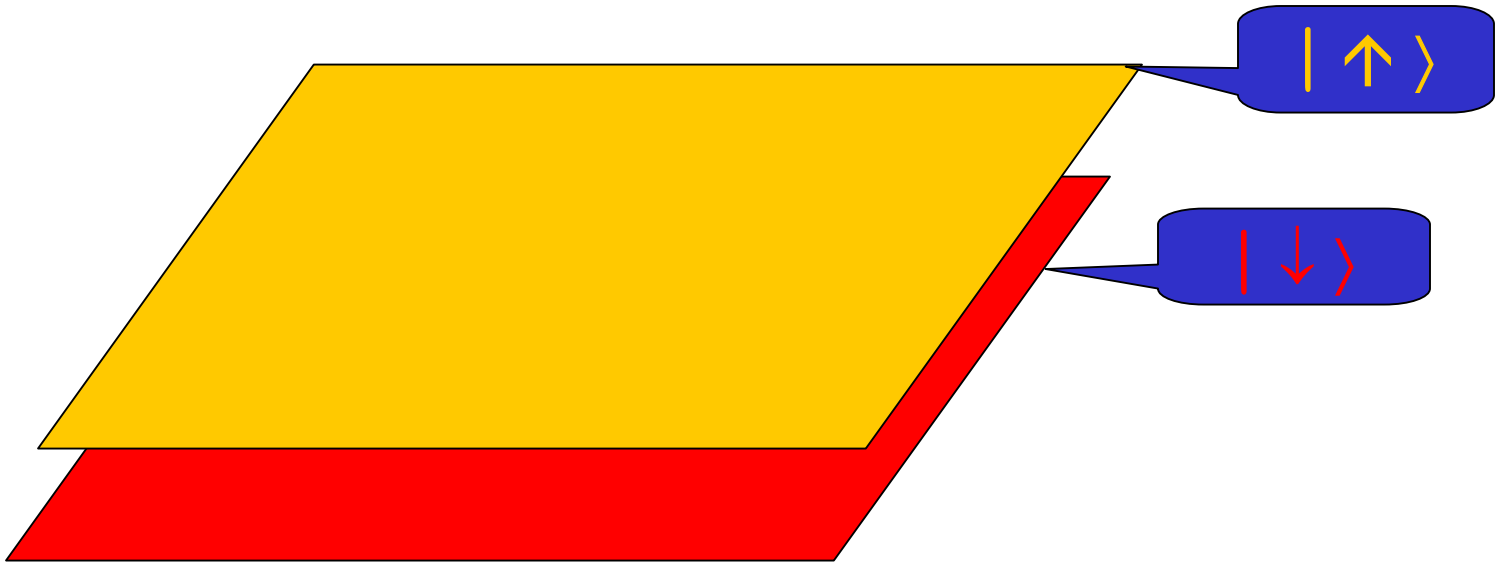


Novelty:

Use a new method for calculating the electrical and spin conductance of fully-interacting, low electron density systems to explore their use for fast, dissipation-less logical switches.

Source: SWAN

Pseudospintronics – What?



Spontaneous Interlayer Phase Coherence

=

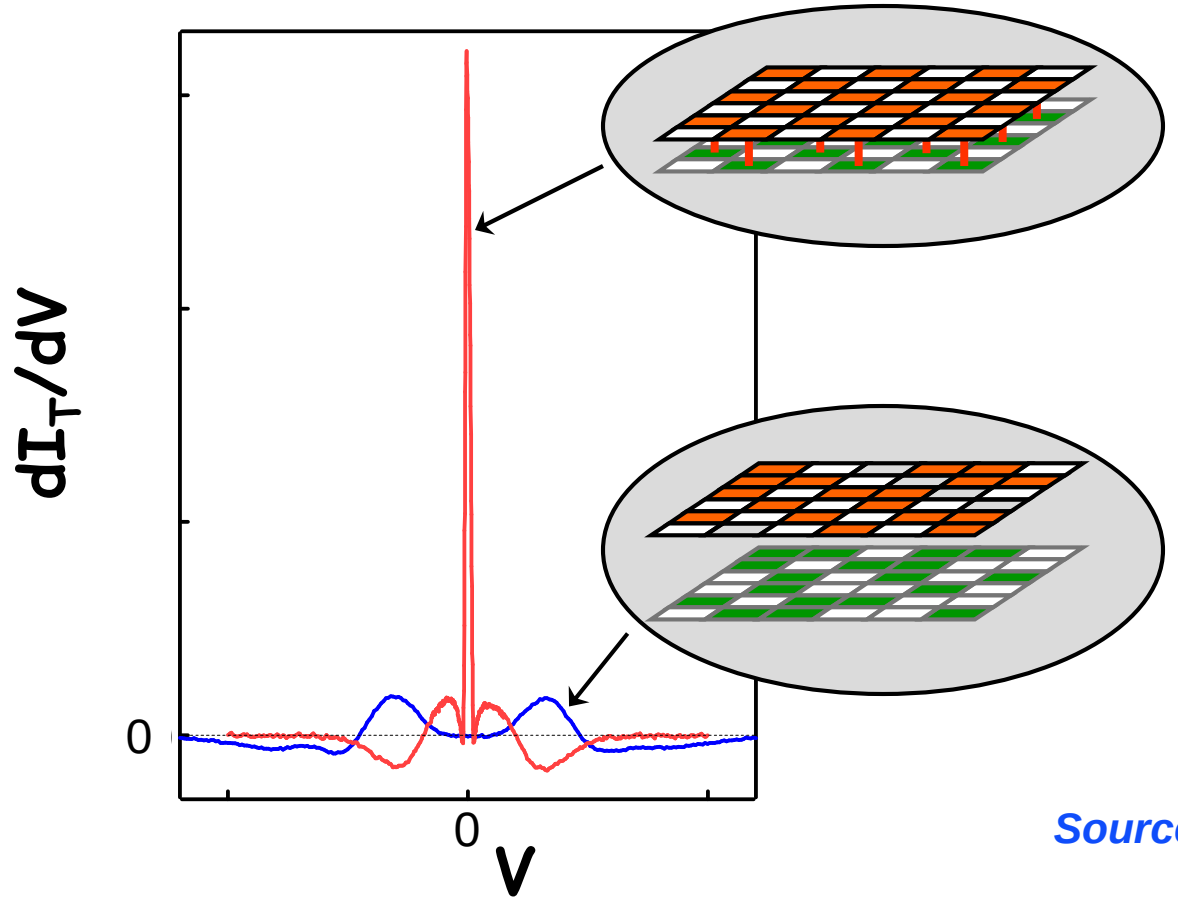
Pseudospin Ferromagnetism

$$|\Psi\rangle_0 = \Pi_i \left(|\uparrow\rangle_i + e^{i\varphi} |\downarrow\rangle_i \right)$$

Source: SWAN

Pseudospintronics - Why?

SWAN

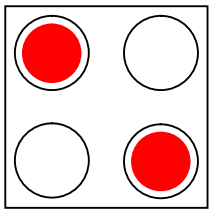


Source: SWAN

Spielman et al. PRL (2000)
Kellogg et al. Wiersma et al., Tutuc et al. PRL (2004)

Quantum-Dot Cellular Automata

A Quantum-Dot Cell

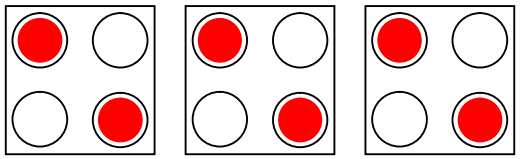


A cell with 4 dots

2 extra electrons

Represent binary information by charge configuration

An Array of Cells



Neighboring cells tend to align due to direct Coulomb coupling

Source: SWAN

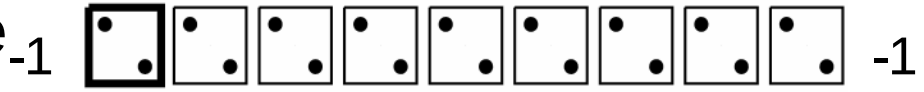
Task 2: Novel Structures

SWAN

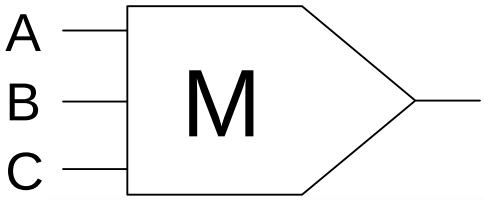
Nanomagnet-Based Logic- MQCA

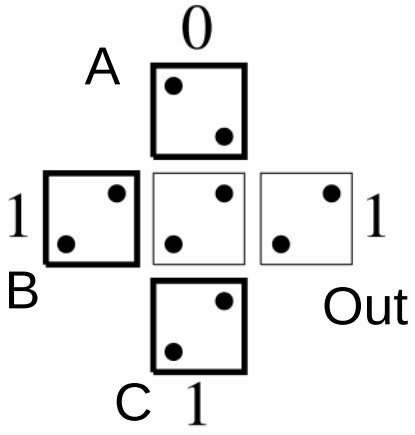
Wolfgang Porod and Gary Bernstein, Univ. Notre Dame

Binary wire

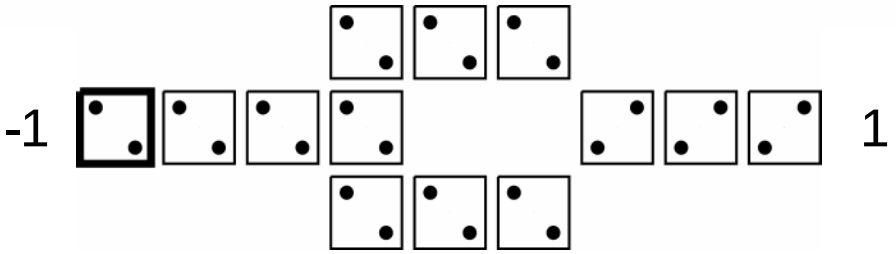


Majority gate





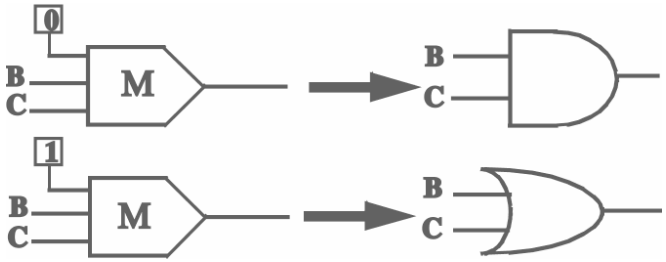
Inverter



A	B	C	Output
0	0	0	0
0	0	1	0
0	1	1	1
0	1	0	0
1	1	0	1
1	1	1	1
1	0	1	1
1	0	0	0

AND gate

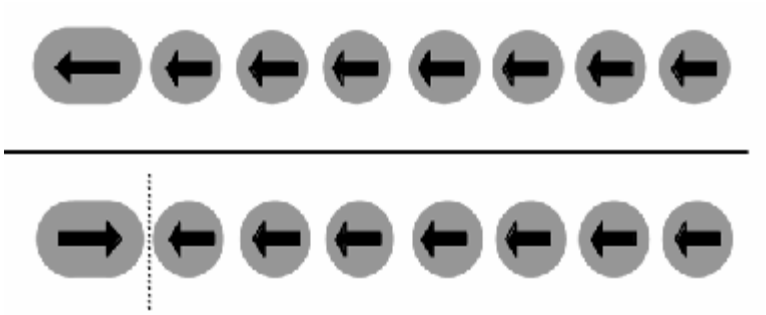
OR gate

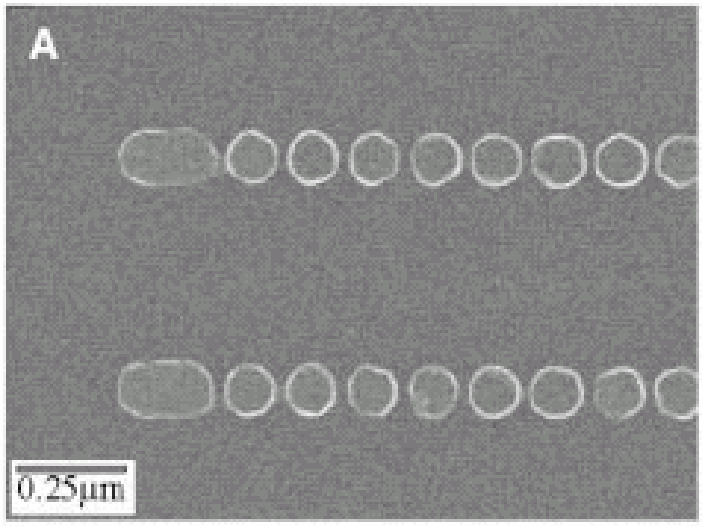


Programmable 2-input AND or OR gate.

Source: SWAN

First room temperature magnetic "quantum-dot cellular automata"





R.P. Cowburn and M.E. Welland SCIENCE, VOLUME 287, 1466 (2000)

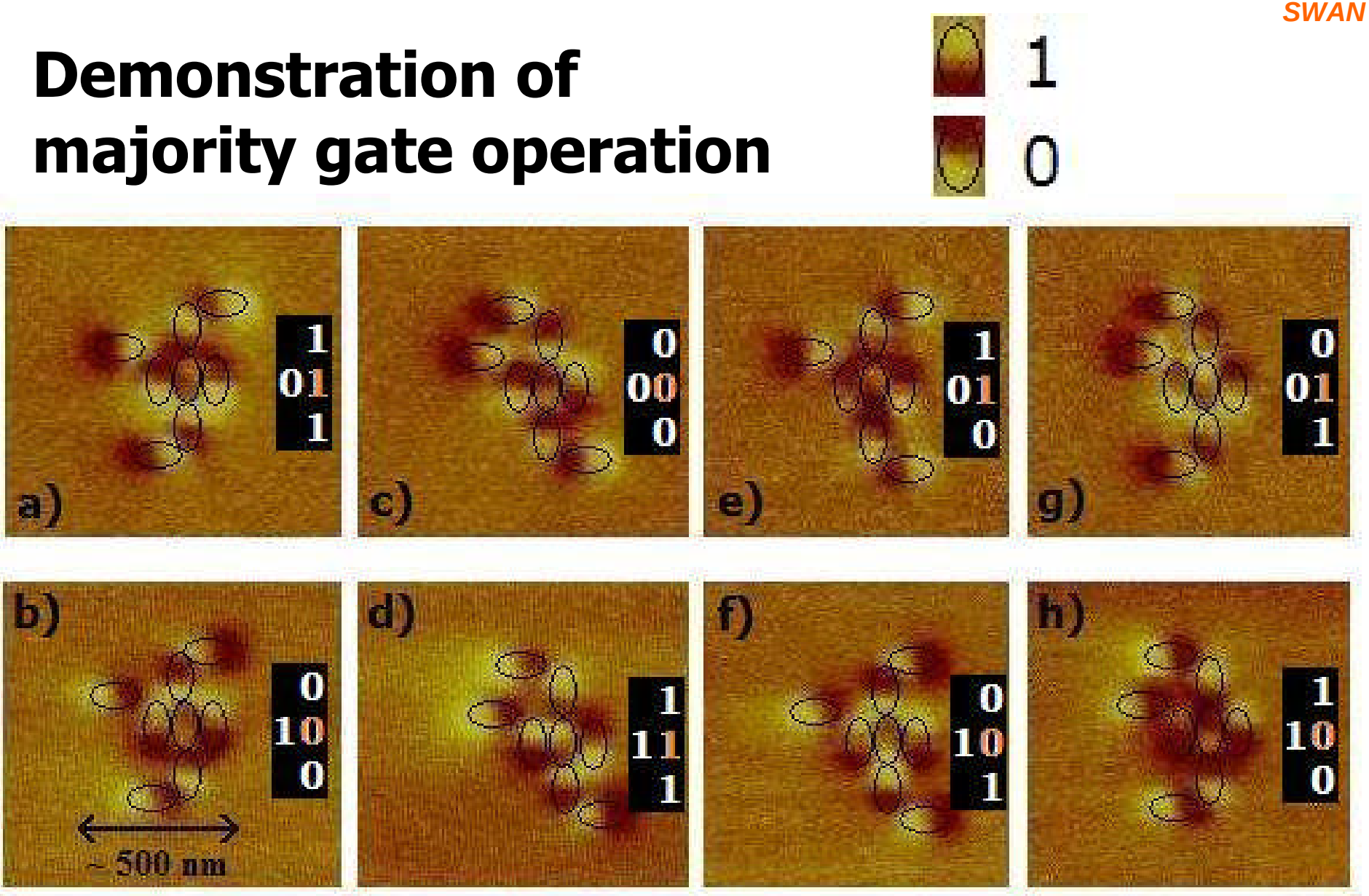
The circular dots, each of diameter 110 nm, placed on a pitch of 135 nm. The dots were 10 nm thick and were made from the common magnetic alloy supermalloy ($Ni_{80}Fe_{14}Mo_5X_1$, where X is other metals) by e-beam lithography and lift-off.

Evolution of a soliton propagating along a chain of coupled nanomagnets under the action of a 30Oe field applied:

R.P. Cowburn *JOURN MAGNETISM MAGNETIC MAT, VOLUME* **242**, 505 (2002)

Source: SWAN

Demonstration of majority gate operation

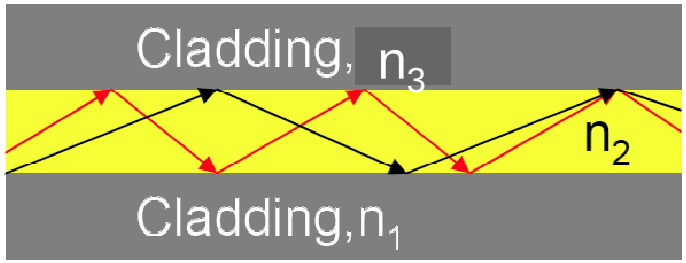


(Note that the output is inverted)

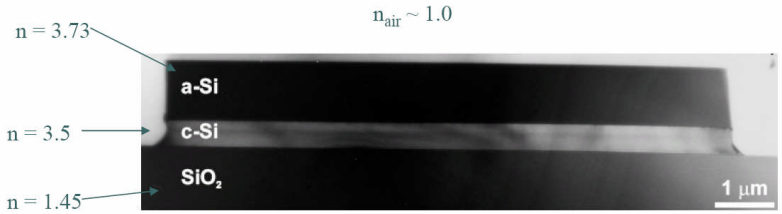
Source: SWAN

Optical Interconnects

Planar optical interconnect



$n_2 > n_1, n_3$



H. Zimmerman, 2000.

Pros:

- **Broad bandwidth**
- **Faster medium**
- **Several channels through one data path**
- **Reduced interference and cross-talk**

Cons:

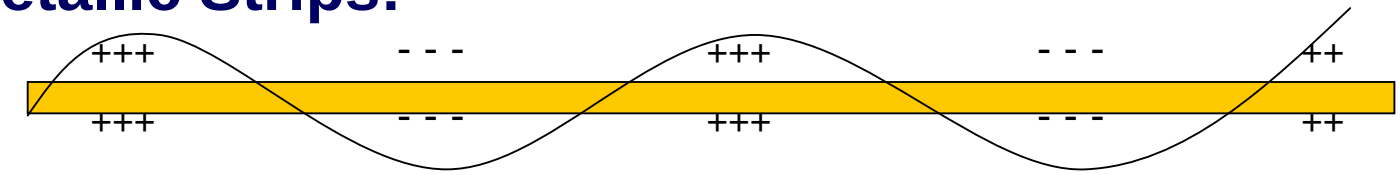
- **Transmitter and receiver units are required**
- **Diffraction limits miniaturization**
  - **min(size) > wavelength/2**
  - **IR-telecom: wavelength = 1.55μm**
- **Difficult and lossy bending**

Source: SWAN

An Alternative: Surface Plasmons

Dielectric\Metallic Strips:

Conceptual Model

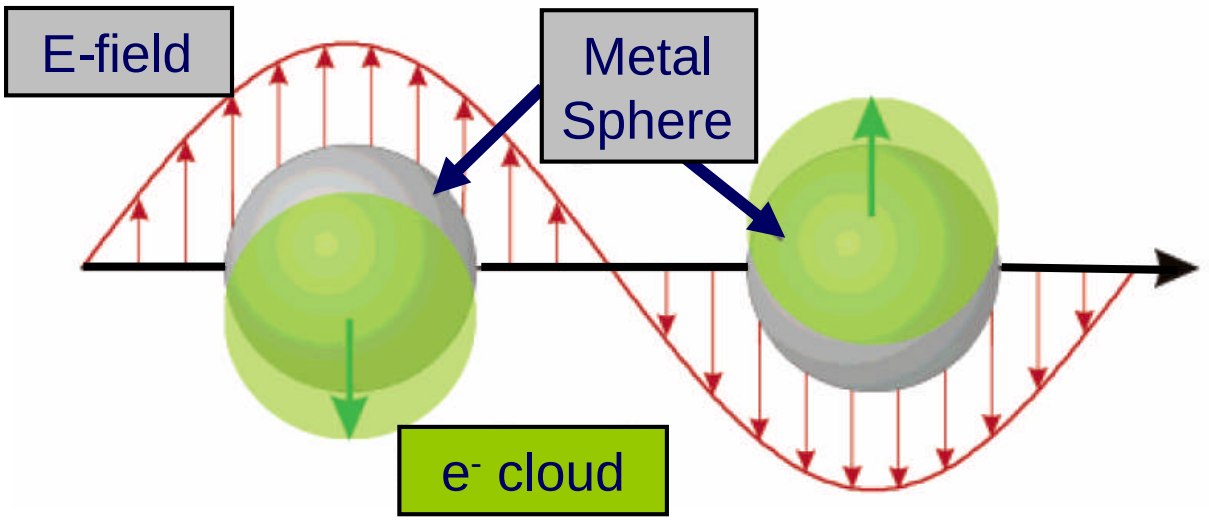


- **Plasmonic Waveguides**
  - **High light-confinement**
  - **Low bending loss**
  - **Single mode propagation**
  - **Fiber accessible**
- **Optoelectronic applications:**
  - **Optical interface**
  - **Filters**
  - **Micro-cavities**
  - **Directional couplers,…**

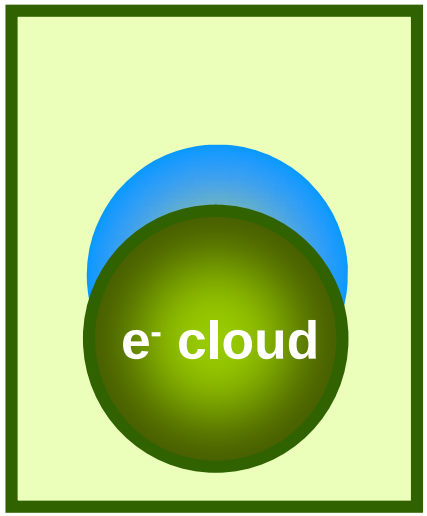
Source: SWAN

Surface Plasmons on Nanoparticle "Wires"

- **Oscillating electric field causes the conduction electrons to oscillate coherently.**



K. L. Kelly et al, 2003.



- **Plasmonic waveguides enable sub-wavelength transmission**
- **Can propagate light at sharp edges**
- **Other applications include chemical sensing\detection**

Source: SWAN

And, we're not yet "crazy idea"-limited!

e.g.: ~ any issue of Nature, Science, …

Devices:

- "Intrinsic Localized Modes" – Physics Today, 1/04
- "Slow Light" -- Nature, 7/11/03
- "Orbital Electronics" – Physics Today, 7/03

Self-Assembly of Devices:

- "DNA-Templated CNT FET" – Science, 11/03
- "Virus Toolkit for Directed Synthesis of Magnetic and Semiconducting Nanowires" -- Science, 1/9/04