Direct RF Sampling for Digital Radio Processing: Principles and Methods

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Outline

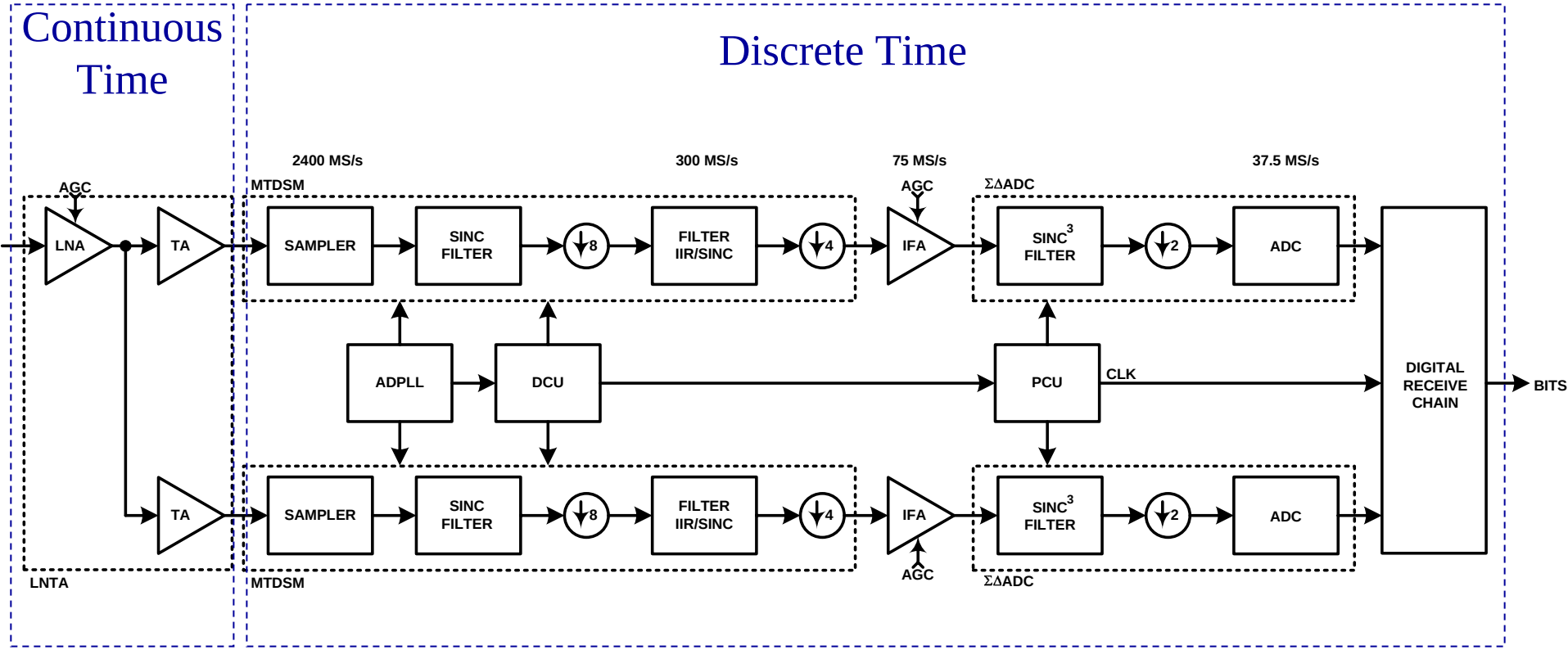
- Motivation
- Deep-submicron low-complexity design
  - Direct rf sampling
  - Discrete-time signal processing receiver architecture
  - Digital Backend
- Analog impairments
- Bluetooth Receiver example (sens: -83dBm)
- GSM/GPRS Receiver example (sens: -110dBm)
- Conclusion

Motivation

- Low-cost
  - Base digital deep-submicron CMOS process
  - Low-power
  - Amenable to migration to newer processes
  - Excellent performance; marketing reasons!
  - Fully integrated
    - Transceiver + Digital BB + Memory + Power Management + RFBIST
    - Analog/RF functions like important “guests” on application centric solutions
      - very large RAM
      - Analog/rf typically occupy < 5% area
  - Built-in calibration mechanisms

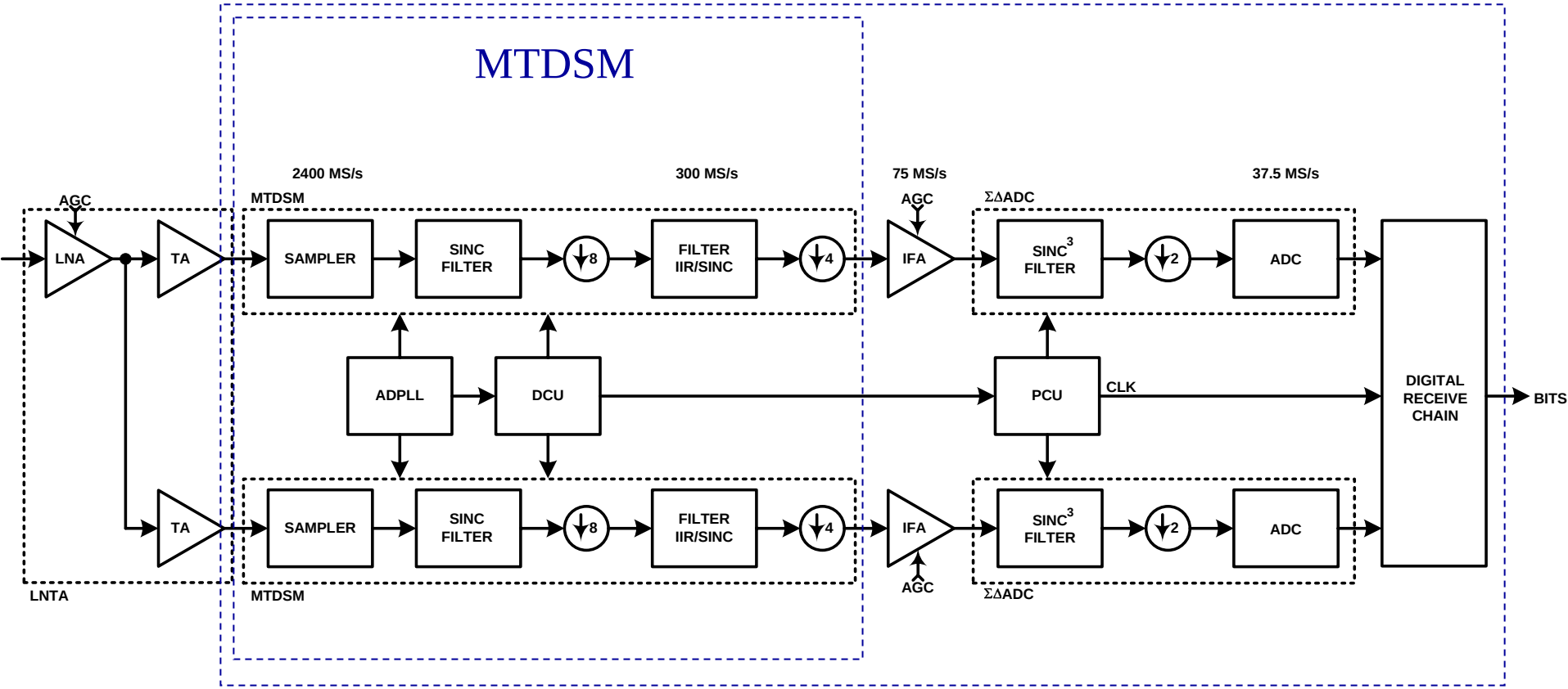
I. Direct RF Sampling

Receiver Architecture Example

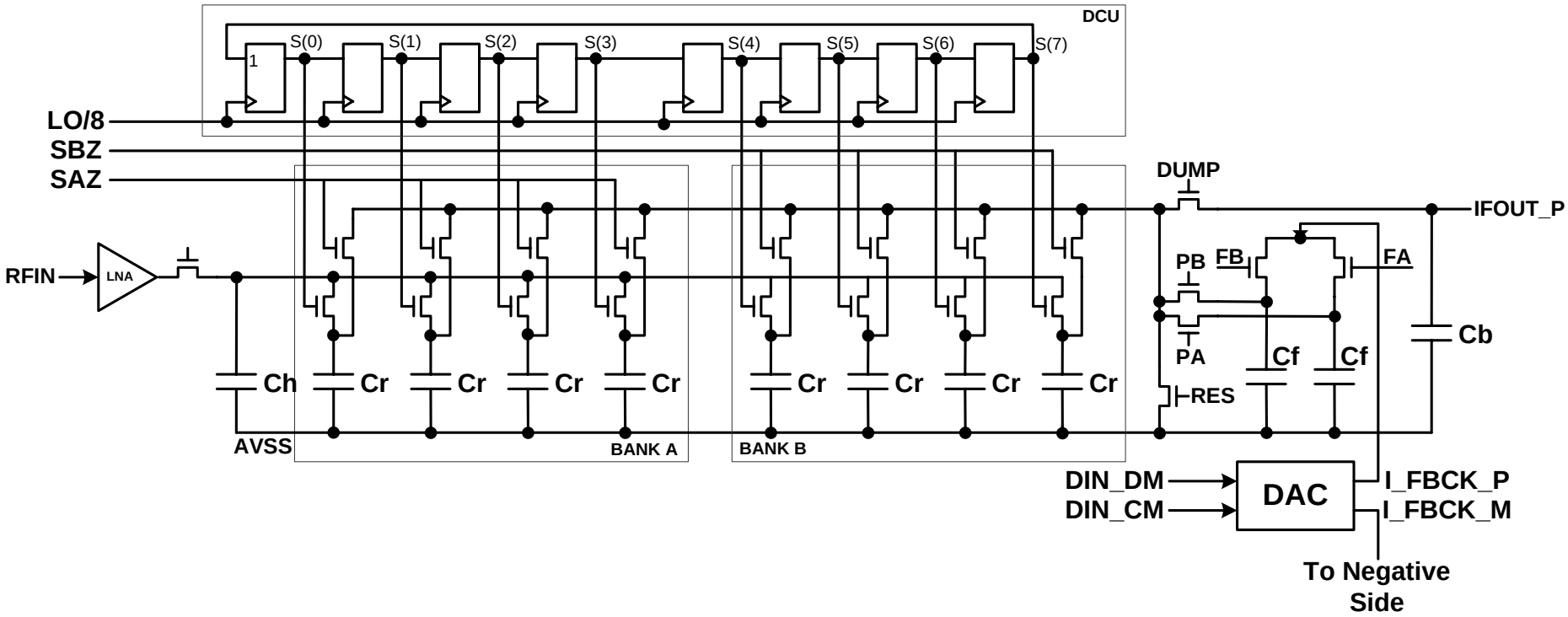


Source: K. Muhammad *et. al.*, "A Discrete-Time Bluetooth Receiver in a 0.13μm Digital CMOS Process," paper 15.1, ISSCC 2004.

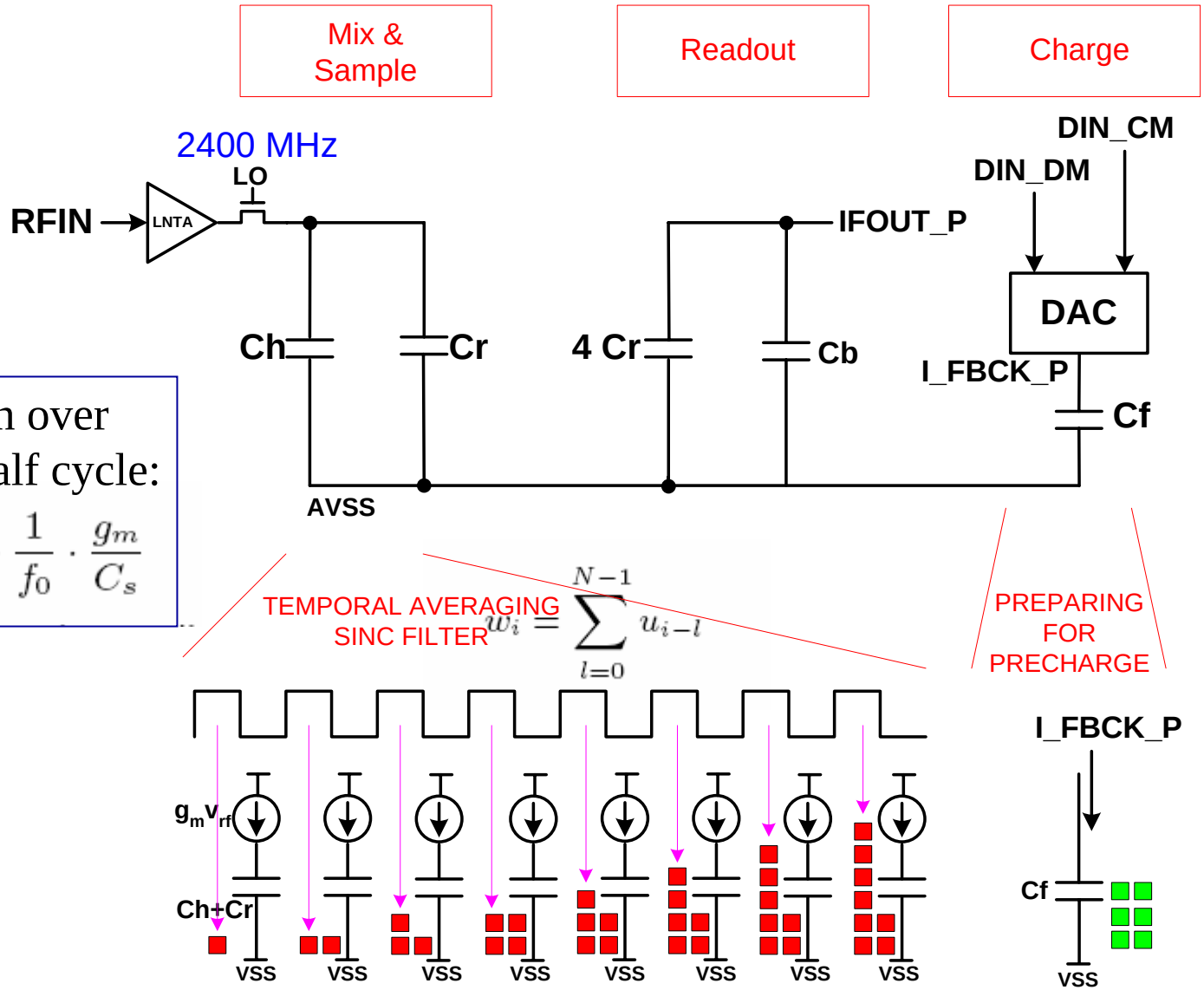
Discrete Time Receiver



MTDSM: Multi-tap Direct Sampling Mixer



MTDSM Sub-Blocks



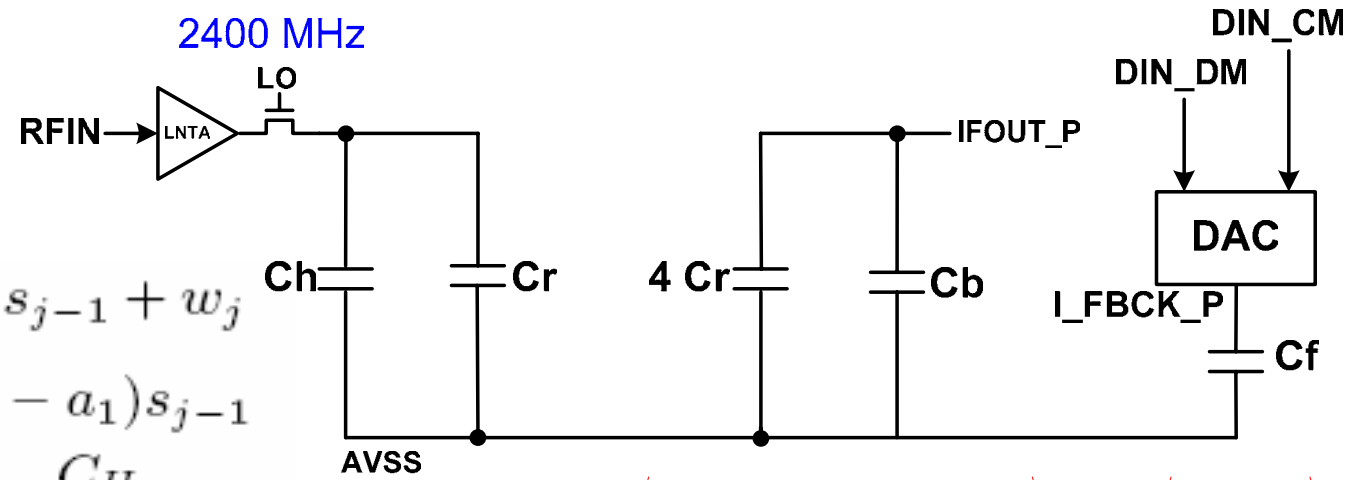
Voltage gain over single RF half cycle:

$$G_{v,RF} = \frac{1}{\pi} \cdot \frac{1}{f_0} \cdot \frac{g_m}{C_s}$$

IIR Filtering

Readout

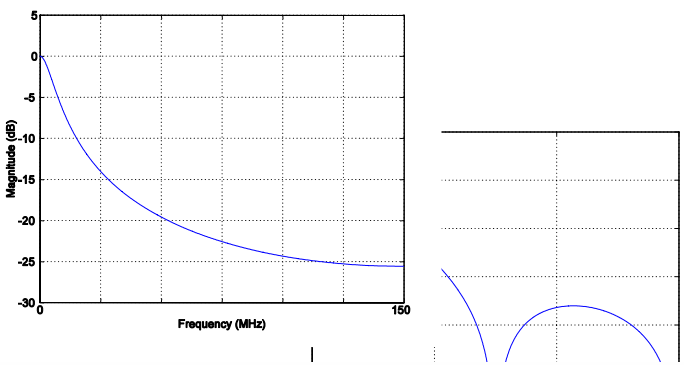
Charge



$$s_j = a_1 s_{j-1} + w_j$$

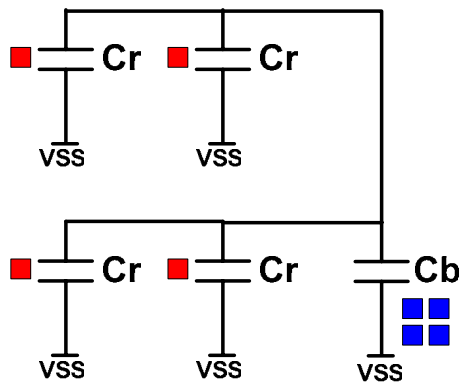
$$x_j = (1 - a_1) s_{j-1}$$

$$a_1 = \frac{C_H}{C_H + C_R}$$

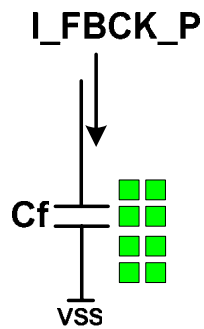


$$f_{c1} = \frac{1}{2\pi}\frac{f_0}{N} \cdot (1 - a_1) = \frac{1}{2\pi}\frac{f_0}{N} \cdot \frac{C_R}{C_H + C_R}$$

SPATIAL AVERAGING
SINC FILTER
+ 1-POLE IIR FILTER



PREPARING
FOR
PRECHARGE



Combined Response

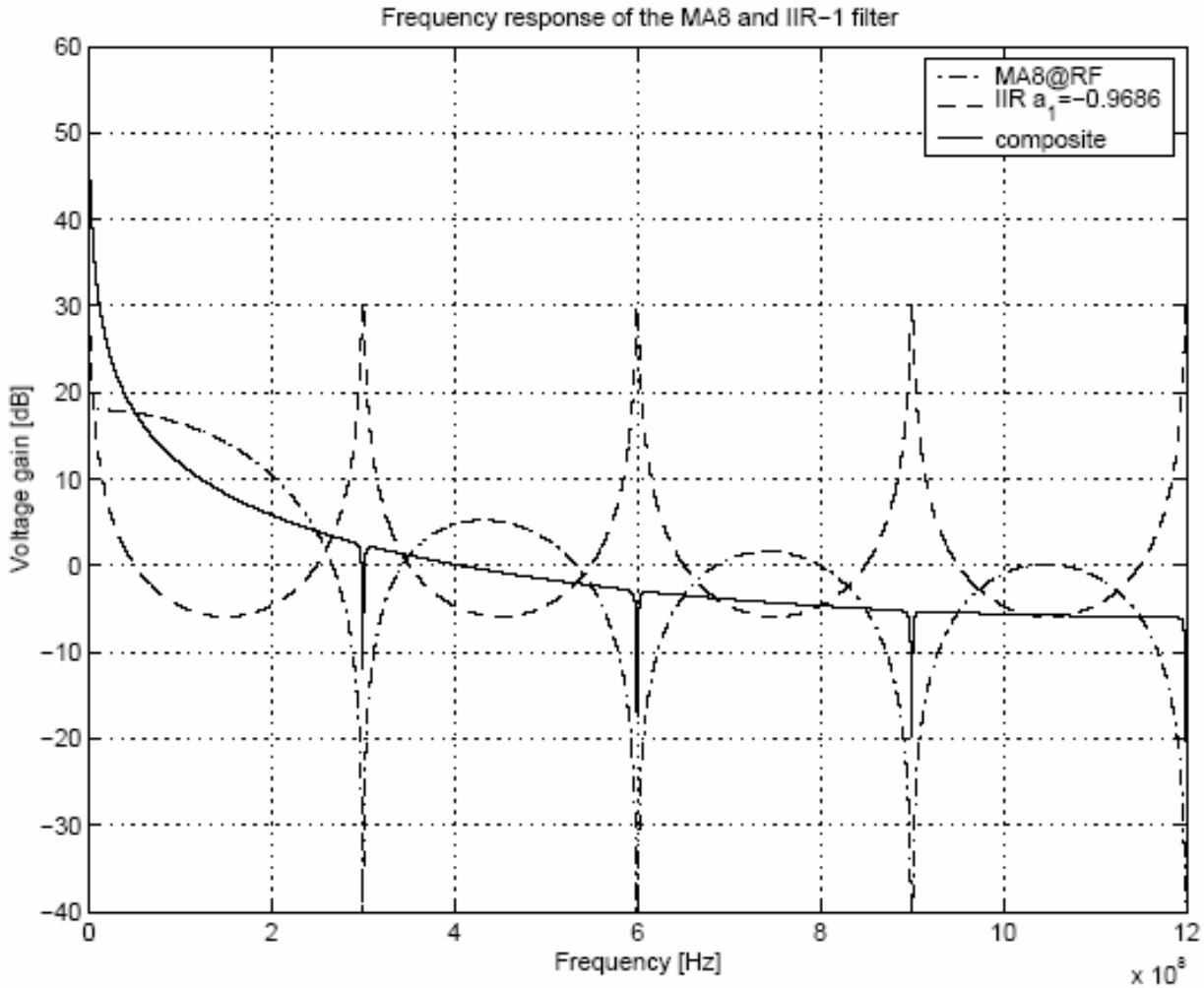
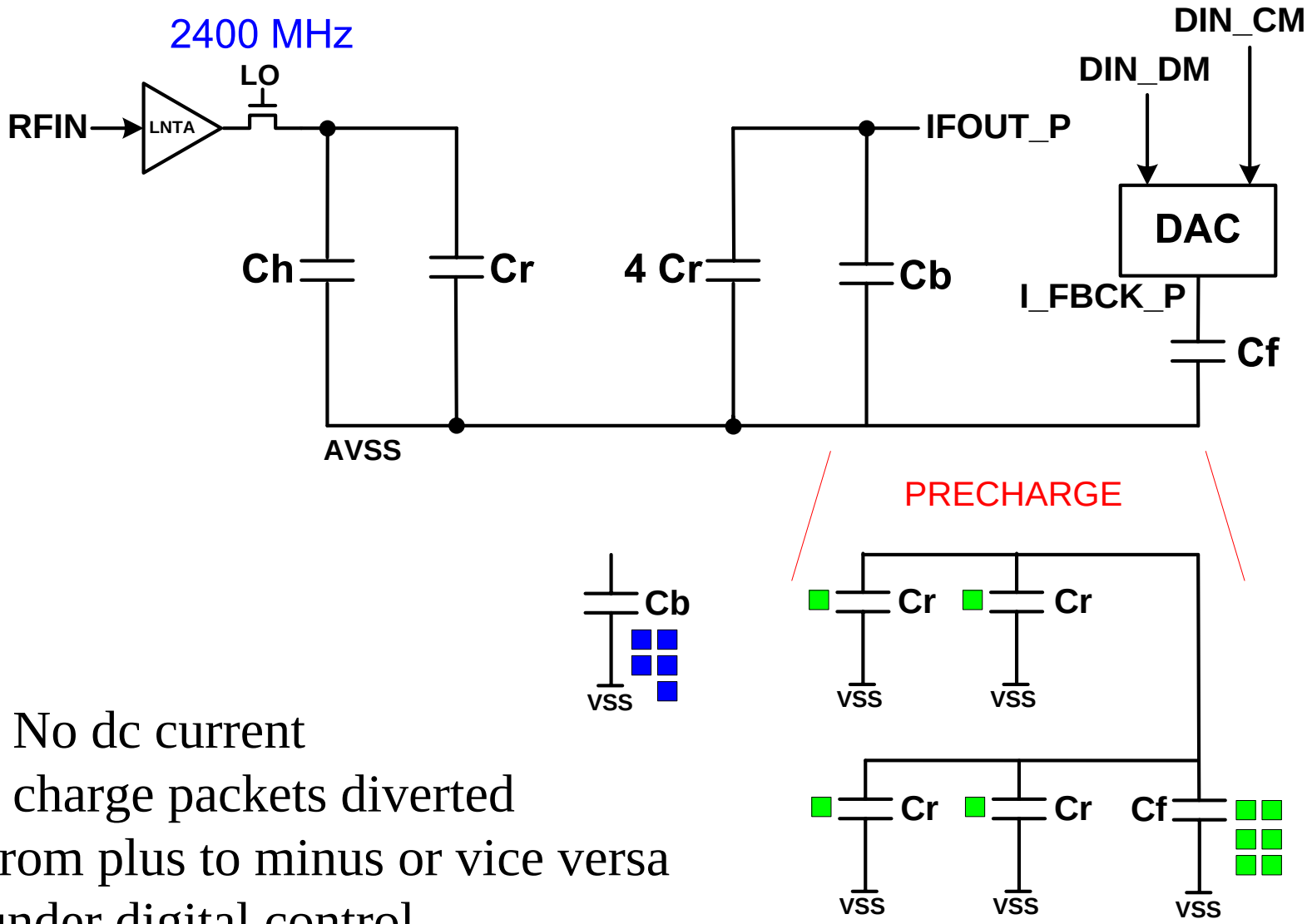


Fig. 5. Transfer function of the temporal moving average with a decimation of 8 and the IIR filter operating at RF/8 rate. The solid line is the composite transfer of both filters.

Ref: K.Muhammad *et. al*, "Direct RF sampling mixer with recursive filtering in charge domain," ISCAS 2004

Offset and CM Control



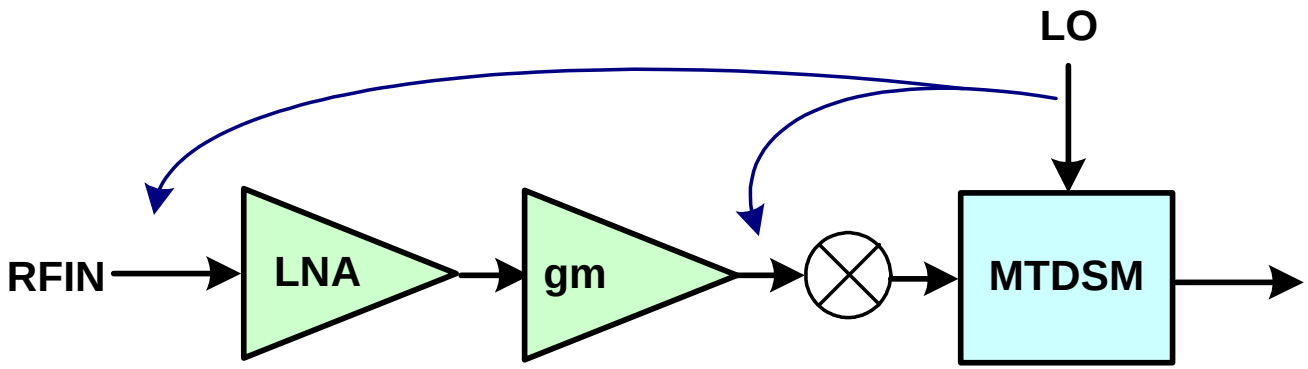
- No dc current
- charge packets diverted

from plus to minus or vice versa under digital control

II. Digital Controls

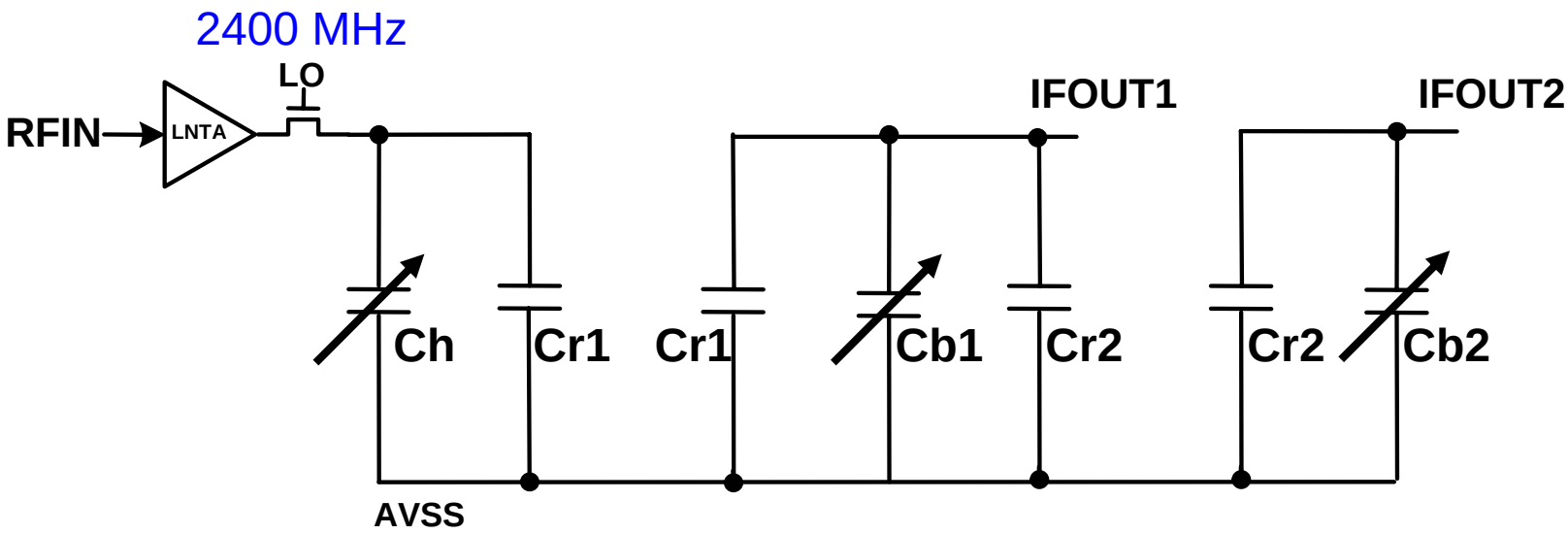
Offsets, Common Mode

- LO leakage and dc offset
- 1/f noise
  - No continuous current flow



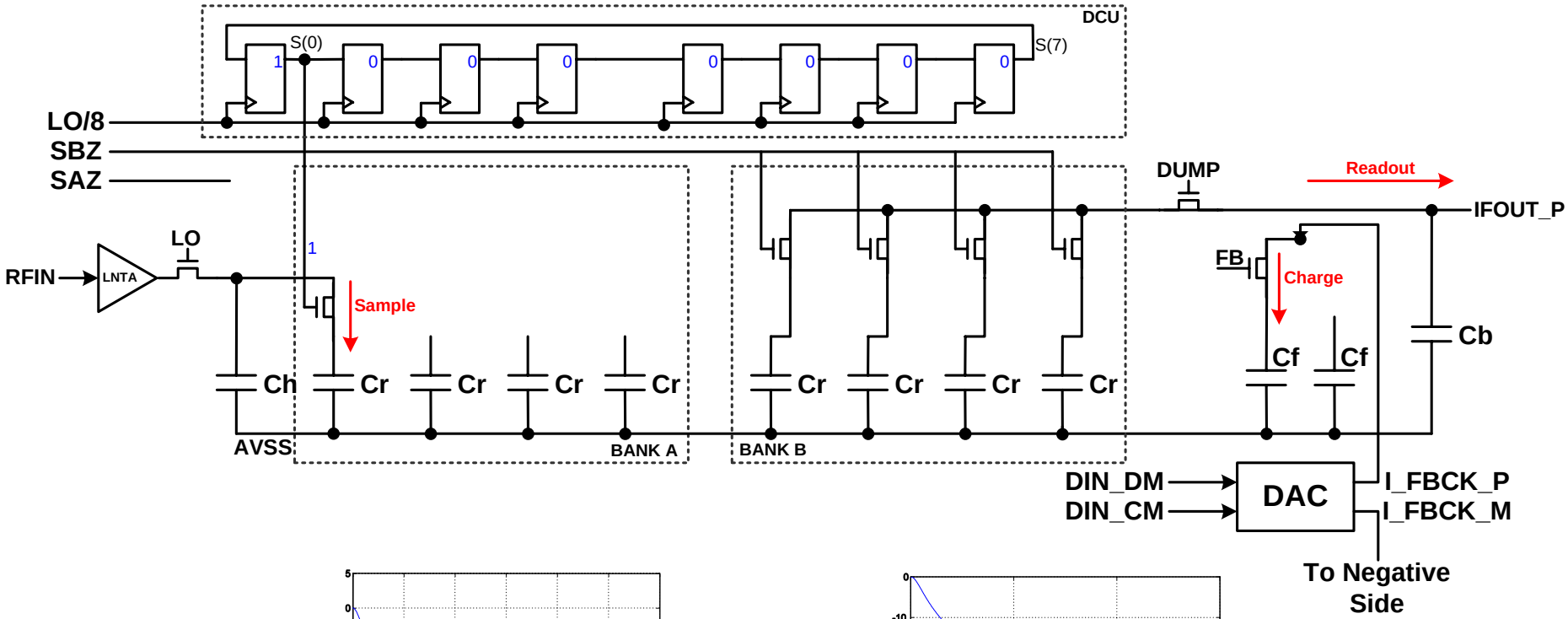
Programmable filtering

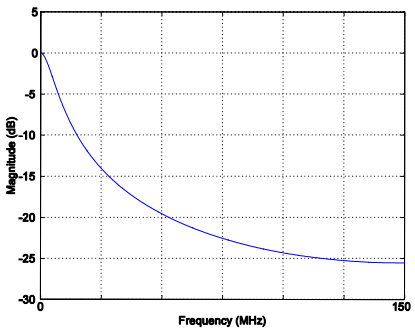
- Corner frequency
- Order
- Rotation rate

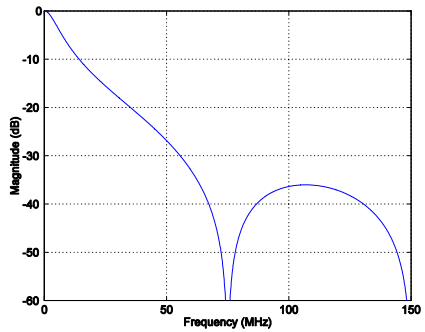


III. Operation

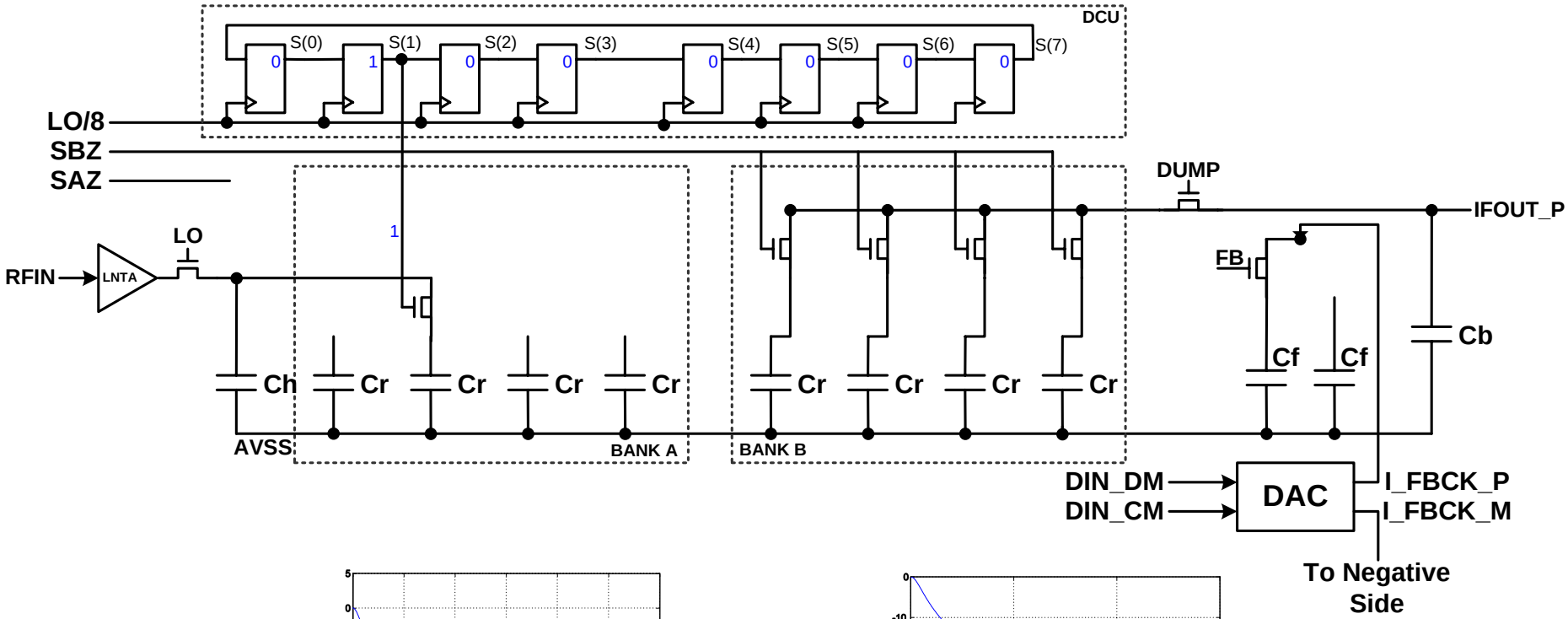
Phase 1

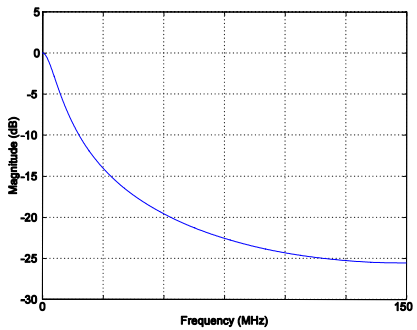

DCU
S(0)
S(7)
1
0
LO/8
SBZ
SAZ
LO
RFIN
LNTA
Sample
Ch
Cr
AVSS
BANK A
BANK B
DUMP
Readout
IFOUT_P
FB
Charge
Cf
Cb
DIN_DM
DIN_CM
DAC
I_FBCK_P
I_FBCK_M
To Negative Side

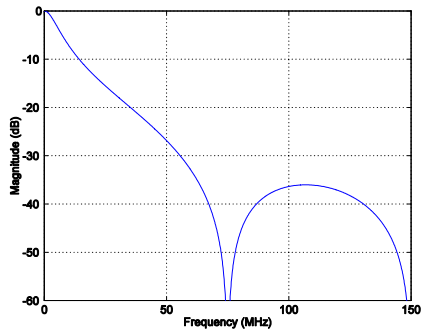

Magnitude (dB)
Frequency (MHz)


Magnitude (dB)
Frequency (MHz)

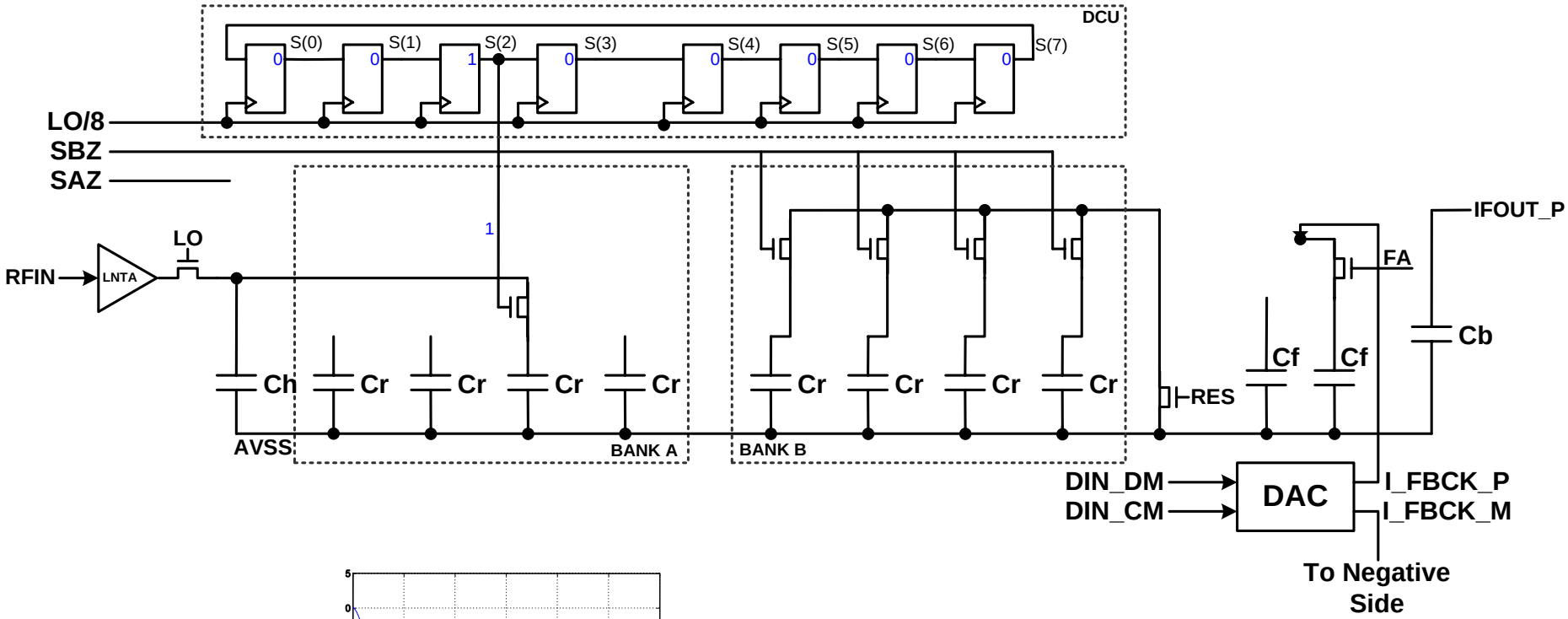
Phase 2

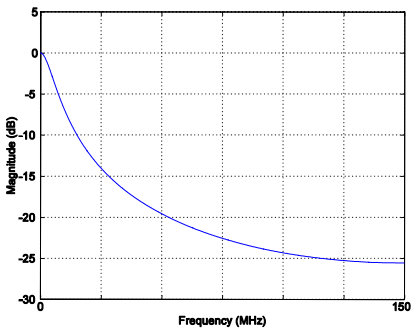

DCU
S(0)
S(1)
S(2)
S(3)
S(4)
S(5)
S(6)
S(7)
LO/8
SBZ
SAZ
LO
RFIN
LNTA
DUMP
IFOUT_P
FB
Cf
Cf
Cb
Ch
Cr
AVSS
BANK A
BANK B
DIN_DM
DIN_CM
DAC
I_FBCK_P
I_FBCK_M
To Negative Side


Magnitude (dB)
Frequency (MHz)

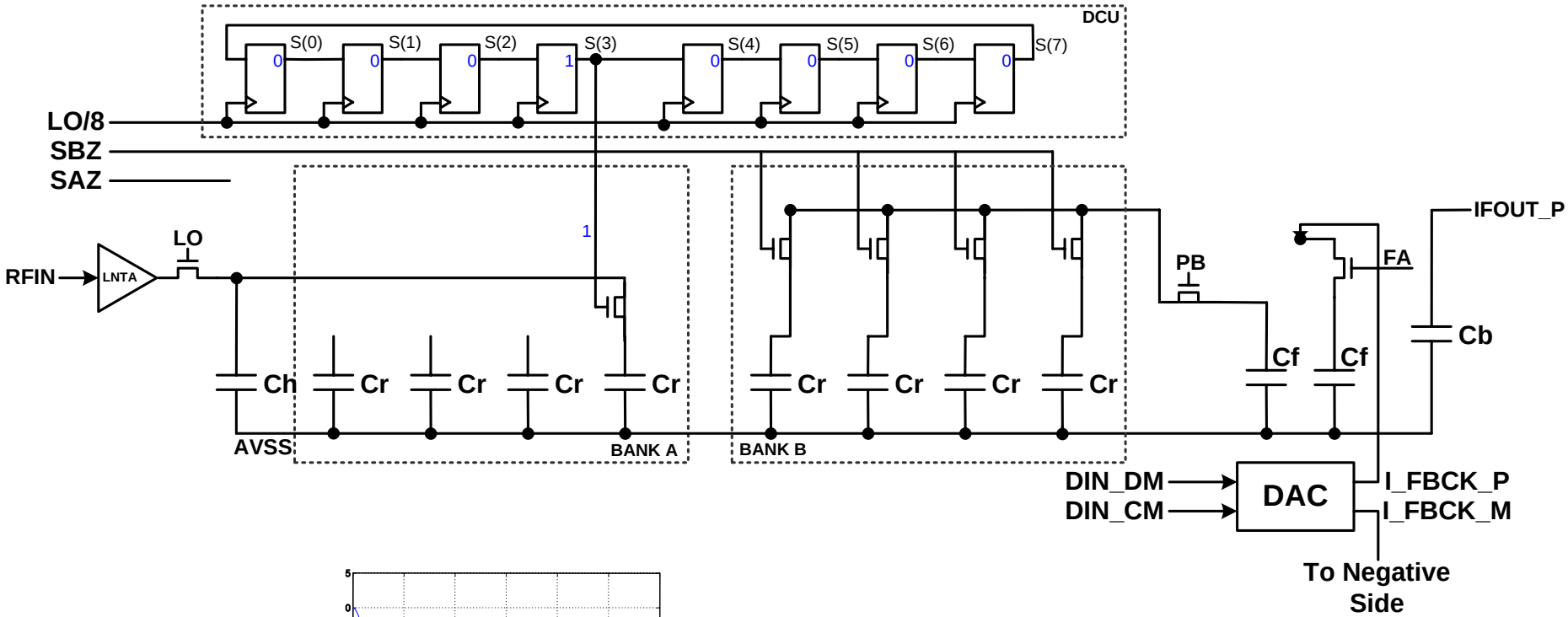

Magnitude (dB)
Frequency (MHz)

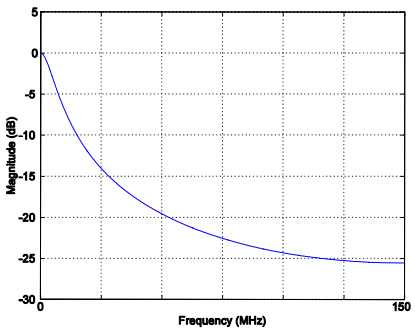
Phase 3


DCU
S(0)
S(1)
S(2)
S(3)
S(4)
S(5)
S(6)
S(7)
LO/8
SBZ
SAZ
LO
RFIN
LNTA
Ch
Cr
AVSS
BANK A
BANK B
RES
Cf
FA
Cb
IFOUT_P
DIN_DM
DIN_CM
DAC
I_FBCK_P
I_FBCK_M
To Negative Side

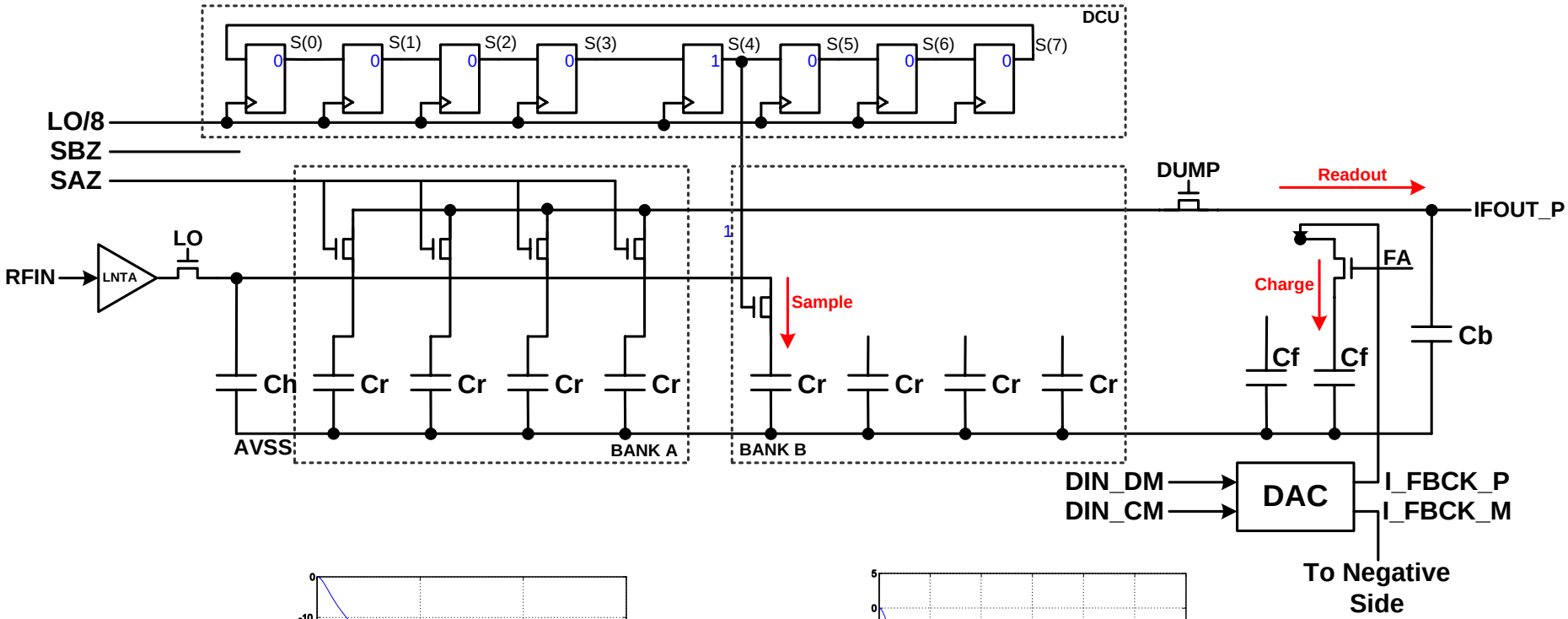

Magnitude (dB)
Frequency (MHz)
5
0
-5
-10
-15
-20
-25
-30
0
150

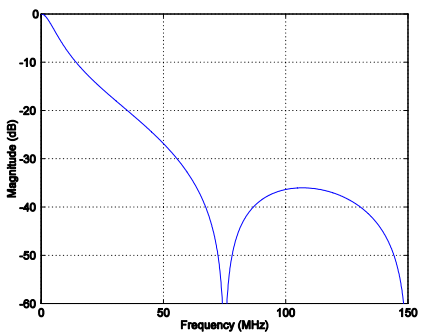
Phase 4

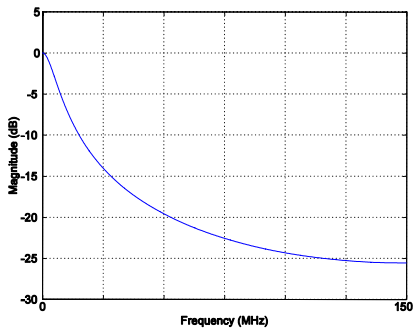

DCU
S(0)
S(1)
S(2)
S(3)
S(4)
S(5)
S(6)
S(7)
0
0
0
1
0
0
0
0
LO/8
SBZ
SAZ
LO
RFIN
LNTA
1
Ch
Cr
Cr
Cr
Cr
Cr
Cr
Cr
Cr
AVSS
BANK A
BANK B
PB
Cf
Cf
FA
IFOUT_P
Cb
DIN_DM
DIN_CM
DAC
I_FBCK_P
I_FBCK_M
To Negative Side


5
0
-5
-10
-15
-20
-25
-30
Magnitude (dB)
0
150
Frequency (MHz)

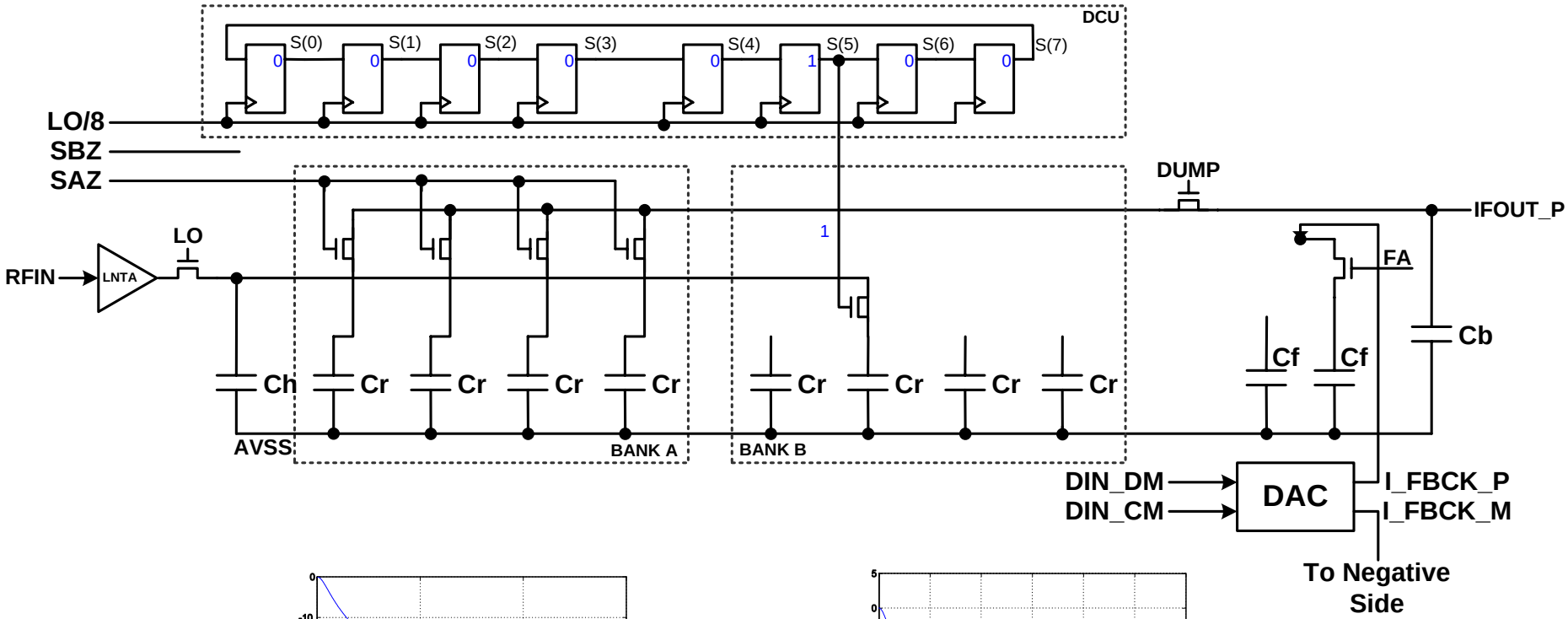
Phase 5

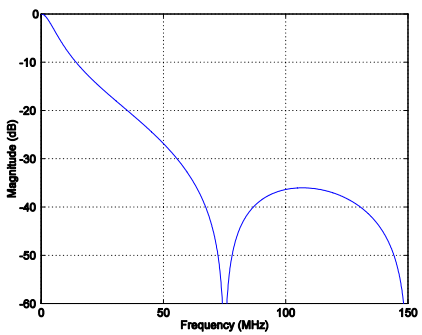

DCU
S(0)
S(1)
S(2)
S(3)
S(4)
S(5)
S(6)
S(7)
LO/8
SBZ
SAZ
DUMP
Readout
IFOUT_P
RFIN
LNTA
LO
Sample
FA
Charge
Cb
Cf
Cf
Ch
Cr
AVSS
BANK A
BANK B
DIN_DM
DIN_CM
DAC
I_FBCK_P
I_FBCK_M
To Negative Side

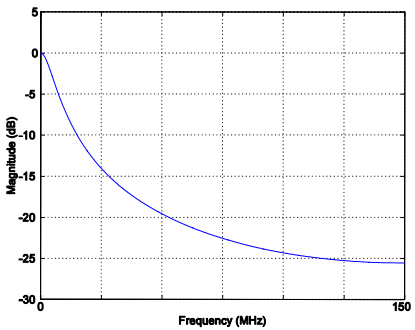

Magnitude (dB)
Frequency (MHz)


Magnitude (dB)
Frequency (MHz)

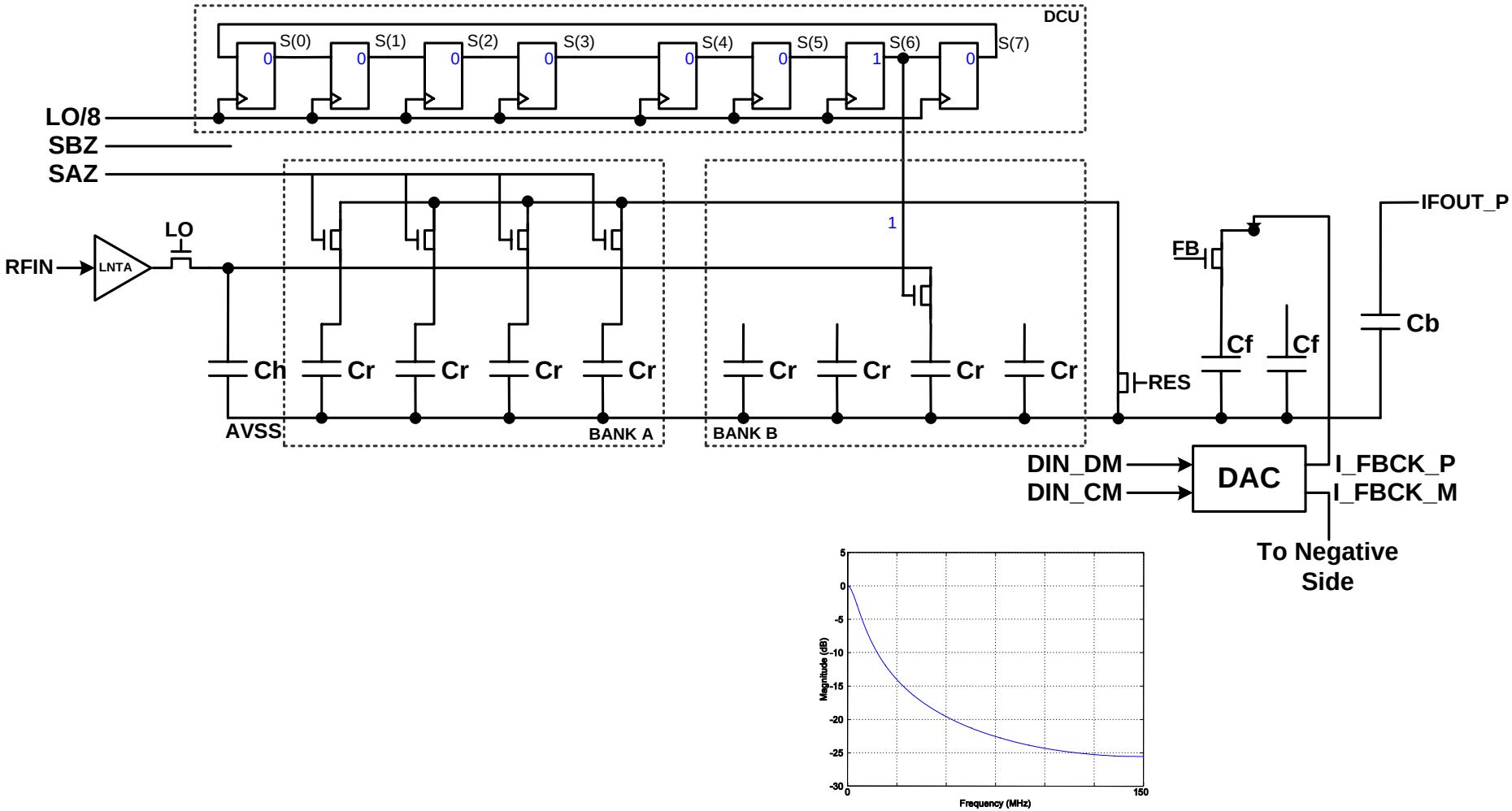
Phase 6


DCU
S(0)
S(1)
S(2)
S(3)
S(4)
S(5)
S(6)
S(7)
0
0
0
0
0
1
0
0
LO/8
SBZ
SAZ
DUMP
IFOUT_P
LO
RFIN
LNTA
1
FA
Cb
Cf
Cf
Ch
Cr
Cr
Cr
Cr
Cr
Cr
Cr
Cr
AVSS
BANK A
BANK B
DIN_DM
DIN_CM
DAC
I_FBCK_P
I_FBCK_M
To Negative Side

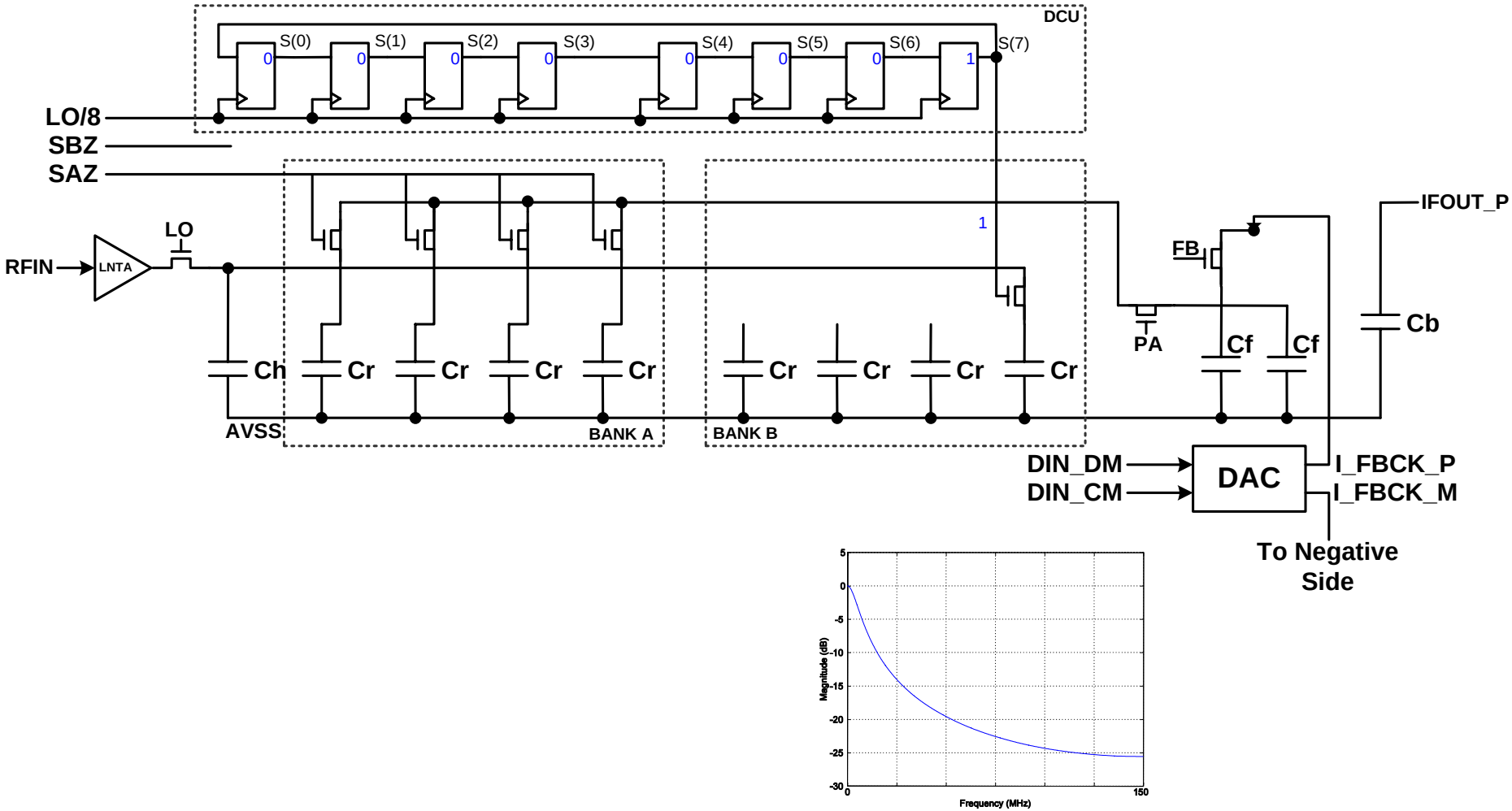

Magnitude (dB)
Frequency (MHz)
0
-10
-20
-30
-40
-50
-60
0
50
100
150


Magnitude (dB)
Frequency (MHz)
5
0
-5
-10
-15
-20
-25
-30
0
150

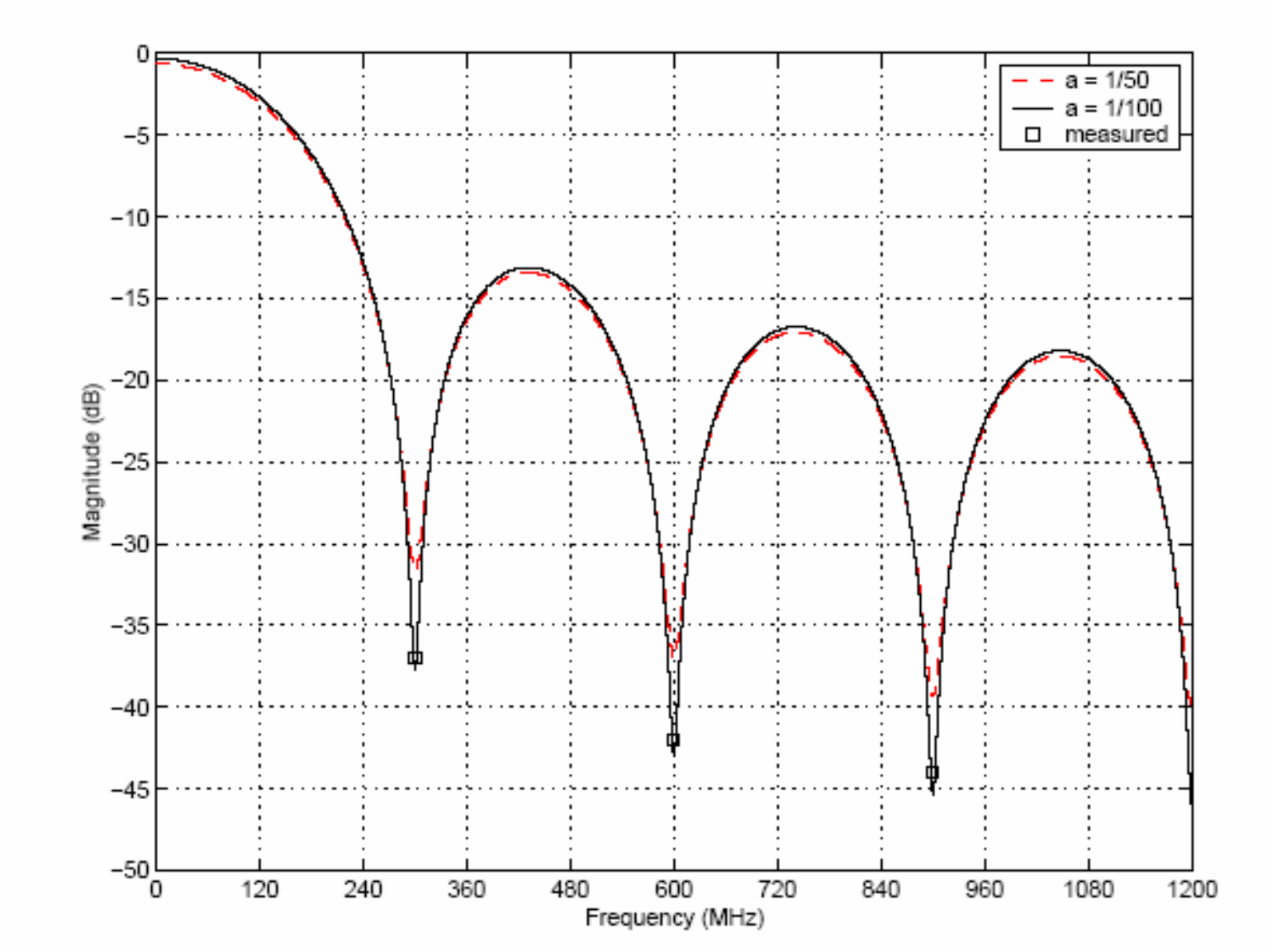
Phase 7


DCU
S(0)
S(1)
S(2)
S(3)
S(4)
S(5)
S(6)
S(7)
LO/8
SBZ
SAZ
LO
RFIN
LNTA
Ch
Cr
AVSS
BANK A
BANK B
RES
FB
Cf
Cb
IFOUT_P
DIN_DM
DIN_CM
DAC
I_FBCK_P
I_FBCK_M
To Negative Side
Magnitude (dB)
Frequency (MHz)

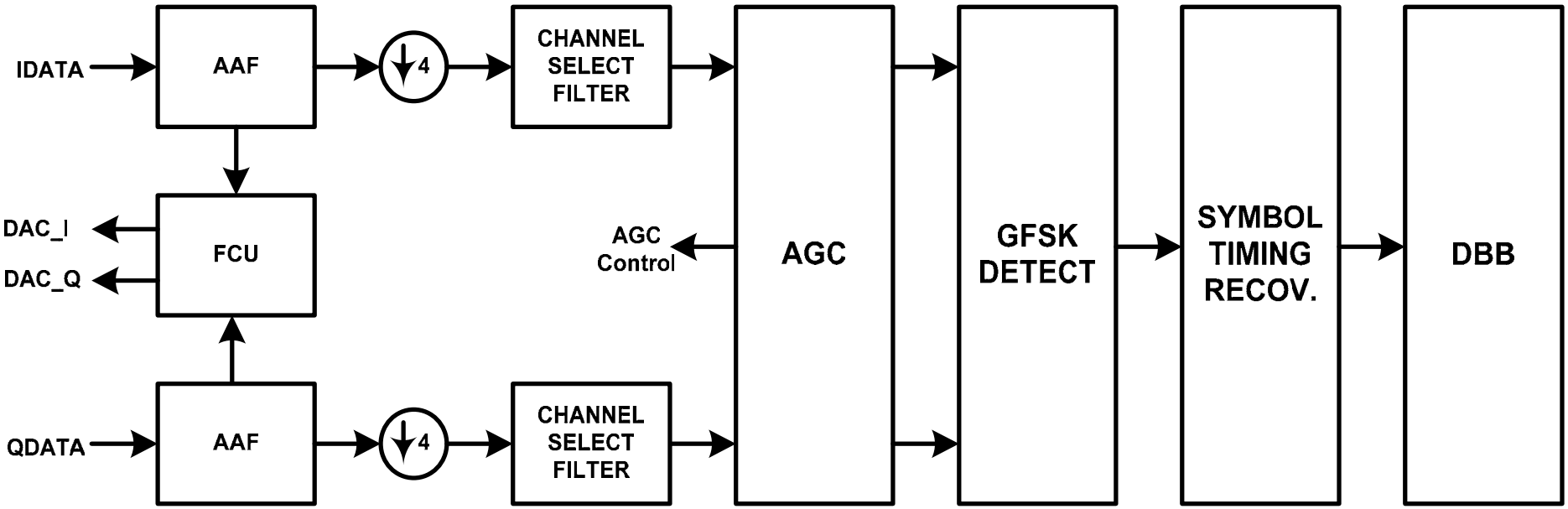
Phase 8


DCU
S(0)
S(1)
S(2)
S(3)
S(4)
S(5)
S(6)
S(7)
0
0
0
0
0
0
0
1
LO/8
SBZ
SAZ
LO
RFIN
LNTA
1
FB
IFOUT_P
PA
Cf
Cf
Cb
Ch
Cr
Cr
Cr
Cr
Cr
Cr
Cr
Cr
AVSS
BANK A
BANK B
DIN_DM
DIN_CM
DAC
I_FBCK_P
I_FBCK_M
To Negative Side
Magnitude (dB)
Frequency (MHz)
5
0
-5
-10
-15
-20
-25
-30
0
150

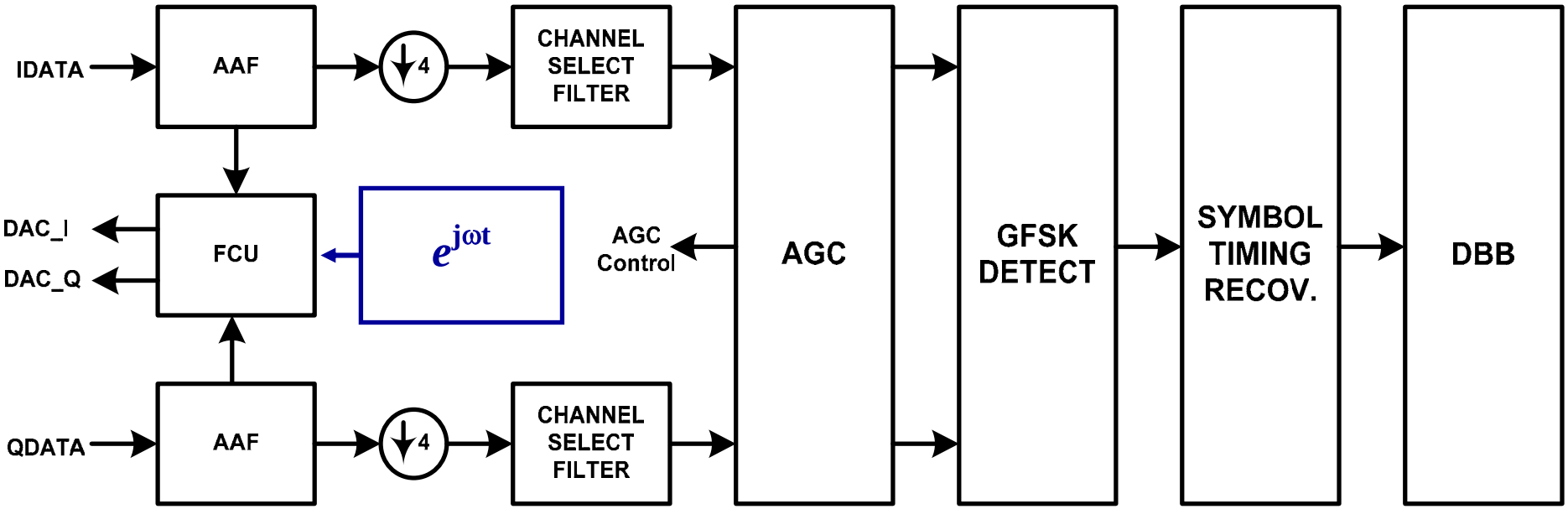
MTDSM Sinc Response



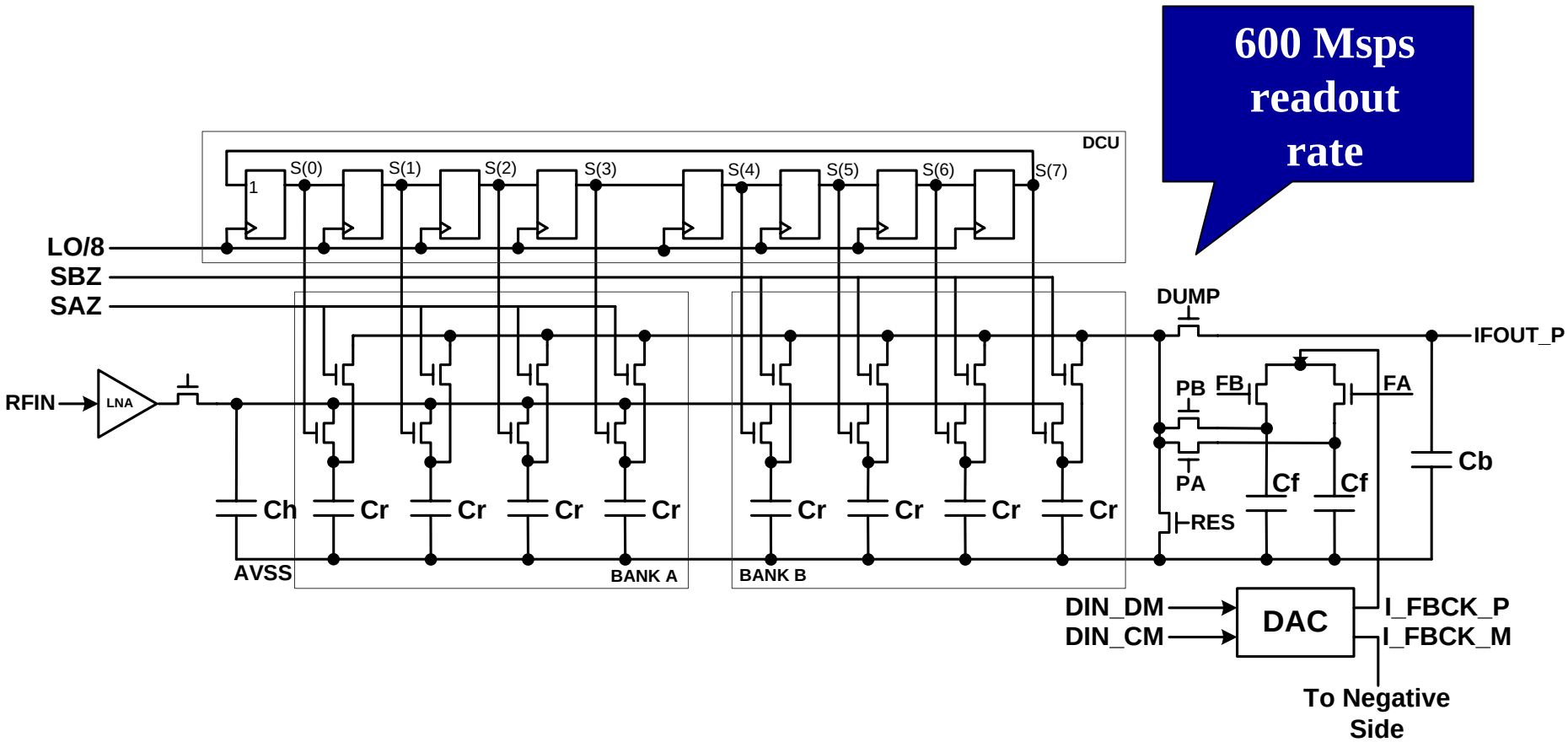
Digital Receiver Backend



Calibration



Higher Rate Sampling: 2-pole system



Bank A ↑ ↑ ↑ ↑ ← Dump/Precharge →

Bank B ← Dump/Precharge → ↑ ↑ ↑ ↑

MTDSM Advantages

- Mixer embedding a filter
  - Anti-aliasing
  - Adjacent channel interferer rejection
    - Reduces linearity requirements of ABE
    - Reduces dynamic range requirements of ABE
      - No further filtering required
  - Modular and scalable
  - Programmable
    - Filtering performance
    - Noise performance
    - Feedback configuration

IV. Results

Implementation

- Digital deep-submicron 0.13μm CMOS process with no analog extensions
- RF and analog integrated with digital

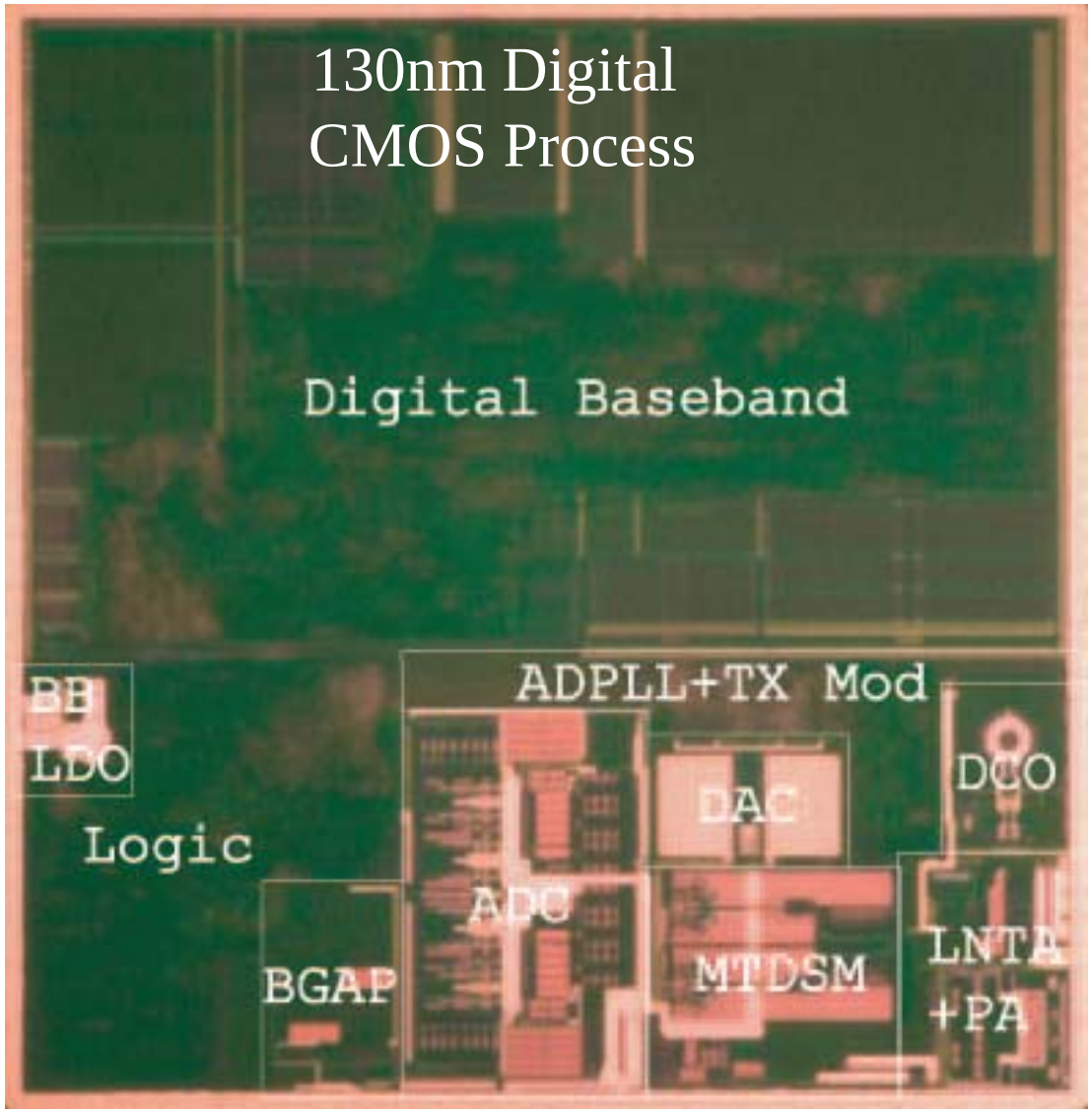
Interconnect material	copper
Minimum metal pitch	0.35 um
Transistor nom. voltage	1.5 V
L drawn	0.11 um
L effective	0.08 um
Gate oxide	29 A

Measurement Results

- Passed the official Bluetooth qualification
- C/I = 10.5 dB, Max. Input = -5dBm, DBB = 4 mA

Work	Technology	TX Current (mA)	RX Current (mA)	Sensitivity dBm
This one	0.13u,1.575V	25	37	-83
[1]	0.18u 2.5-3.0V	35.5	30.5	-78
[2]	0.18u 2.7V	37	39	-83
[3]	0.25u ?V	36	45	≤ -70
[4]	0.25u 2.5V	<70	<50	-80

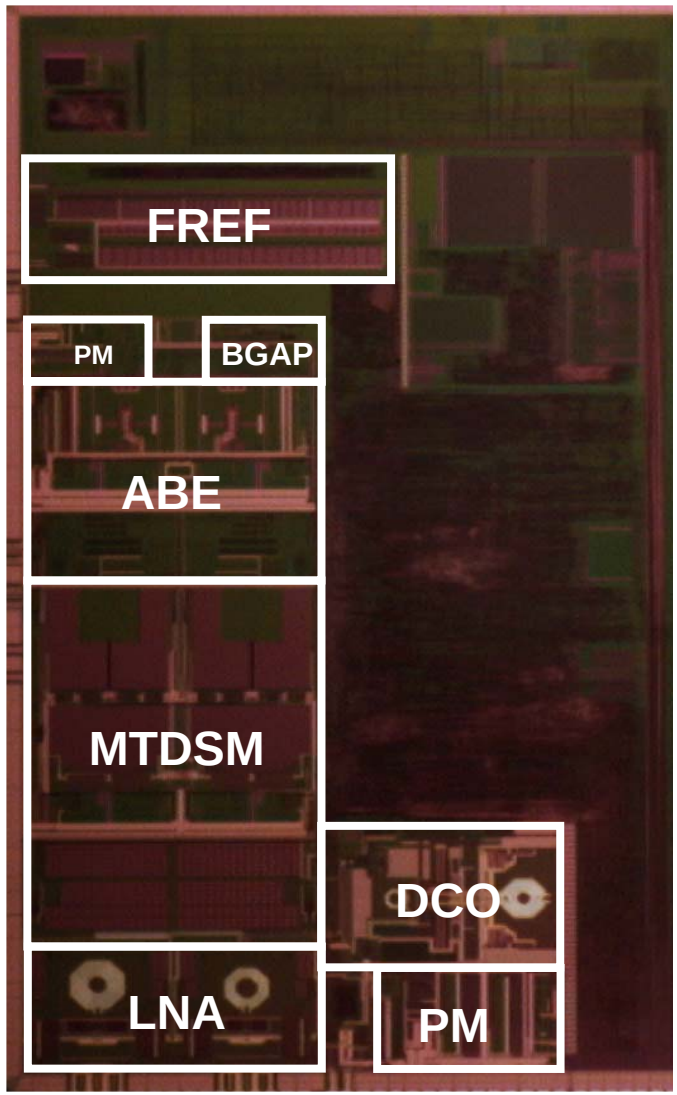
Chip Micrograph - Bluetooth



- Single-chip Bluetooth radio
- RX path
  - Direct RF Sampling
  - Discrete time RX path with $\Sigma\Delta$ ADC
- 1.575V / 37mA current consumption in continuous RX mode

Chip Micrograph – GSM/GPRS

90nm Digital CMOS Process



RX path

- Direct RF Sampling
- Discrete time RX, ΣΔADC@500Msps
- 1.4V design
- Scalable architecture

Conclusions

- The first commercial discrete time wireless RX at par with continuous time architectures
  - Bluetooth
  - GSM/GPRS
  - …
- Direct rf sampling followed by discrete-time signal processing
- Performance demonstrated in single-chip fully-compliant radios

References

[1] P. T. M. van Zeijl et al., “A Buetooth Radio in 0.18um CMOS,” *ISSCC Dig. Tech. Papers*, pp. 86–87, Feb. 2002.

[2] G. Chang et al., “A Direct-Conversion Single-Chip Radio-Modem for Bluetooth,” *ISSCC Dig.Tech. Papers,* pp. 88–89, Feb. 2002.

[3] J. Cheah et al., “Design of a Low-Cost Integrated 0.25um CMOS Bluetooth SOC in 16.5mm2 Silicon Area,” *ISSCC Dig. Tech. Papers,* pp. 90–91, Feb. 2001.

[4] Eynde et al., “A Fully-Integrated Single-Chip SoC for Bluetooth,” *ISSCC Dig. Tech. Papers*, pp. 196–197, Feb. 2001.