Sigma-Delta ADC Tutorial and Latest Development in 90 nm CMOS for SoC

Jinseok Koh

Wireless Analog Technology Center

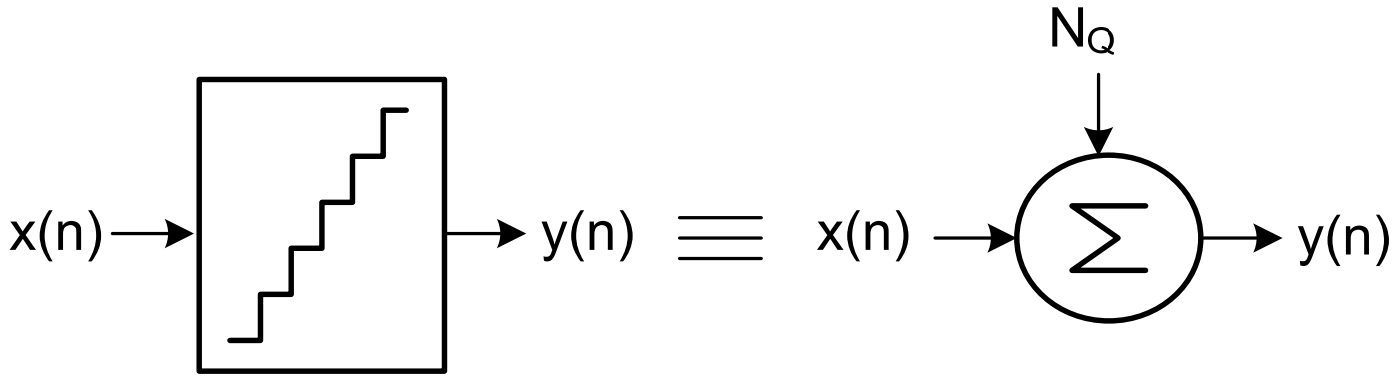
Texas Instruments Inc.

Dallas, TX

Outline

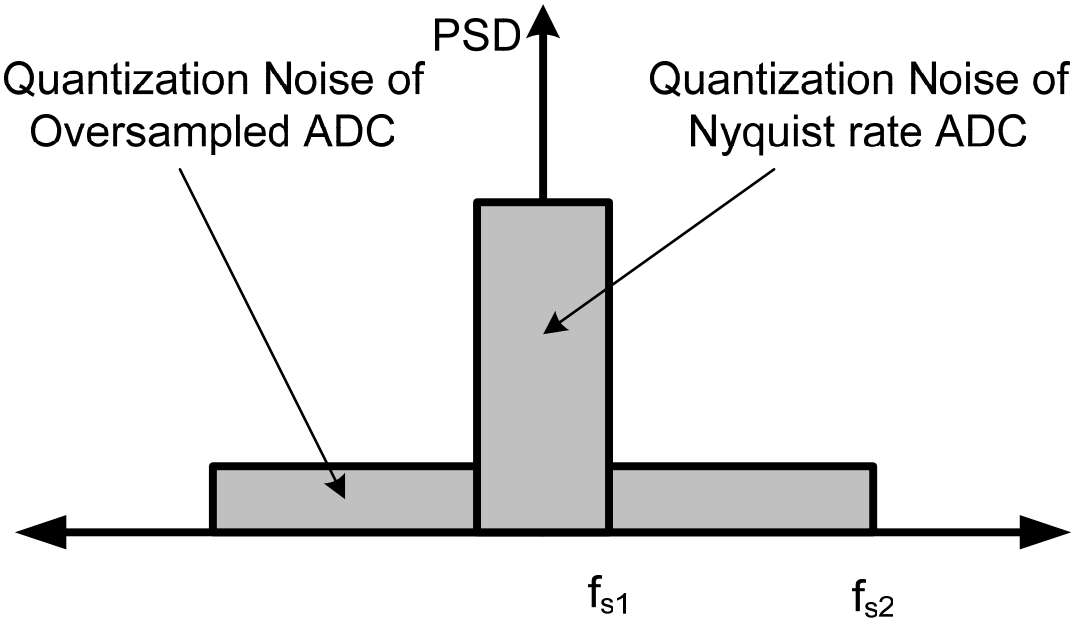
- Fundamentals for ADCs
- Over-sampling and Noise shaping
- Sigma-Delta ADC
- Double Sampling Technique
- 2nd Order Single Amplifier Sigma-Delta ADC
- Implementation in 90nm CMOS for SoC
- Conclusions

Modeling of Quantizer



- **Quantizer is non-linear building block**
  - Need modeling for simplifying the analysis
- **White additive noise assumptions**
  - It is not fulfilled in many applications, However
  - It makes analysis easy and makes possible the use of z-tansformation

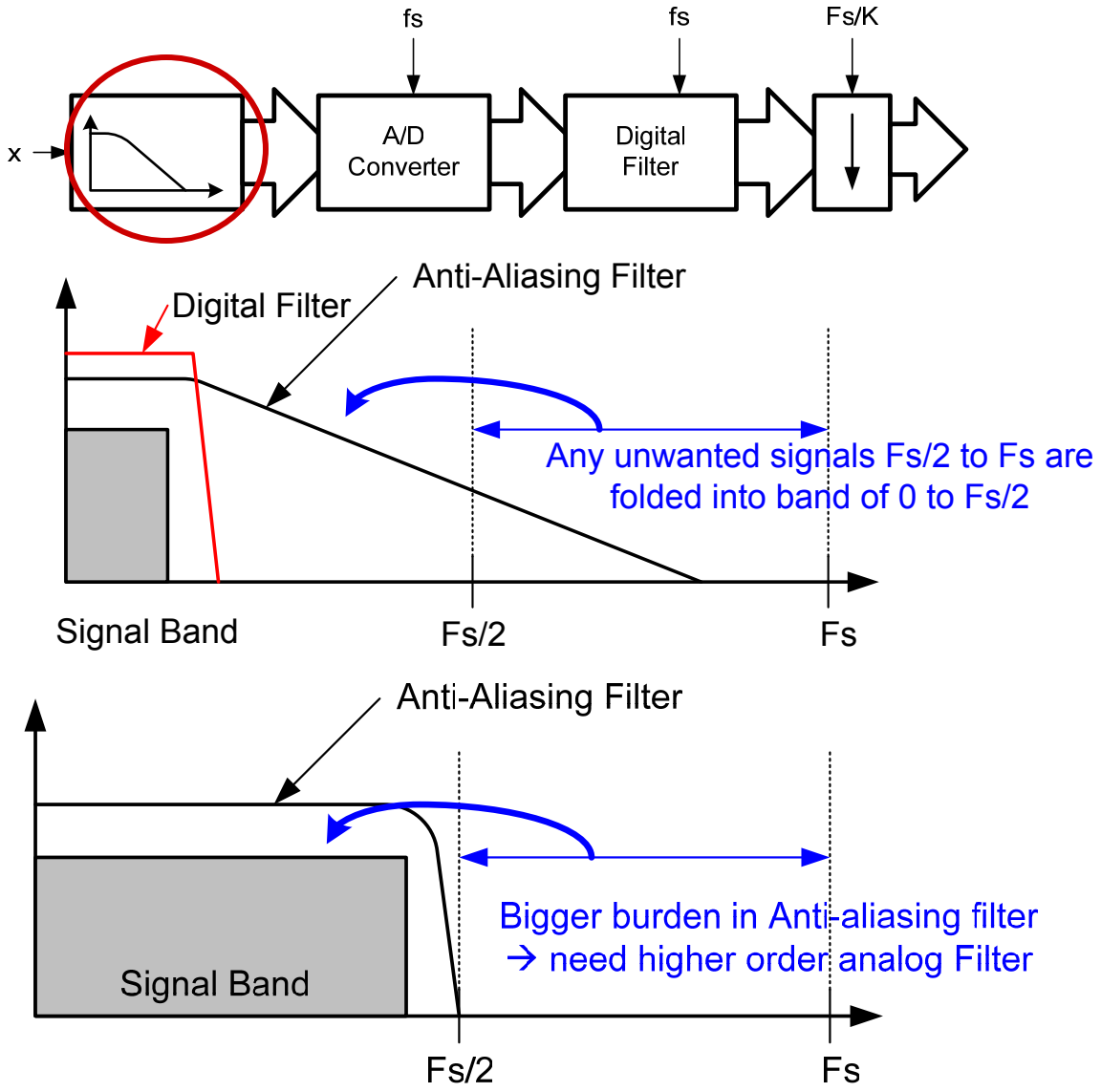
Quantization Noise



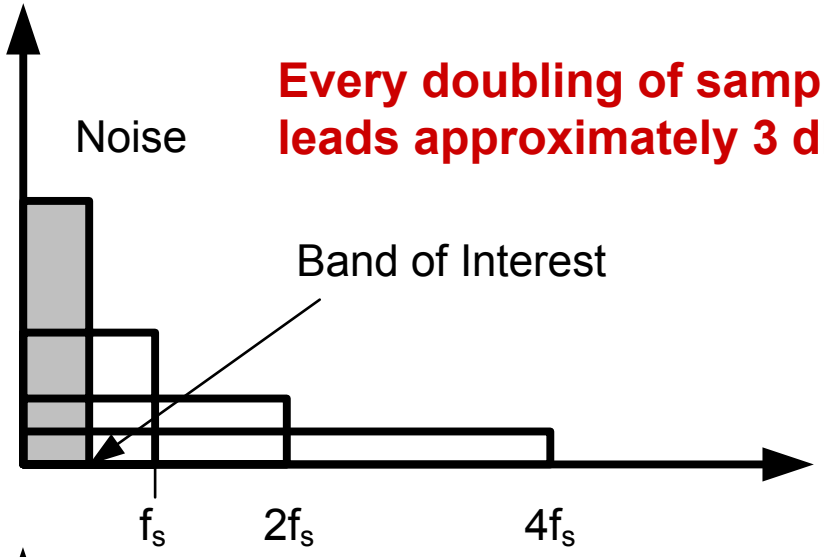
- **Quantity of in-band noise depends on the over-sampling ratio**
  - SNR = $10\log(\sigma_x^2) - 10\log(\sigma_n^2) + 3.01r$(dB), where
  - σ_x^2 and σ_n^2 are input signal power and in-band noise power respectively, and
  - r is defined by over-sampling ratio, $f_s/2f_b=2^r$

Pervez M. Aziz, "An overview of sigma-delta converters," IEEE Signal processing Magazine, pp 61-84, Jan. 1996

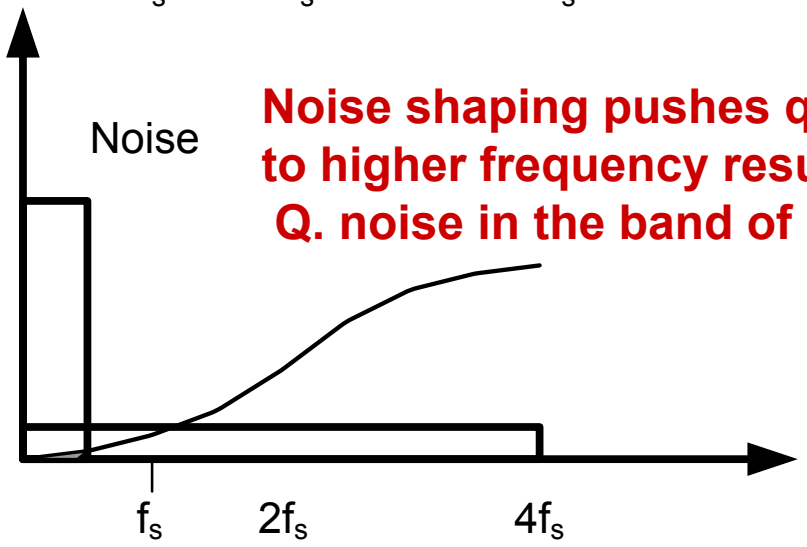
Nyquist Rate vs. Oversampled



Over-sampling and Noise Shaping

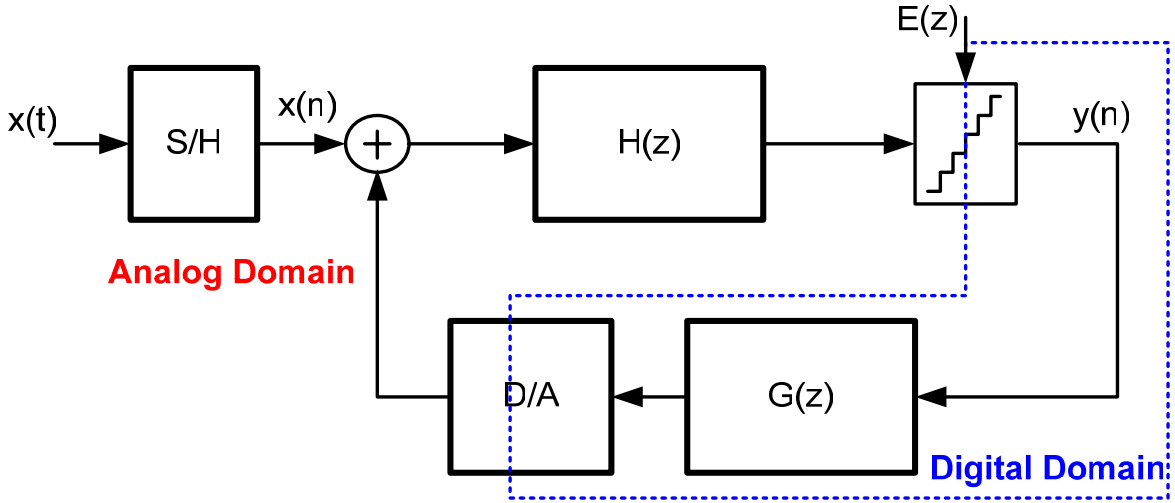


Every doubling of sampling frequency leads approximately 3 dB enhancement in SNR



Noise shaping pushes quantization noise to higher frequency resulting in suppressing Q. noise in the band of interest

How to Shape the noise?

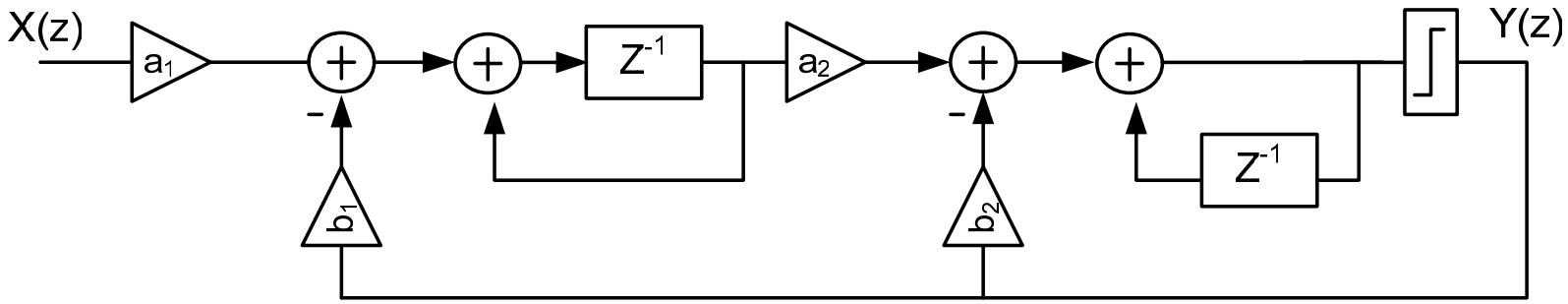


$$Y(z) = \underbrace{\frac{H(z)}{1+H(z)G(z)}}_{STF} \cdot X(z) + \underbrace{\frac{1}{1+H(z)G(z)}}_{NTF} \cdot E(z)$$

If $H(z) = z^{-1}/1-z^{-1}$ and $G(z)=1$, NTF and STF will be:

$$NTF = \frac{Y(z)}{E(z)} = 1 - Z^{-1} \qquad STF = \frac{Y(z)}{X(z)} = Z^{-1}$$

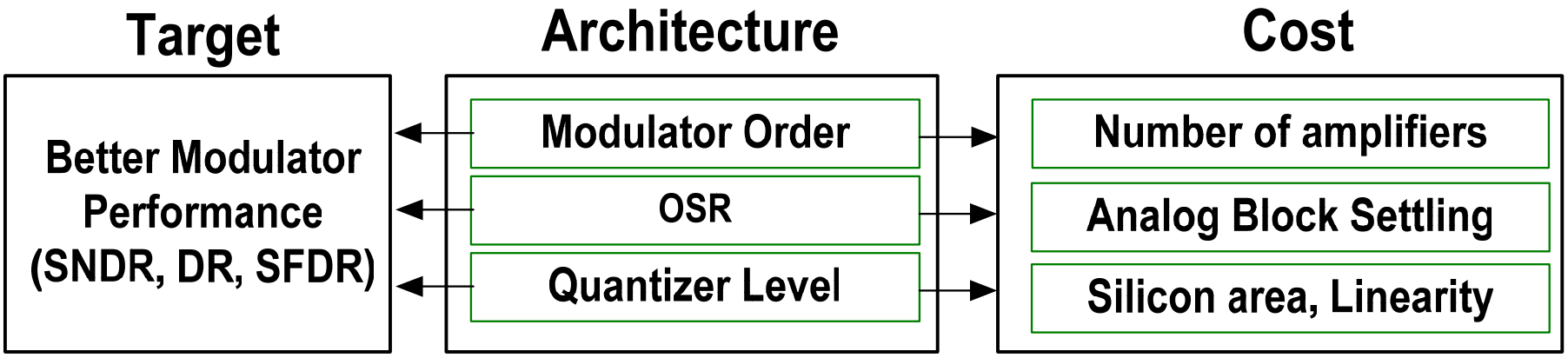
Example, 2_{nd} order Sigma-Delta ADC



Summary

- **Sigma-delta ADC provide trade-offs between:**
  - **Power consumption,**
  - **Over-sampling ratio (*OSR*)**
  - **System performance (*SNR*)**
- **High OSR implies:**
  - **Lower number of quantization levels**
  - **Lower modulator order, but**
  - **More demanding settling requirements for the analog building blocks**

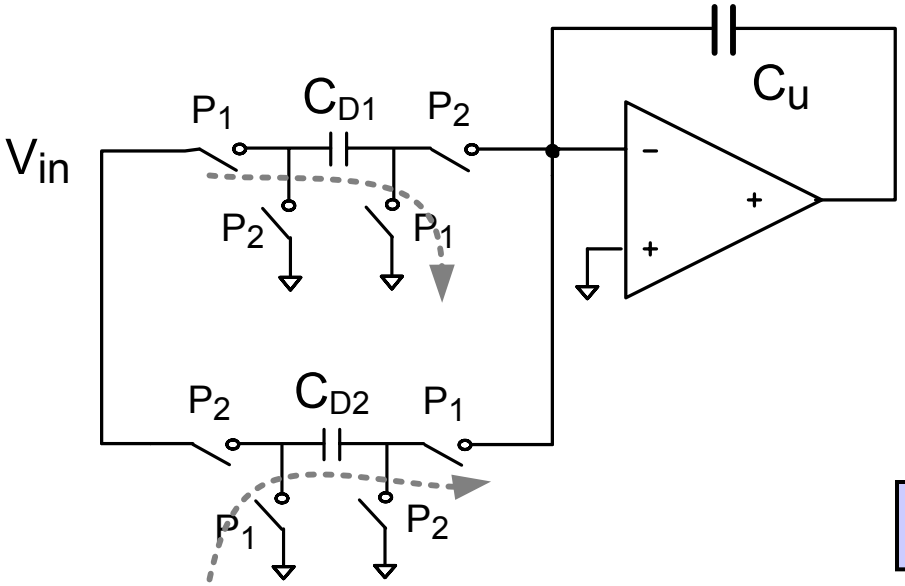
Objectives

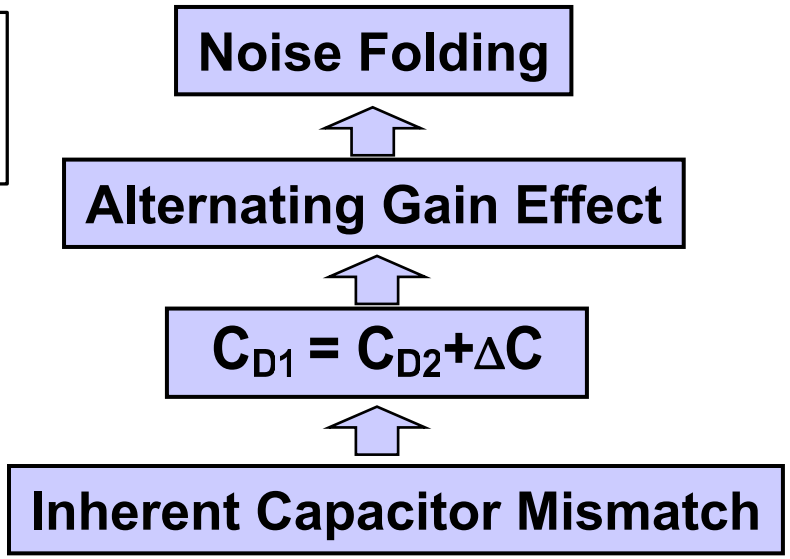


- **For a given performance requirement, power consumption and area are optimized by:**
  - **Increasing sampling frequency → Double sampling technique**
  - **Increasing modulator order → Single Amplifier topology**
  - **Higher number of levels in Quantizer → 5-level quantizer with ILA**

Double sampling

- **Advantages:**
  - **Efficient technique to double the OSR**
    - **Doesn't need faster op-amp settling**
    - **Provides improvement of SQNR by 6n+3 dB (n=order)**
- **Disadvantage:**
  - **Mismatch between capacitors creates noise folding**

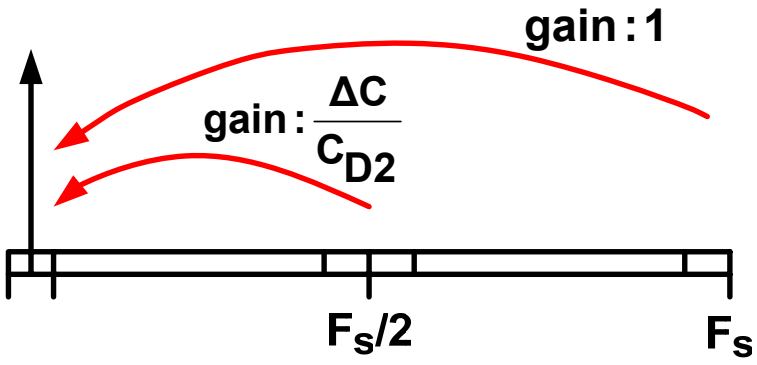
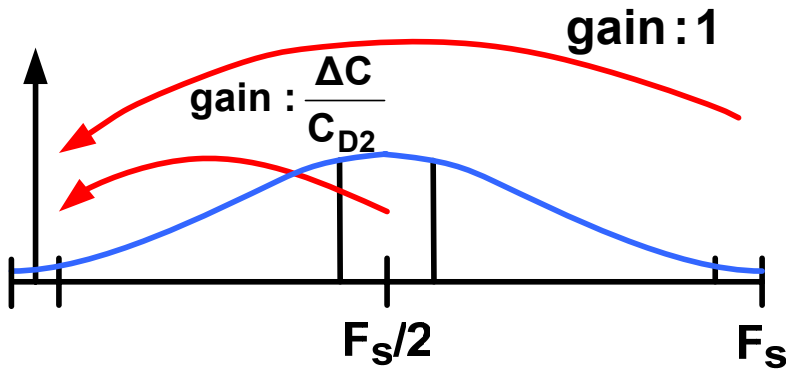




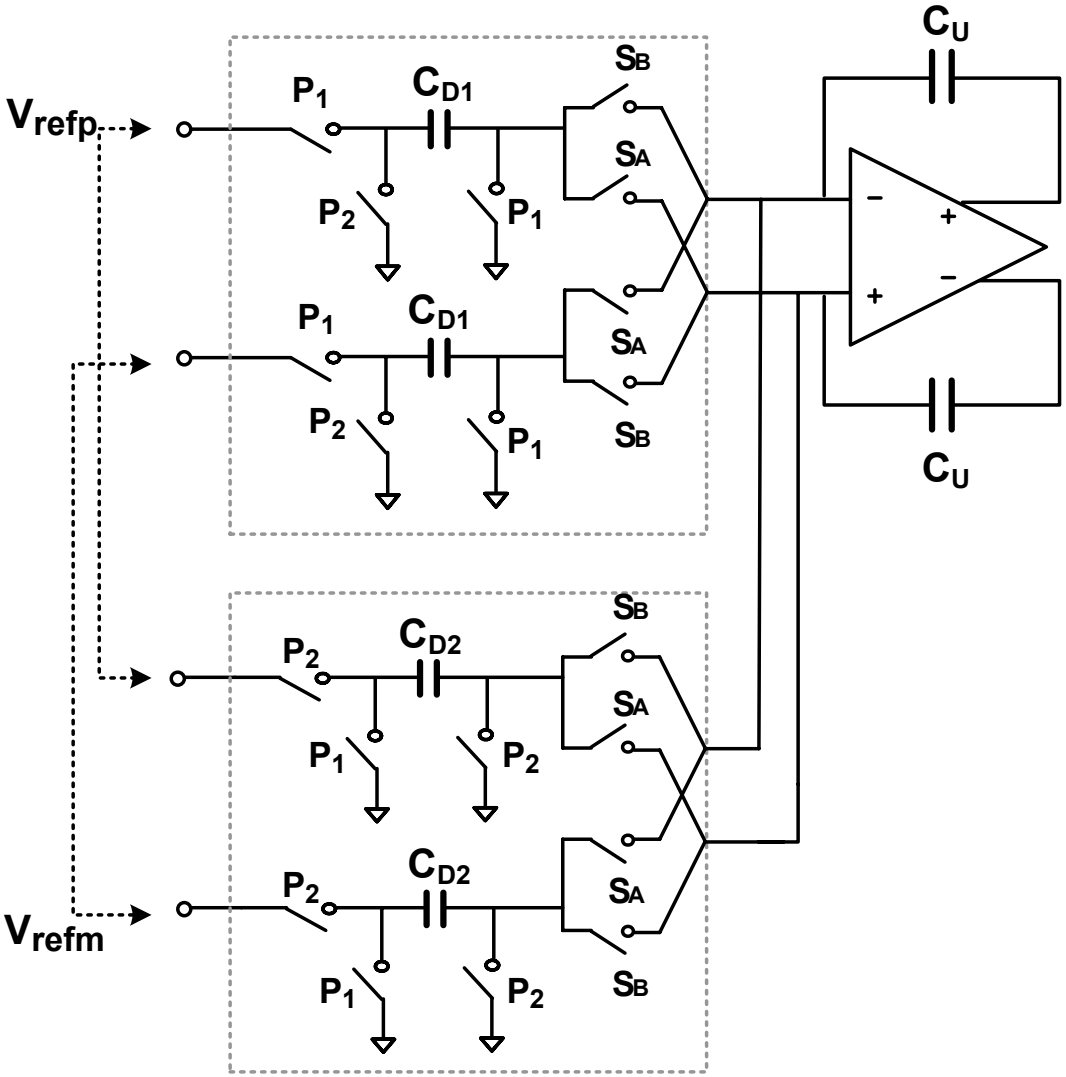
Noise Folding In Double Sampling

- **Alternating gain effect**

  → Noise at $F_s/2$ is folded into Signal bandwidth

Noise folding (Input sampling circuit)	Noise folding (DAC in feedback path)
	
• Noise at $F_s/2$ is suppressed by - Anti-aliasing filter - Pre-filtering	• No filtering on quantization noise

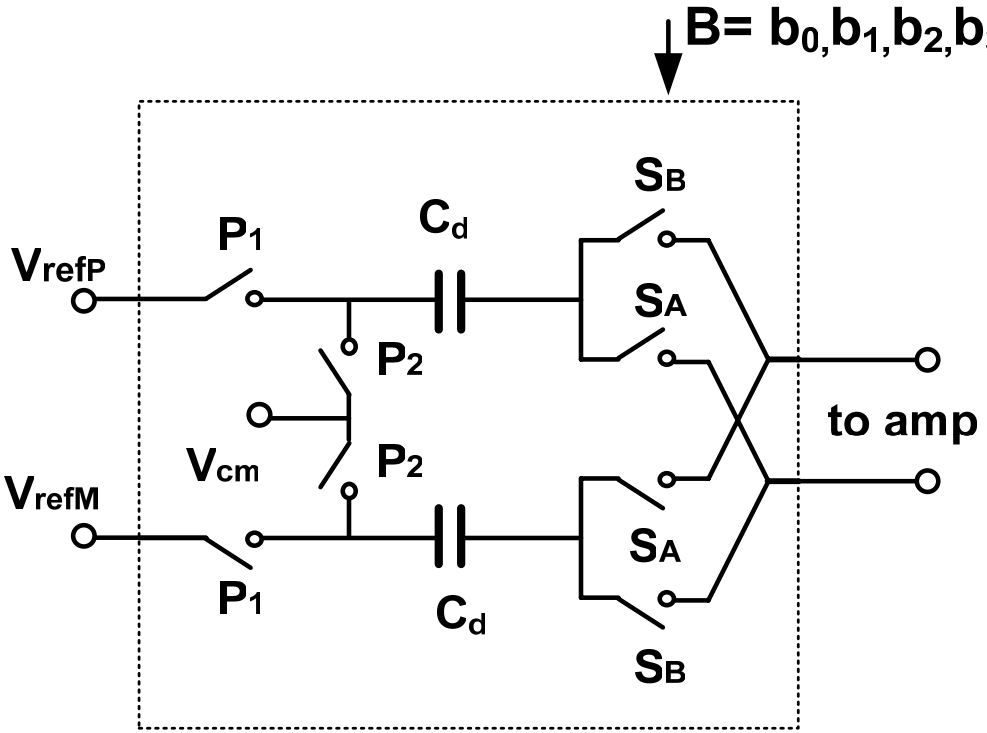
Conventional Double Sampling DAC



- On P1 phase,
  Stored charge in C_{D1} :
  $C_{D1}(V_{refp}-V_{refm})$
- On P2 phase,
  Stored charge in C_{D2} :
  $C_{D2}(V_{refp}-V_{refm})$

- Requires two sets of switched capacitor DACs
- Mismatch on stored charge causes alternating gain effect

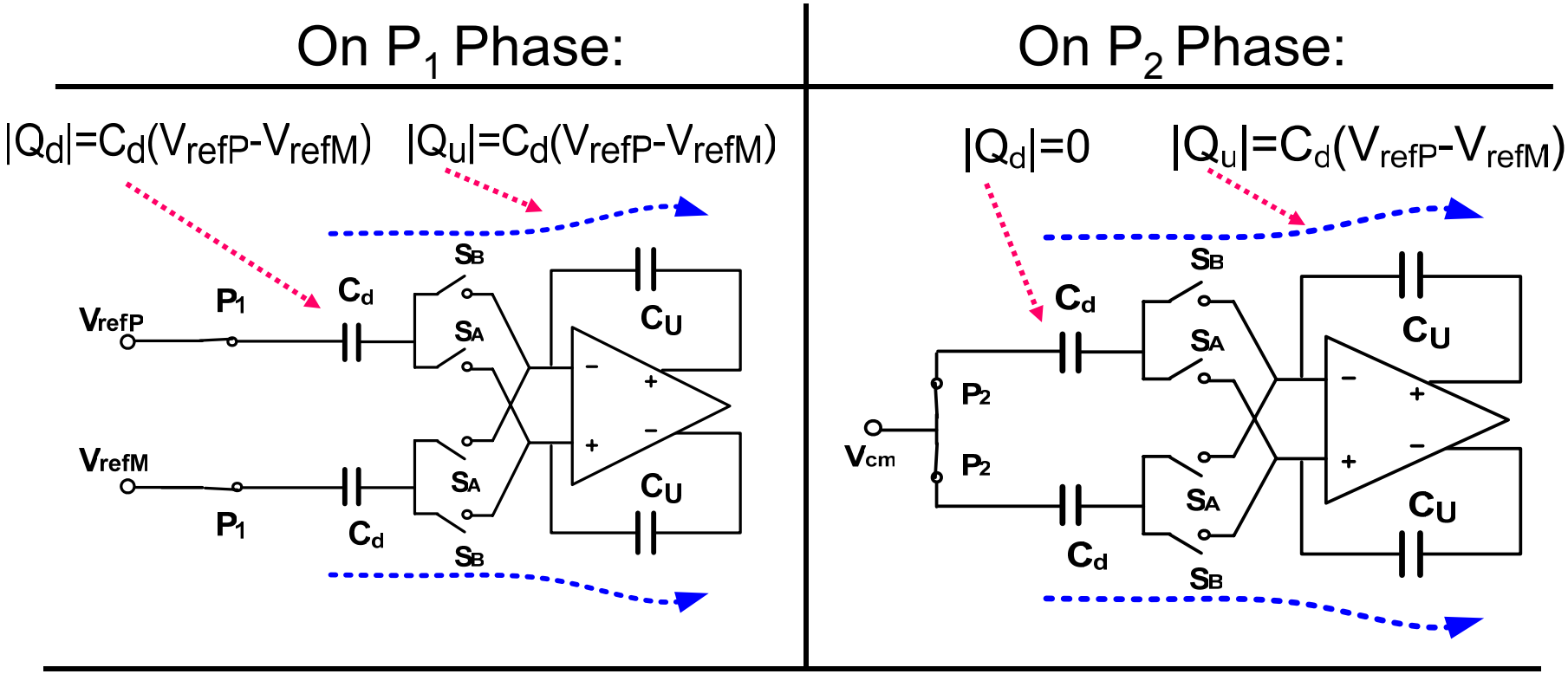
Proposed SC DAC element for double sampling



	b_i=1		b_i=0	
P_1				
P_2				
S_A	ON	OFF	OFF	ON
S_B	OFF	ON	ON	OFF

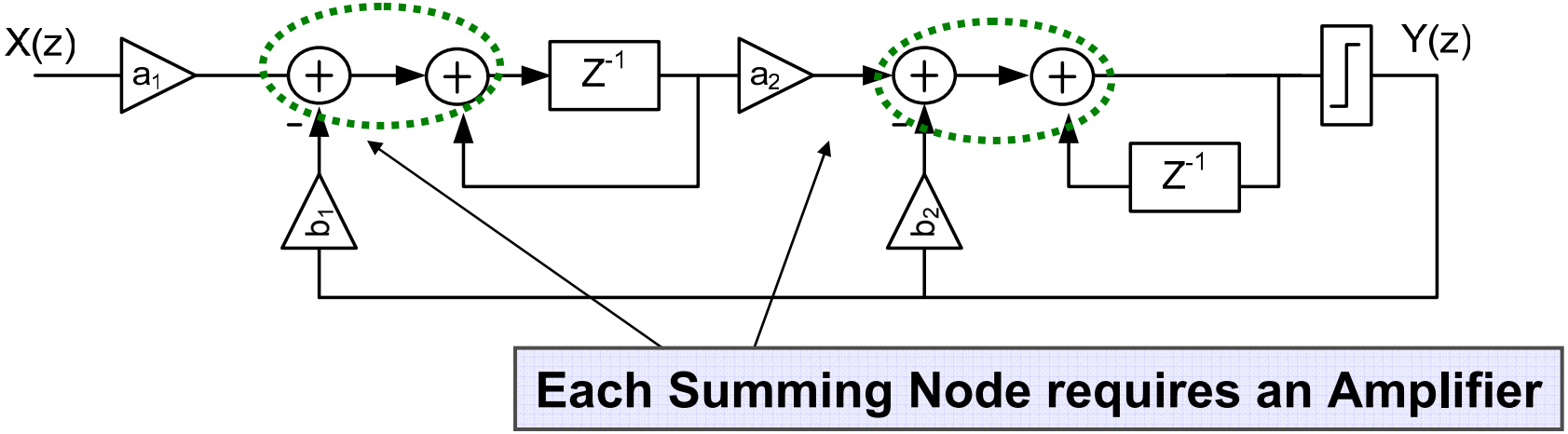
- **Advantages of this approach vs. conventional approach:**
  - **Only one pair of capacitors needed**
  - **No "alternating-gain" effect**
  - **No additional circuitry needed for matching purposes**

Operation of Proposed SC DAC element



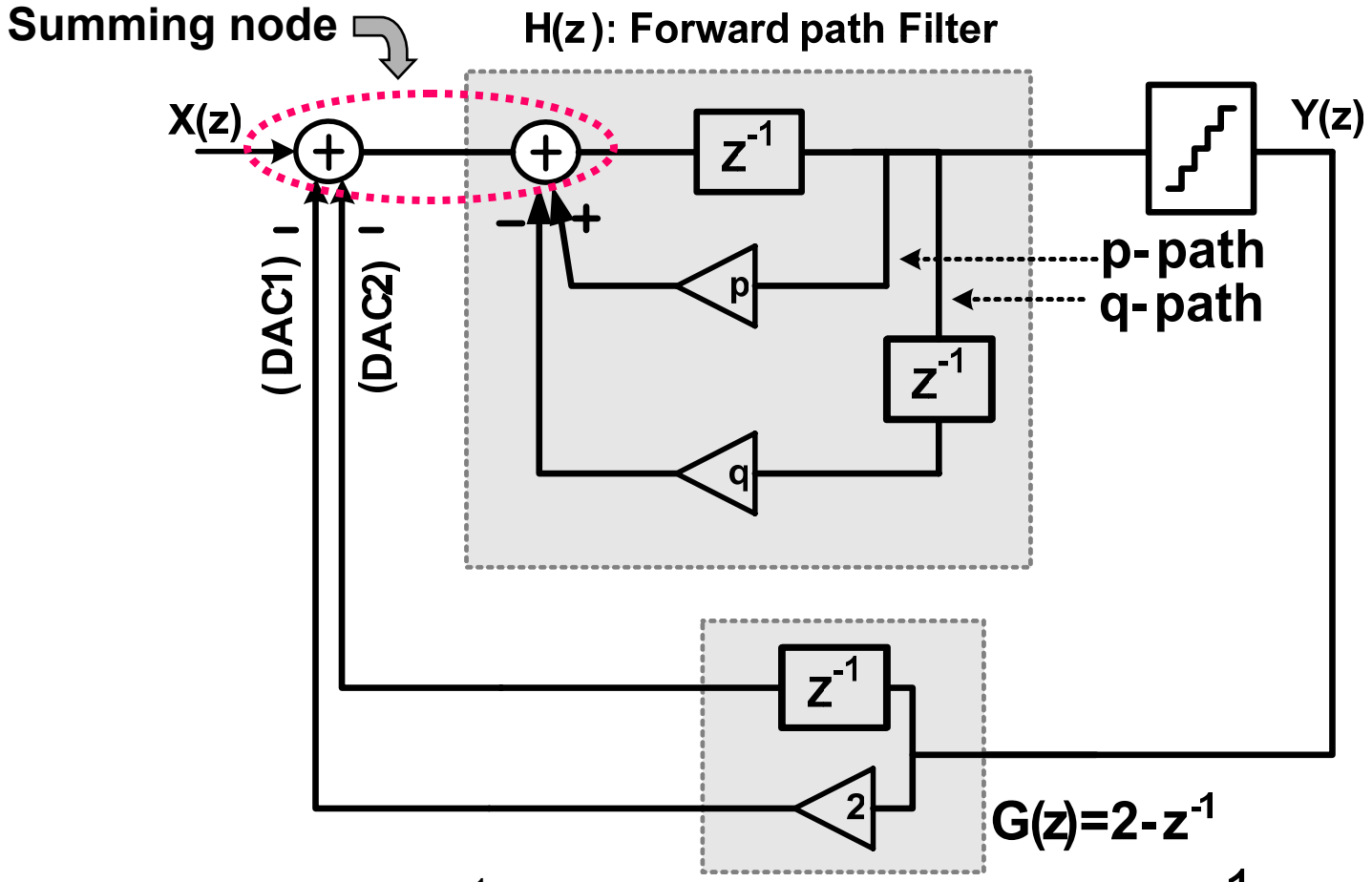
- **On phase P_1 the charge transferred to Integrating Capacitor is:**
  - **$Q_u = C_d(V_{refp}-V_{refm})$**
  - **Q_u is equal to the charge stored into C_d**
  - **This charge will be used during next integration phase**

Conventional 2nd Order Sigma-Delta ADC



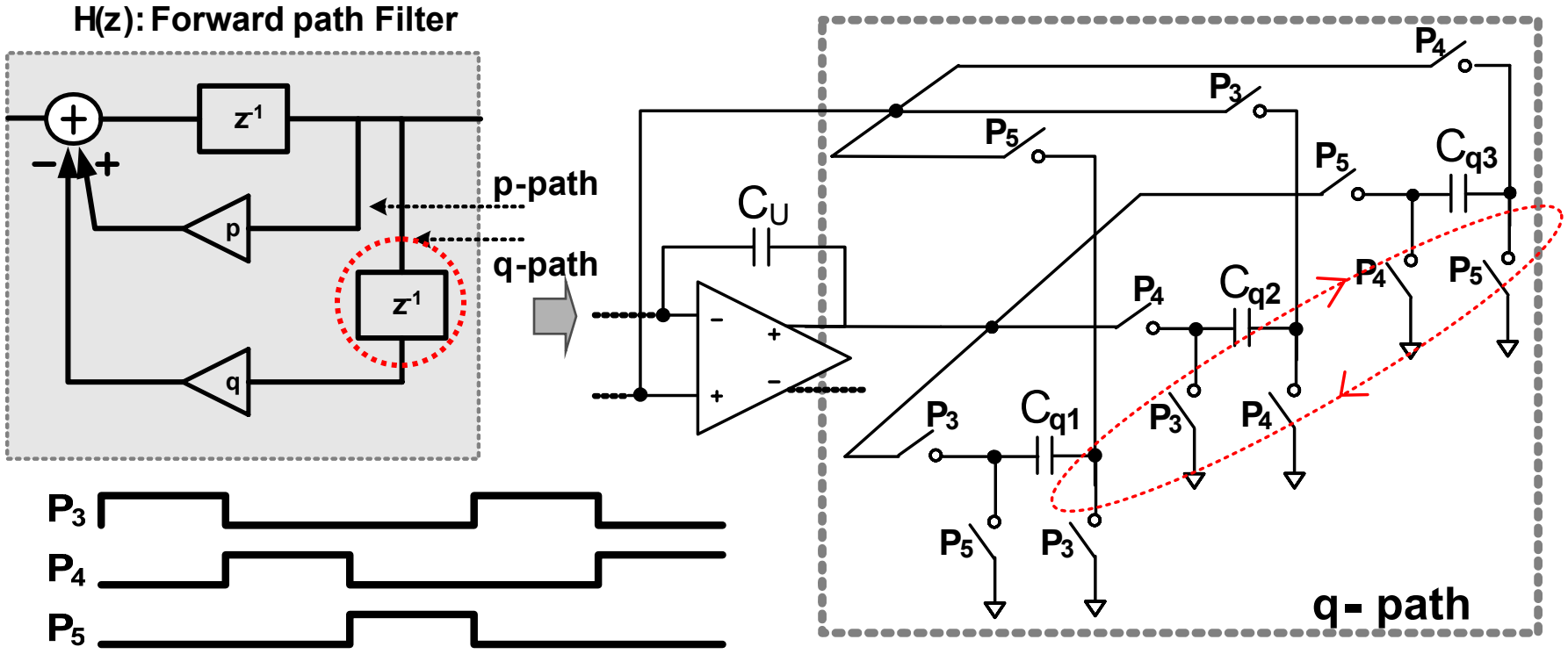
- **Conventional Sigma-delta ADC:**
  - **Needs an amplifier per summing node**
  - **Poles and zeros are chosen by a_i and b_i ,where i=1,2**

Single Amplifier 2nd Order Sigma-Delta ADC



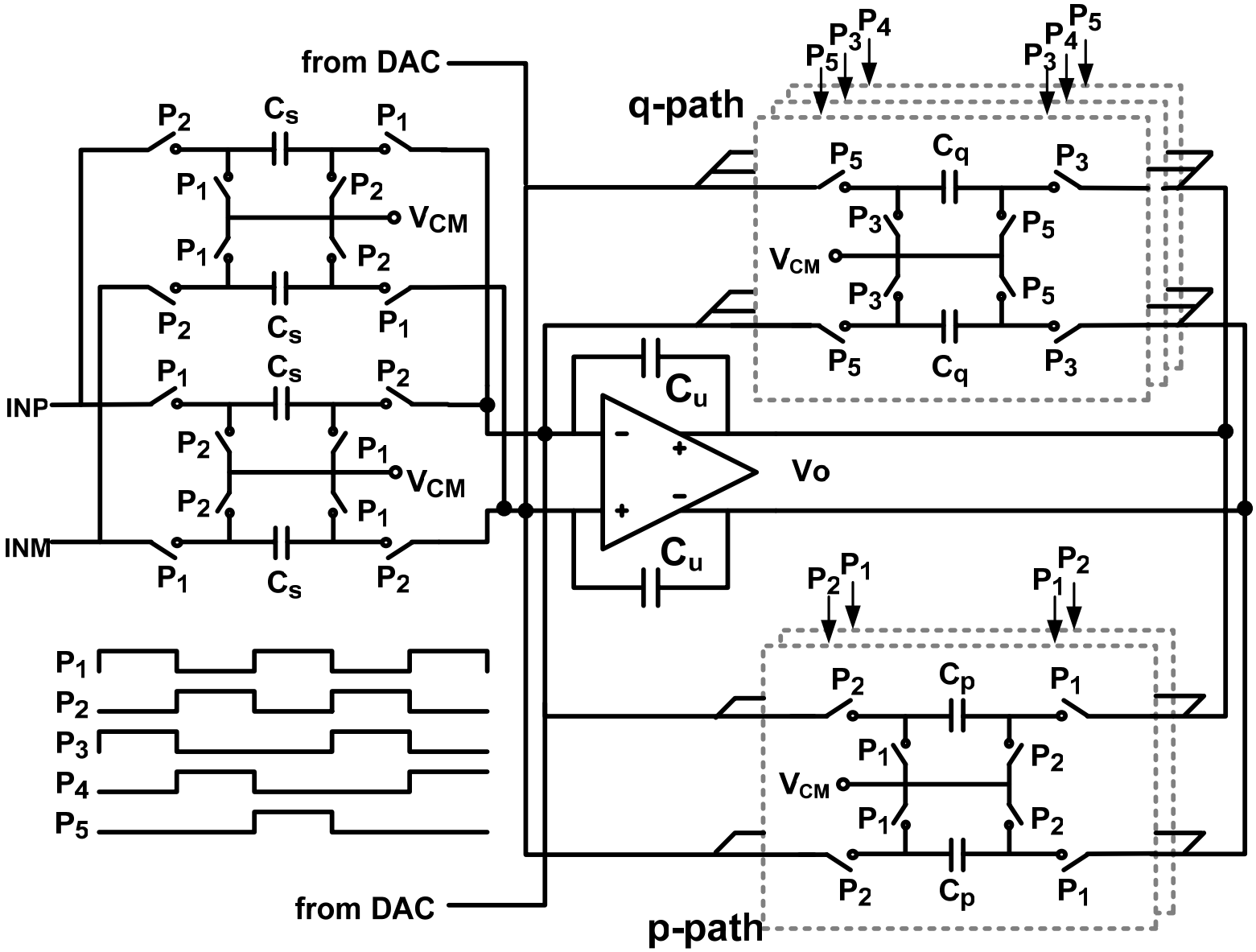
$$STF = \frac{z^{-1}}{1 - p \cdot z^{-1} - q \cdot z^{-2} + z^{-1}G(z)} \quad NTF = \frac{1 - p \cdot z^{-1} - q \cdot z^{-2}}{1 - p \cdot z^{-1} - q \cdot z^{-2} + z^{-1}G(z)}$$

Q-path Operation

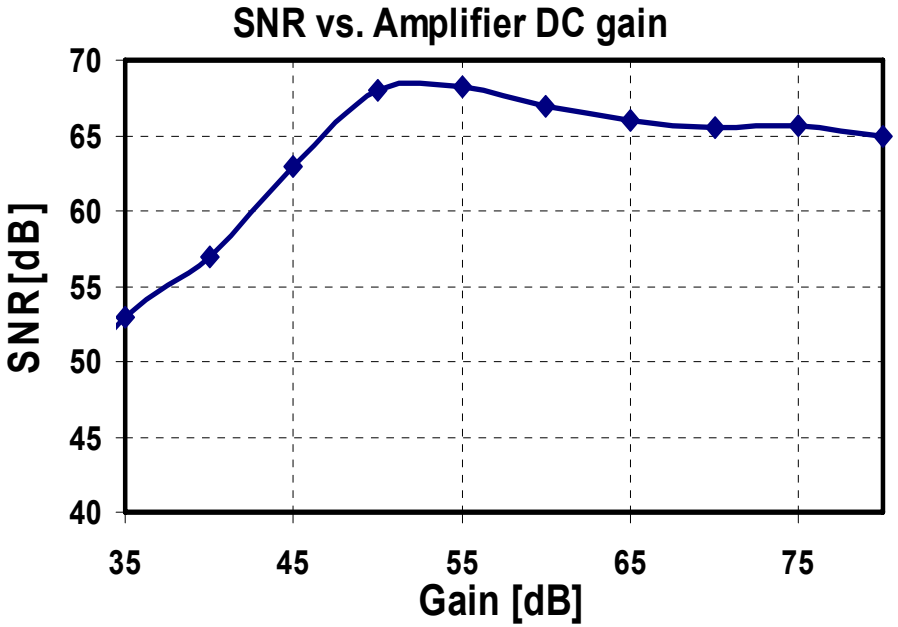


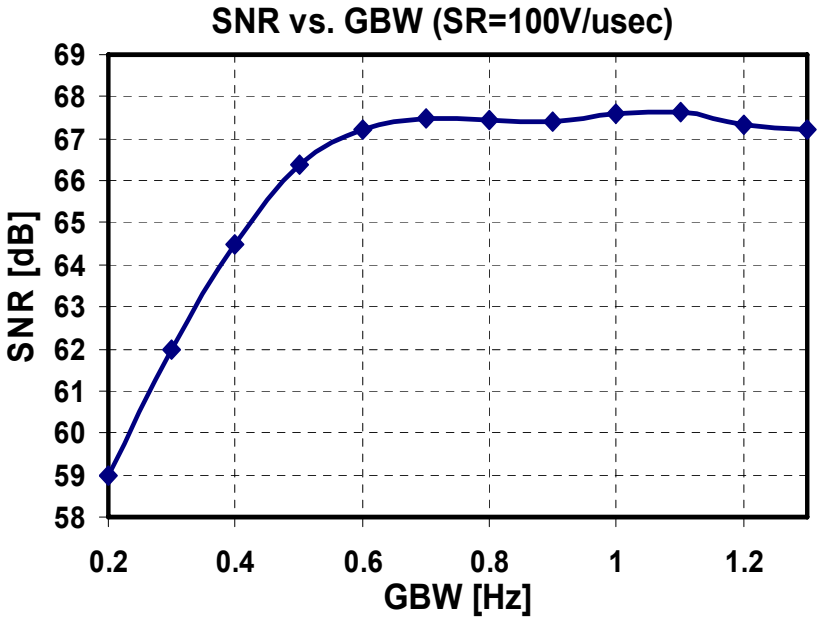
- Rotating to do sampling, holding and integrating functions
  - **The first SC circuit samples the output $v_o(n)$**
  - **while the second one holds the previous output $v_o(n-1)$**
  - **and the third one transfers $v_o(n-2)$ to the integrating capacitor, C_U**

Full Filter implementation



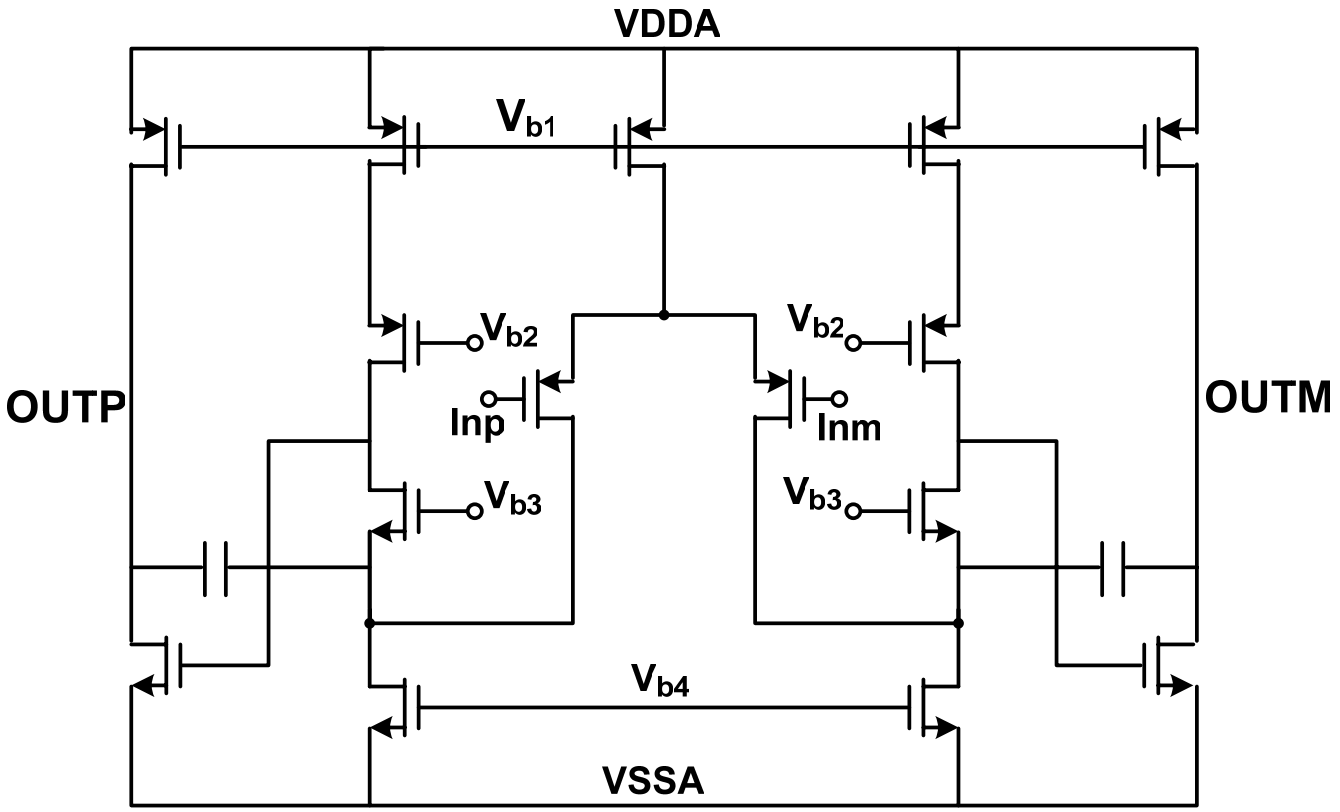
Amplifier design (SR, GBW)





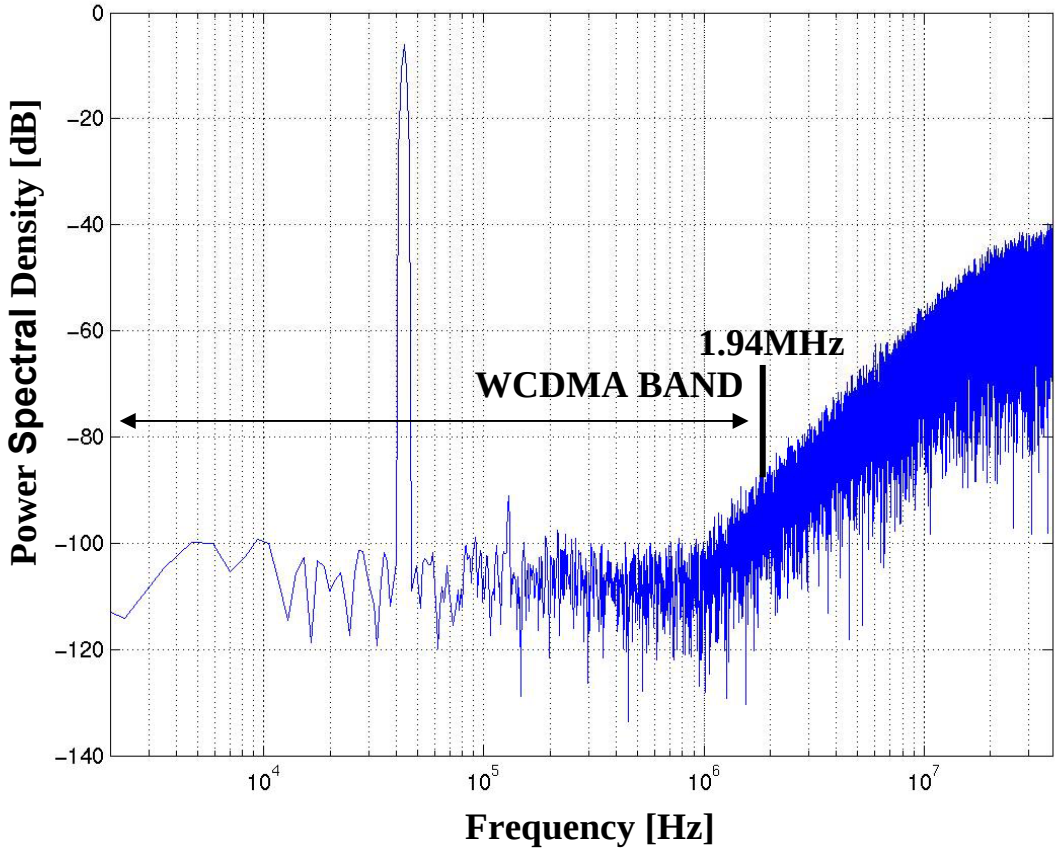
- GBW and SR were simulated in Matlab behavioral model
- Amplifier was designed to have:
  - DC Gain>60dB, SR>100V/µsec and GBW > 50MHz
- Single amplifier topology has a benefit since settling requirement is lower than conventional one

Amplifier implementation



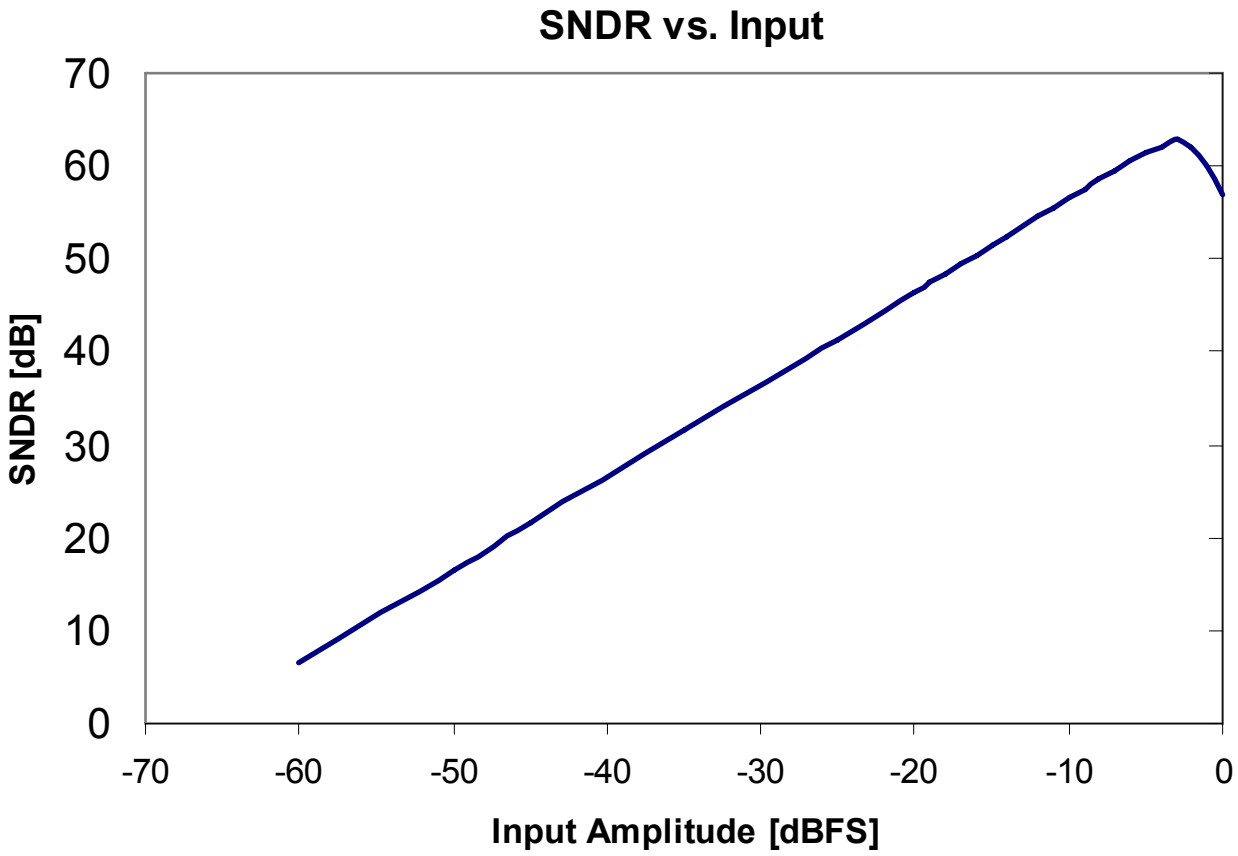
Load Capacitance	1.6 pF
GBW	100 MHz
Input referred Noise*	70 uVrms
Slew Rate	200 V/usec
Current Consumption	700 uA

Measured Power Spectral Density



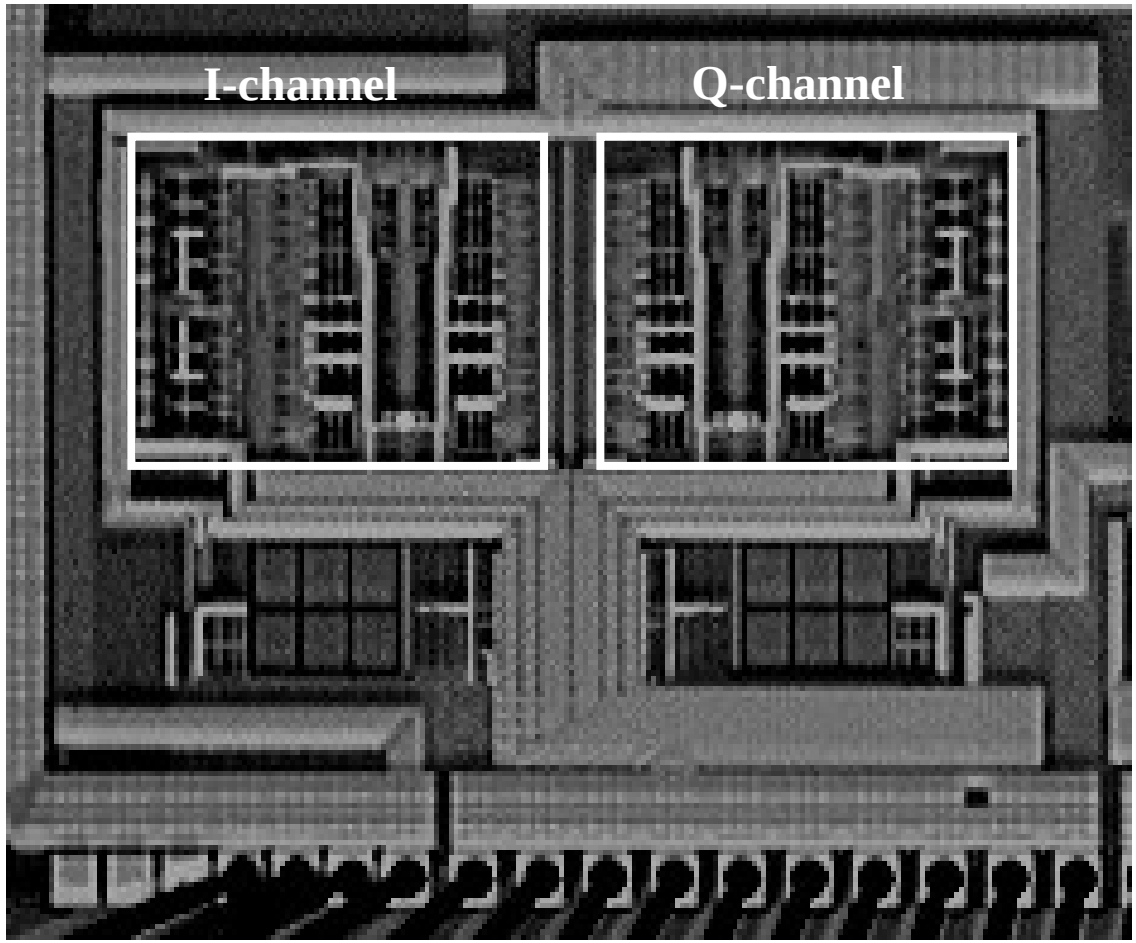
- Input signal: -6 dBFS sine at 448 kHz
- 3rd harmonic shows up at -91 dBV
- Noise floor shows no noticeable noise folding

SNDR vs. Input power



- **63dB peak SNDR happens at -3dBFS input sinusoidal**

Die Photography for dual channel ADCs



- **Implemented in 90nm 5 metal digital CMOS process**

Performance Summary

Technology	90 nm Digital CMOS
Signal Bandwidth	1.94 MHz
Clock Frequency	38.4 MHz
Sampling Frequency	76.8 MHz
Peak SNDR	63 dB
Dynamic Range	66 dB
Input Range	1.5 V_{pp} (differential)
Voltage Supply	1.2 V
Power Consumption	1.2 mW per ADC
Core Area	0.2 mm^2 per ADC

Conclusions

- Second order 5 level Single Amplifier Sigma-Delta ADC with double sampling technique was realized in 90 nm CMOS.
- By using double sampling technique, OSR is doubled with no increase of power consumption and silicon area.
- Single-capacitor double-sampling DAC solved “alternating-gain” error effect.
- 2^{nd} order modulator is implemented using a Single-amplifier architecture. Higher order modulator is feasible.
- Low power consumption: 1.2mW for WCDMA, measured with a 1.2V power supply.
- 66dB dynamic range was achieved in 1.94MHz bandwidth.