Frequency-Domain-Sampling Receivers for Broadband Communication Systems

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Acknowledgements: Pradeep Kotte, Mandar Kulkarni, Xi Chen, Prof. José Silva

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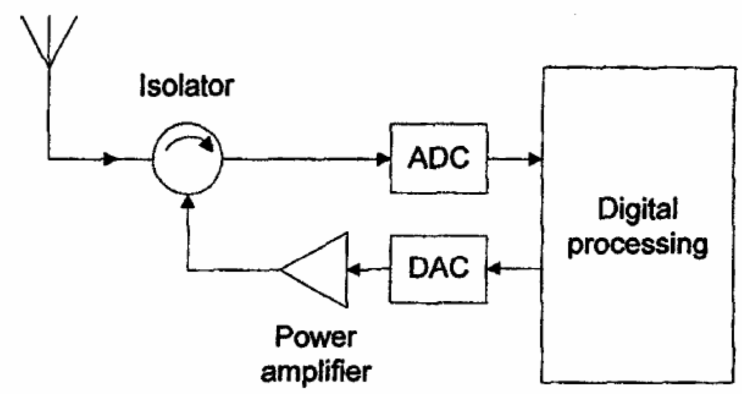
Outline

- Narrow-band, wideband and ultra-wideband in software-defined radio (SDR) architectures.
- Parallelization of ADCs and RF front-ends for broadband receivers. The frequency-sampling solution.
- Broadband multicarrier communication receiver based on analog to digital conversion in the frequency domain.
- Fully calibrated frequency-domain receiver.
- Design examples :
  - Multi-standard GSM, Bluetooth, IEEE802.11g, Wimax and UWB.
  - 2 Gs/s, 11 bits broadband multicarrier receiver via sampling in the frequency-domain.
- Conclusions.

A Lot of New Names for Future Broadband Communication Systems

The Names

- Software Defined Radios
- Multi-Standard Radios
- Cognitive Radios
- Universal Radios



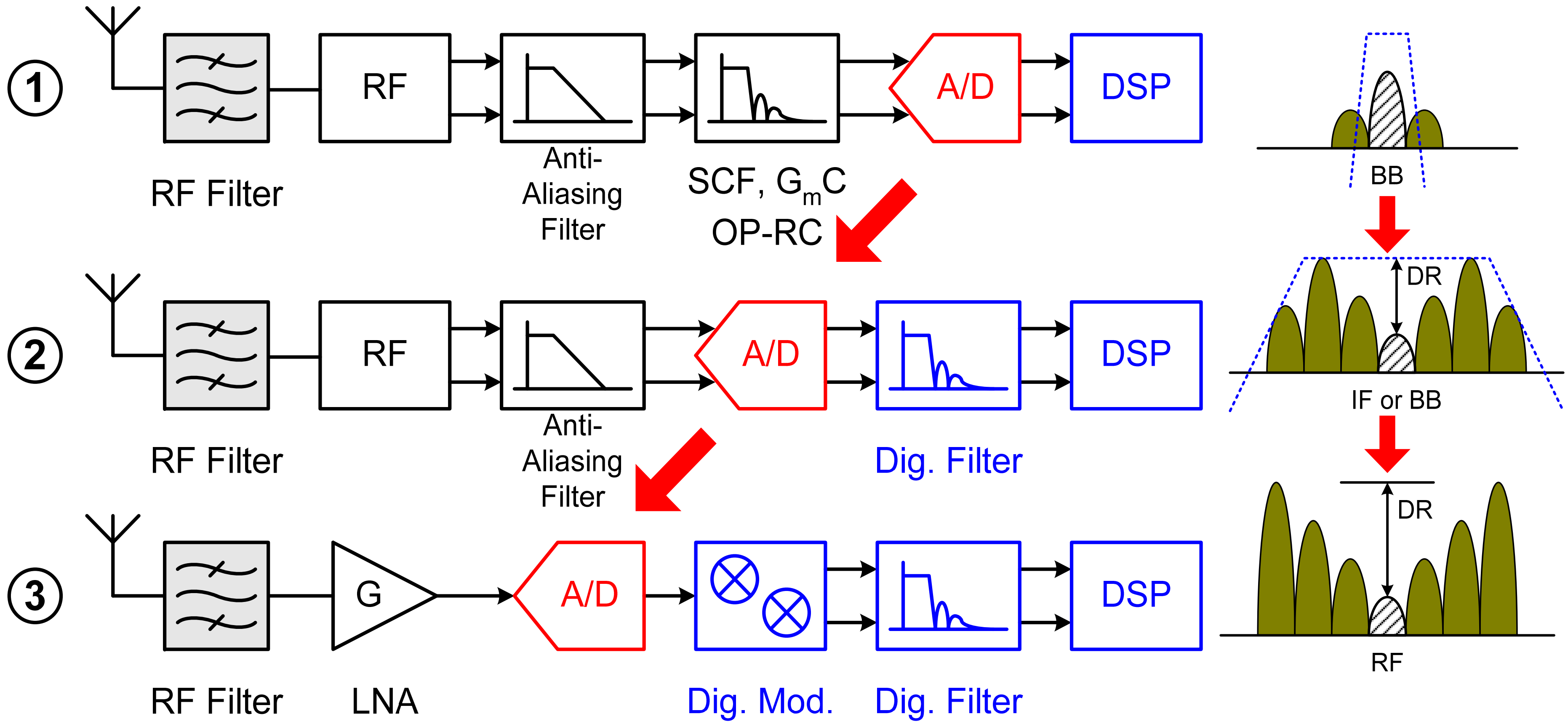
Common Features

- Very wideband systems, multiband channels, opportunistic frequency allocation, bandwidth reuse, intensely digital, scalable/reconfigurable RF/analog.

Challenges

- Conflicting requirements, large bandwidth/dynamic range but still want low power/small area.

The Receiver Design Problem in Broadband Communications



- How much RF processing do I do before the ADC?
- How do I take advantage of technology scaling in this RF pre-procesing?
- How do I make the front-end scalable and configurable to fit multiple standards?

Some of the New Approaches to Broadband Receivers

- A high-frequency software defined radio

N. C. Davies, “A high performance HF software radio,” in *Proc. 8th Int. Conf. HF Radio Systems and Techniques*, Guildford, U.K., 2000, pp. 249–256.

- Frequency channelizers

D. R. Zahirniak, D. L. Sharpin, and T. W. Fields, “A hardware-efficient, multirate, digital channelized receiver architecture,” *IEEE Trans. Aerosp. Electron. Syst.*, vol. 34, no. 1, pp. 137–152, Jan. 1998.

- Selectable RF filters and downconversion

H. Yoshida, T. Kato, T. Tomizawa, S. Otaka, and H. Tsurumi, “Multimode software defined radio receiver using direct conversion and low-IF principle: Implementation and evaluation,” *Electr. Commun. In Japan (Part I: Communications)*, vol. 86, pp. 55–65, 2003.

- Subsampling and undersampling

- Analog decimation

D. Jakonis, K. Folkesson, J. Dabrowski, P. Eriksson, and C. Svensson, “A 2.4-GHz RF sampling receiver front-end in 0.18-mCMOS,” *IEEE J. Solid-State Circuits*, vol. 40, no. 6, pp. 1265–1277, Jun. 2005.

Some of the New Approaches to Broadband Receivers (cont…)

- Sampling with built-in anti-aliasing

Y. S. Poberezhskiy and G. Y. Poberezhskiy, "Sampling and signal reconstruction circuits performing internal antialiasing filtering and their influence on the design of digital receivers and transmitters," *IEEE Trans. Circuits Syst. I*, vol. 51, no. 1, pp. 118–129, Jan. 2004.

- Sample rate, downsampling and filtering

R. Crochiere and L. Rabiner*, Multirate Digital Signal Processing*. Englewood Cliffs, NJ: Prentice Hall, 1983.

- A discrete-time RF sampling receiver

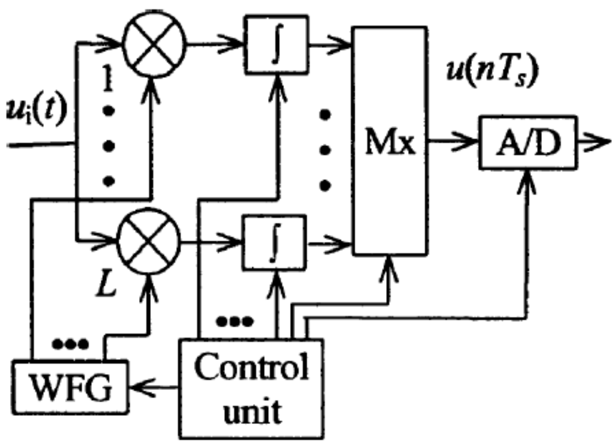
R. B. Staszewski, et. al. "All-digital TX frequency synthesizer and discrete-time receiver for Bluetooth radio in 130-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2278–2291, Dec. 2004.

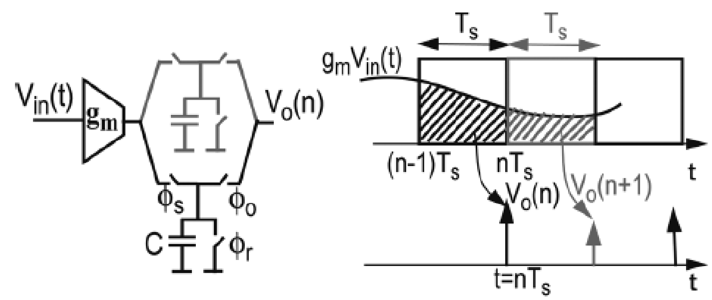
- UCLA SDR receiver

Abidi, "The path to software-defined radio receiver", IEEE JSSC, May 2007

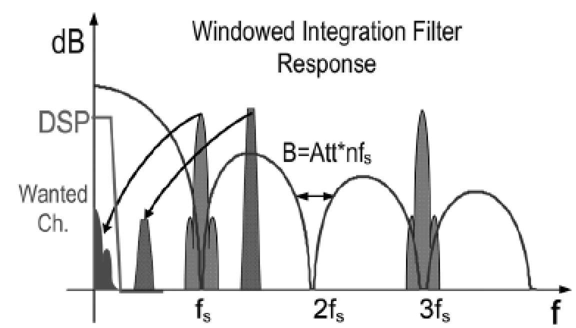
- Frequency-domain-sampling receivers
  - S. Hoyos, B. M. Sadler, and G. R. Arce, "**Broadband Multicarrier Communications Receiver Based on Analog to Digital Conversion in the Frequency Domain,**" *IEEE Transactions on Wireless Communications*, March 2006.
  - S. Hoyos and B. M. Sadler, "**Ultra-wideband analog to digital conversion via signal expansion,**" *IEEE Transactions on Vehicular Technology*, Vol. 54, No. 5, Sept. 2006, Pages: 1609-1622. Invited
  - S. Hoyos, B. M. Sadler **"UWB Mixed-Signal Transform-Domain Direct-Sequence Receiver,"** *Accepted for publication in IEEE Transactions on Wireless Communications*, 2007.

Sampling with built-in anti-aliasing





(a)

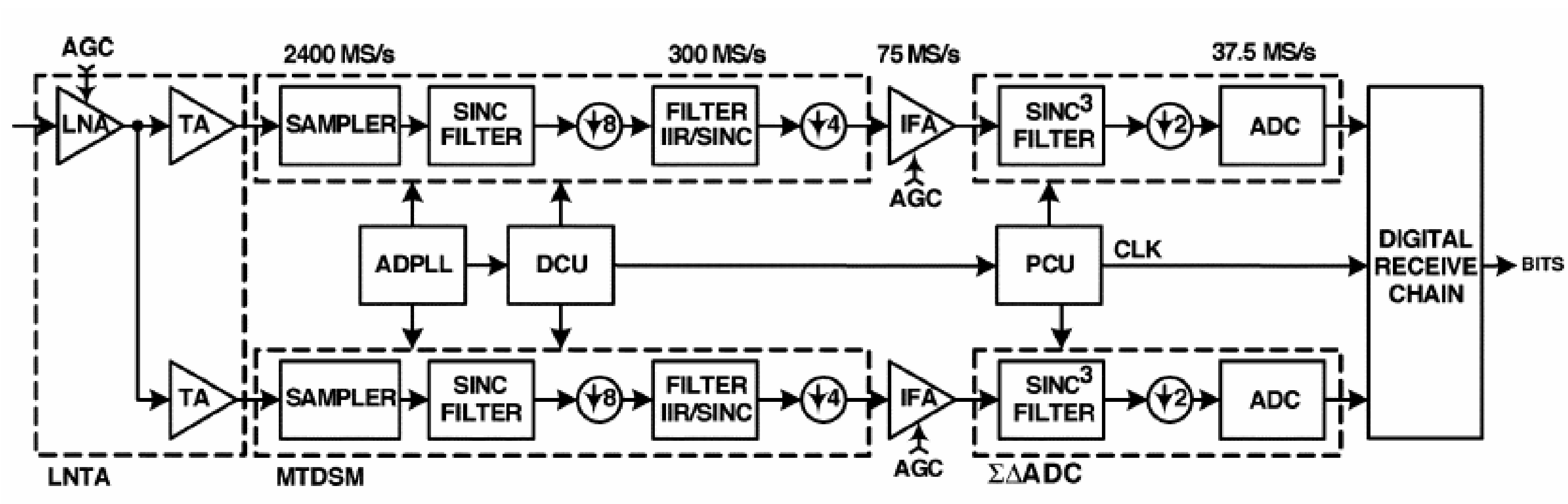


(b)

- Sinc(x) anti-aliasing provided by windowing and integration. The sidelobes decay at 20 dB/decade with zeros at fs, 2fs, ..
- More general mixing waveforms can be used, although complexity goes up.

Y. S. Poberezhskiy and G. Y. Poberezhskiy, “Sampling and signal reconstruction circuits performing internal antialiasing filtering and their influence on the design of digital receivers and transmitters,” *IEEE Trans. Circuits Syst. I*, vol. 51, no. 1, pp. 118–129, Jan. 2004.

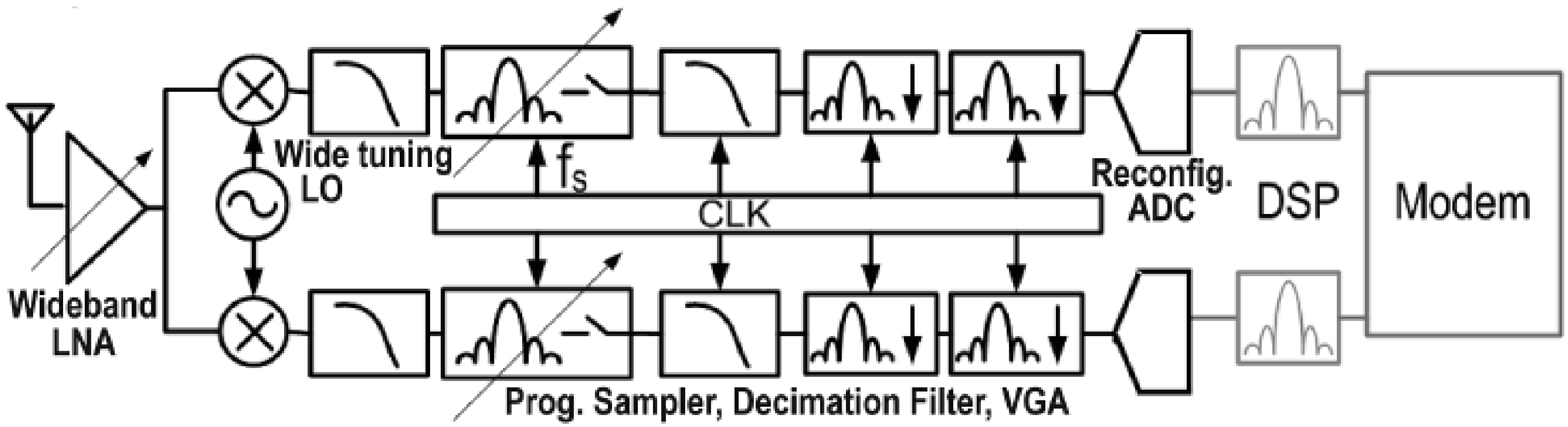
A discrete-time RF sampling receiver



- Bluetooth and GSM receivers from TI use integrate and dump sampling followed by down sampling and filtering.
- A lot of programable filtering and decimation to achieve the anti-aliasing needed.

R. B. Staszewski, et. al. “All-digital TX frequency synthesizer and discrete-time receiver for Bluetooth radio in 130-nm CMOS, ” *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2278–2291, Dec. 2004.

UCLA SDR receiver



- Direct conversion with tunable LO in the freq. range 800 MHz to 6 GHz.
- Cascade of sinc^N filters followed by decimation to achive the antialisign needed.
- Good for narrowband signals as a single ADC can handle the bandwidth. But SDR should also be good for wideband and ultra-wideband signals. Need parallel ADC to sample at a fraction of Nyquist rate. Parallelization of the front-end will be needed if want to keep the ADC sampling rate down.

A. Abidi, “The path to software-defined radio receiver”, IEEE JSSC, May 2007

SDR for narrowband, wideband and ultra-wideband signals

- Assume we have a tunable front-end that provides the downconversion and the antialiasing filtering needed for a wide range of standards.
- The problem now is that the signal bandwidth will have > 10X range. Example : 802.11g (ΣΔ ADC @ 50 Ms/s and 8 bits), UWB (ADC @ 500 Ms/s and 5 bits). Say you can run the ΣΔ ADC @ 100Ms/s and 5 bits, i.e. exchange OSR by DR). Can we use 5 of these ΣΔ ADCs to cope with UWB ?
- Note that the same ΣΔ ADC could operate @ 200 KHz and 14 bits for GSM and @ 1MHz and 12 bits for Bluetooth.
- How do you parallelize the ADCs and even the RF front-end to create a SDR for narrowband, wideband and ultra-wideband signals?

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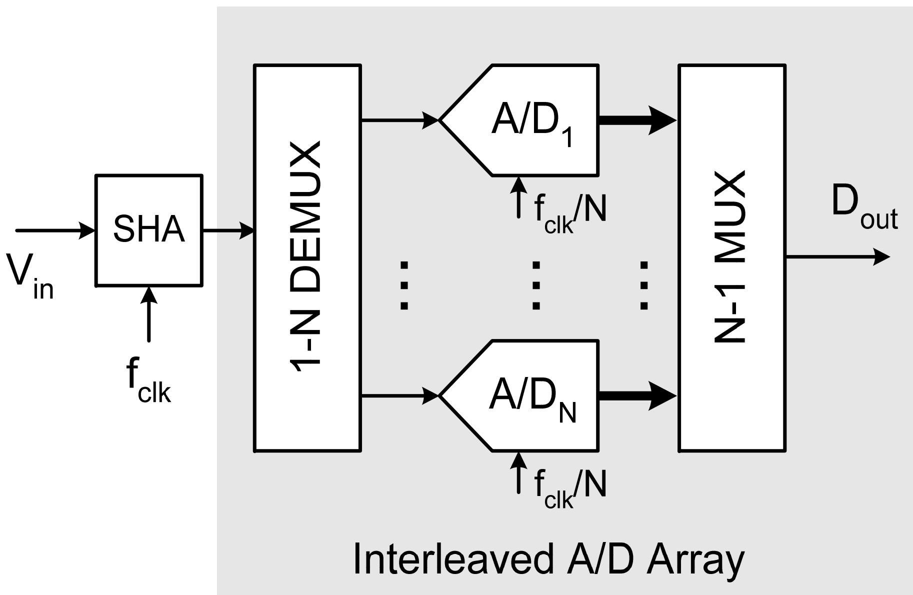
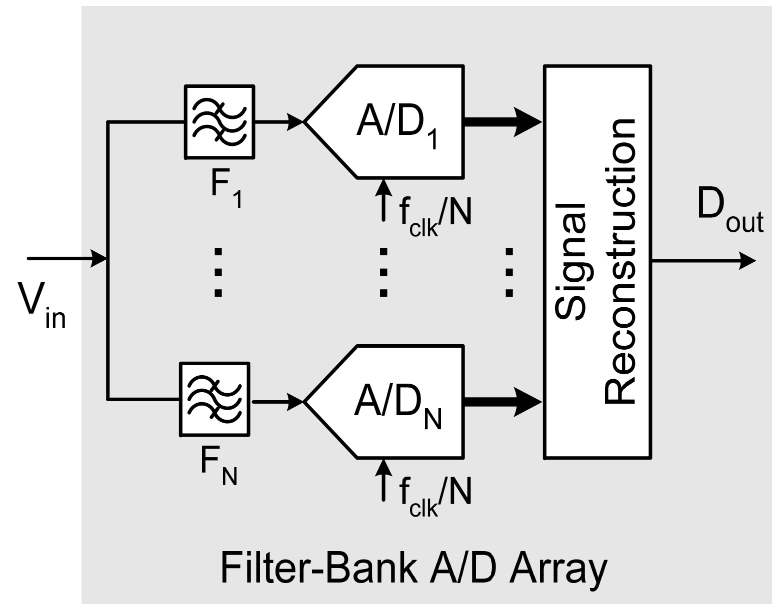
Parallelized ADCs for Broadband Signals

Time-interleaved ADC



Filter-bank ADC



Problems

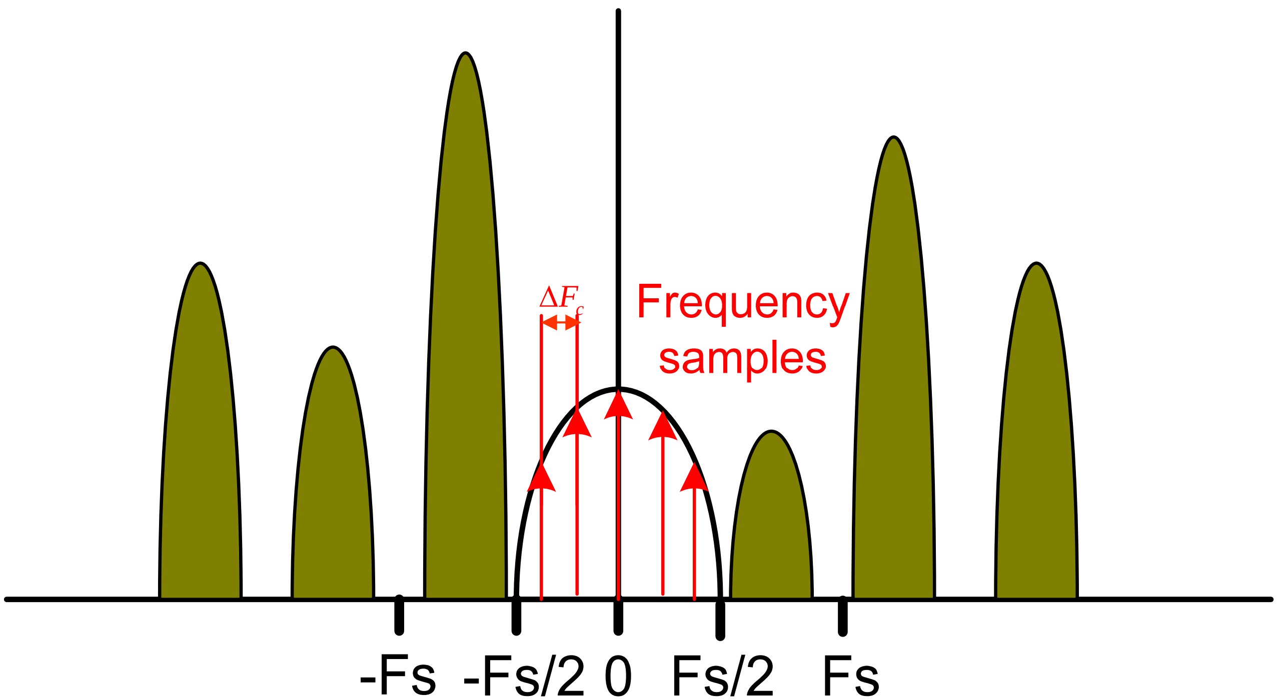
- ❑ Jitter.
- ❑ All ADCs see the full input signal bandwidth (nonlinearities, aliasing).

Problems

- ❑ Filters with tough specs (aliasing).
- ❑ Signal reconstruction increases complexity.

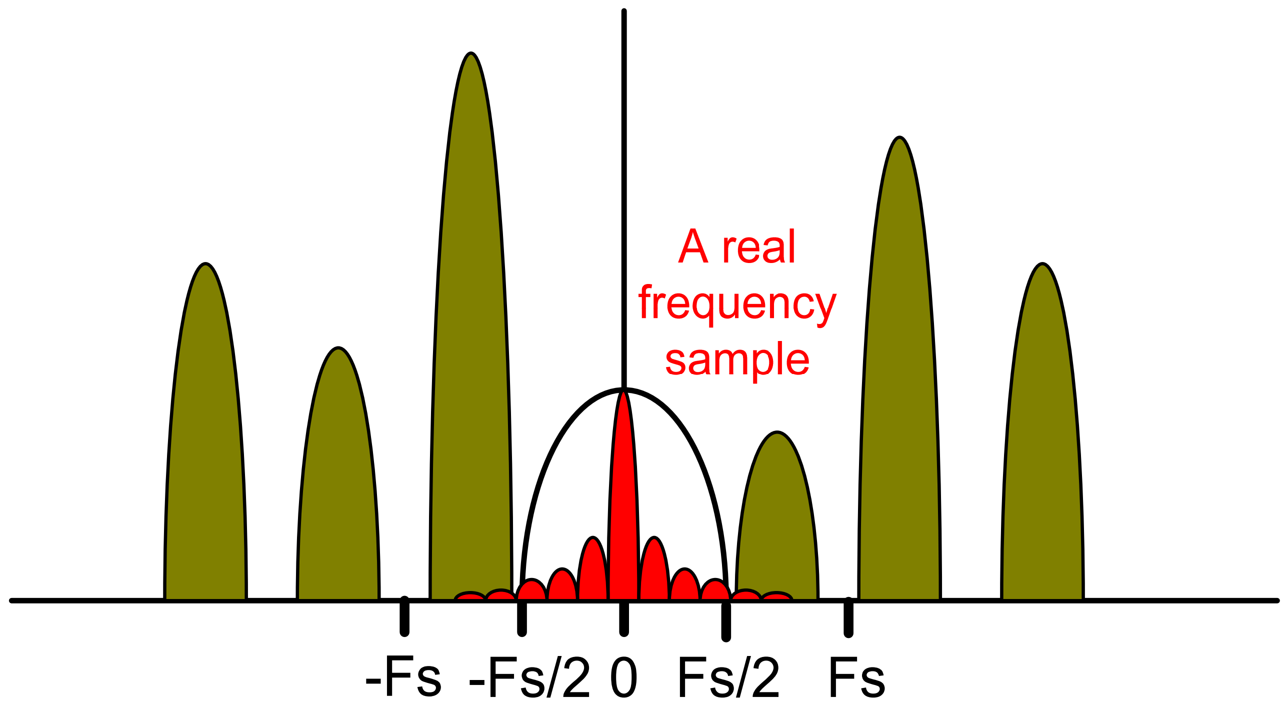
☞ Goals are to relax sample and hold requirements, relax filter specifications without introducing aliasing and minimize signal reconstruction.

Frequency-Domain Sampling



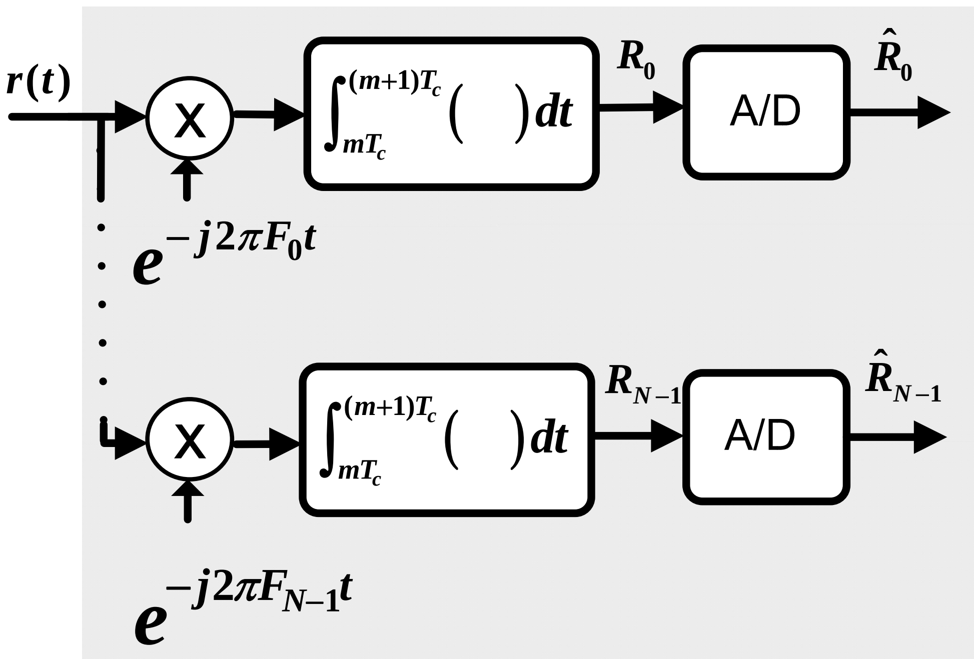
- Ideal frequency-domain sampling is aliasing free.
- Orthogonality between frequency samples and adjacent interferers is the key.
- However, in practice few frequency samples can be taken to keep the complexity low.

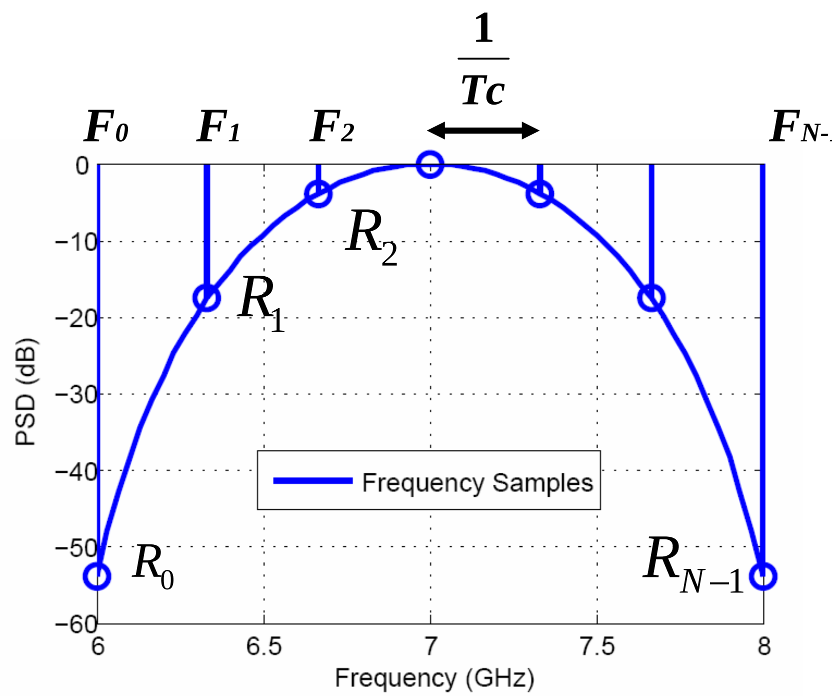
Frequency-Domain Sampling



- ❑ A real frequency sample spills over the adjacent interference, so the antialiasing filter still helps.
- ❑ What does it take to sample in the frequency domain?

Frequency-Domain ADC

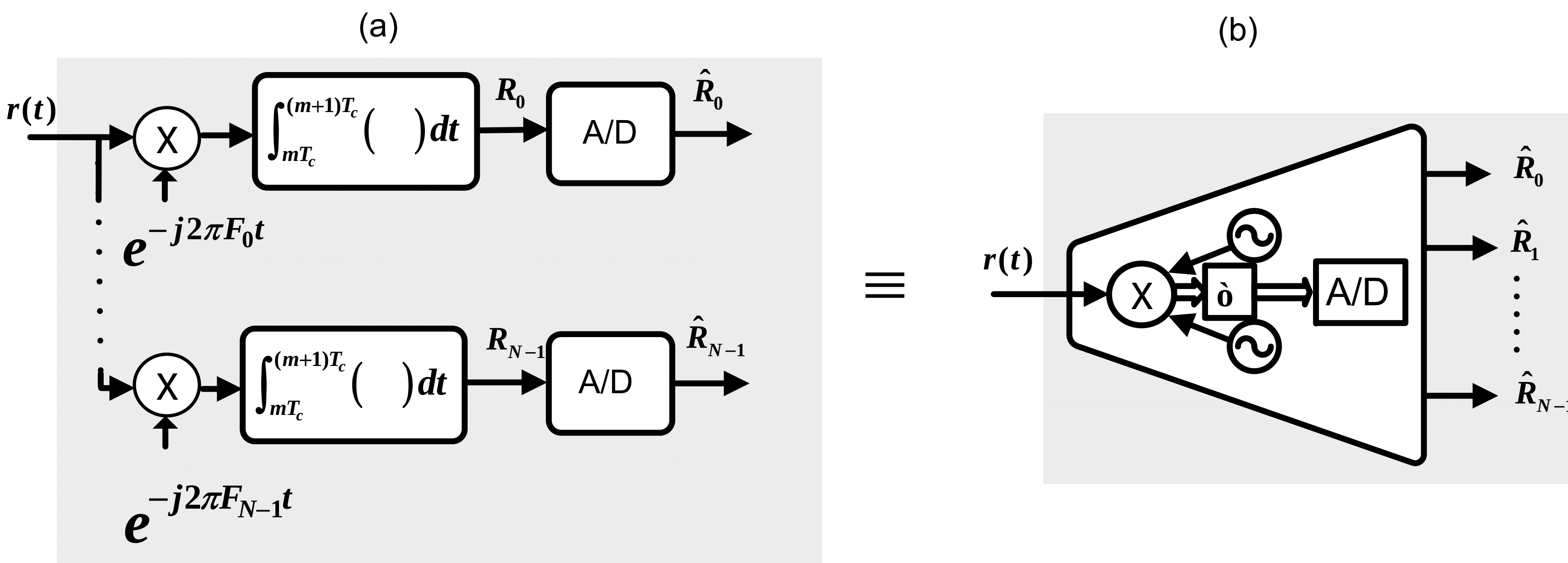




- ❑ Simple mixers and integrators.
- ❑ Lower sample and hold requirements. Integrator will hold the frequency sample.
- ❑ No signal reconstruction. Parallel digital processing.
- ❑ Optimal bit allocation minimizes quantization error. Some samples may not be quantized at all.

S. Hoyos and B. M. Sadler, "**Ultra-wideband analog to digital conversion via signal expansion,**" *IEEE Transactions on Vehicular Technology*, Vol. 54, No. 5, Sept. 2006, Pages: 1609-1622. Invited

Frequency-Domain ADC Representation

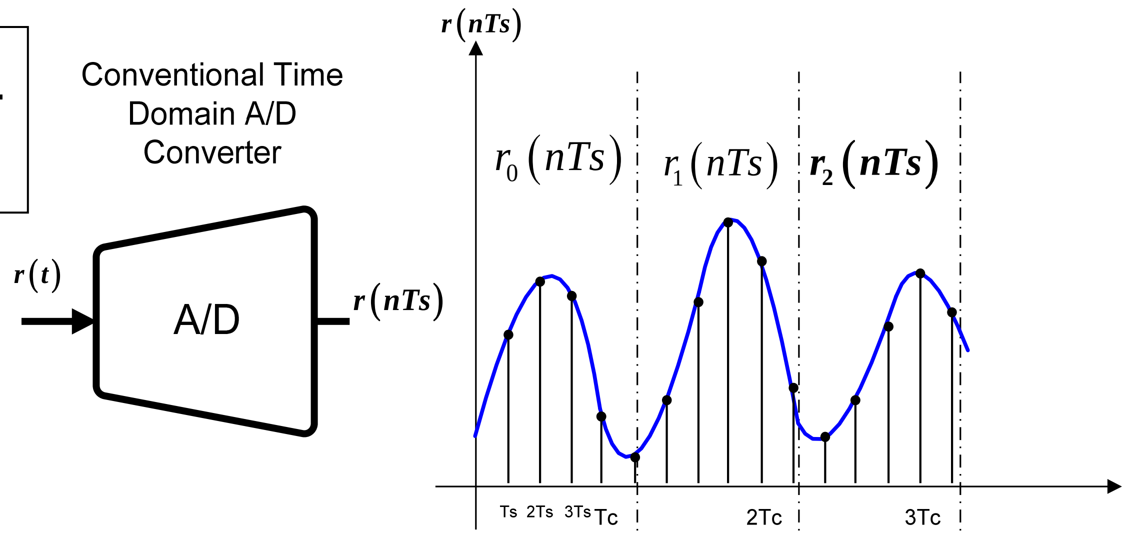


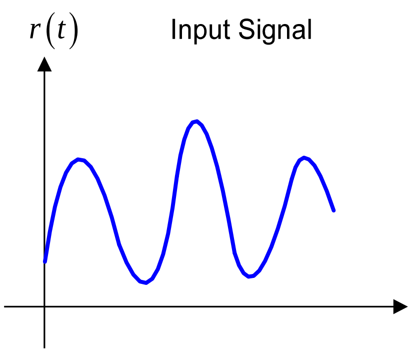
(a) Frequency-Domain ADC implemented with a bank of oscillators, mixers and integrators

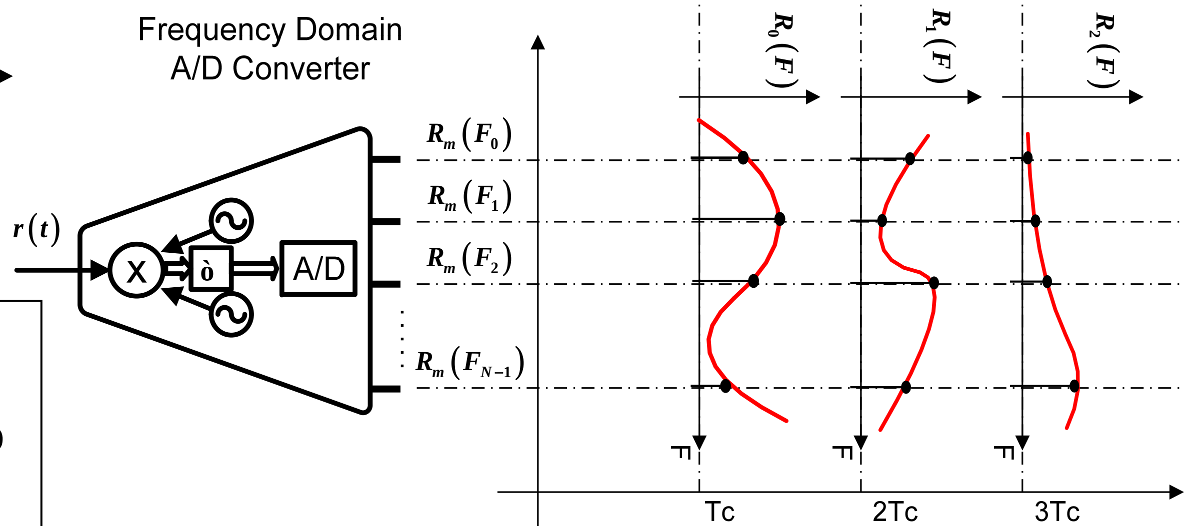
(b) Block diagram representation

Frequency-Domain vs. Time-Domain ADC

- *N* samples every *Tc* seconds.
- Longer *Tc* needs a larger *N*.







- Windows can overlap.
- Robustness to jitter due to continuous time processing.

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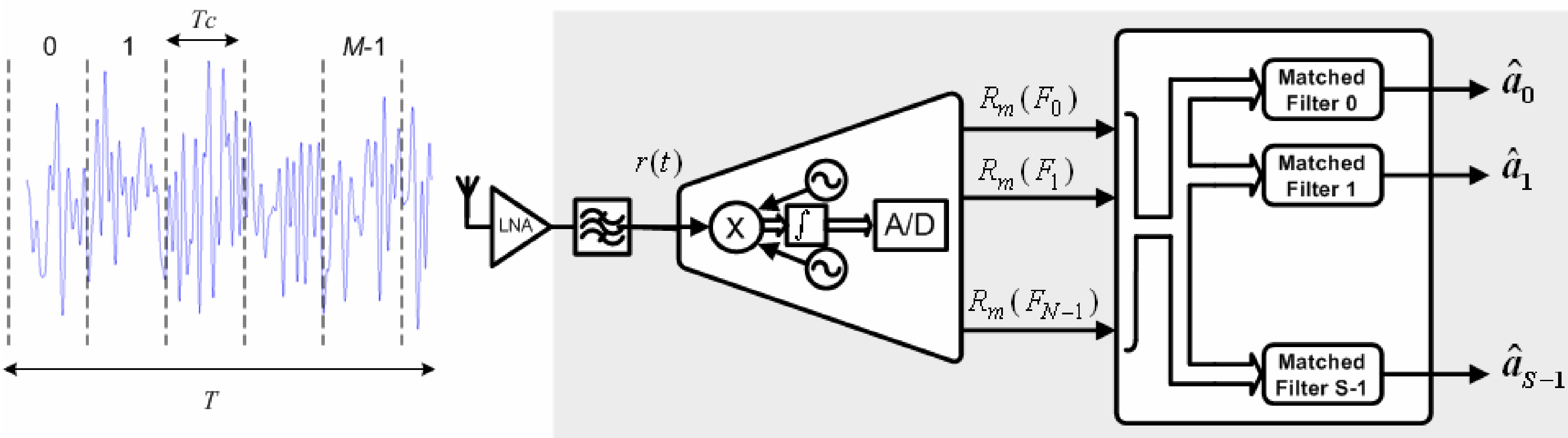
Frequency-Domain Multicarrier Receiver

- The received multicarrier signal with *S* carriers:

$$r(t) = x(t) * h(t) + z(t) \approx \sum_{s=0}^{S-1} a_s e^{j2\pi f_s t} H(f_s) + z(t), \quad 0 \leq t \leq T$$

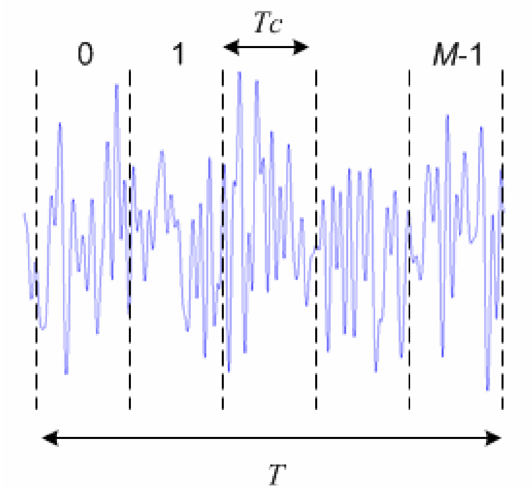


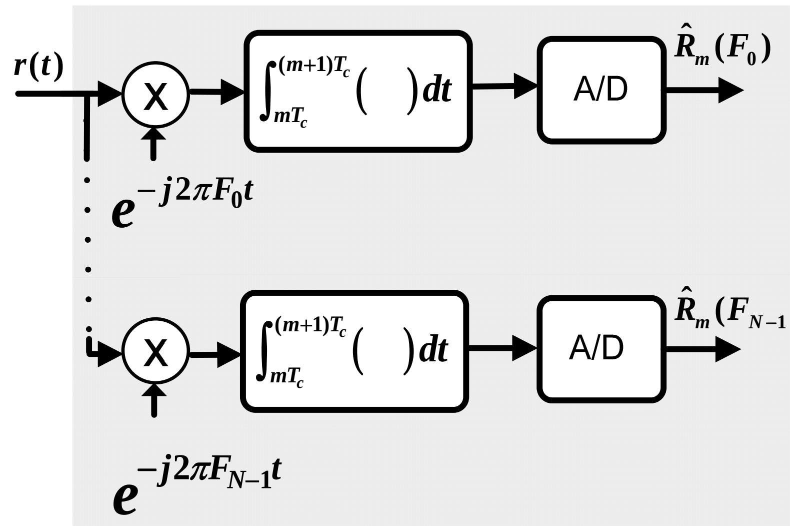
- Number of frequency-samples in *T* is *MN*. *T = MTc.*

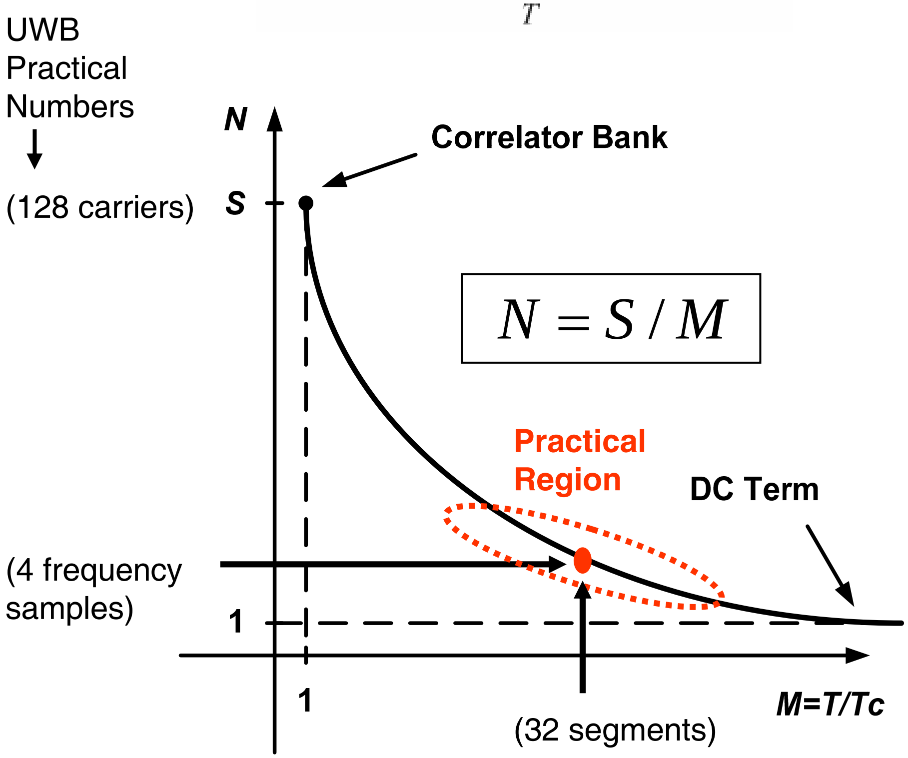
- How do I pick the number of samples *N,* the number of segments *M* for a given number of carriers *S ?*

S. Hoyos, B. M. Sadler, and G. R. Arce, "**Broadband Multicarrier Communications Receiver Based on Analog to Digital Conversion in the Frequency Domain,**" *IEEE Transactions on Wireless Communications*, March 2006.

Number of Samples *N* vs. Number of Segments *M*

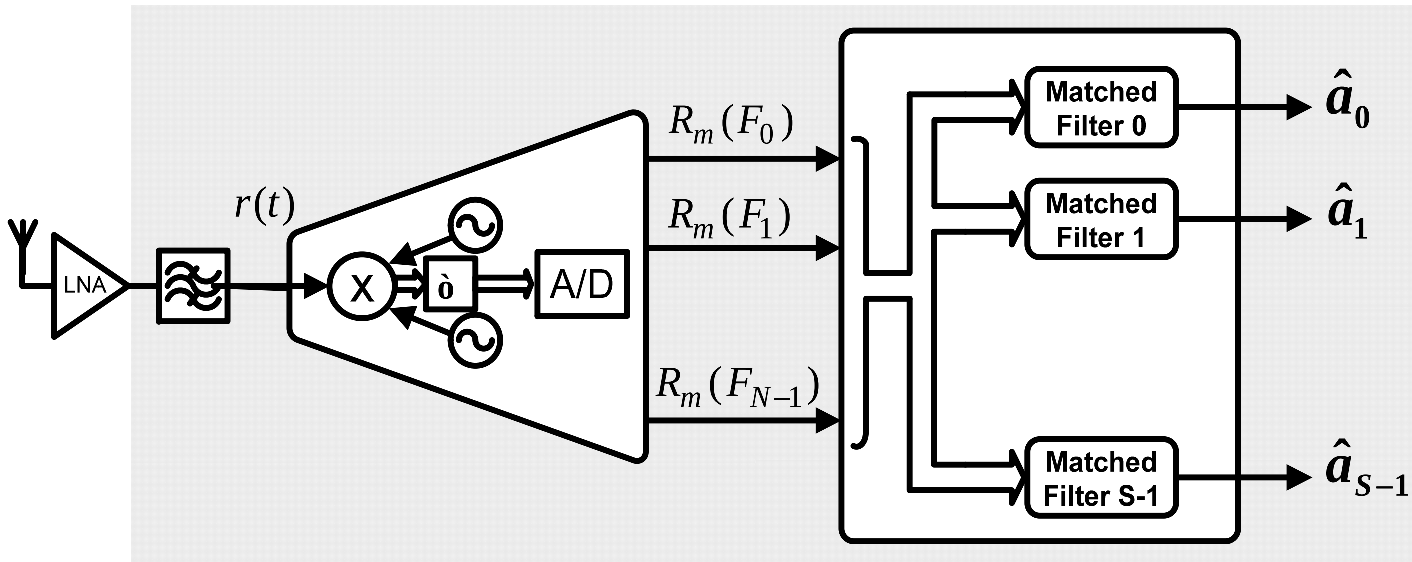






- Three regions of operation:
  1. *M=1, N=S*, correlation bank (no practical use).
  2. *M>S, N=1*. DC terms. Low-pass filter followed by Nyquist rate or oversampled ADC.
  3. *M>1, N<S*, Frequency-Domain ADC.

Matched Filter Digital Baseband



- ❑ Matched filter estimates: Truncation of continuous frequency matched filter equation. [Hoyos *et al* TWC'06]

- ❑ Estimates are linear combinations for samples with AWGN noise.

- ❑ MMSE, LS, ML solutions are possible and offer better performance

$$\hat{a}_s = \sum_{m=0}^{M-1} \int_{-\infty}^{\infty} R_m(F) G^*_{s,m}(F) \, \mathrm{d}F \approx \sum_{m=0}^{M-1} \Delta F_c \sum_{n=0}^{N-1} R_m(F_n) \hat{G}^*_{s,m}(F_n),$$

$$\hat{G}_{s,m}(F_n) = H(f_s) \frac{\sin(\pi T_c(F - f_s))}{\pi(F - f_s)} e^{-j\pi T_c(2m+1)(F - f_s)},$$

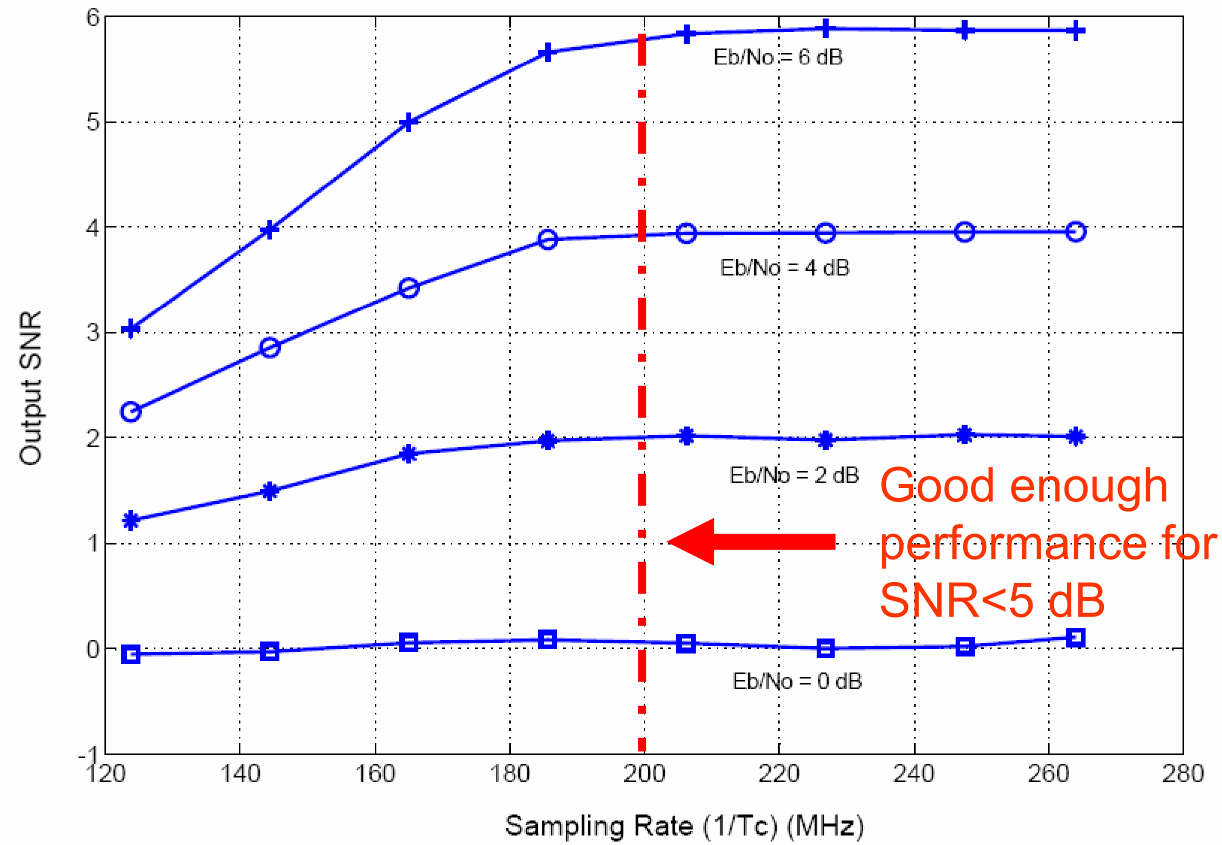
Output SNR in UWB Example

- ❑ UWB Multiband

OFDM standard draft

- ❑ Fc= 3.1~10.6 GHz
- ❑ 128 carriers
- ❑ 3 bands of 528MHz
- ❑ Resolution = 4 bits
- ❑ Eb/No = 4~5 dB
- ❑ Frequency domain

ADC with *N* = 6 (12 ADCs)

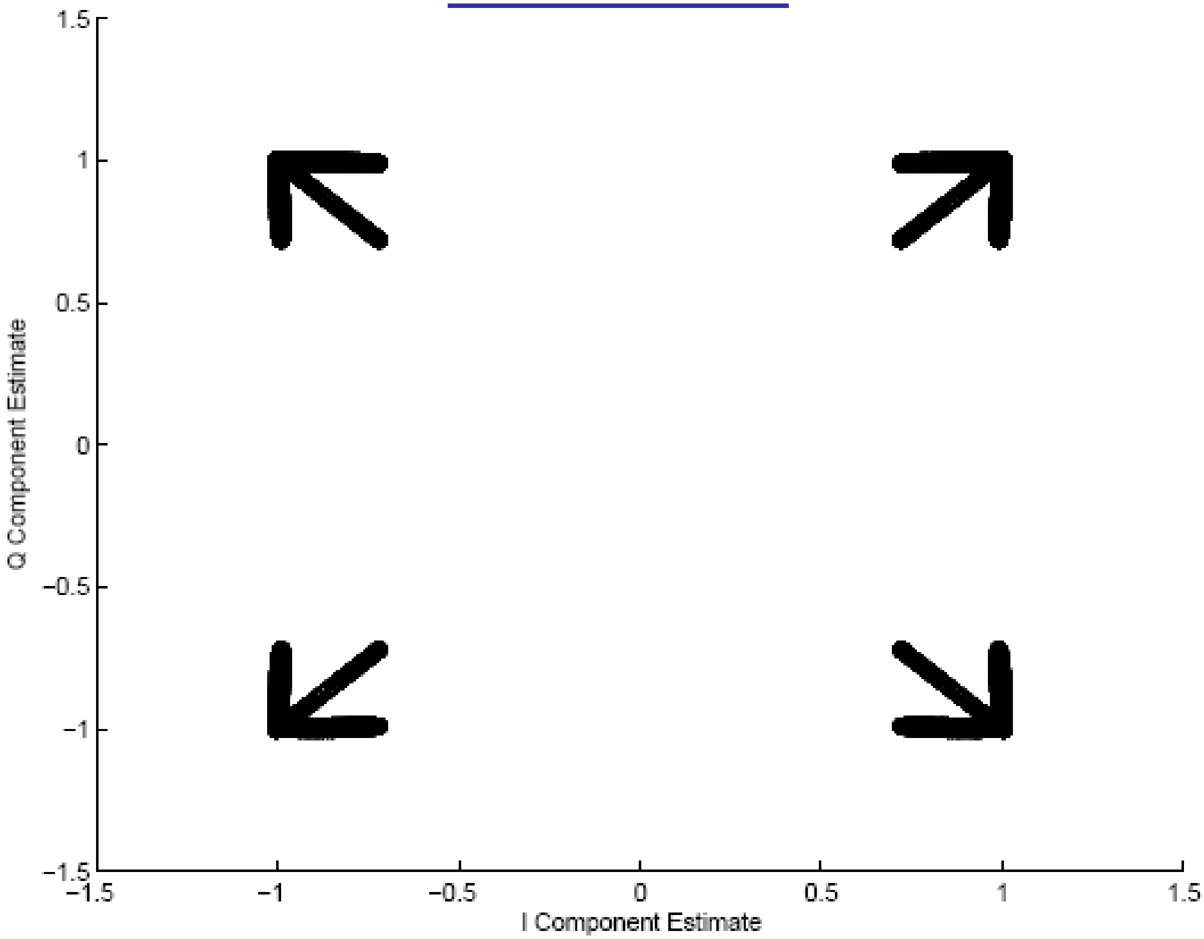


- ❑ 200 Ms/s is sufficient for Eb/No = 4~5 dB.

☞ Time-interleaved ADC architecture needs: 12 ADCs @ 264 Ms/s.

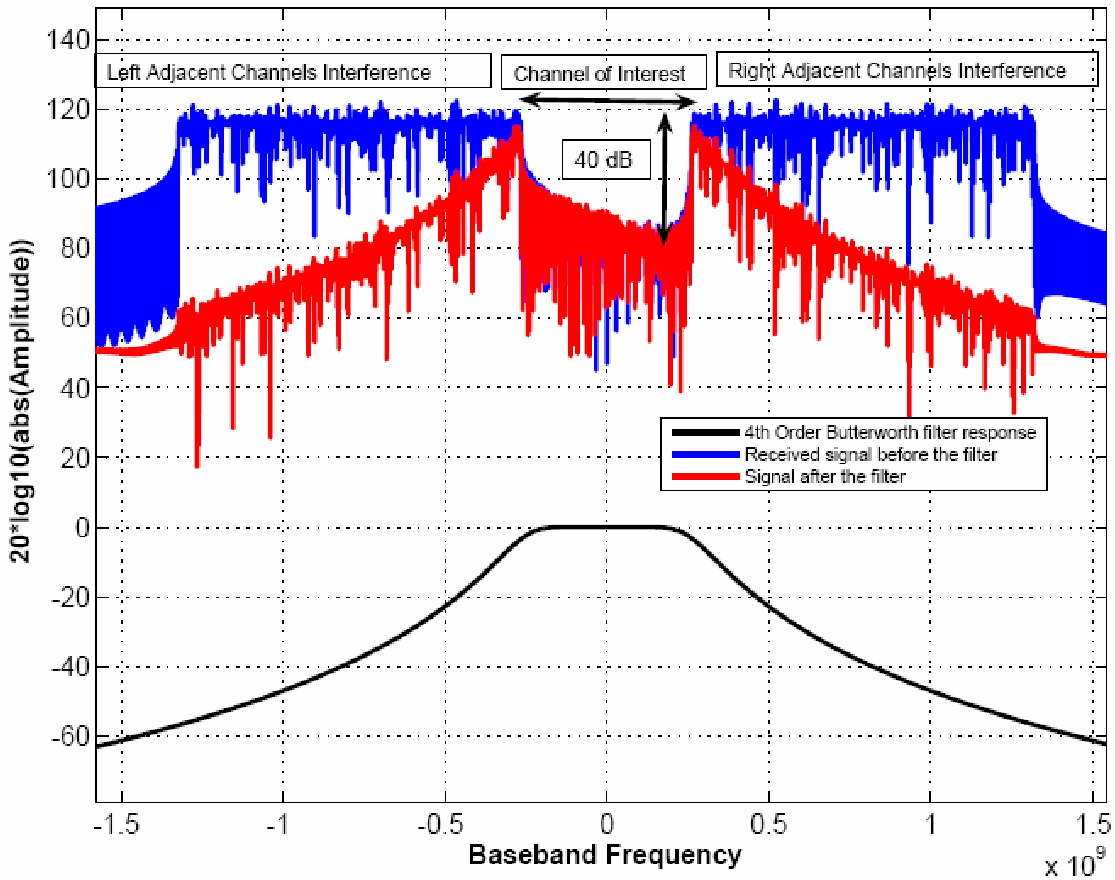
☞ This is an aggregated sampling rate reduction of 768 Ms/s.

Structure of Error in Truncated MF Solution



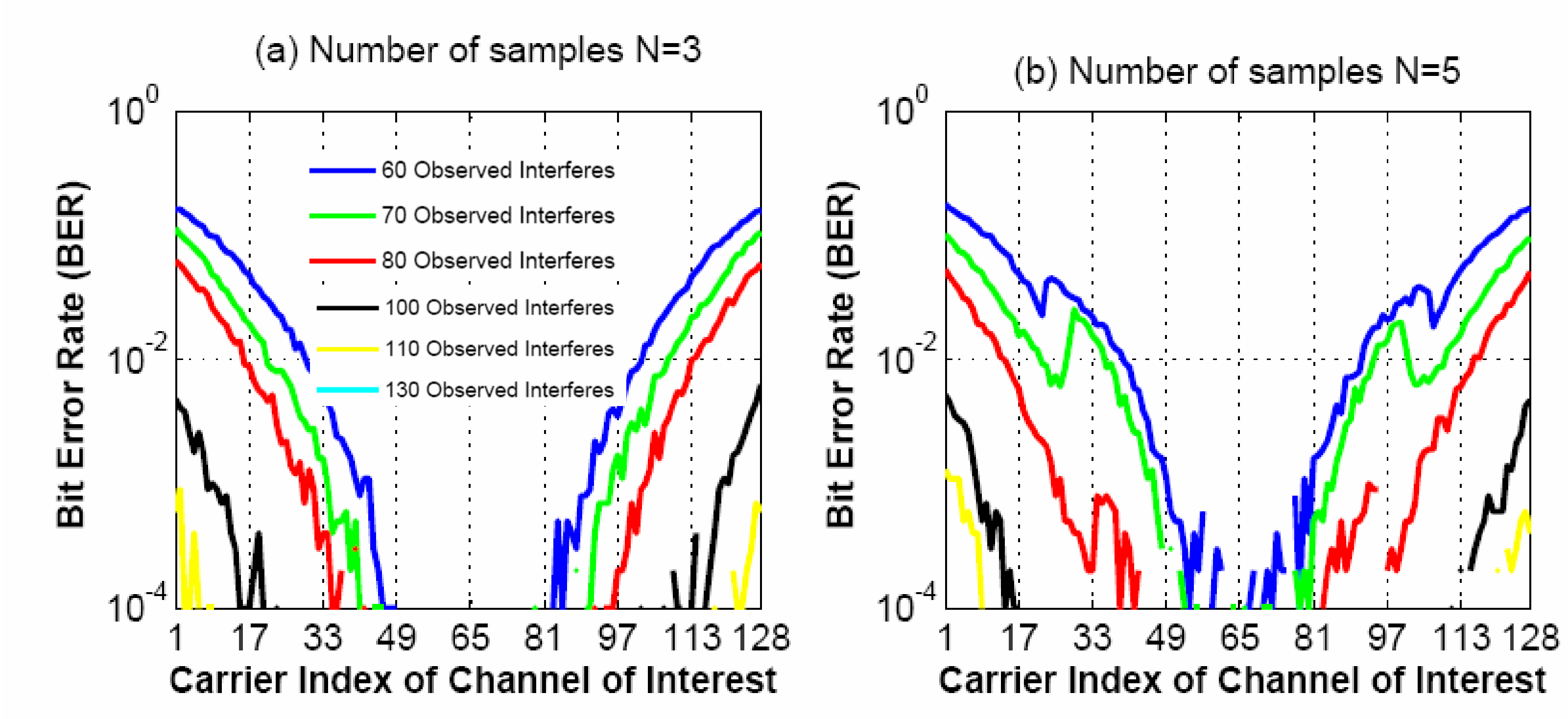
- ☞ For SNR > 6 dB this truncation error limits the performance.
- ☞ Least-Squares or MMSE are possible but come with higher complexity.

Robustness to Adjacent Interference



- Each channel has 128 carriers
- 5 channels of 528MHz each
- Adjacent channels are 40 dB stronger
- 4th order Butterworth filter used at the front end.
- Standard OFDM receiver would be blocked by the interferers.

BER Performance



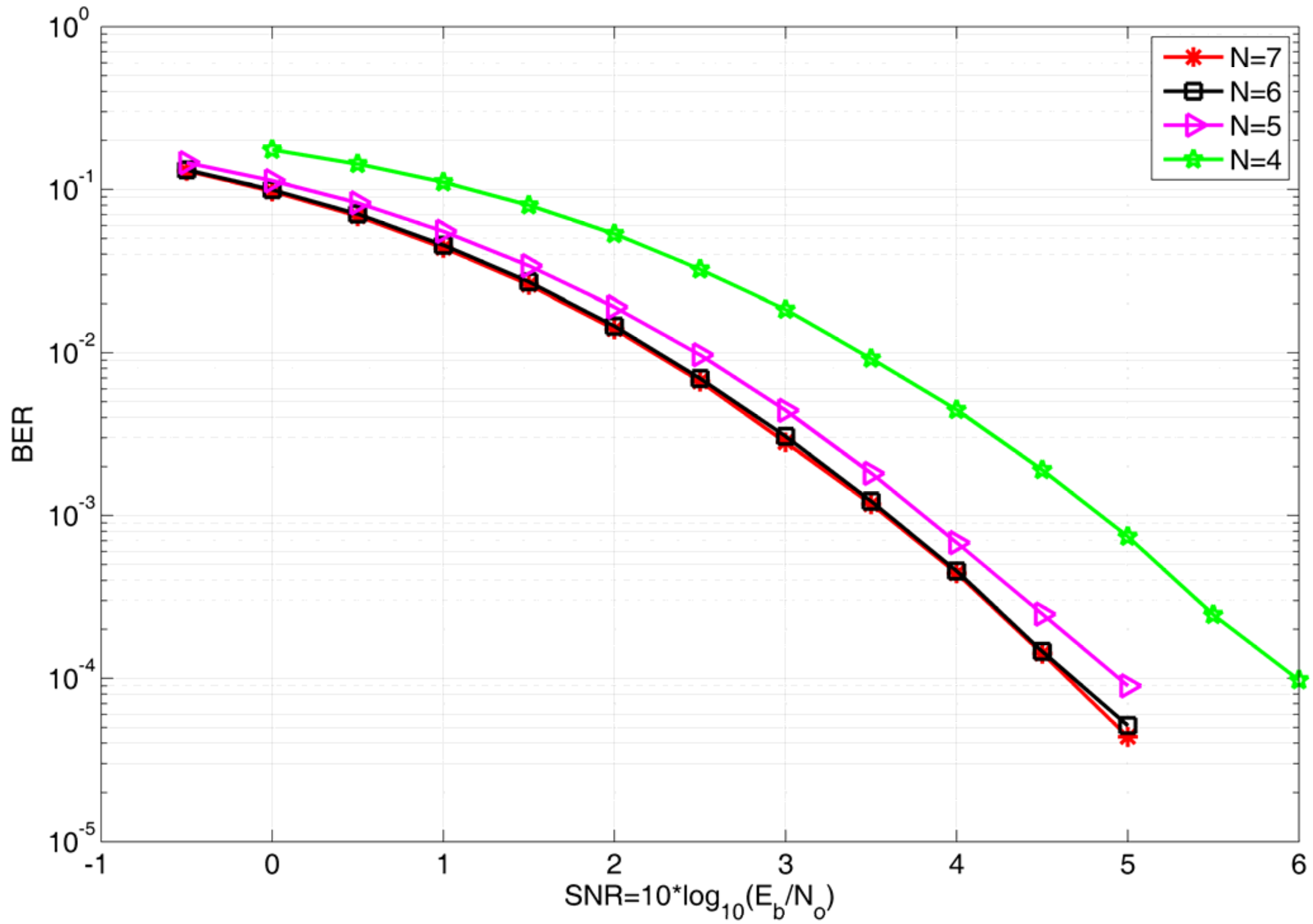
- ❑ Adjacent carriers spill over the channel of interest due to the limited number of frequency samples.
- ❑ In this example, need to detect additional 130 adjacent interferers to achieve perfect symbol recovery.

DS-SS Coded BER Performance

- Rc=1/2 convolutional code :

$$\left[1 \quad \frac{1+D^2}{1+D+D^2}\right]$$

- N=8 samples per chip duration is Nyquist rate.
- No performance loss for N=7 and N=6
- Slight performance loss for N=5
- 1 dB loss @ 10^-4 for N=4 (half Nyquist rate)



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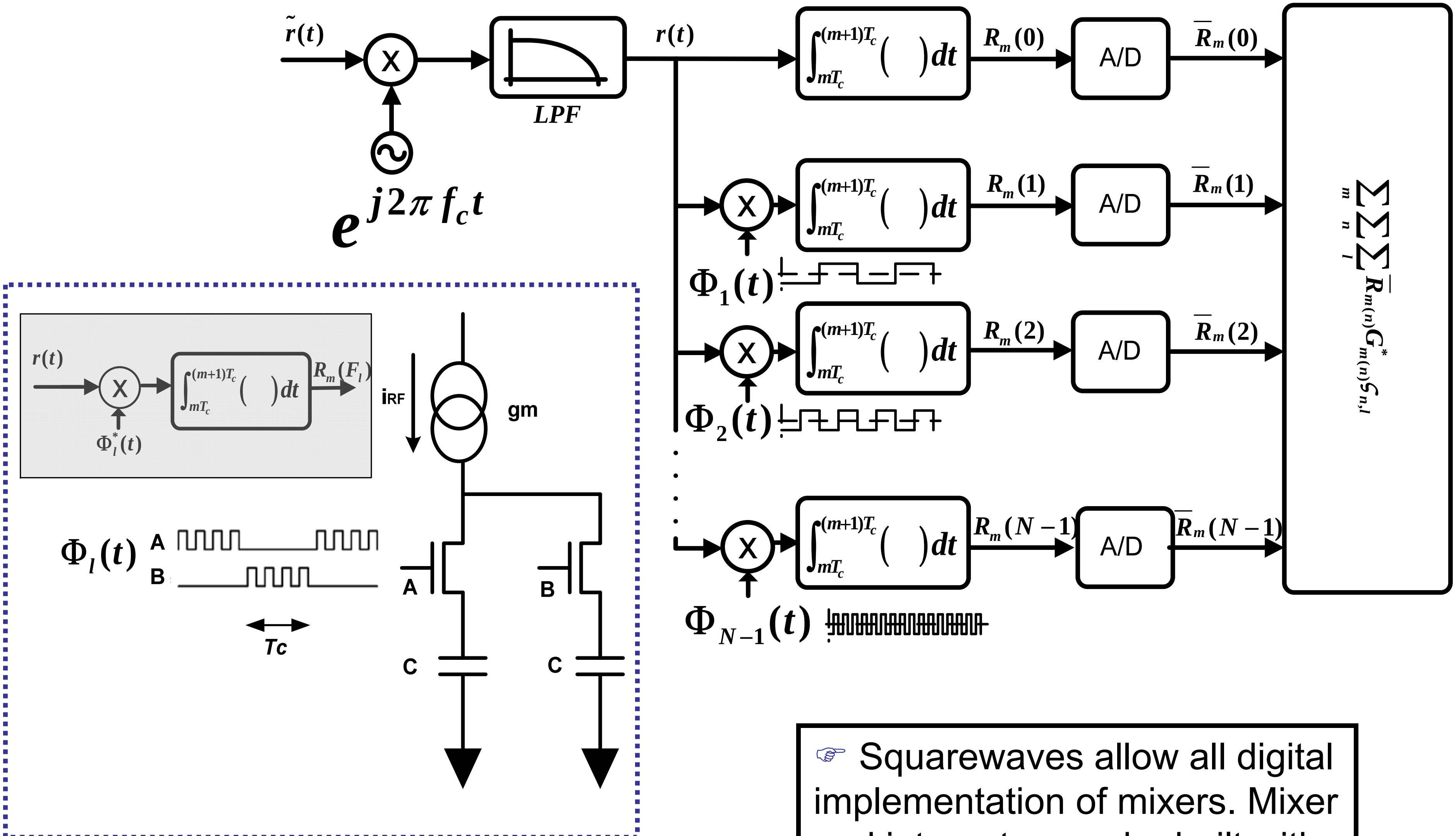
Frequency-Domain MC Receiver



☞ Squarewaves allow all digital implementation of mixers. Mixer and integrator can be built with passive switched caps.

Receiver Impairments

- *Gain mismatches* : Mismatches of capacitors and currents. This can be calibrated.

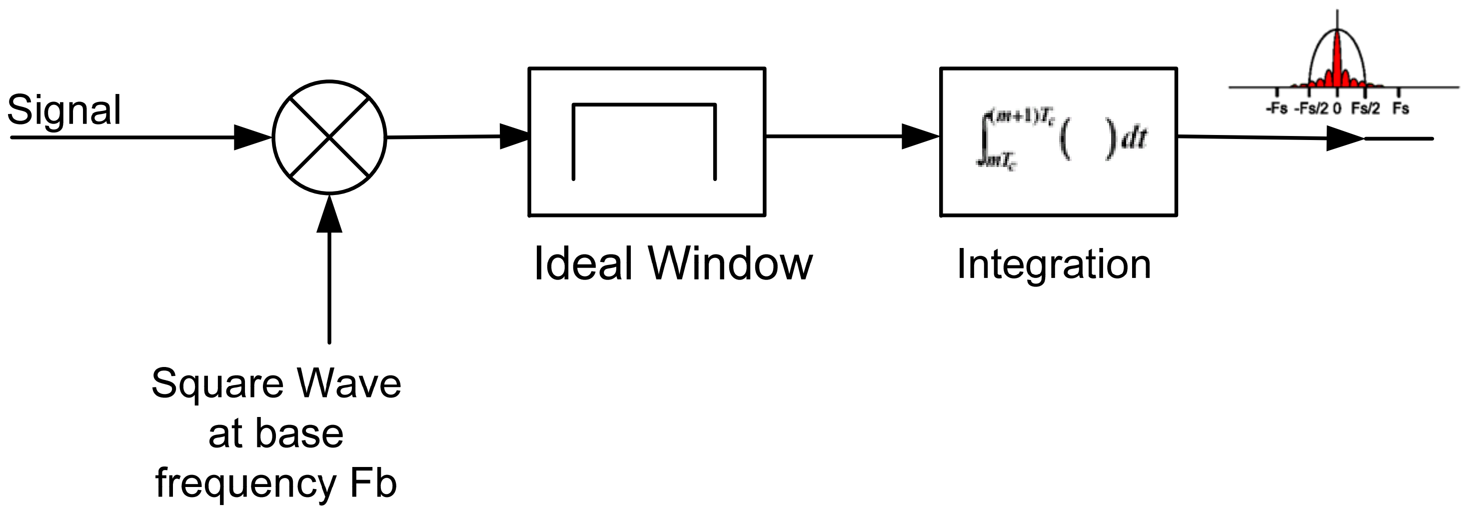
- *Linearity of mixers*: Mixers with very high linearity have been reported for front-end filtering in GSM and Bluetooth.

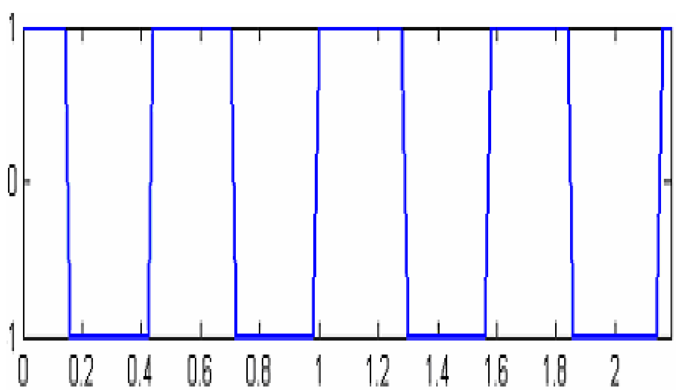
- *Frequency Offset*: Frequency mismatch between TX and RX oscillator frequencies. It can also be calibrated to certain extend.

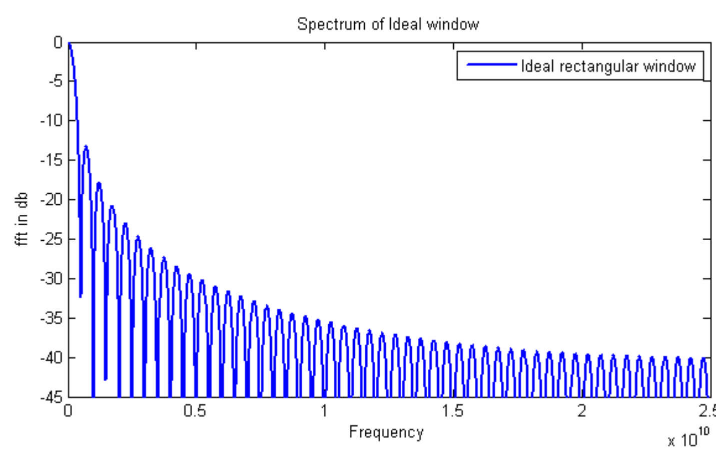
- *Phase noise*: Jitter in oscillators and integration window. This is random noise and cannot be completely removed.

LO Mixing

1) Ideal square wave LO signal and sharp window:

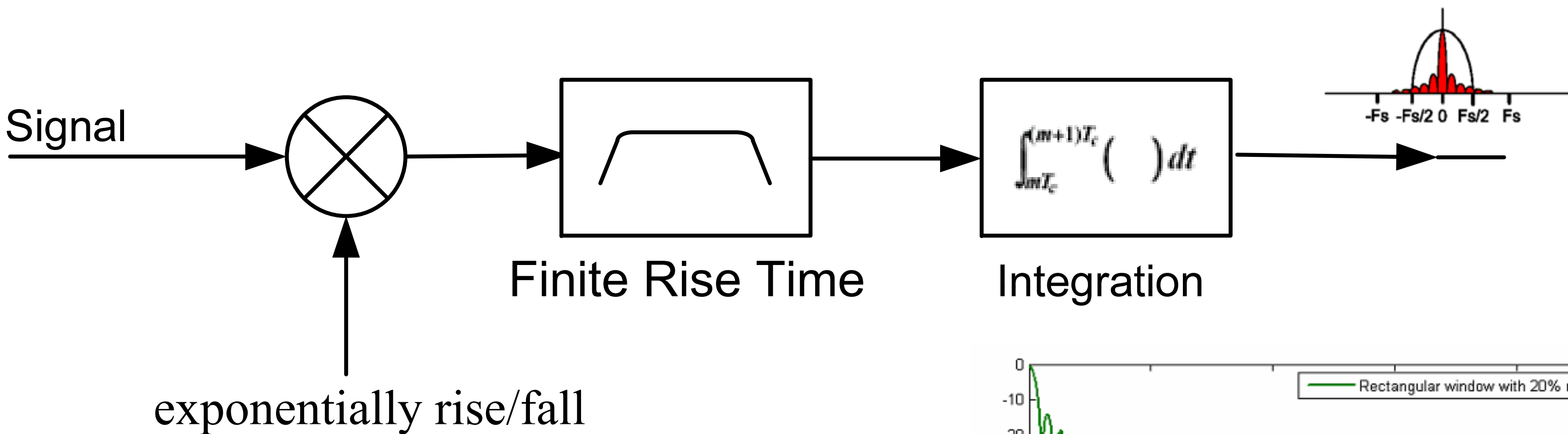


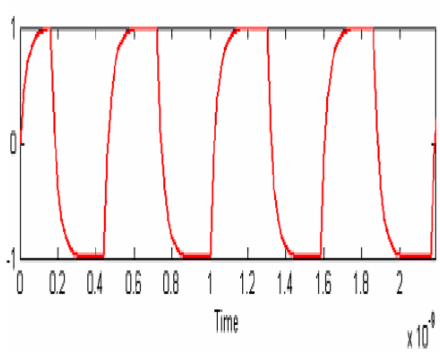


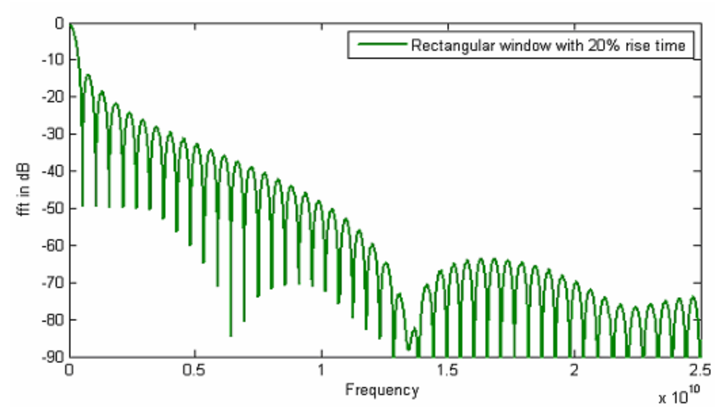


LO Mixing (Contin…)

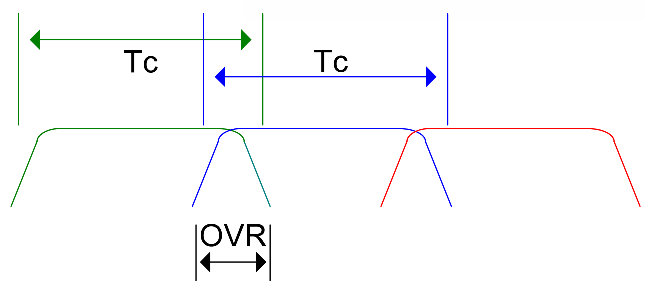
2) Exponentially rising/falling LO signal and smooth window:



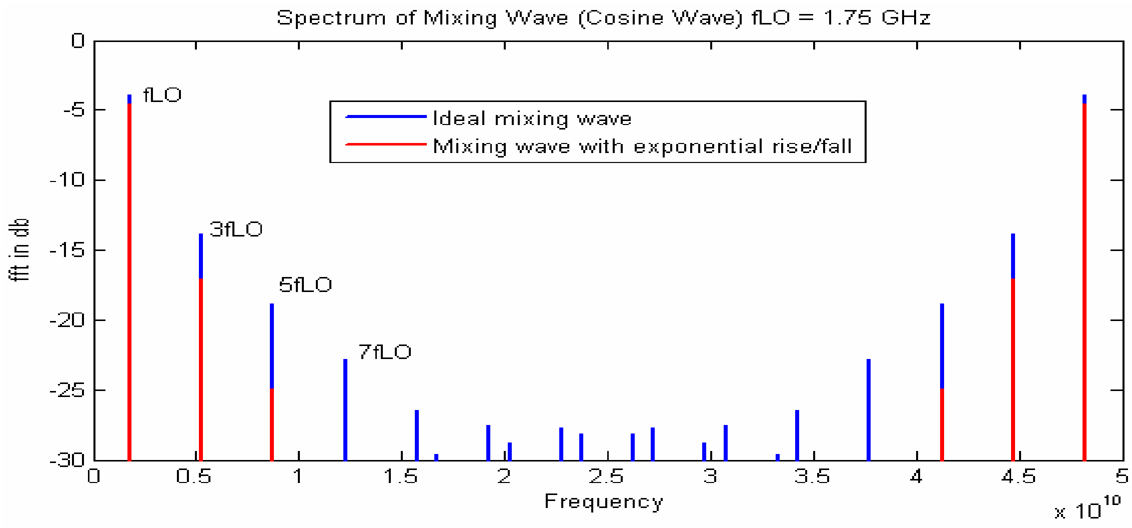


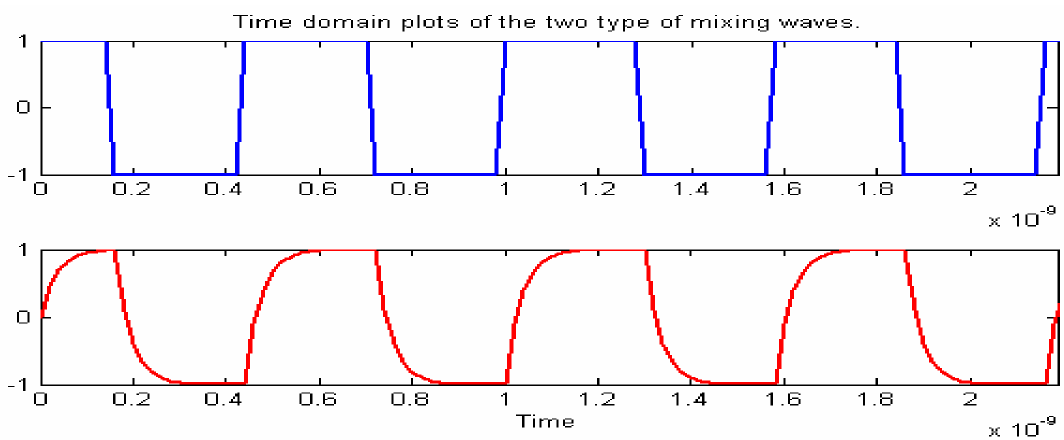


Window overlapping :

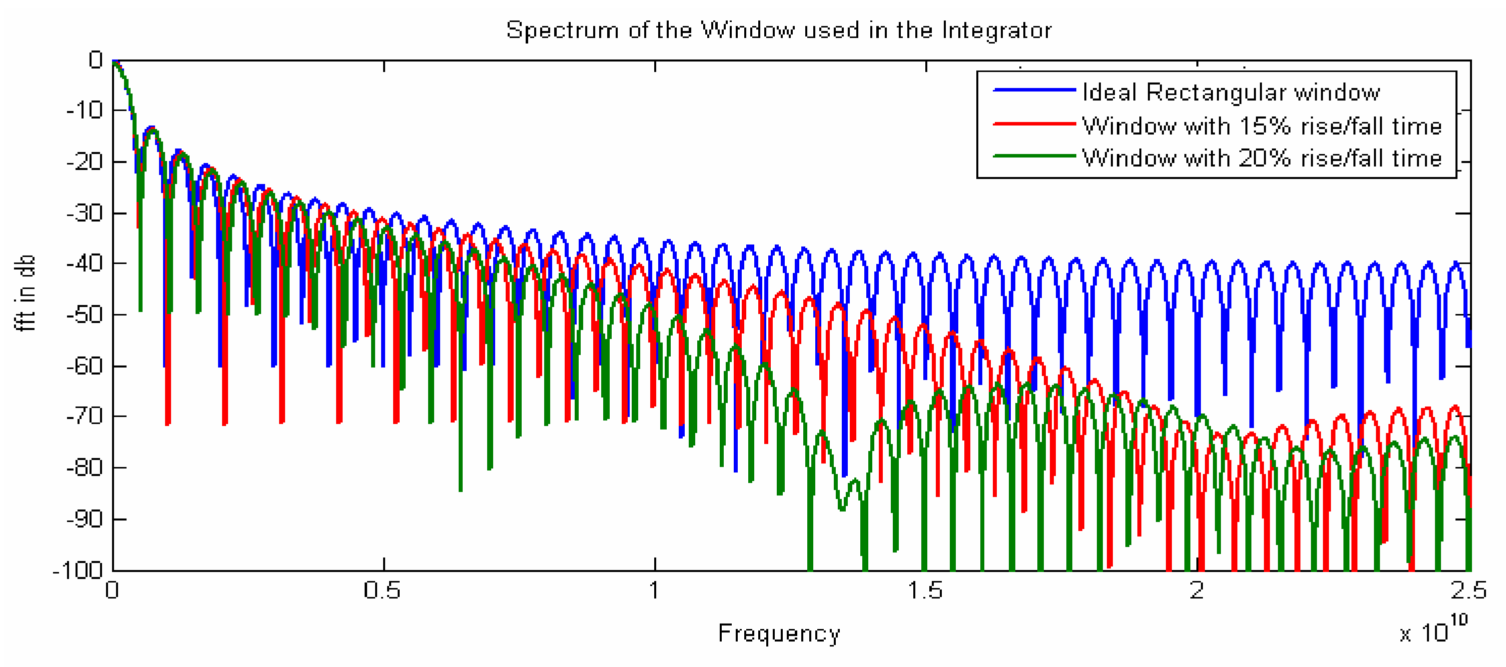


LO clock rising/falling times

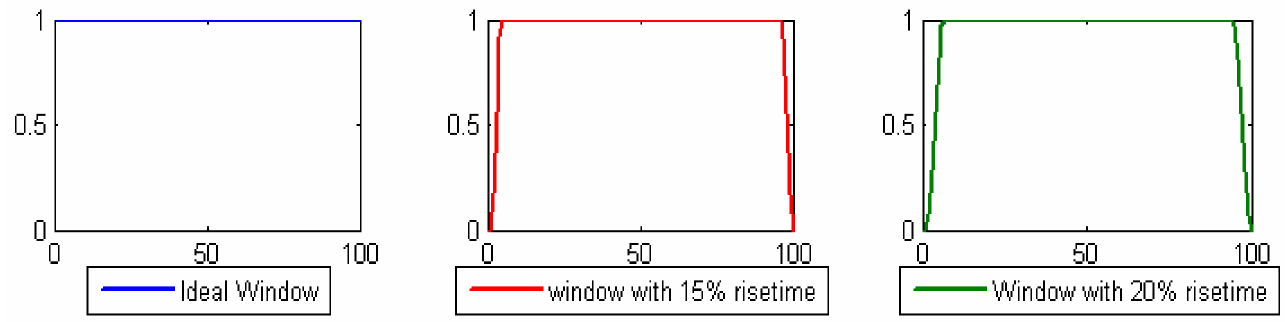




Windowing



Spectrum of the Window used in the Integrator
fft in db
Frequency
x 10^10
Ideal Rectangular window
Window with 15% rise/fall time
Window with 20% rise/fall time
0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
0
0.5
1
1.5
2
2.5



Ideal Window
window with 15% risetime
Window with 20% risetime
1
0.5
0
50
100

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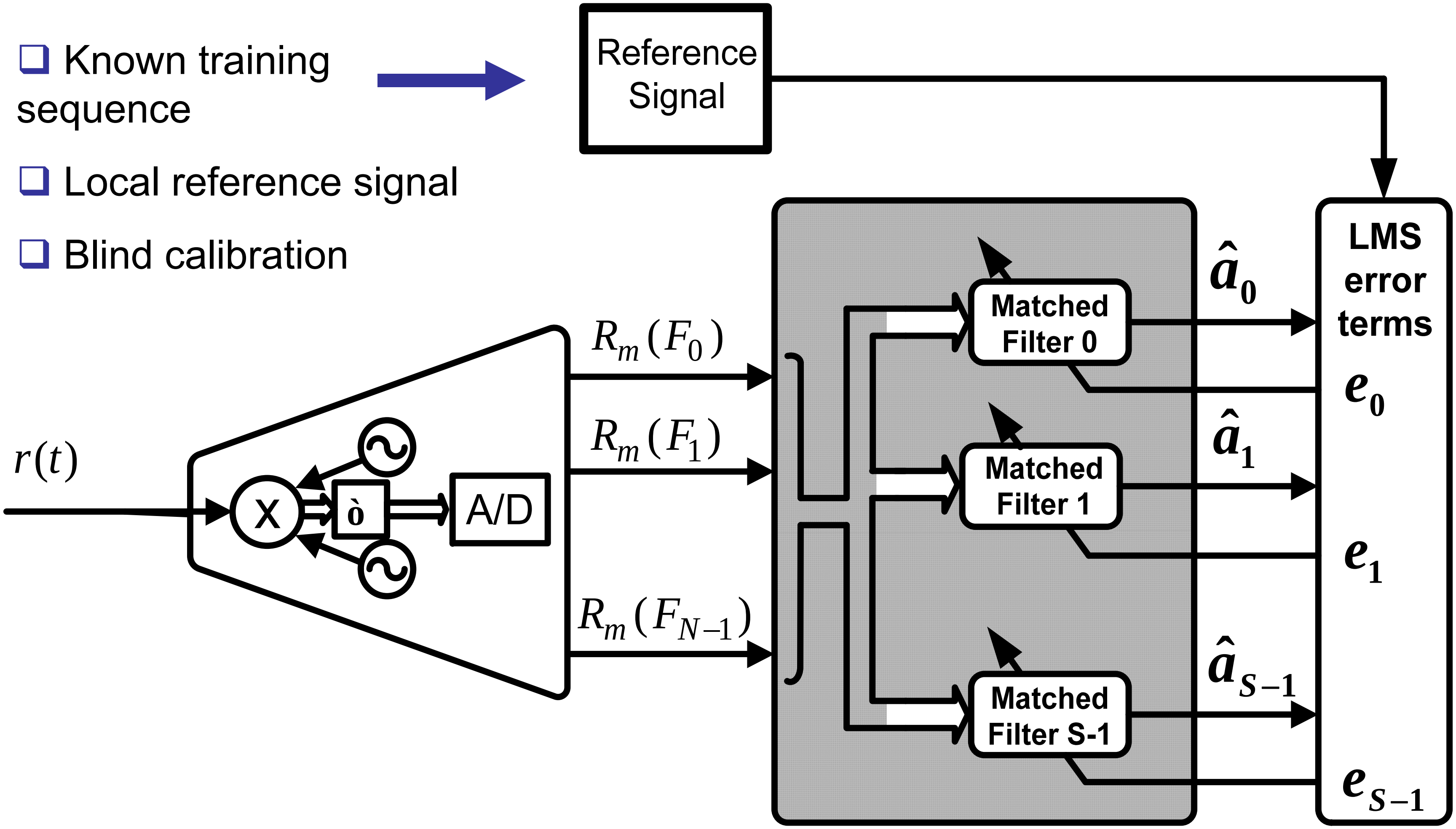
- Conclusions.

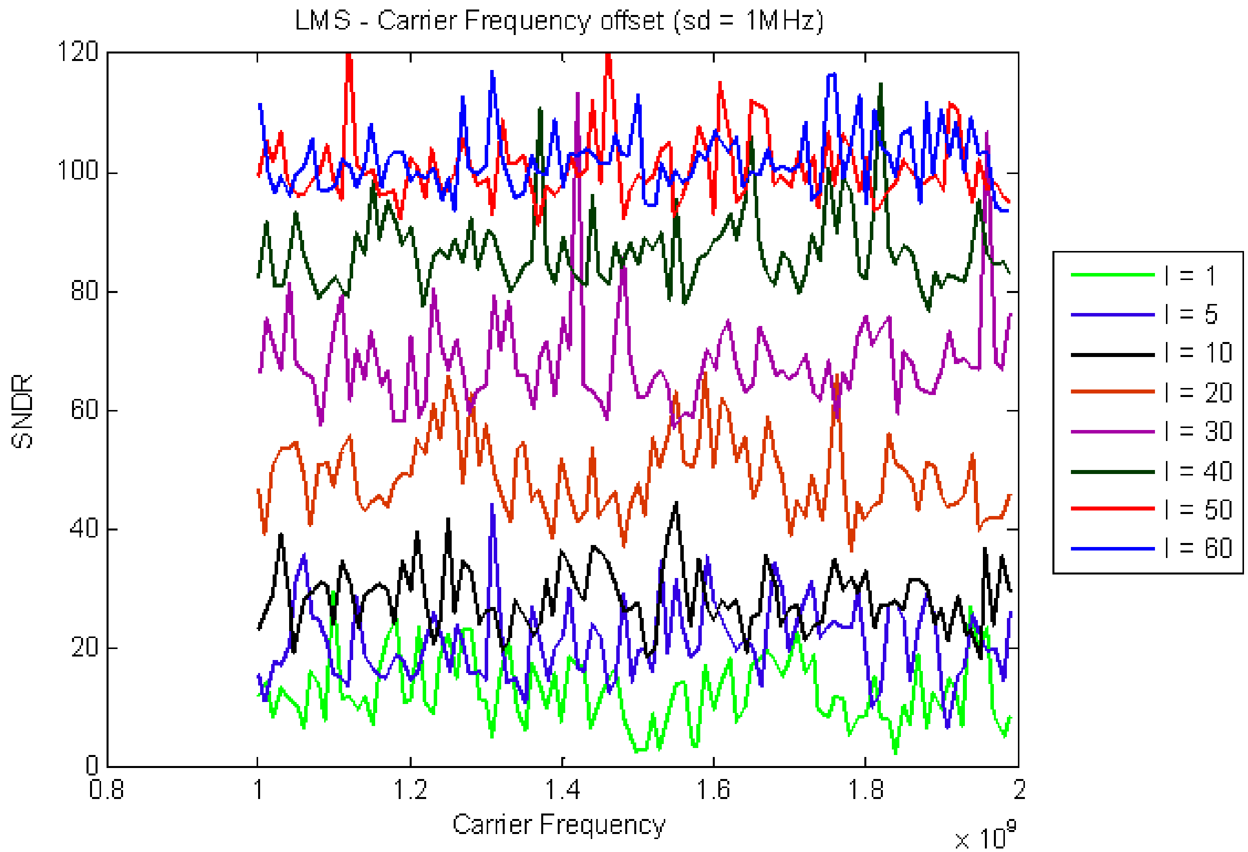
Fully Calibrated Frequency-Domain Receiver

- ❑ Known training sequence
- ❑ Local reference signal
- ❑ Blind calibration



☞ RF, analog, digital baseband and mixed-signal algorithm are jointly designed. Can this scheme calibrate RF (oscillators, mixers) ?

LMS calibration for mismatches in the receiver



❑ Mismatches included in the simulations:

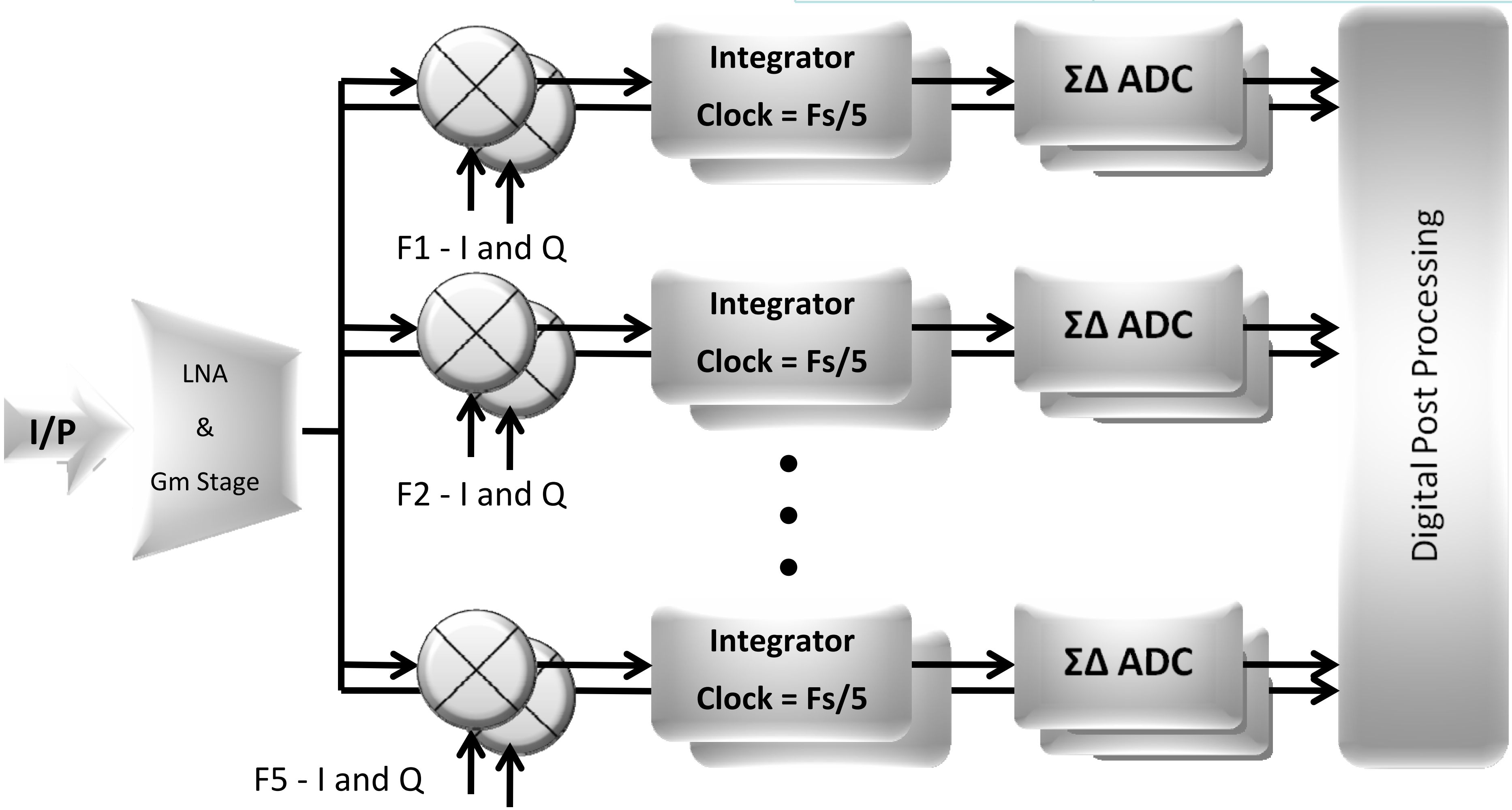
- Input Signal has an SNDR of 100 db. ‘I’ indicates the number of iterations.
- A time offset in the input signal block (1 ns)
- Type of mixing wave (The estimation matrix assumes ideal square waves, but the actual receiver has an exponential rise and fall in the square wave.
- Frequency offset in the mixing wave and the input sub-carriers.

Outline

- Narrow-band, wideband and ultra-wideband in software define radio architectures.
- Parallelization of ADCs and RF front-ends for broadband receivers. The frequency-domain sampling solution.
- Broadband multicarrier communication receiver based on analog to digital conversion in the frequency domain.
- Fully calibrated frequency-domain receiver.
- Design examples :
  - Multi-standard GSM, Bluetooth, IEEE802.11g, Wimax and UWB.
  - 2 Gs/s, 11 bits broadband multicarrier receiver via sampling in the frequency-domain.
- Conclusions.

Multi-Standard Receiver Front-end

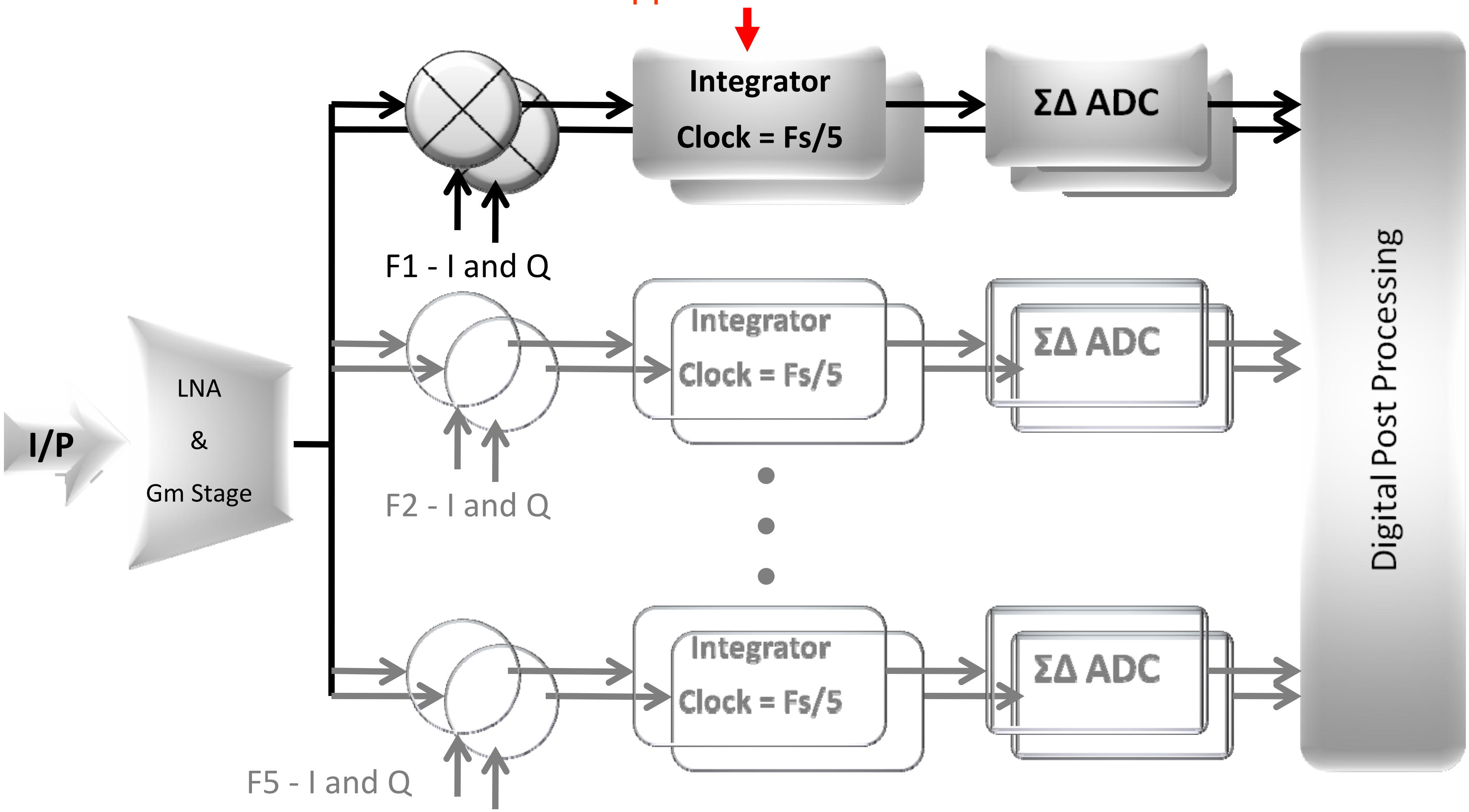
STANDARD	SPECIFICATIONS
UWB	500 M S/s and 5 bits
802.11 G	50 M S/s and 8 bits
Bluetooth	1 MHz and 12 bits
GSM	200 KHz and 14 bits



Multi-Standard Receiver Front-end

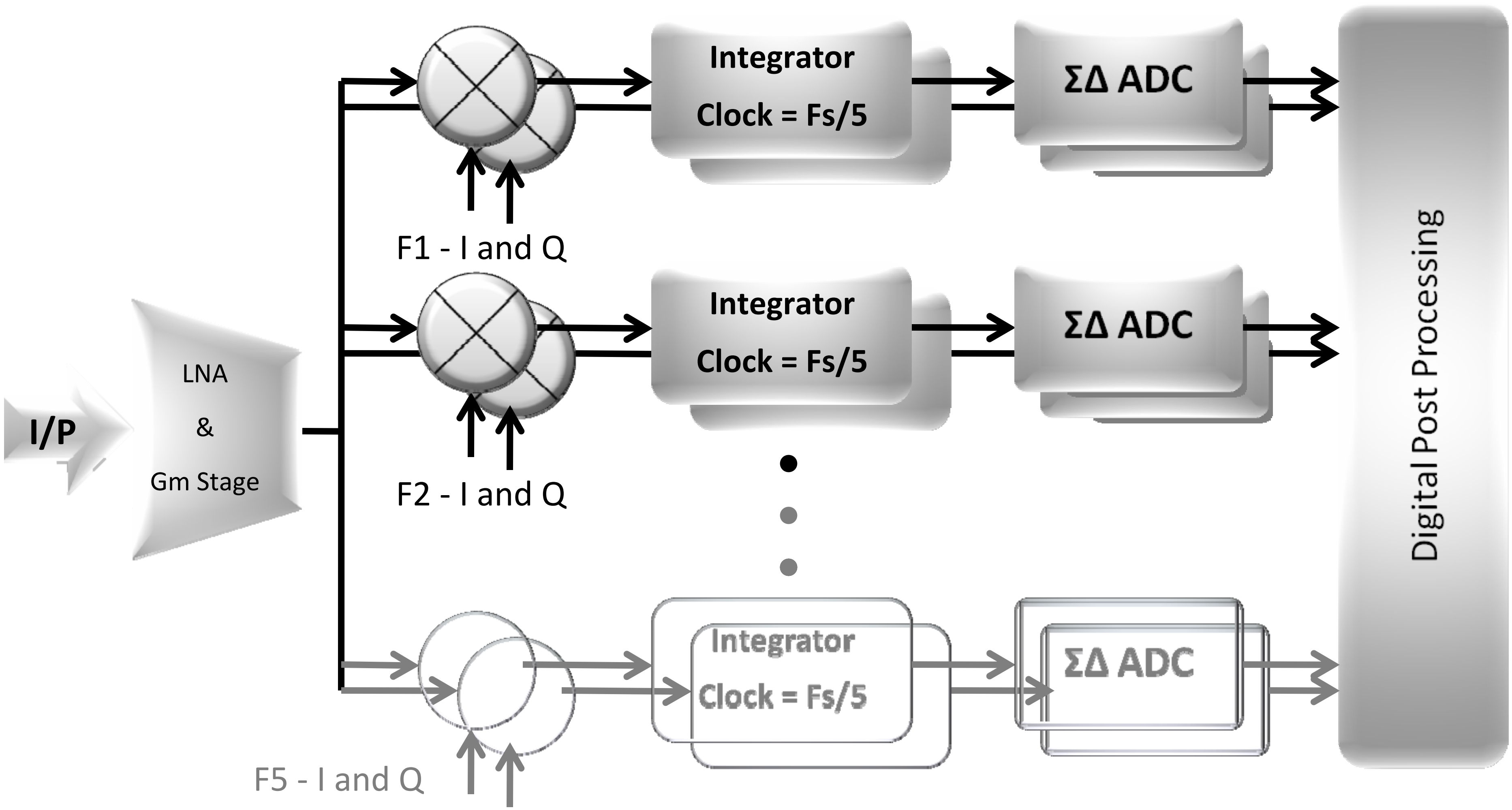
GSM	200 KHz and 14 bits
Bluetooth	1 MHz and 12 bits

Can use a better filter; TI DRP group approach for instance



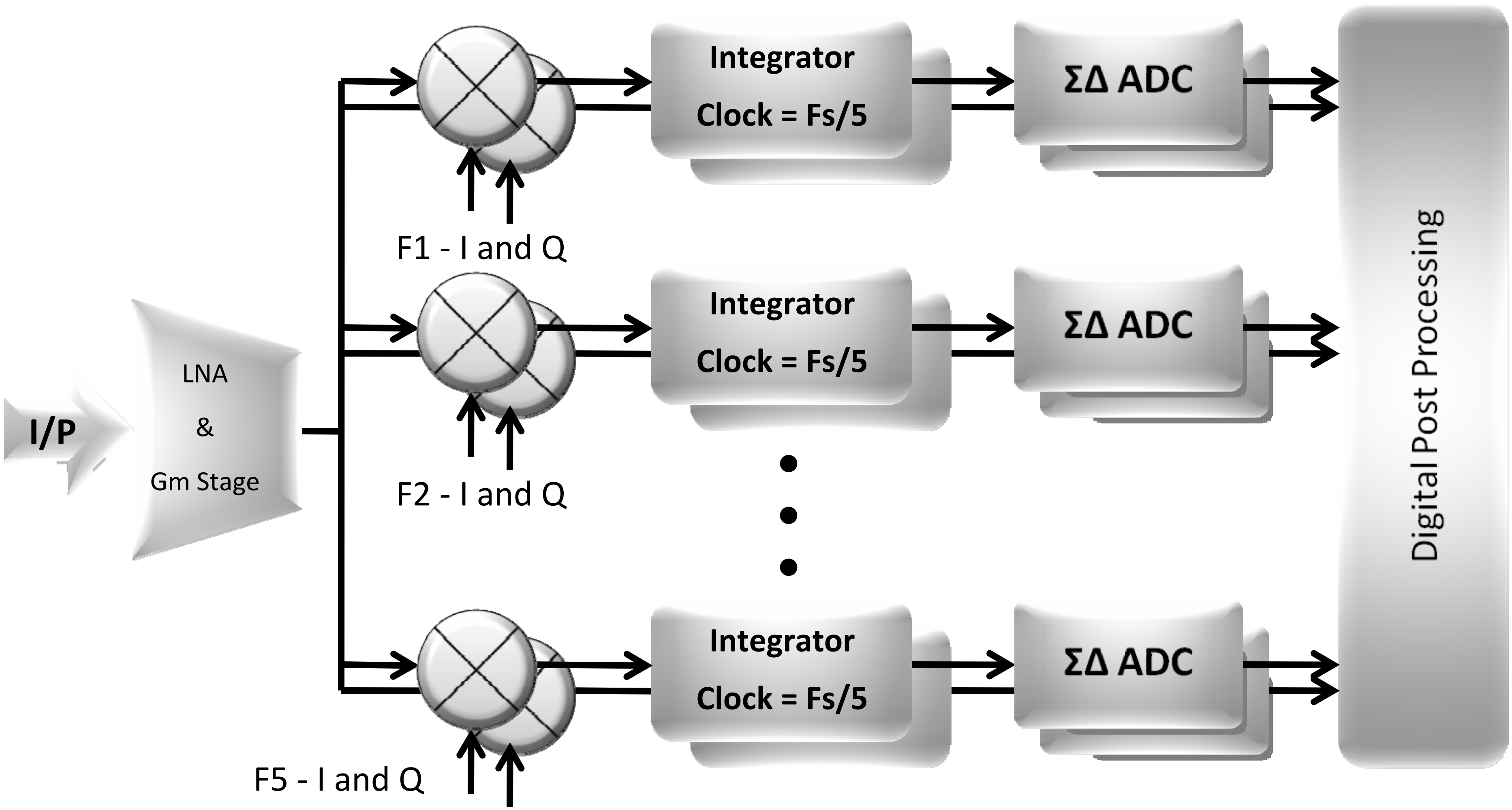
Multi-Standard Receiver Front-end

802.11 G	50 M S/s and 8 bits

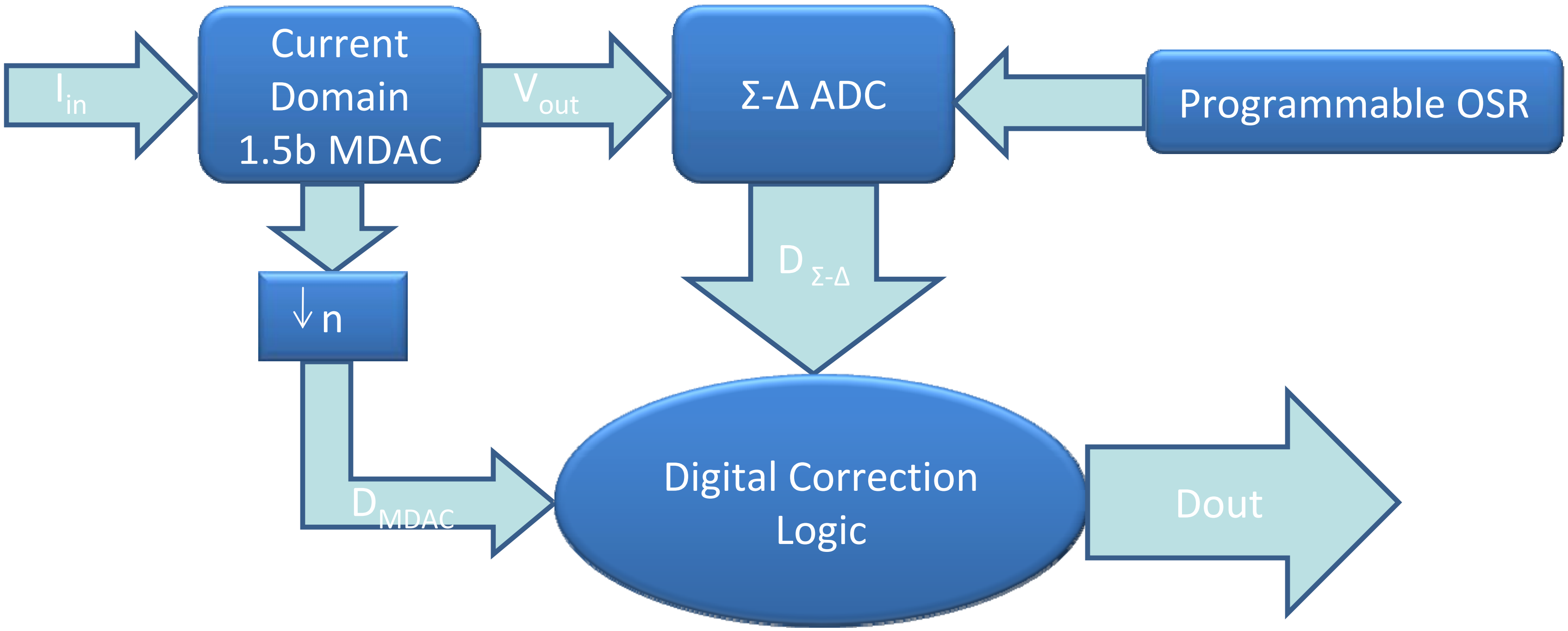


Multi-Standard Receiver Front-end

UWB	500 M S/s and 5 bits



Multi-Standard Receiver Programmable ADC



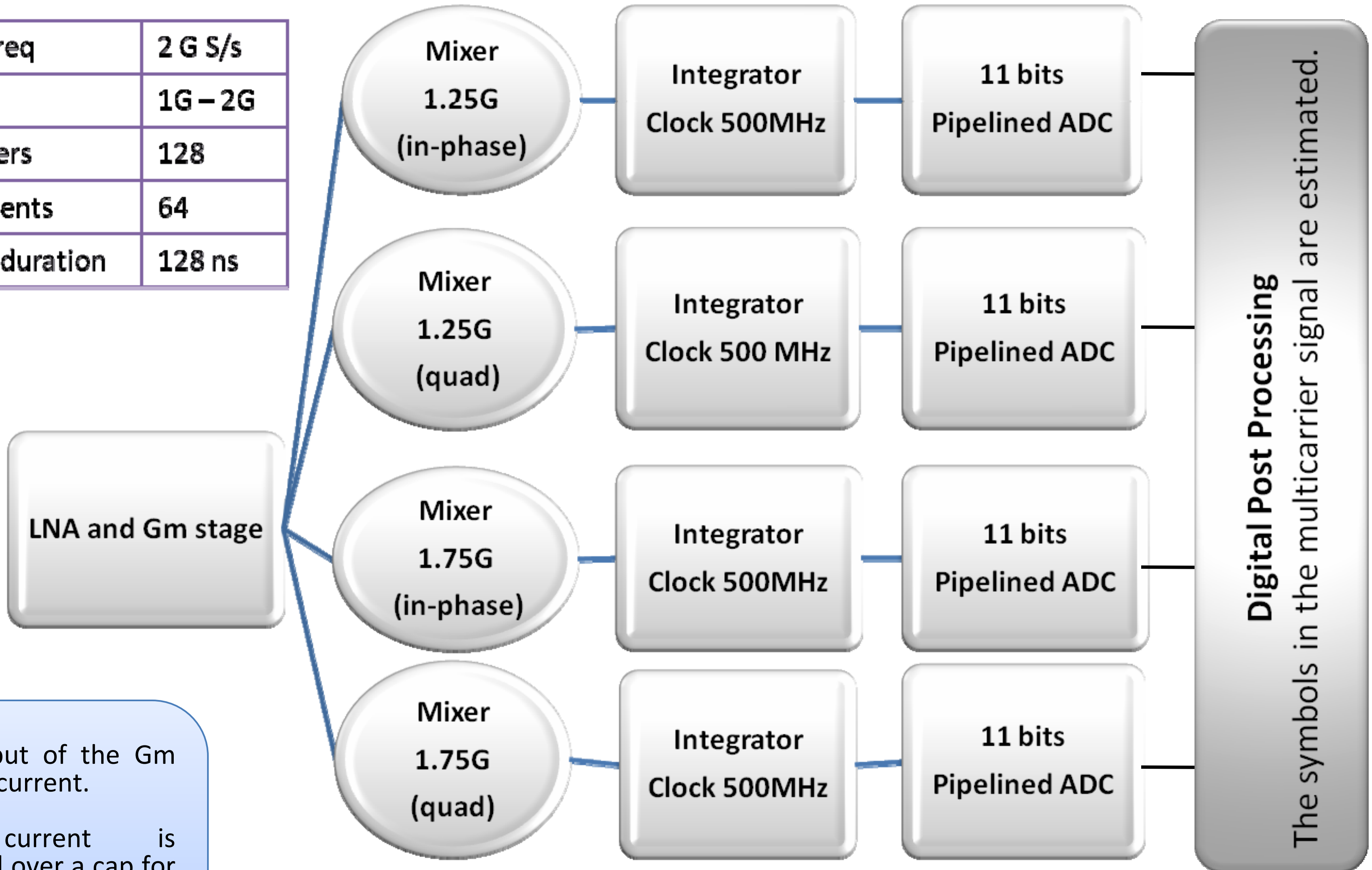
STANDARD	SPECIFICATIONS
UWB	500 M S/s and 5 bits
802.11 G	50 M S/s and 8 bits
Wimax	11MHz/Channel and 11 bits
Bluetooth	1 MHz and 12 bits
GSM	200 KHz and 14 bits

Advantages

- OSR of the Σ-Δ can be changed to exchange resolution and sampling rate
- Sampling capacitor of the MDAC is smaller by the OSR

2 Gs/s, 11 bits Multicarrier Receiver

Sampling Freq	2 G S/s
Bandwidth	1G – 2G
No. of Carriers	128
No. of segments	64
Total Signal duration	128 ns

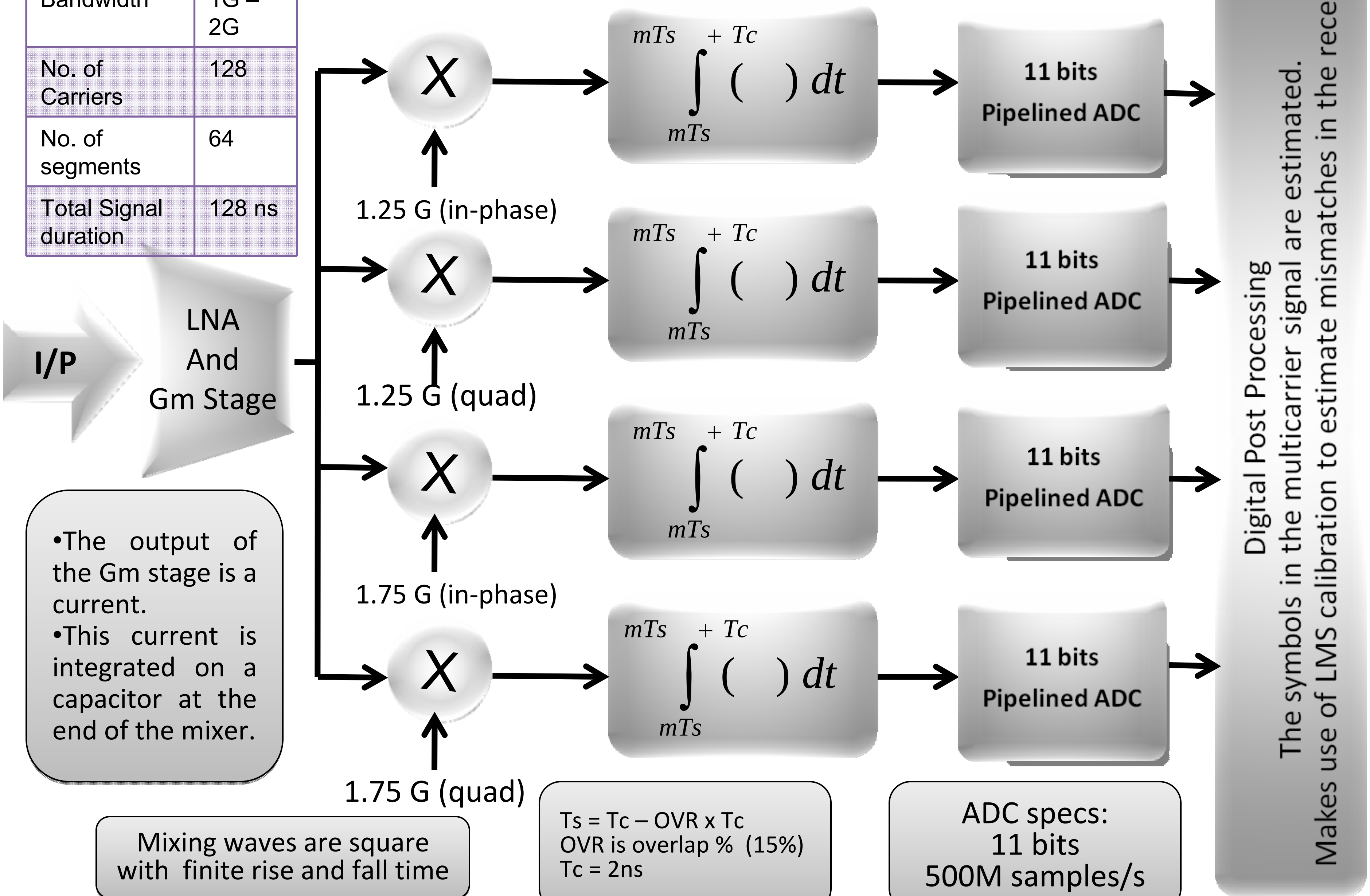


- The output of the Gm stage is a current.
- This current is integrated over a cap for 2ns.
- This integrated value is sampled and quantized.

The Digital Post Processing block has LMS calibration to learn for mismatches in the receiver like time offset, carrier frequency offset and mismatches in the mixing wave.

Architecture of the High Speed Multicarrier Receiver

Sampling Freq	2 G S/s
Bandwidth	1G – 2G
No. of Carriers	128
No. of segments	64
Total Signal duration	128 ns



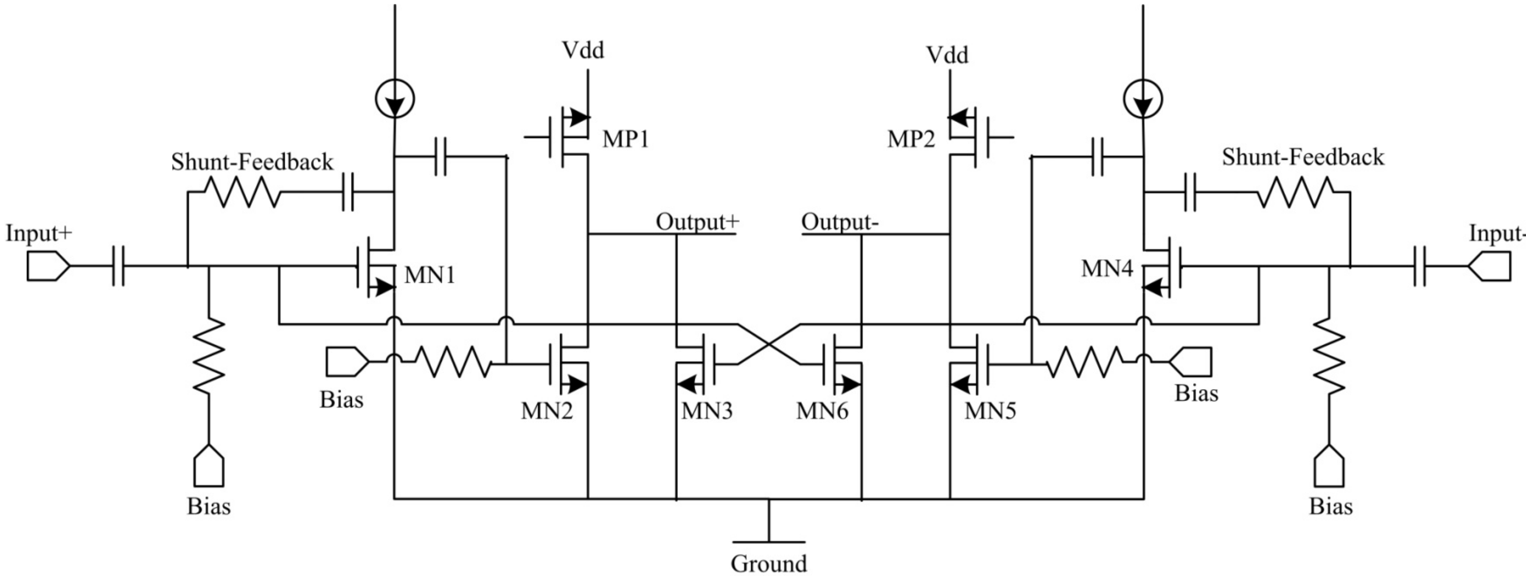
- The output of the Gm stage is a current.
- This current is integrated on a capacitor at the end of the mixer.

Mixing waves are square with finite rise and fall time

Ts = Tc – OVR x Tc
OVR is overlap % (15%)
Tc = 2ns

ADC specs:
11 bits
500M samples/s

LNA Architecture



Advantages

- The first of the LNA is a shunt feedback stage
- Second stage consists of cross coupled transconductance to cancel noise generated in the first stage
- Noise of second stage is less when referred to the input
- The corner frequency of Flicker noise in 65nm is around 3GHz
- Topology provides good Noise Figure

LNA Specification

Stage – 1 Gain Stage

Parameter	Specs
Gain	13dB
IIP3	5dBm
S11	<-10dB
Bandwidth	2GHz

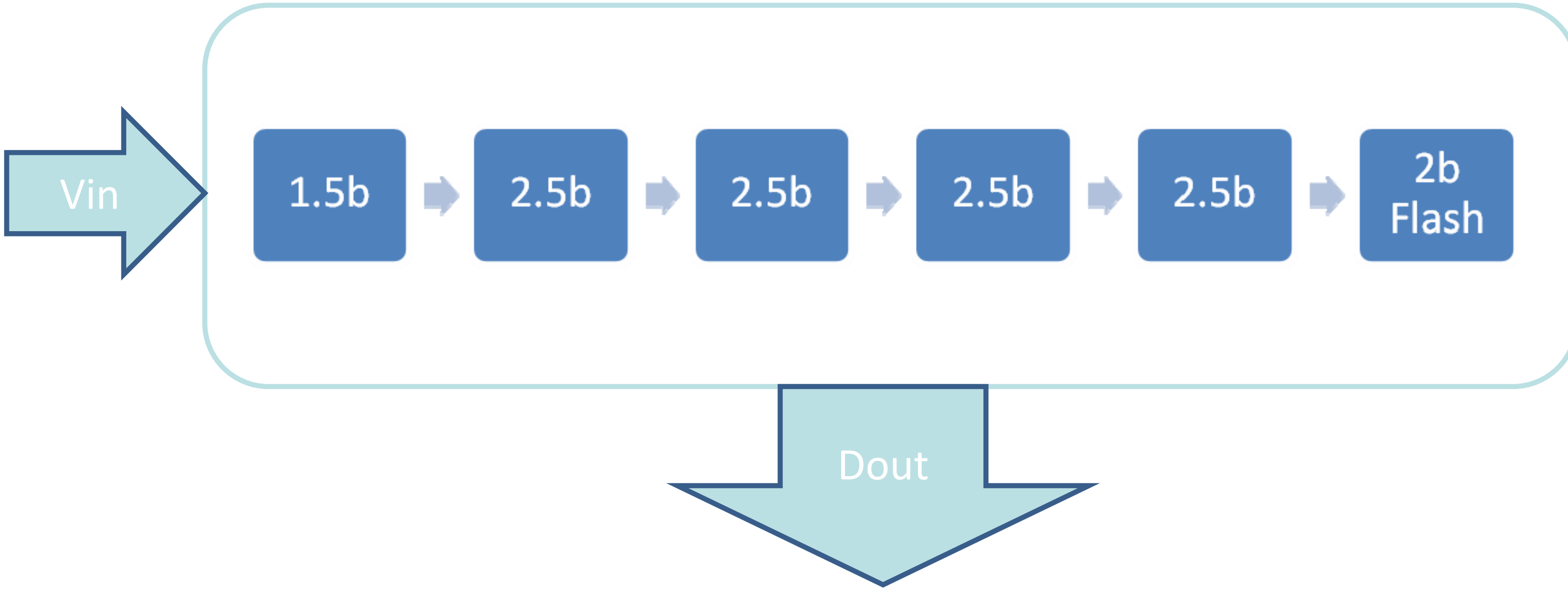
Stage – 2 Transconductance

Parameter	Specs
Gm	140mA/V
IIP3	13dBm

Overall

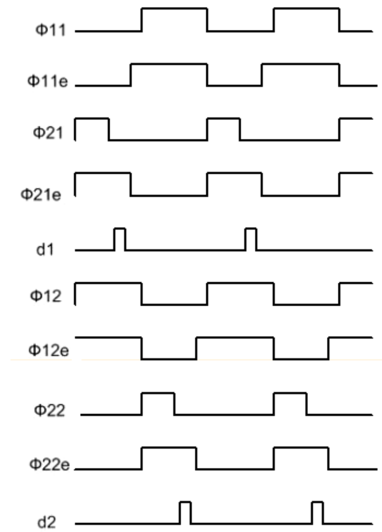
Parameter	Specs
Gm	0.63A/V
IIP3	-2dBm
S11	<-10dB
Bandwidth	2GHz
Output Current @input=-37dBm	2mA

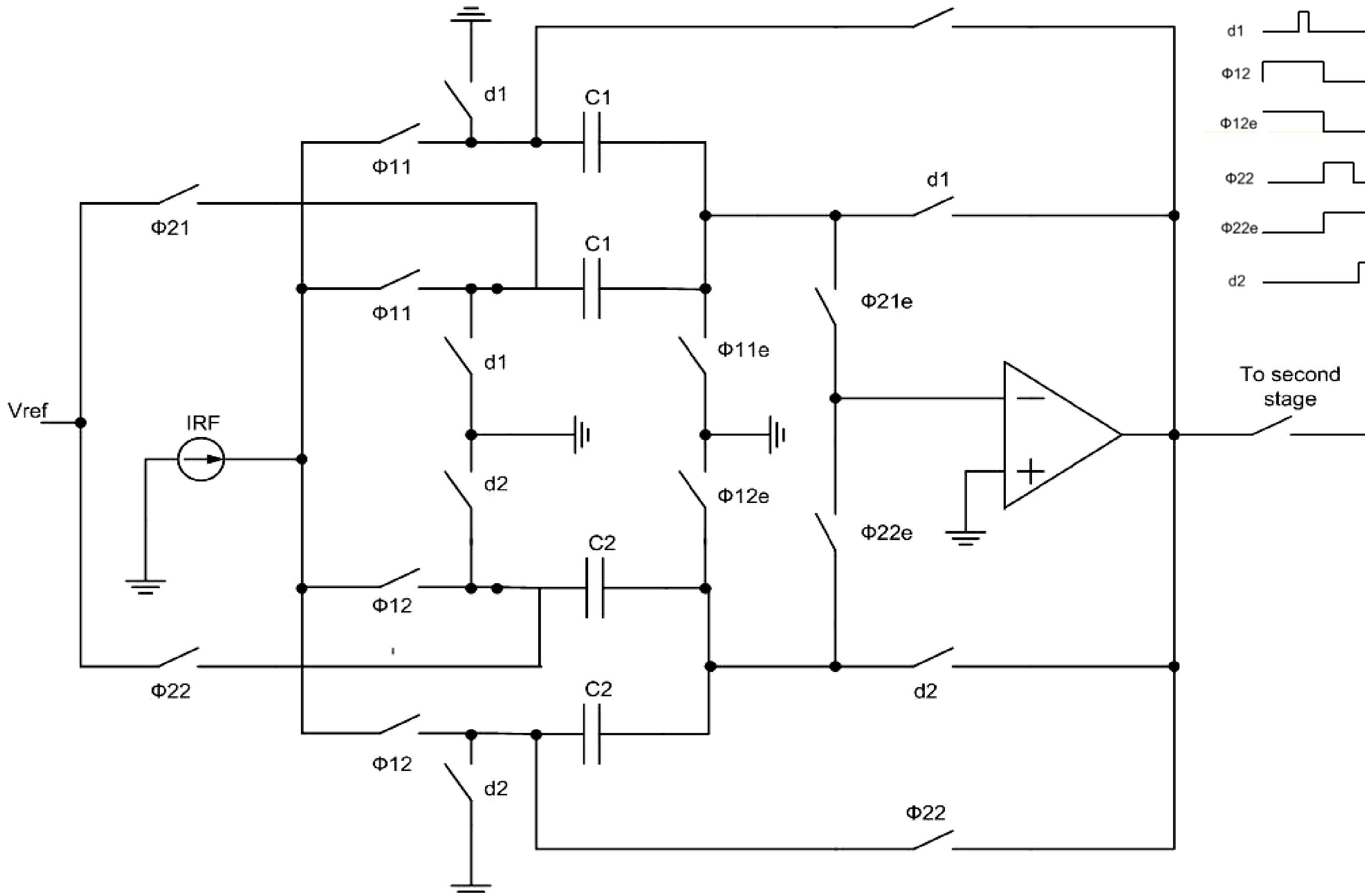
Pipeline Architecture 11 bits, 500MHz



- First stage of the pipeline needs to be designed for current sampling
- Later stages are the same as in any normal ADC
- Flicker noise is a major problem in 65nm - PA auto zeroing employed to cancel some of the flicker noise

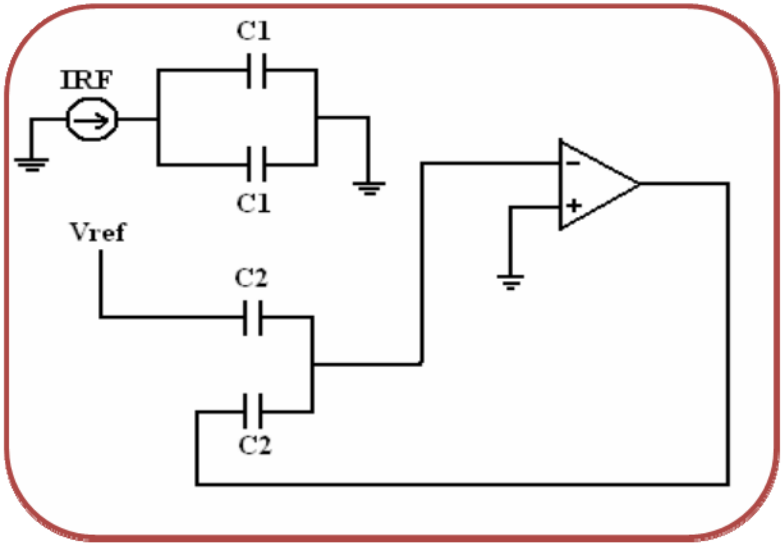
MDAC First Stage



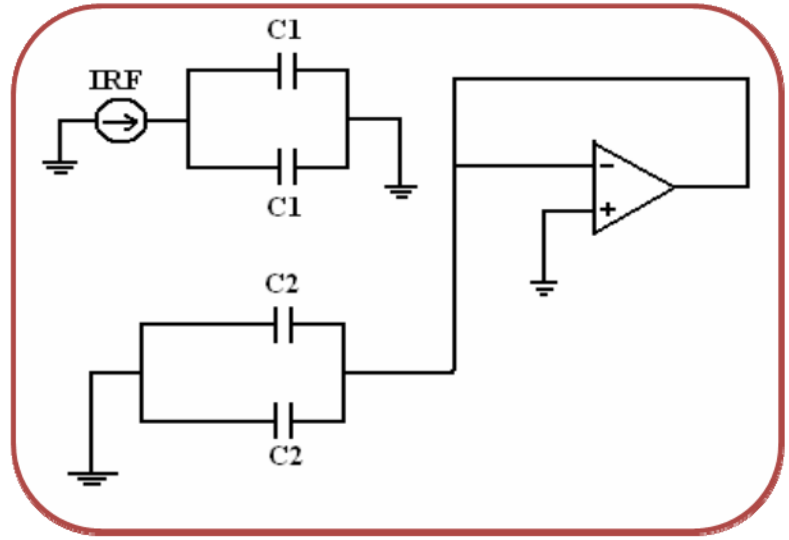


- C1 and C2 integrate for 2ns but the amplifying phase for each of them is 1ns – similar to Op-amp sharing
- Discharging and offset sampling is done during phases d1 and d2

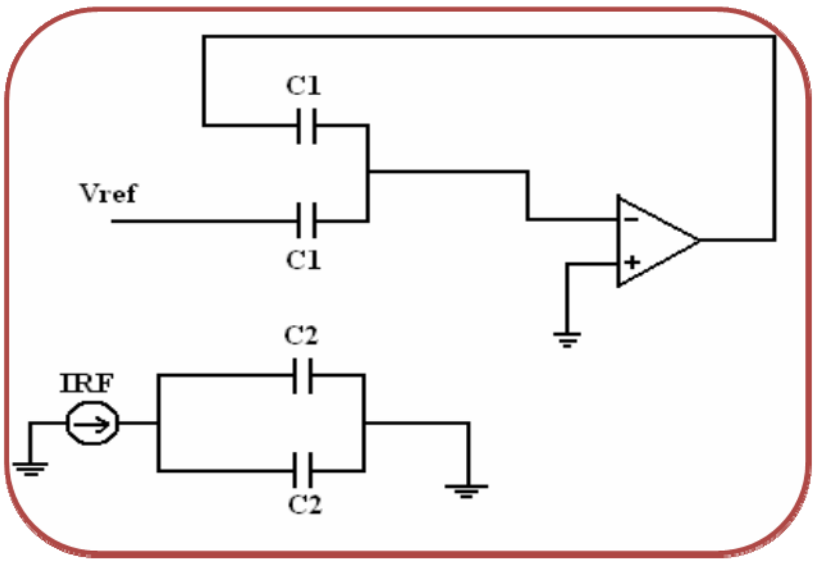
MDAC First Stage – Current Sampling and interleaving



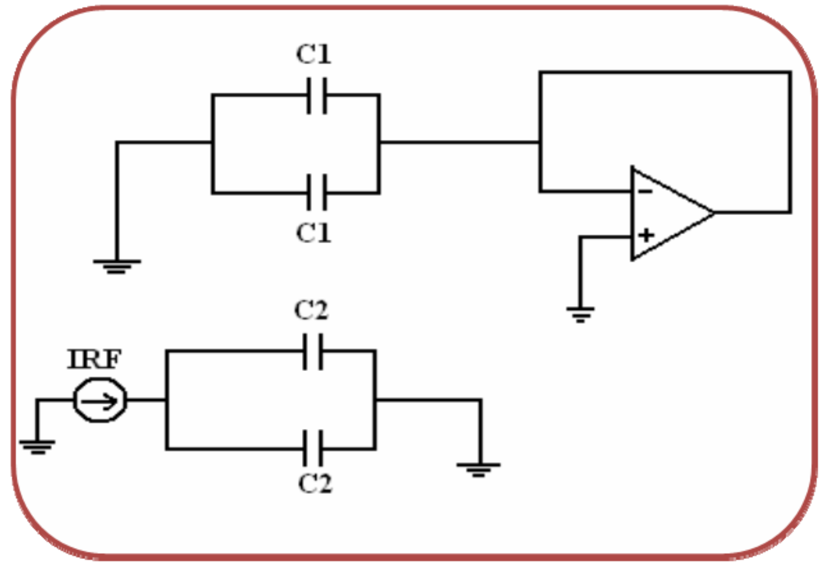
1ns; C1 - Integrating, C2 - Amplifying



1ns; C1 - Integrating, C2 – Discharge + Offset



1ns; C1 - Amplifying, C2 - Integrating



1ns; C1 - Discharge + Offset, C2 - Amplifying

Let’s recap: main features of the frequency domain sampling receiver

- Advantages over time domain sampling
  - Parallelization of the signal processing
  - Each path operates at a much slower rate. ADC design is relaxed as each path only operates on a portion of the signal band.
  - In time-interleaving all ADCs see the entire signal bandwidth. So design of ADC is still a challenge.
  - Sampling speeds that would be a challenge in the conventional time domain circuits, can be achieved using this topology.
  - There is no signal reconstruction in the receiver. Symbol estimation is done directly from the integrated samples by digital post processing.
  - High performance can be achieved by employing LMS calibration in the post- processing to estimate mismatches.
- Advantage of charge sampling over voltage sampling
  - Tracking bandwidth depends on the width of the integration window and not on C. There is no direct limitation on the value of C.
  - A 3db improvement in Jitter performance is seen at high frequencies in charge sampling.

Conclusions

- Frequency-domain ADC solution for broadband digital receivers has multiple advantages.
- New frequency-domain multicarrier receiver has multiple advantages versus OFDM traditional receiver.
- Joint design of RF, analog, digital baseband and mixed-signal background calibration has been introduced.
- Calibration of full systems will minimize overhead in power and area of calibration engine. Can also calibrate more than just the ADC.
- Calibration of RF building blocks should be further explored.

Thanks !!