Design Trends in deep-submicron CMOS with example of GPS-Receiver

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- **In the late 1950s, a new aircraft carrier had 350,000 electronic components, requiring millions of hand-soldered connections – "tyranny of numbers" (Jack Kilby)**

  - **Transforming Nature**
  - **Michael E. Gorman, University of Virginia**

Today…

- Shrinking geometries enable more than 10-Million devices per die.
  - **New problems and issues.**
  - **New Opportunities for innovation**

Deep-Submicron CMOS- Opportunities

- Shrinking geometries → **more transistors.**
- Smaller devices → **Higher ft & faster transistors.**
- More transistors → **Complex digital processing and more digital content.**
- More integration → **The economic drive of lowering the cost of electronics.**

Deep-Submicron CMOS - Issues

- Smaller geometry → Lower supply voltage.
- Smaller devices → More 1/f noise.
- Smaller devices → More leakage.
- Higher digital gate density → Larger portion of silicon is taken by analog circuits (Need to shrink, to gain economic edge).
- More integration → Isolation issues between various sub-modules of the system.

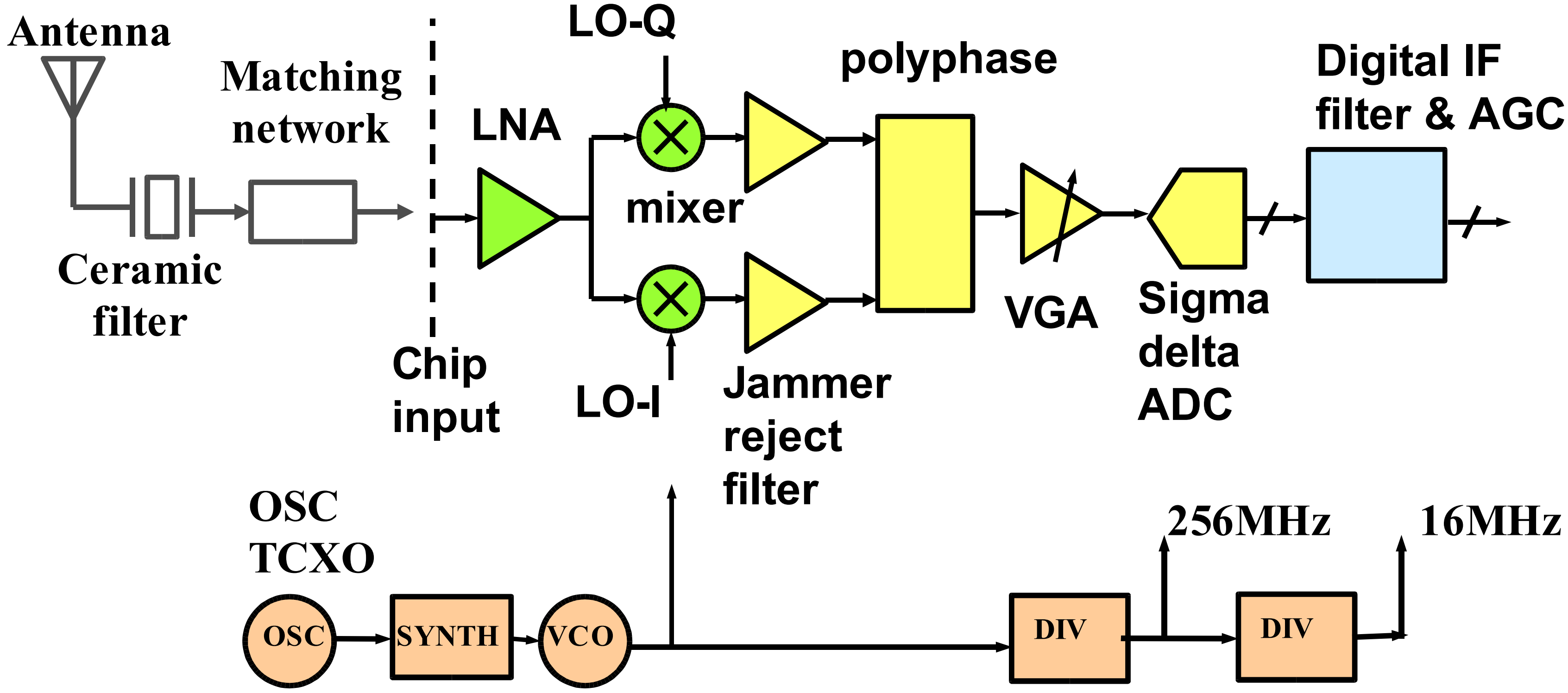
System-on-chip - Examples

- **Network processors**
- **Graphics Processors**
- **Bluetooth transceivers**
- **WLAN transceivers**
- **GPS receivers**
- **GSM transceivers**

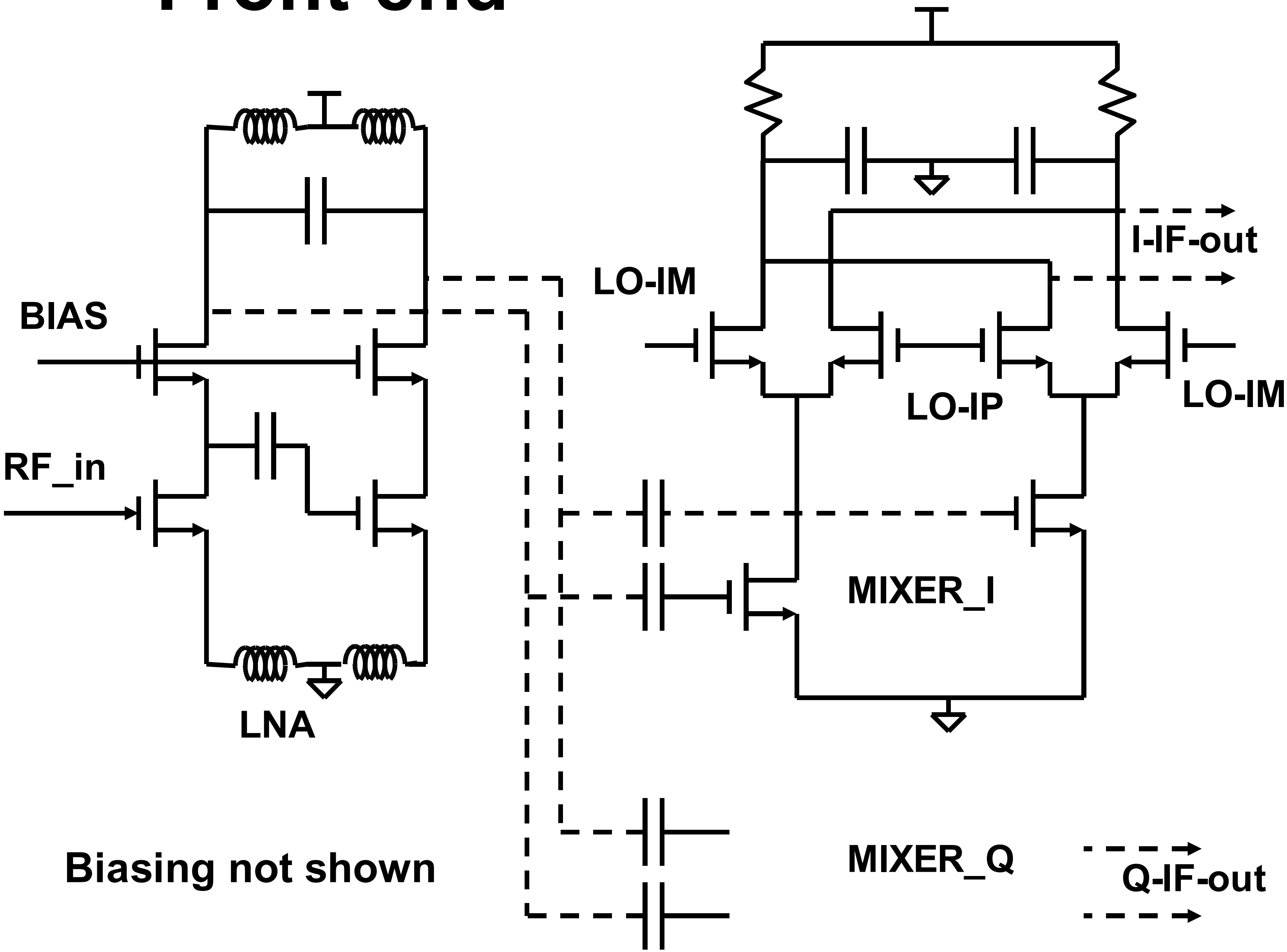
System design – Changing paradigms

- What works in regular system design may-not work for SoC.
- The building blocks available are slightly different –
  - **Eg: Transmission lines & stubs are not available easily on an IC.**
  - **Using SAW filters is an expensive option, mainly due to off-chip interface, pins & board space.**

GPS Receiver architecture



Front-end

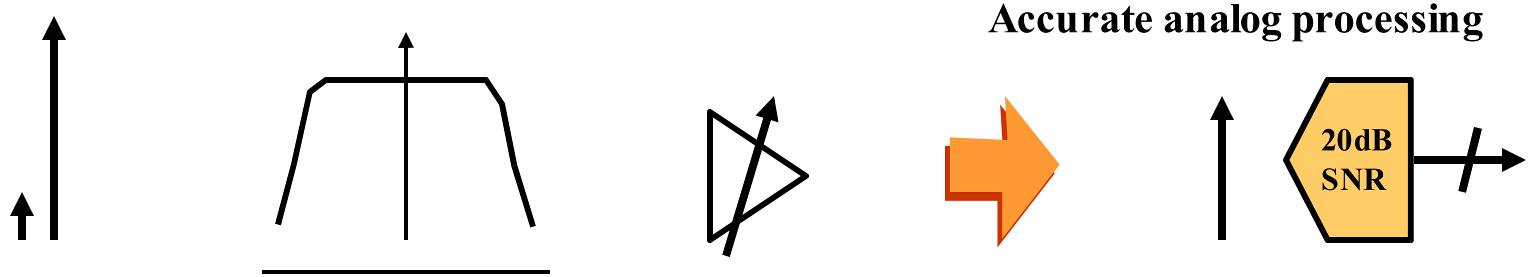


Biasing not shown

IF chain signal processing

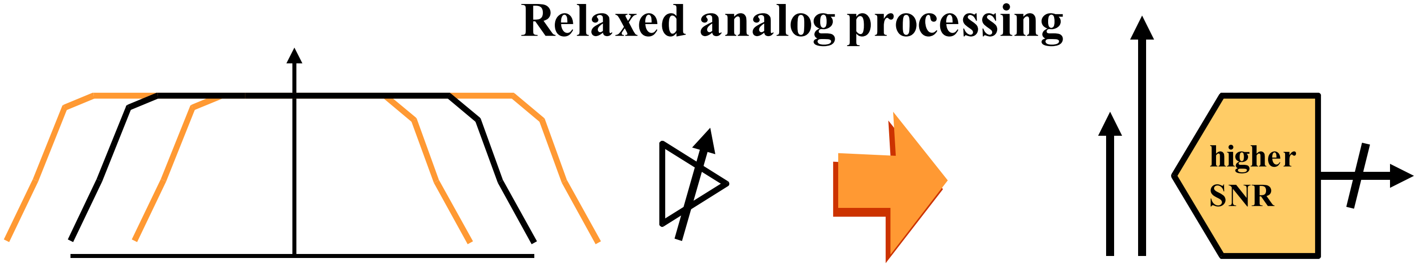
- **Deep-submicron process not suitable for accurate analog filtering**

Accurate analog processing



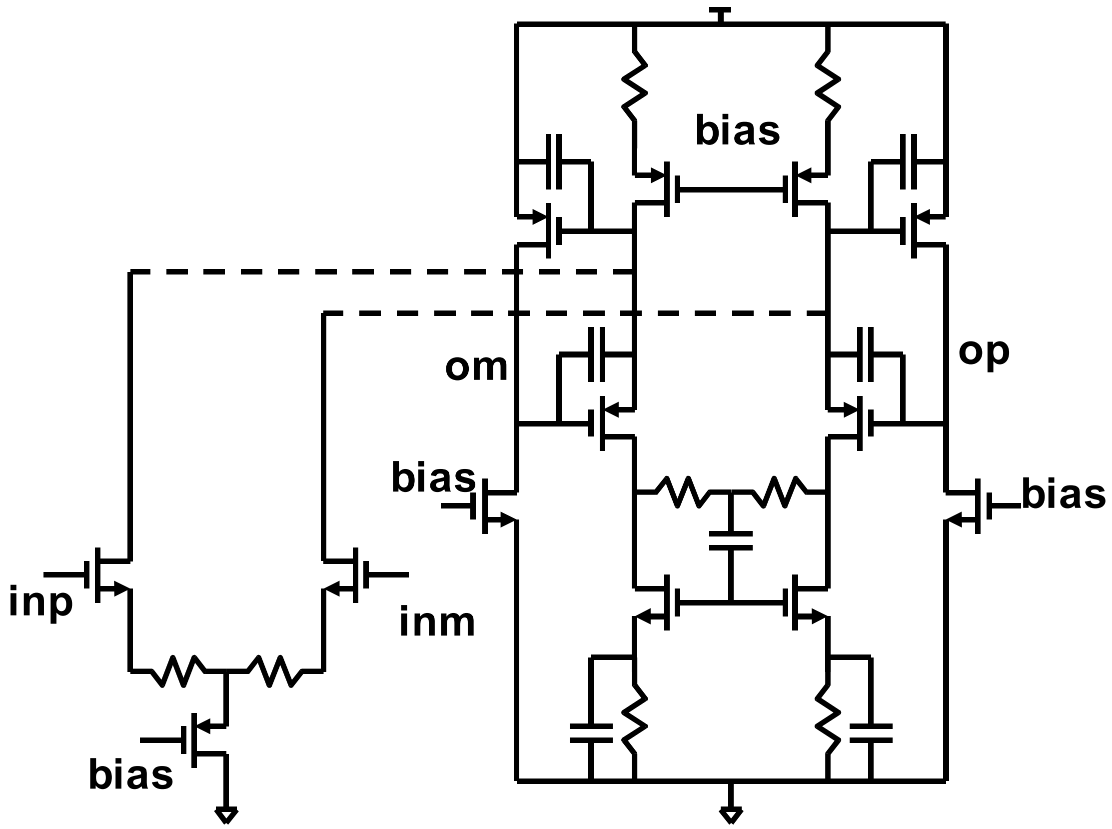
Variable signal Level at IF input | Accurate filter | fine gain step | Fixed power level

Relaxed analog processing

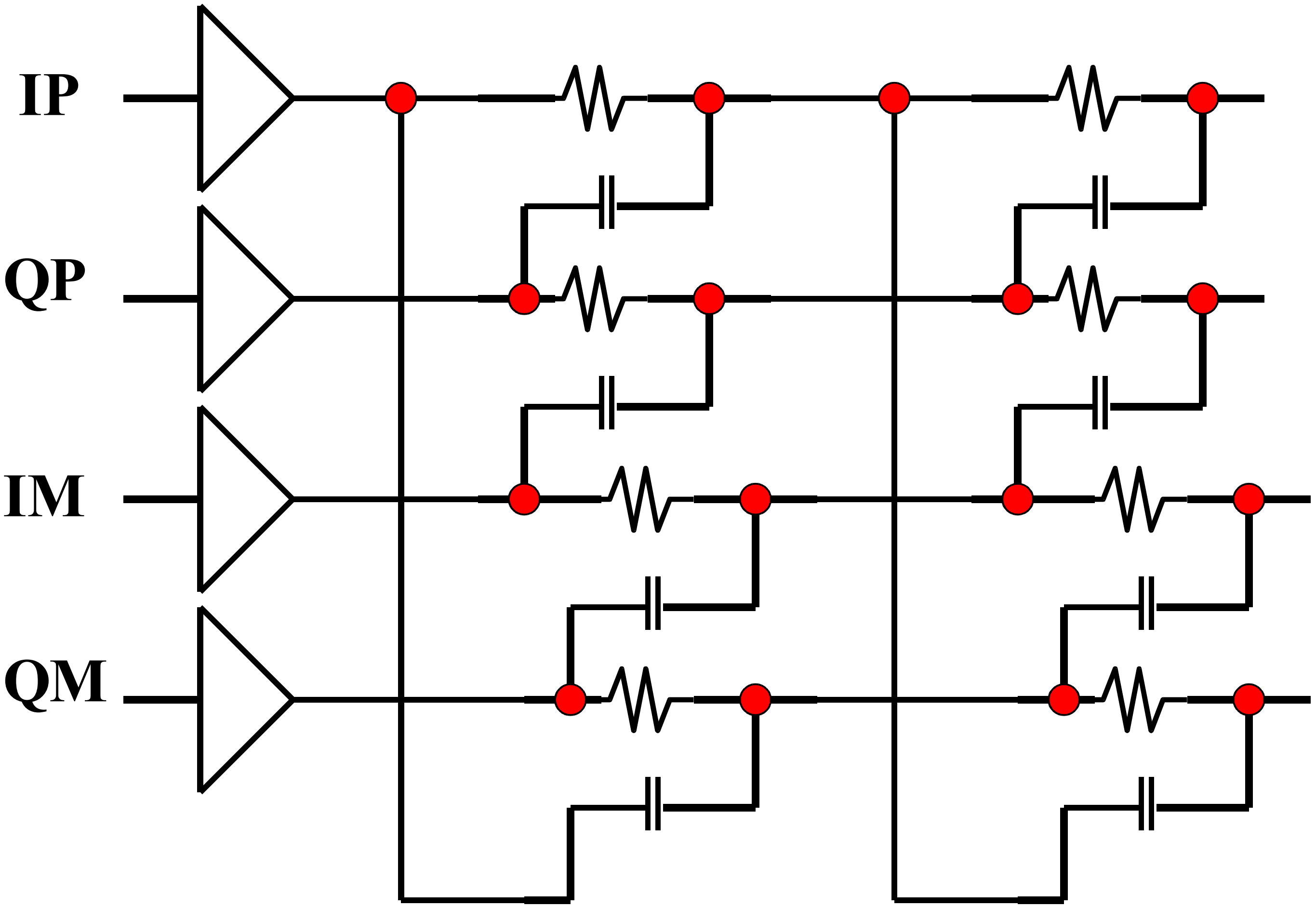


Variable signal Level at IF input | wider filter | coarse or no gain step | Excess noise and variable power level

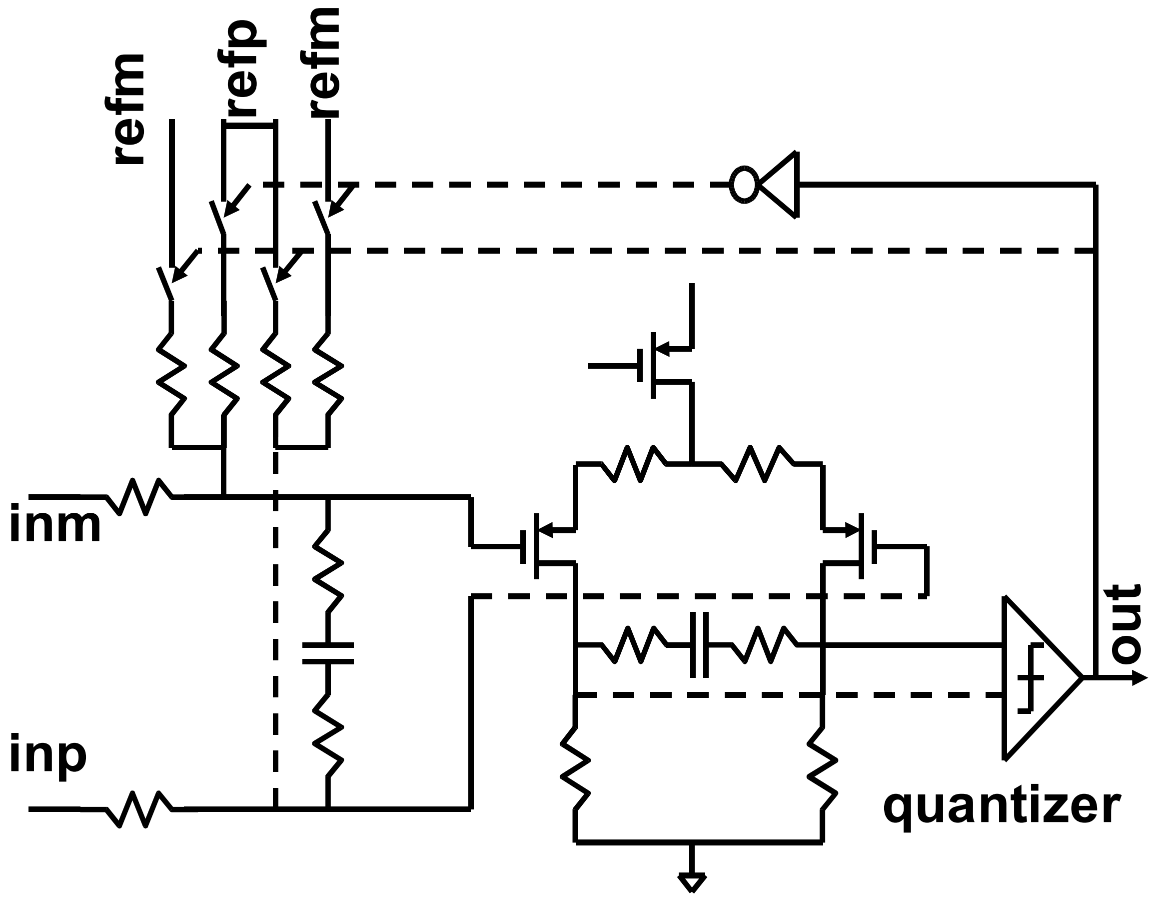
Jammer reject filter



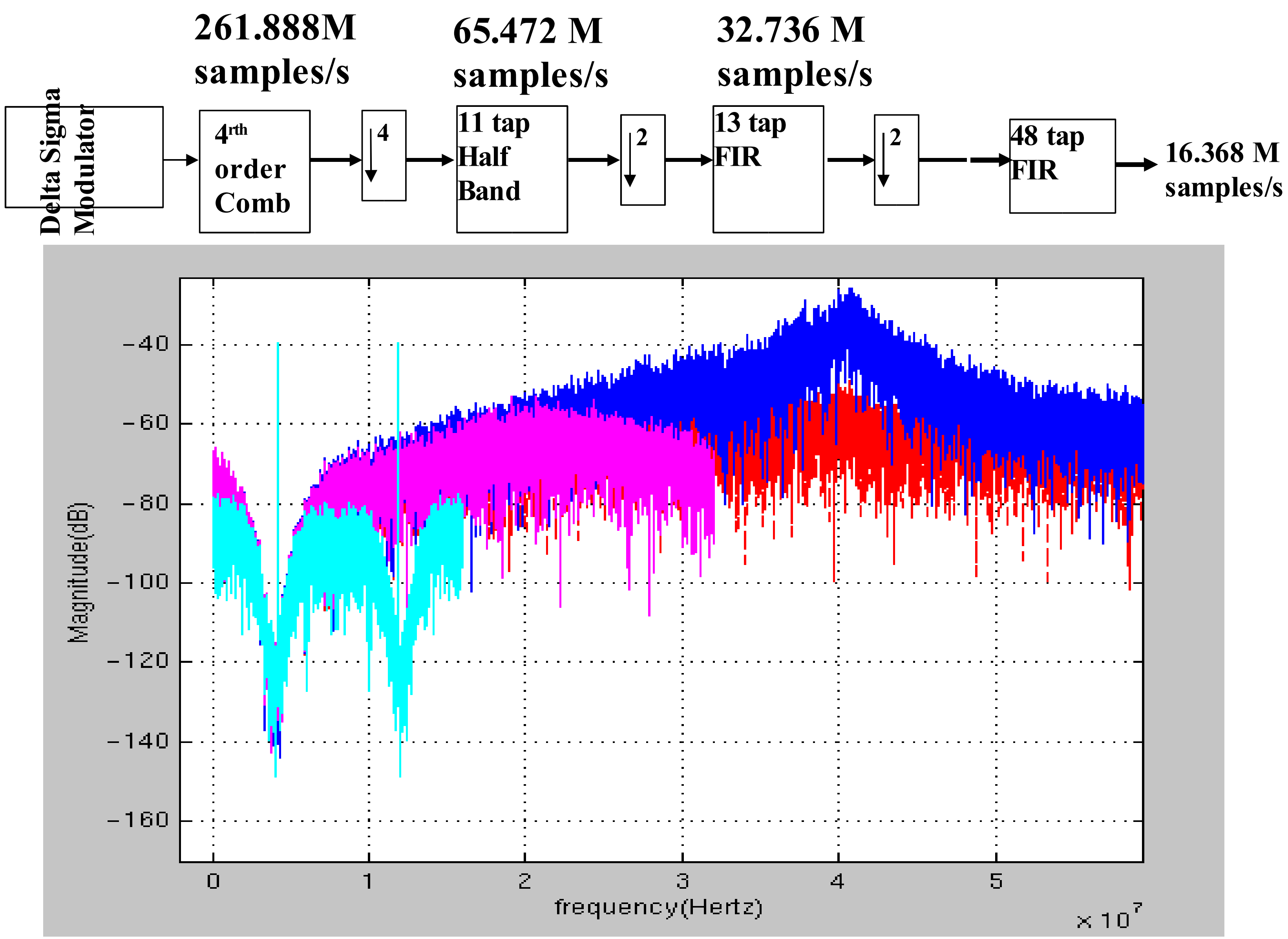
PolyPhase Filter



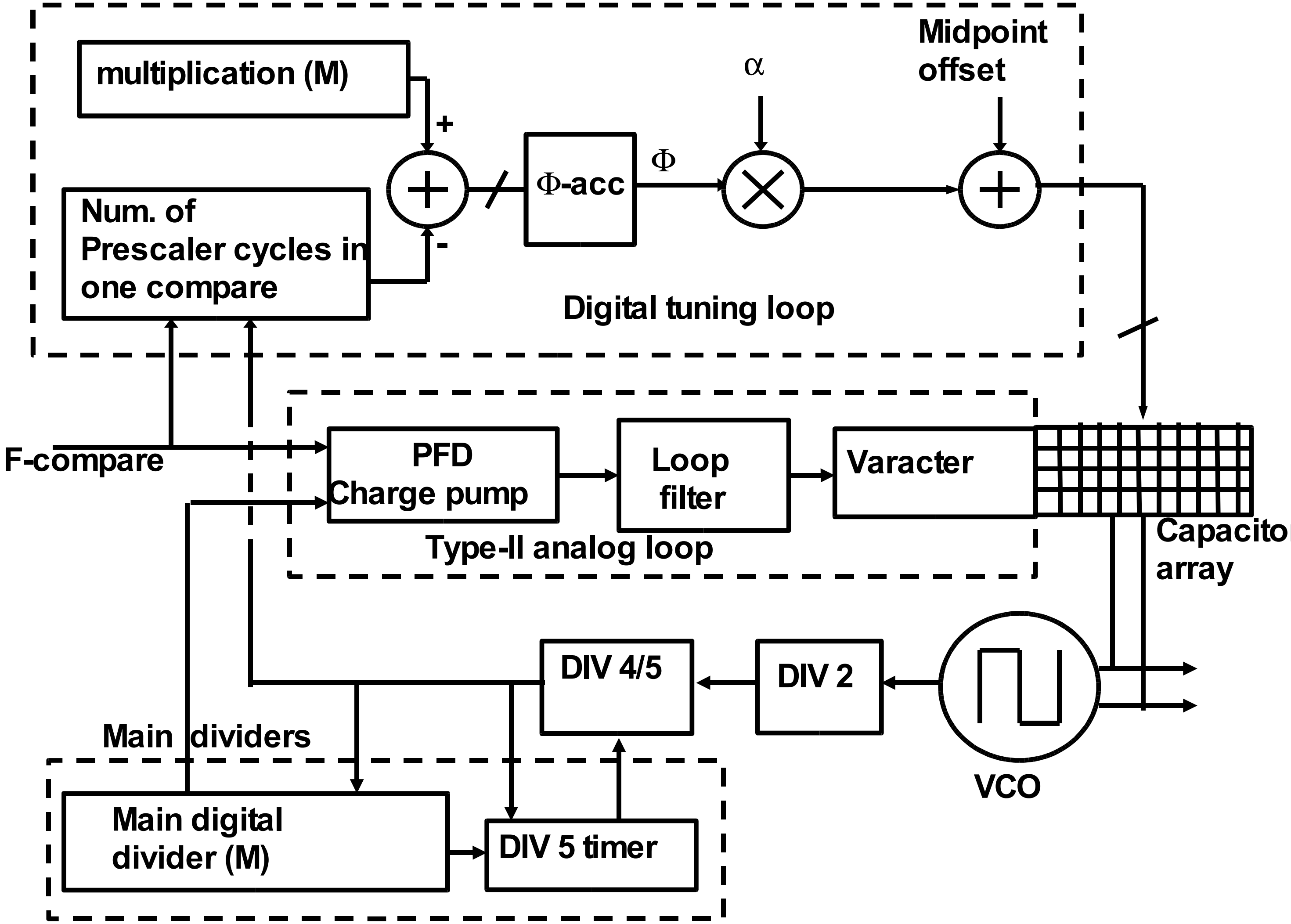
Passive continuous time delta-sigma ADC



Digital filter architecture

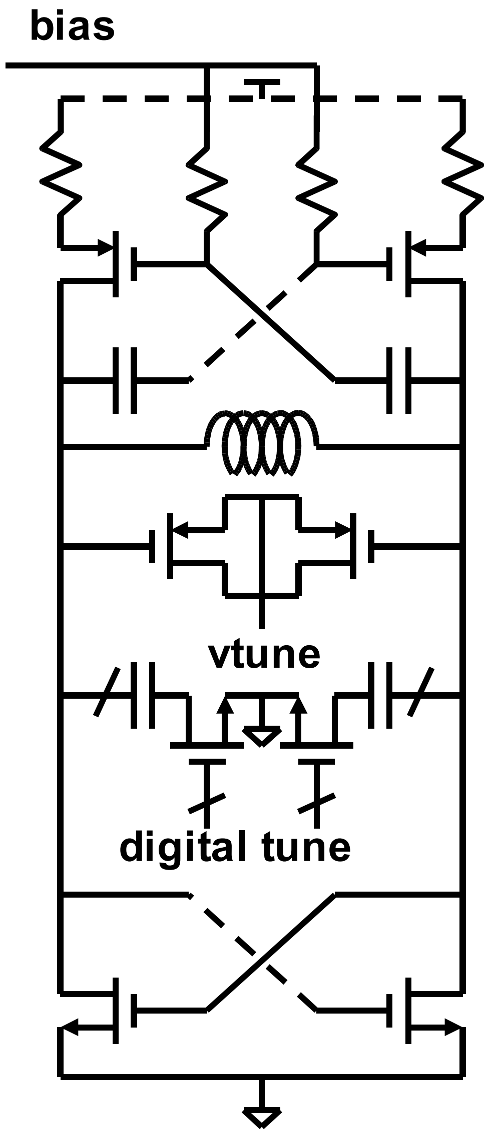


Synthesizer architecture



- Type-II analog integer-N PLL
- Type-I digital tuning loop for PVT calibration of VCO Freq.

VCO

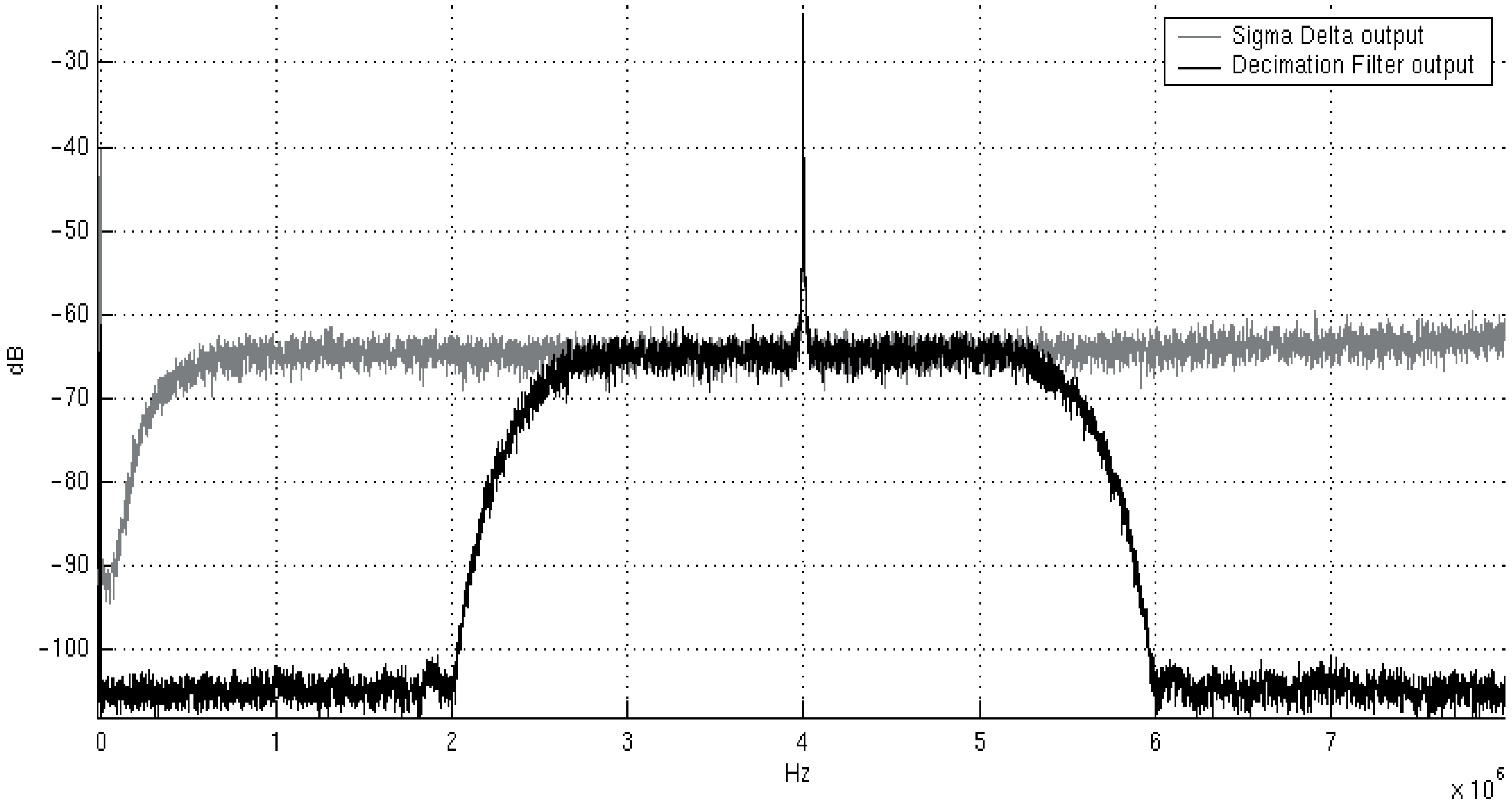


- LC tank with metal-spiral and MOS varactor
- Switched capacitor (MIM) array to augment the tuning range
- Cross-coupled MOS gain stage for negative resistance
- Self-tracking bias to minimize supply pull on VCO frequency

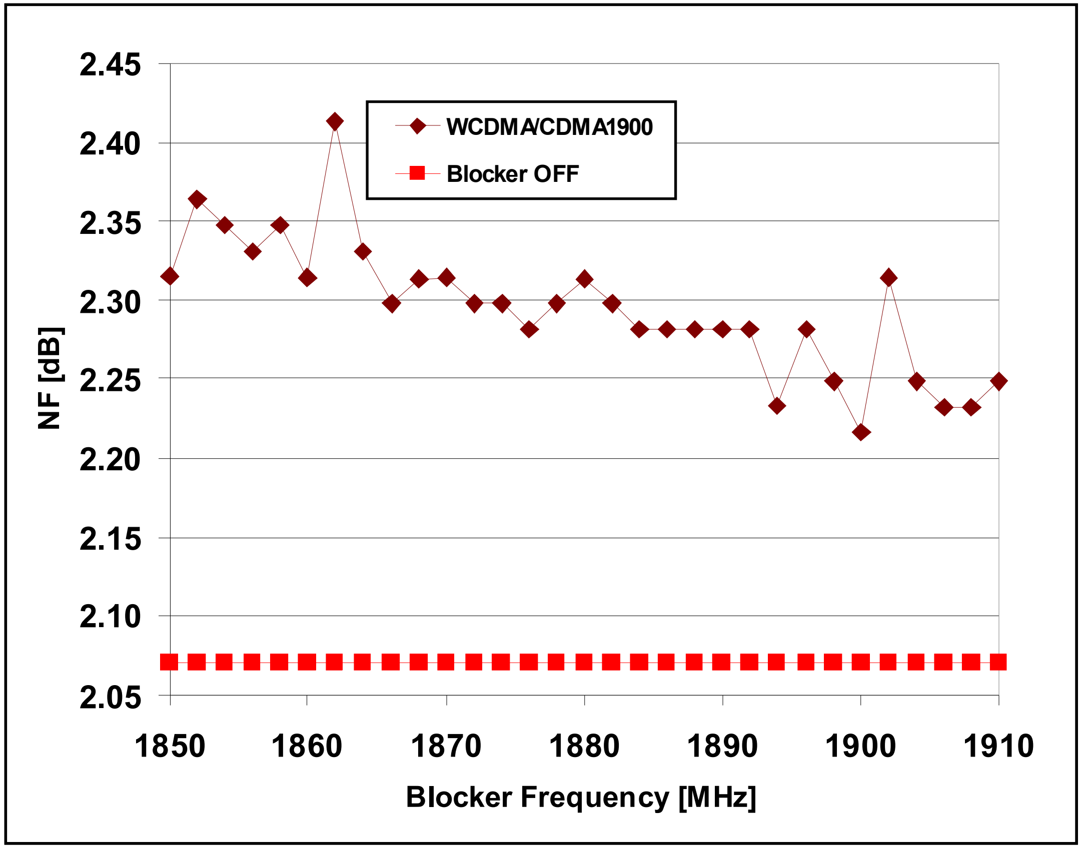
Challenges

- Low Supply Voltage (1.4 volts).
- SoC integration of RF + Base-band.
- Achieve high-linearity of RF front-end.
- Choice of pin-out to minimize package coupling.
- Floor-plan to minimize influence of digital noise on RF circuits.
- Isolation of supplies and grounds (power supply coupling).
- IR drop analysis and isolation of high-activity regions.
- Minimize power-supply spikes and use de-coupling capacitors to provide switching current.
- Judicious use of guard rings to isolate noise.

Receiver response

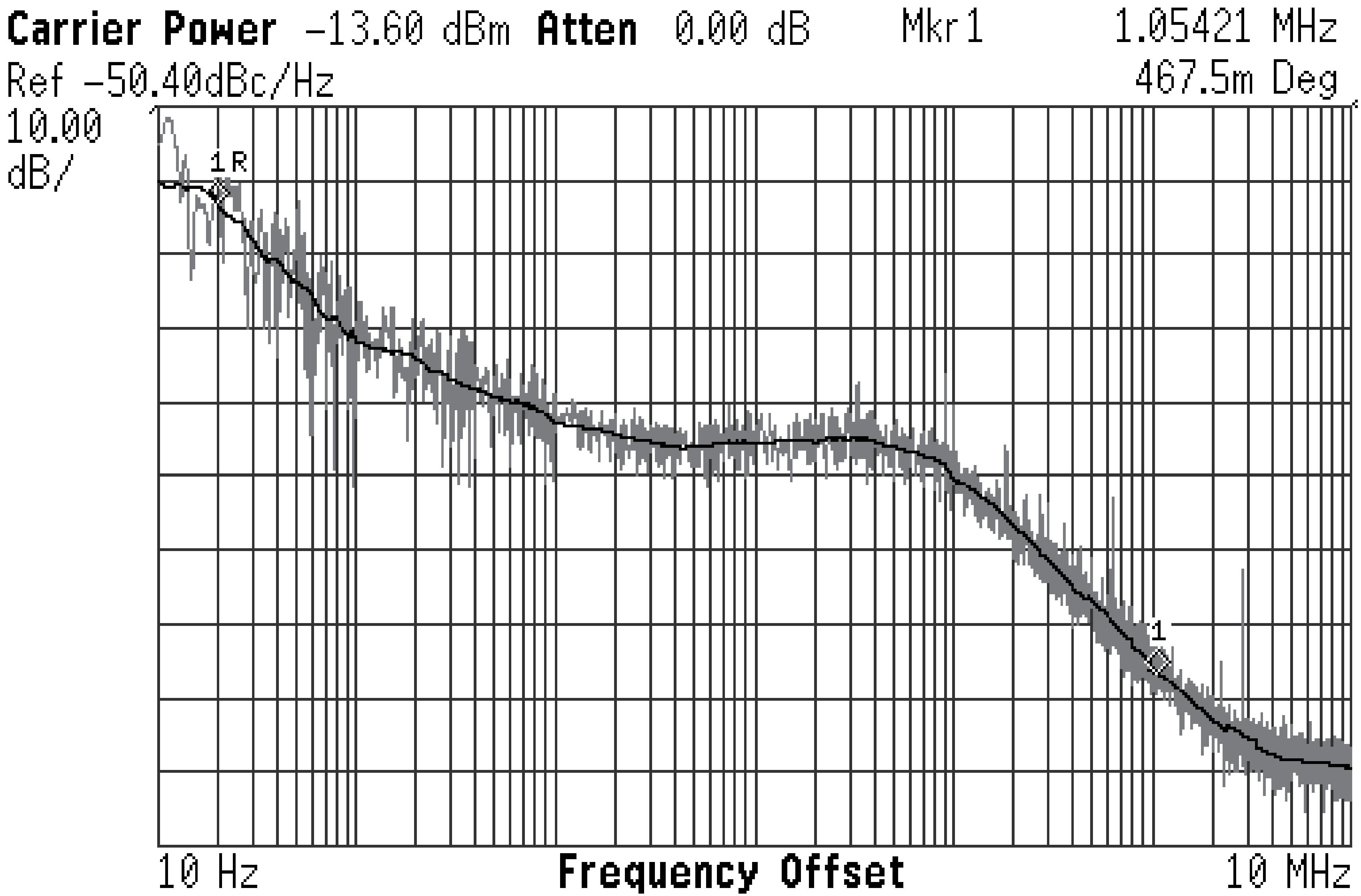


De-sense with out-of-band jammers



- Noise figure without any jammer is 2.05 dB
- With -31dBm jammer at 1850MHz the Noise figure goes up to 2.3 dB
- With stronger LO drive (elevated supply) the desense is < 0.1dB

Phase noise at LO/4



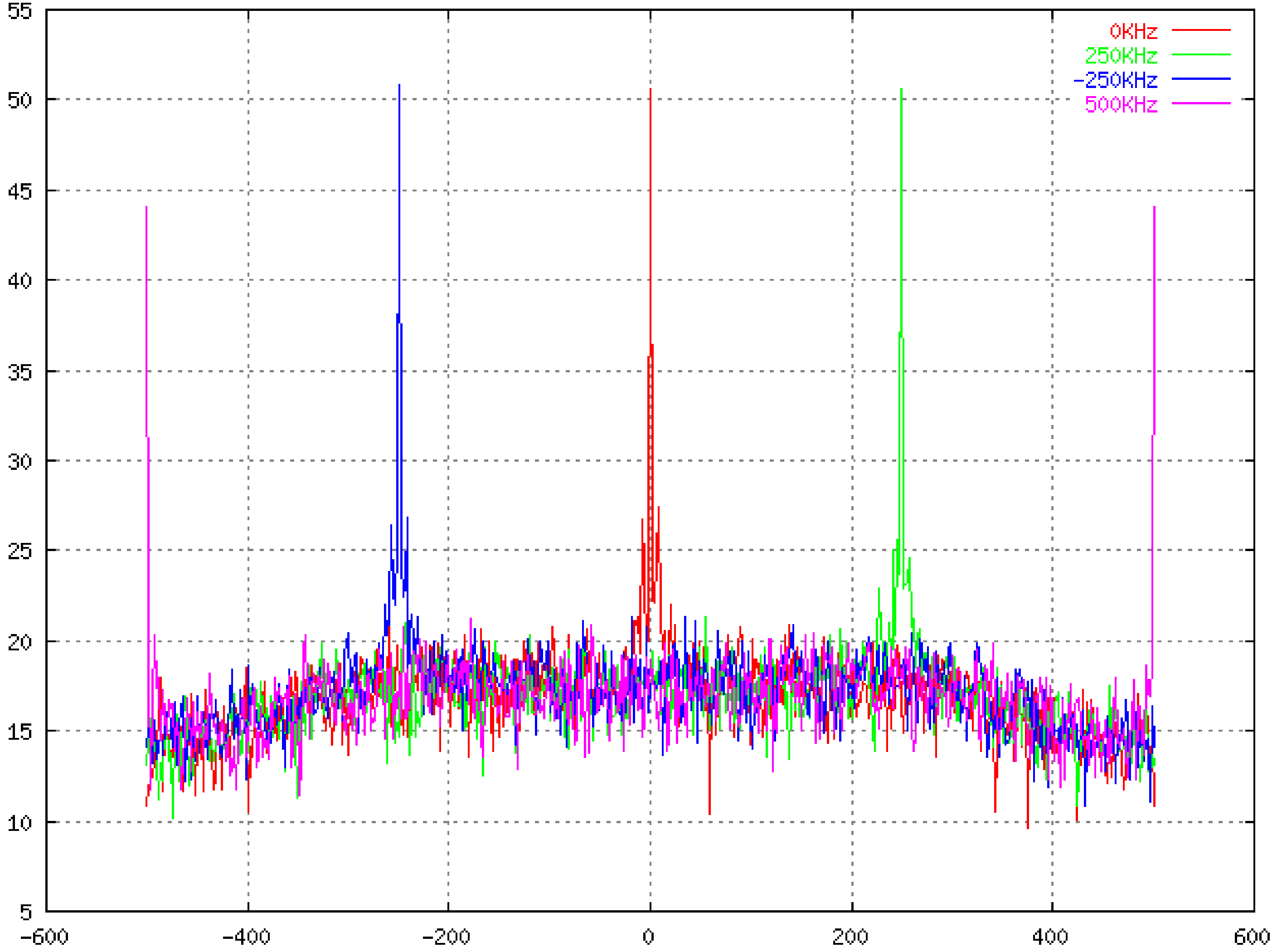
Measured Performance

LNA + IRM	
Gain	38 dB
Noise Figure	1.8 dB
S11	-11 dB
IIP3 (@ 1576MHz and 1576.5MHz)	5dBm
PCS band jammer desense	0.1dB
ADC	
Dynamic Range	38dB

Performance Continued…

SYNTHESIZER	
Phase noise at 100KHz	-88dBc/Hz
Phase noise at 1MHz	-113dBc/Hz
Integrated rms Phase error	2 deg
Lock Time	100ms
Reference Spur	-60dBc
FULL RECEIVER	
Die Area	12.8 mm^2
Image rejection	18dB
Power	60mA @ 1.4V

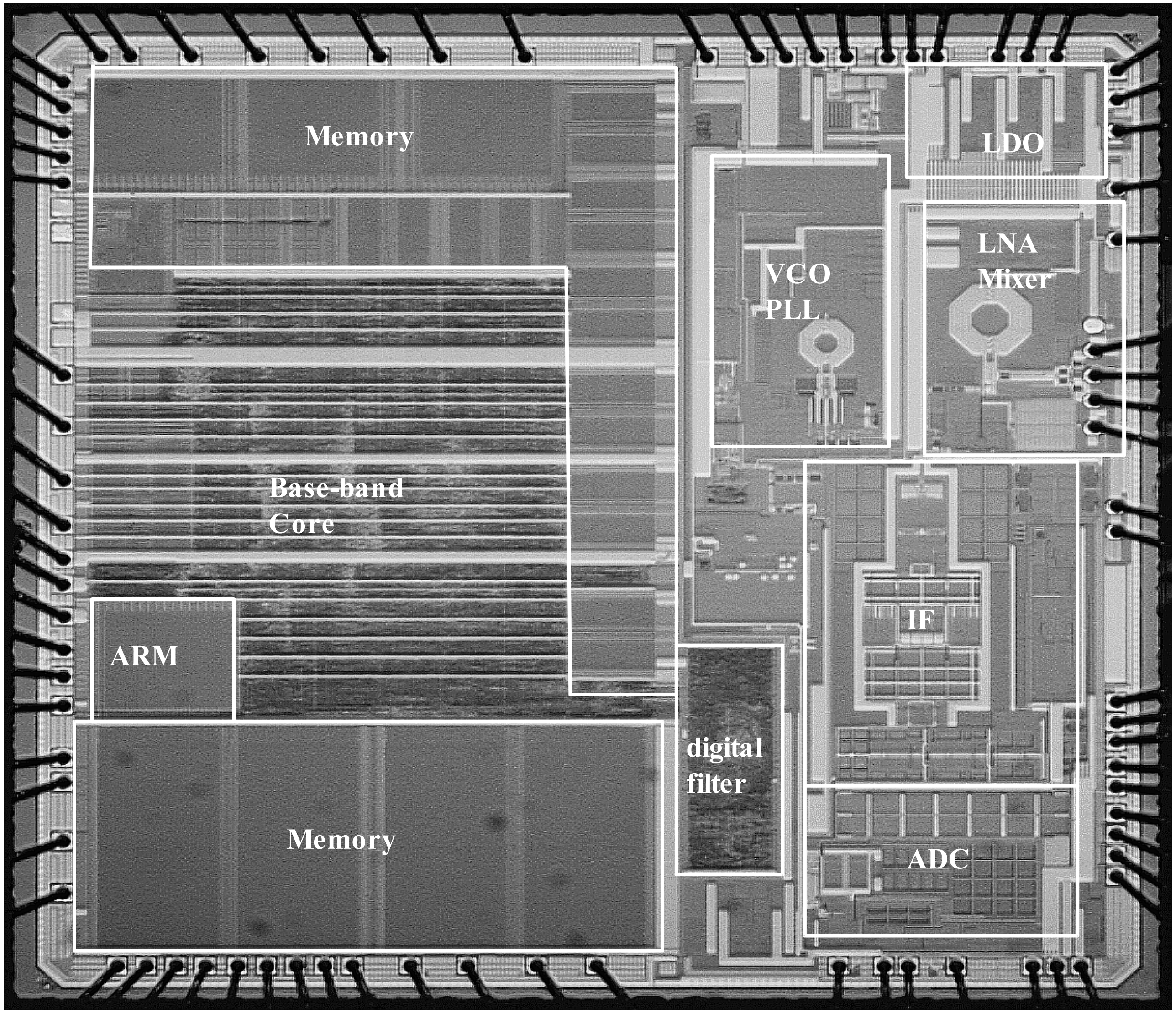
Single-Tone Response of Receiver



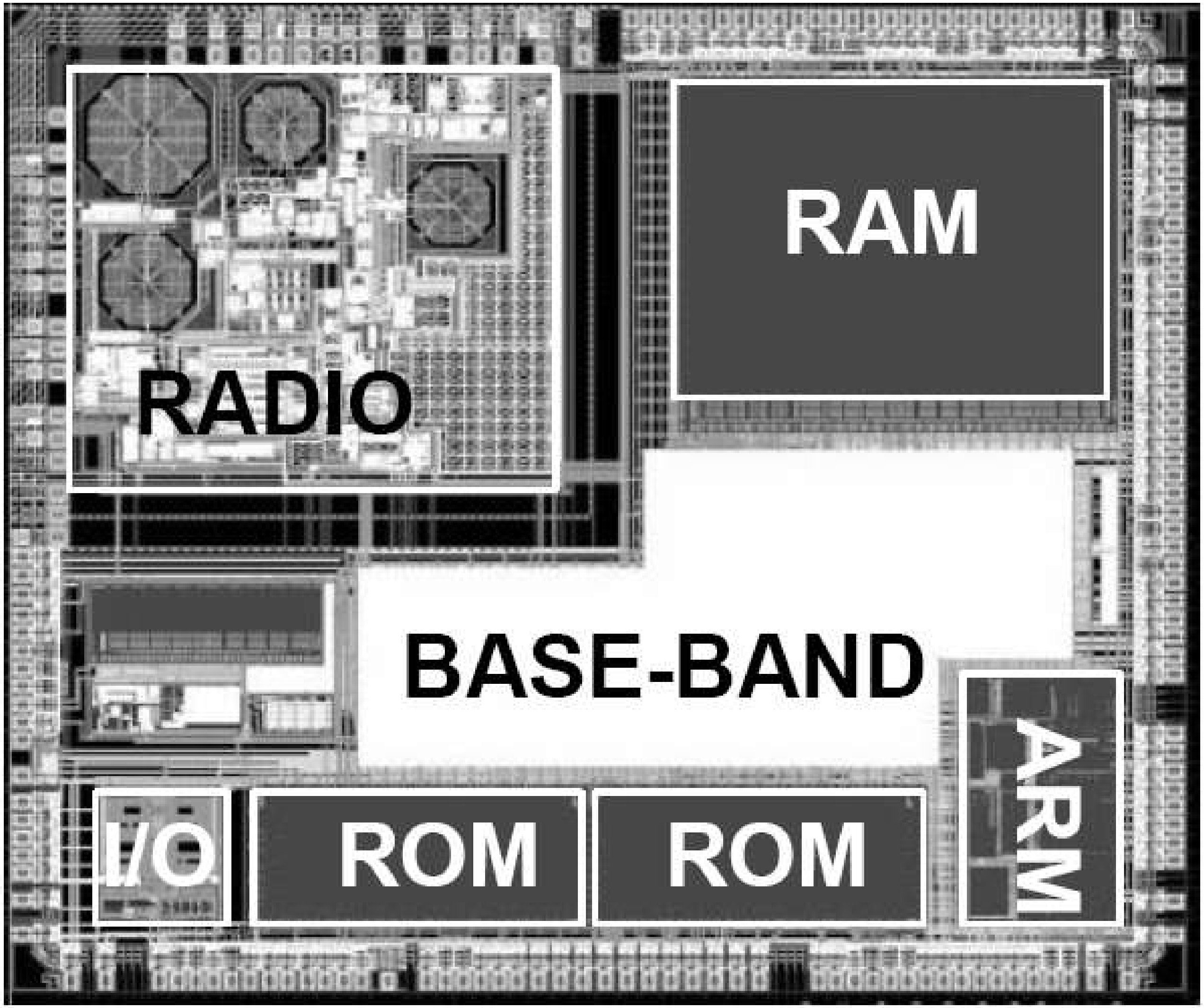
Spot Noise-Figure of Receiver

Baseband freq.(kHz)	-500	-250	0	250	500
NF (dB) at Baseband	8.43	2.49	2.59	2.63	8.87
NF at ADC output (dB)	2.26	3.06	3.54	3.68	2.82
Front-end NF (dB)	1.51	1.51	1.51	1.51	1.51

- NF at ADC output is degraded due to high speed digital output
- NF from base-band is better as digital test buffers are off
- NF within the narrow bandwidth of base-band filter is good
- Indicates substrate coupling does not degrade the RF performance

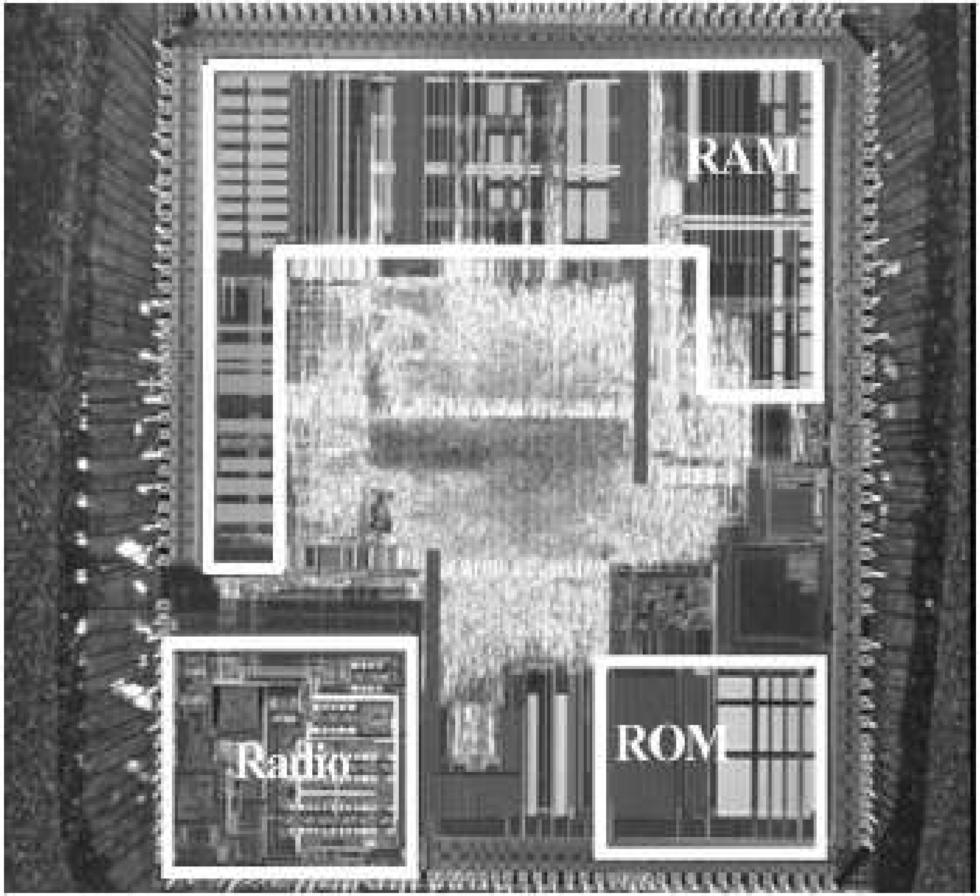


GPS Receiver – Texas Instruments
13 mm^2 – 0.09 µM CMOS (2005)



Single-chip GPS receiver **ST-Microelectronics**

23 mm² – 0.18 µM CMOS (2004)



Single-chip GPS Receiver - Sony Corporation

40 mm² - 0.18 µM CMOS (2004)

Conclusion

- It is possible to get high-performance SoC for complex functions.
- Effective isolation methods are necessary before such SoC products can be widely used.
- Shifting analog gain and processing into digital domain is still necessary for SoCs.
- Regular 90nm CMOS process can still be used, provided design innovations address the shortcomings.

Open Problems

- **Power dissipation** and power-density is high.
- **Thermal issues** – too much heat generation.
- **Isolation issues** – Getting enough isolation is still a black-magic art. Modeling & design methods need to improve, so that it can be routinely achieved.
- **New architectures** that use wider bandwidth (faster transistors, but lower capacitance and area are needed).
- **Driving interfaces takes power** – be it air-interface or off-chip interfaces. RF power amplification needs to be effectively addressed.

References

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References

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