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Seminar

Highly-Interleaved 5b 250MS/s ADC with Redundant Channels in 65nm CMOS

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Wednesday, February 20, 2008
6:30pm: Pizza & Drinks; 7:00pm: Presentation

Dallas Texins Activities Center, Conf Room 1
(North end of Texas Instruments expressway site,
13900 N Central Expwy.; site entrance on north-bound access road, between Midpark Rd. & Spring Valley Rd.)

Abstract:

A 36-channel interleaved 5b ADC demonstrates the use of parallelism in mixed-signal circuits to reduce the core supply voltage to 800mV and to improve energy efficiency. At 250MS/s, the total ADC power is 1.20mW, and the ENOB is 4.42 at the Nyquist rate. Six redundant channels counter yield loss from local variations in 65nm CMOS, and the yield of chips meeting the specification increases from 42% to 88%.