

2003 ISSCC SHORT COURSE ON SOC DESIGN

Current Trends in Analog Design for SoCs

John W. Fattaruso

Texas Instruments

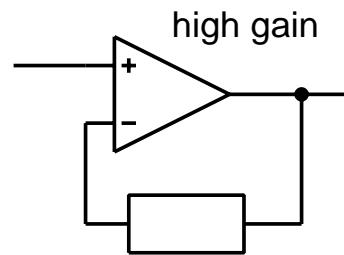
johnf@ti.com

OUTLINE

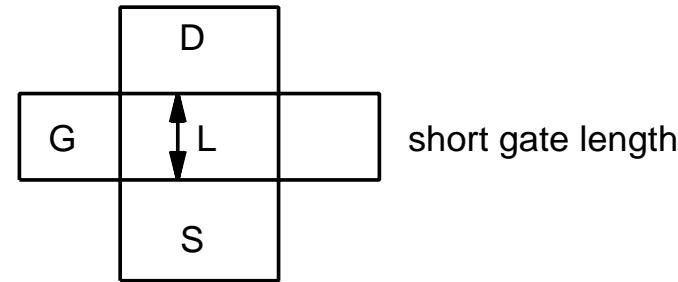
- Introduction
- Low supply voltage constraints
- Low power constraints
- Common substrate constraints
- Interconnect constraints

ANALOG PROCESSING REQUIREMENTS

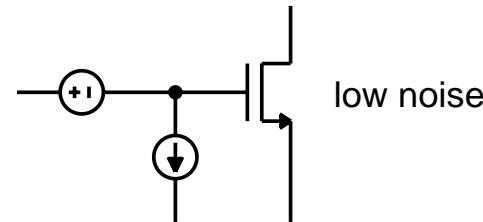
High SFDR requires:



High speed requires:

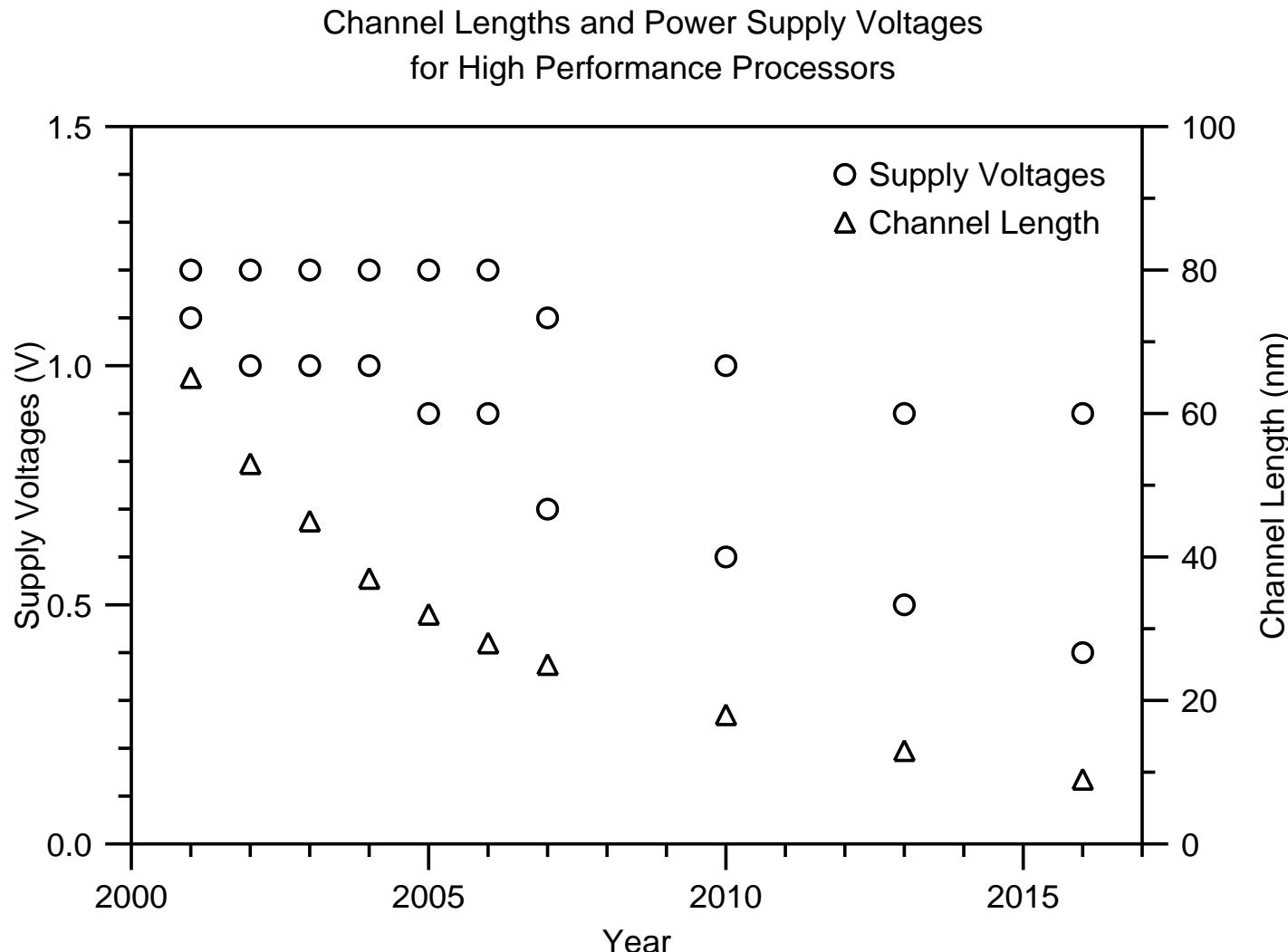


High SNR requires:

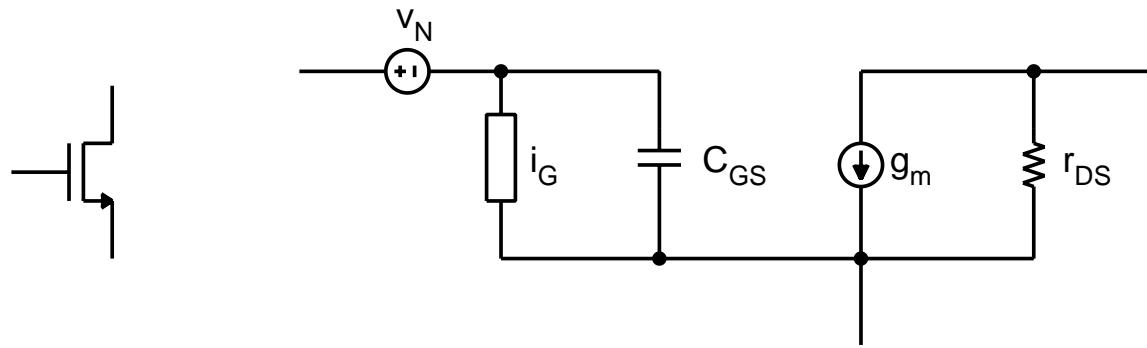


DOWNTWARD TREND IN SUPPLY VOLTAGES

Source: 2001 International Technology Roadmap for Semiconductors



ANALOG PERFORMANCE OF SCALED MOSFETS



$$f_T = g_m / 2\pi C_{GS}$$

$$A_V = g_m r_{DS}$$

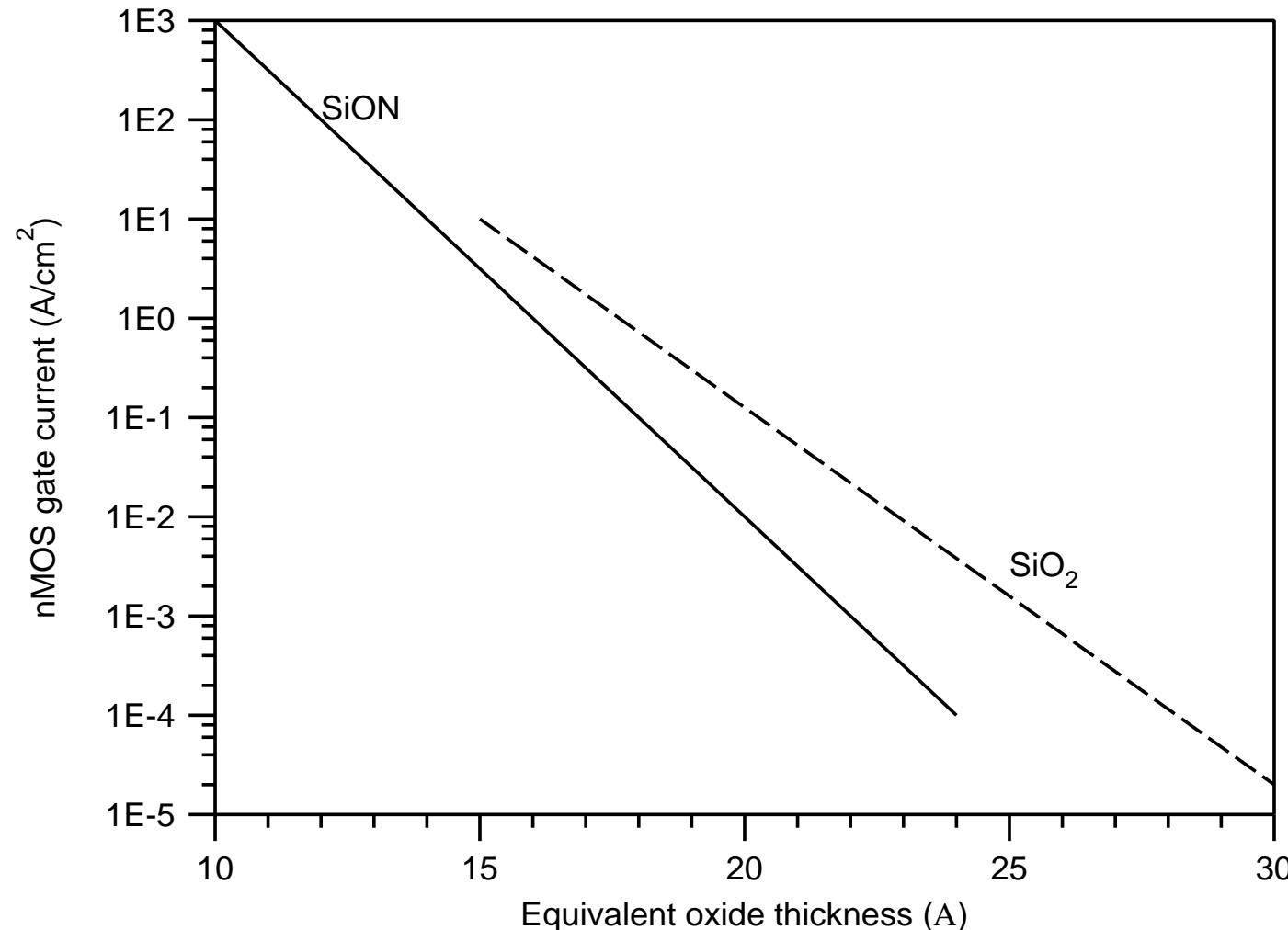
$$V_N^2 = \gamma 4kT \Delta f / g_m$$

long channel: $\gamma=2/3$

short channel: $2 < \gamma < 8$

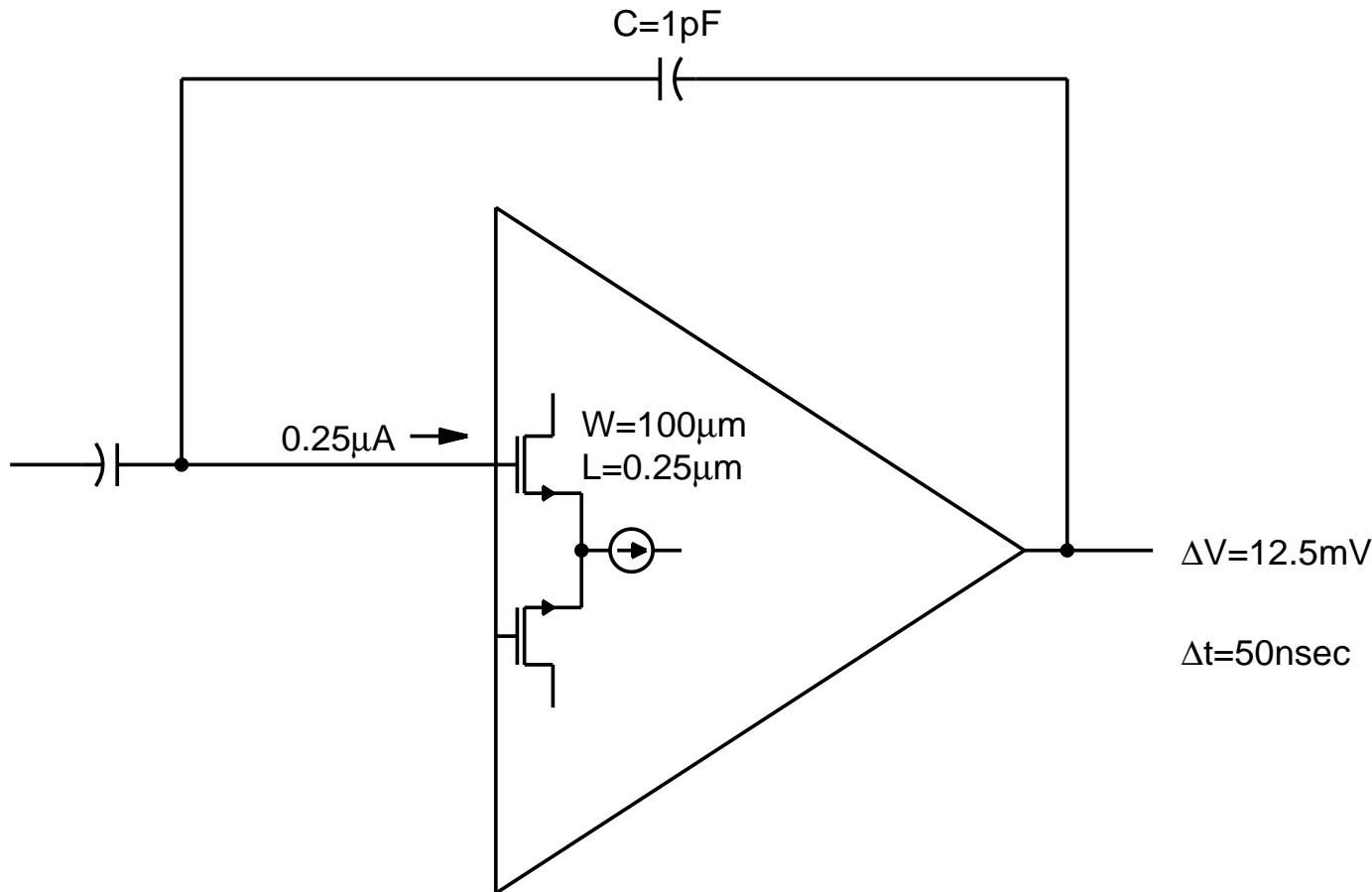
MEASURED GATE CURRENT OF SCALED MOSFETS

D. Buss (TI) Invited for upcoming TED



GATE CURRENT DISTURBANCE OF INTEGRATOR STAGE

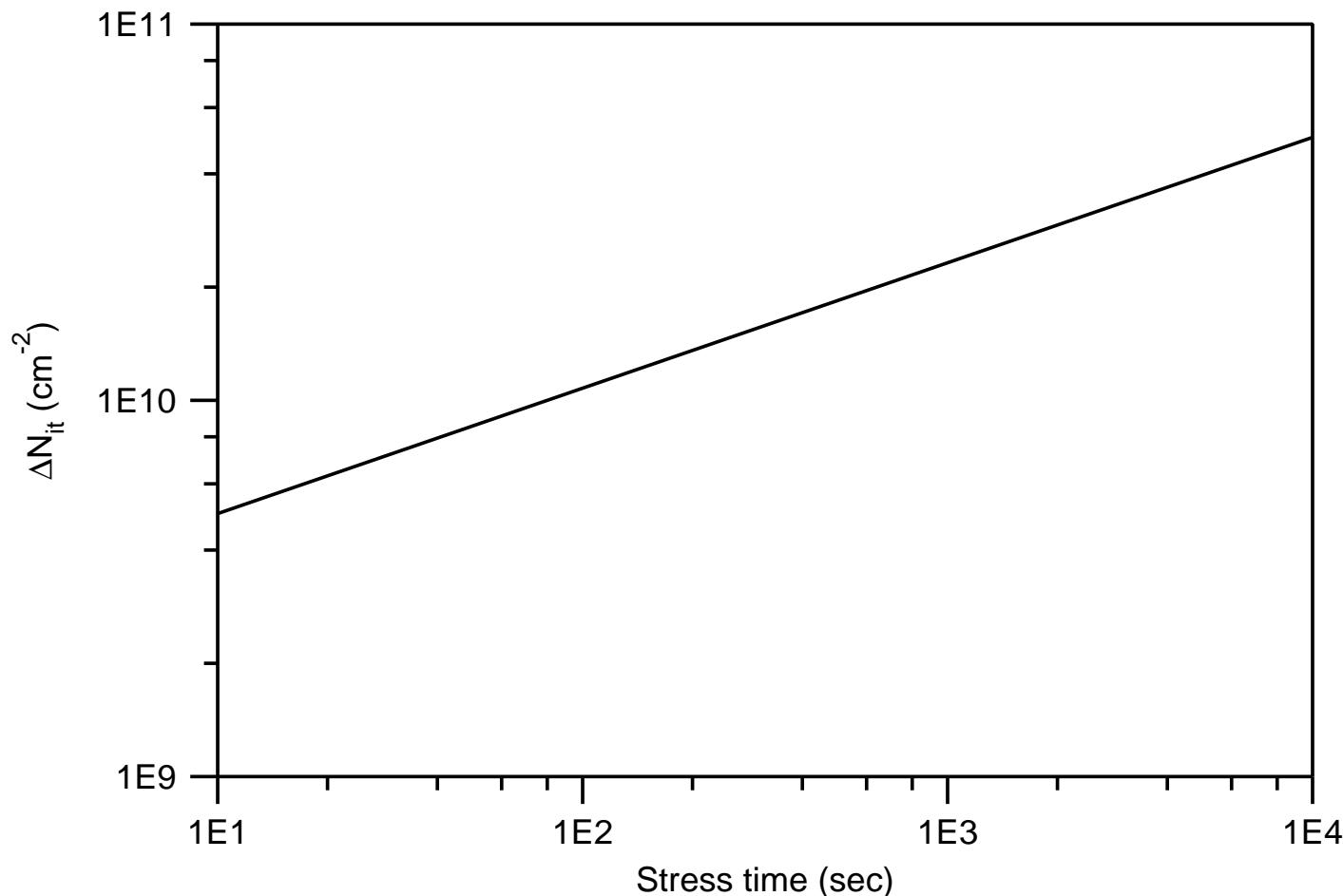
$f_{CLOCK}=10\text{MHz}$ $I_G=1\text{A/cm}^2$



MEASURED NBTI OF SCALED MOSFETS

V. Reddy (TI)

$V_G = -2.8V$ $T = 105^\circ C$



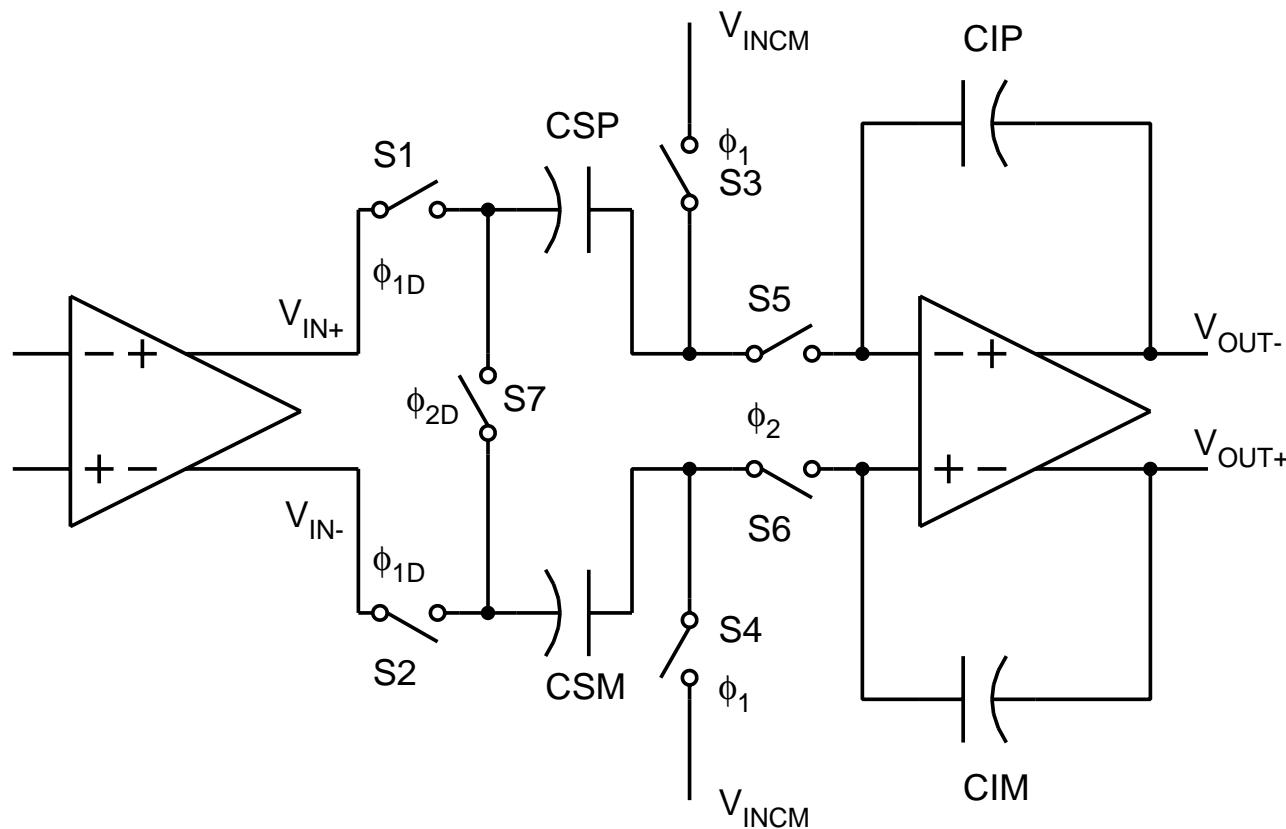
OUTLINE

- Introduction
- **Low supply voltage constraints**
- Low power constraints
- Common substrate constraints
- Interconnect constraints

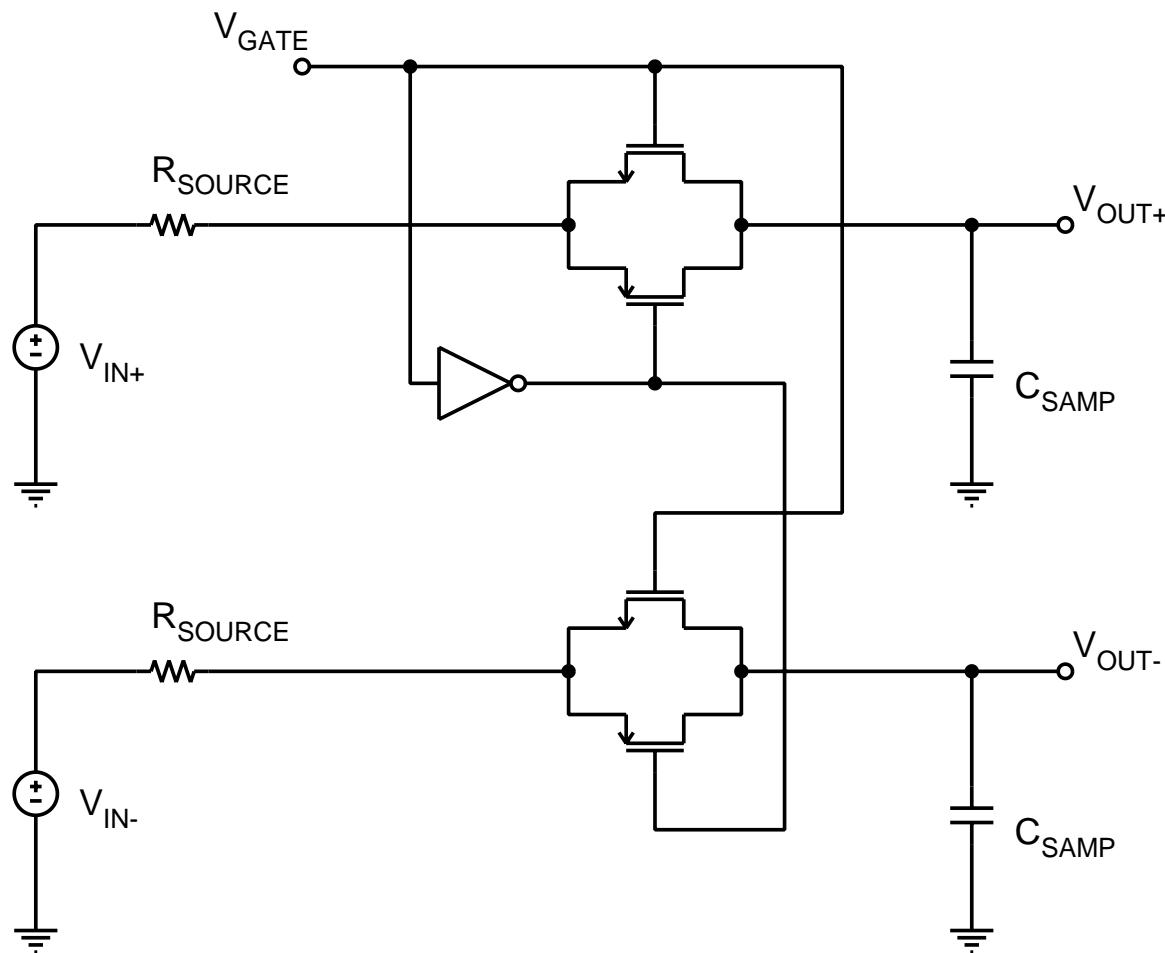
CONSTRAINTS OF DYNAMIC RANGE AT LOW SUPPLY VOLTAGES

- For device noise limitations, as $V_{DD} \downarrow$, $\bar{V}_{signal}^2 \downarrow$, so to maintain SNR, \bar{V}_{noise}^2 must \downarrow , so g_m must \uparrow , so I_{DD} must \uparrow (generally more than $V_{DD} \downarrow$) and $P_{DD} \uparrow$
- For kT/C noise limitations, as $V_{DD} \downarrow$, $\bar{V}_{signal}^2 \downarrow$, so to maintain SNR, \bar{V}_{noise}^2 must \downarrow , so C_{sample} must \uparrow , so $P_{DD} \uparrow$
- High precision costs lots of power at low supply voltages
- Applications of low voltage opamps probably will be in medium precision preamps, buffers, oversampled or pipeline data converters and filters in mixed-signal systems where integration with DSPs or μ Ps makes sense, or where the same supplies must be used across a board.
- Other applications of low voltage opamps are in battery operated systems, such as portable wireless devices.

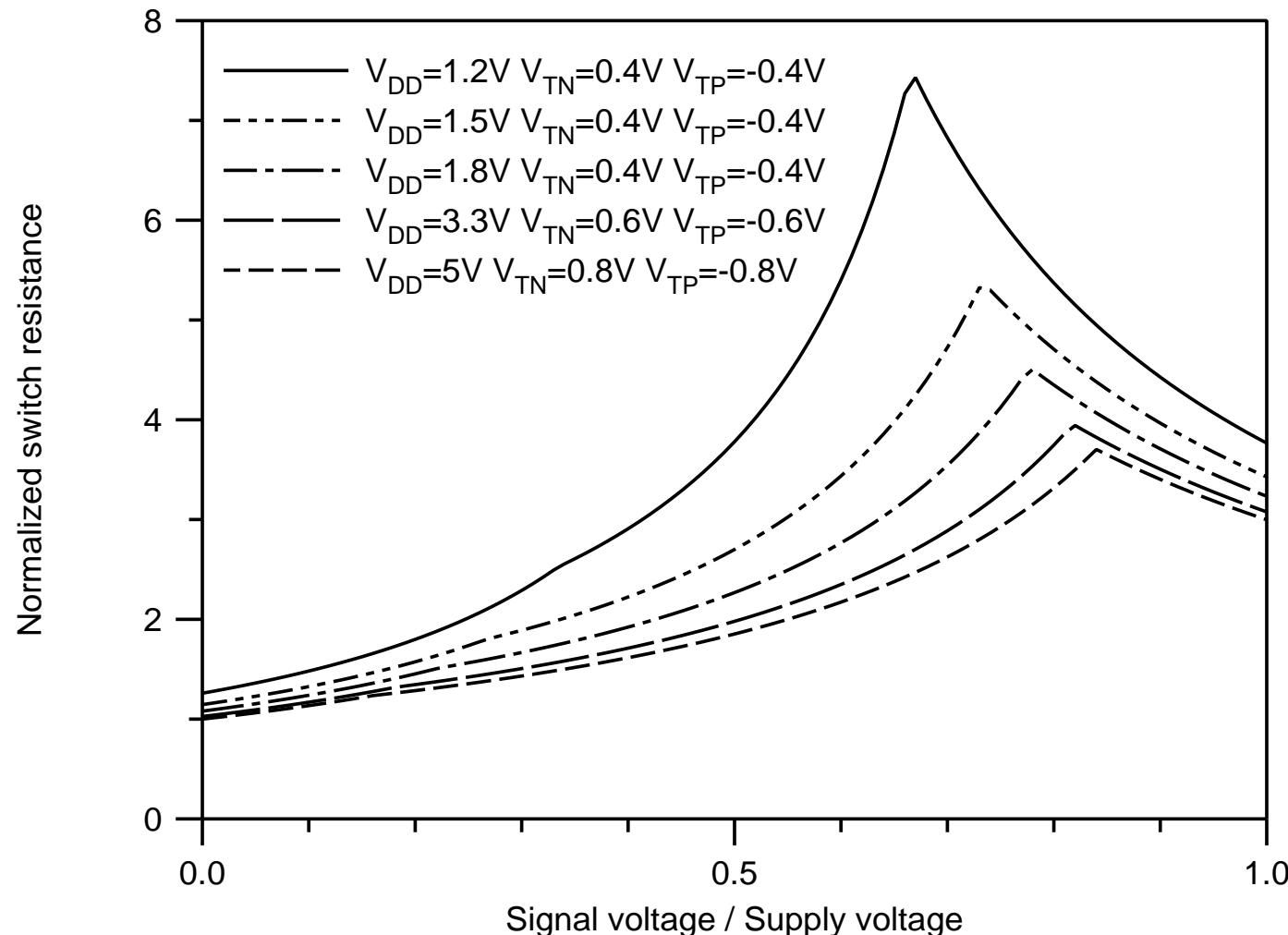
BASIC SWITCHED-CAPACITOR INTEGRATOR STAGE



GENERAL CMOS DIFFERENTIAL SAMPLING NETWORK

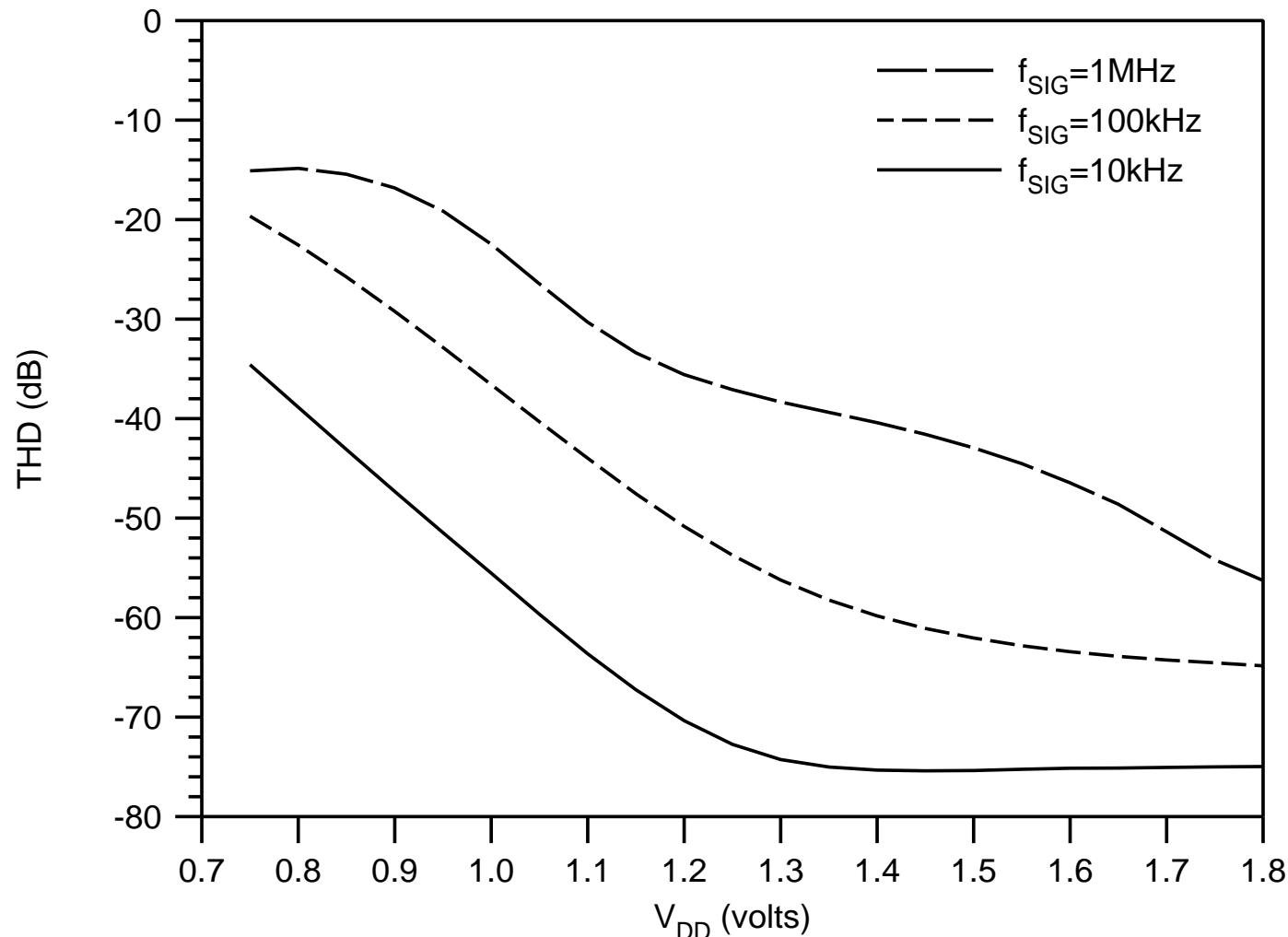


NORMALIZED RESISTANCE OF CMOS SAMPLING SWITCH FOR DIFFERENT POWER SUPPLY AND THRESHOLD VOLTAGES



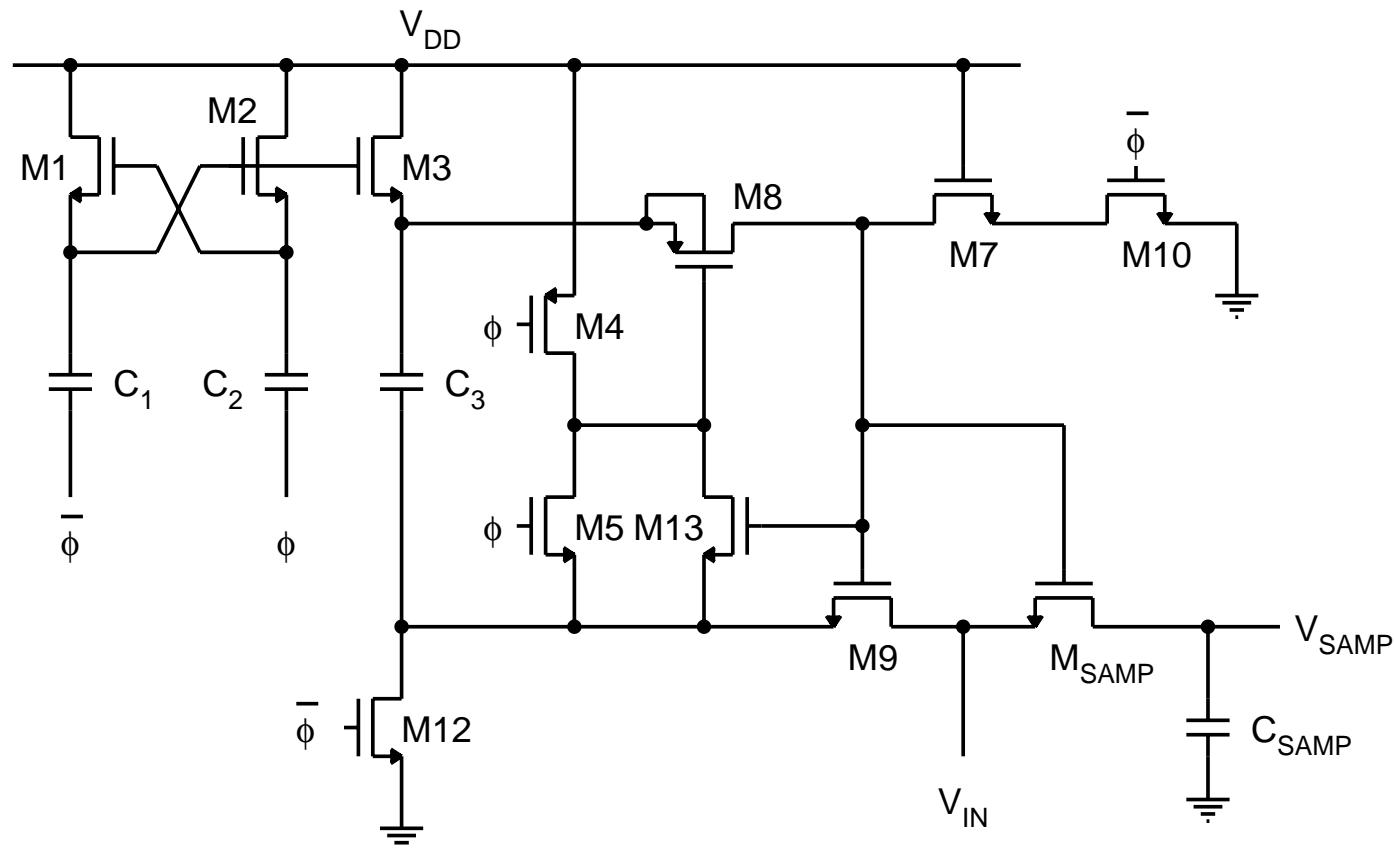
HARMONIC DISTORTION OF CMOS SAMPLING SWITCH VERSUS POWER SUPPLY VOLTAGE

$W_N=1\mu\text{m}$ $W_P=1\mu\text{m}$ $L_N=L_P=0.5\mu\text{m}$ $f_{SAMP}=10\text{MHz}$ $C_{SAMP}=1\text{pF}$



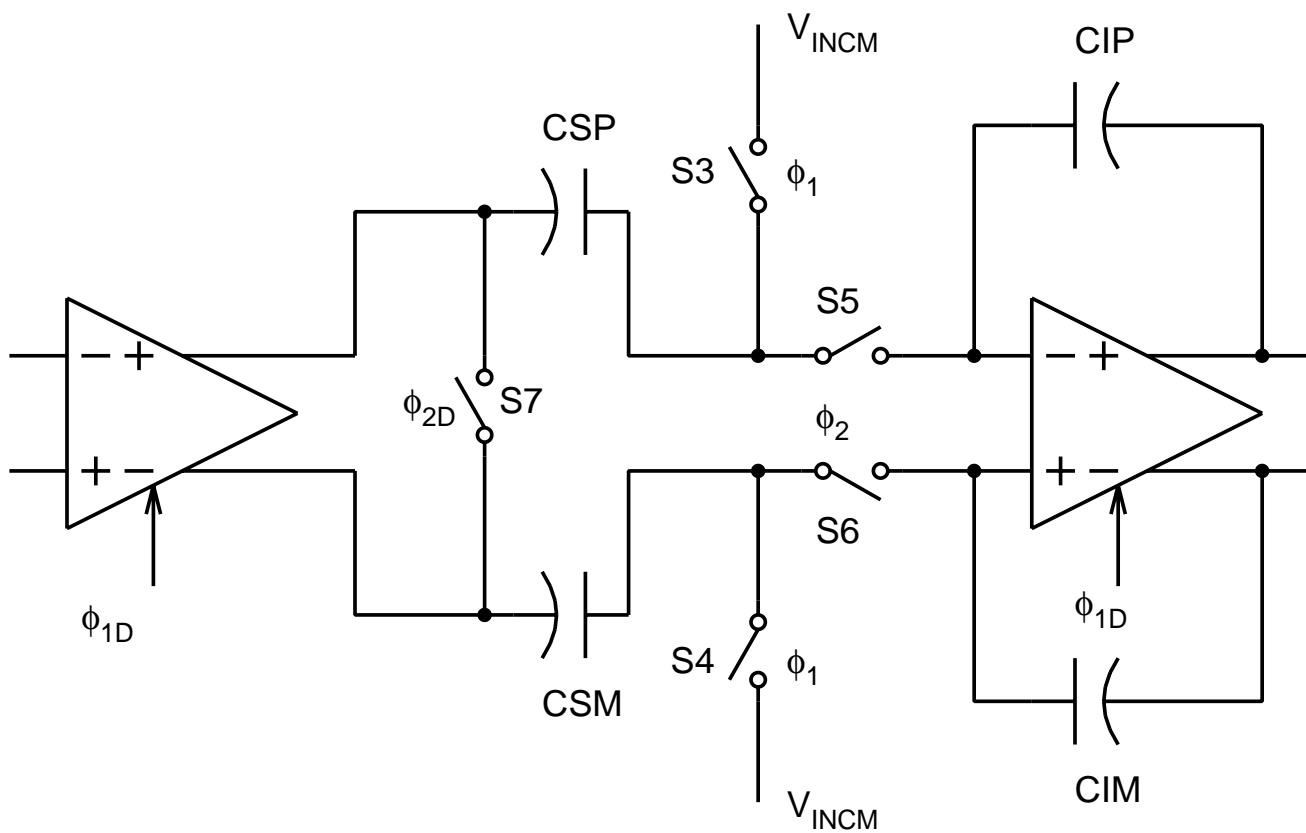
BOOTSTRAPPED SAMPLING GATE DRIVER

Abo and Gray (UC Berkeley) JSSC 5/99



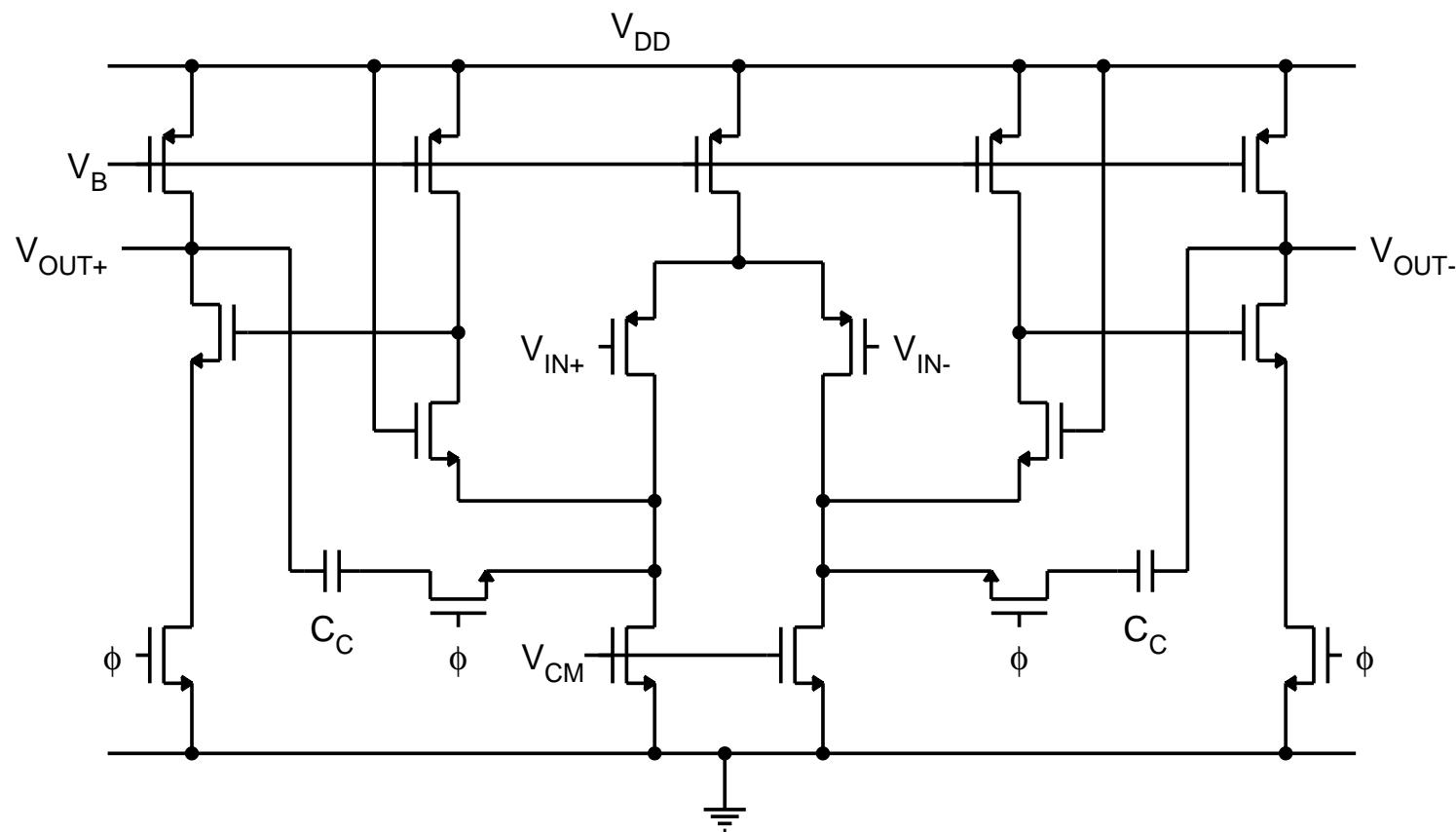
BASIC SWITCHED-OPAMP INTEGRATOR STAGE

Crols and Steyaert (K. Univ. Leuven) JSSC 8/94



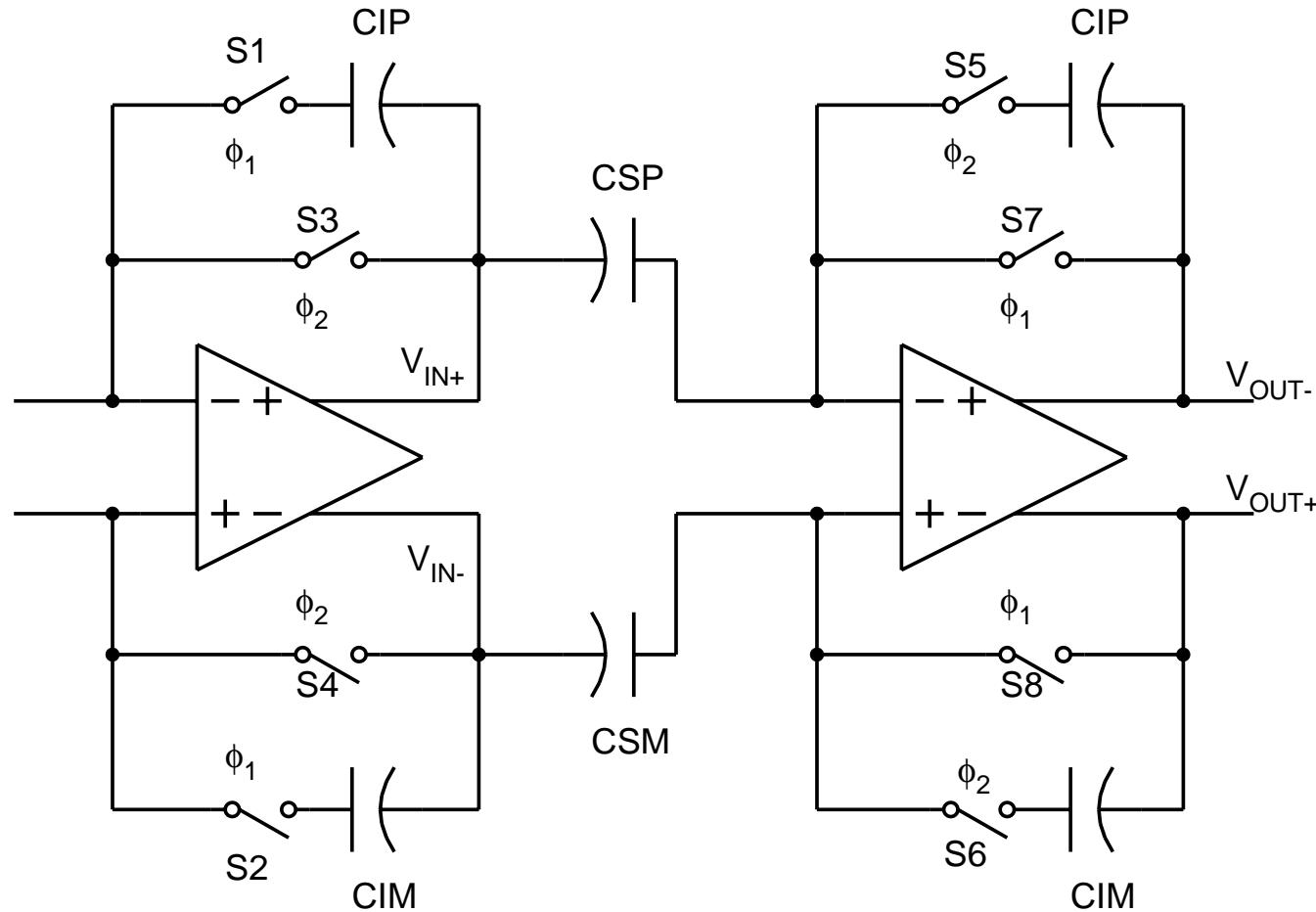
EXAMPLE SWITCHABLE OPAMP

Baschirotto and Castello (Univ. Pavia) JSSC 12/97

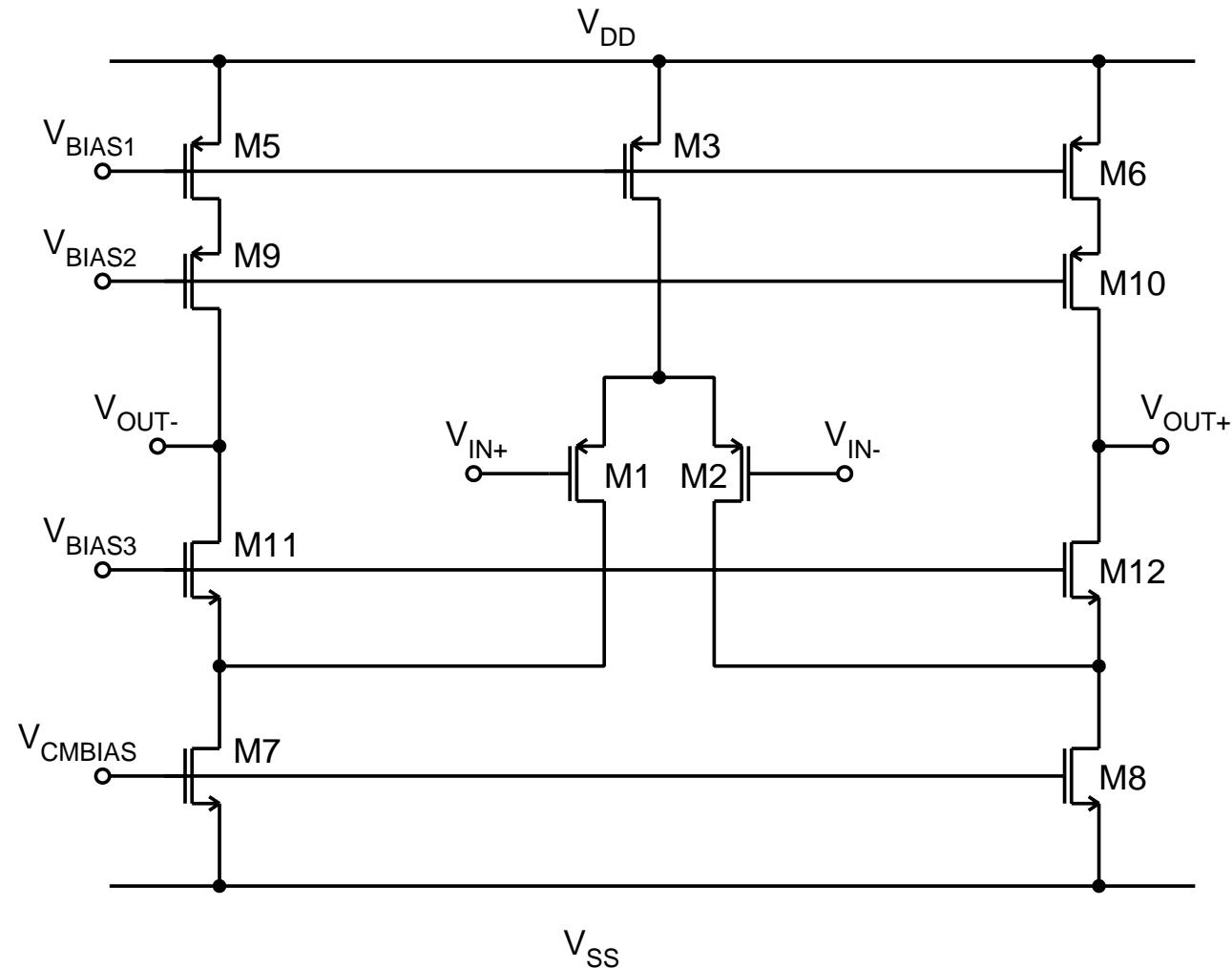


BASIC OPAMP-RESET INTEGRATOR STAGE

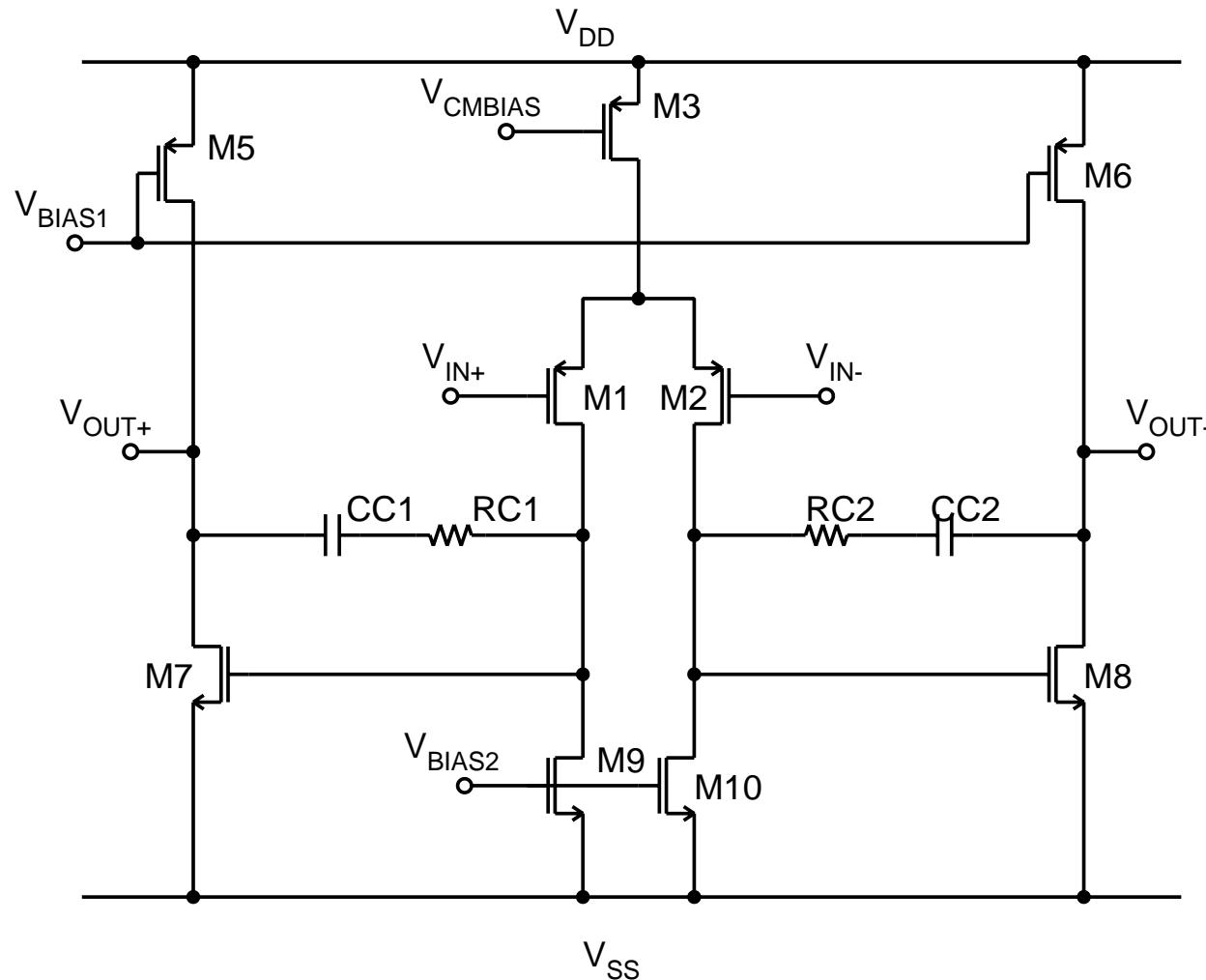
Bidari et al. (Oregon State) ISCAS 1999



CONVENTIONAL FOLDED CASCODE OPAMP

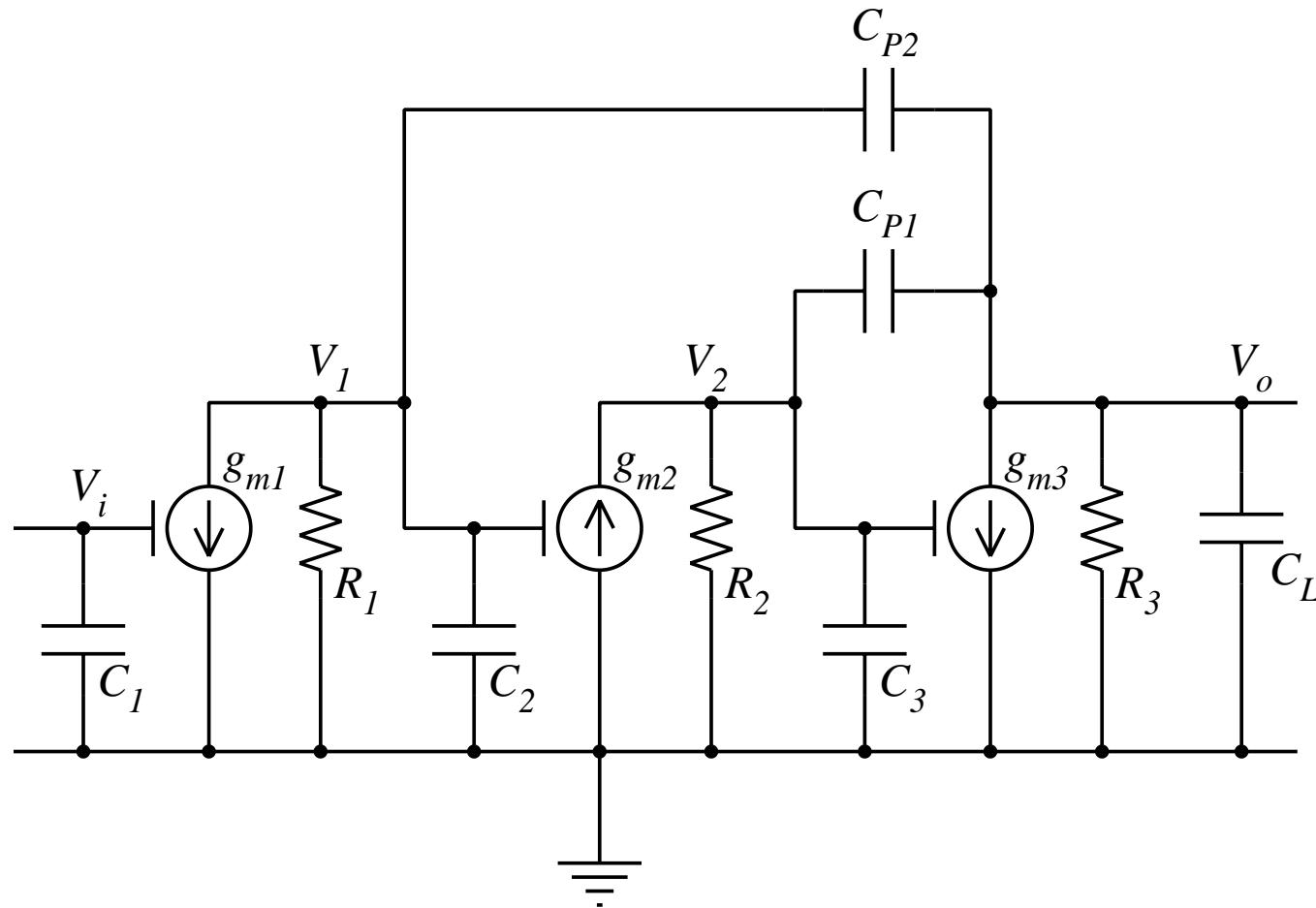


TWO STAGE MILLER COMPENSATED OPAMP



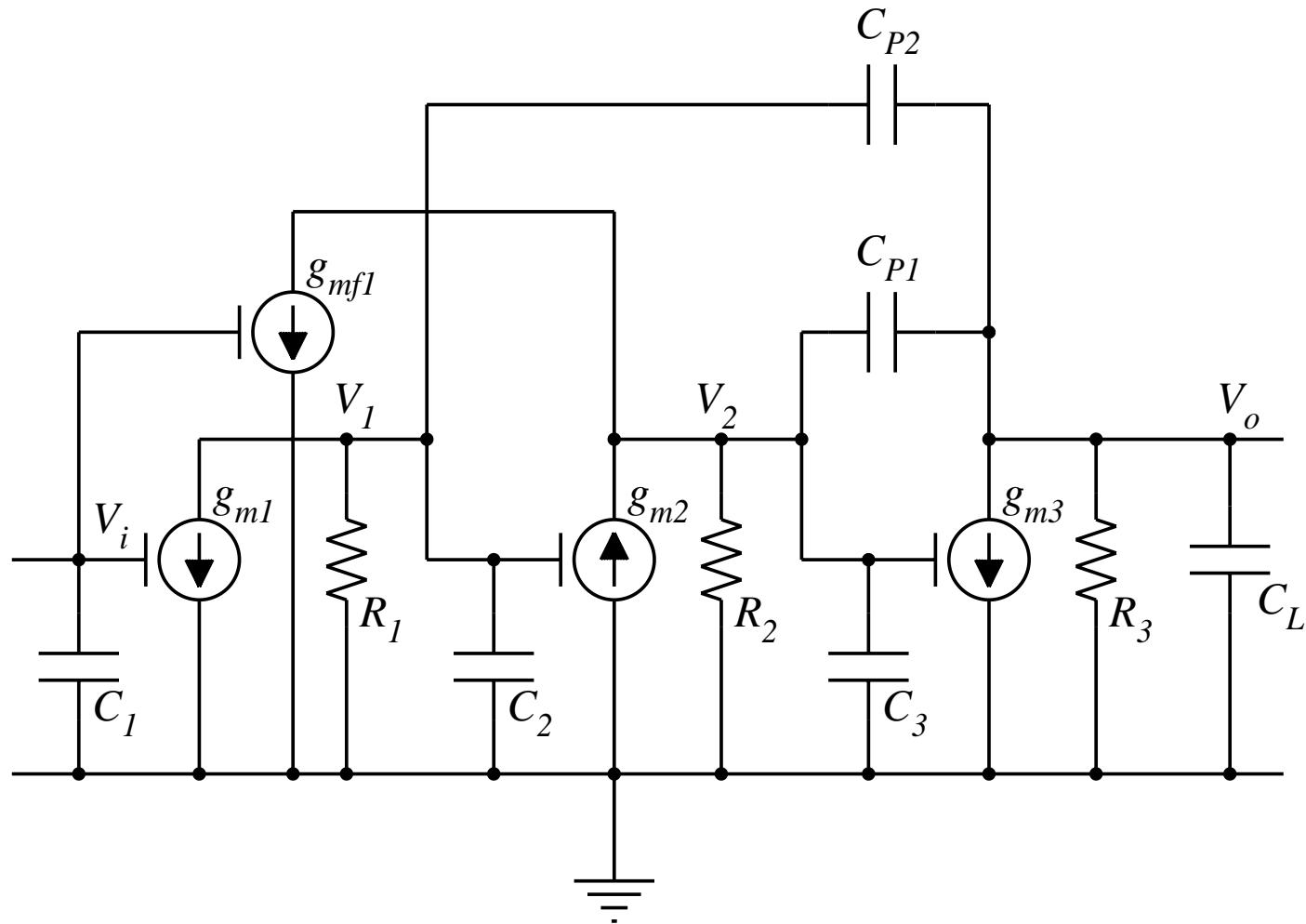
THREE STAGE OPAMP WITH NESTED MILLER COMPENSATION

Eschauzier, et al. (Delft Univ.) JSSC 12/92



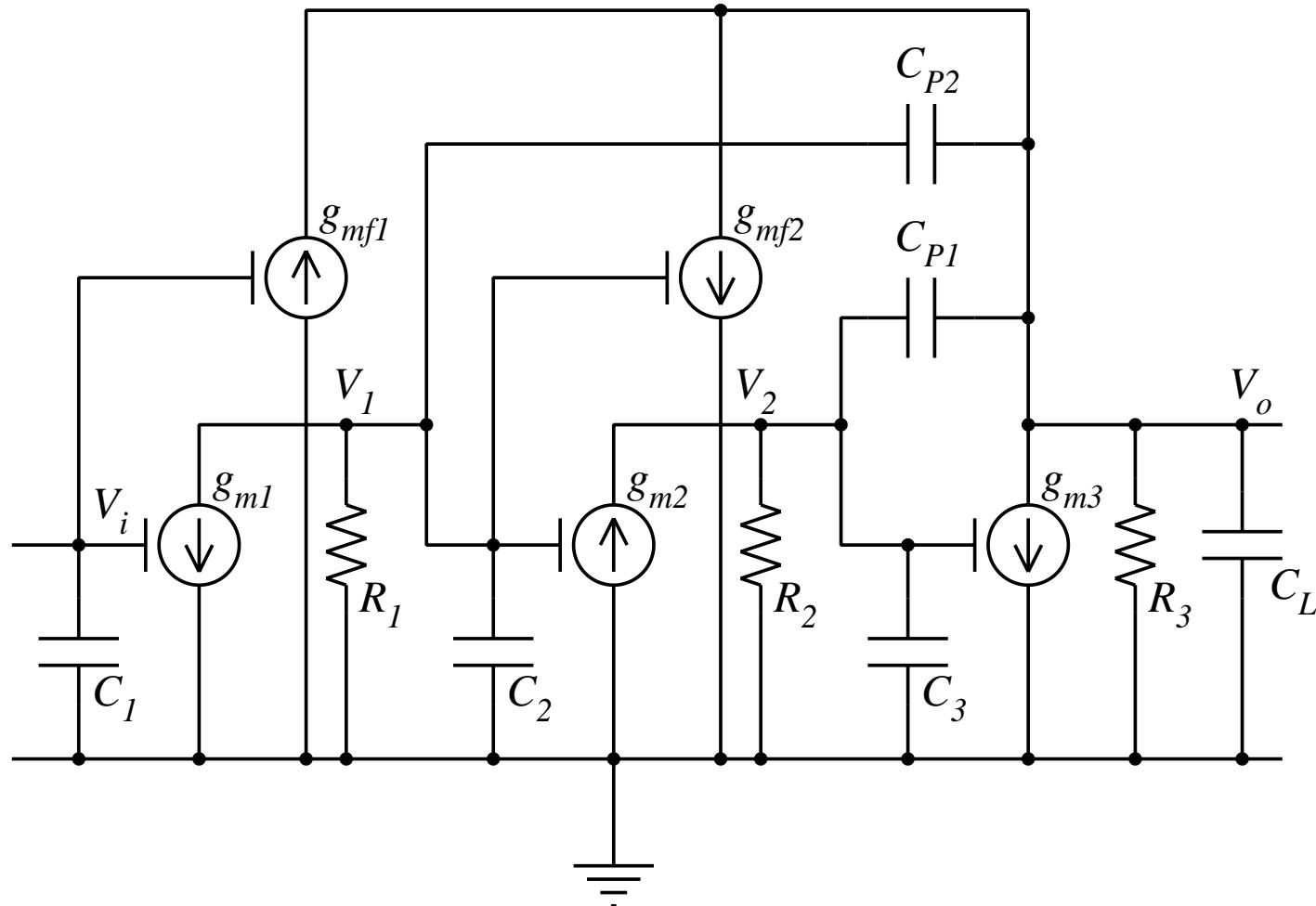
MULTIPATH NESTED MILLER COMPENSATION

Eschauzier, et al. (Delft Univ.) JSSC 12/92



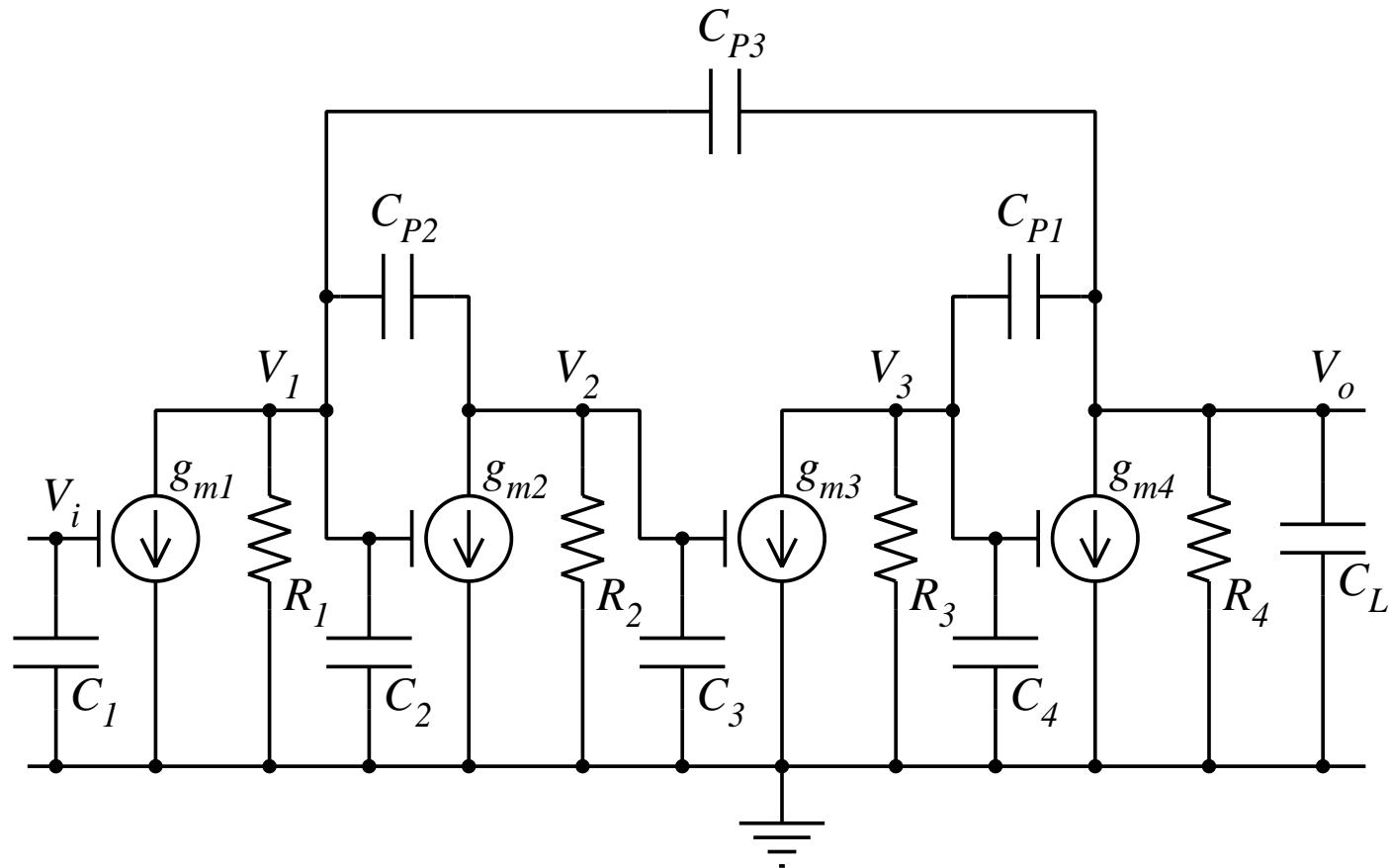
FEEDFORWARD CANCELLATION OF RIGHT HALF PLANE ZERO

You, et al. (TA&M Univ.) JSSC 12/97



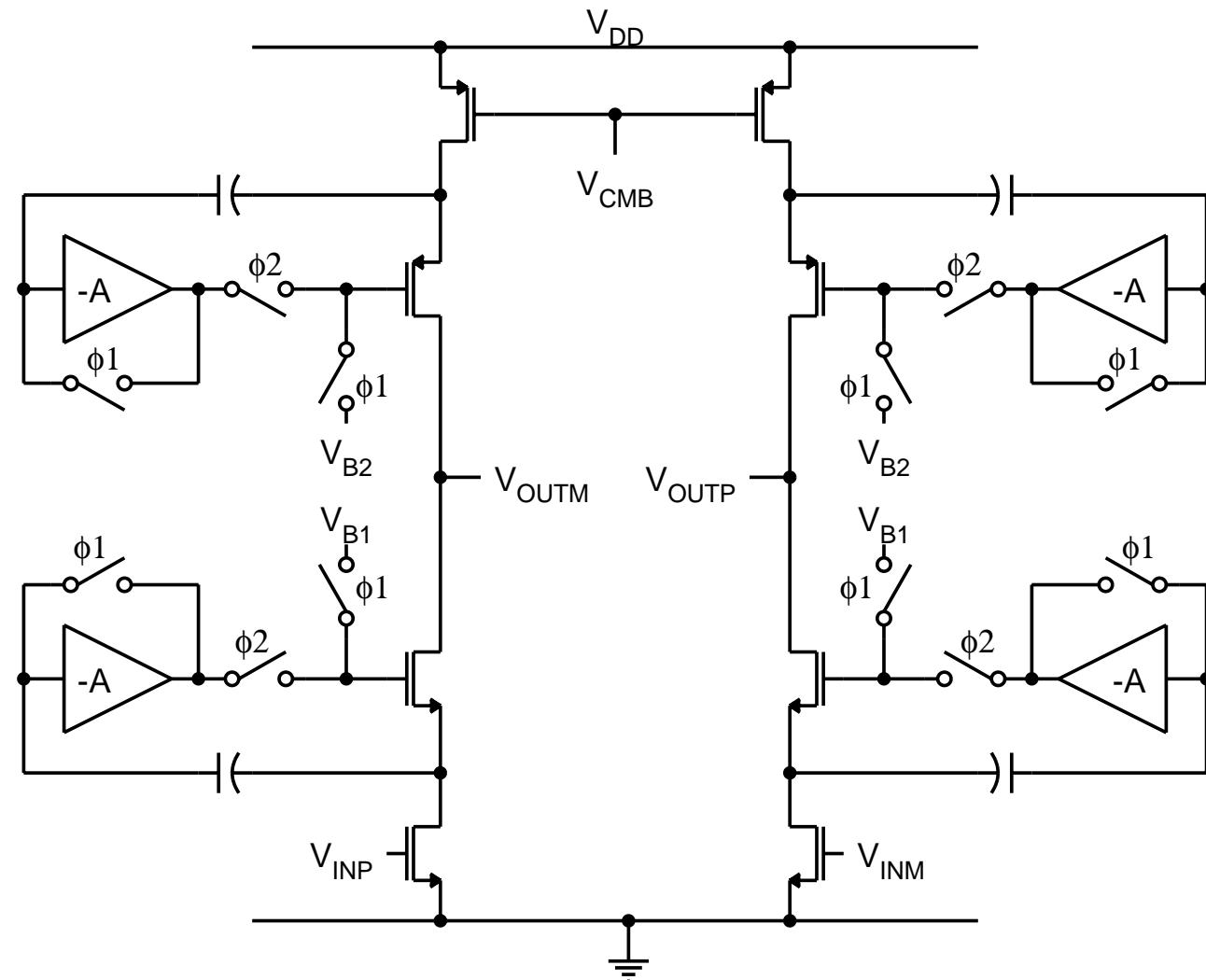
FOUR STAGE OPAMP WITH NESTED MILLER COMPENSATION

Eschauzier, et al. (Delft Univ.) JSSC 12/94

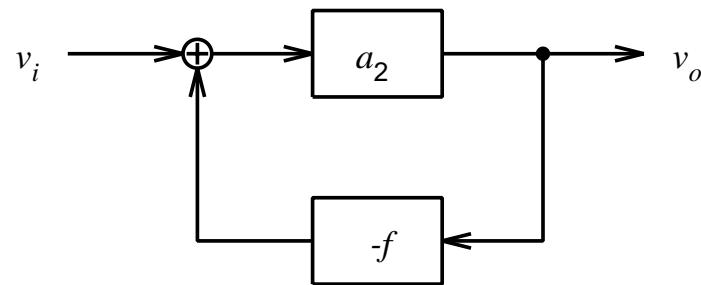
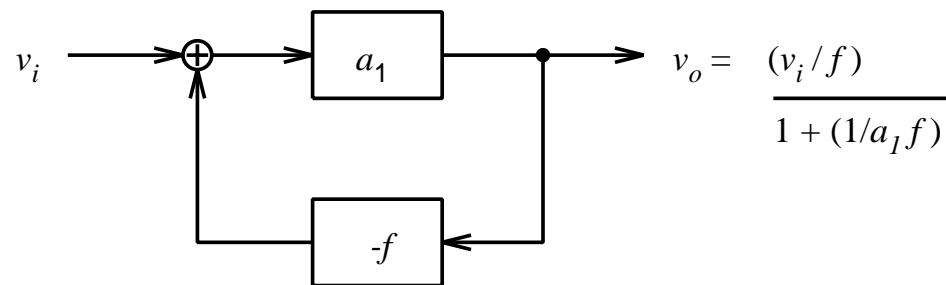


PSEUDO DIFFERENTIAL OPAMP WITH SC REGULATED CASCODE

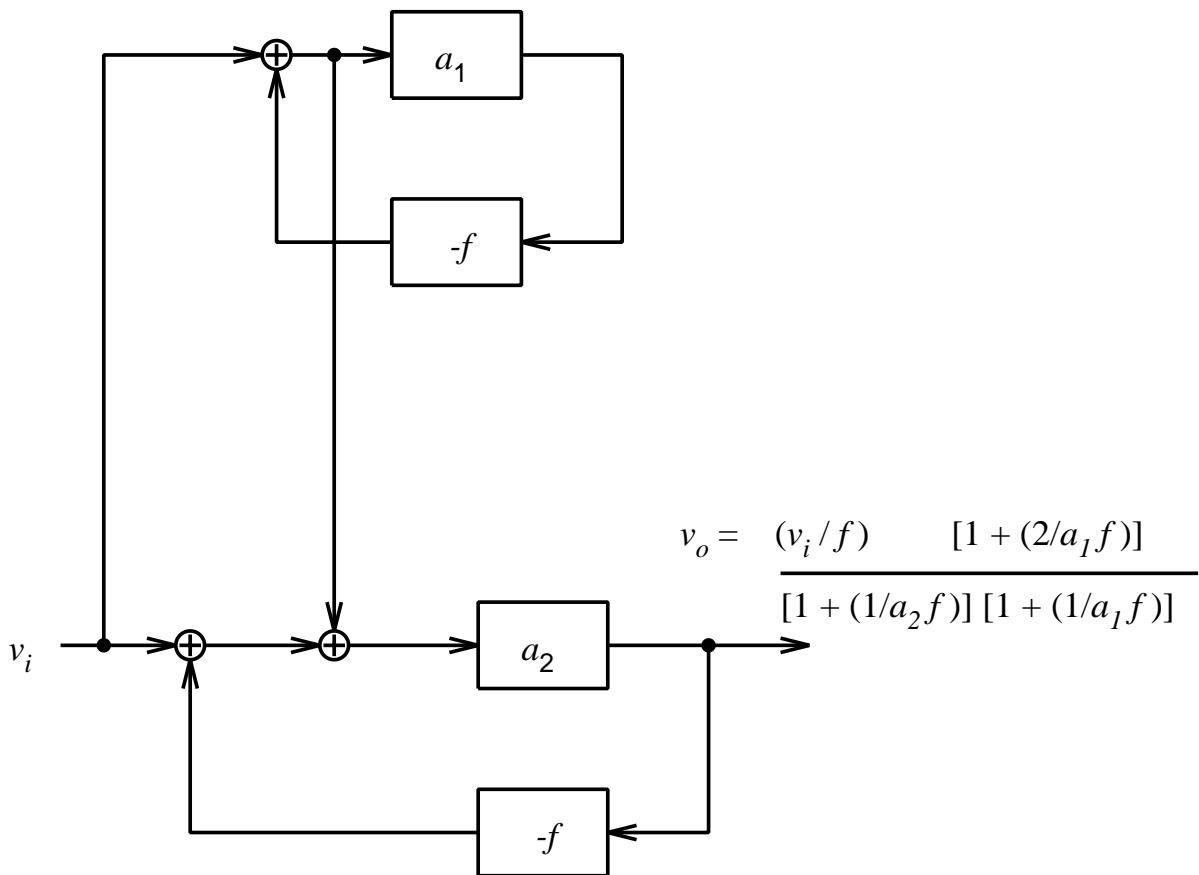
Gunay (TI and TA&M Univ.) CICC 1998



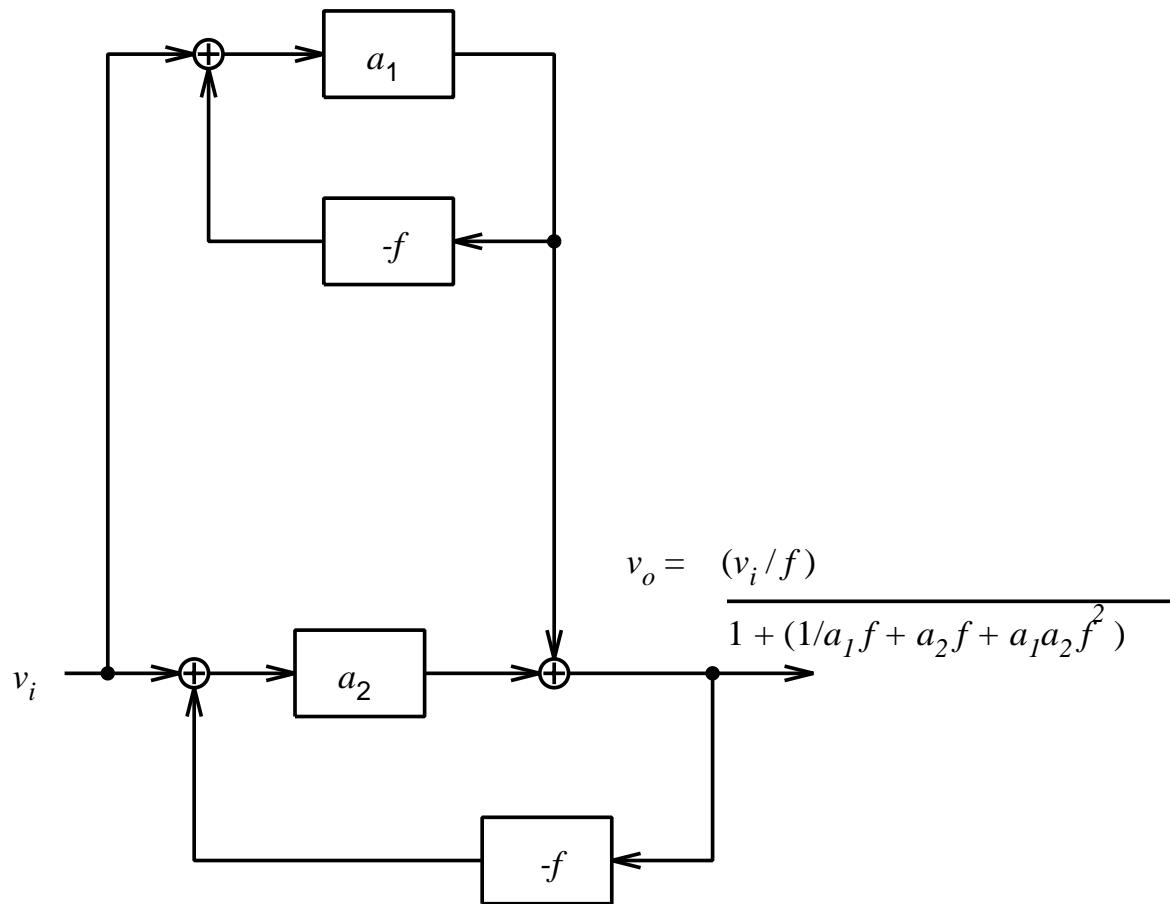
UNCORRECTED OPAMP FEEDBACK CIRCUITS



OPAMP FEEDBACK WITH INPUT CORRECTION

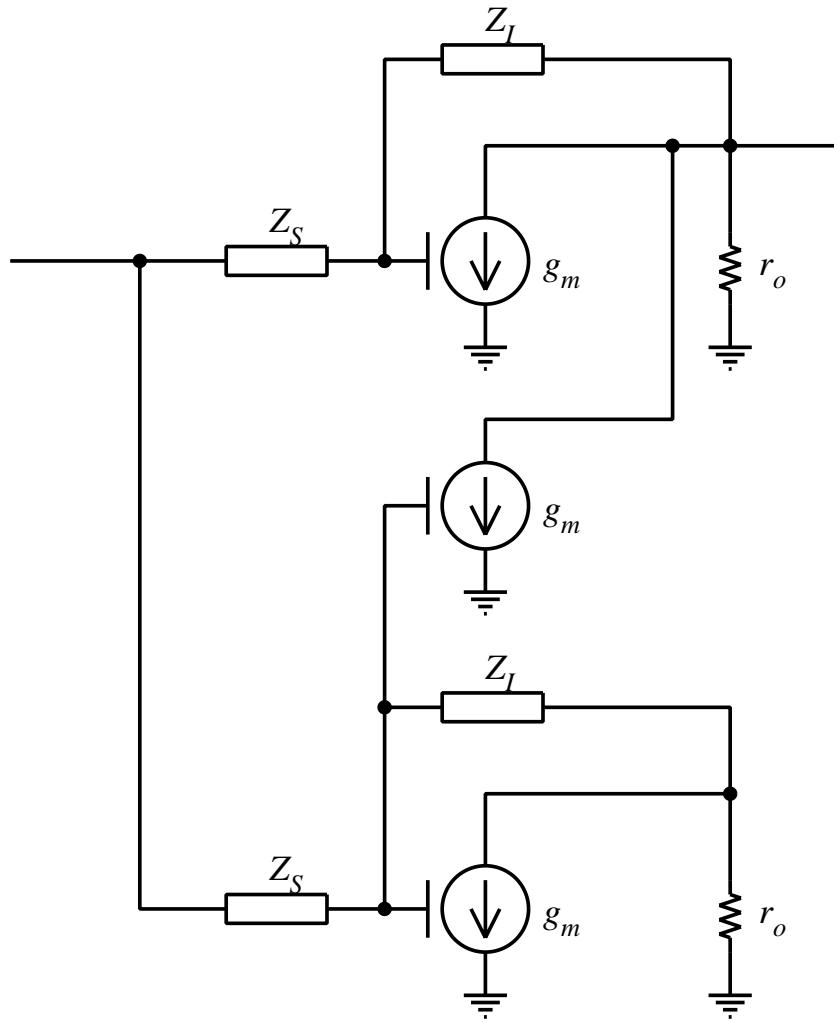


OPAMP FEEDBACK WITH OUTPUT CORRECTION



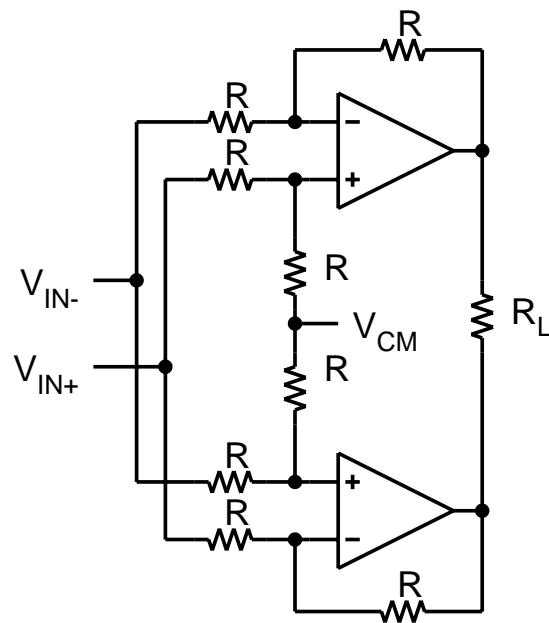
OPAMP GAIN CORRECTION WITH REPLICA

Yu and Lee (MIT) JSSC 12/93

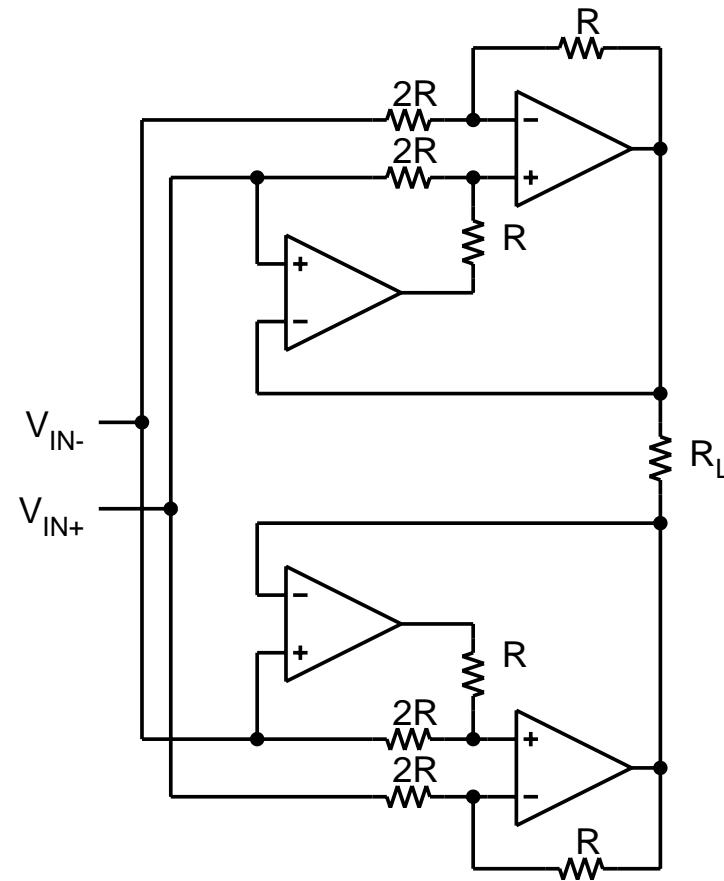


LOW DISTORTION BRIDGE AMPLIFIER FOR RESISTIVE LOADS

Muza (T.I.) US Patent 6,275,102 8/01



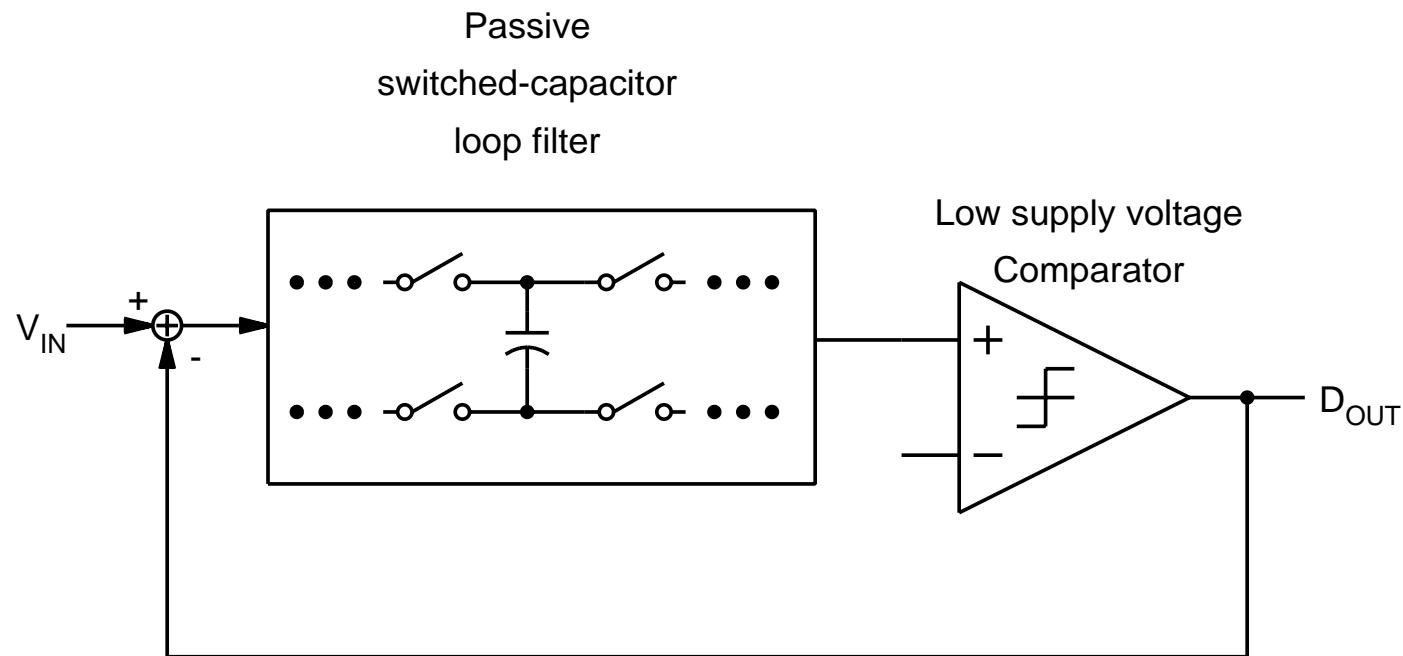
Conventional



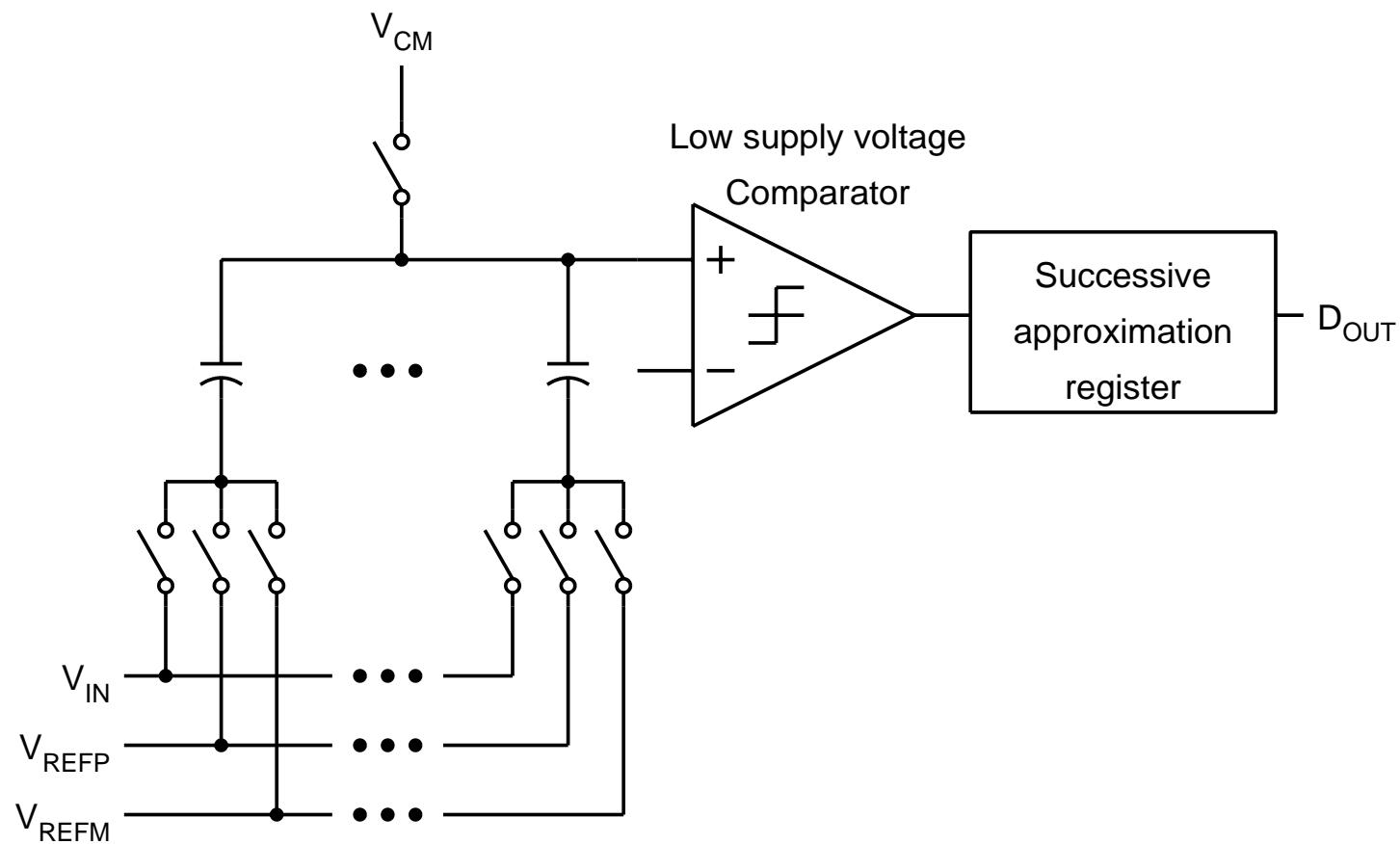
Correction amplifiers suppress distortion

LOW VOLTAGE PASSIVE $\Sigma\Delta$ MODULATOR

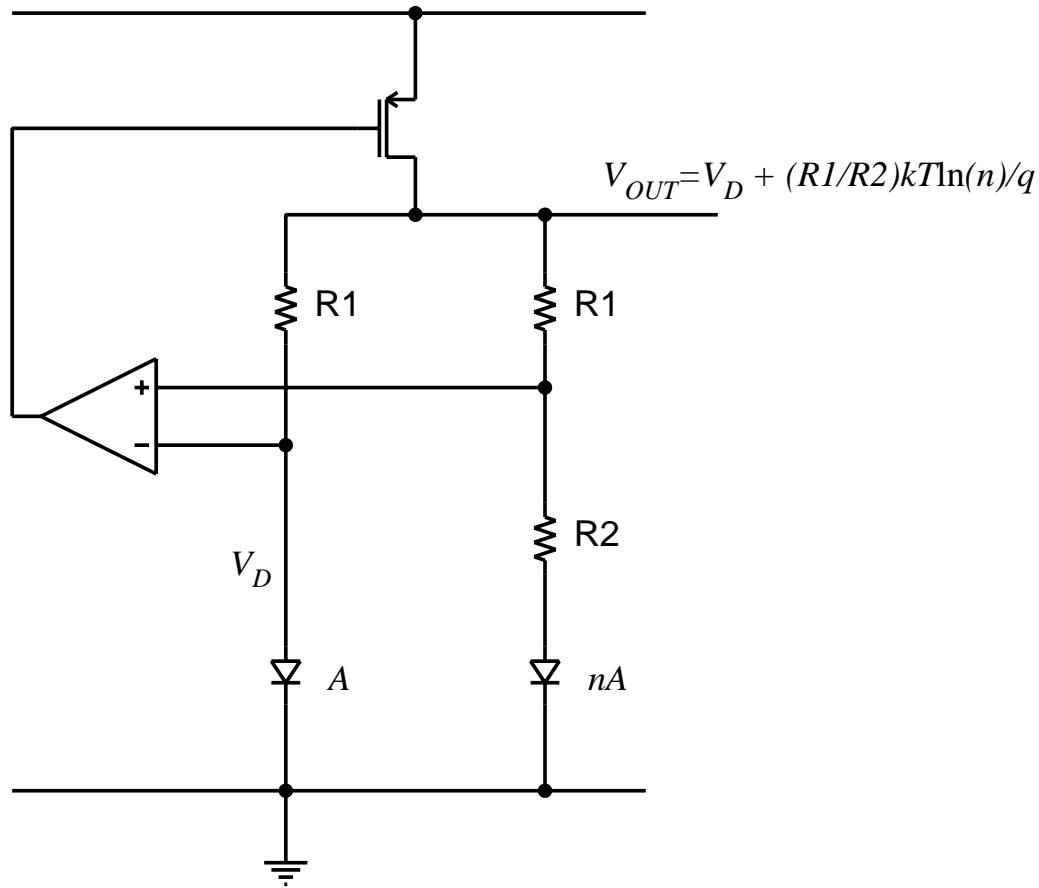
Chen, et al. (TI) ISSCC 2003



CHARGE-REDISTRIBUTION SUCCESSIVE APPROXIMATION ADC

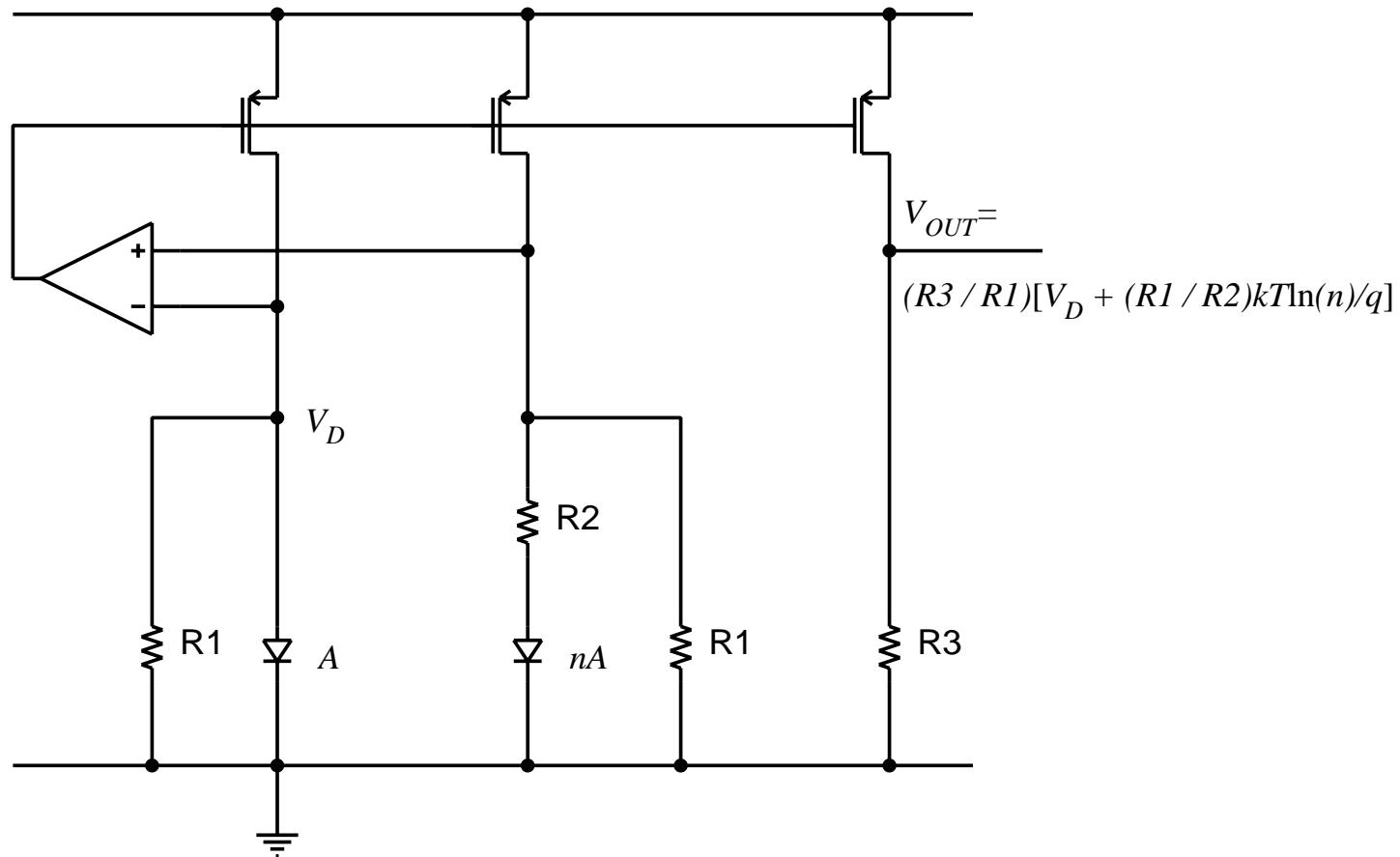


BASIC BANDGAP REFERENCE GENERATOR



LOW VOLTAGE BANDGAP REFERENCE GENERATOR

Banba, et al. (Toshiba) JSSC 5/99

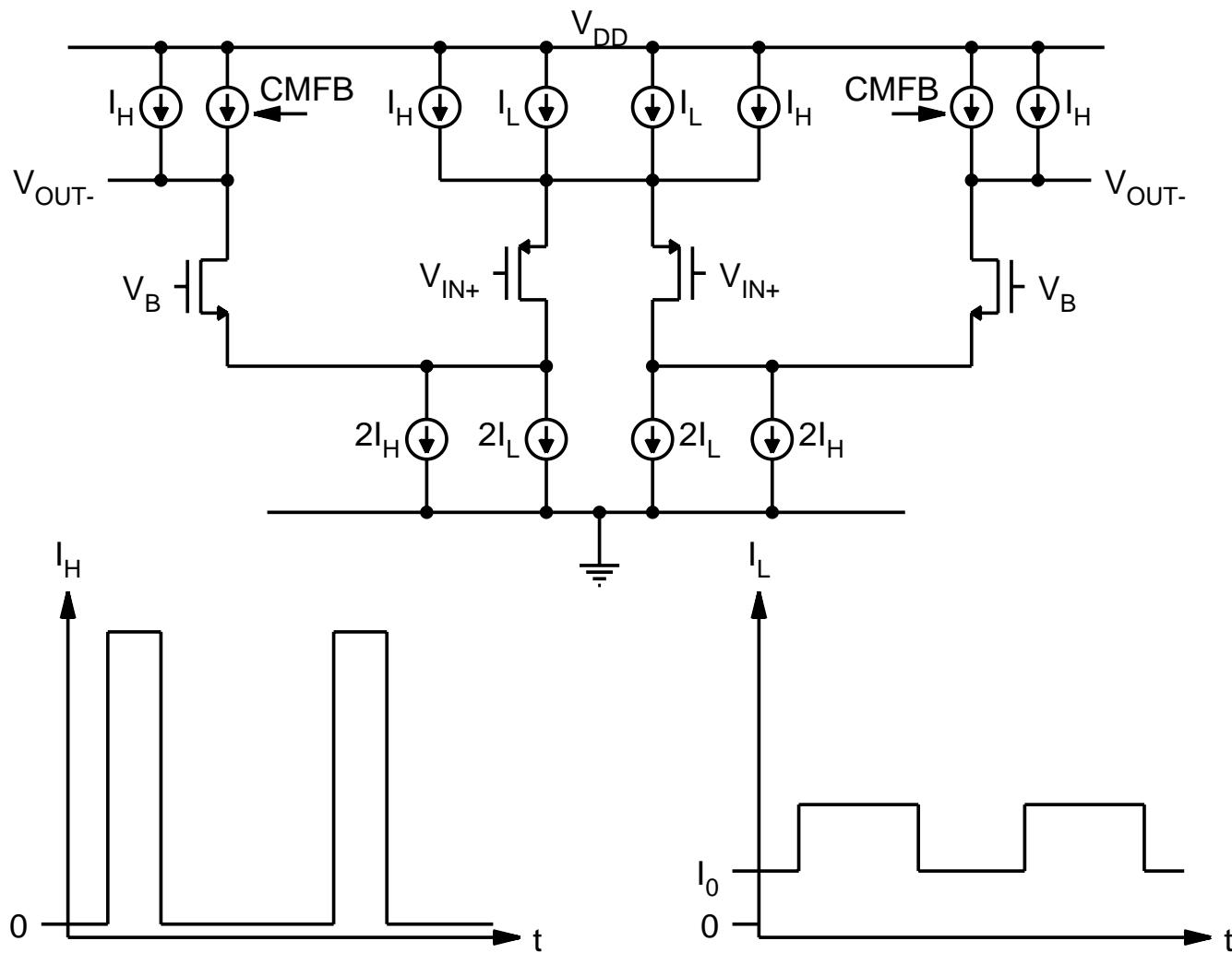


OUTLINE

- Introduction
- Low supply voltage constraints
- **Low power constraints**
- Common substrate constraints
- Interconnect constraints

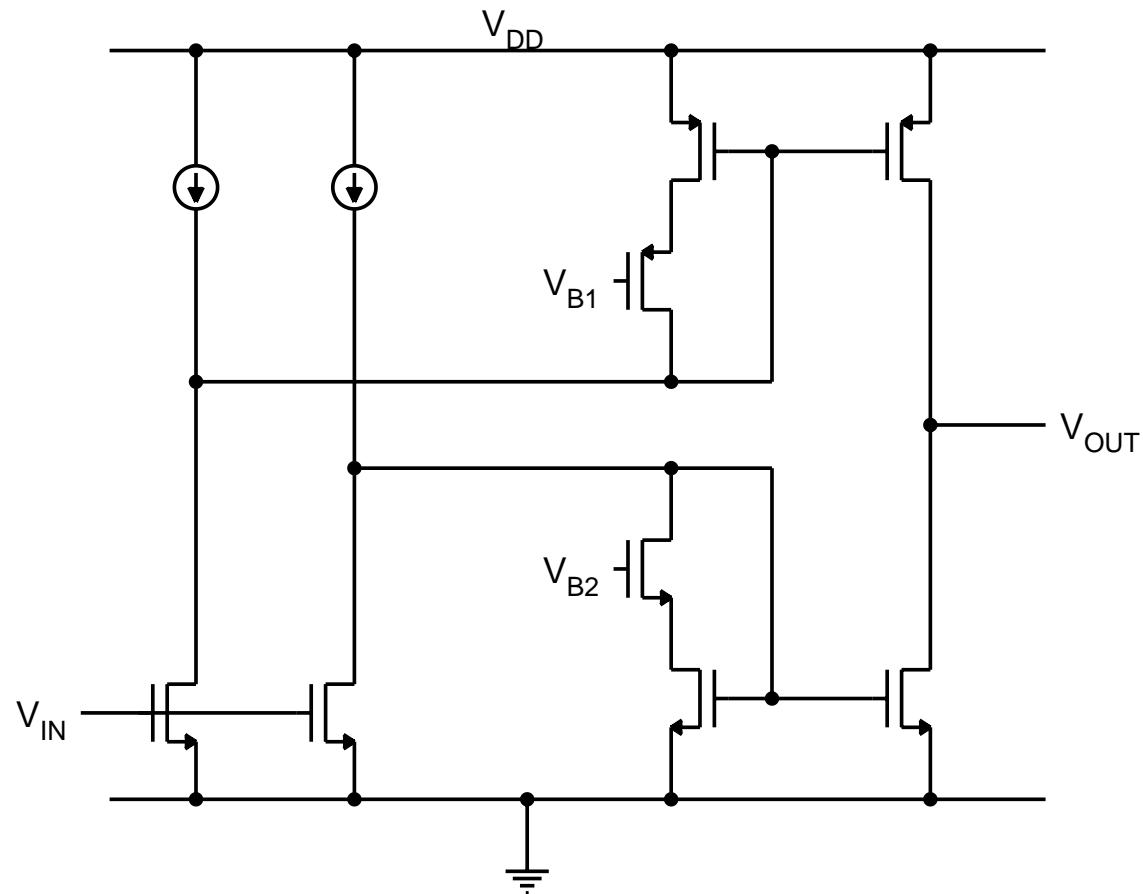
DYNAMICALLY BIASED OPAMP FOR SWITCHED CAPACITORS

Kasha, et al. (Crystal) JSSC 7/99

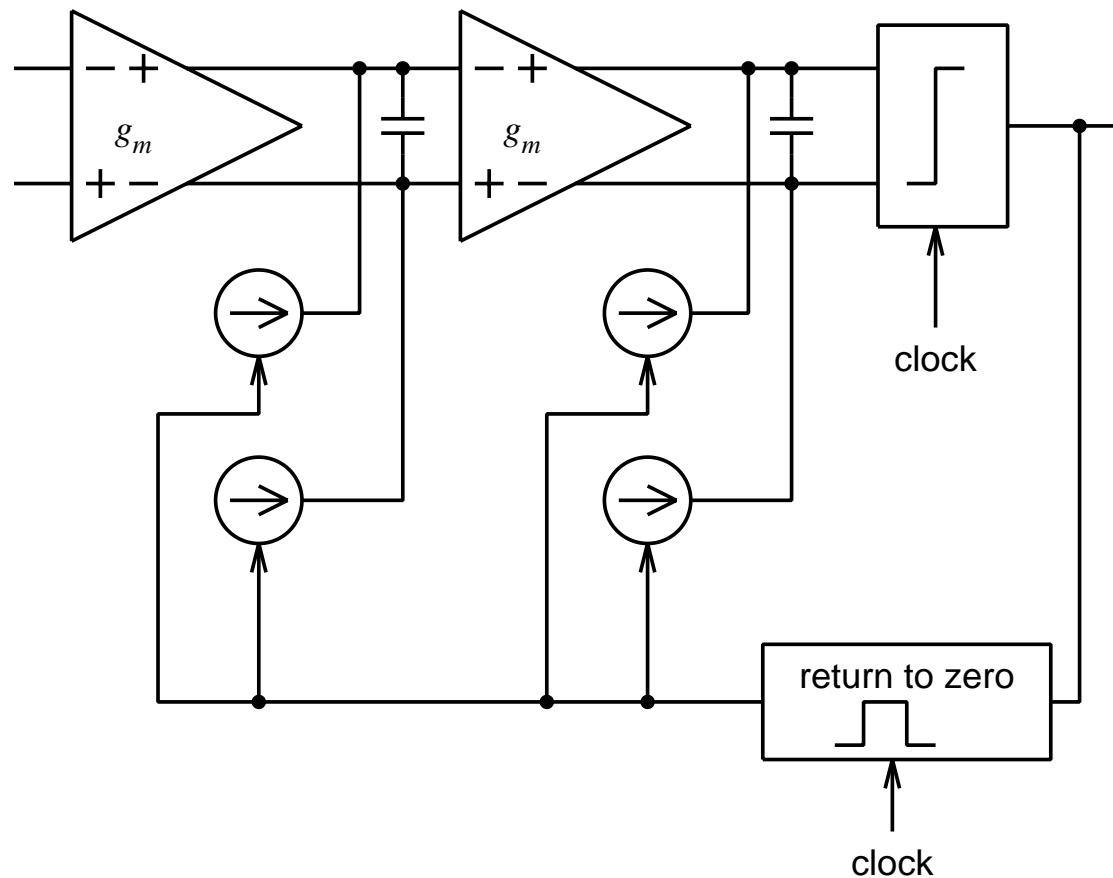


LOW VOLTAGE CLASS AB OPAMP OUTPUT STAGE

You, et al. (TA&M Univ.) JSSC 6/98

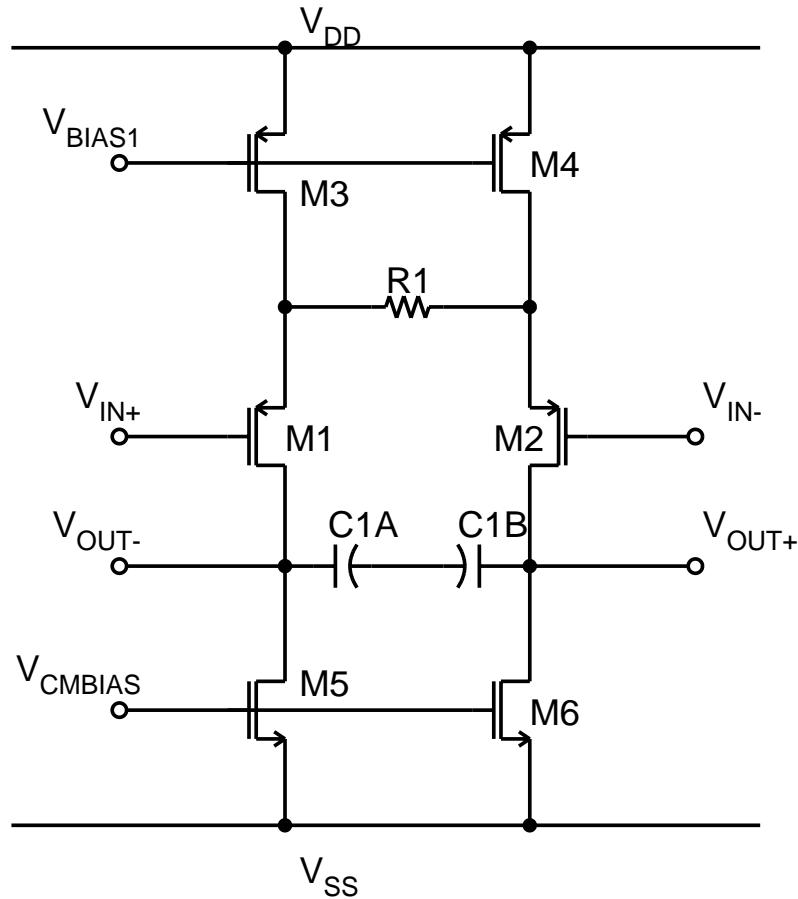


SECOND-ORDER CONTINUOUS TIME $\Sigma-\Delta$ MODULATOR



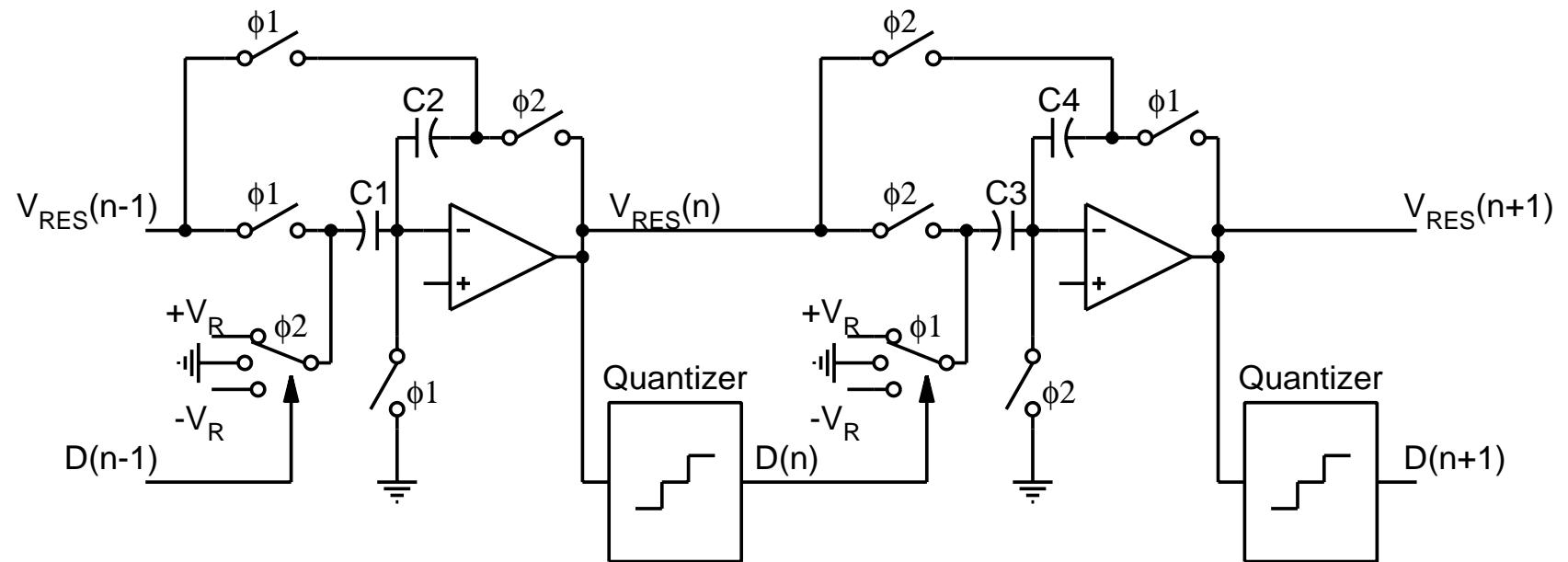
BASIC CONTINUOUS TIME INTEGRATOR STAGE

van der Zwan and Dijkmans (Philips) JSSC 12/96



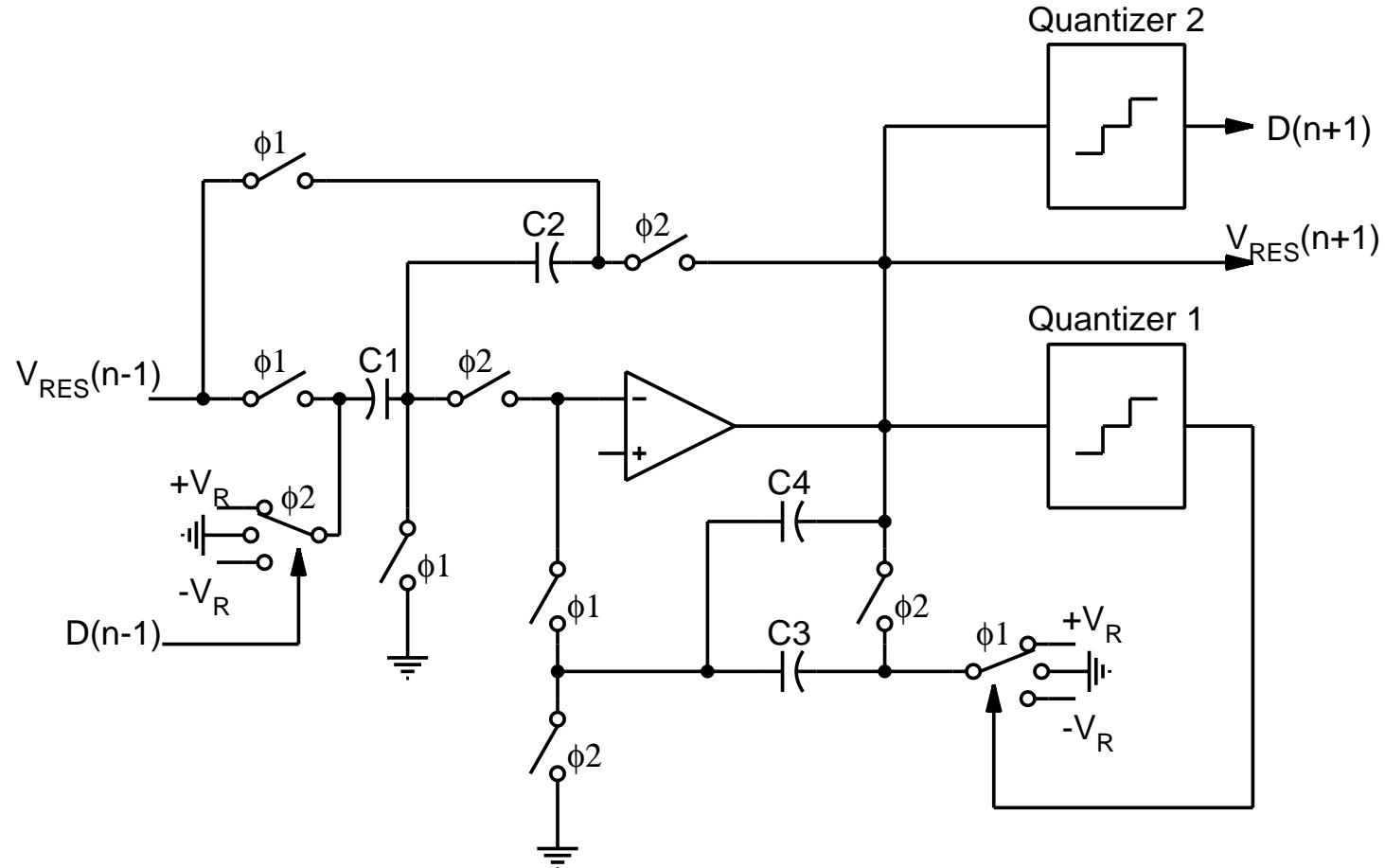
CONVENTIONAL PIPELINE ADC

Two successive stages, with two opamps

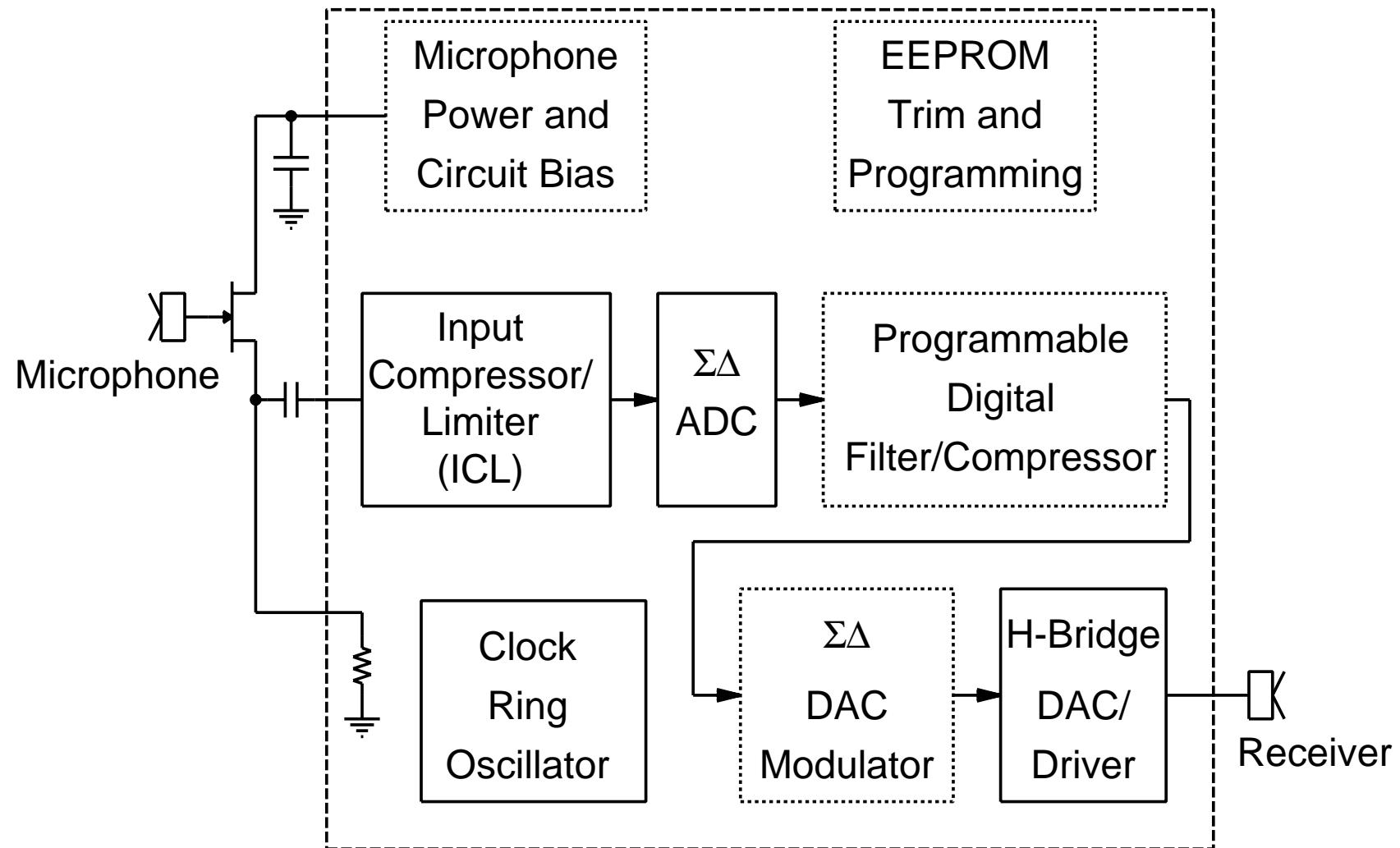


PIPELINE ADC WITH SHARED OPAMPS

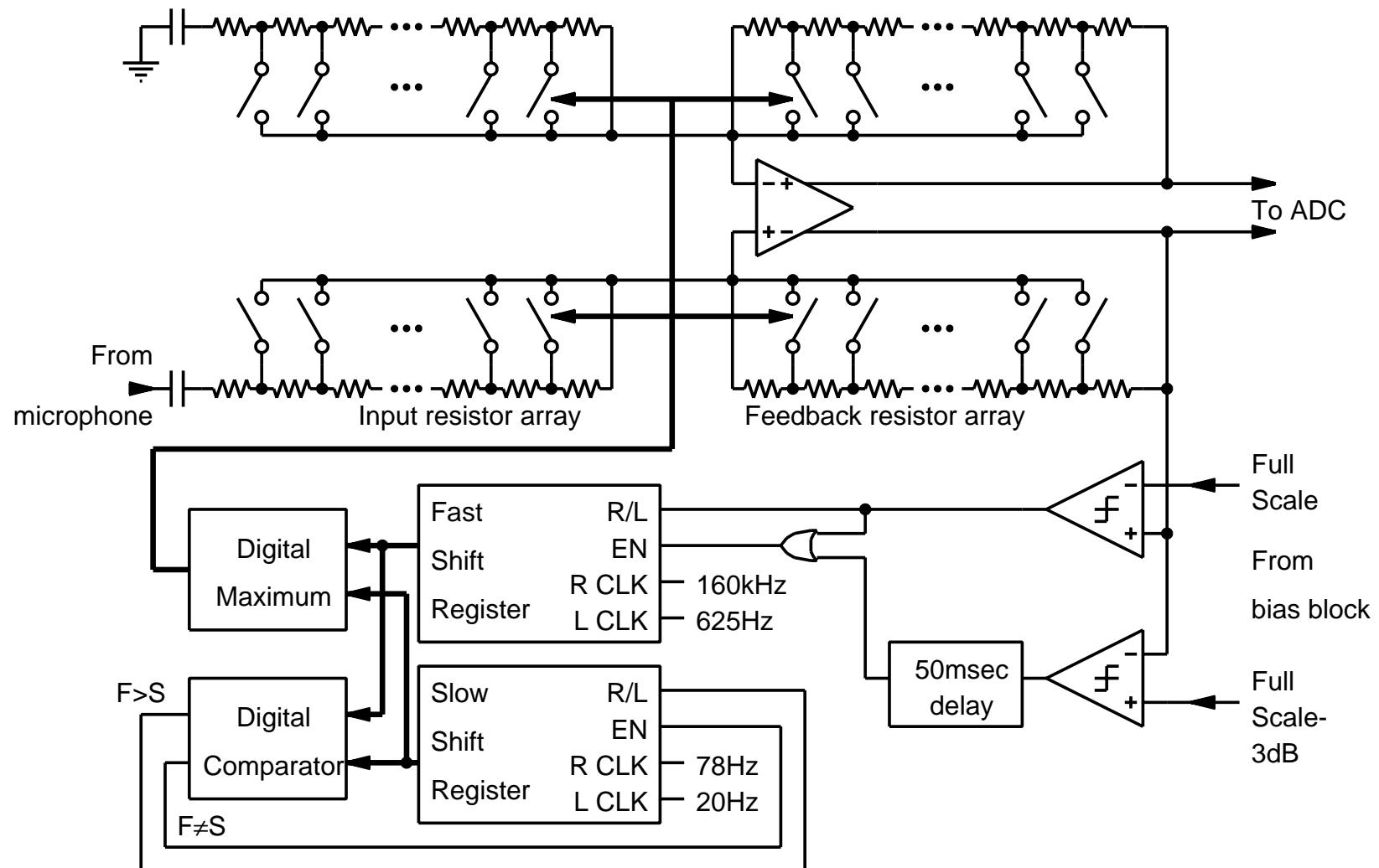
Nagaraj, et al. (Lucent) JSSC 3/97



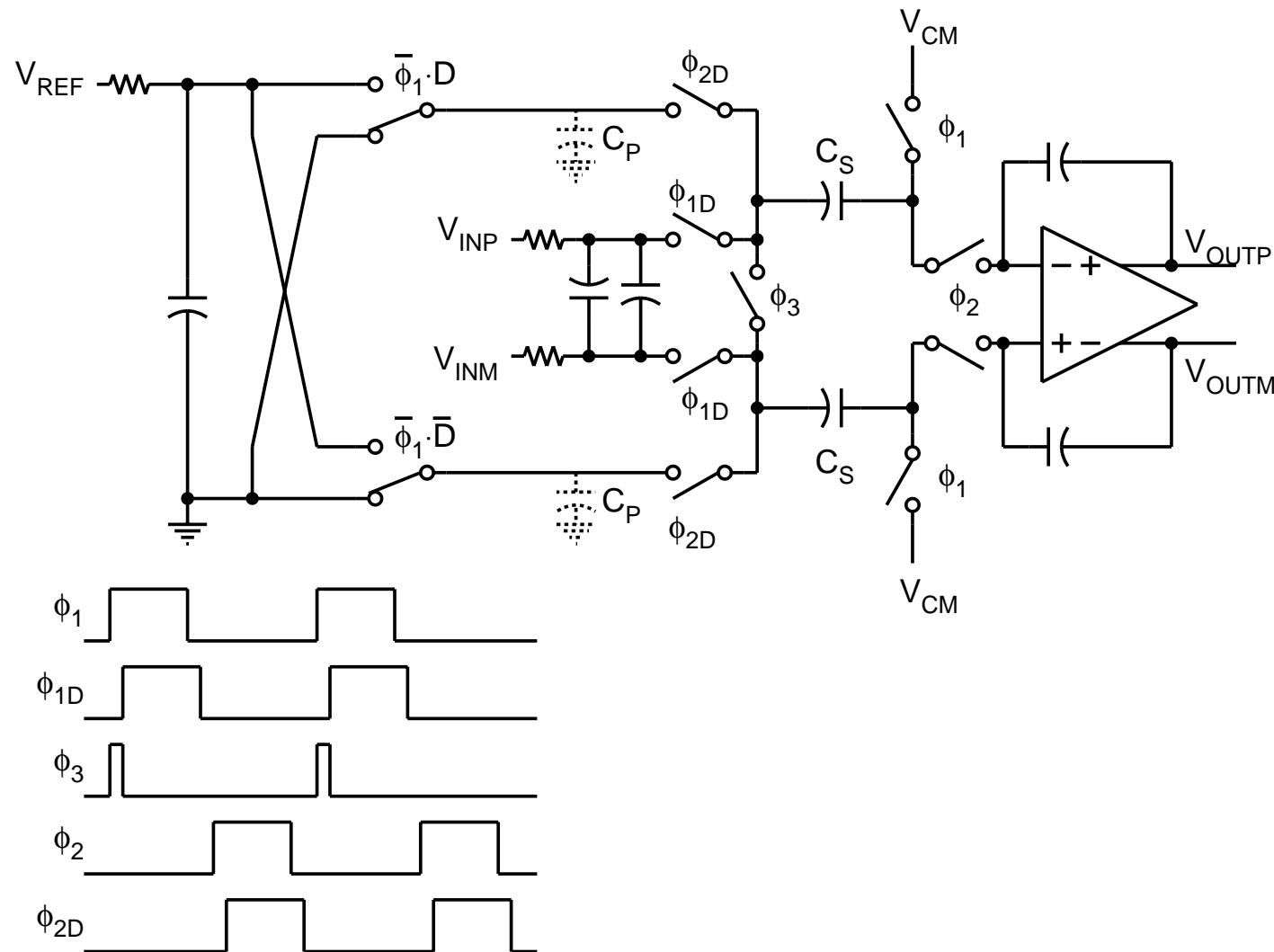
SINGLE-CHIP HEARING AID BLOCK DIAGRAM



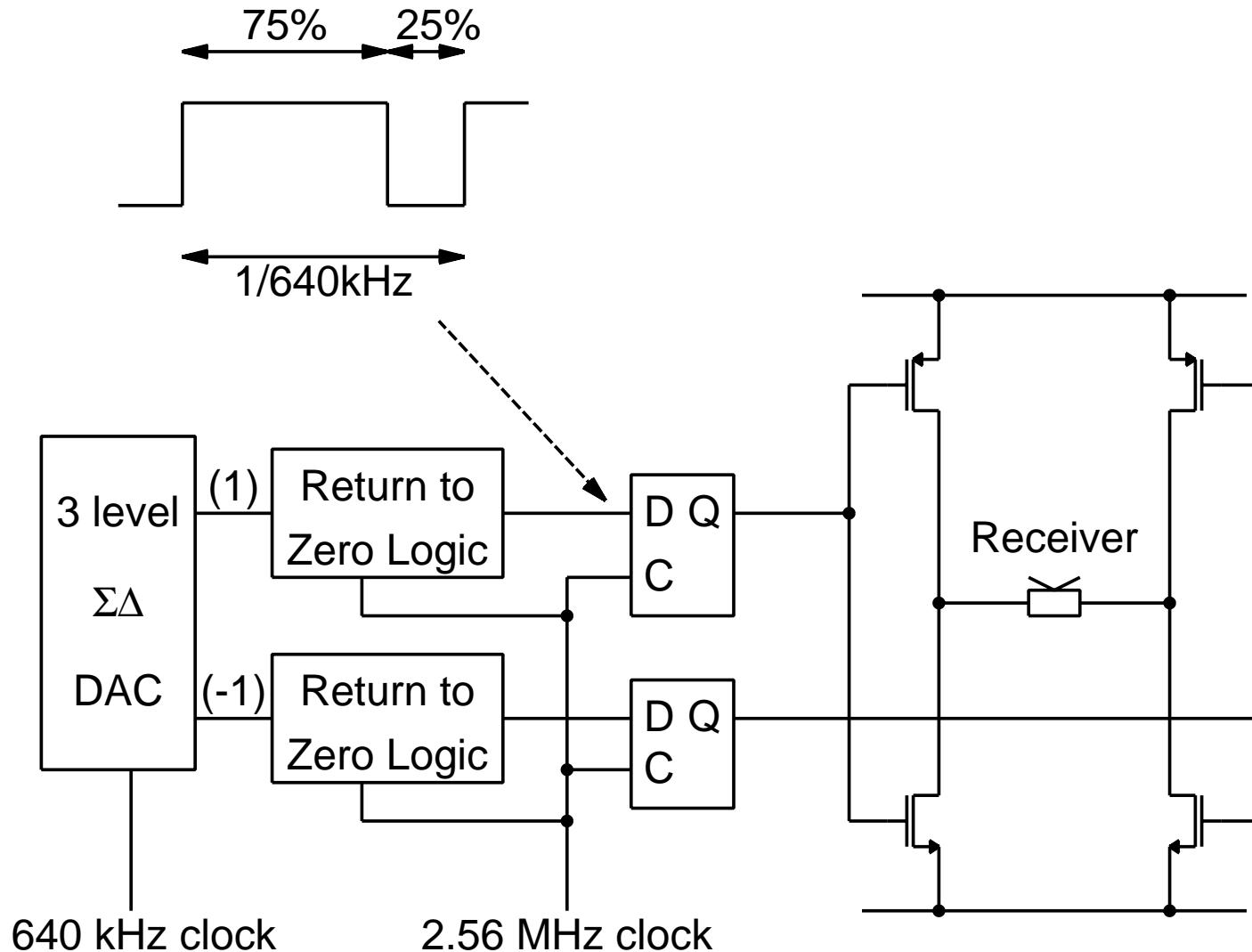
INPUT COMPRESSOR/LIMITER (ICL) ARCHITECTURE



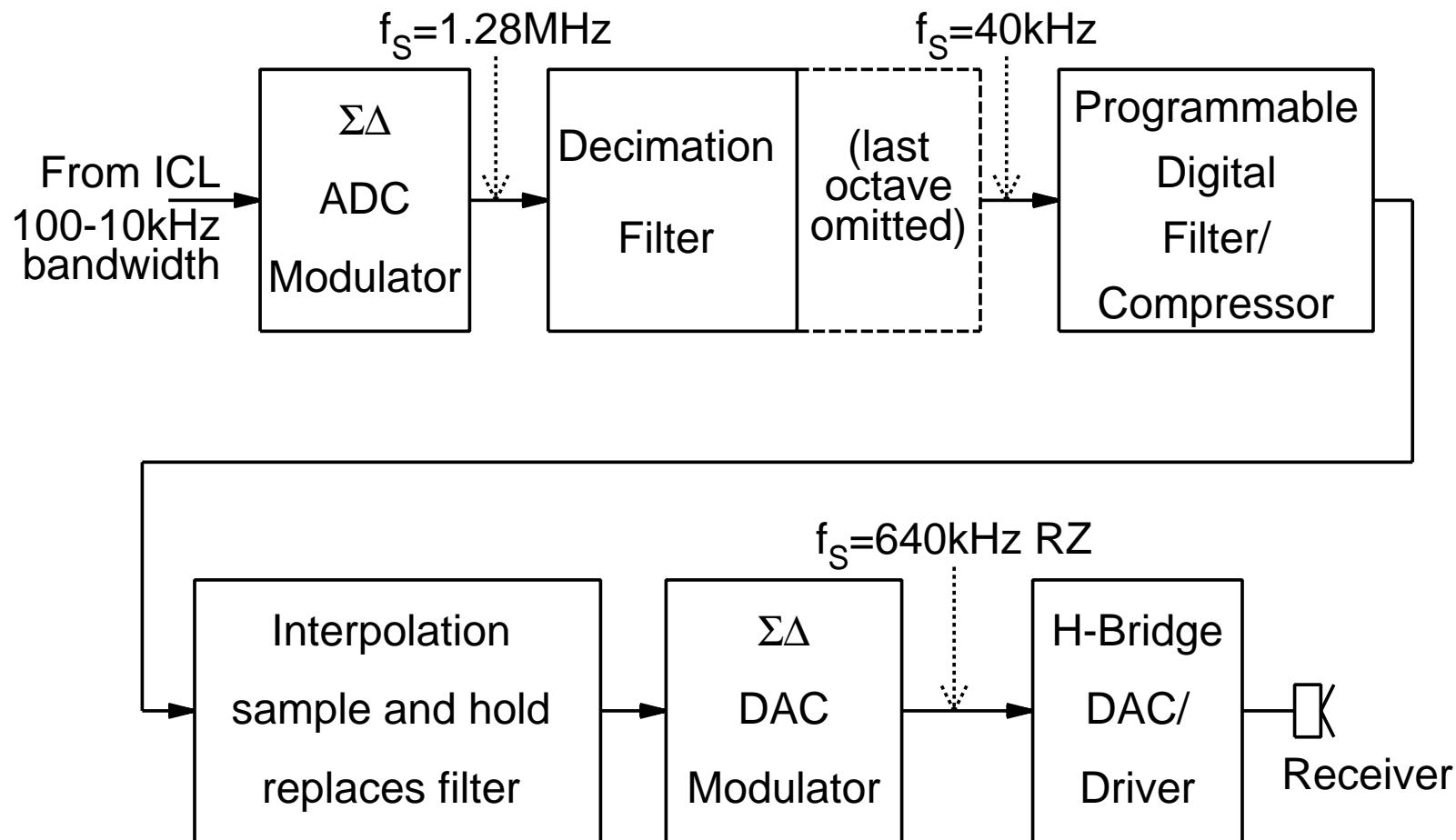
FIRST $\Sigma\Delta$ ADC INTEGRATOR



$\Sigma\Delta$ DAC AND H-BRIDGE TIMING



SAMPLING RATES FOR LOW POWER

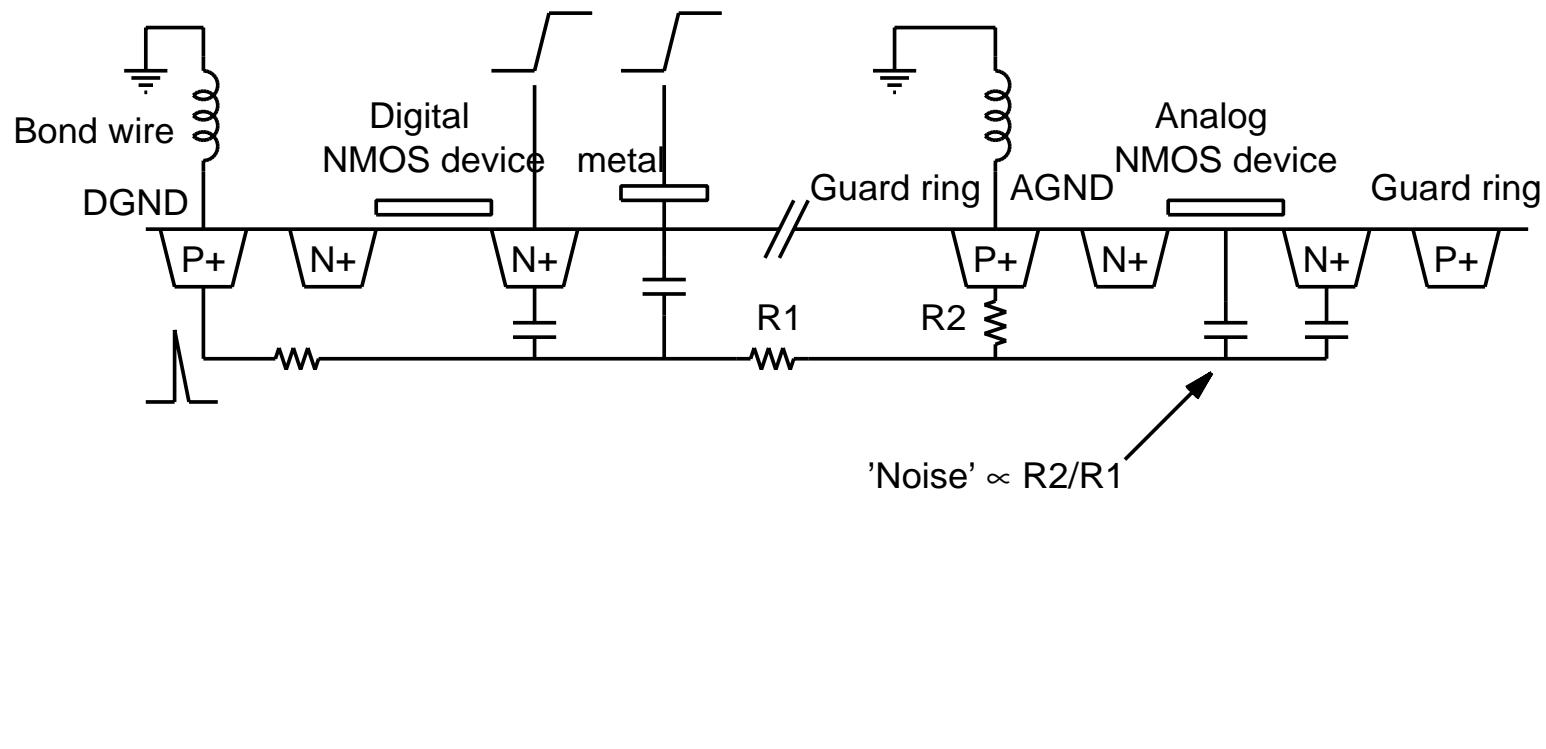


OUTLINE

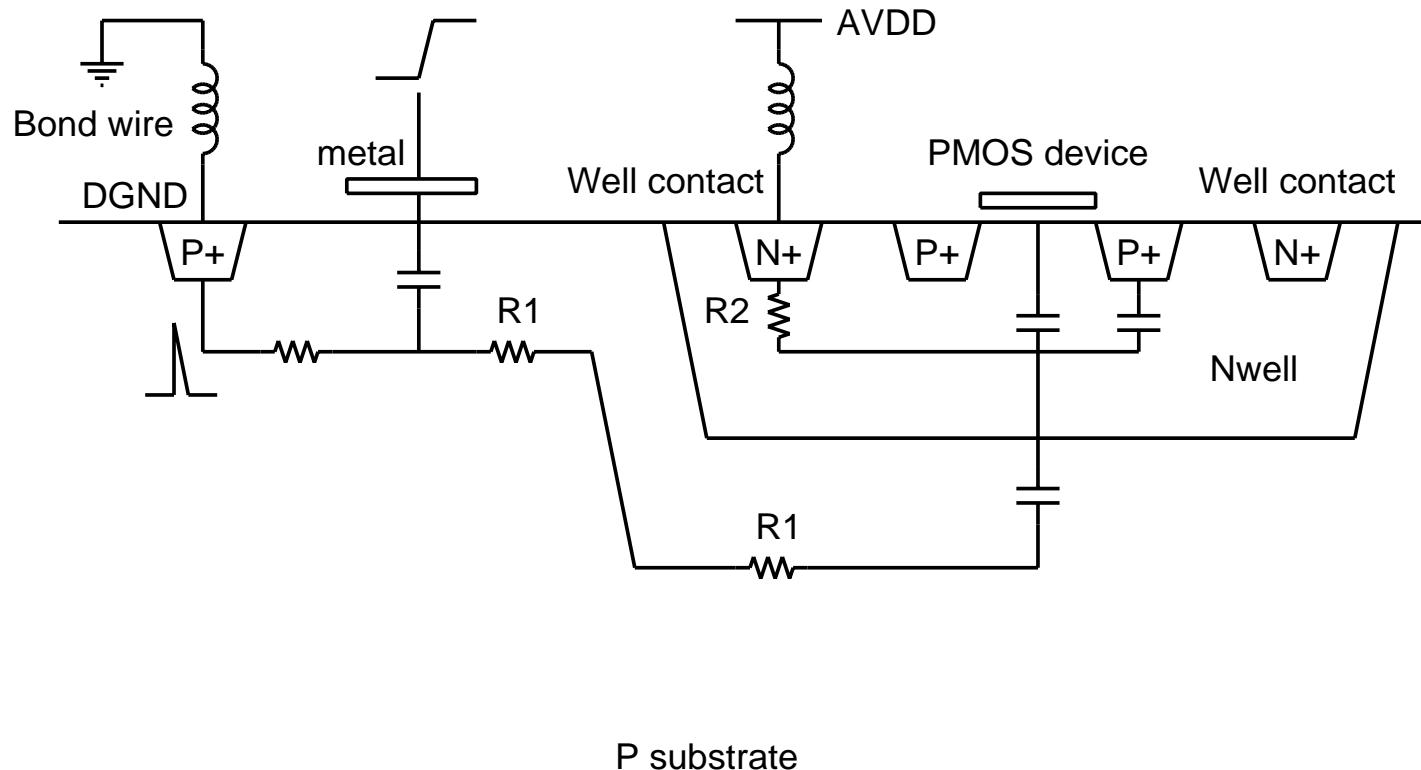
- Introduction
- Low supply voltage constraints
- Low power constraints
- **Common substrate constraints**
- Interconnect constraints

SUBSTRATE COUPLING TO ANALOG NMOS

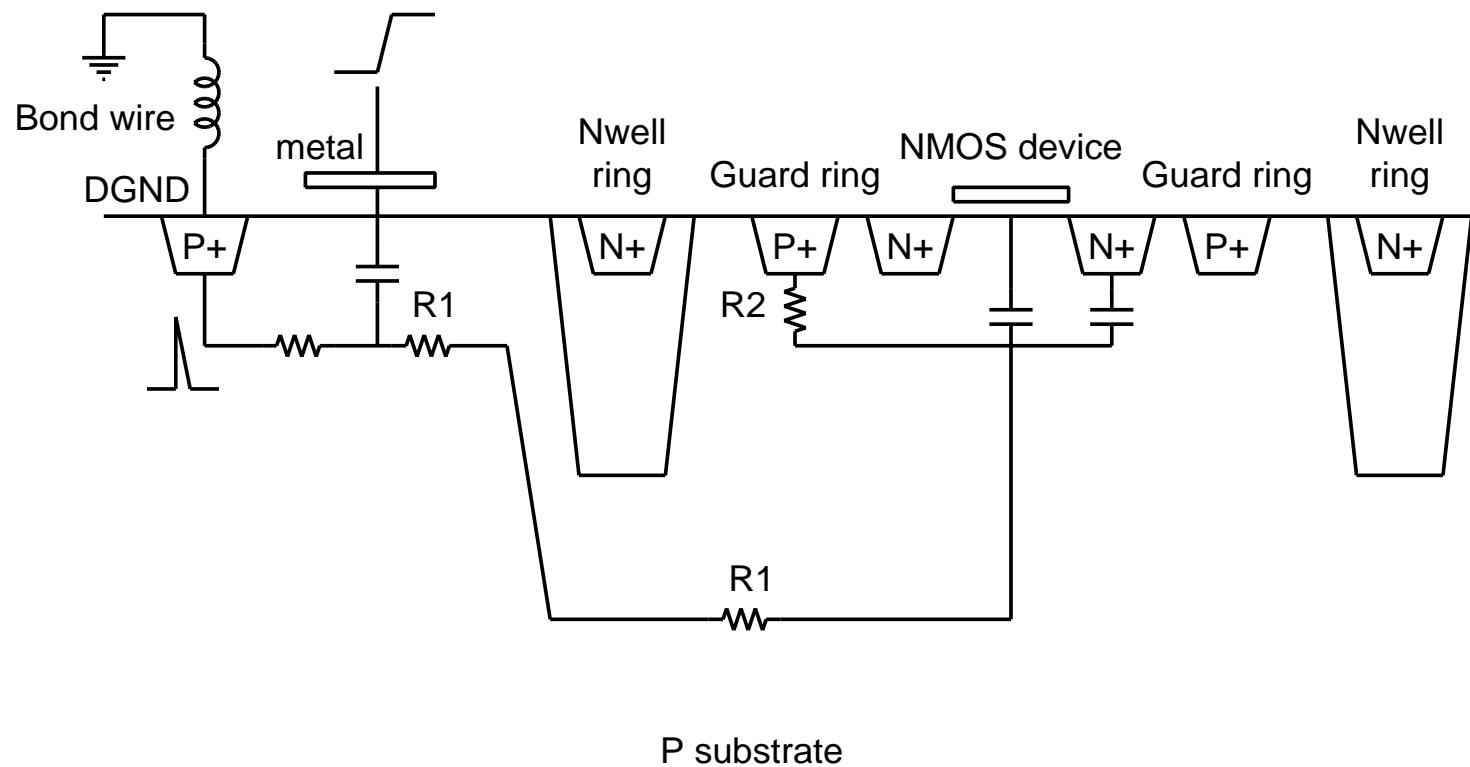
B. Haroun, M. Mahmoud, G. Gomez (T.I.)



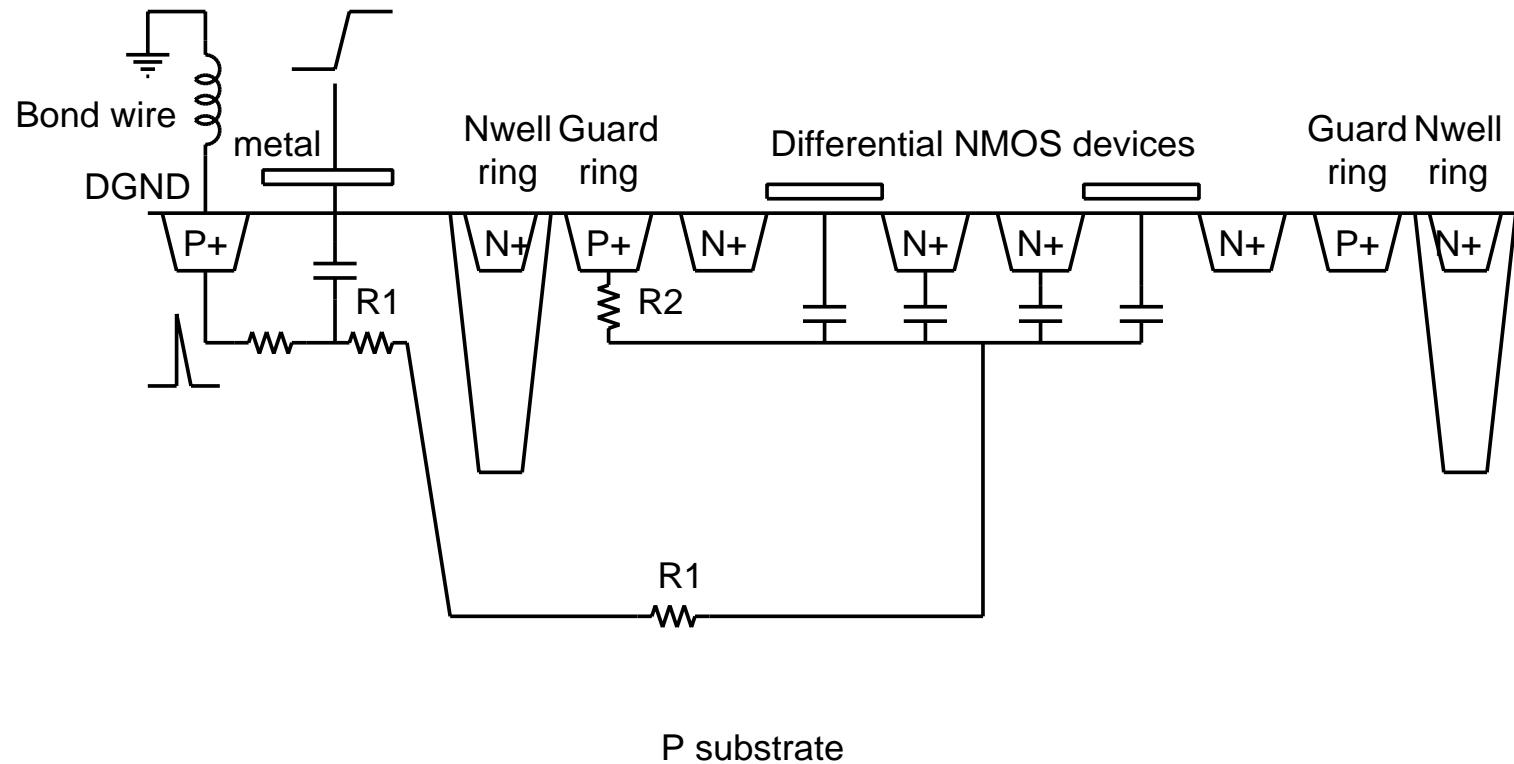
SUBSTRATE COUPLING TO ANALOG PMOS



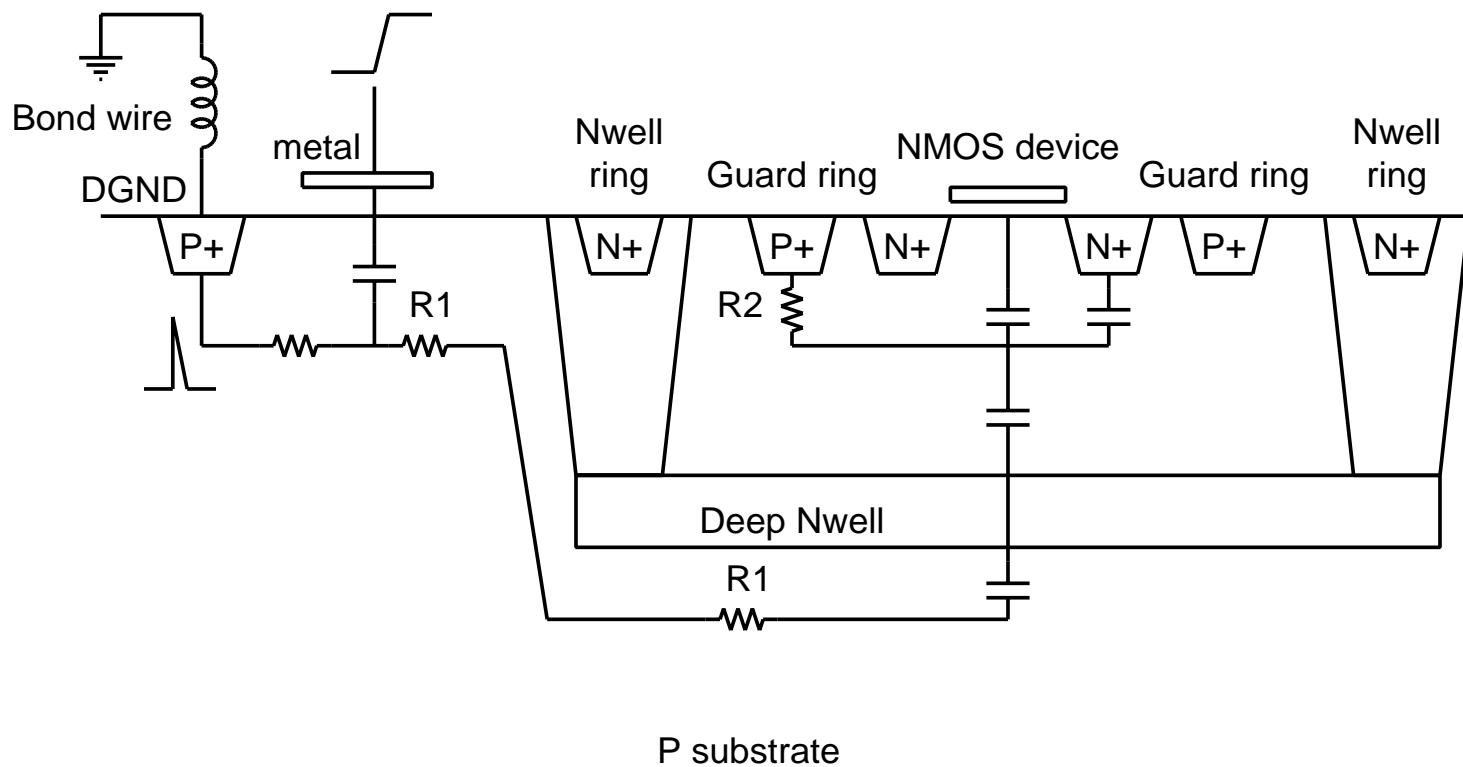
SUBSTRATE COUPLING WITH NWELL RING



DIFFERENTIAL SUBSTRATE COUPLING WITH NWELL RING



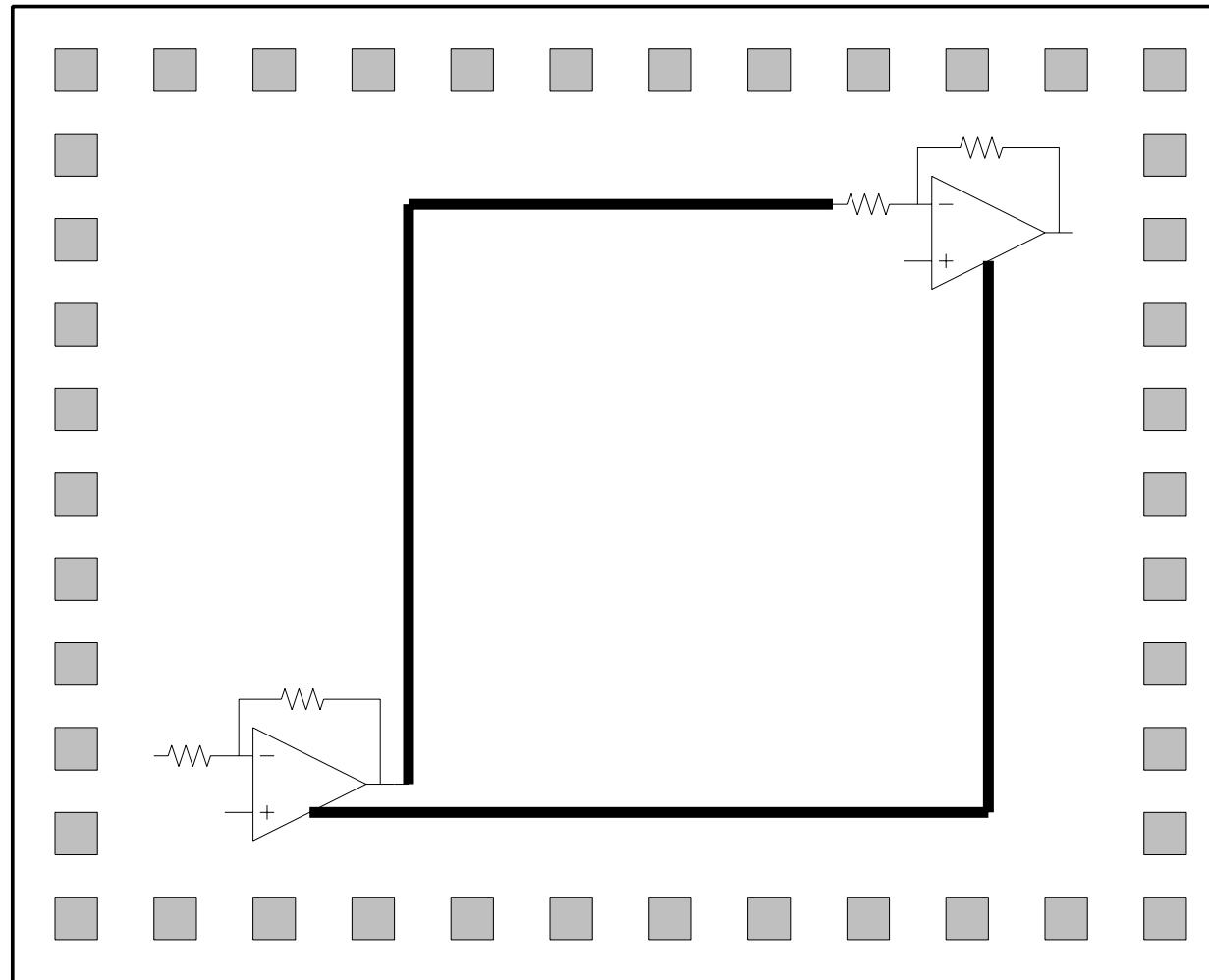
SUBSTRATE COUPLING WITH DEEP NWELL



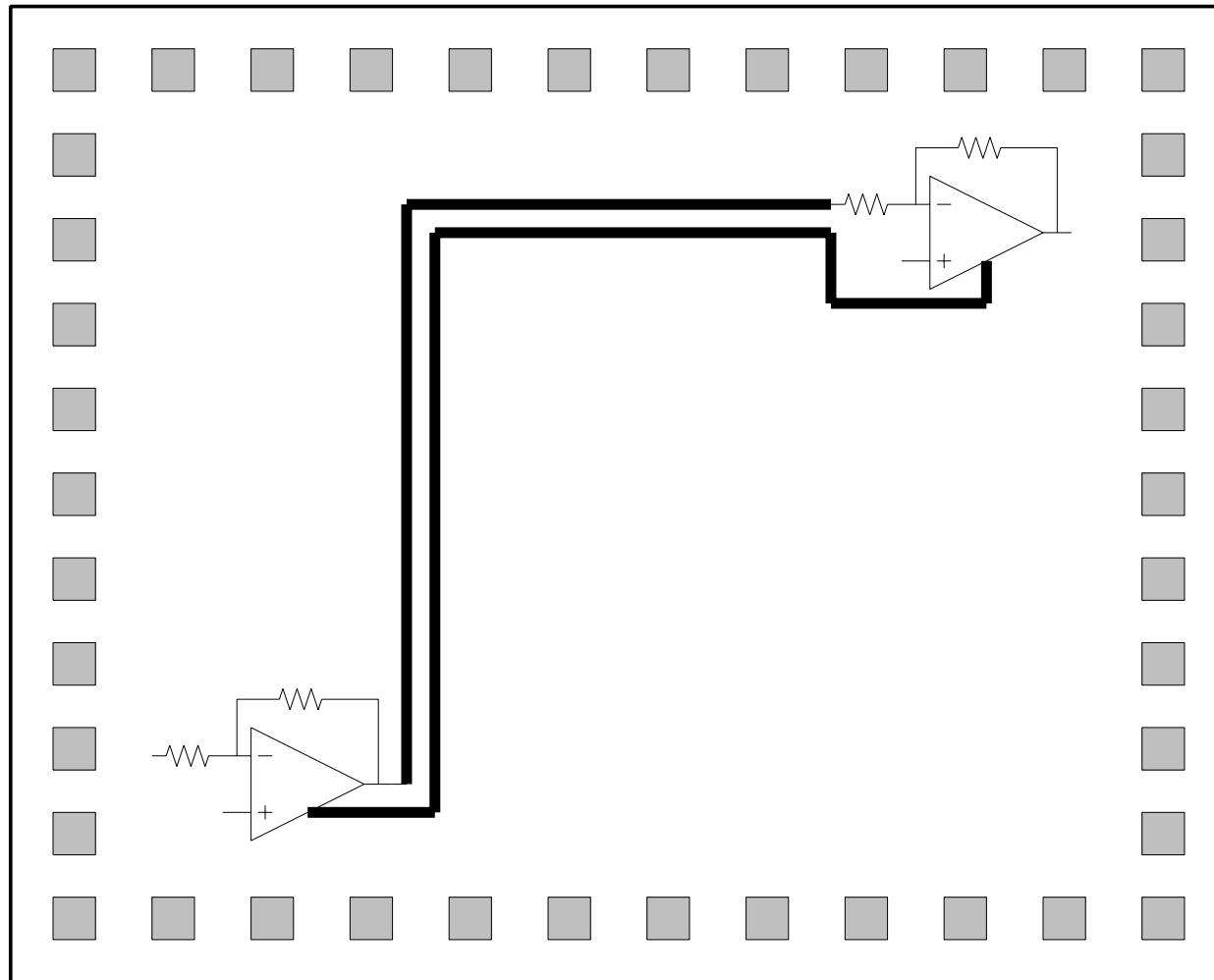
OUTLINE

- Introduction
- Low supply voltage constraints
- Low power constraints
- Common substrate constraints
- **Interconnect constraints**

INTERCONNECT INDUCTANCE



REROUTED INTERCONNECT FOR MINIMUM INDUCTANCE



REFERENCES AND FURTHER READING

Low voltage design

- R. J. Widlar, "Low voltage techniques", *IEEE Journal of Solid State Circuits*, Vol. SC-13, No. 6, pp. 838-846, December 1978.
- F. N. L. Op't eynde, P. F. M. Ampe, L. Verheyen and W. M. C. Sansen, "A CMOS large-swing low-distortion three-stage class AB power amplifier", *IEEE Journal of Solid State Circuits*, Vol. 25, No. 1, pp. 265-273, February 1990.
- R. G. H. Eschauzier, L. P. T. Kerklaan and J. H. Huisink, "A 100-MHz 100-dB operational amplifier with multipath nested Miller compensation structure", *IEEE Journal of Solid State Circuits*, Vol. 27, No. 12, pp. 1709-1717, December 1992.
- R. G. H. Eschauzier and J. H. Huisink, "An operational amplifier with multipath Miller zero cancellation for RHP zero removal", *Proceedings of the ESSCIRC*, 1993.
- S. Pernici, G. Nicollini and R. Castello, "A CMOS low-distortion power amplifier with double nested Miller compensation", *IEEE Journal of Solid State Circuits*, Vol. 28, No. 7, pp. 758-763, July 1993.
- R. G. H. Eschauzier, R. Hogervorst and J. H. Huisink, "A programmable 1.5V CMOS class-AB operational amplifier with hybrid nested Miller compensation for 120 dB gain and 6 MHz UGF", *IEEE Journal of Solid State Circuits*, Vol. 29, No. 12, pp. 1497-1504, December 1994.

REFERENCES AND FURTHER READING (continued)

- R. G. H. Eschauzier and J. H. Huisings, *Frequency Compensation Techniques for Low-Power Operational Amplifiers*, Kluwer Academic Publishers, Boston, 1995.
- K.-J. de Langen, R. G. H. Eschauzier, G. J. A. van Dijk and J. H. Huisings, "A 1 GHz bipolar class-AB operational amplifier with multipath nested Miller compensation for 76 dB gain", *IEEE Journal of Solid State Circuits*, Vol. 32, No. 4, pp. 488-498, April 1997.
- Fan You, S. H. K. Embabi and E. Sanchez-Sinencio, "Multistage amplifier topologies with nested G_m -C compensation", *IEEE Journal of Solid State Circuits*, Vol. 32, No. 12, pp. 2000-2011, December 1997.
- R. M. Ziazadeh, H.-T. Ng and D. J. Allstot, "A multistage amplifier topology with embedded tracking compensation", *Proc. IEEE 1998 Custom Integrated Circuits Conference*, pp.361-364.
- G. Palumbo and S. Pennisi, "Design methodology and advances in nested-Miller compensation," *IEEE Trans. on Circuits and Systems - I*, vol. 49, no. 7, pp. 893-903, July 2002.
- K. Leung and P. Mok, "Analysis of multistage amplifier-frequency compensation," *IEEE Trans. on Circuits and Systems - I*, vol. 48, no. 9, pp. 1041-1056, September 2001.

REFERENCES AND FURTHER READING (continued)

Low voltage switched capacitor design

T. B. Cho and P. R. Gray, "A 10b, 20 Msample/s, 35 mW pipeline A/D converter," *IEEE Journal of Solid-State Circuits*, vol. 30, no. 3, pp. 166-172, March 1995.

A. Abo and P. R. Gray, "A 1.5V, 10b, 14.3 MS/s, CMOS pipeline analog-to-digital converter," *IEEE J. of Solid-State Circuits*, vol. 34, no. 5, pp. 599-606, May 1999

J. Crols and M. Steyaert, "Switched-opamp: an approach to realize full CMOS switched-capacitor circuits at very low power supply voltages," *IEEE Journal of Solid State Circuits*, vol. 29, No. 8, pp. 936-942, August 1994.

V. Peluso, P. Vancorenland, A. Marques, M. Steyaert and W. Sansen, "A 900-mV low-power $\Delta\Sigma$ A/D converter with 77-dB dynamic range," *IEEE Journal of Solid State Circuits*, vol. 33, No. 12, pp. 1887-1897, December 1998.

A. Baschirotto and R. Castello, "A 1-V 1.8MHz CMOS switched-opamp SC filter with rail-to-rail output swing," *IEEE Journal of Solid State Circuits*, Vol. SC-32, No. 12, pp. 1979-1986, December 1997.

A. Baschirotto, "A low-voltage sample-and-hold circuit in standard CMOS technology operating at 40Ms/s," *IEEE Trans. on Circuits and Systems - II*, Vol. 48, No. 4, pp. 394-399, April 2001.

REFERENCES AND FURTHER READING (continued)

E. Bidari, et al., "Low-voltage switched capacitor circuits", *Proc. IEEE Int. Symposium on Circuits and Systems*, May 1999.

D.-Y. Chang, L. Wu, U.-K. Moon, "Low-voltage pipelined ADC using opamp-reset switching technique", *Proc. IEEE 2002 Custom Integrated Circuits Conference*, pp.461-464.

Z. Gunay, E. Soenen, S. Embabi, E. Sanchez-Sinencio, "A 1.8V pseudo-differential switched-capacitor amplifier", *Proc. IEEE 1998 Custom Integrated Circuits Conference*, pp.373-376.

F. Chen, et al., "A 1.5V 1mA 72dB passive $\Sigma\Delta$ ADC for a GSM tranceiver in $0.13\mu\text{m}$ digital CMOS", *Int. Solid State Circuits Conference Digest of technical papers*, Feb. 2003, paper 3.1.

H. Banba, et al., "A CMOS bandgap reference circuit with sub 1V operation", *IEEE 1998 Symposium on VLSI Circuits Digest of Technical Papers*, pp.228-229.

Low power design

M. Degrauwe, J. Rijmenants, E. Vittoz and H. de Man, "Adaptive biasing CMOS amplifiers," *IEEE Journal of Solid State Circuits*, Vol. SC-17, No. 3, pp. 522-528, June 1982.

REFERENCES AND FURTHER READING (continued)

F. You, S. Embabi and E. Sanchez-Sinencio, "Low-voltage class AB buffers with quiescent current control," *IEEE Journal of Solid State Circuits*, Vol. SC-33, No. 6, pp. 915-920, June 1998.

D. Kasha, W. Lee and A. Thomsen, "A 16-mW, 120-dB linear switched-capacitor delta-sigma modulator with dynamic biasing," *IEEE Journal of Solid State Circuits*, Vol. SC-34, No. 7, pp. 921-926, July 1999.

P. Cusinato, F. Stefani and A. Baschirotto, "Reducing the power consumption in high-speed SD bandpass modulators," *IEEE Trans. on Circuits and Systems - II*, Vol. 48, No. 10, pp. 952-960, October 2001.

Y. P. Tsividis, "Integrated continuous-time filter design - an overview," *IEEE Journal of Solid-State Circuits*, vol. 29, pp. 166-176, March 1994.

R. Schreier and B. Zhang, "Delta-sigma modulators employing continuous-time circuitry," *IEEE Trans. on Circuits and Systems - I*, vol. 44, no. 4, pp. 324-332, April 1996.

E. J. van der Zwan and E. C. Dijkmans, "A 0.2-mW CMOS sigma-delta modulator for speech coding with 80dB dynamic range," *IEEE Journal of Solid-State Circuits*, vol. 31, pp. 1873-1880, December 1996.

REFERENCES AND FURTHER READING (continued)

K. Nagaraj, "A 250mW, 8b, 52Msample/s parallel-pipelined A/D converter with reduced number of amplifiers", *IEEE Journal of Solid-State Circuits*, vol. 32, no. 3, pp. 312-320, March 1997.

J. Fattaruso, et al., "Analog processing circuits for a 1.1V 270uA mixed-signal hearing aid chip.", *Int. Solid State Circuits Conference Digest of technical papers*, Feb. 2002, paper 23.3, page 384.

Substrate coupling

R. Gharpurey and R. G. Meyer, "Modeling and analysis of substrate coupling in integrated circuits," *IEEE Journal of Solid State Circuits*, Vol. SC-31, No. 3, pp. 344-353, March 1996.

J. Briaire and K. S. Krisch, "Principles of Substrate Crosstalk Generation in CMOS Circuits", *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems*, vol. 19, n. 6, pp. 645-653, June 2000.

B.R. Stanisic, N.K. Verghese, R.A. Rutenbar, L.R. Carley and David J. Allstot, "Addressing substrate coupling in mixed-mode ICs: simulation and power distribution synthesis", *IEEE Journal of Soild State Circuits*, vol. 29, n. 3, pp. 226-238, March 1994.

S. Mitra, R.A. Rutenbar, L.R. Carley, D.J. Allstot, "A methodology for rapid estimation of substrate-coupled switching noise", *Proc. IEEE 1995 Custom Integrated Circuits Conference*

REFERENCES AND FURTHER READING (continued)

F.J.R Clement, E. Zysman, M. Kayal, M. Declercq, "LAYIN: Toward a Global Solution for Parasitic Coupling Modeling and Visualization", *Proc. IEEE 1994 Custom Integrated Circuits Conference*

N. Verghese and D.J. Allstot, "Verification of RF and mixed-signal integrated circuits for substrate coupling effects", *Proc. IEEE 1997 Custom Integrated Circuits Conference*

Nishath K. Verghese and David J. Allstot, "Computer-Aided Design Considerations for Mixed-Signal Coupling in RF Integrated Circuits", *IEEE Journal of Solid State Circuits*, vol. 33, n. 3, pp. 314-323, March 1998.

A.M. Niknejad, R. Gharpurey, R.G. Meyer, "Numerically stable Green function for modeling and analysis of substrate coupling in integrated circuits", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 17, n. 4, pp. 305-315, April 1998.

T. Smedes, N.P. van der Meijjs and A.J. van Genderen, "Extraction of circuit models for substrate cross-talk", 1995 International Conference on Computer-Aided Design.

A. Samavedam, A. Sadate, K. Mayaram and T.S. Fiez, "A scalable substrate noise coupling model for design of mixed-signal ICs", *IEEE Journal of Solid State Circuits*, vol. 35, n. 6, pp. 895 -904, June 2000.

REFERENCES AND FURTHER READING (continued)

M. Mahmoud, B. Haroun, M. Elmasry, "A quantitative analysis of substrate noise isolation techniques." *To be published.*

Interconnect inductance

H. M. Greenhouse, "Design of planar microelectronic inductors," *IEEE Trans. Parts, Hybrids and Packaging*, Vol. PHP-10, no. 2, pp. 101-109, June 1974.

Y. Massoud and Y. Ismail, "Grasping the impact of on-chip inductance", *IEEE Circuits and Devices Magazine*, July 2001, pp 14-21.