An IC Design Perspective "Why Would We Choose Flip Chip"

Scott Wood

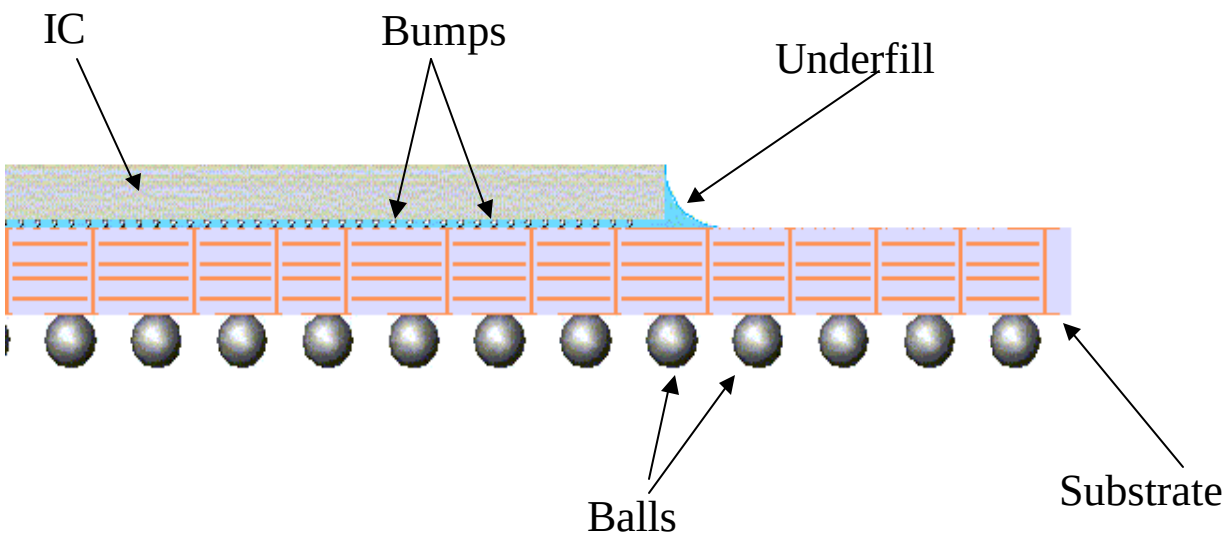
ISQED 2003

Outline

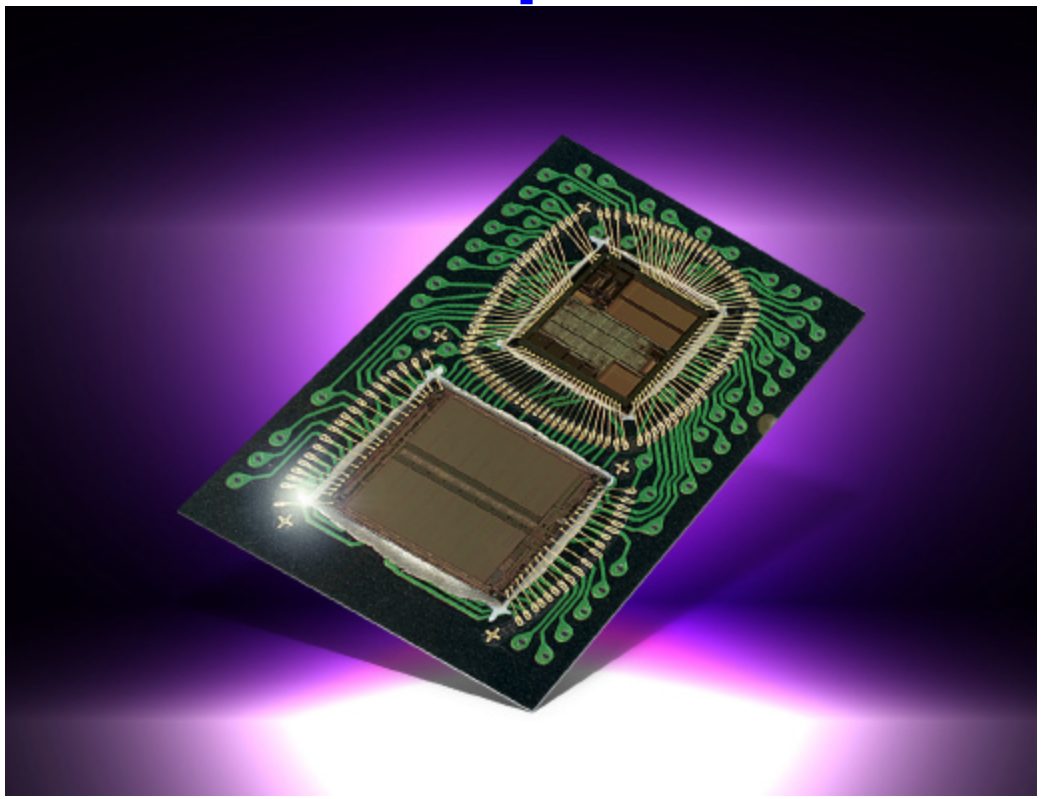
- What is Flip Chip?
- Why Choose Flip Chip?
- Design Requirements that Drive to Flip Chip
- Tradeoffs in Flip Chip
- CAD Problems to be Solved

What is Flip Chip?

Flip-chip Cross-section

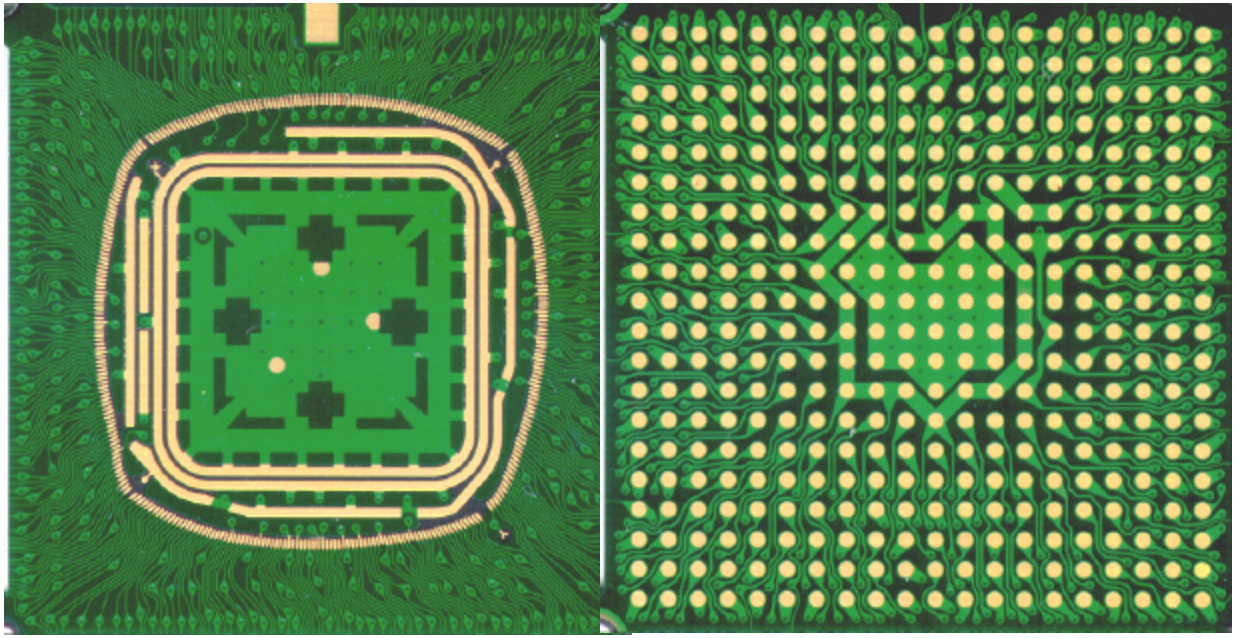


Example: AB58

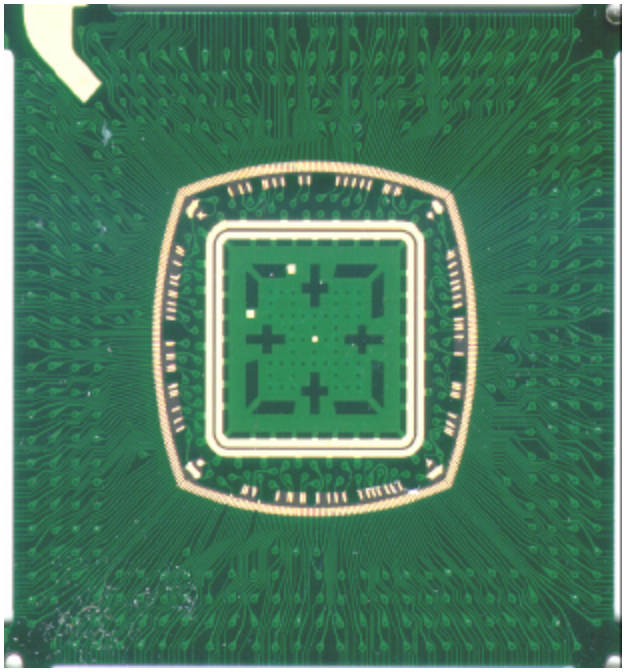


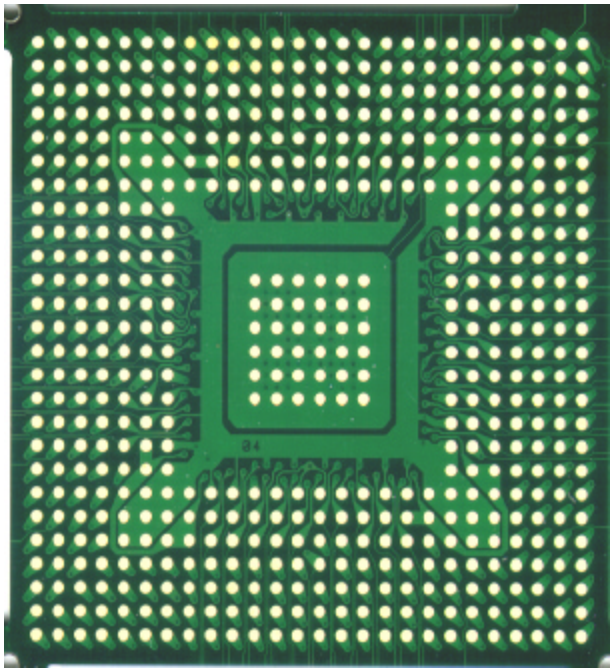
IC and pinout optimized to minimize size 12x16 mm

Example: Graphics IC



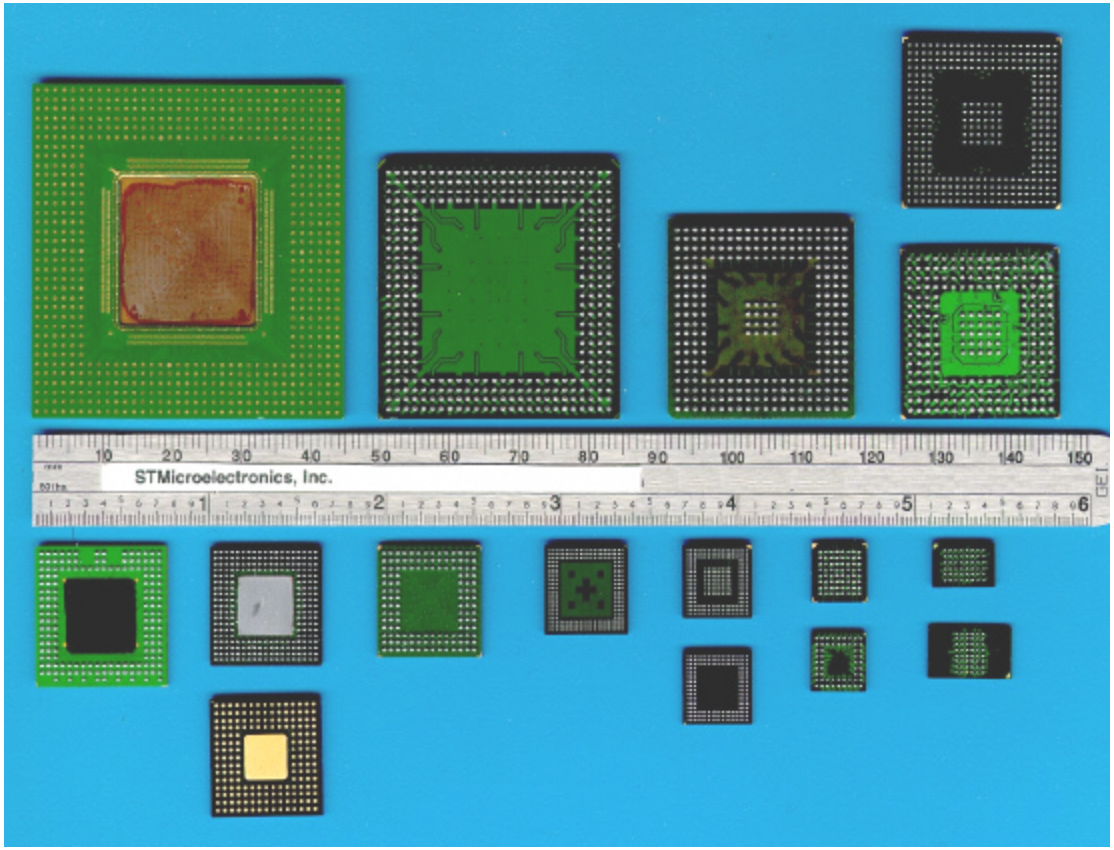
Example: Set-top Box IC





432 signals, 636 bondwires

BGA

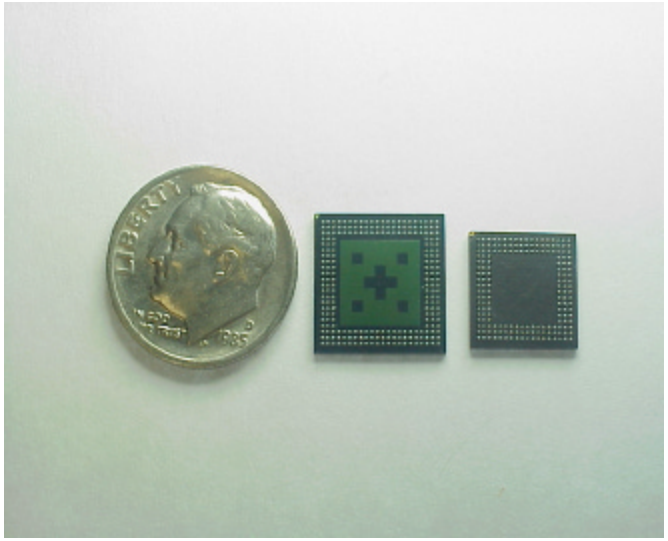


Large BGAs

622 Mb/sec data switch

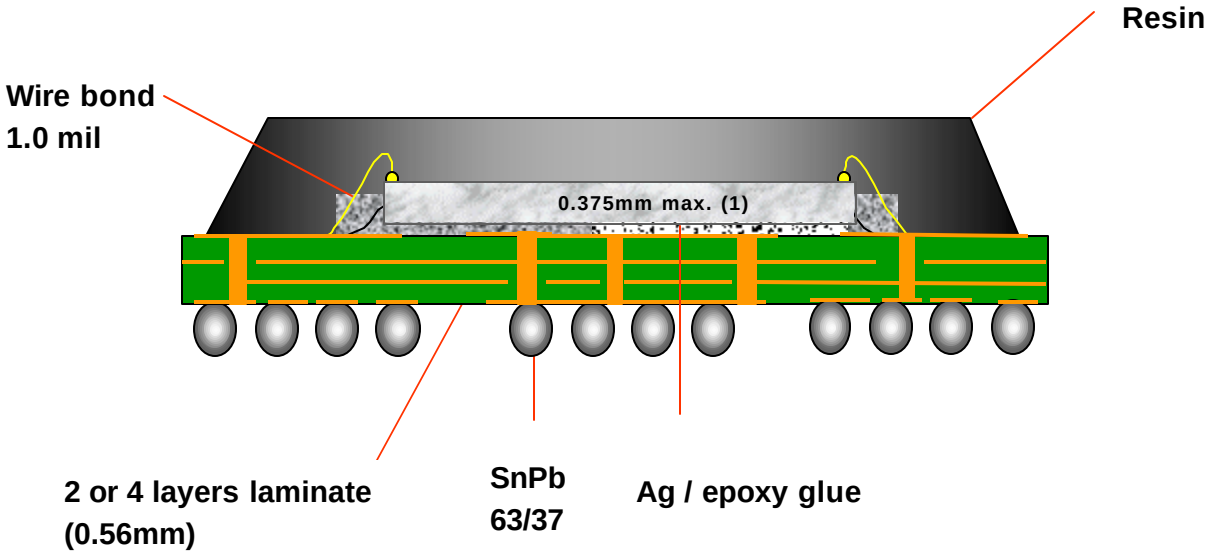
703 bondwires
696 balls

Small BGA

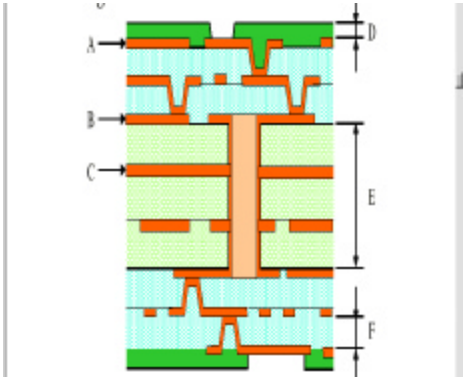


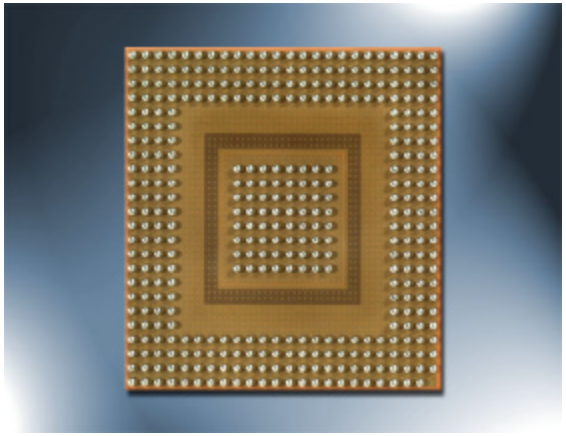
- Very small
- Very inexpensive
- Many applications

Wirebond PBGA Cross-section



FlipChip BGA (Organic Build-up)

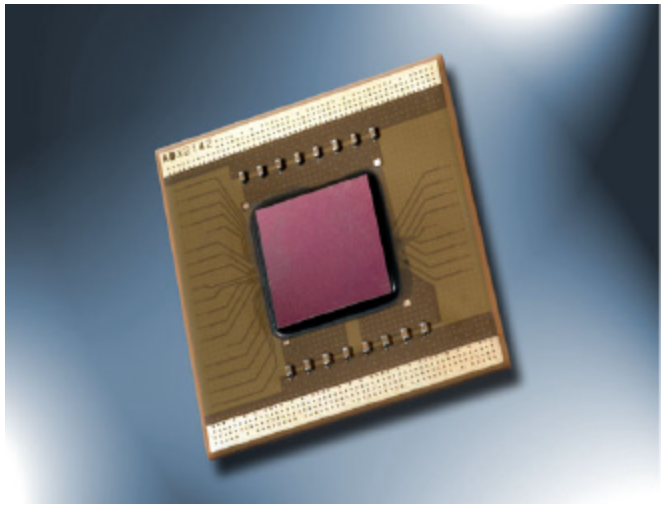




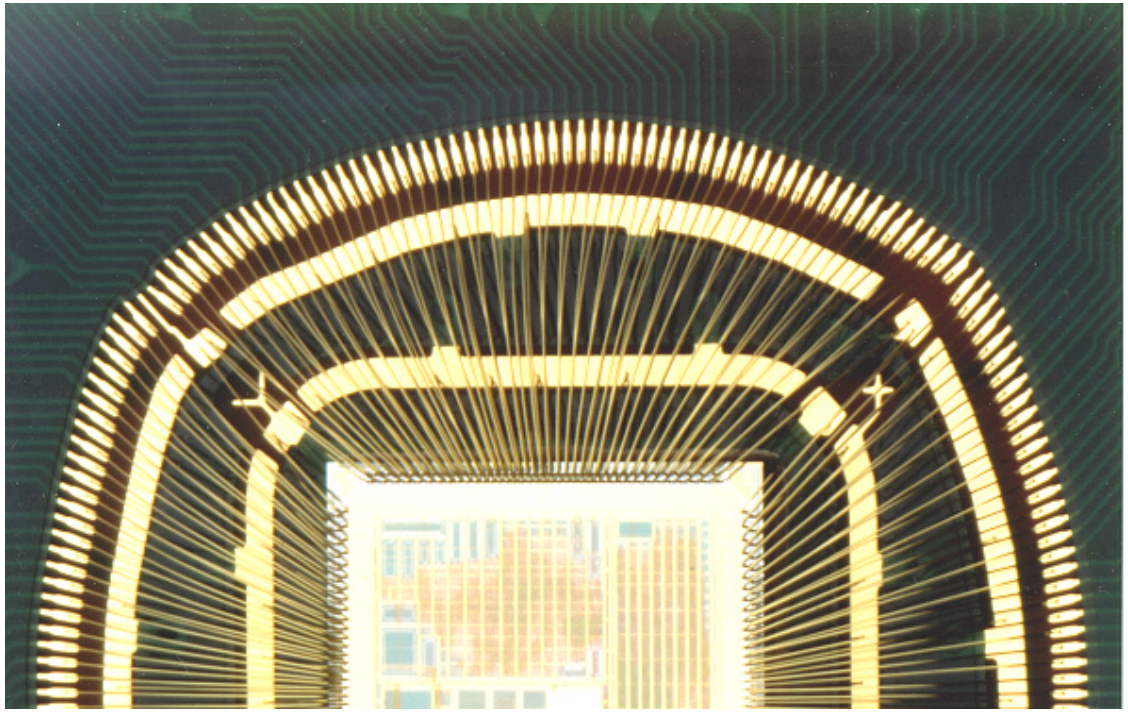
- High density layers over low density core
- 2 to 10 metal layers
- Organic dielectrics (BT epoxy, BCB, PTFE)
- Cu metallization
- Medium to high cost
- 15 to 50 mm sizes
- 1.27, 1.0, 0.8 mm pitch
- Ball count >1500
- Optional metal lid

Why Flipchip in Package?

- The package is the bridge between the IC and the application:
  - Protection
  - Testability
  - Reduce PCB complexity
  - Enhance electrical
  - Enhance thermal



Wirebonding



Advantages

- BGA is very adaptable to application by correct design of substrate
- BGA is very adaptable to low-cost high-volume manufacturing – for the IC vendor and for the user
- Standard tooling can be used – ball pattern, handling, assembly, molding, etc.
- Optimized package can be had with minimum impact on cost and manufacturing.

Why Choose Flip Chip?

Reasons to use FlipChip

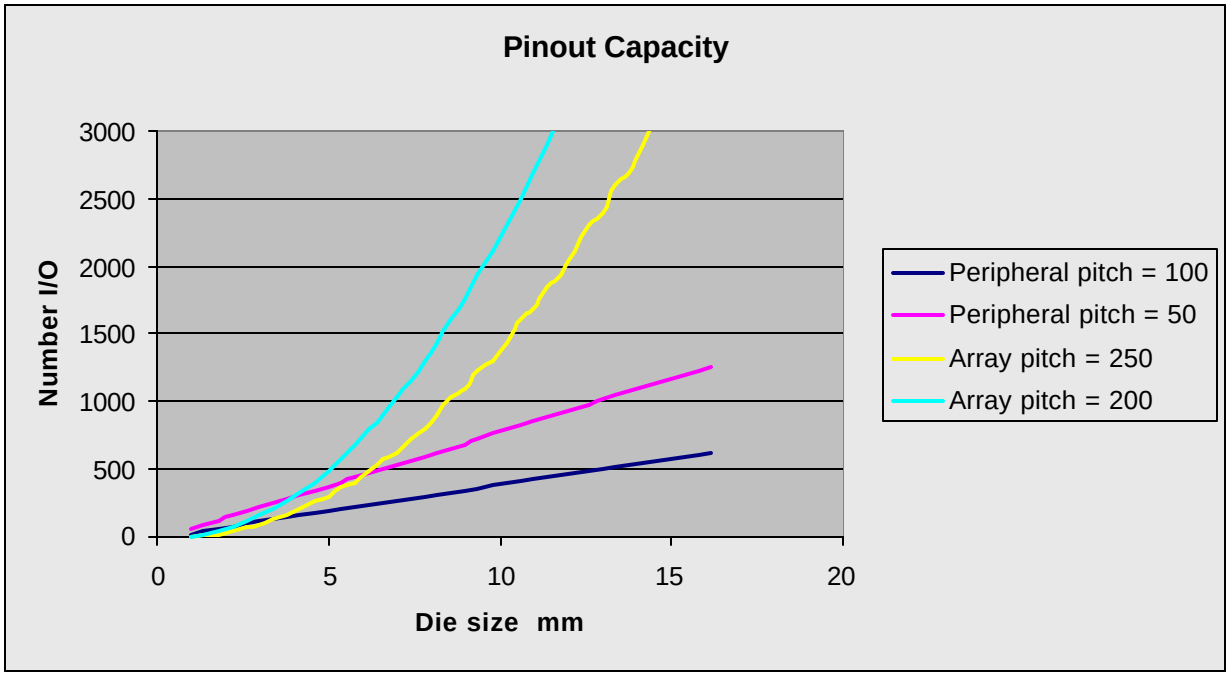
- I/O count
- Performance
- Power dissipation
- I/O density
- IC size
- Cost
- Manufacturing

But careful design is required!

Considerations for 1000+ I/O

- MUST be BGA
- MUST be flip chip
- Multilayer package substrate required (4-10L)
- Material choice depends on many factors – customer preference, signal integrity, cost, etc
- Substrate design WILL be custom

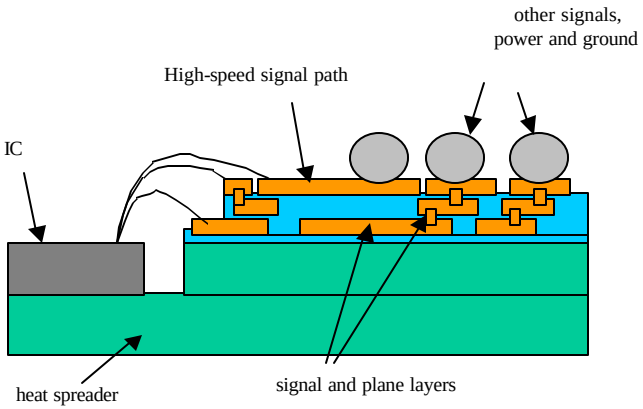
Flipchip vs Wirebond – I/Os

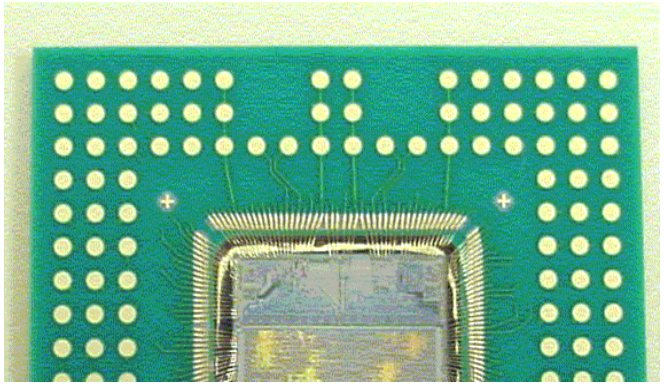


Flipchip Basic Limits

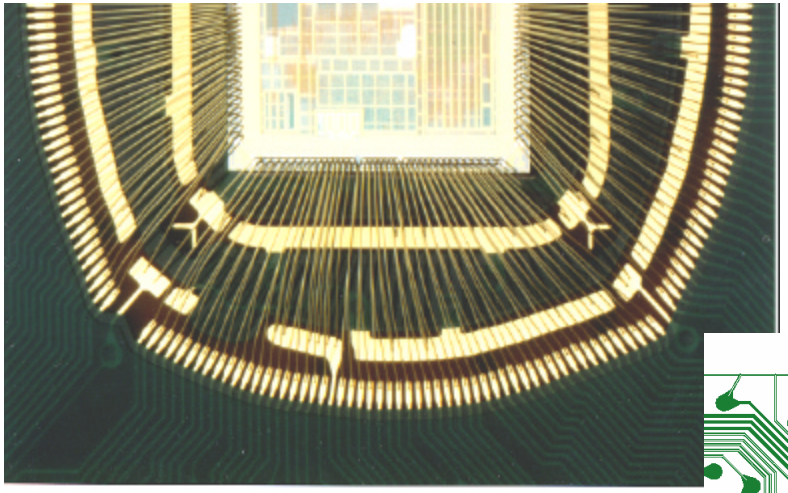
- Bump height strongly affects assembly – especially time and cost of the underfill process
  - Smaller height means increased cost
- Bump height and IC size strongly affect reliability
  - Stress is generated by mismatch in thermal expansion
  - Smaller bump increases stress
  - Larger IC increases stress
  - Max IC size depends on substrate and bump height
  - Desired bump height typically 100 to 125μ

Example: Design for high speed

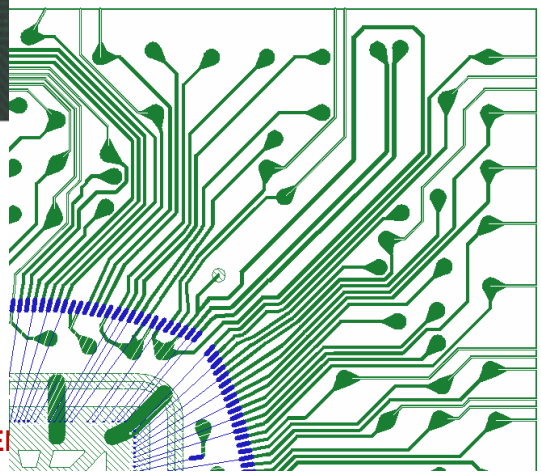




Design Flexibility

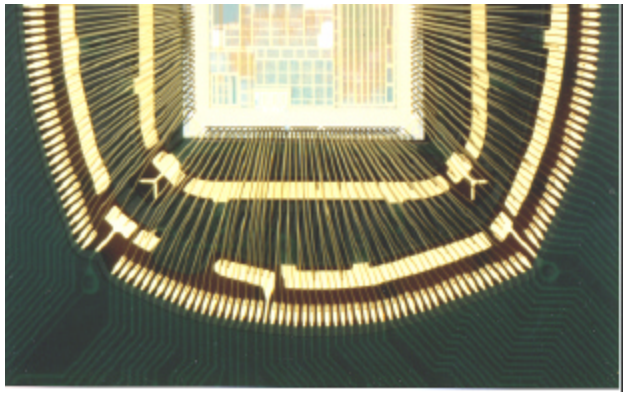


Multiple power/ground
Flexible bondfinger location
Analog signals
Shielding
Isolation
Control impedance if needed

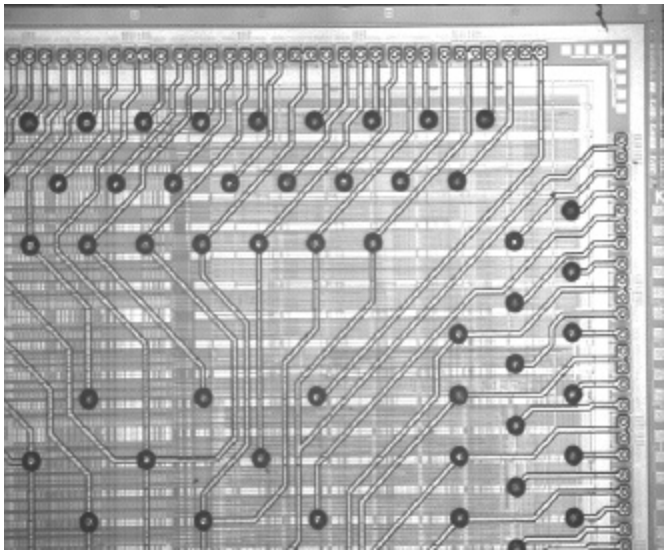


Flipchip Design issues: Power/Ground

- In W/B, multiple P/G are handled with multiple segmented bonding rings
- In F/C we will need more vias and probably more layers
- Substrate will be more complex, this complexity controlled by IC/package trade-offs
- Complexity = cost



I/O, power/ground schemes

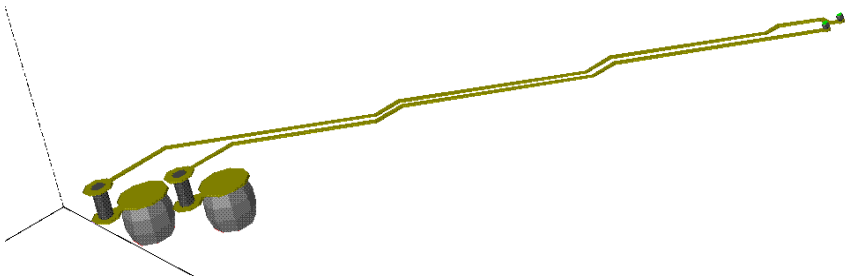


- Signals on the outside, power/ground on the inside -- more dense outside, less dense inside
- Easier routing on package
- Easier probe
- Easier assembly

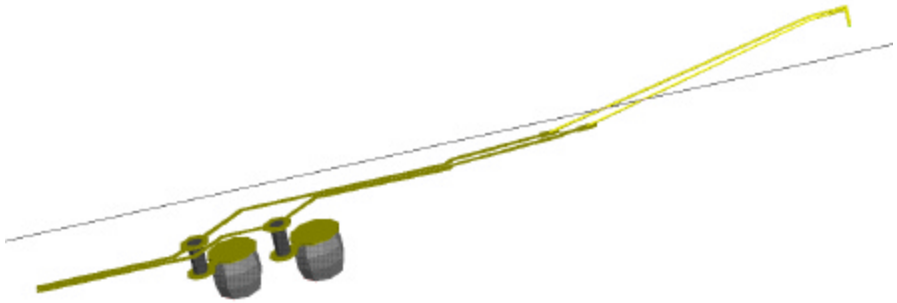
- *But don't get locked in:*
  - *Not always adequate*
  - *Closely tied to IC design*
  - *Acceptable paths through package?*

Signal traces – total path length is still the same!

Electrical Performance



Ls = 14nH
Lm = 7.5 nH
C = .78 pF



Ls = 13.1 nH
Lm = 7.2 nH
C = .92 pF

Note plating traces in W/B case

Tradeoffs in Flip Chip

Flipchip Design Issues: Routing

- Multiple rows of signal bumps on IC must escape on package substrate
- Trade-off is IC signal density vs. substrate cost and complexity

  (Substrate via size, trace size, layers)

Flipchip Design Issues

- High density routing capability is needed on the package substrate in the bump escape area, but nowhere else
- In wirebond parts, the wires take up most of the translation from IC pitch to substrate pitch.

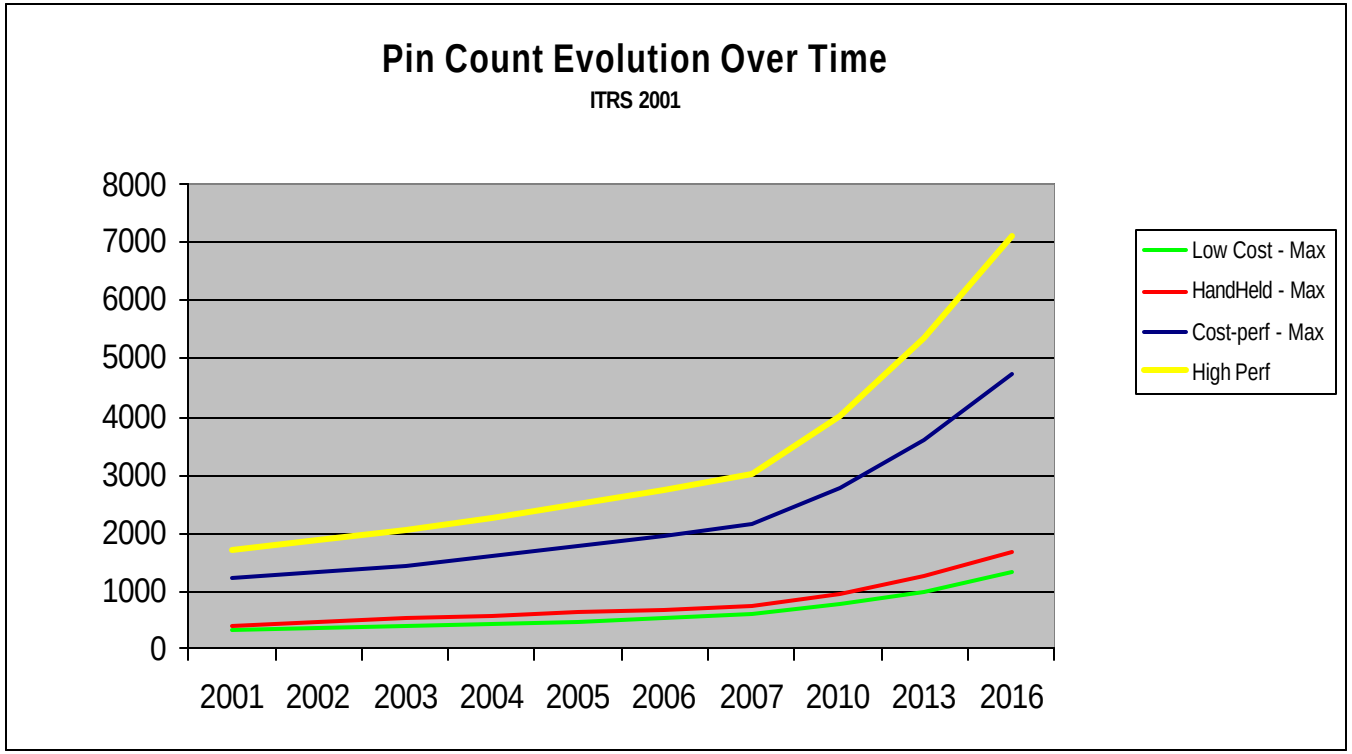
BGA Applications and Design

- BGA is the only practical package choice for high I/O (200+) designs
- In the BGA world, 95+% of chips require a custom design
- In high-speed, high I/O arena this becomes 100%

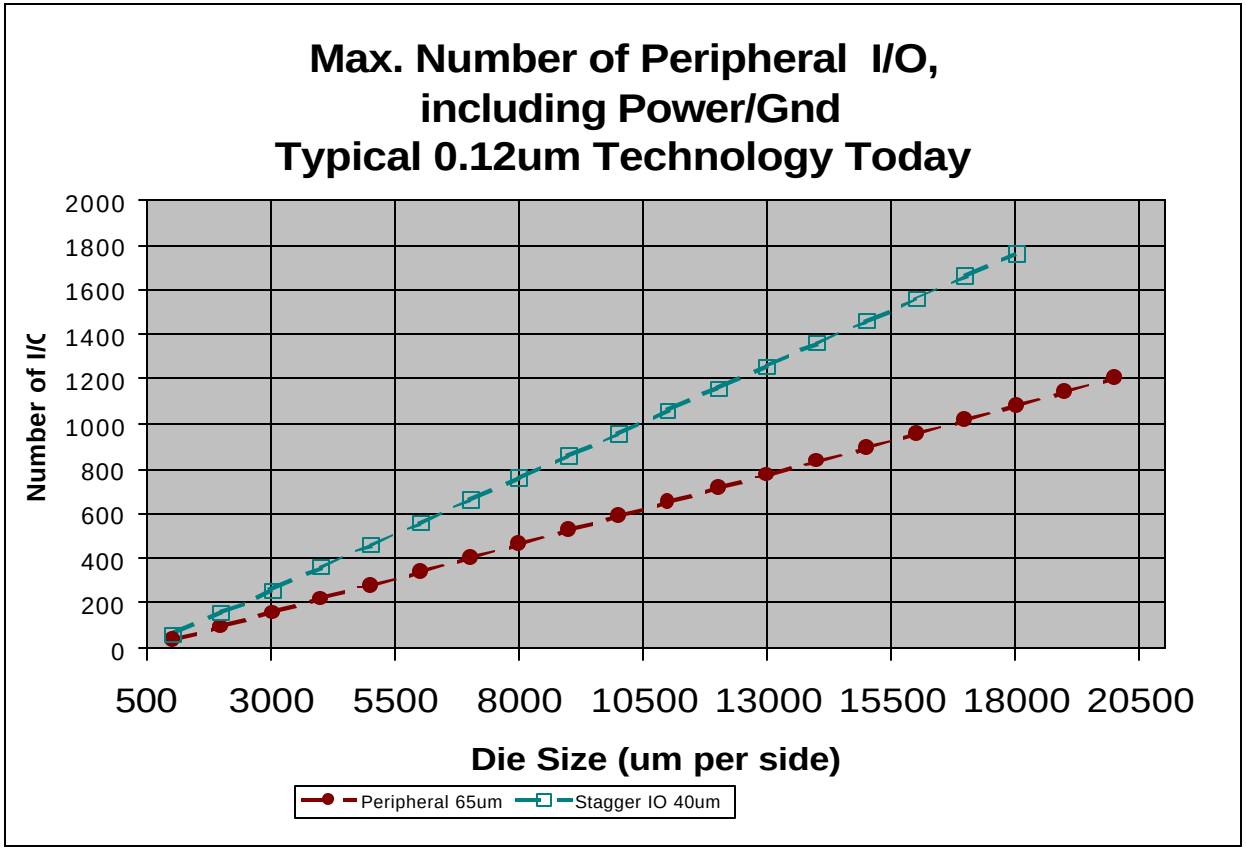
Design Requirements that Drive to Flip Chip

- Large numbers of IO (>1200)
- Large numbers of Power/Gnd connections (>1200)
- High Performance Packaging (high speed, low inductance)
- High Power Consumption (40-60+ watts)
- Nominal Die Size (~13mm/side for ~2400 I/O + Power/Gnd + >8 Million Gates Logic + Memory)
- Multiple Power Supplies Separated on Chip (IO and Core)

Increasing Pin Counts



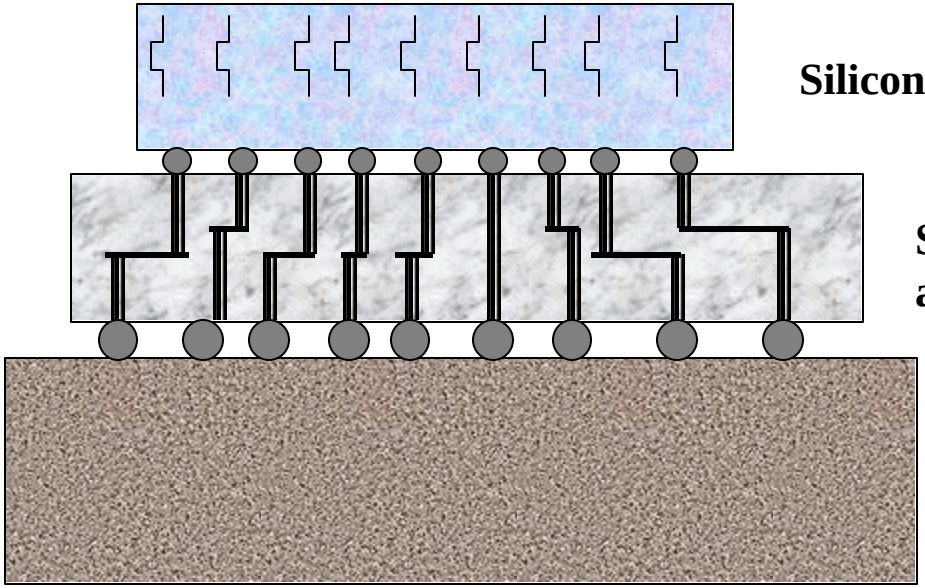
Today's Capability



Design Concerns with Flip Chip

- PCB/Ball Constraints
- Substrate Constraints
- Bump Constraints
- Silicon Constraints

Flip Chip Cross Section

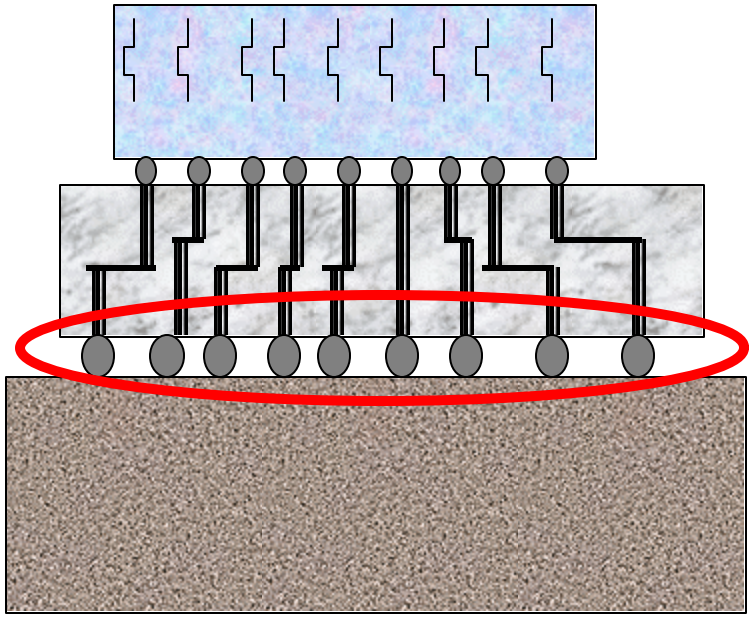


Silicon /Bumps – defined by layout

Substrate- defined by layout and PCB

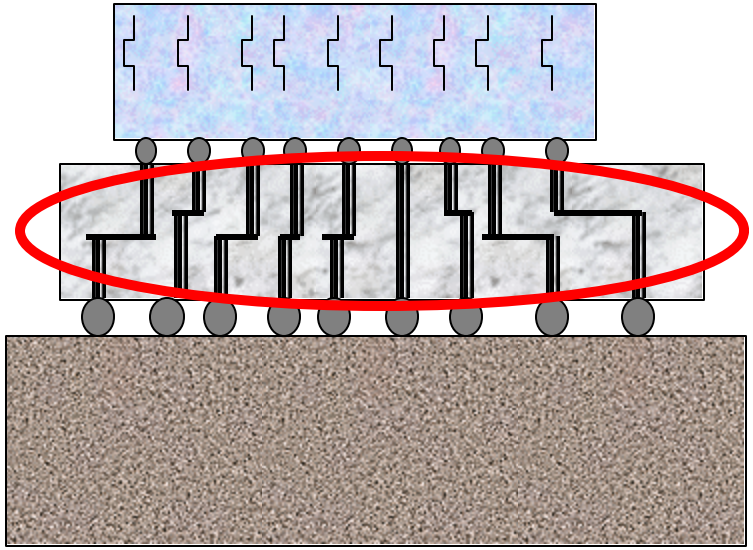
Balls/PCB – defined by System

Ball Constraints



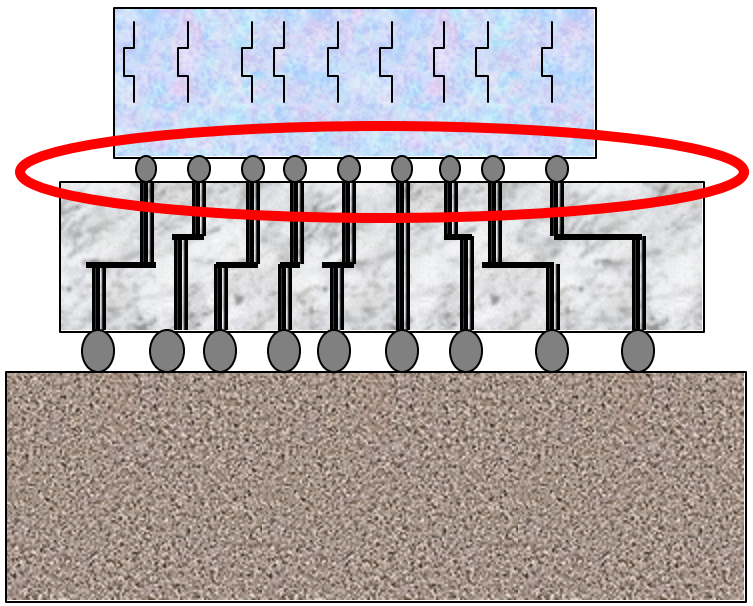
- PCB Trace Pitch
- Ball Size
- Ball Pitch
- Reflow Temperature

Substrate Constraints



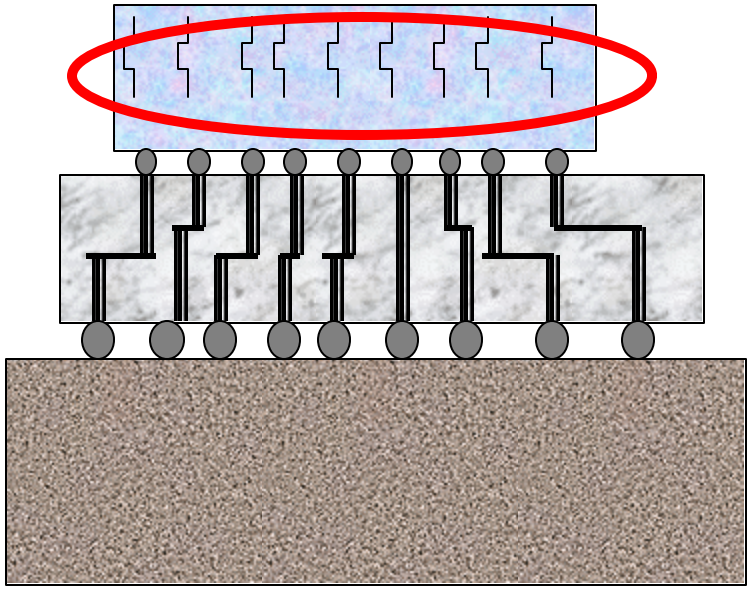
- Trace Pitch
- Via Size
- Number of Layers
- Cost
- Substrate composition
- Complexity (defined by silicon to PCB matching)

Bump Constraints



- Bump Size
  - Width and Height
- Bump Pitch
- Under fill
- Alpha Particle Emission/Lead Content
- Reflow Temperature
- Current Carrying Capability

Silicon Constraints



- I/O Construction, Placement and Size
- Auto Routing
- Electromigration
- Cross Talk
- Die Size
- Large Number of Signals
- “Keep Out” Areas
- Die Stress

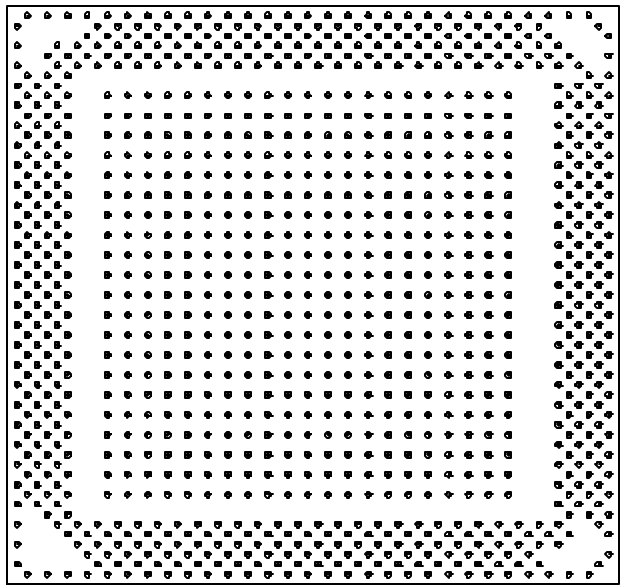
Trade Offs in Flip Chip

- IO Methodology
  - Peripheral IO vs. Area IO
  - Peripheral Power/GND vs. Direct Connect
- Bump Methodology
  - Peripheral Bumps vs. Area Array Bump
- Place and Route
  - Bumps in Netlist
  - Exclusion Areas
  - Power Grids

Variations

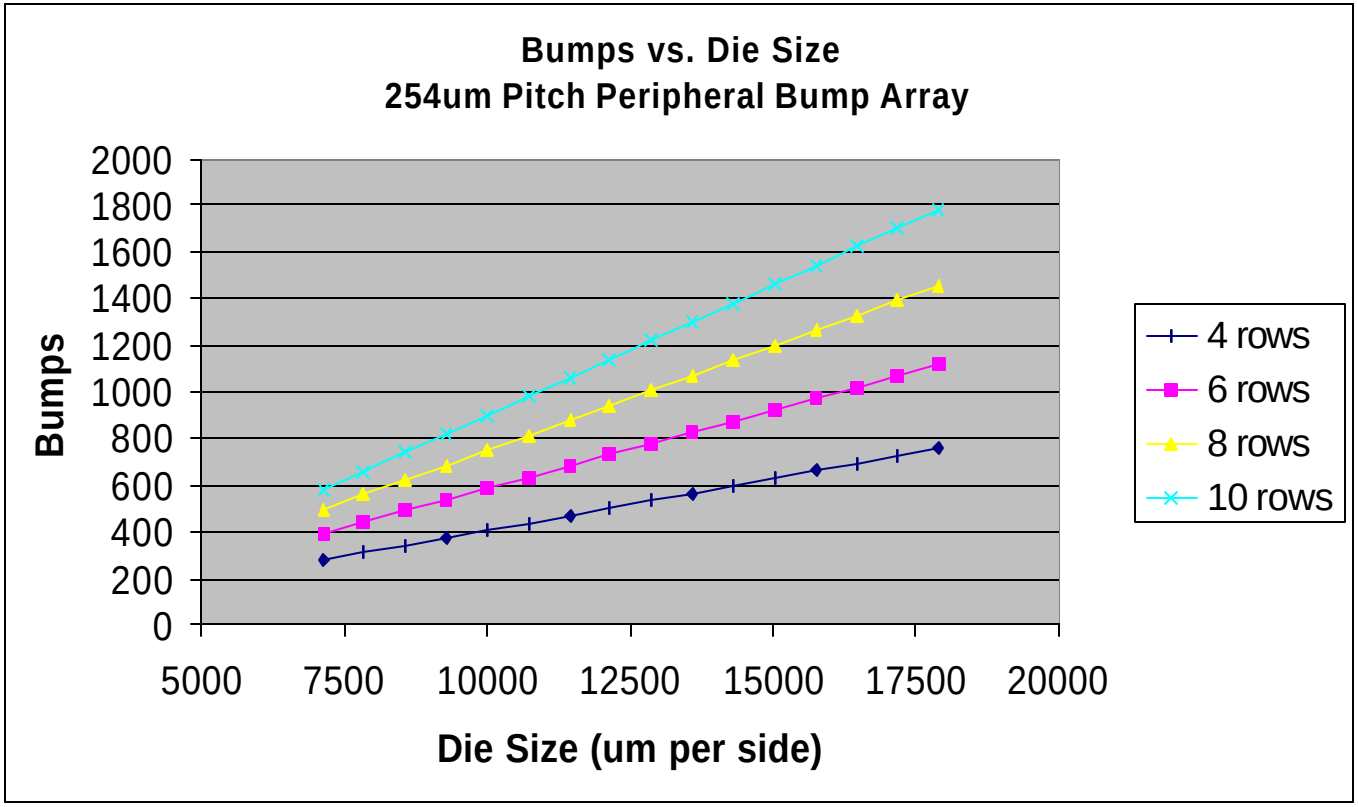
- Peripheral Bumps vs. Full Array Bumps
  - Trade off bump pitch vs. cost
  - Trade off bump pitch vs. substrate complexity and routing complexity
- Peripheral IO vs. Array IO
  - Staggered Pads with fine pitch
  - Multiple IO Rows
  - Core Area IO Rings
  - Trade off substrate complexity

Peripheral Bump Array

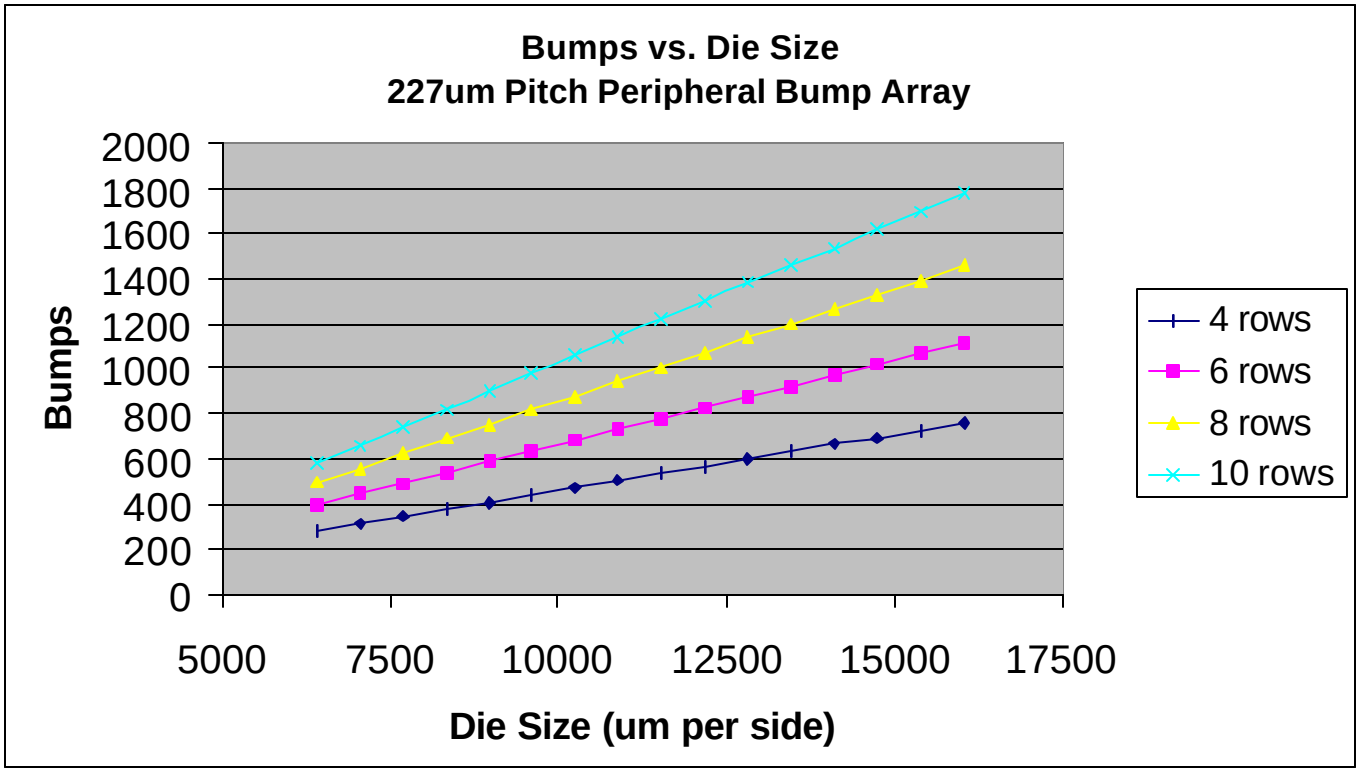


- Number of Rows Limits Substrate Routing
- Costly Substrate May Be Required
- Bump Pitch Must be Aggressive For Large Number of IO
- Redistribution Layer May Still be Needed

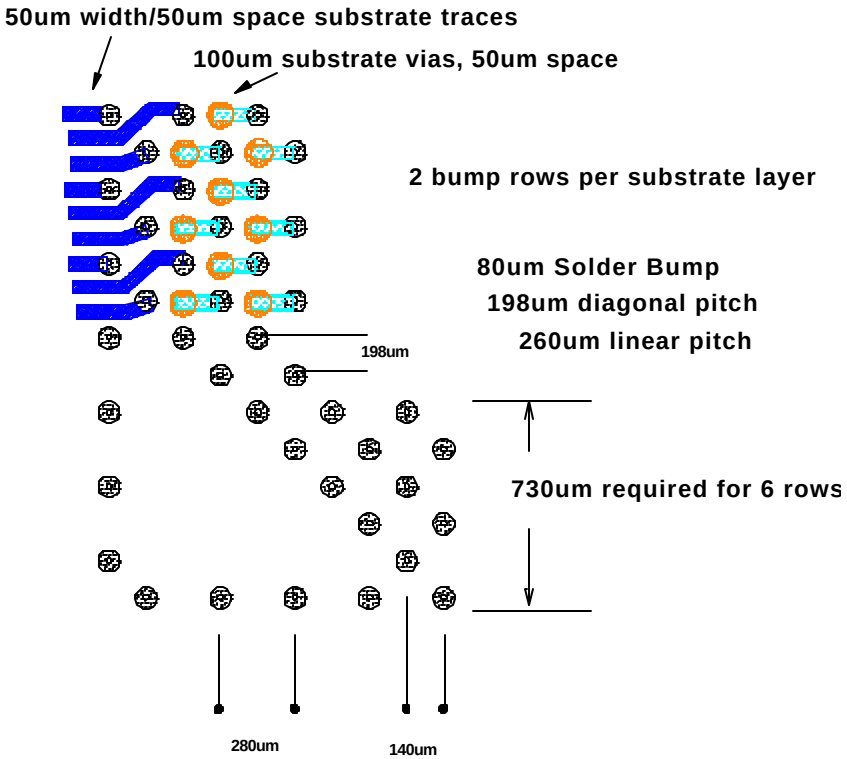
Bump Count vs. Bump Pitch
254um Peripheral Array



Bump Count vs. Bump Pitch
227um Peripheral Array

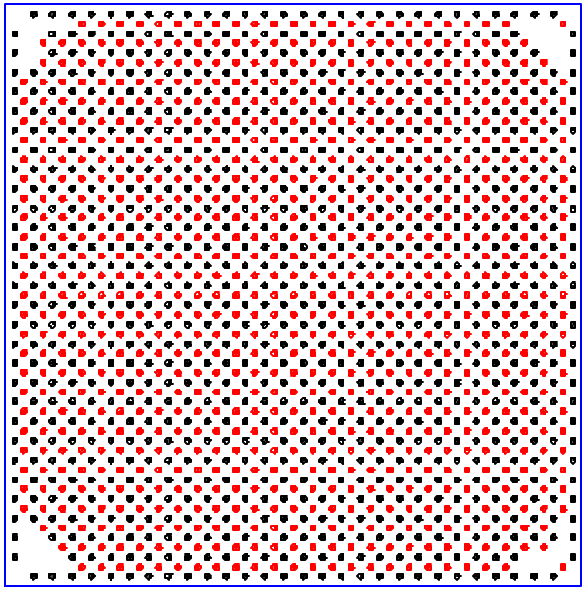


Peripheral Bump Array Corner Section



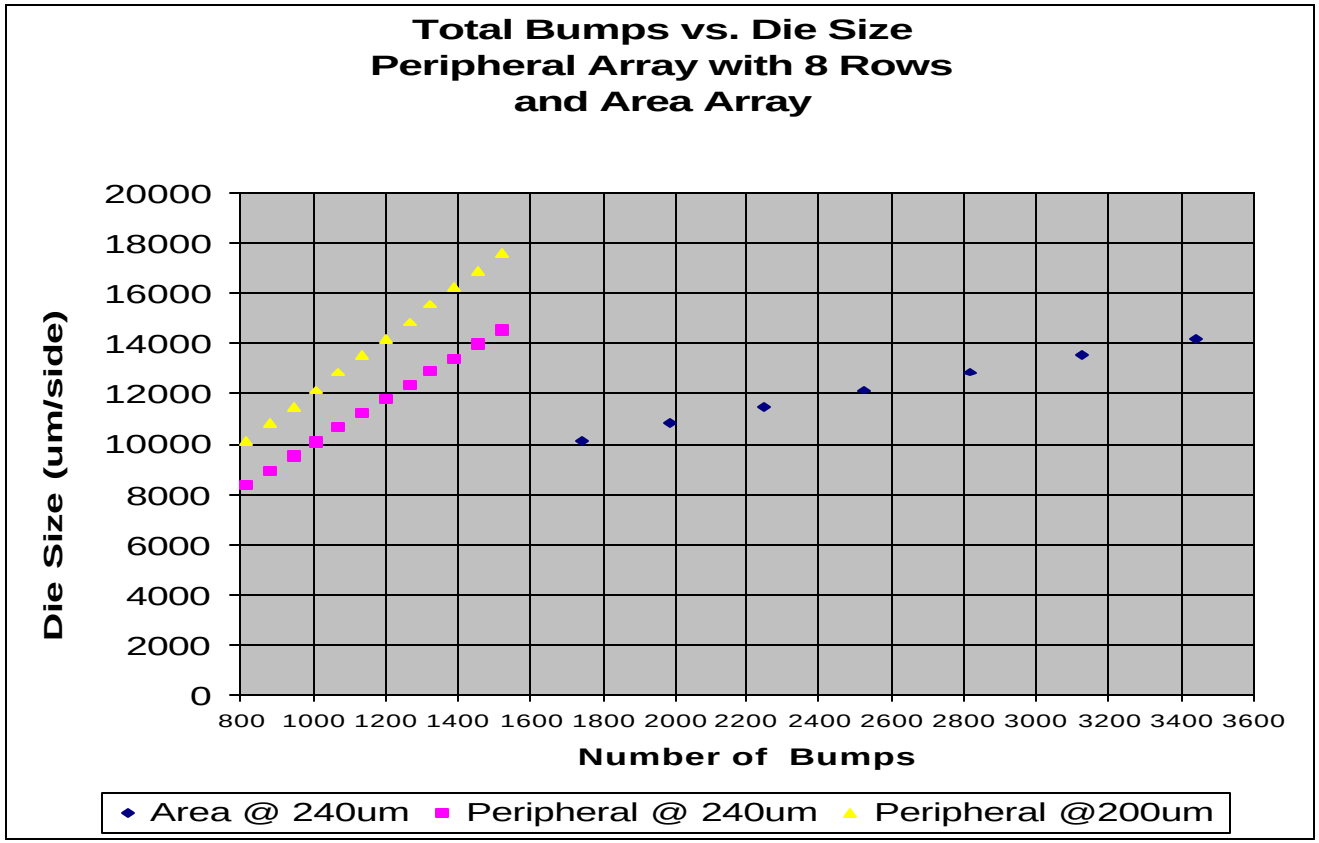
Full Array

Fully Populated Array



- Many More Bumps Can Be Placed
- Less Aggressive Bump Pitch Can Be Used
- Less Aggressive Bump Size Can Be Used
- Must Have Ability To Place IO As Standard Cell
- Simplify Substrate Design
- Possibly Reuse Bump Masks
- Redistribution Layer Probably Not Required

Area vs. Peripheral Array



Bump Count vs. Bump Pitch
Full Array

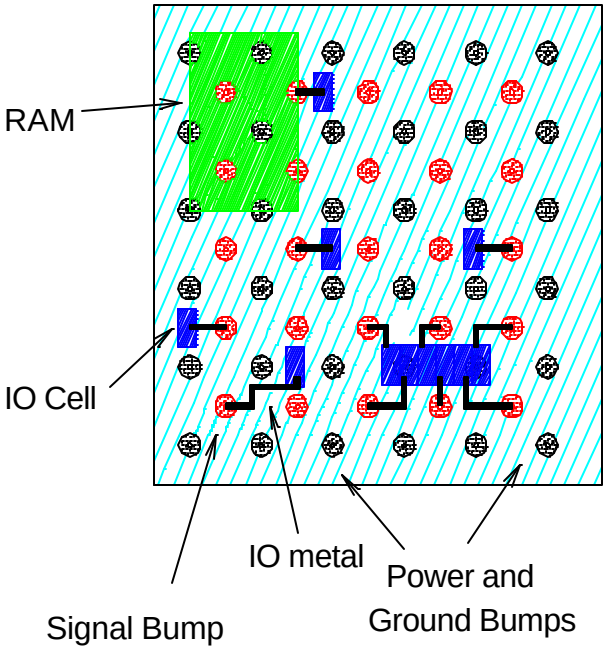
Bump Comparison - Similar Die Size
Full Area Array vs. Peripheral Bumps

Bumps Outside	Bump Rows	Bump Pitch	Periph/ Array	Bumps	Die Size
40	8	200	P	1136	11220
45	8	200	P	1296	12620
50	8	200	P	1456	14020
30	30	240	A	1741	10142
38	38	240	A	2813	12858
42	42	240	A	3445	14215

Note: 100um edge clearance, no other assumptions were made on exclusions for corners, etc.

Full Array - Section

Exploded View



- Development Required for Core Placed IO (IO's, Power Grids, ESD,….)
- Development Required for Place and Route
- Not All Bumps Can Be Used (i.e., over Sensitive Blocks)
- Alpha Particles Can Be Reduced With Alternate Bump Materials

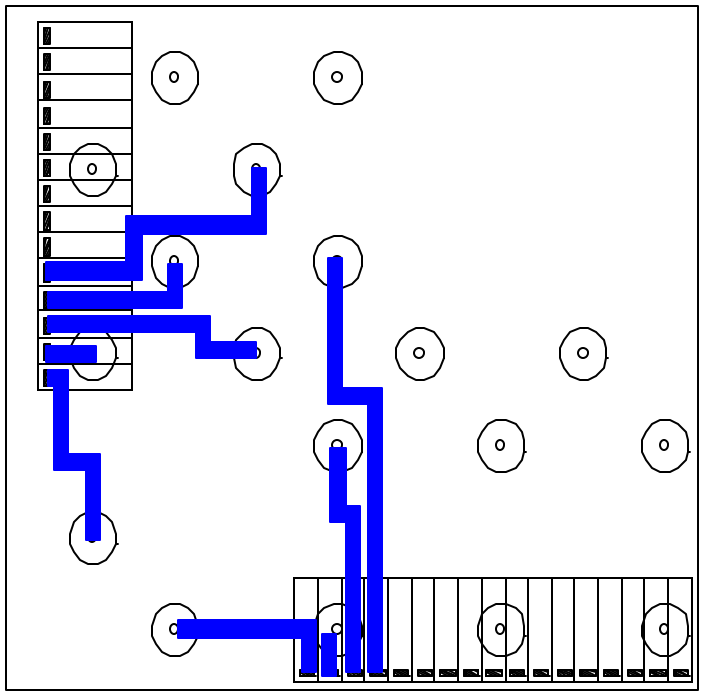
Summary of Trade Offs

- Assembly costs
- Substrate complexity
- Power/performance
- I/O density
- Flexible Netlist
  - inclusion of bumps
  - flexibility between substrate and silicon

IO Placement and Design

- Solution 1: IO ring as usual at chip periphery
- Solution 2: direct access to core vdd & gnd
- Solution 3: double IO ring at chip periphery
- Solution 4: center IO ring, one or more in chip core
- Solution 5: chip scale IO distribution – IO's placed like standard cells anywhere in die

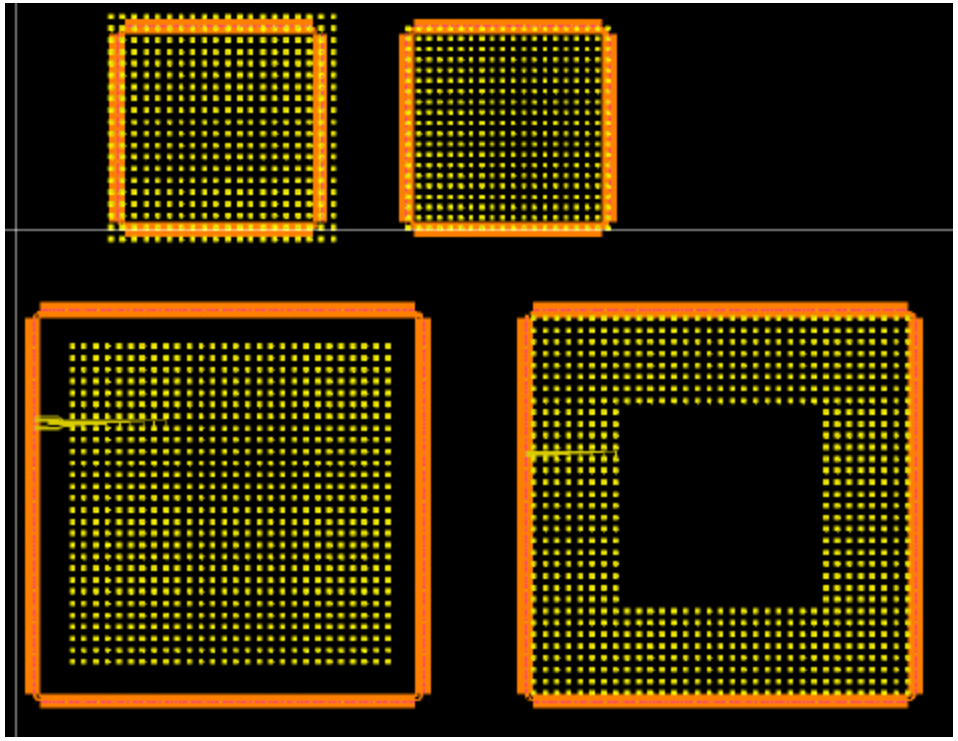
IO Placement Method #1



- Solution 1: IO ring as usual at chip periphery
  - Chip design very close to bonding solution
  - Simple replacement of IO's for bonding with IO flip chip layout
  - Library solution easily available
  - Complex redistribution layer required
  - Limited number of IO’s

IO Placement Method #1

400 pins
250um pitch
bumps



400 pins
225um pitch
bumps

800 pins
250um pitch
bumps

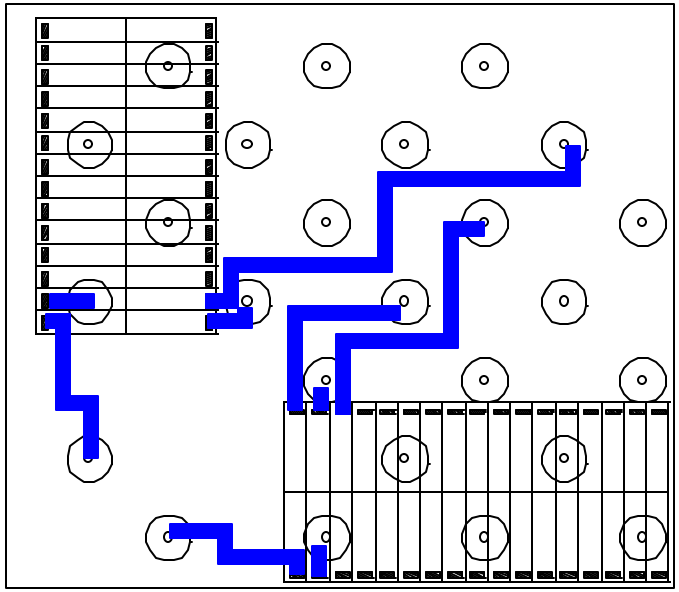
800 pins
250um pitch
bumps

No chip area benefit for small chips - Full bump array redistribution very difficult

IO Placement Method #2

- Solution 2: direct connect core power grid
  - IO ring includes:
    - All signal IO's
    - Access to IO power supplies
    - Core ESD protections (= IO slots without access
    - Core power bumps connect directly to gnd & vdd power grids.
- Benefits
  - Better core power distribution (less voltage drop)
  - Simplifies redistribution layer
  - Somewhat reduces the IO number at periphery.
- Risk: ESD level will must be evaluated

IO Placement Method #3

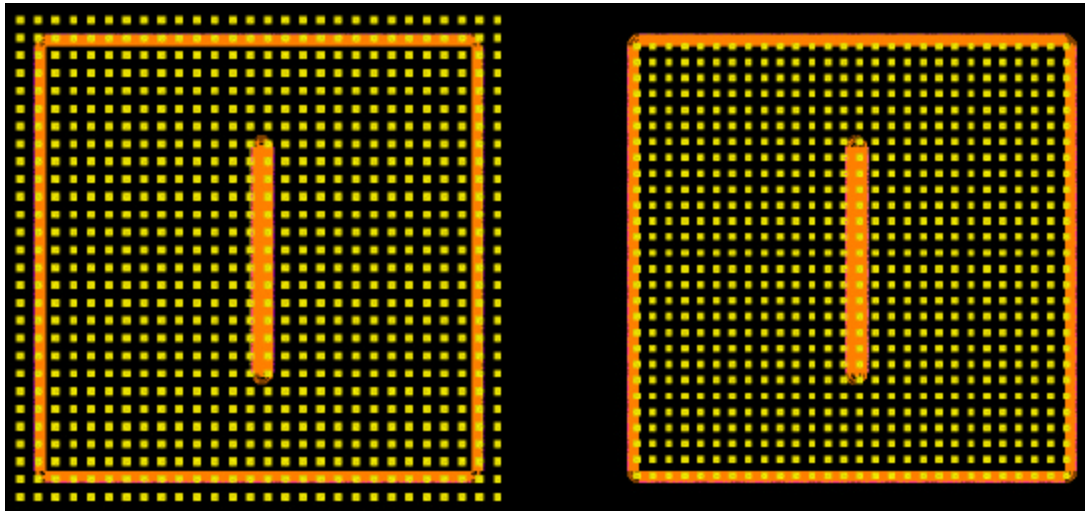


- Solution 3: double IO ring
  - Two IO rings at chip periphery
  - Equivalent IO pitch ½
  - Allows to fit higher number of IOs.
  - Redistribution extremely problematic
  - Chip size very likely to be limited by bump constraints
- IO library would need only minor, if any, rework.

IO Placement Method #4

- Solution 4: center IO ring
  - One or more IO ring in chip core
  - Ring in core can also be simple row(s) of IOs
  - Less flexibility in core floor planning
- Benefit
  - Potentially less distance to reach IO buffer from core blocks.
  - Redistribution considerably less complex
- IO library would need little, if any, rework.

IO floor planning: Method #4



Inner “ring”shown is flattened (left and right sides abutted)

Other arrangements possible

IO Placement Method #5

- Solution 5: IOs anywhere
  - IOs are distributed throughout the core chip, individually or in small groups.
  - IO buffer distribution can closely reflect the bump distribution.
- Benefit
  - No redistribution layer required
  - Direct connections to IO buffers
- Prospective solution for High Pin Counts
- Development Needed:
  - *IO's, Power Grids, ESD*
  - *CAD place and route tools*
  - *Verification tools*

CAD Issues to be Solved

CAD Problems to be Solved

- Need appropriate IO Design for Area Array IO
- Need to be able to place IO like Core Macro Cells
- Need to comprehend Single/Multiple Power Grids/Domains
- Need Connectivity Checking of Transistor to Substrate Trace to PCB (silicon/bump/trace/ball)
- Need the ability to instantiate Bumps in Gate Level Netlist for Placement in relation to IO and power grids

CAD Problems to be Solved

- Need the ability to Extract and Simulate across boundary connections of silicon/bump/substrate
- Need the ability to exclude Bumps from some areas
- Need the ability to perform top level routing from IO macro to Bump (redistribution layer)
- Need Concurrent Design of PCB, Substrate and Silicon

Design Solutions that Drive to Flip Chip

- Large numbers of IO (>1200) – Flip Chip has greater number of connection points available
- Large numbers of Power/Gnd connections (>1200) – Flip Chip can directly connect to Power grid
- High Performance Packaging (high speed, low inductance) – Flip Chip eliminates/reduces bond wire effects
- High Power Consumption (40-60+ watts) – BGA package allows heat sink attachment to die mount area
- Nominal Die Size (~13mm/side for ~2400 I/O + Power/Gnd + >8 Million Gates Logic + Memory) – Full array of bumps reduces pad limited die
- Multiple Power Supplies Separated on Chip (IO and Core) – Substrate can have multiple power planes

Conclusions

- IO count is increasing dramatically due to increased silicon content and power/ground requirements
- Gate count is increasing dramatically due to increased processing capability driving very high power consumption
- New packaging methodologies must be introduced

Conclusions

- IOs not necessarily a limiting factor
  - Pad limited chips may very well become bump limited with flip chip.
  - Congestion in redistribution must be taken into account
- Peripheral IO and Peripheral Array Options will be feasible for medium pin counts
- Full Array Options required for high pin counts
- IO libraries may need major redesign for some solutions, OK for other solutions
- Development work required for high pin counts
  - IO design, power grid, place and route
  - Codesign, verification
  - Reliability, ESD