Mixed Signal Behavioral Modeling in the Integrated Circuit Industry

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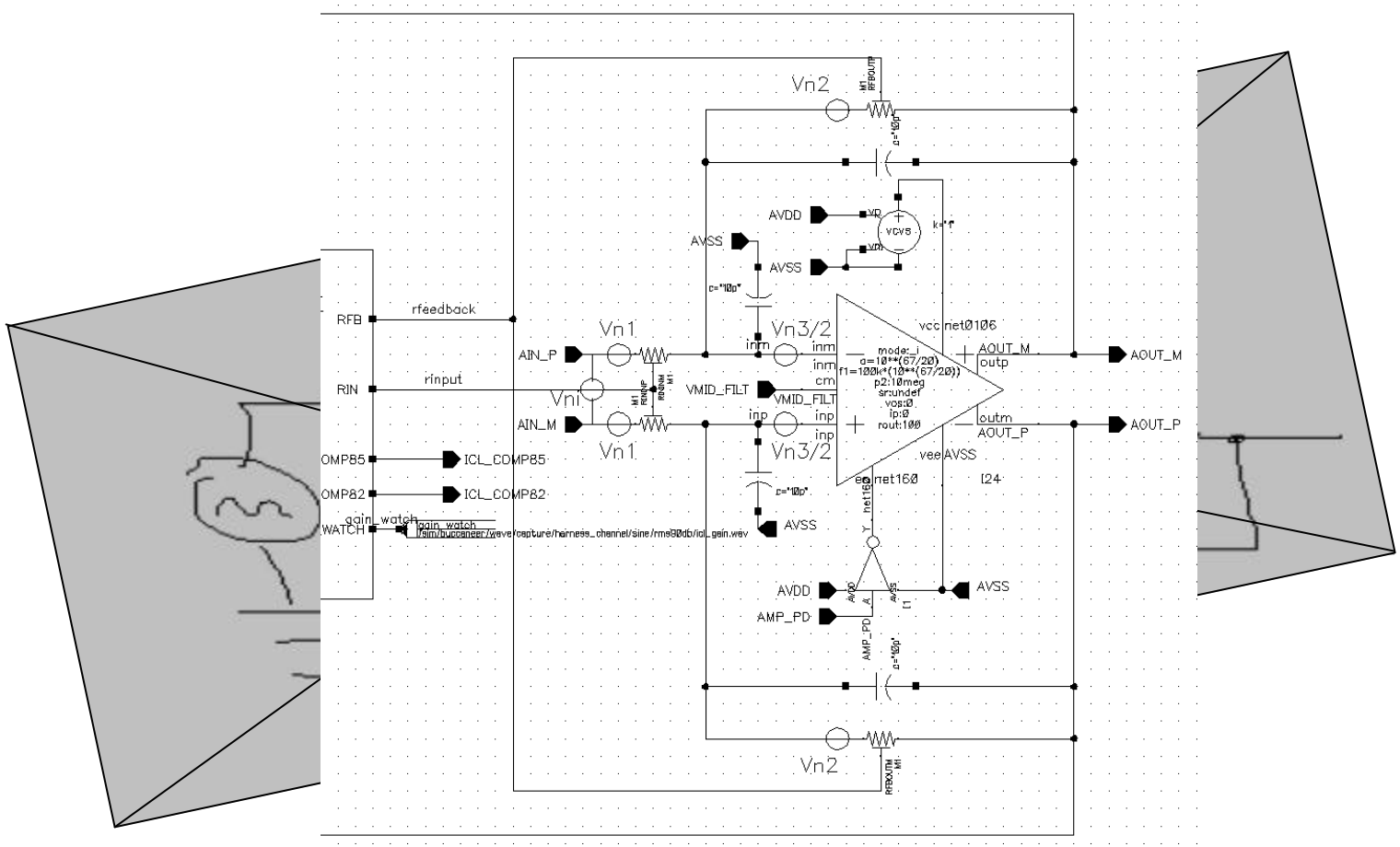
Overview

- Background
  - Origins of hardware description
  - Comparative anatomy of analog and digital simulation
- Comparative Evolution of Digital and Analog Design Flows
- Mixed Signal Simulation
  - Looking for the Reese's Pieces Experience
  - The Mine Field
  - Products and approaches built on the new standards.
- The Muddying of the Waters
- SoC and System-C
- Q & A

Describe Some Hardware

- The schematic



Circuit Analysis

- Hey, lets use computers to do this KCL and KVL stuff...
  - Non Linear Differential Equation Solver
    - Chord, Newton-Raphson, Secant
    - Making the most of the sparse matrix
      - Memory allocation
      - Remember the order of variable elimination
  - Numerical Integration
    - Forward Euler
    - Backward Euler
    - Trapezoidal
    - Gear-Shichman
  - Applied to
    - AC Analysis
    - Transient Analysis
- Feeding the Animal...

The Netlist

- Stamp matrix with electrically meaningful modules, I.e. vccs, iccs, r, c, l, mos, bjt, etc
- Make a way to describe the sharing of variables:

File Edit Search Preferences Shell Macro Windows Help

/users/holmes/spi.txt line 7, col 27, 106 bytes

```
VIN IN 0 SIN 1.5 1 1K
L1  IN N1 L=1U
R1  N1 N2 RES=1MEG
C1  N2 N3 C=1U

M1  D G S B MODEL=NCH W=3.6 L=0.8
```

Rapid Evolution of the Description

- Netlist Enhancements
  - Hierarchical Instantiation
  - Multiplicity
  - Global Signals
  - Global Parameters
  - Hierarchical Parameter Passing
  - Structured Parameters

- Simulator Enhancements
  - Matrix Fracturing and Multi-rate simulation
  - Object Orientation of Process Parameters
  - Links to Design of Experiments
  - Optimization Loops
  - The User Defined Element

The User Defined Model (Two flavors)

- Spice UDM developer flavor *(hackers need not apply)*
  - Direct access to simulator variables (tol, time, timestep)
  - Can do things that change the size and density of the matrix (capacitor, or capacitor with parasite resistor)
  - Requires a lot of mathematical analysis up front.
  - All in all extremely dangerous, since it exposes a lot of simulator details.

- Spice UDM user flavor *(color inside the lines)*
  - Matrix stamp is predetermined, i.e. vcvs, vccs, etc
  - Non linear equations allowed (if then else)
  - No direct access to simulator tolerances
  - Safe, but not very flexible. Requires maintenance of special schematics.
  - Sequential Programming languages are used, like C or Fortran to implement a function but with the limitation that static variables are not allowed.

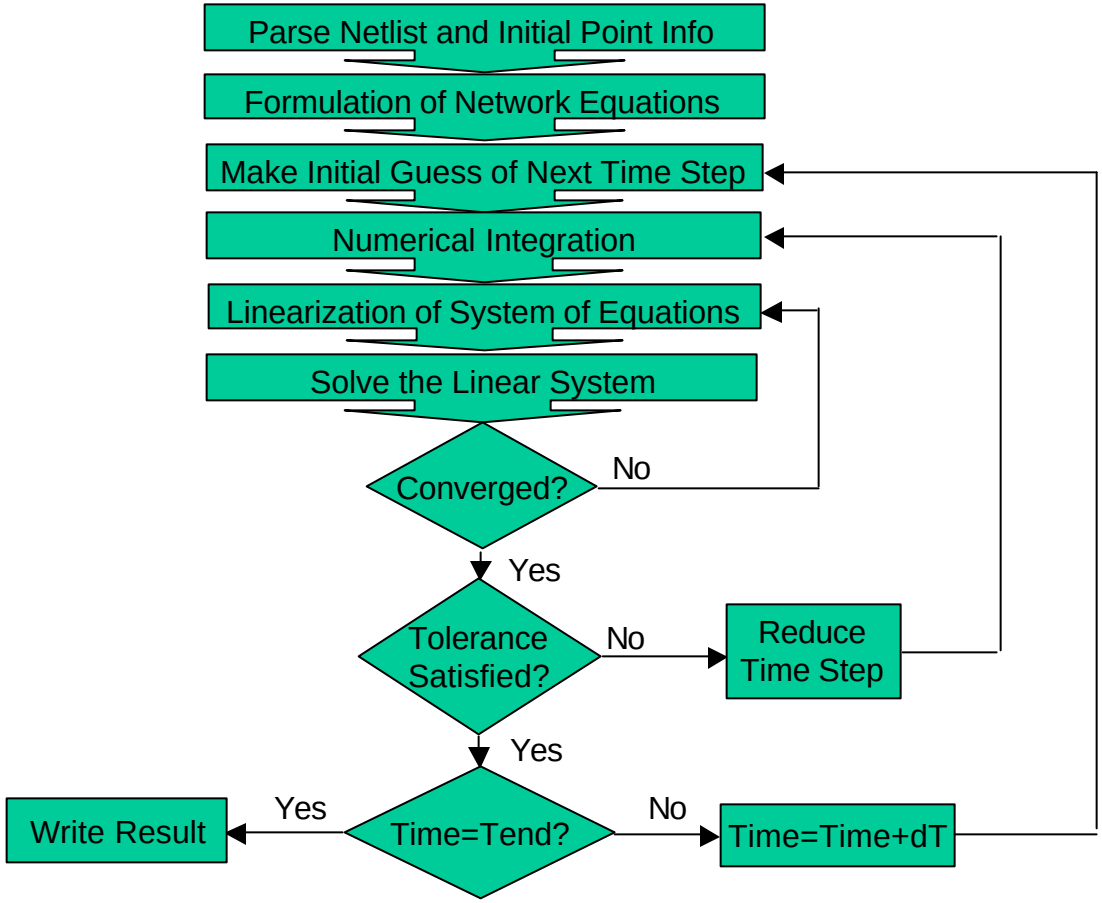
The UDM Space

- Drawbacks
  - The developer UDM requires a developer, and they're pretty expensive
  - The user UDM is trapped inside a dependent source so this requires a macro model
    - Macro models complicate parameter processing
    - Require maintenance of another schematic
    - Require convoluted netlisting protocols
- Some Notable Success
  - Simulation times were marginally improved
  - IP was hidden

The MaST

- The Matrix Stamp Template
  - Creates a “protective” layer between the user and the internals of the simulator.
  - Can actually change the size of the matrix
    - Hierarchy semantics (embedded netlists)
    - Differential equations
    - Non linear equations
    - Formalized semantics for calibration
    - Automatically Applies concurrency rules to the scoping of variables and parameters.
- First proprietary solutions
  - Saber MAST
  - Spectre HDL
  - Verilog-A

Quick Review of Typical SPICE Transient Analysis Algorithm



A Brief History of Digital Hardware Description

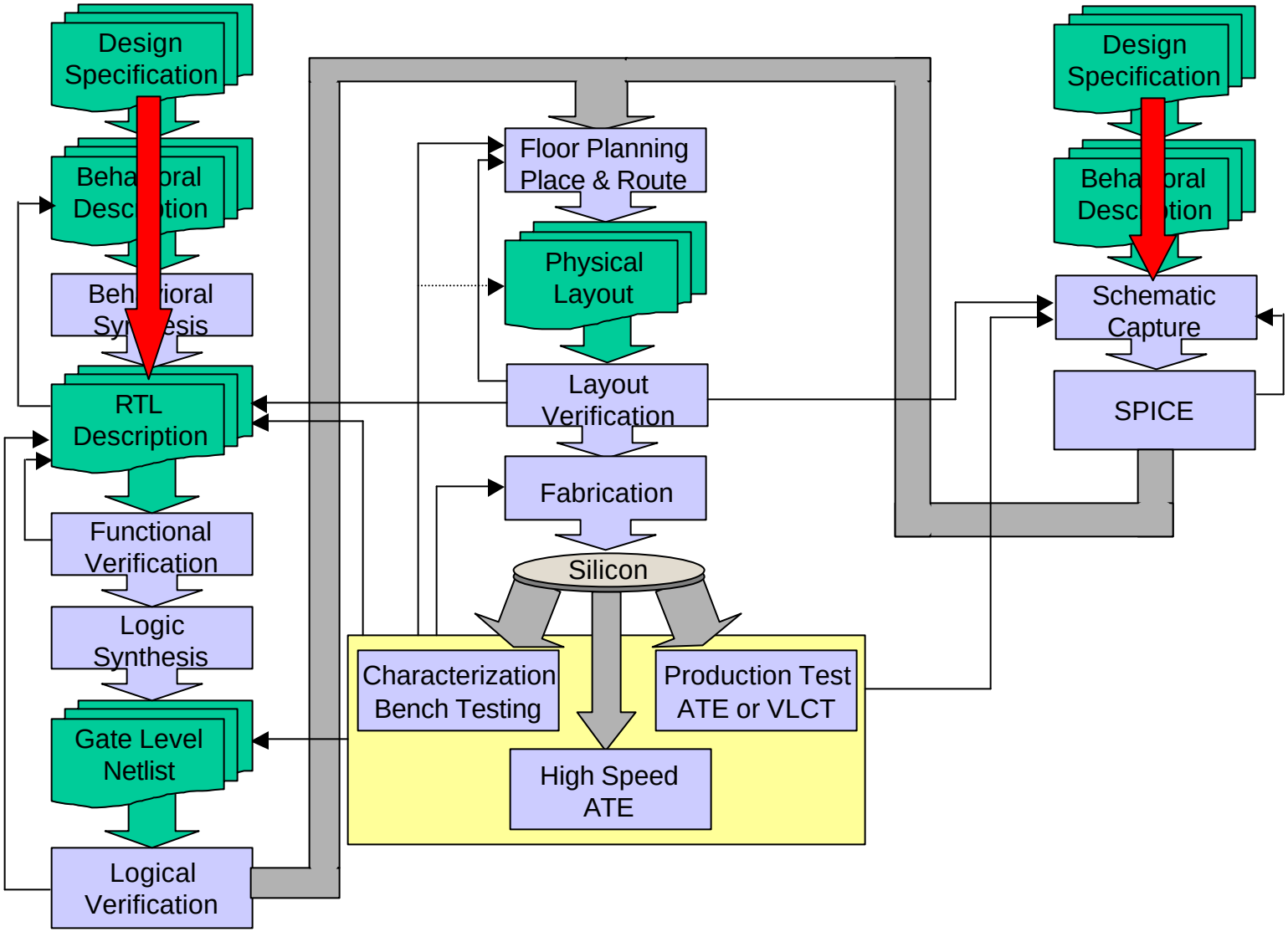
- Verilog
  - 1983 - Verilog Proprietary HDL developed by Gateway Design Systems
  - 1987 Licensed to Synopsys for RTL synthesis project
  - 1987 made public domain (VHDL wind shadow)
  - Verilog IEEE 1364

- VHDL
  - VHDL - DARPA driven project
  - VHDL-87
  - VHDL-95 IEEE 1076

The CMOS Assumptions

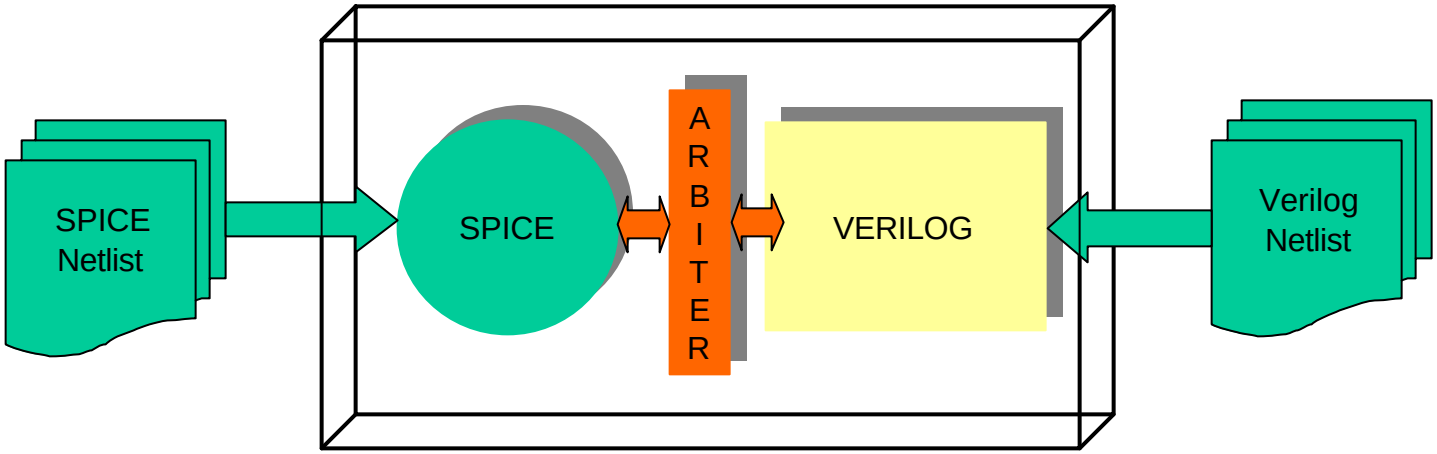
- The digital HDLs had two lessons learned from SPICE
  - The netlist (object orientation)
  - Concurrency
- Things that weren't learned from SPICE
  - Parameter Passing
  - Global Signals
- Dare to ignore physics
  - Charge, Voltage, Current Replaced by Time Events
  - Logic High assume the net voltage is VDD
  - Logic Low assume the net voltage is VSS
  - Logic Z assume the currents are 0
  - Logic X simply don't know what to assume
- Pin directions… input, output, inout;
  - Gate connected inputs
  - Drain connected outputs

Digital Vs Analog IC Design Flow



Mixed Signal Behavioral Modeling

- Looking for the Reese's Pieces Experience
  - Two Simulators in a Box

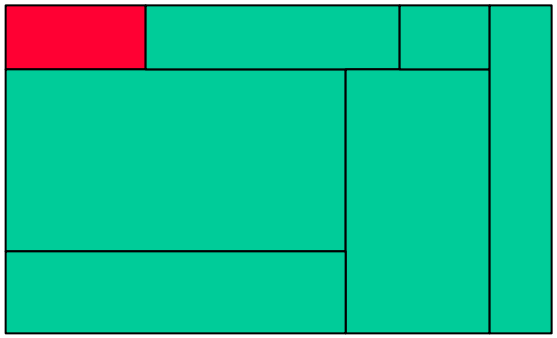


  - Mixed signal arbitration algorithms
    - Lock Step
    - Ping Pong
    - Predictive Ping Pong
    - Calaveras

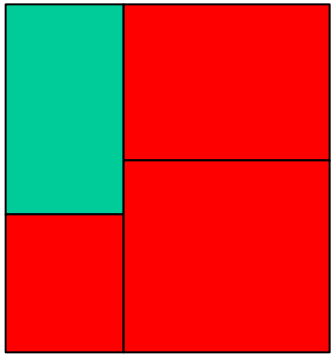
The Classic "DAC" Topology

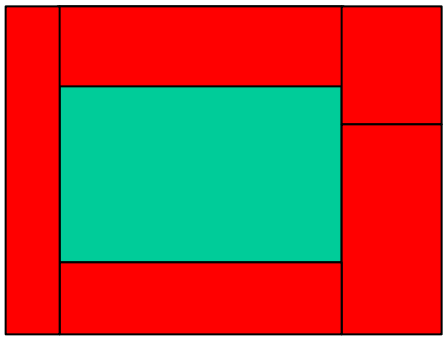
Analog

Digital



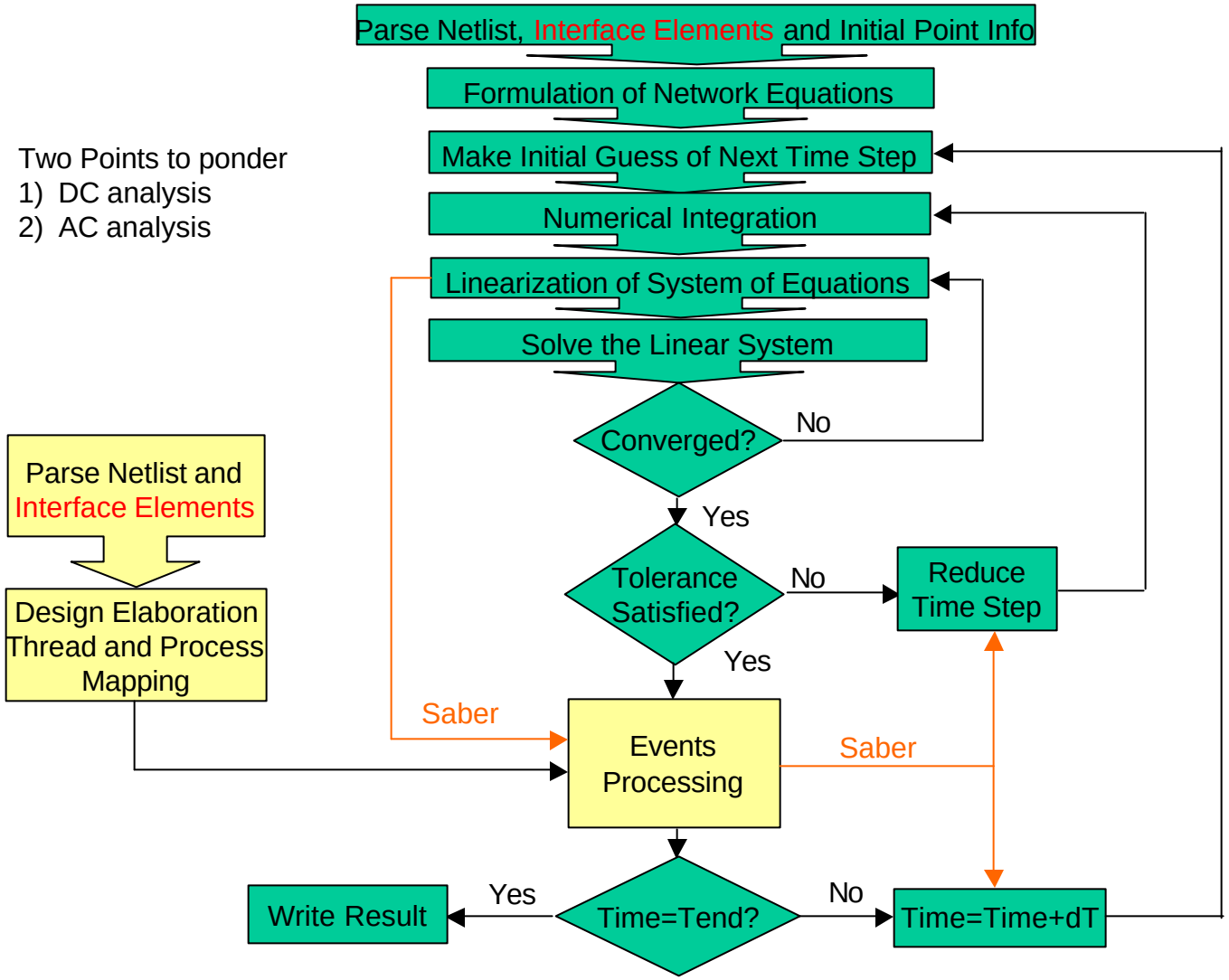
Thank you very little, but how about...





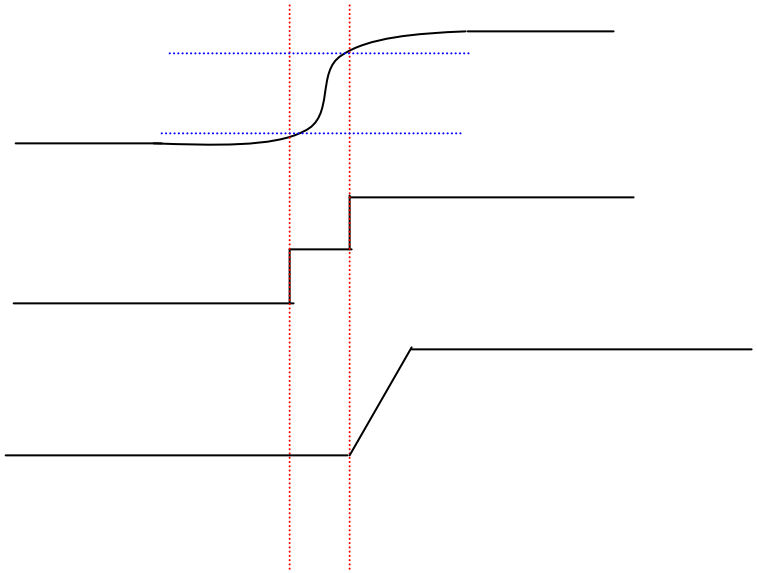
Mixed Signal Simulation

Two Points to ponder
1) DC analysis
2) AC analysis

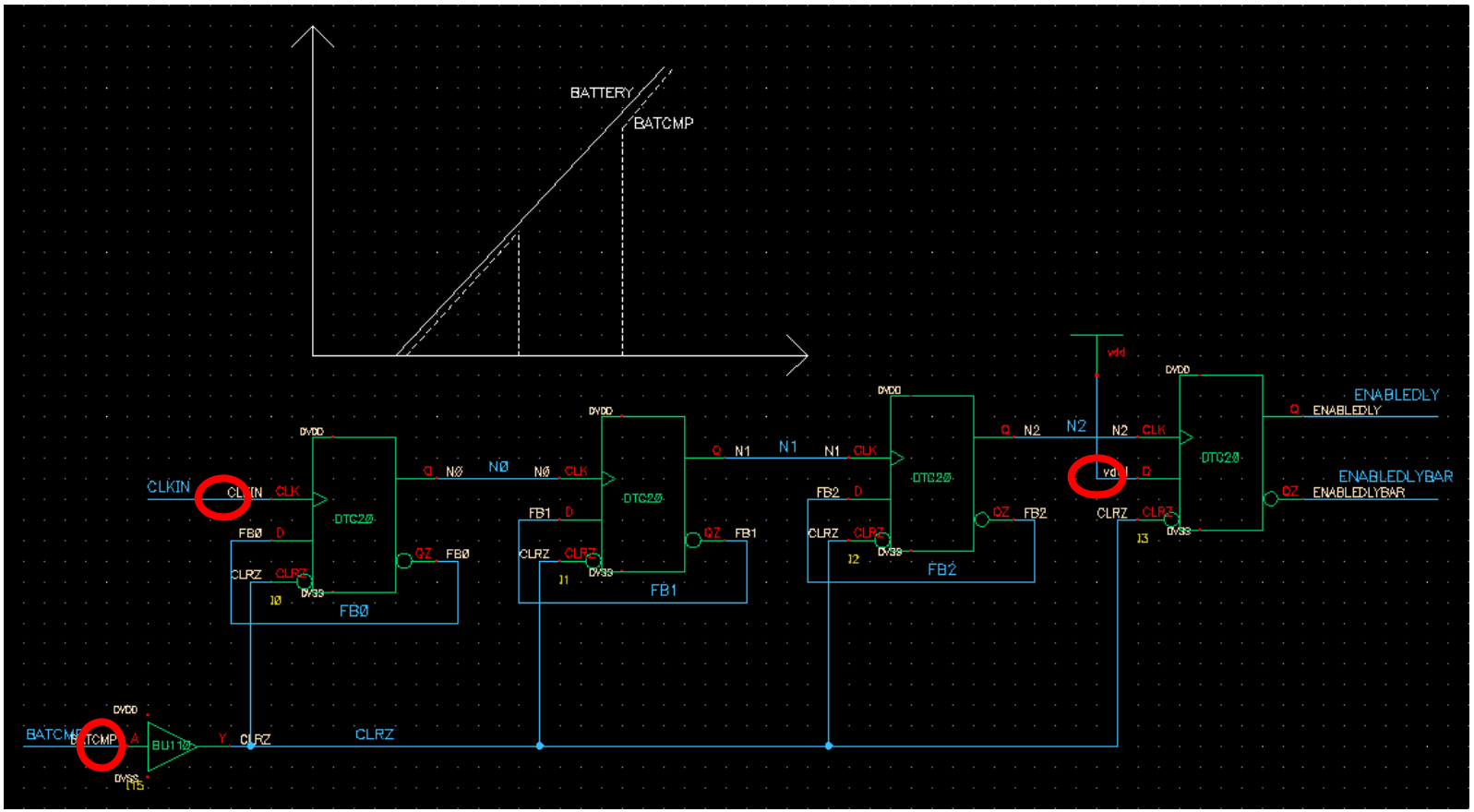


Signal Forensics

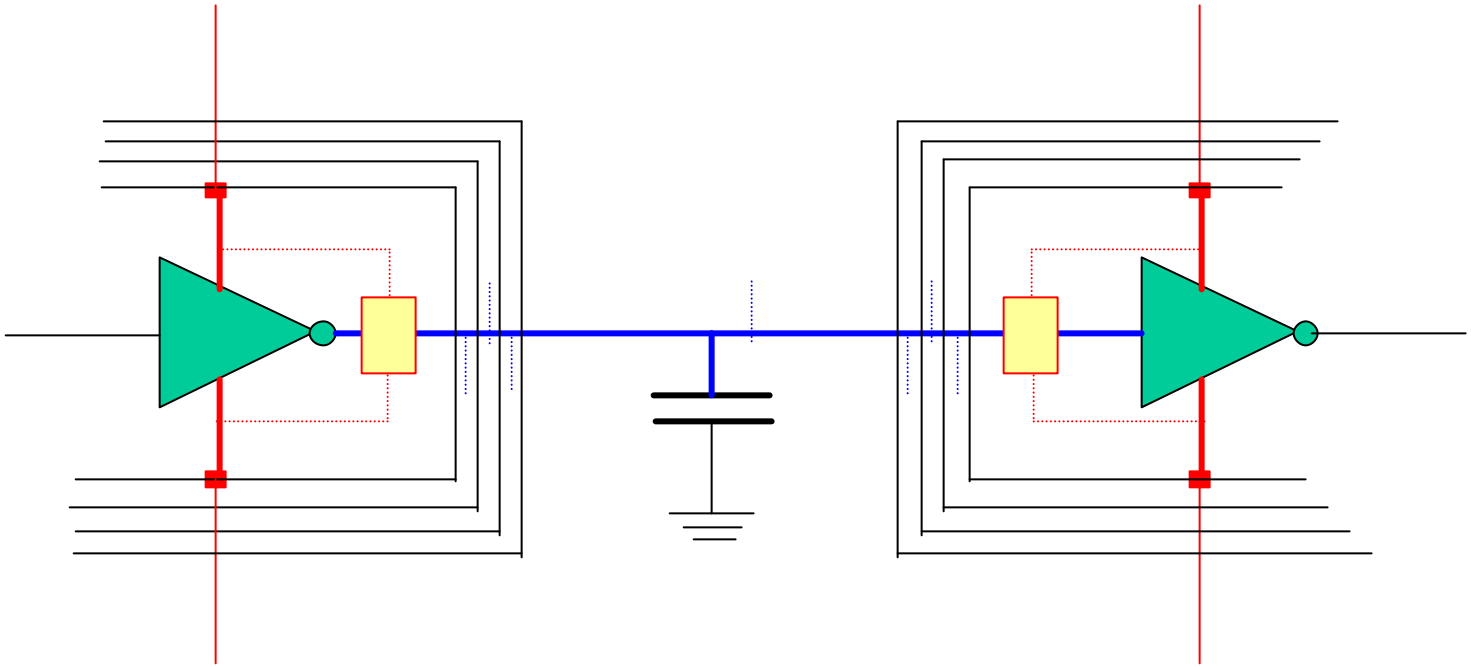
- Interface Elements are required to make the simulation work
  - a2d - from a continuous signal determine the time at which an event should be applied to the queue. This is seen as a primary input.
  - d2a - from an event reconstruct the signal waveform



The X Land Mine

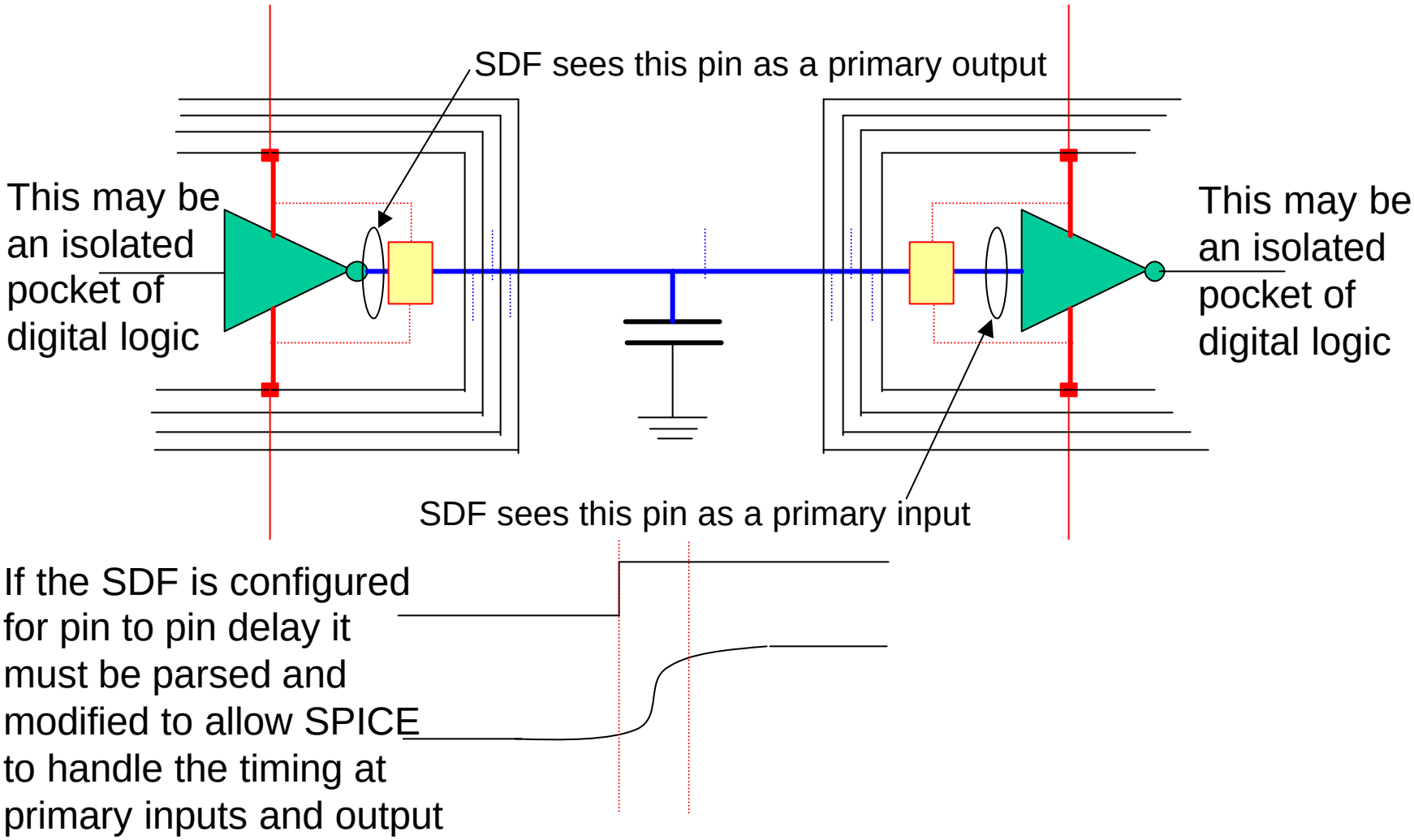


The Supply Land Mine



```
state logic_4 A #PORT(AOUTM_TEST)
                #Dir:output
                #Model:iv110_shm
                #Power:DVDD
                #Ground:DVSS
```

The Timing Land Mine



Different Approaches

- Advanced AMS - VHDL-AMS *(Mentor Graphics)*
  - Incomplete heuristics for interface element insertion
  - Two separate netlists required to complete the hardware connectivity description
- Verilog-AMS *(Cadence)*
  - Highly configurable heuristics for interface element insertion
  - IEs are not editable or debugged like other models
  - IEs are inserted at elaboration, not during netlisting.
  - The netlists are created incrementally.
- Saber VHDL-AMS & MAST *Synopsys(Avant!(Analogy)))*
  - Single kernel simulator with interface heuristics embedded in the model pin definition
  - Interface Elements inserted as extra elements in monolithic MAST or VHDL-AMS netlist
  - Interface Elements are debugged and modified like any other VHDL-AMS model

Muddying of the Waters

- Just as mixed signal modeling was reaching a critical mass the "accelerated" SPICE simulators hit the scene…
- Anagram, StarSim with the big winner seems to be PowerMill, with the new simulator Nassda HSIM on the horizon.
- PowerMill's success can be attributed to:
  - Replaces BSIM differential equation stamp with I-V look up tables.
  - Default is non-charge conservative piece wise constant currents.
  - No modeling required for huge through put improvements
  - Created support structure to build parsers for major SPICE netlist formats
  - Virtually no training required to run the tool
  - If properly configured it can reach 3% of SPICE
  - Provides a UDM interface to ANSI-C

History Repeats Itself

- The step function in through-put distracted resources from mixed signal modeling, for a while. Eventually Moor's Law caught up with the it…
- SoC quickly loaded down the fast transient simulators and the escape valve is once again the UDM.
  - Proprietary UDM interfaces delivered first.
  - Vendors stepping gingerly toward industry standard HDLs

SoC and System-C

- SoC is creating demand for HW/SW validation. Present day HDLs and their simulators are not flexible enough.
- Behavioral level needs to coexist with RTL level description of the SoC digital portions
- System-C appears to be filling this vacuum. The token based simulation kernel of System-C allows for very fast high level simulation with RTL that is suitable for synthesis.
- A highly directed effort would be required to bring the simulation through-put of a mixed signal behavioral model to the same ball park as System-C at the SoC Level.

Conclusions

- Mixed signal behavioral modeling is difficult.
- Most of the traditional flows and work habits work against a successful use mixed signal modeling.
- Mixed signal simulators are inherently confused.
- The analog behaviors are pretty much always the bottleneck.
- The default settings are to get the quick answer instead of the right answer.
- Multi-level simulation plans - BEWARE!

Questions and Answers

1.