IEEE DALLAS CIRCUITS AND SYSTEMS SOCIETY

HIGH SPEED AND RESOLUTION D/A CONVERTERS

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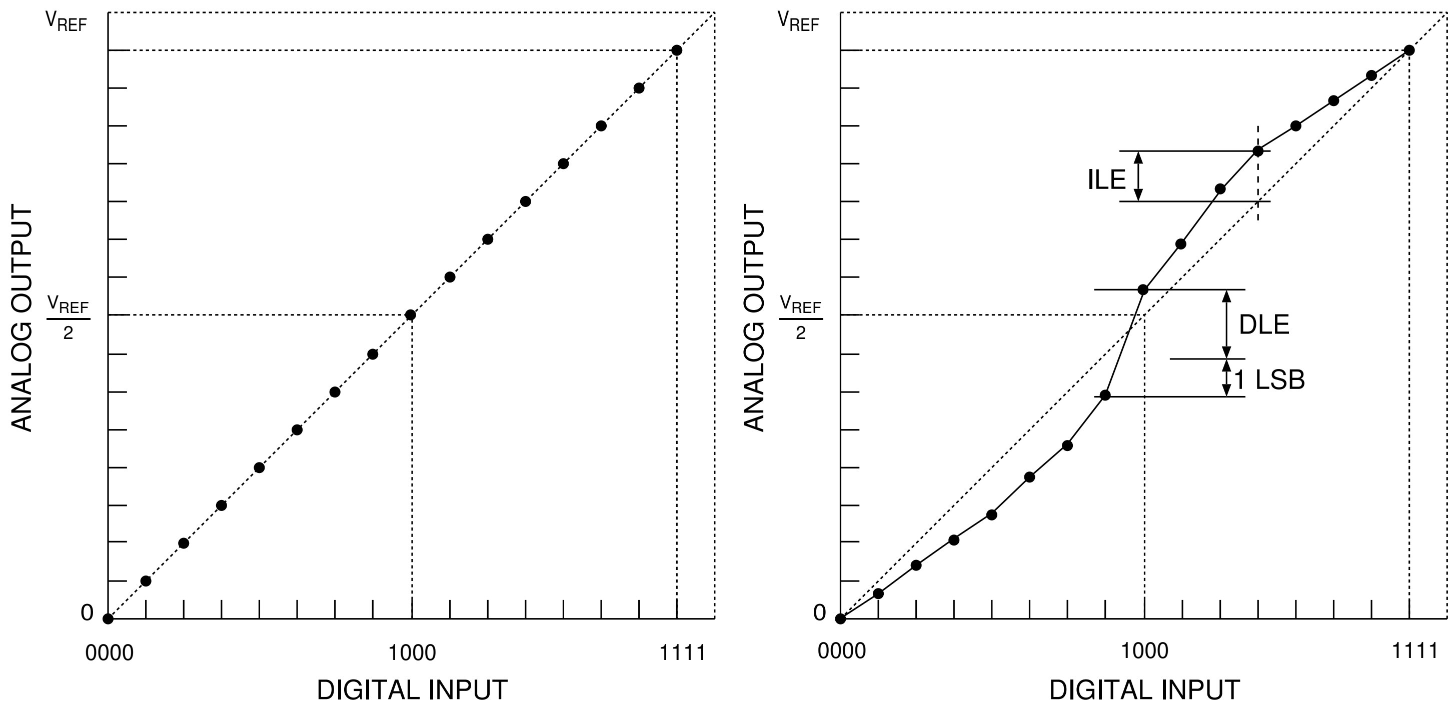
September 20, 1999

Outline

- *Introduction - Principles and Basic Circuits*
- Recent High Speed/Resolution D/A Converters
- Research: A high speed/resolution DAC for Spectral Performance

DAC Static Characteristics

a



- INL: Max deviation from staight line between 0 and FS
- DNL: Max deviation of any output step from 1 LSB
- Static Characteristic gives information about DC only

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[a] Introductory Material Reference: *The Circuits and Filters Handbook*, IEEE Press, 1995, Chapter 64

Monotonicity, SNR

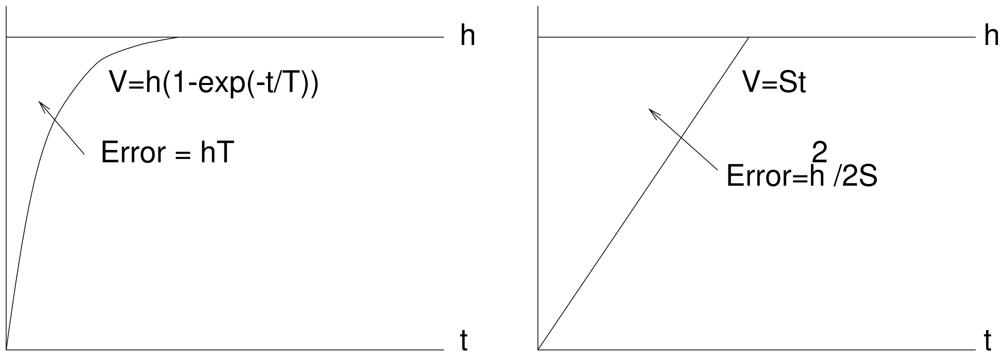
SNR

- Minimum resolution of N-bit DAC: $V_{ref}/2^N$
- SNR: Power Ratio of maximum signal to inband uncorrelated noise
- $SNR = \frac{3}{2}2^{2N} \approx 6N + 1.8dB$
- Quantization noise is distributed evenly up to Nyquist Bandwidth

Monotonicity

- Monotonicity – DAC output increases with each input code increase
- Monotonicity requires DNL $\geq$ 1 LSB at all points
- Problems with monotonicity typically arise when switching from LSBs to MSBs

DAC Conversion Speed



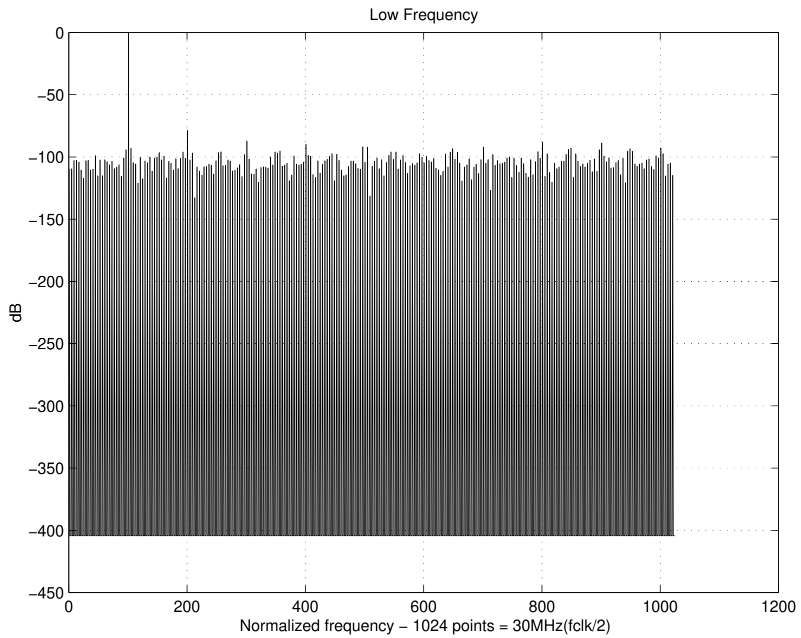
Single Time Constant Settling

Slew Rate Limited Settling

Above are responses to a voltage step of height h

- Exponential Response Ideal if time constant is signal-independent
- Slew Rate Limiting commonly occurs due to output buffers
- Signal-dependent time constants occur in buffers and resistor ladders

Output Frequency Spectrum



- Ideal DAC exhibits only quantization noise floor
- Harmonics arise due to DAC dynamic nonlinearities
- Measure of dynamic performance: Spurious Free Dynamic Range (SFDR)

Basic DAC Circuit Types

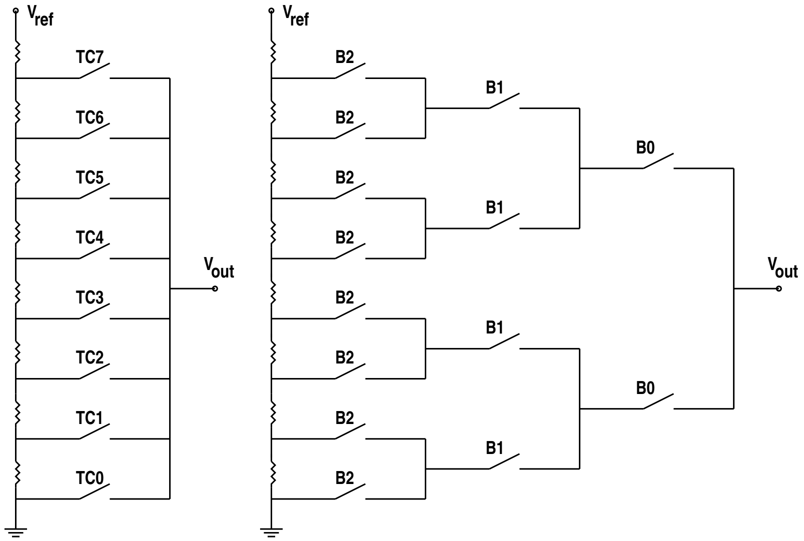
High Speed Operation:

- Voltage Scaling D/A Converters
- Charge Scaling D/A Converters
- Current Scaling D/A Converters

- Combinations also possible, e.g. voltage + charge scaling

- Algorithmic/oversampling DACs not considered here (limited speed)

Voltage Scaling DACs - Resistor String



Thermometer Decoded

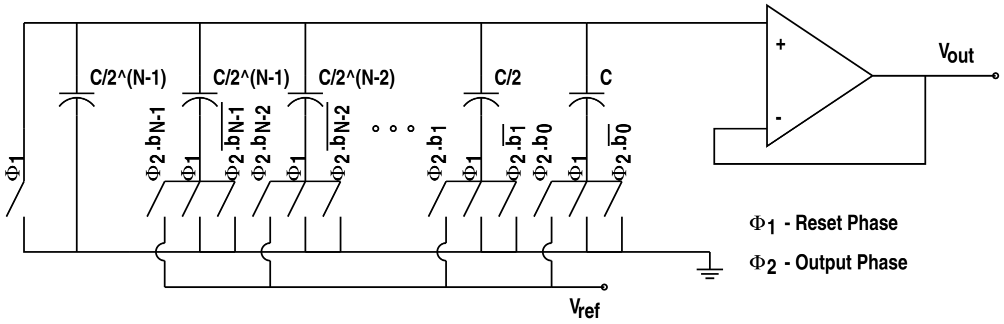
(a)

Binary Decoded

(b)

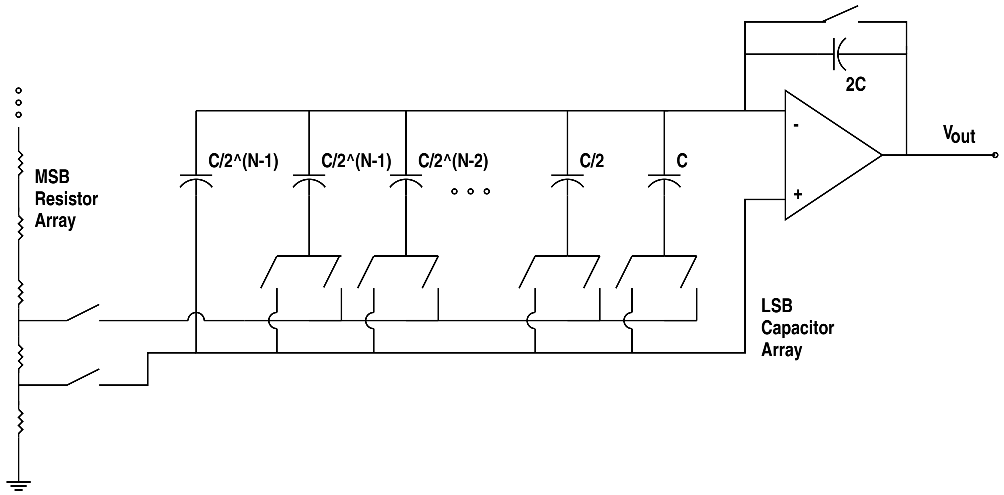
- Thermometer/Binary Encoded variants shown
- Static characteristics limited by resistor matching, output load
- Output resistance is signal-dependent

Charge Scaling DACs - Capacitor Arrays



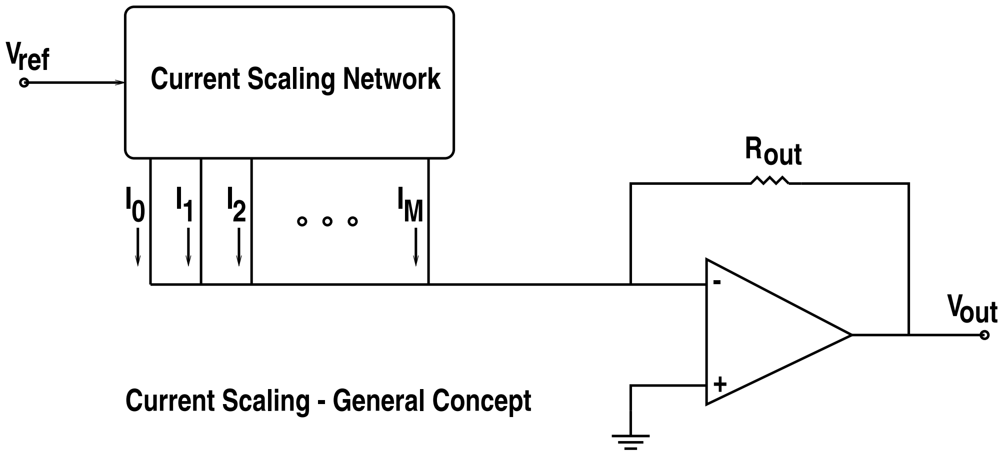
- Requires 2-phase non-overlapping clock, output buffer
- Static characteristics limited by capacitor matching
- Dynamic characteristics limited by output buffer

Voltage + Charge Scaling Combination DACs



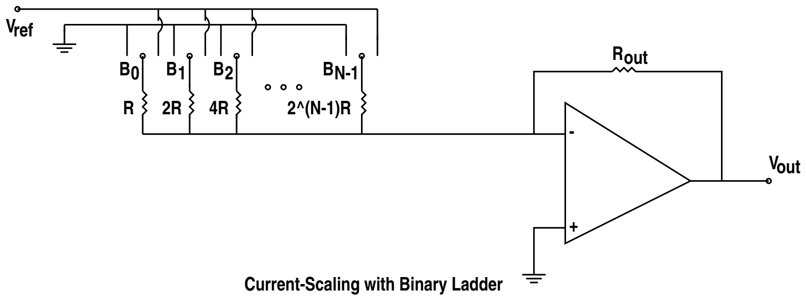
- Increases number of bits without exponential component increase or extra array and buffer
- RC DAC: Monotonic MSBs, LSBs depend on capacitor array DAC
- CR DAC: MSBs depend on capacitor array, monotonic LSBs

Current Scaling DACs



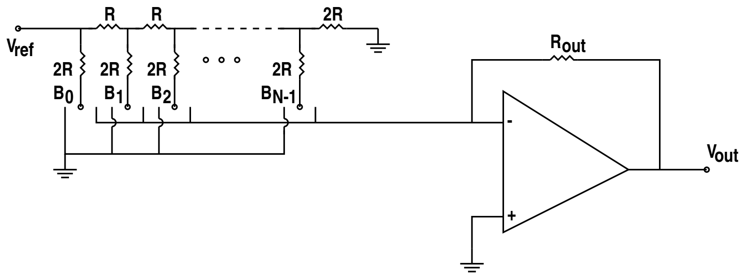
- Scaled currents are switched to output load depending on code
- Current scaling networks using current sources need no output buffer
- High speed DACs: current sources driving resistive loads directly

Current Scaling - Resistive Ladder Converters



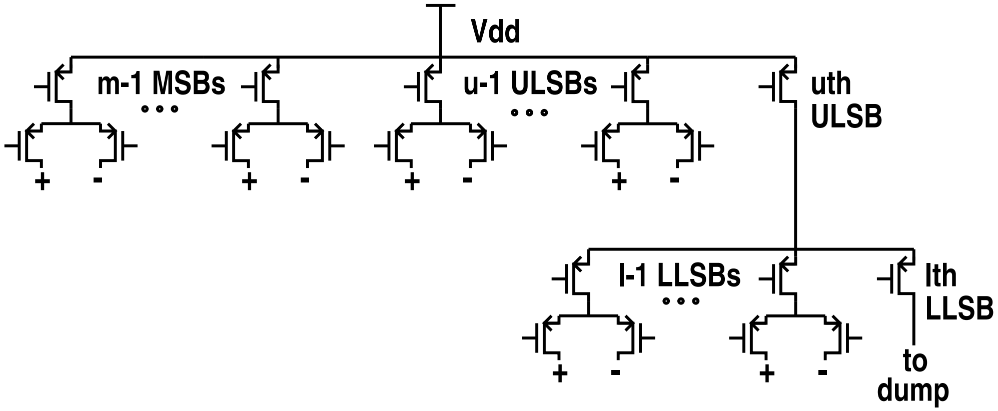
Current-Scaling with Binary Ladder

(a)



- R/2R ladder avoids binary-weighted resitors
- Both implementations need output buffer
- Code-dependent time constants (due to parasitics) for R/2R ladder
- Sometimes used as LSB dividers in current source DACs

Current Scaling - Current Source DACs



- Most often used architecture for high speed/resolution
- Current sources drive resistive loads directly
- Can be implemented in MOS or Bipolar or both
- Differential implementation is straightforward

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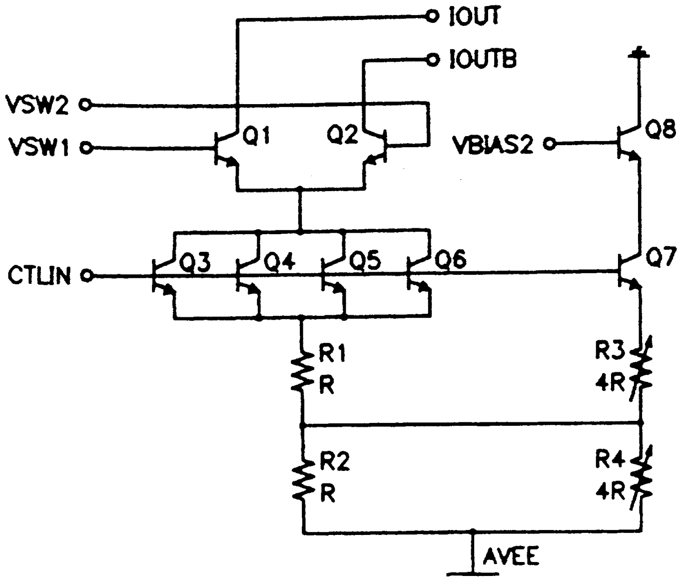
Bipolar Trimmed DAC - Architecture

[a]



- Bipolar DAC, 4 Thermometer MSBs, 10 LSBs from R/2R ladder
- Linearity from trimming: Bidirectional Trim Current Cells

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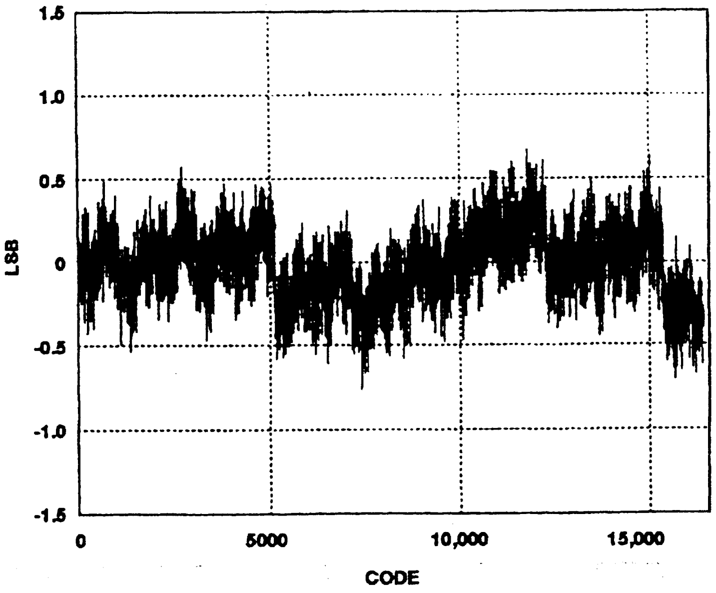
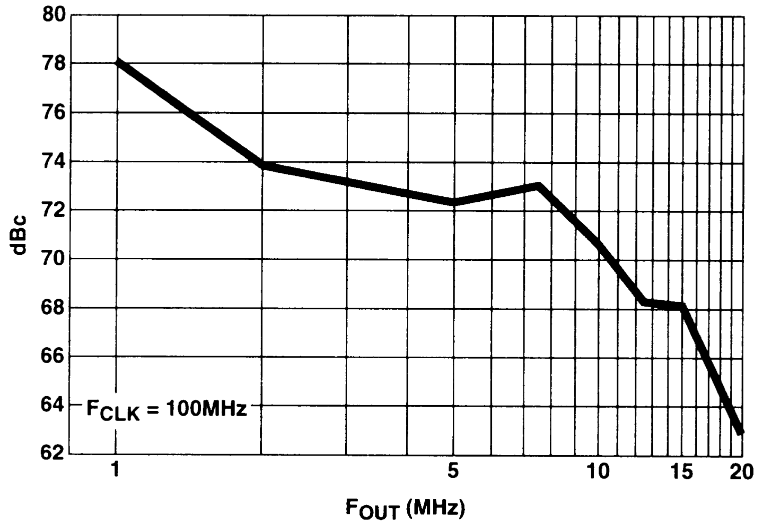
[a] *A Low Glitch 14-b 100-MHZ D/A Converter*, B.J.Tesch and J.C.Garzia, IEEE Journal of Solid-State Circuits, Vol.32 No.9

Bipolar Trimmed DAC - Performance

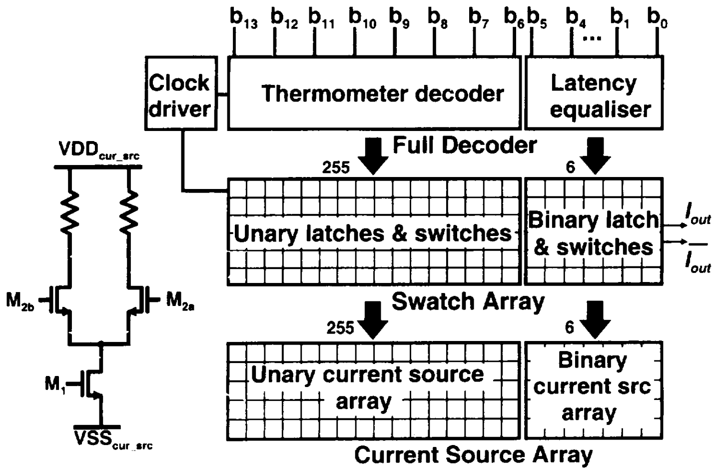




- Almost 14-bit static performance from trimming
- Characteristic dynamic performance dropoff with increasing IF
- 10MHz IF - $\approx$ 70dB SFDR

CMOS Untrimmed DAC - Architecture

[a]



- Full rather than row/column decoder
- MSB current sources divided into 16 sub-sources
- Switching order optimized to eliminate linear and quadratic gradient errors

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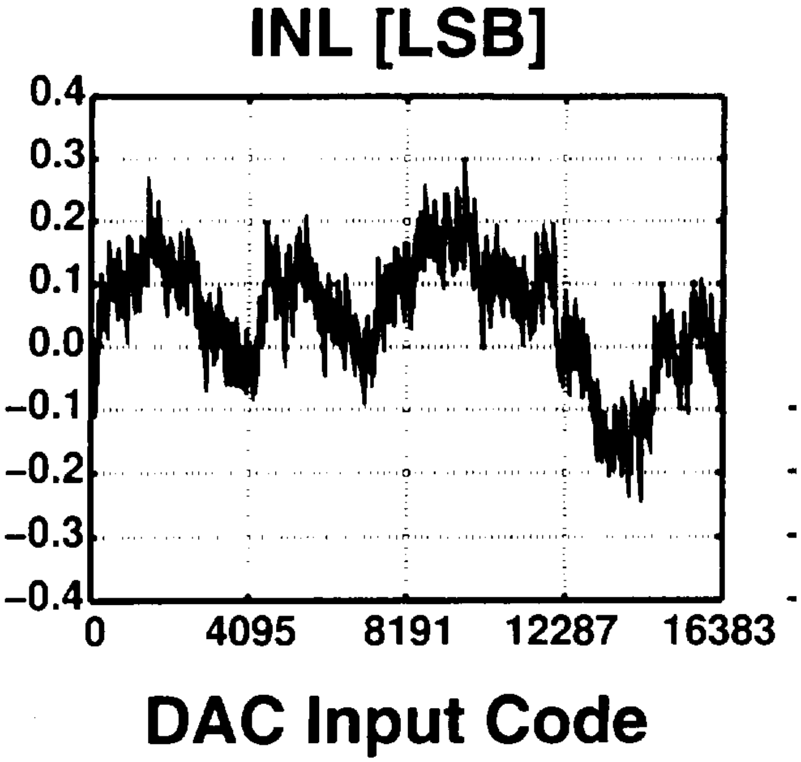
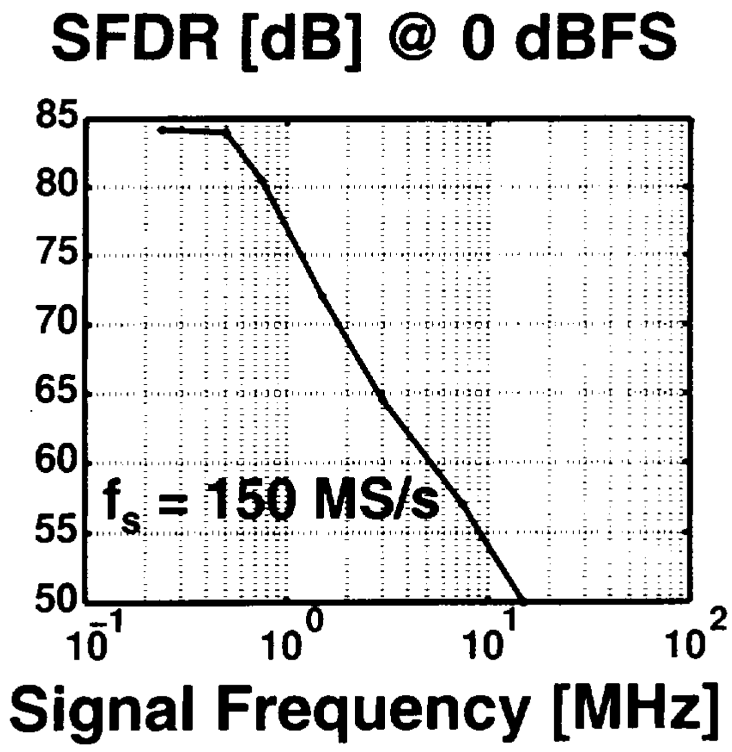
[a] *A 14-bit, 150MS/S Update Rate Q^2 Random Walk CMOS DAC*, J.Vandenbussche *et al*, International Solid-State Circuits Conference, February 1999

CMOS Untrimmed DAC - Performance





- Almost 15-bit static performance from device matching
- Dynamic performance dropoff enhanced by large switching node parasitics
- 10MHz IF - $\approx$ 55dB SFDR

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[a] *A 14-bit 100MS/S CMOS DAC Designed for Spectral Performance*, A.R.Bugeja, B.S.Song, P.L.Rakers, and S.F.Gillig, International Solid-State Circuits Conference, February 1999