A 14-b 100MS/s CMOS DAC Designed for Spectral Performance

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Outline

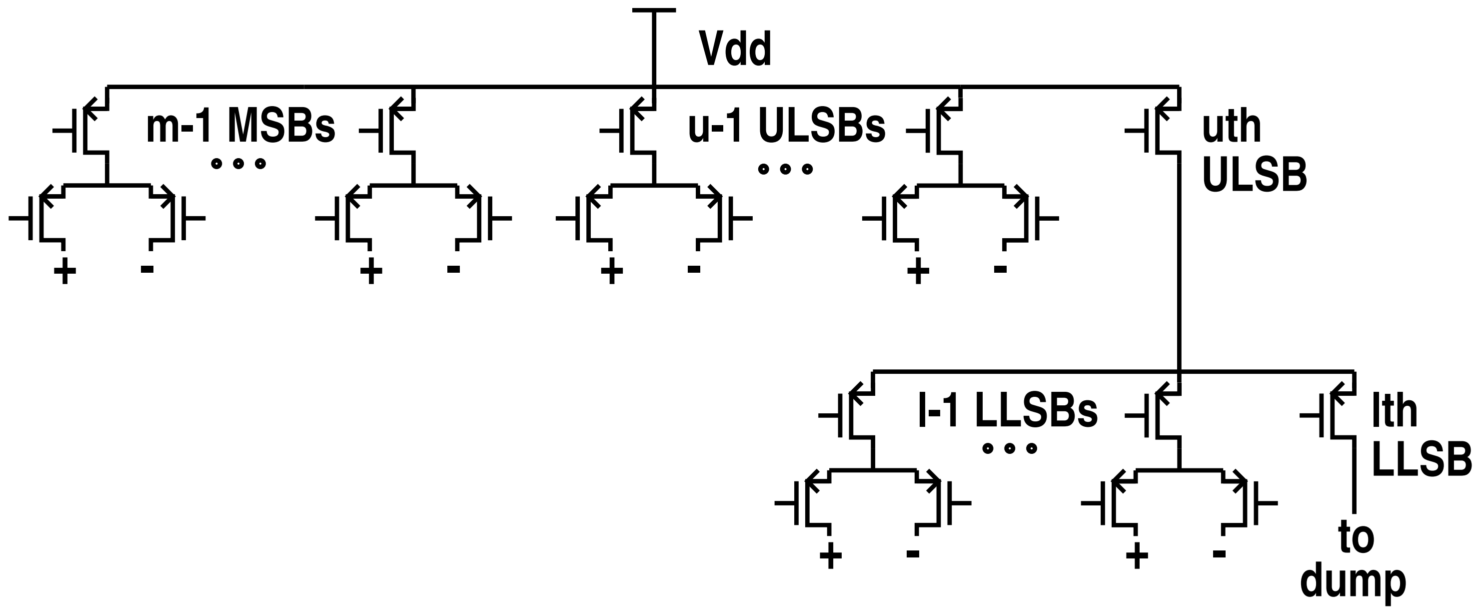
I. Introduction

II. Linearity Enhancement Technique

III. Experimental Results

IV. Conclusion

Conventional DAC Architecture

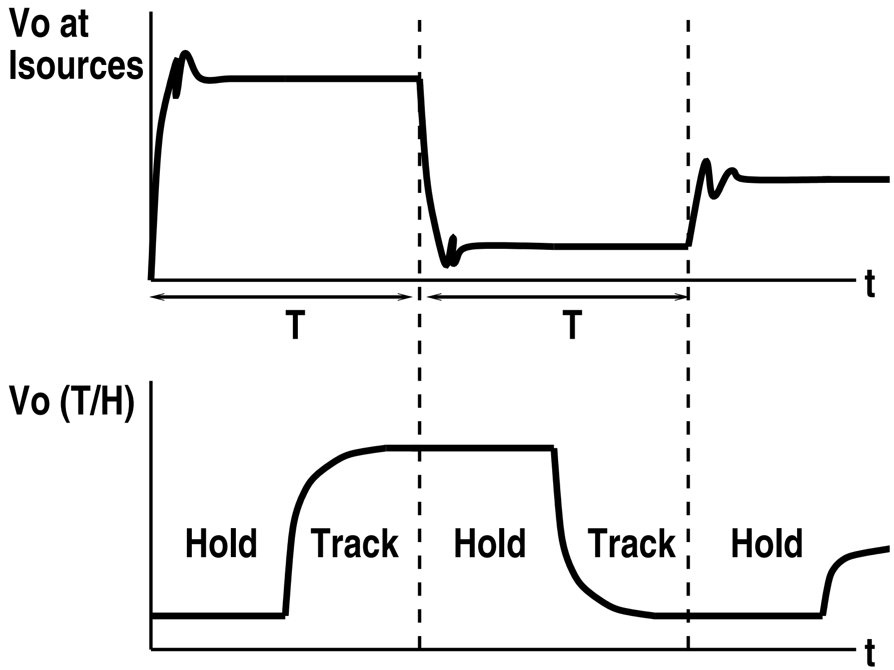


- Thermometer-coded MSBs
- Thermometer-coded ULSBs
- Binary-coded LLSBs
- Current outputs fed directly to resistive load.

Conventional DACs - Dynamic Nonlinearities

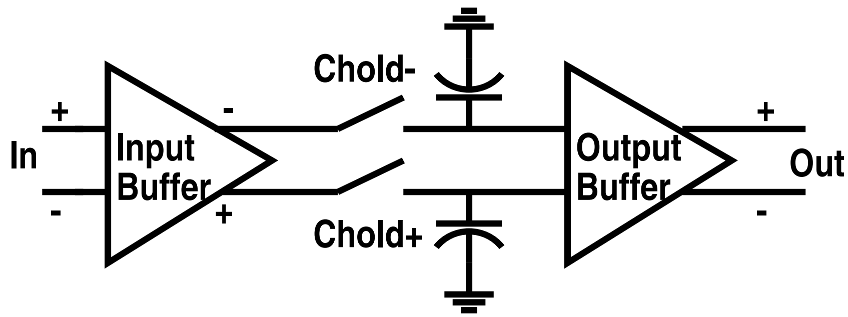
- Code-dependent settling time constants
- Code-dependent switch feedthrough
- Timing skew between current sources
- Glitch at major carries
- Increase as signal frequency increases.

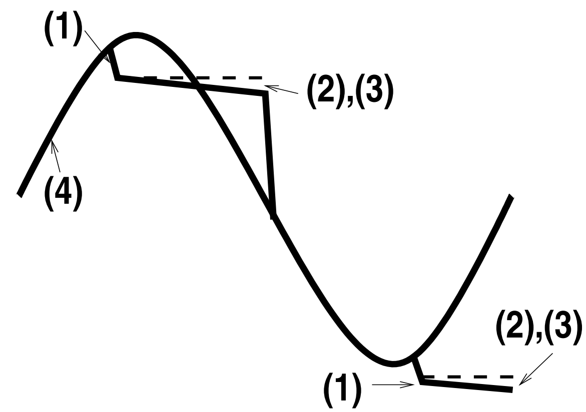
Track/Hold Stage at DAC Outputs



- Ideally track/hold corrects dynamic nonlinearities.
- Track settling should be linear function of signal.

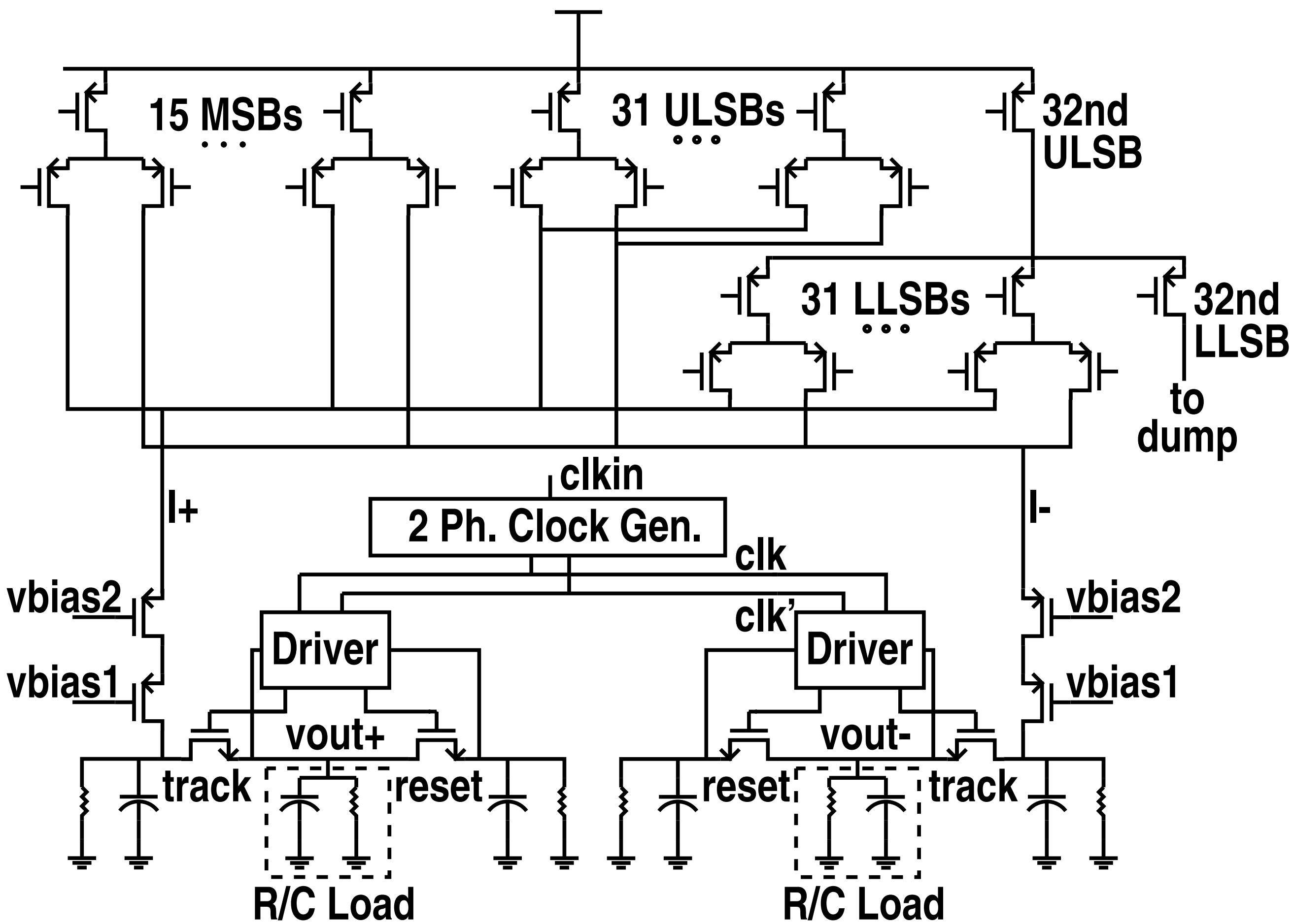
Problems of Track/Hold Circuits



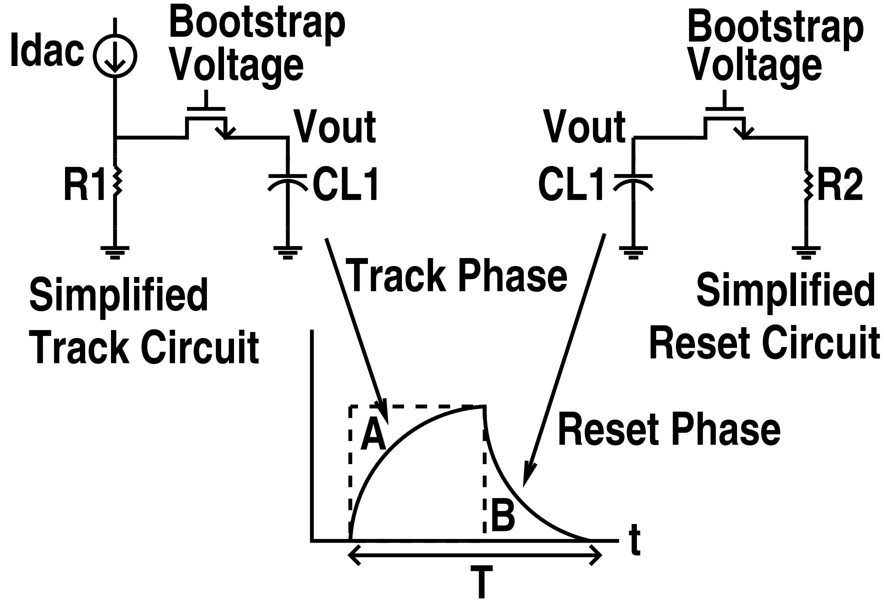


- Track-to-hold step (1)
- Droop rate error (2)
- Hold mode feedthrough (3)
- Track mode charging/discharging errors (4)

Return-to-Zero High Speed DAC



Return-to-Zero Action

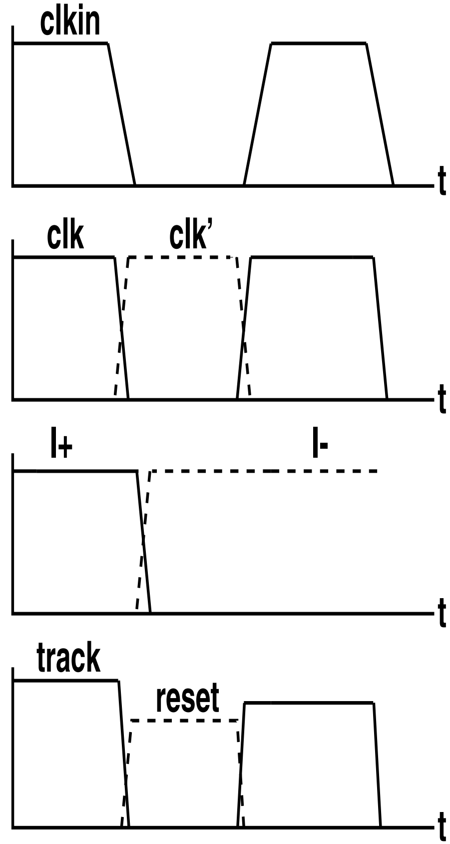


Return-to-Zero Output Waveform

A-Error During Track Phase

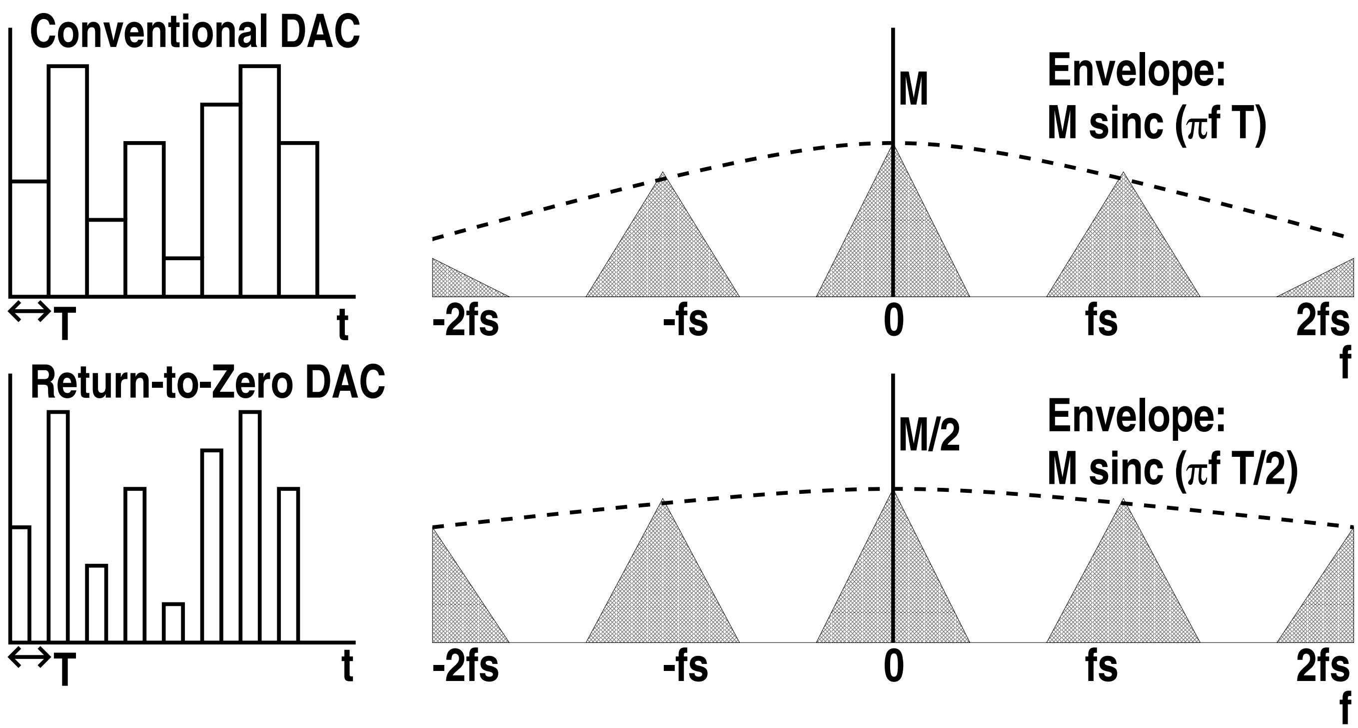
B-Error During Reset Phase

Timing Diagram



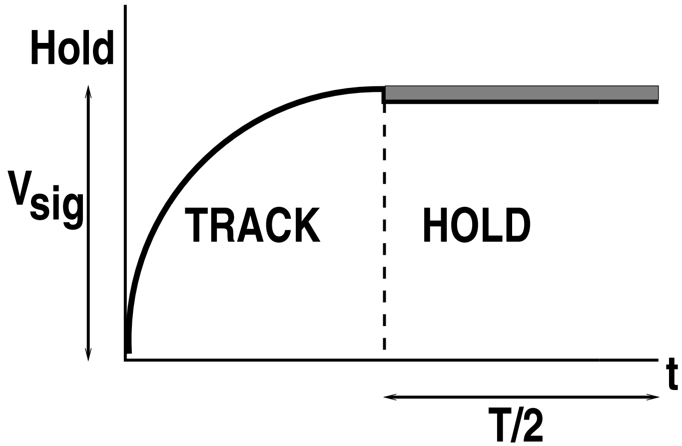
Track/Reset switch precedes Current switch.

Spectrum - Theoretical Considerations

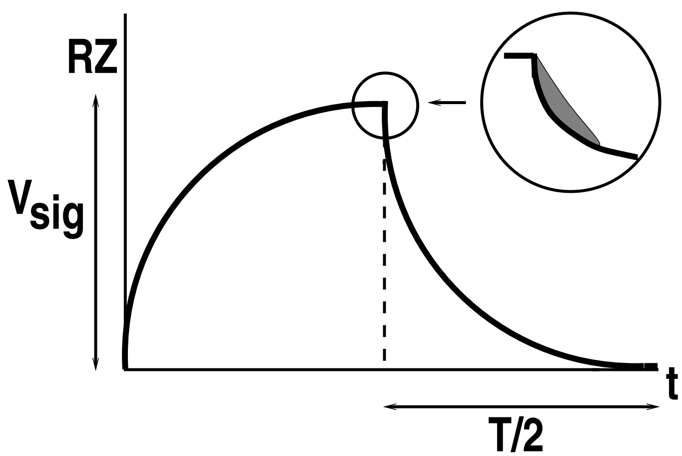


- Conventional DAC has more output power.
- RZ DAC has flatter spectrum envelope.

RZ vs. Track/Hold

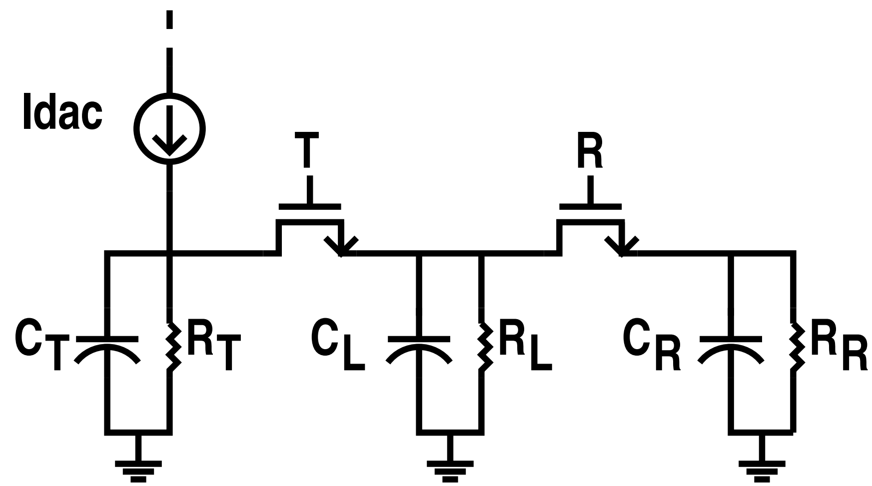


$$\text{Error} = \frac{T\ Q_{INJ}}{2C_L}$$



$$\text{Error} = \tau\,\frac{Q_{INJ}}{C_L}\left[1 - \text{Exp}\left(-\frac{T}{2\tau}\right)\right]$$

Practical Linearity Considerations



- R_{on}, Q_{CH}, C_J all scale with switch size.
- N-well process: n-devices optimize switch size.
- High differential symmetry

Treshold Voltage Effect

- 1st-order model:

$$V_{TH} = k + \gamma\sqrt{(2\Phi_f + V_S)}$$

- Expanding in series form:

$$V_{TH} = k + \gamma\left(\sqrt{2\Phi_f} + \frac{V_S}{2(2\Phi_f)^{\frac{1}{2}}} - \frac{{V_S}^2}{8(2\Phi_f)^{\frac{3}{2}}} + \ldots\right)$$

- Model V_{TH} as $V_{TH} = k + k'V_S$.
- k' is constant (k'<1).

(V_{GS}-V_{TH})-dependent Switch Operation

- 1st-order model:

$$R_{ON} = \frac{1}{\mu_n C_{OX} \left(\frac{W}{L}\right)(V_{GS} - V_{TH})}$$

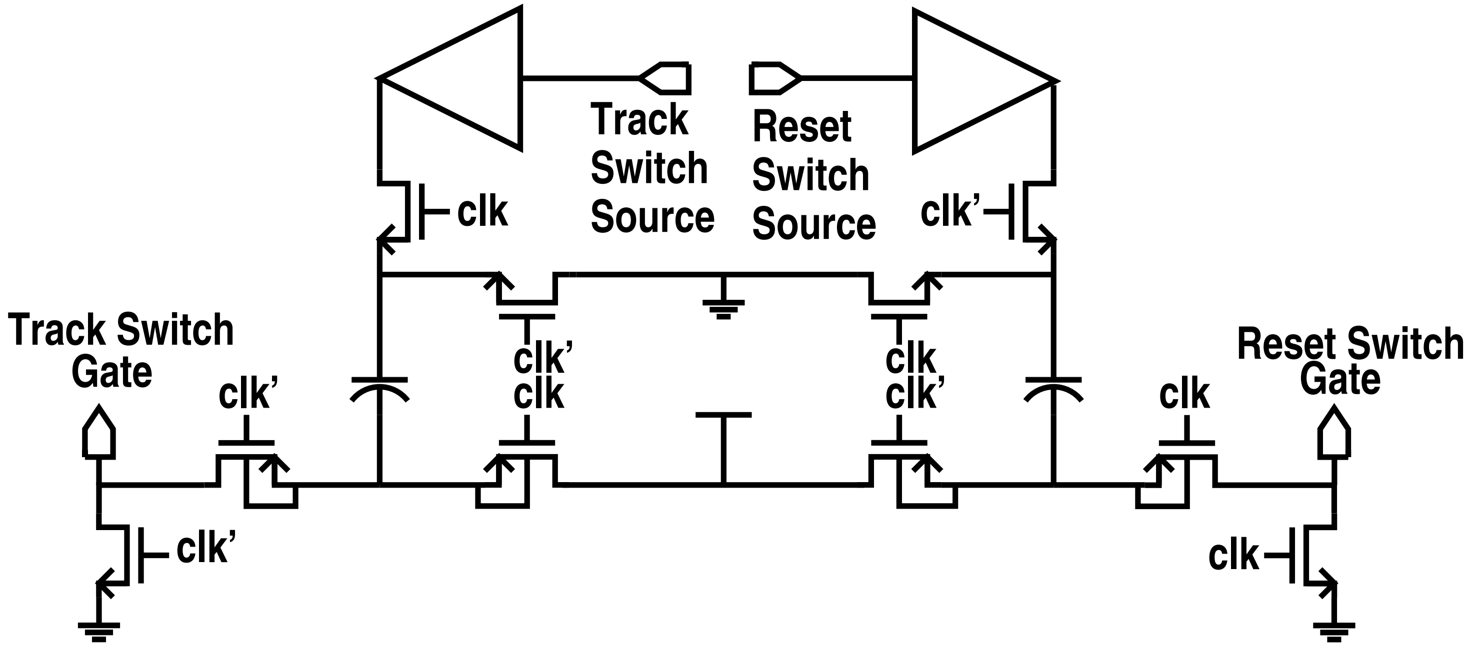
$$Q_{CH} = -(W\ L\ C_{OX})(V_{GS} - V_{TH})$$

- Constant (V_{GS}-V_{TH}) term desirable.

- Bootstrap such that V_{GS} ~ k'' + k'V_S.

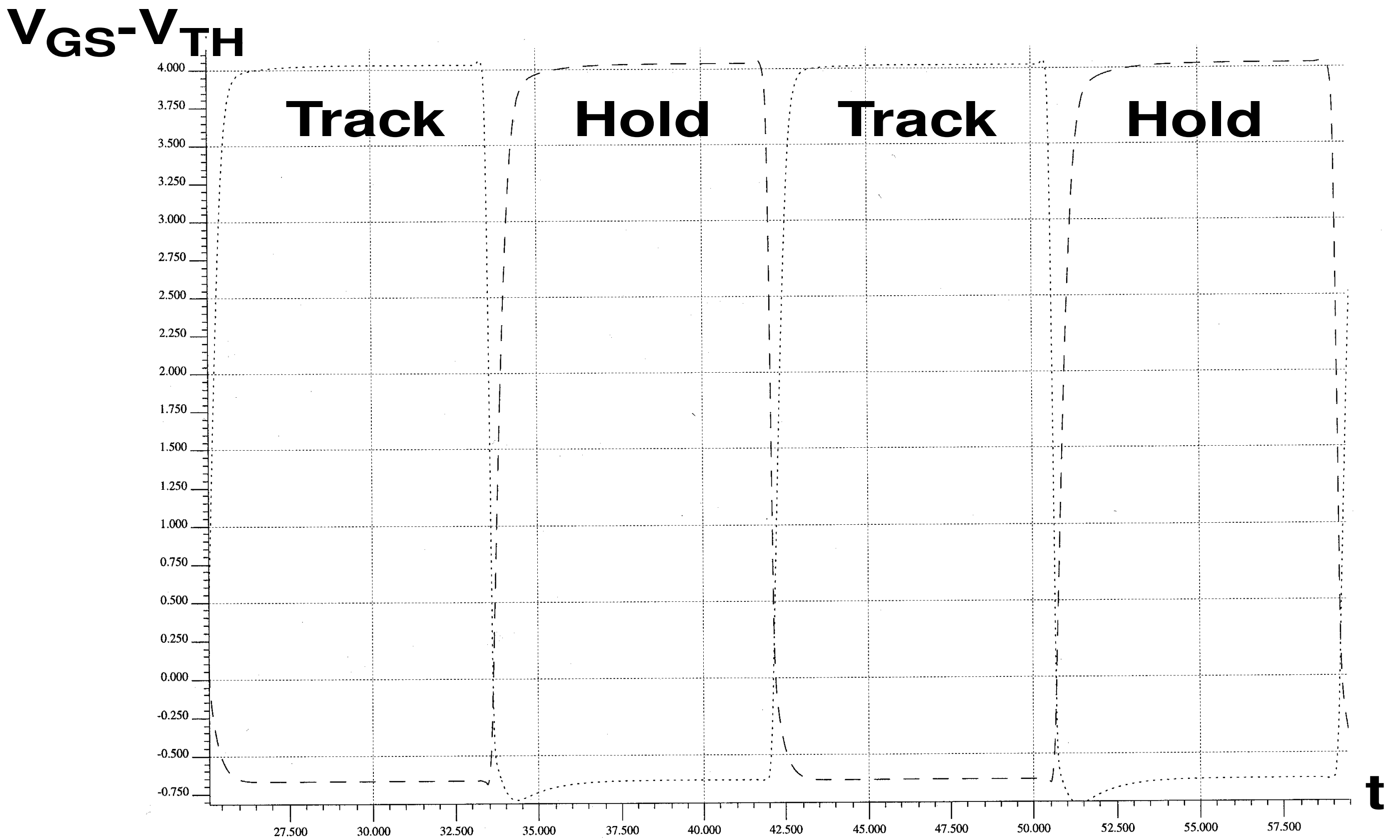
- (V_{GS}-V_{TH}) ~ constant.

Bootstrapping Circuit



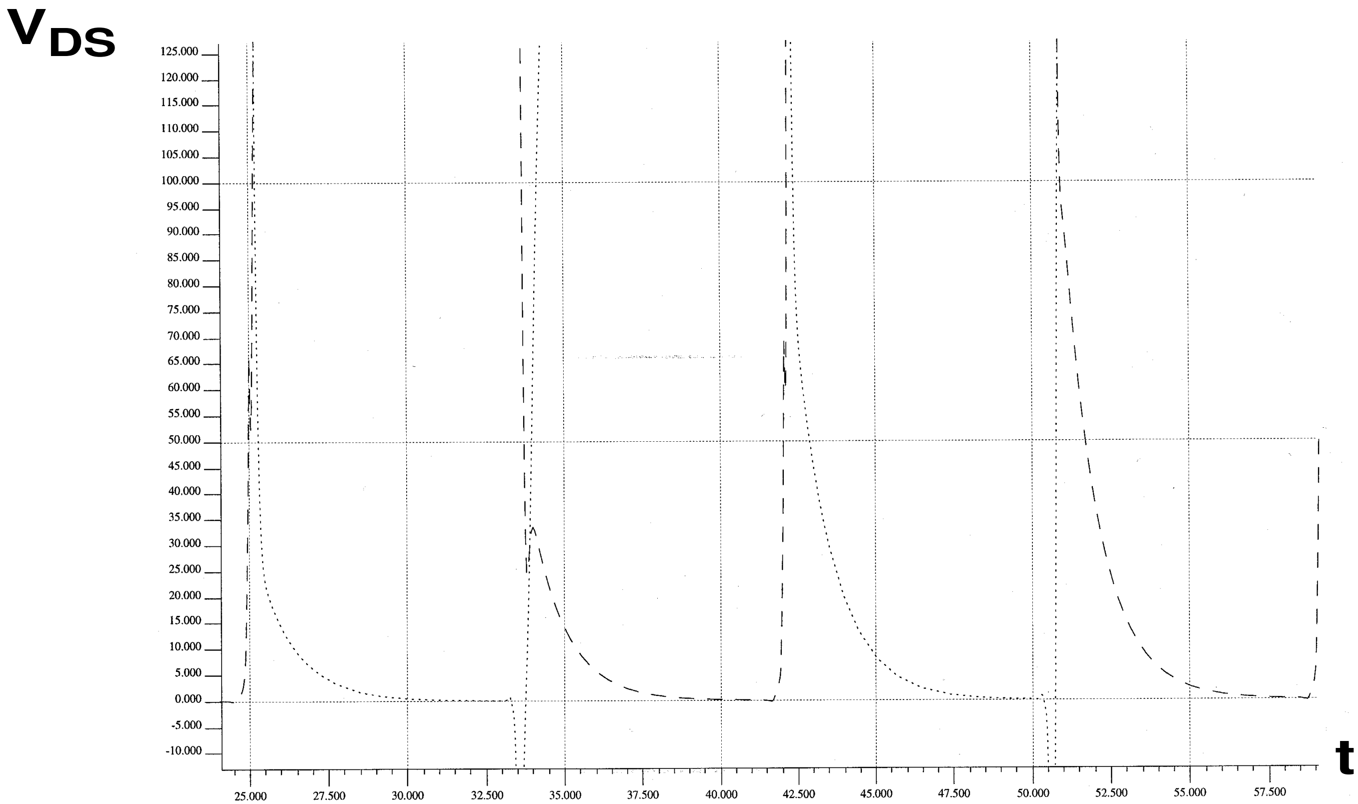
Buffer compensates for V_{TH}, capacitive divider loss.

Bootstrap Circuit Simulation



V_{GS}-V_{TH} ~ constant (Track-to-Reset, Cycle-to-Cycle)

Simulated Nonlinearity Cancellation



- Symmetrical V_{DS} behavior built into circuit.
- Point-to-point track/reset nonlinearity matching

Example: Switch Resistance

Including V_{DS} dependency:

$$R_{ON} = \frac{1}{\frac{\partial I_D}{\partial V_{DS}}} = \frac{1}{\mu_n\ C_{OX}\left(\frac{W}{L}\right)(V_{GS} - V_{TH} - V_{DS})}$$

- **V_{GS}-V_{TH} kept constant by bootstrapping circuitry.**
- **V_{DS} matched point-by-point from track to reset.**
- **R_{ON} matched point-by-point from track to reset.**

Junction Capacitance Nonlinearities

$$C_J = \frac{C_{Jo}}{\sqrt{1 + \frac{V_{JB}}{\Psi_o}}}$$

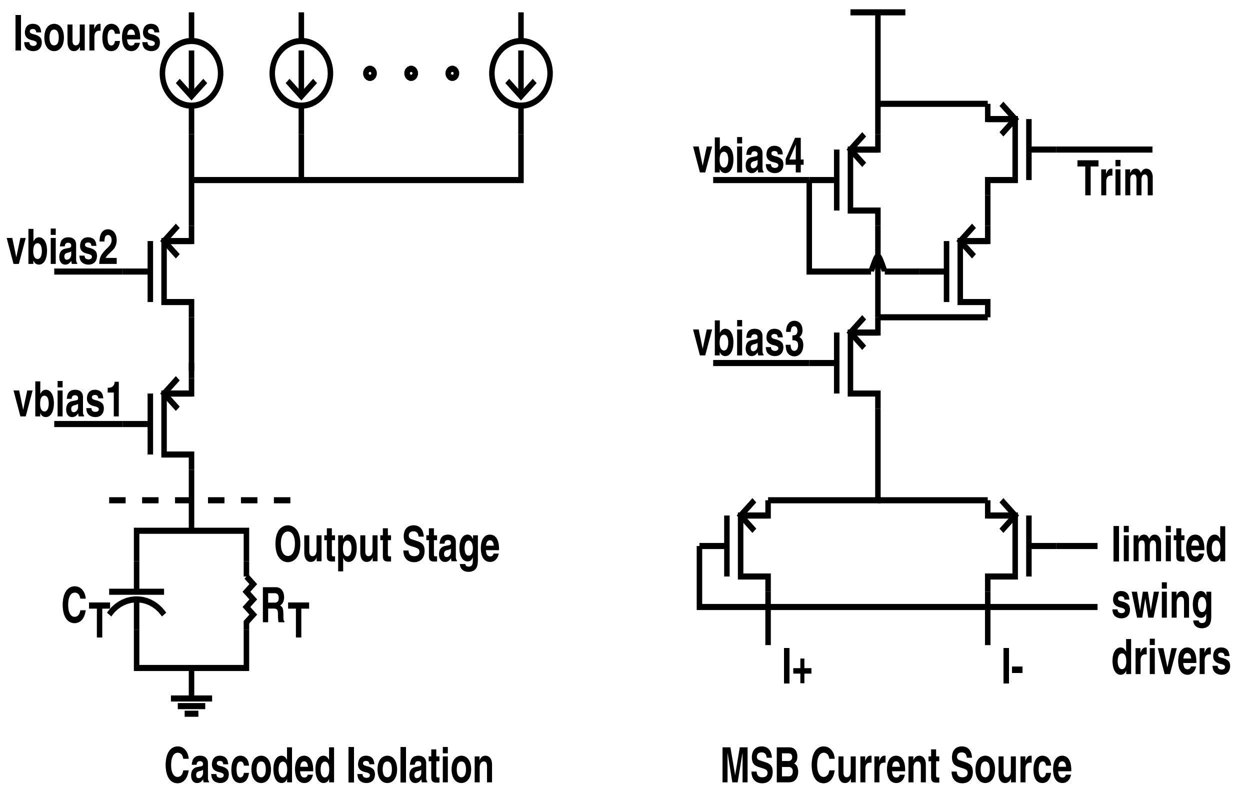
- Larger nonlinear terms than V_{TH}.

- Simulate C_J in test circuit with ideal components:

$$C_{TOT} = C_K + \frac{C_X}{\sqrt{1 + \frac{V_{OUT}}{\Psi_o}}}$$

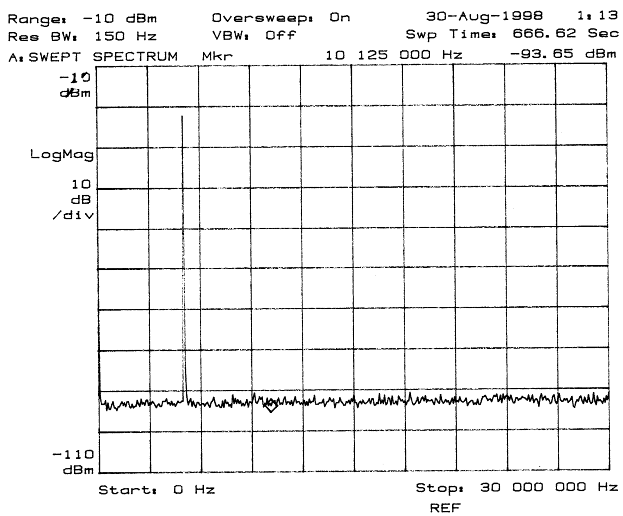
- Differential SFDR >98dBc requires $C_X:C_K < 1:30$.

Isolation Circuitry

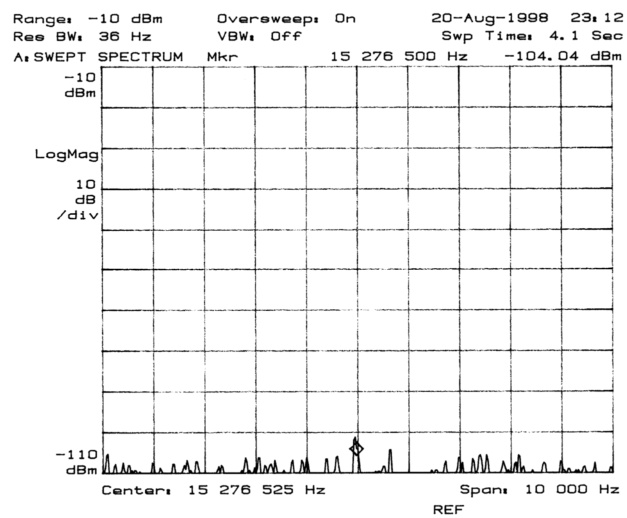


- Cascode circuitry common to all DAC.
- Individually cascoded current sources

Experimental Results - LF Spectra



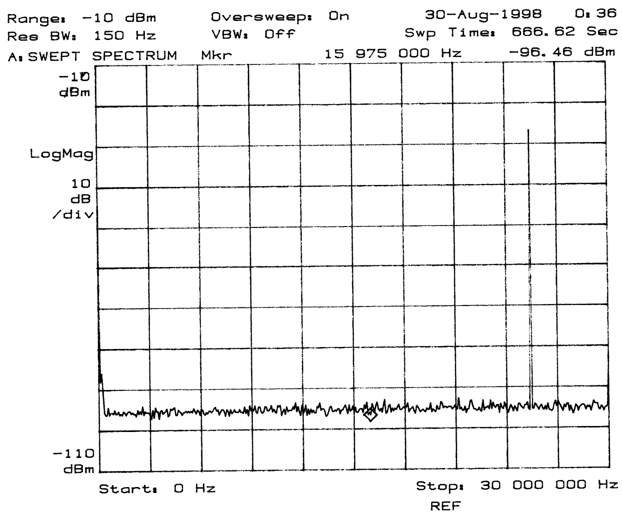
(a)



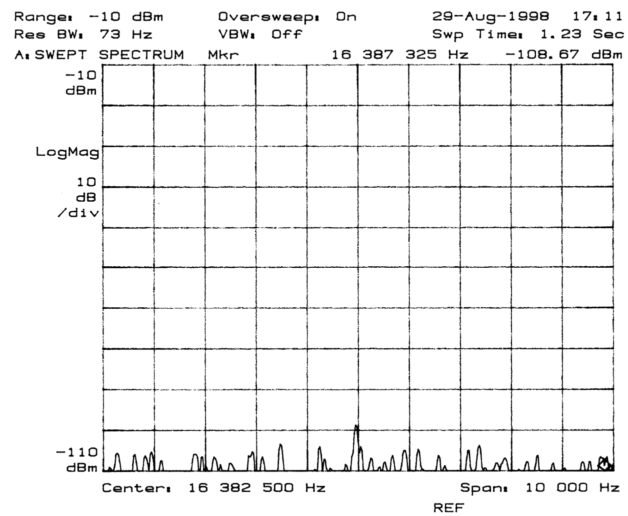
(b)

(b) is closeup of largest spur on same vertical axis.

Experimental Results - HF Spectra



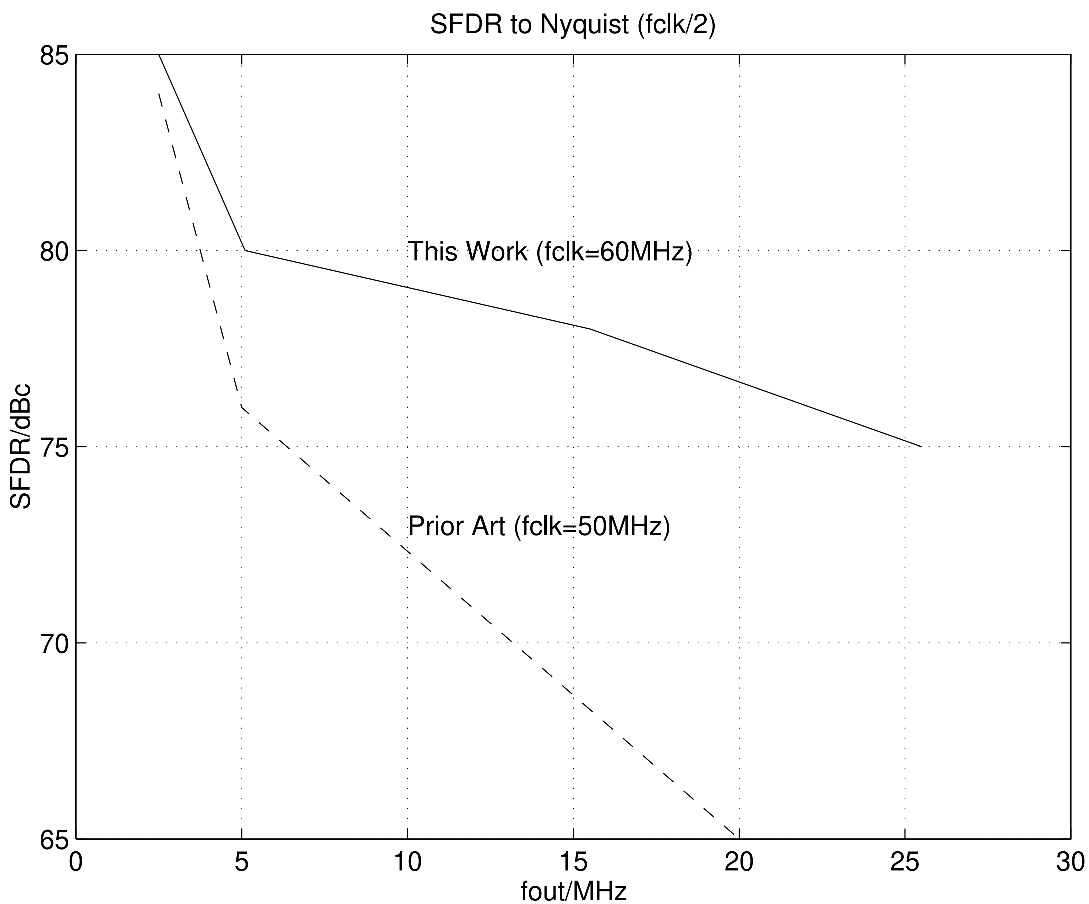
(a)



(b)

(b) is closeup of largest spur on same vertical axis.

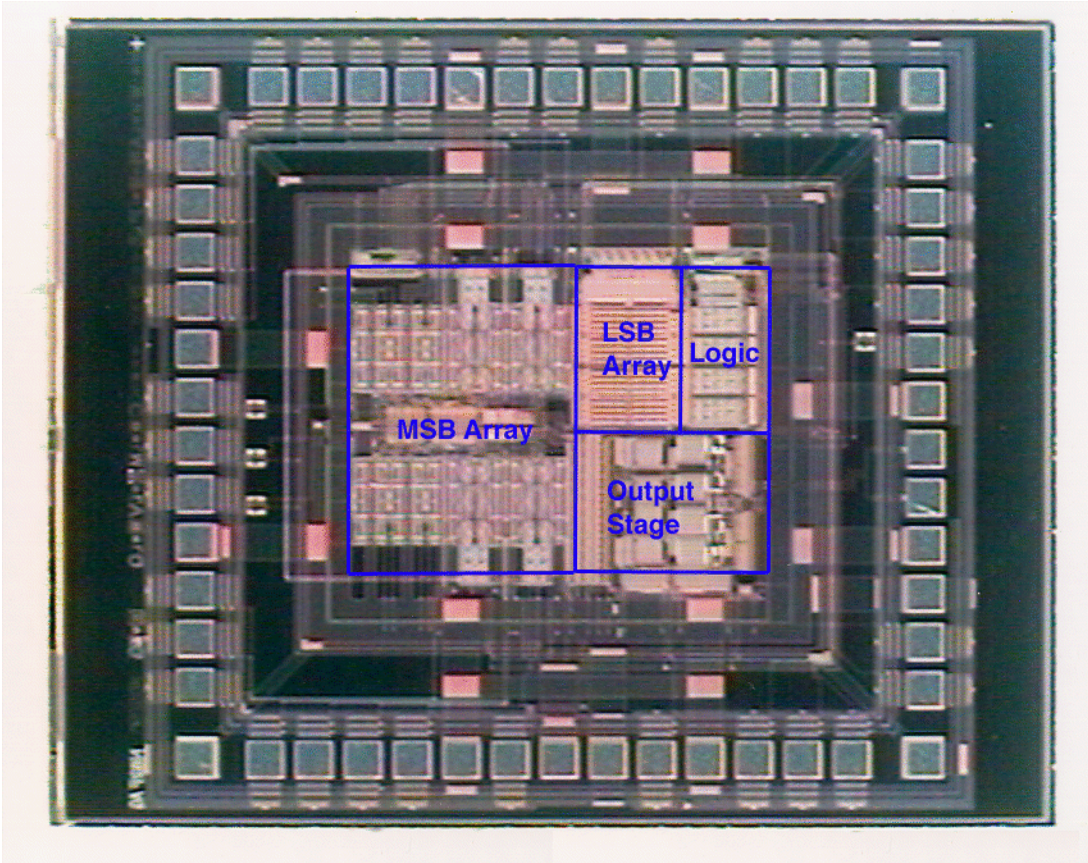
Comparison with Prior Art



Summary of the Work

Resolution	14-bit
Update Rate	100MS/s
Load	50Ω, tested at up to 30pF
Output Swing	1Vp-p differential, transformer coupled
Power Dissipation at 5V	750mW (100MS/s)
Die Area (0.8μm CMOS)	3.69 x 3.91 sq. mm

Die Photograph



Conclusions

Demonstrated high speed/dynamic linearity DAC.

Key features:

- **Differential linear RZ output stage**
- **Tracking at midcycle to avoid switch-on transients**
- **Fast settling current-mode DAC**
- **Isolation of output stage from current-mode DAC**