Variability and SRAM Design

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Apr 23, 2008

Outline

- What's the problem?
- Bit Cell related design techniques
- Non-Bit Cell related design techniques
- Conclusion

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- Non-Bit Cell related design techniques
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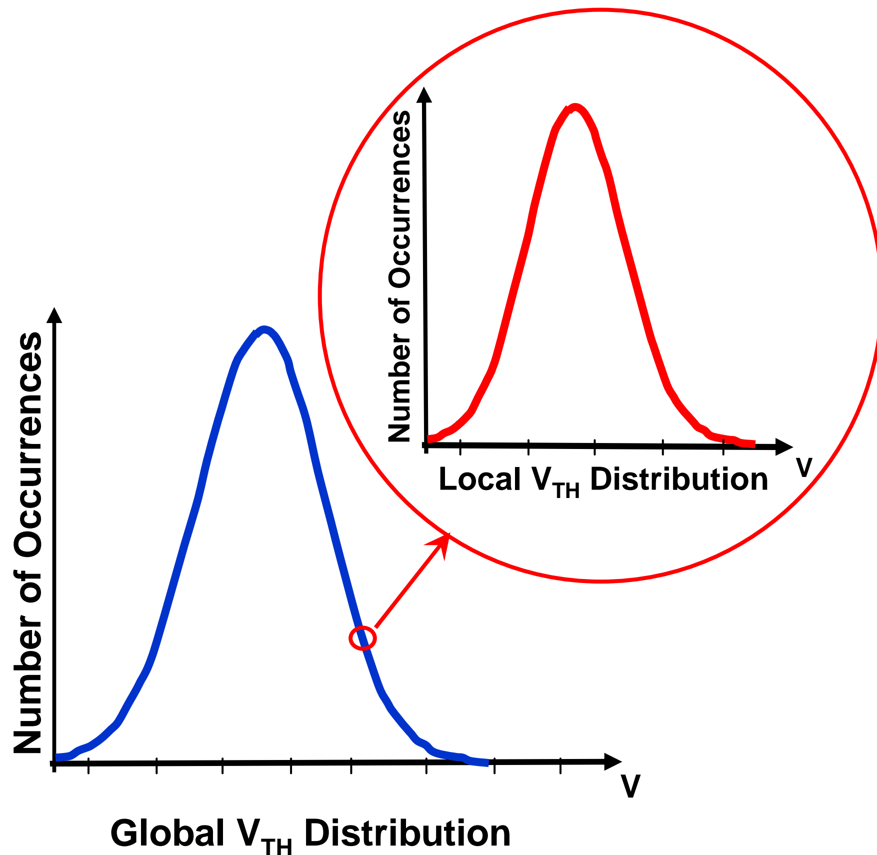
What's the problem?



Sources of "Within Die Variation"

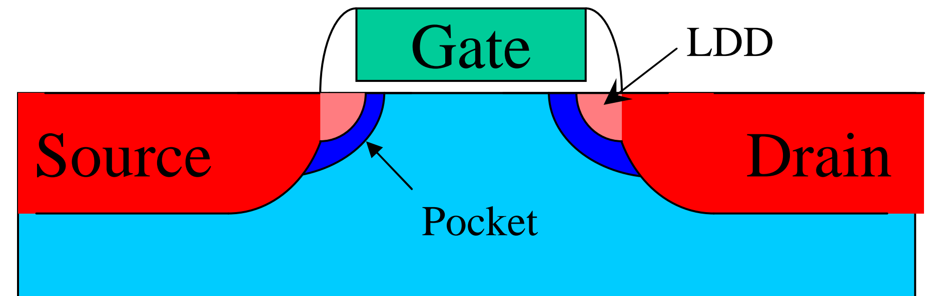
- Random Dopant Fluctuations (RDF)
- Line Edge Roughness (LER)
- Gate Stack (t_{OX}, etc.)
- Lithography (ACLV, edge effects, etc.)
- Temperature and temperature gradients
- Different sensitivity to back gate bias
- Hot Carriers
- NBTI

⇨ *Local transistor mis-match:*

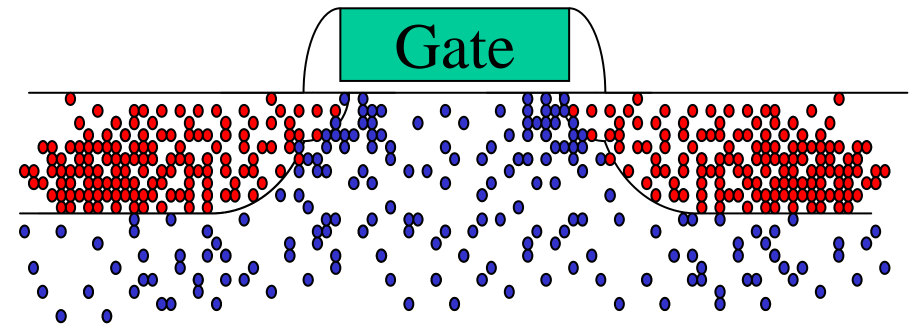
$$\sigma_{Vth} = \sqrt{\sigma^2_{Vth}(RDF)+\sigma^2_{Vth}(LER)+\sigma^2_{Vth}(other)}$$

Random Dopant Fluctuation (RDF) [2]

- Statistical variation in the number and placement of dopants in the channel



- At 32nm it is expected the channel doping may only be made up of <100 atoms.



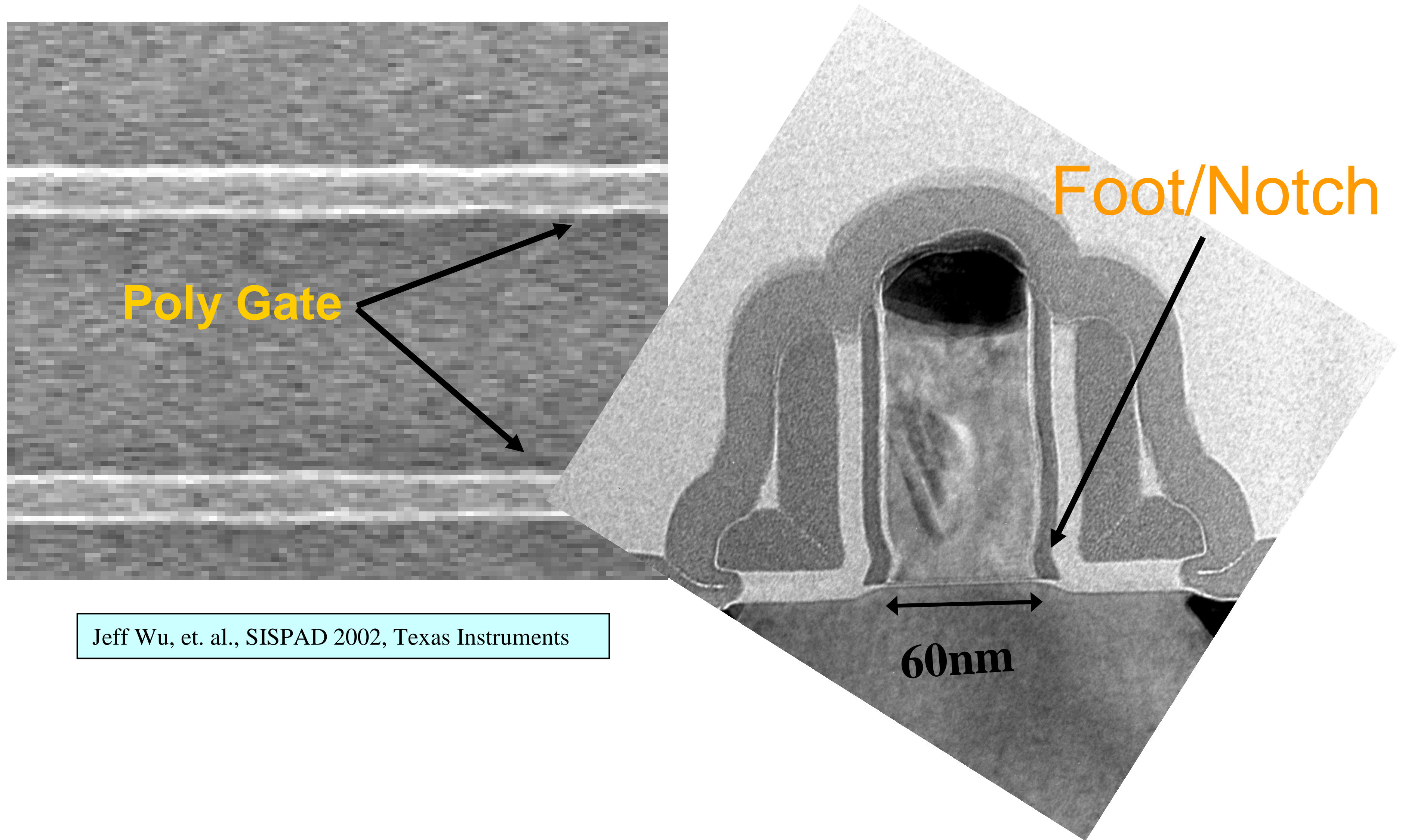
David Scott, ISSCC 2007 Short Course, Texas Instruments

- The variability of V_{th} due to RDF:

$$\sigma_{Vth} \propto 1/\sqrt{(WL)}$$

SRAM bit cell devices will have a higher σV_{th} than the logic devices, due to the channel area difference

Line Edge Roughness (LER) [3]



Jeff Wu, et. al., SISPAD 2002, Texas Instruments

What's the problem for SRAM's?

Variability in the SRAM Bitcell

- Difficult to reduce the Operating Voltage (VDD_{MIN})
  - Read Fails (SNM)
  - Write Fails (VTRIP)
  - Access Fails (I_{READ} or I_{CELL})
  - Data Retention Fails (V_{HOLD})
- Increased leakage (IDDQ Fails)

Variability in the Sense Amp

- Increased input offset for differential BL sensing
- Decreased accuracy of timing tracking circuits
- Shifted trip points for large signal sensing

What are the consequences?

Scaling less than Entitlement

- Bit Cell & SRAM area is scaling less than 50%:
  - 65nm: bit cell area > 0.50um^2
  - 45nm: bit cell area > 0.25um^2
- Difficult to get SRAM performance scaling
- SRAM VDD is not scaling
- SRAM leakage is increasing

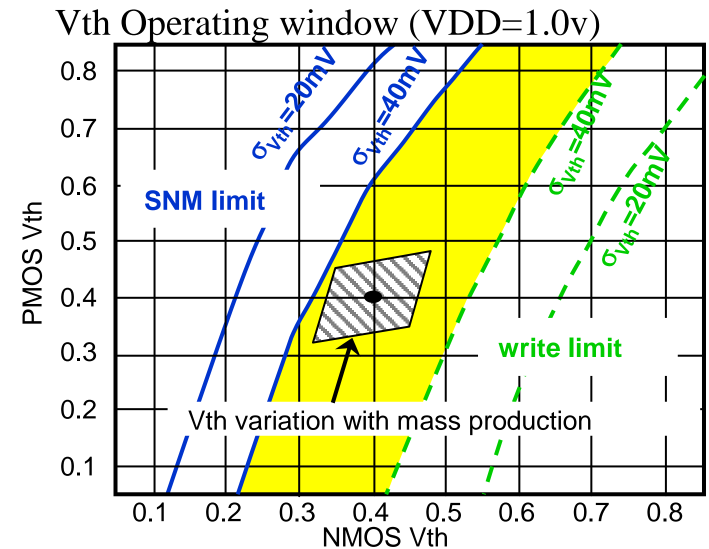
- What's the problem?
- Bit Cell related design techniques
  - Minimum Operating voltage
  - Read Margin improvement
  - Write Margin improvement
  - Alternative SRAM Bit Cell options
  - IDDQ improvement
- Non-Bit Cell related design techniques
- Summary

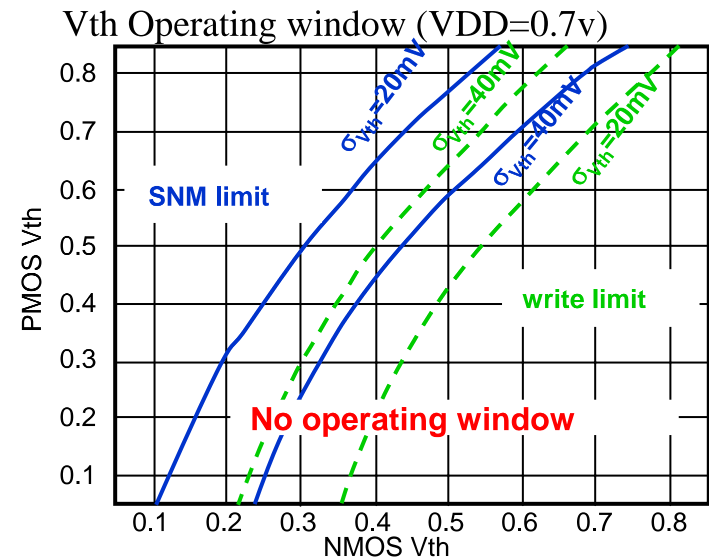
VDD_{MIN} Failures [6]

- The SRAM bit cell is much more sensitive to lowering VDD than standard logic gates

- The SRAM bit cell is a ratioed circuit which depends on the relative strengths of its transistors

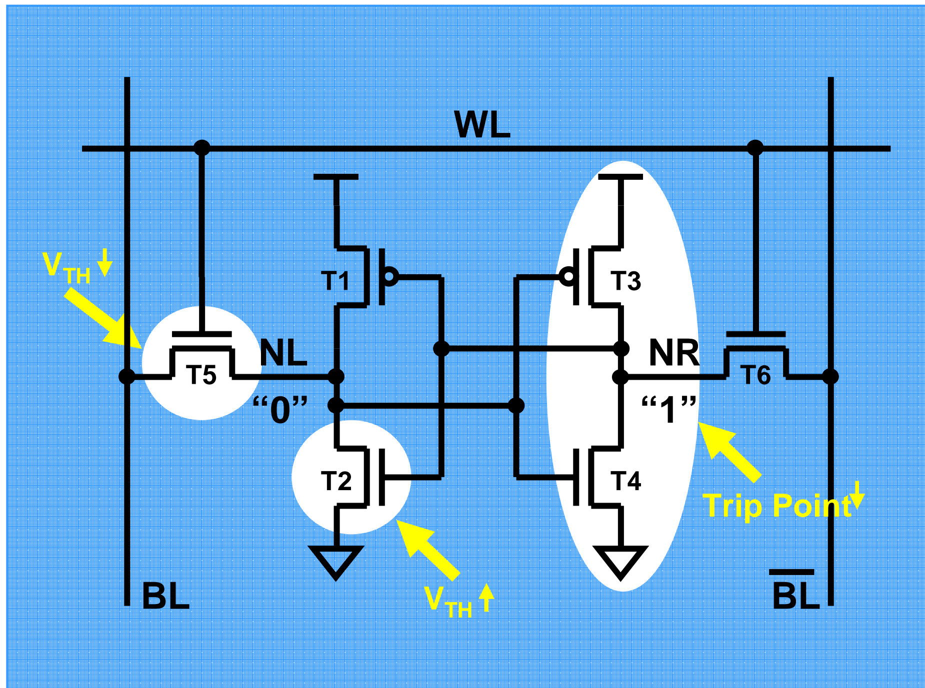
- <u>Every</u> bit cell must work properly

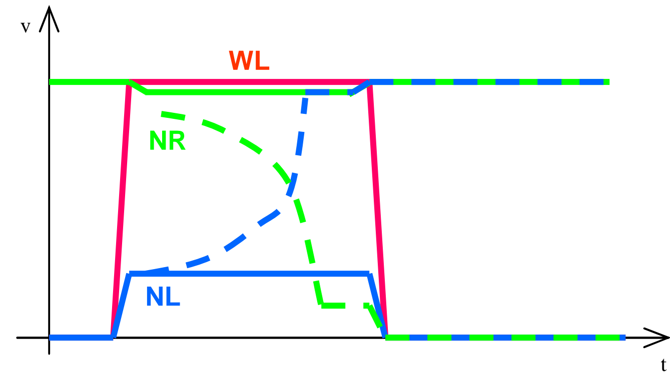




Diagrams: Masanao Yamaoka, et. al., VLSI 2004, Hitachi

READ Failures (SNM)

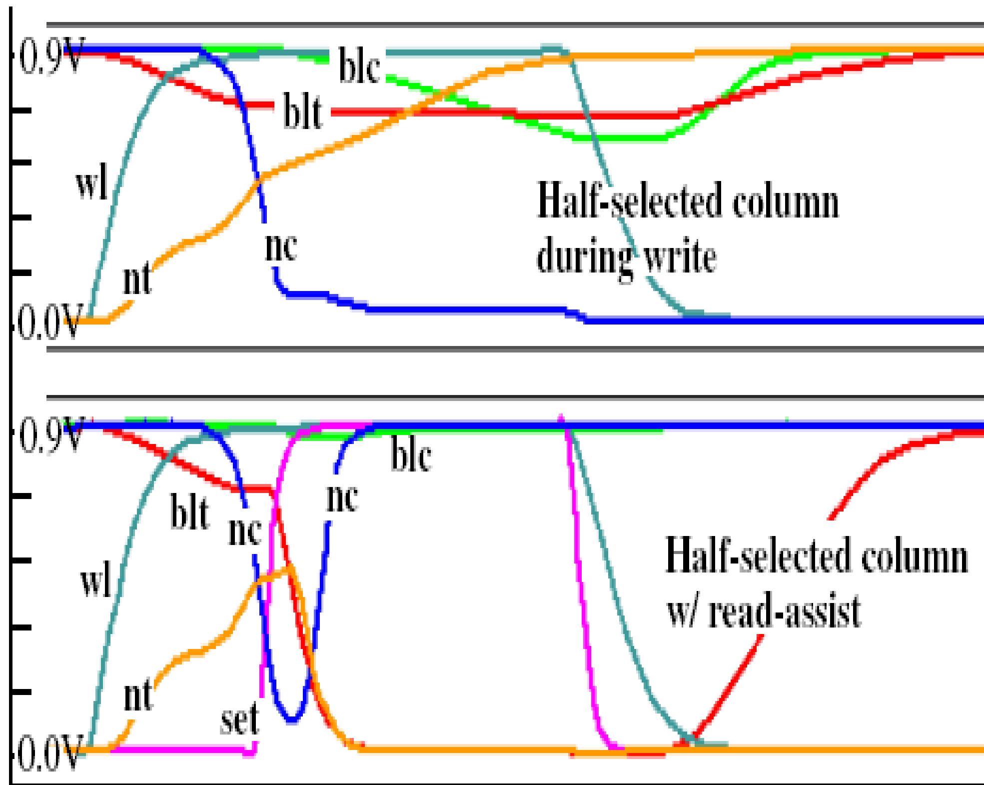




Device	Vth M/M for Read Failures
T1	Decrease
T2	Increase
T3	Increase
T4	Decrease
T5	Decrease
T6	Increase

- When the WL turns on node NL will rise due to voltage divider action between T5 and T2
- If this level is higher than the trip point on of the INV(T3,T4) the latch will loose it's state: Read Failure

Read Assist: Read & Write-Back

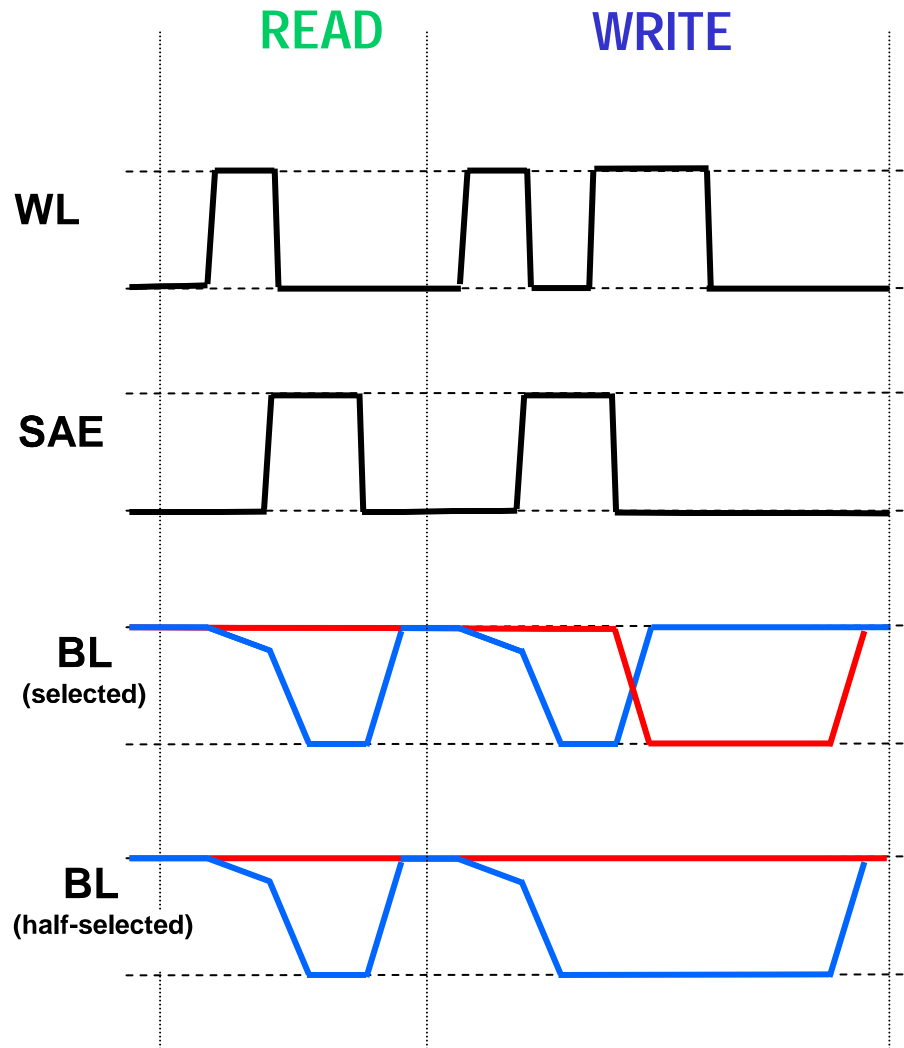


Waveforms: Harold Pilo et. al.; VLSI 2006, IBM

- SRAM's typically use a multiplexed column architecture
- Columns with an active wordline, but not being accessed are "half-selected" columns
- The half-selected BL's have the greatest chance of causing an upset due to longer time the BL is at a high level

- Placing a sense amp on every column amplifies the half selected columns on every read and write cycle (eliminating the half-selected state)

Read Assist: Pulsed Wordline (PWL) [8]

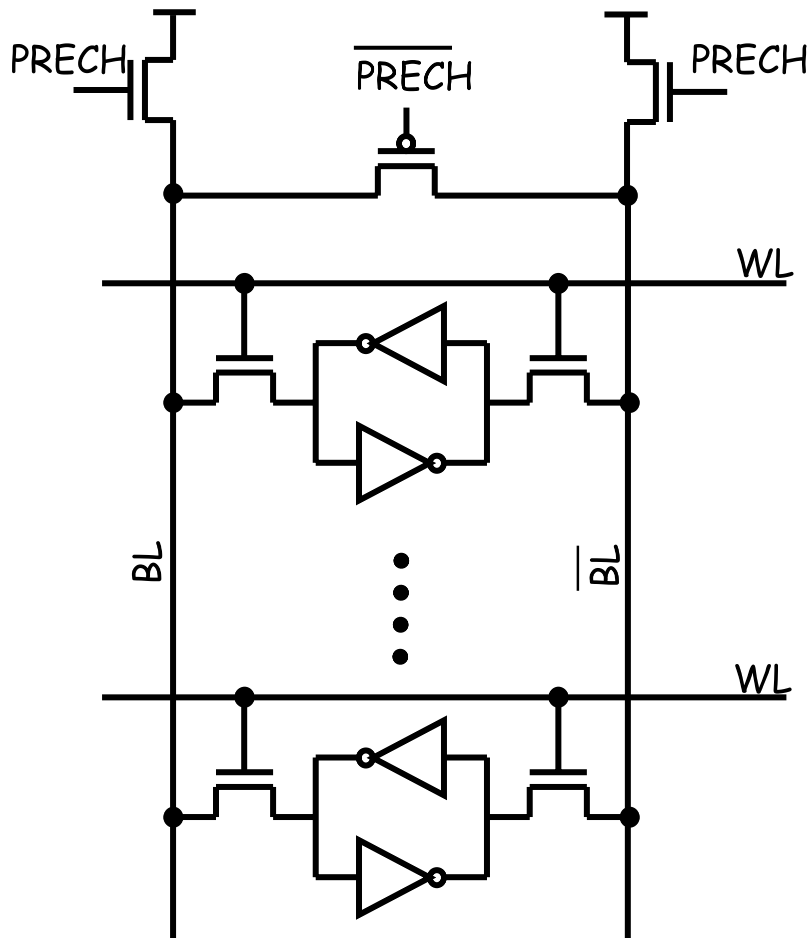


- Pulse WL only long enough to transfer signal to BL's, but not long enough to allow weak bits to flip

- Write requires wider WL pulse, so unselected columns must first be read then written back along with normal writes (aka Read-Modify-Write)

- RMW requires Sense Amp on every column

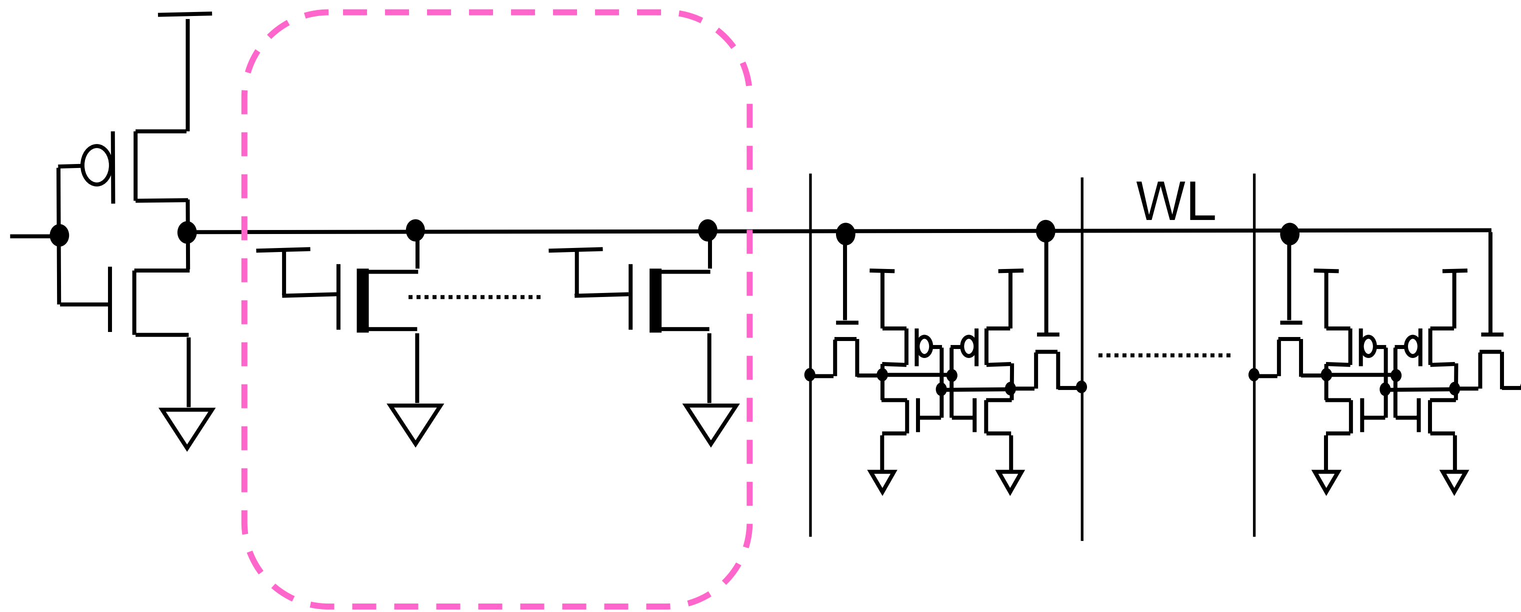
Read Assist: Lower BL Precharge [8,10]



- When the WL turns on the voltage divider action between the PG and PD causes the low node of the bit to rise
- The optimum BL precharge voltage is VDD-V_{TH}(PG) [10]
- Several proposals for generating the BL precharge voltage:
  - Precharge with NMOS
  - Pulsed BL pull-down
  - Separate/generated supply

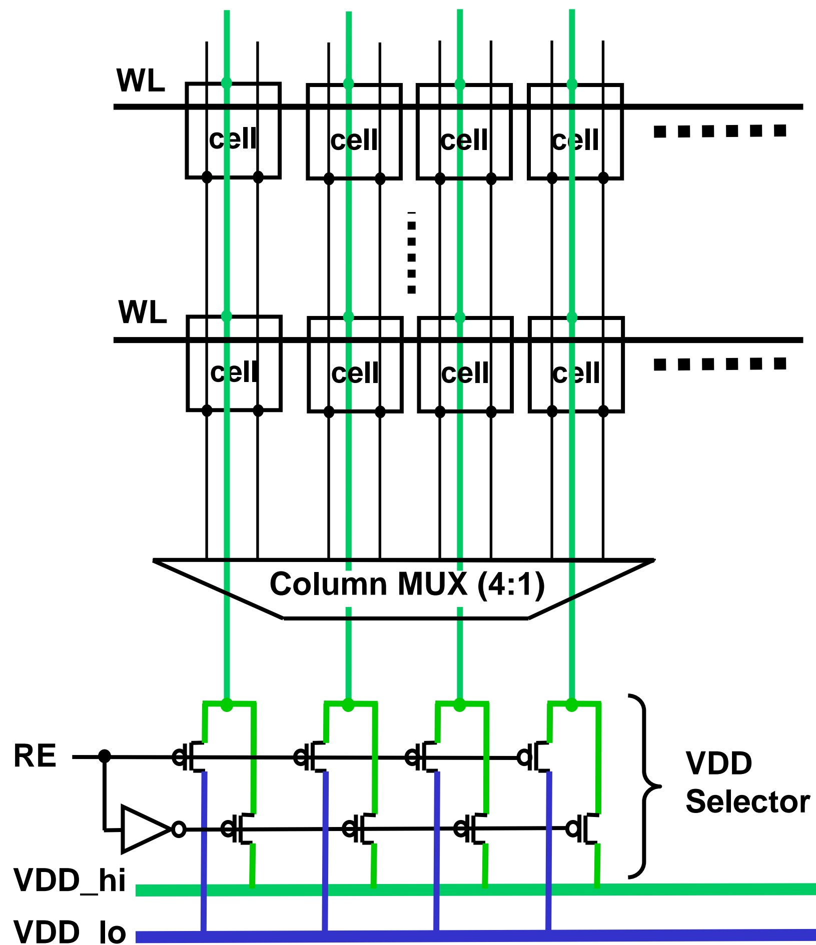
- Precharge levels below the optimum value cause a dramatic increase in fails due to disturb from the high node

Read Assist: Lower WL Level [11,12]



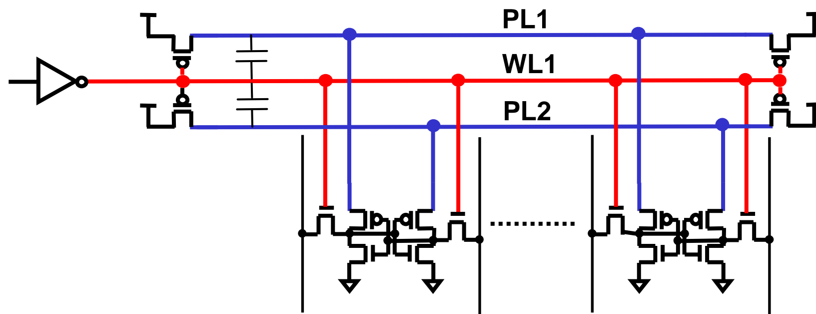
- The WL level is held below the memory VDD
- The gate drive of the Pass Gate is reduced, relative to the Pull-Down device and SNM is improved
- Read current is reduced, and write is more difficult

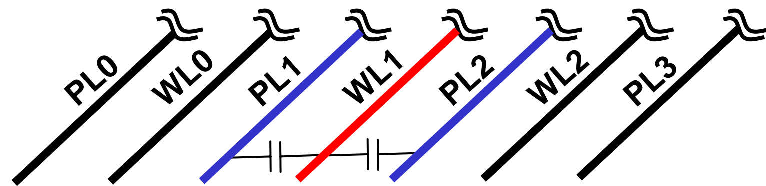
Read Assist: Raised VDD Level [15]

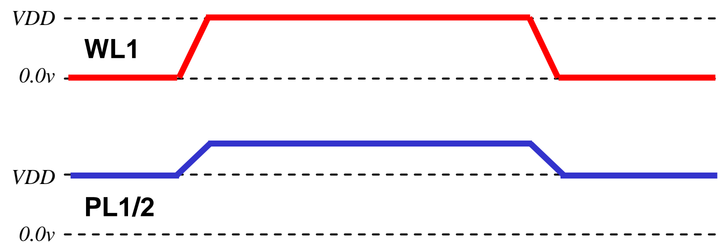


- Raise VDD level of the bit cell above the WL voltage
- This will increase the gate drive of the Pull-Down device and improve SNM
- During a read, VDD of all columns must be raised
- When the memory is inactive, the lower VDD will reduce leakage

Read Assist: Raised VDD Level [9, 13]







- Raise VDD level of the bit cell above the WL voltage, using capacitive coupling
- This will increase the gate drive of the Pull-Down device and improve SNM
- This scheme does not require additional power supplies

Review: Read Assist Techniques

- Control of the bit cell supplies can compensate for mis-match between the PG and PD transistors during a read operation and improve SNM

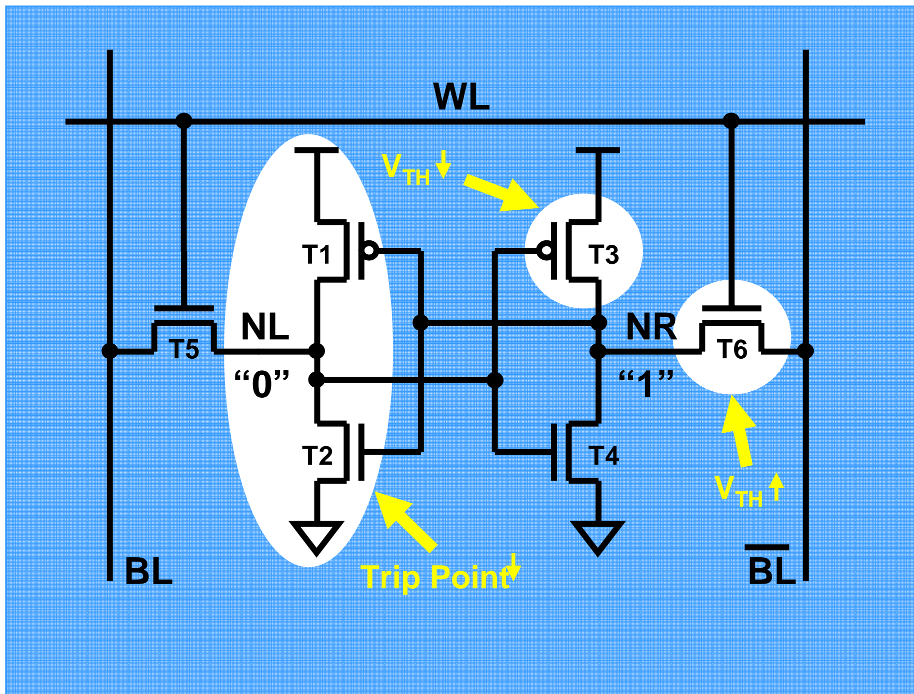
- Reduce influence of the bitline bias to stress bit cell SNM:
  - Pulsed Wordline
  - Amplify signal on all bitlines
  - Short Bitlines
  - Lower Bitline precharge level

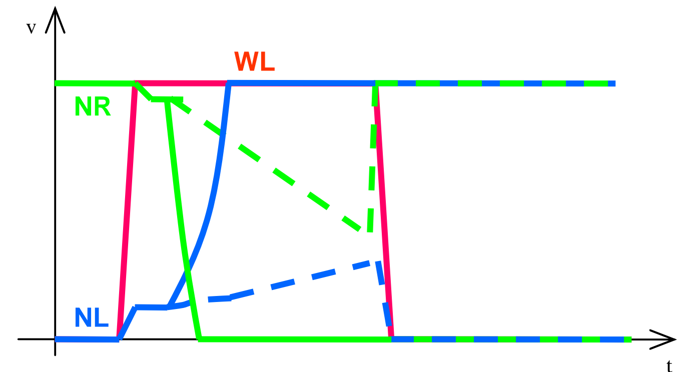
- Reduce gate drive of PG relative to PD device
  - Reduce Wordline level below the bit cell VDD level

- Increase gate drive of PD relative to PG device
  - Raise bit cell VDD above Wordline level

- Raise the trip point of the cross-coupled inverters

Write Failure





Device	Vth M/M for Write Failures
T1	Increase
T2	Decrease
T3	Decrease
T4	Increase
T5	Increase
T6	Increase

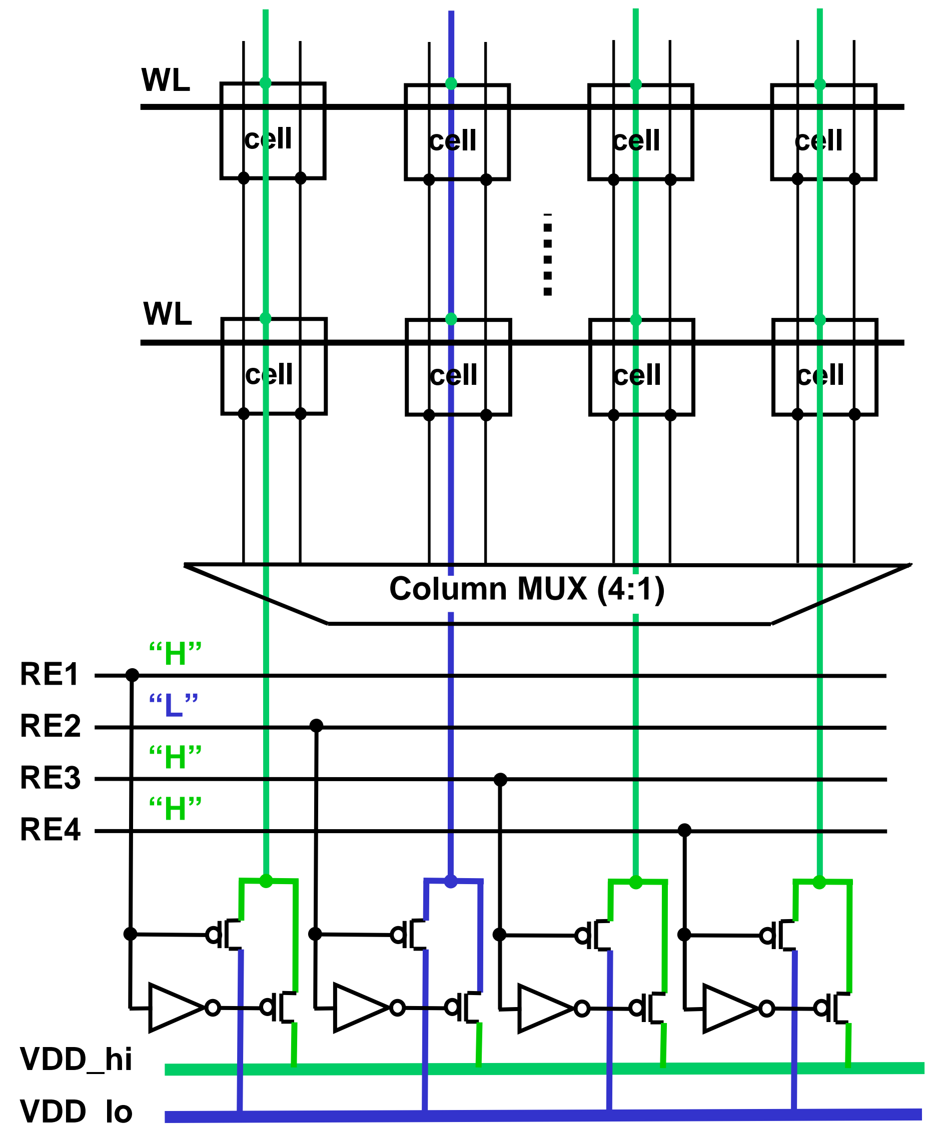
- During a write node NR must be pulled low through T6
- If NR cannot be discharged below the trip point of INV(1,2), during the WL pulse, the result is a write failure

Write Assist: Lower VDD by Column [15]

- Similar to read assist techniques, we can dynamically change rail voltages and improve the write margin of the bitcell

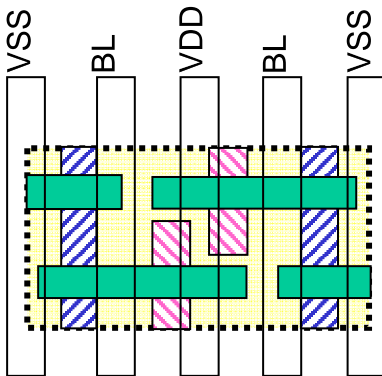
- Write margin is improved with VDD lower than the WL voltage

- The gate drive of the PU device is reduced, relative to the Pass Gate

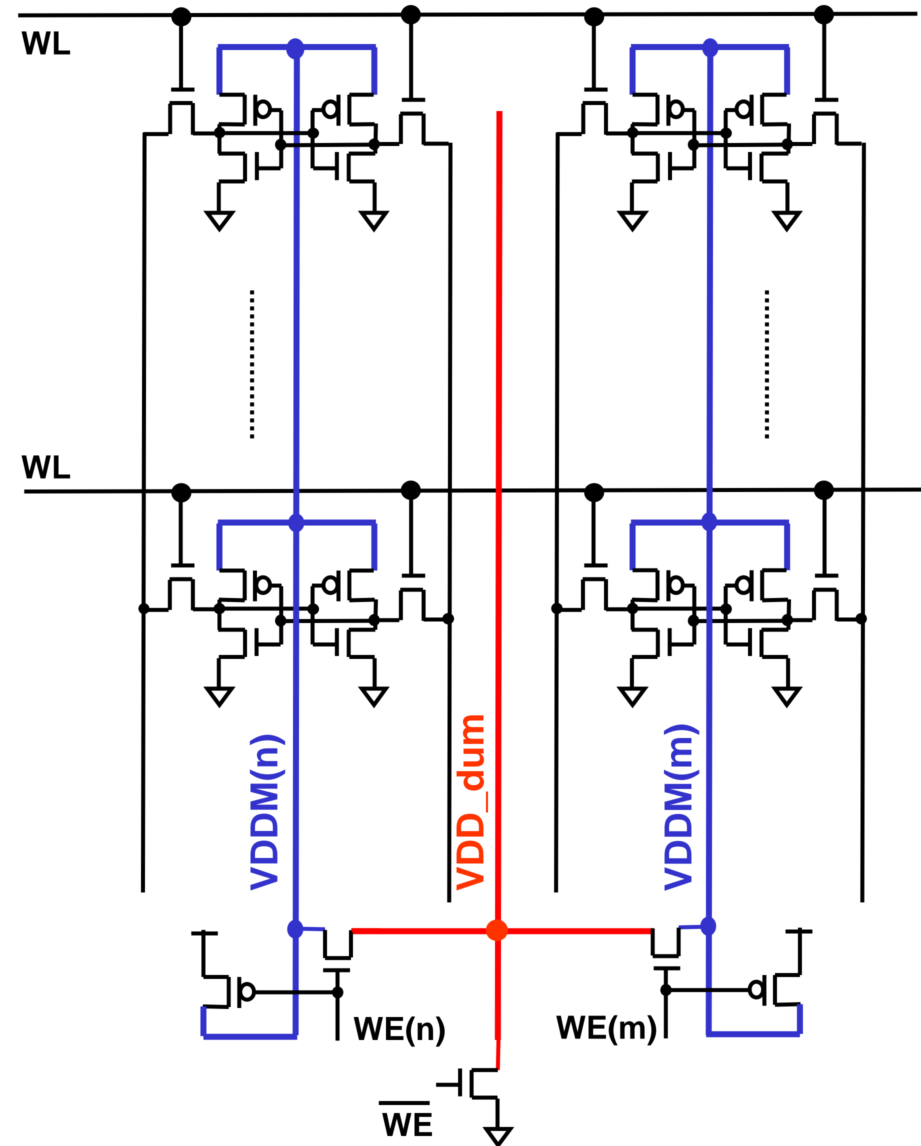


Write Assist: Lower VDD by Column [11,12]

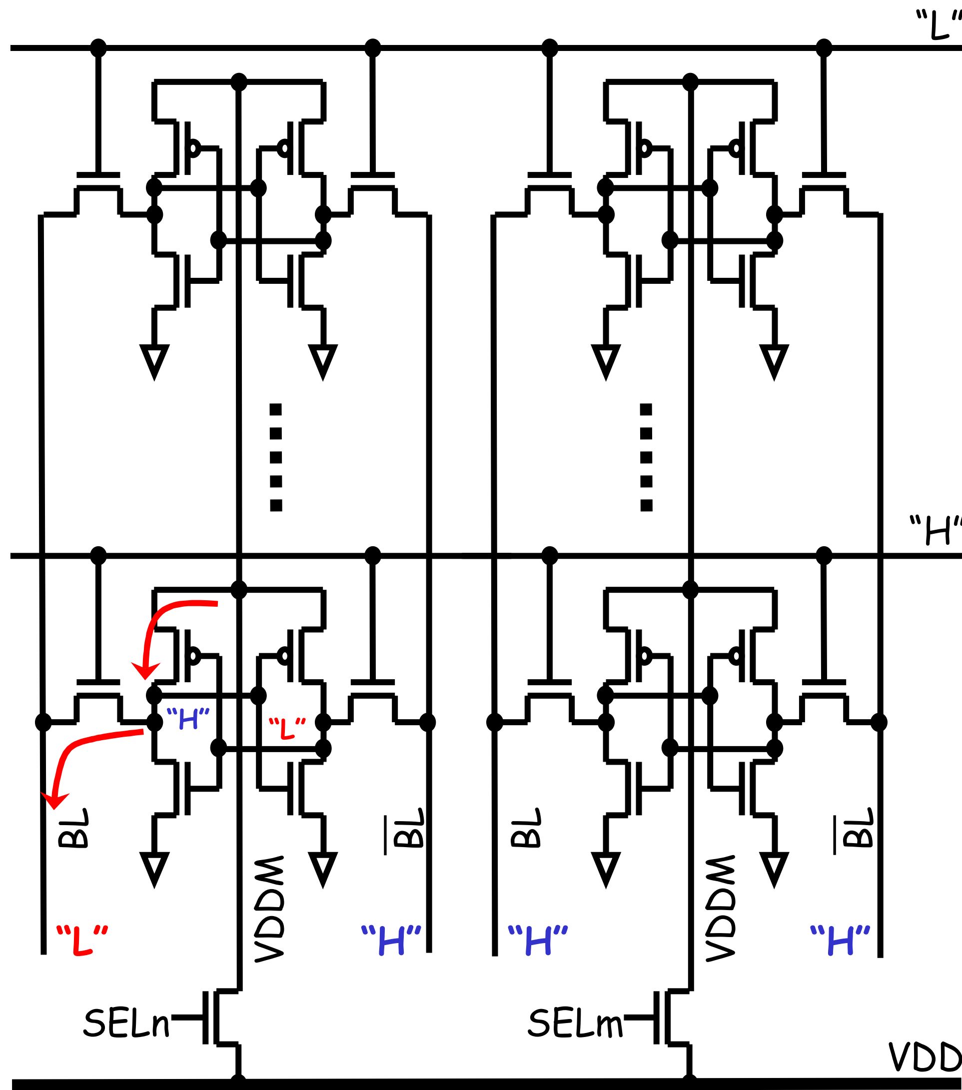
- Typically, the VDD wire is not shared between adjacent columns



- The bit cell VDD is lowered below the WL level, thru a capacitive charge sharing scheme



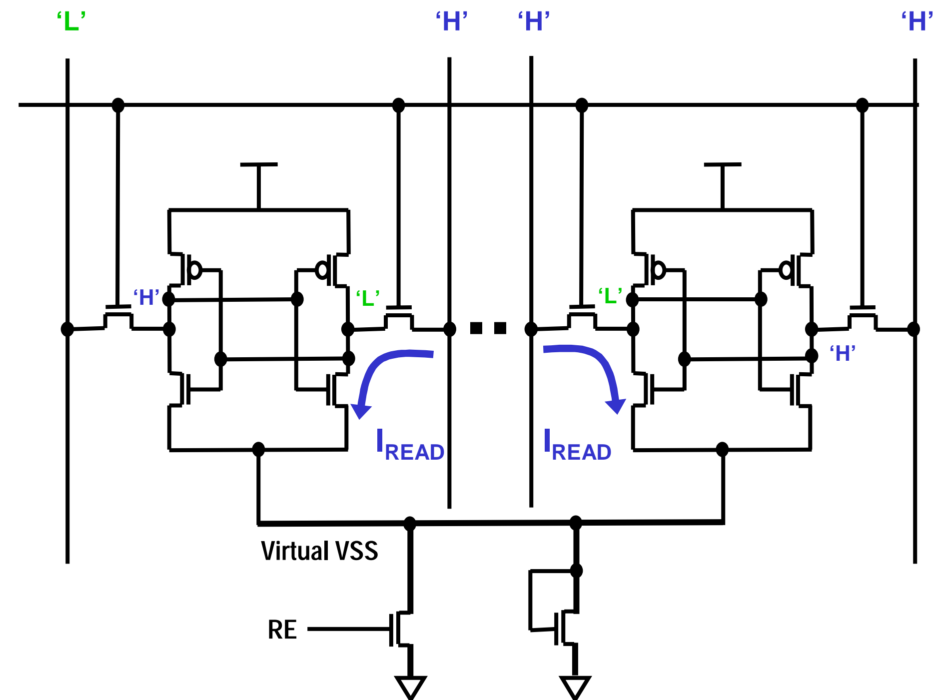
Write Assist: Lower VDD by Column [16]



- Requires separate VDD by column
- Float VDD of selected columns during a write
- This is a self-limiting technique: current flow will cease once the bit is written
- Lower VDD is shared with unselected rows along the same column

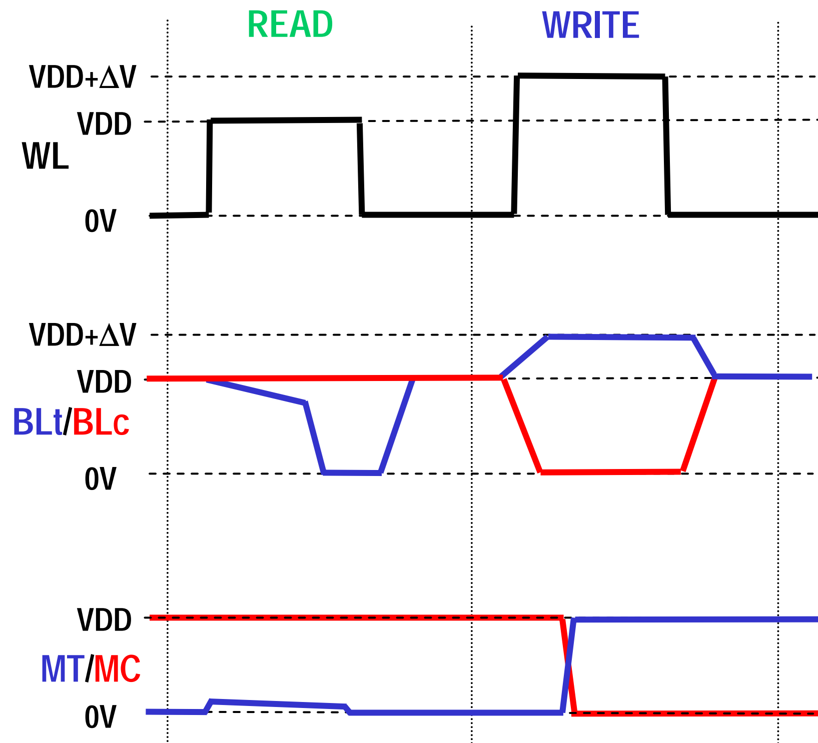
Write Assist: Raised VSS [10,17]

- During a write VSS of the bit cell is floated
- When the wordline turns on the floating VSS begins to charge up
- The raised VSS level assists the write operation



- VSS is typically shared between adjacent columns, which raises SNM concerns on half-selected columns
- Unlike the “float VDD” scheme, this technique is not self limiting, so clamp devices are required

Write Assist: Boosted WL [18]



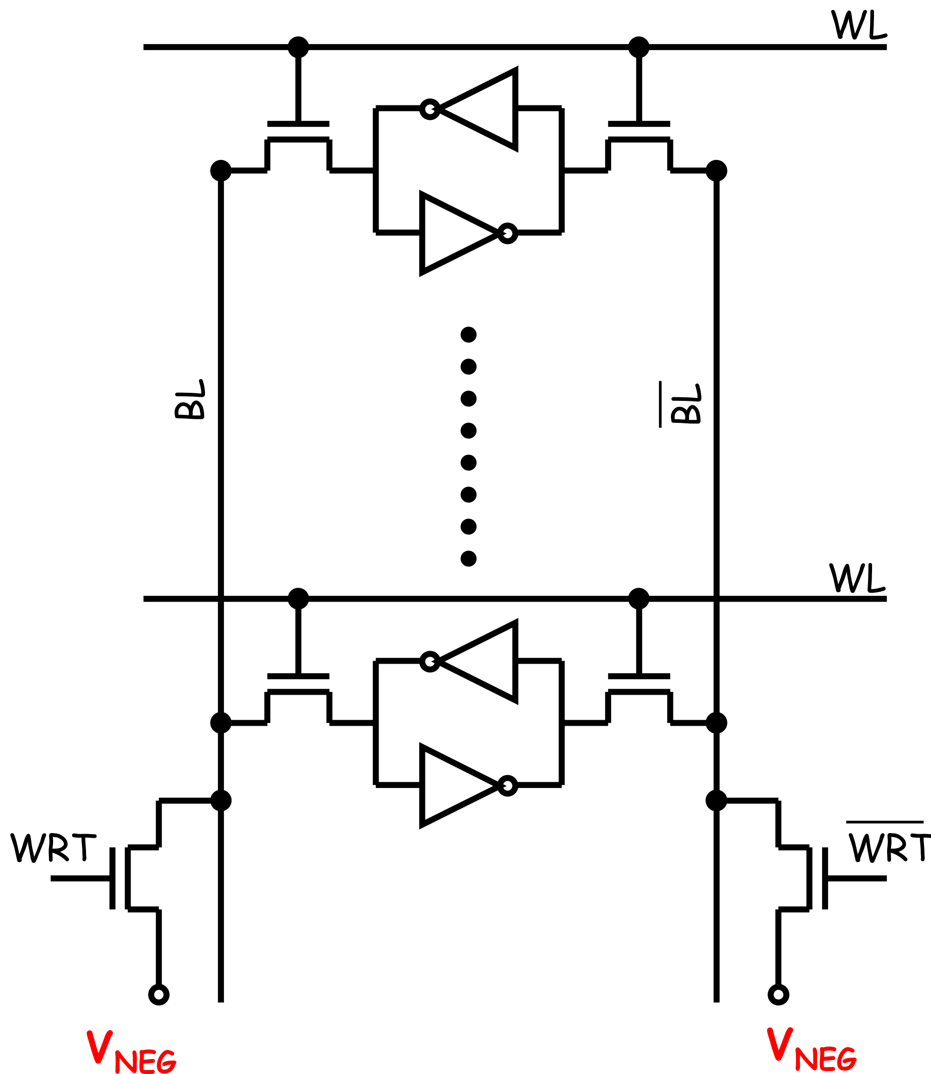
- Driving the wordline to a voltage higher than the array VDD, will destabilize the accessed bit cell

- The gate drive of the Pass Gate is increased relative to the Pull-Up device, and VTRIP is improved

- Since the WL services all columns, all bit cells along the WL become unstable

- Non-interleaved columns or a read and write-back scheme is required

Write Assist: Negative Bitline Voltage



- During a write, connect the source of the driver to a negative voltage (V_{NEG})
- The low BL will get pulled below VSS
- This will increase the gate drive of the PG relative to the PU device, and improve write margin

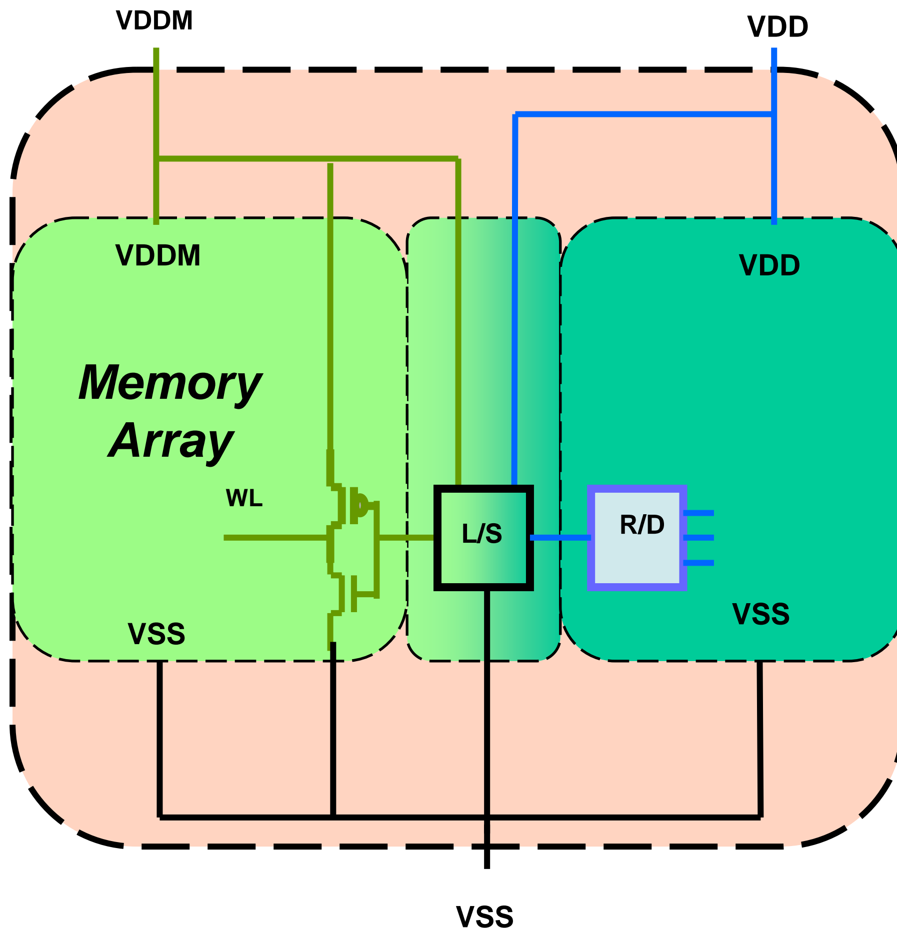
Review: Write Assist Techniques

- Dynamic control of the bit cell supplies can compensate for mis-match between the Pass Gate and Pull-Up transistors during a write operation to improve WRITE margin:

- Reduce gate drive of Pull-Up relative to Pass Gate:
  - Lower bit cell VDD
  - Raised bit cell VSS

- Increase gate drive of the Pass Gate drive relative to Pull-Up device
  - Boosted Wordline Voltage
  - Negative Bitline Voltage

Dual Rail Architecture [19]



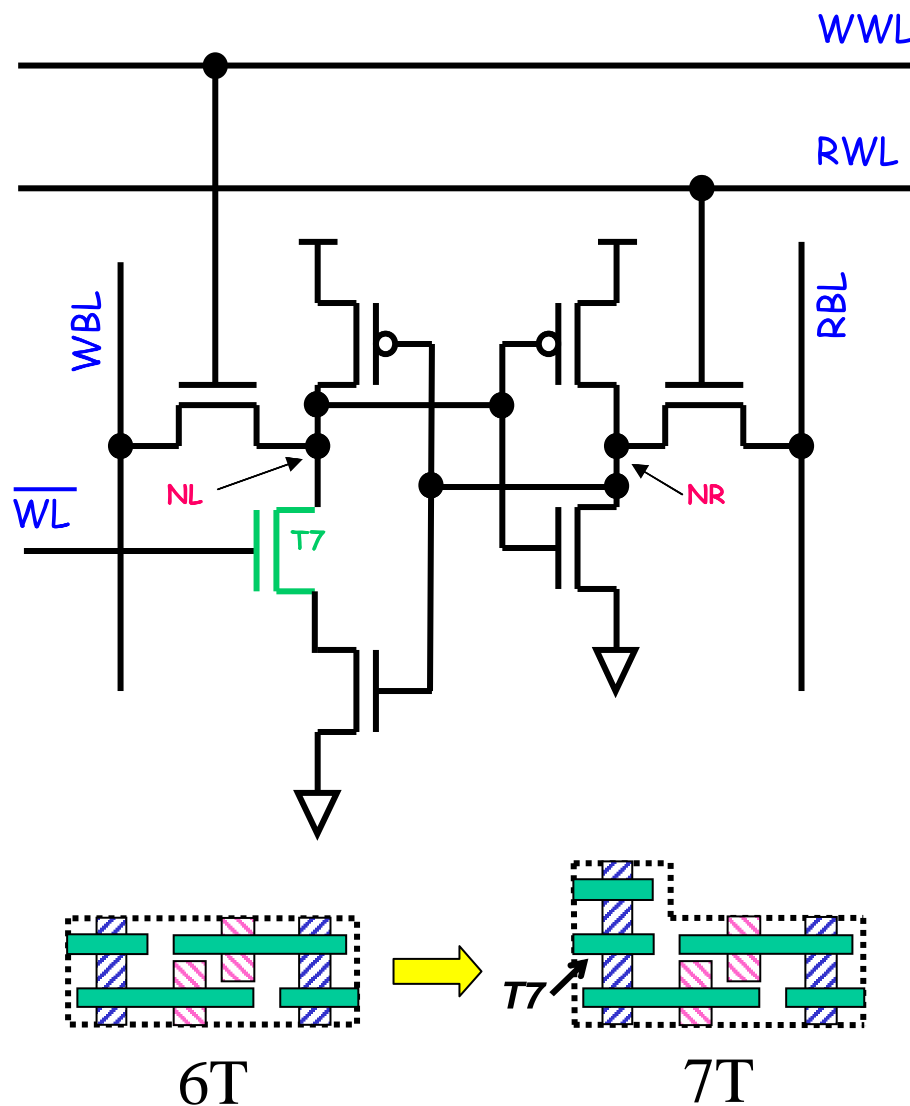
- An alternative to using dynamic power rail techniques is the dual rail architecture
- Decouples logic VDD from SRAM bit cell constraints
- Chip level power routing is compromised and a second power supply is introduced

- Operate SRAM array at 1.2v for SNM, VTRIP and I_{READ}
- Logic can operate with 0.7v to 1.2v VDD for low power

Alternative Bit Cells

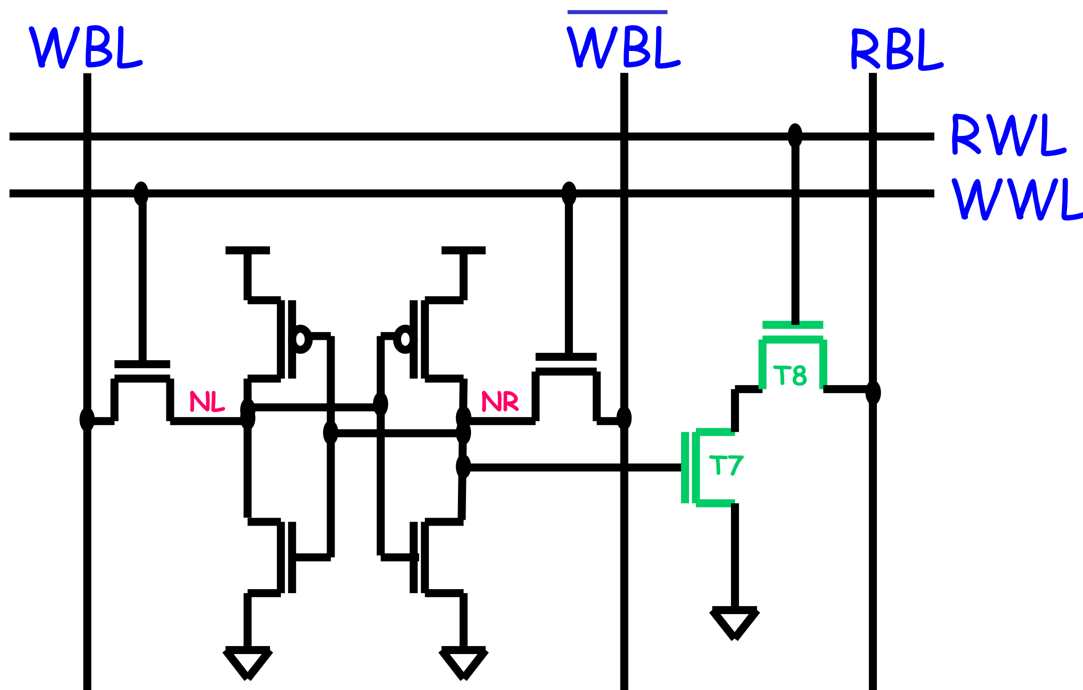
- At 45nm and 32nm; R/W Assist techniques or dual rail may not be sufficient to allow operation at low VDD
- Bigger bit cells can have less variability, greater I_{READ} and better operating margins at low VDD levels
- If we consider bigger bit cells, there are alternatives to the standard 6T SRAM bit cell which can improve VDDmin operation

Alternative SRAM Bit Cells: 7T [20]



- SNM-free bit cell
- Single-ended read
- Single-ended write
- Non-Interleaved columns
- Floating node issues
- “L” shaped layout, allows precharge and sense amp devices to be placed throughout the memory array

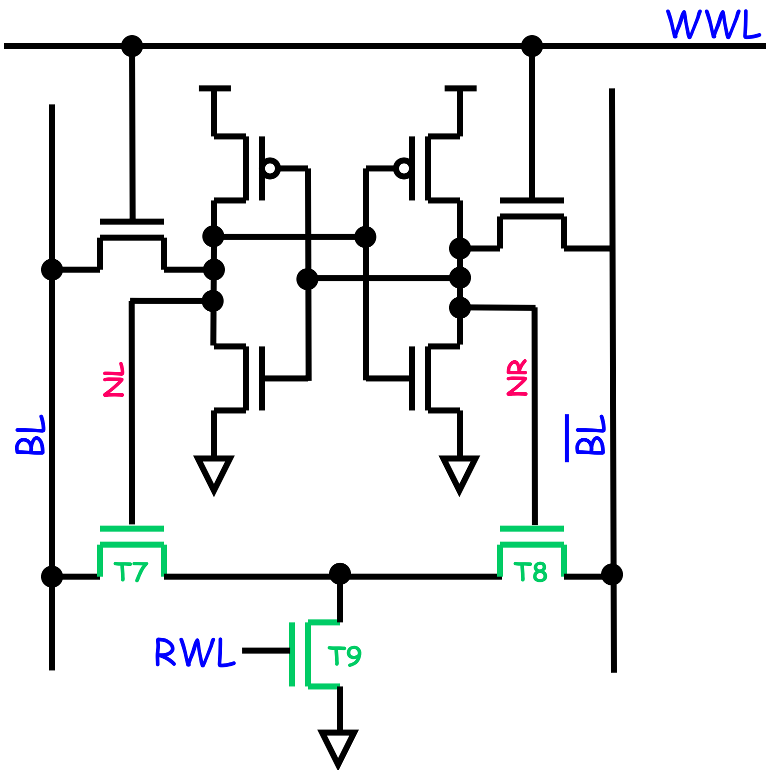
Alternative SRAM Bit Cells: 8T [21,43,44,45]



- SNM-free bit cell
- Single-ended read
- I_{READ} is determined by read buffer
- Device sizes may be optimized to reduce leakage and V_{MIN}

- The latch can be designed with very good write margin (i.e. poor stability when WWL is high)

Alternative SRAM Bit Cells: 9T [22]



- SNM-free bit cell
- Differential Sensing
- I_{READ} is determined by T7/T8 and T9
- Device sizes may be optimized to reduce leakage and V_{MIN}

- The latch can be designed with very good write margin (i.e. poor stability when WWL is high)

Review: Alternative Bit Cells

- Read margin and Write margin force conflicting requirements on the SRAM bit cell designer
- The alternative bit cell's discussed remove this conflicting requirement:
  - Separate the read and write ports
  - Margins associated with each of these operations can be improved without concern for the other
- Main problem with Alternative Bit Cells: AREA!!!
  - More bit cell transistors
  - Additional periphery circuits (e.g. WL drivers)
  - Additional metal wires
  - non-interleaved columns

V_{HOLD} Failures [29]

- SRAM leakage reduction techniques often apply the lowest possible voltage when the bit is not accessed
- If the bit cell cannot retain the proper data at the reduced voltage, this is referred to as a V_{HOLD} failure
- V_{HOLD} failures occur when the voltage on the high node is lower than the trip point of the latch
- In addition to lower VDD what can cause the high node to become lower than the trip point of the latch:
  - Variability can increase driver transistor leakage
  - Variability can reduce load transistor drive current
  - Variability can shift the trip point of the latch

- What’s the problem?
- Bit Cell related design techniques
- Non-Bit Cell related design techniques
  - Sense Amps and Data Sensing
  - Digital Techniques
- Conclusion

Sense Amps and Data Sensing

- Variability has always been an issue for S/A design
  - Layout styles which reduce device mis-match
  - Common mode noise rejection
  - BL coupling noise reduction (twisting, shielding…)
  - Design using statistical simulations & analysis

- At 45nm and 32nm, as device dimensions shrink, device mis-match poses much greater problems for the SRAM data path designer

- Increased variability also leads to the occurrence of very low I_{READ} bit cell's
  - Power, performance and area may be compromised in order to sense these weak bits

Small Signal Sensing [32, 34]

Column Select Devices

Sense Devices

Set Device

- How quickly node V_S is pulled down to set latch can affect the influence of mis-match between set devices[34]
- Ideally, V_S is brought down slowly and after the latch starts setting in the right way, V_S can be pulled to VSS

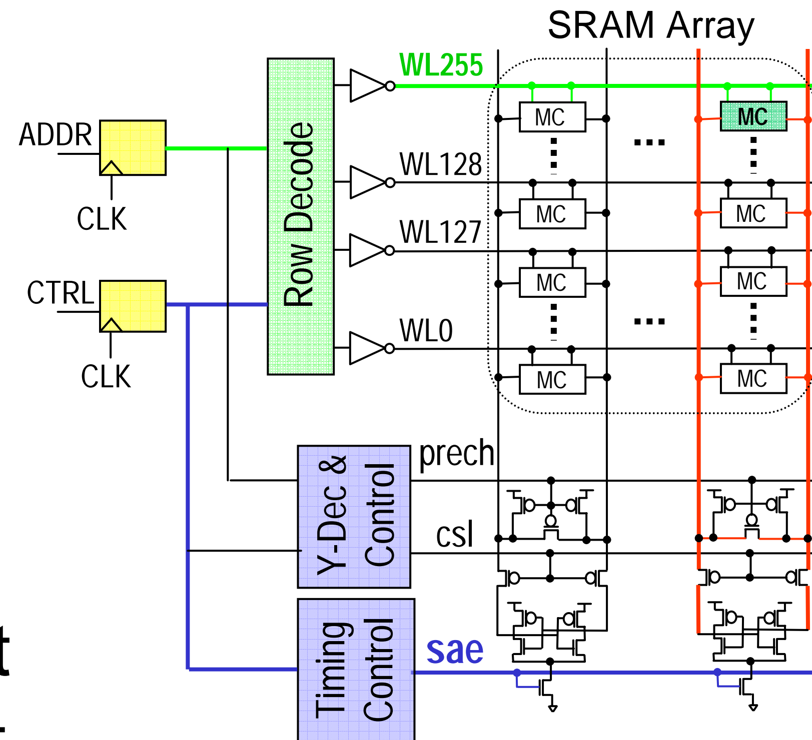
- Increasing device dimensions appropriately can reduce the probability of failure due to device mis-match by 99%[32], but………at a cost:
  - Power, Performance and Area

Sense Amp Enable Timing Variation

• Divergent timing paths for signal development and sense amp enable

• Transistor variability will affect these two paths differently

• The SAE timing circuit must allow for a slow bit and a fast timing path



• Various techniques used for SAE timing control; dummy MC's[35], BL and WL RC tracking circuits……..

Offset Cancellation Techniques

• Auto-zero techniques have been described to cancel the input offset voltage of various S/A applications:

– DRAM's
– NVRAM's
– SRAM 's

• The general idea: measure the input offset of the S/A and adjust the input levels (voltage sense) or current levels (current sense) to zero-out the mismatch

• When applied to SRAM's these techniques have usually added too much complexity, area or delay

• Work continues in the OC area, but another option is to completely eliminate small signal sensing……

Large Signal Sensing

- Issues related to sense amp device matching can be eliminated with large signal (typically single-ended) sensing schemes
- Just as the name implies, large signal sensing relies on the bit cell to develop a full logic level on the bitline
  - Bitlines will be shorter than allowed with small signal sensing (for performance reasons)
  - The low I_{READ} bit will still limit performance
- The full logic level is then “sensed” by a transistor, inverter or other type of logic gate (S/A enable timing no longer limits performance)

Large Signal Sensing [37, 38, 44, 45]

- Small signal sensing is not scaling well:
  - Performance: I_{READ} and SAE timing variability is preventing entitlement performance improvements
  - Area: in order to minimize input offset, s/a area is not scaling like logic
- Large signal sensing can offer performance and area scaling similar to logic

bPRE1
bGPRE
WL31t
MC
LBLt
WL00t
MC
MC
WL00b
LBLb
MC
WL31b
GBL
bPRE0

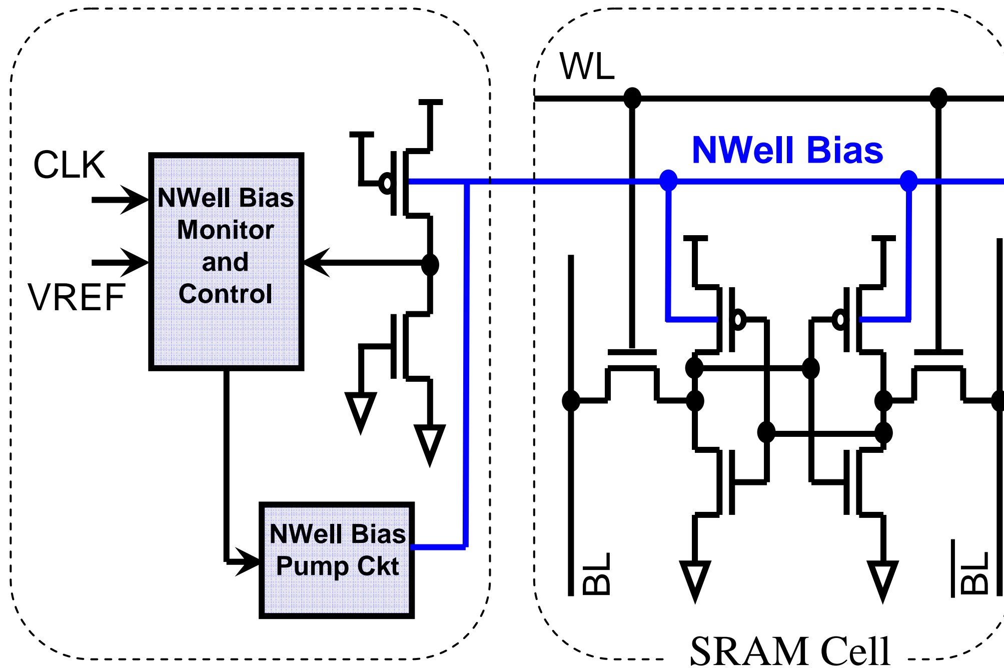
Review: Sense Amplifiers

- Increased variability leads to larger input offset voltage for the SRAM sense amplifier
- As a result Sense Amp area and performance is not scaling with technology
- Several design techniques have been described which address the increased input offset:
  - Selective upsizing of devices
  - Adding additional transistors
  - More effective timing control of SA enable
  - Auto-Zeroing of input offset voltage
- Eliminate sense amps and use large signal sensing
  - Best suited to high performance designs

Digital Techniques Overview

- The random variability being seen at 45nm and 32nm cannot be addressed simply by process modification or lithography compensation
- The circuit design techniques described earlier are effective ways to allow the SRAM bit cell to continue to operate with increased local variation
- Another design approach is to measure and compensate for variation with digital techniques
- Digital techniques use on-chip monitors or test structures which can evaluate the amount of device mis-match in a circuit and then feed this information back to the appropriate compensating circuit

Digital Techniques [27]



- Write margin degrades with a strong PU device and weak PG device
- This circuit monitors the relative strength of the bit cell PMOS and NMOS

- An NWell pumping circuit which controls the bit cell NWell bias is raised or lowered
- The V_{th} of the PMOS can be increased by raising the NWell bias voltage or decreased by lowering the bias

Review: Digital Techniques

- Digital techniques generally employ a monitor and feedback system
- These techniques are effective in reducing die-die or global variation
- Digital techniques can also be used to limit the skew between NMOS and PMOS transistors
- Digital techniques are also being used to get a better balance between power and performance
- A more centered, less skewed design will be less sensitive to local variation and device mis-match

Conclusion

- Transistor variability presents many problems for SRAM designers in nanometer-scale technologies

- During the course of this talk I have shown several of the innovative techniques being used by SRAM designers to meet this challenge

- Different applications will require different solutions:
  - Various circuit design techniques offer different trade-offs between power, performance and area
  - System/architecture options may be available

- Success in the future requires close collaboration between process/device/litho/manufacturing teams with the SRAM designer

Acknowledgements:

Ted Houston

David Scott

Hugh Mair

Wah Kit Loh

Andrew Marshall

Peter Rickert

Dennis Buss

Jeff Wu

Robert Baumann

Clive Bittlestone

Ajith Amerasekera

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