Mitigation of Self-Interference in Mixed-Signal Transceiver SoCs

Oren Eliezer

(OrenE@ieee.org)

Wireless Terminals Business Unit

Texas Instruments Inc.

Dallas, Texas

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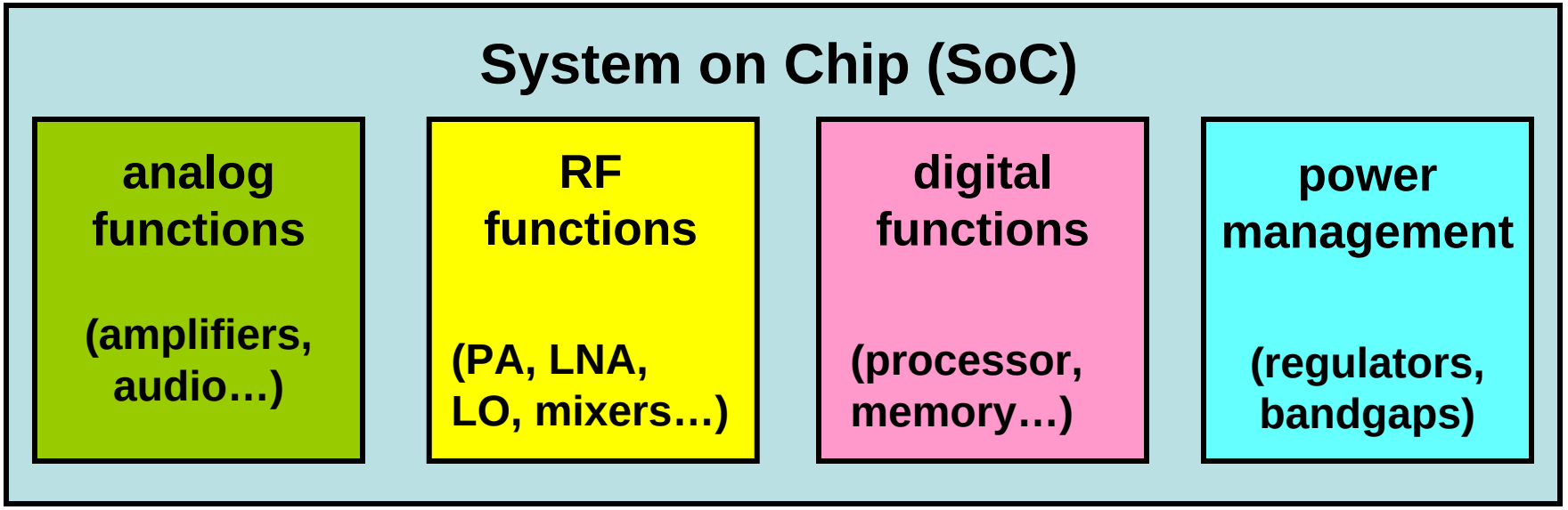
Outline

- **Introduction** (motivation, modeling challenges)
- **Definition and examples for self-interference**
- **Types of interference mitigation solutions**
- **The Design-for-Interference-Mitigation (DfIM) approach**
- **Examples for interference mitigation solutions**
- **The novel phase domain approach and its application**

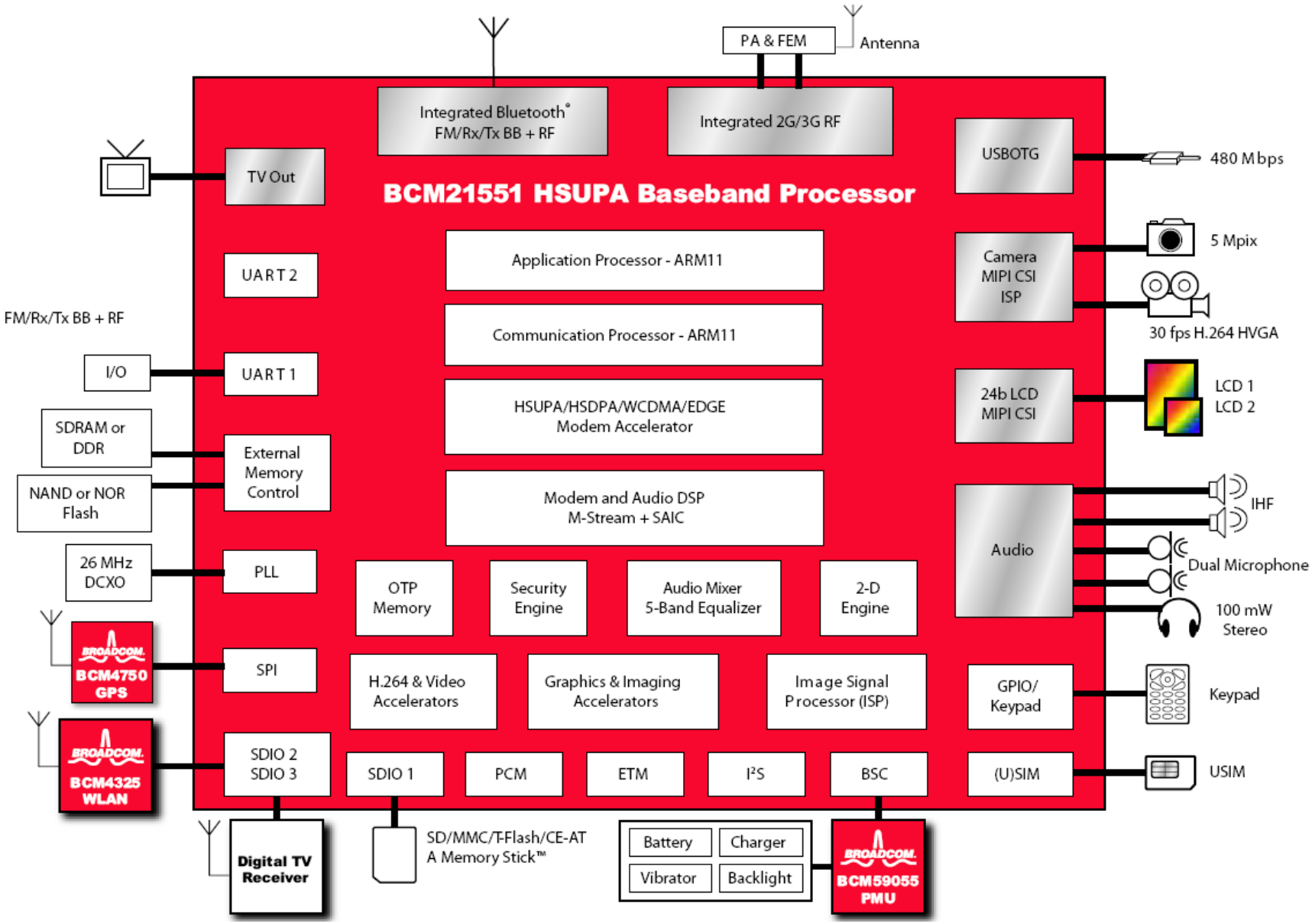
  (PhD research under the supervision of Prof. Poras Balsara, UTD, and Bogdan Staszewski, Texas Instruments)

Introduction - Motivation (1/2)

- Aggressive cost and size targets are driving ever increasing level of integration
- A typical transceiver CMOS system-on-chip (SoC) may include not only a digital processor and the RF transceiver, but even multiple radios (e.g., Bluetooth + WLAN + FM).
- The potential for self-interference in the SoC grows exponentially with the increase in complexity and integration.

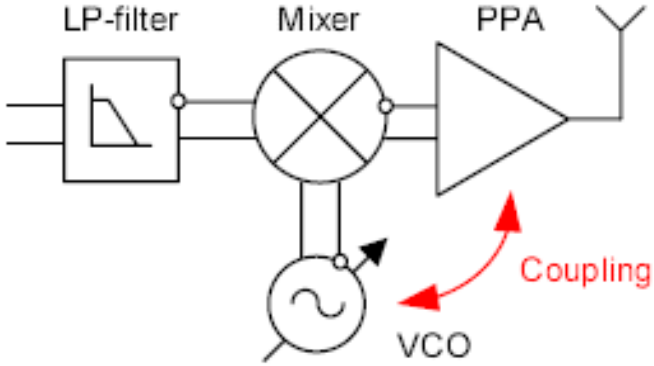


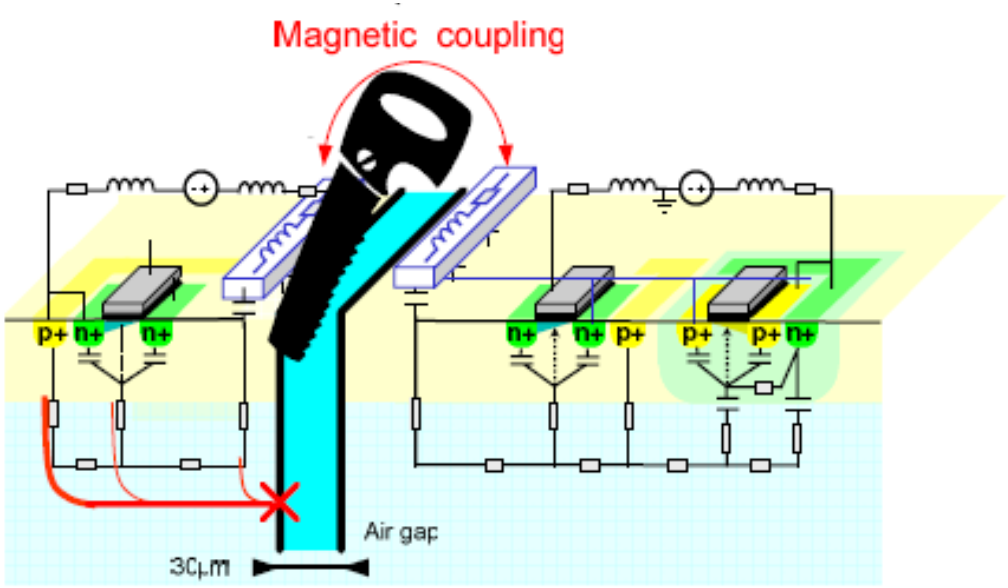
SoC Example from Broadcom BCM21551



Introduction - Motivation (2/2)

- Interference has become a hot topic !
  - research in academia
  - publications (substrate noise, frequency-pulling in transmitters, interference-mitigation techniques…)
  - full-day workshop at RFIC 2008 and RFIC 2009, technical session





S. Bronckers
IMEC, Vrije Universiteit Brussel, Belgium

"Study of the different coupling mechanisms between a 4 GHz PPA and a 5-7 GHz LC-VCO", (RFIC 2008)

Modeling Capabilities and Limitations

- Modeling of all possible interference mechanism and parasitic coupling at the design stage is extremely challenging.
- Can circuit level simulations be run (including layout/package parasitics) at the system level, to verify that actual performance targets are met?
- Simulation accuracy and verification coverage are compromised…

	Block1	Block2	Block3	Block4
Test 1	**Behavioral**	**Behavioral**	**Behavioral**	**Behavioral**
Test 2	**Spice**	**Behavioral**	**Behavioral**	**Behavioral**
Test 3	**Spice**	**Spice**	**Behavioral**	**Behavioral**
Test 4	**Behavioral**	**Behavioral**	**Spice**	**Behavioral**
Test N	**...**	**...**	**...**	**...**

From:

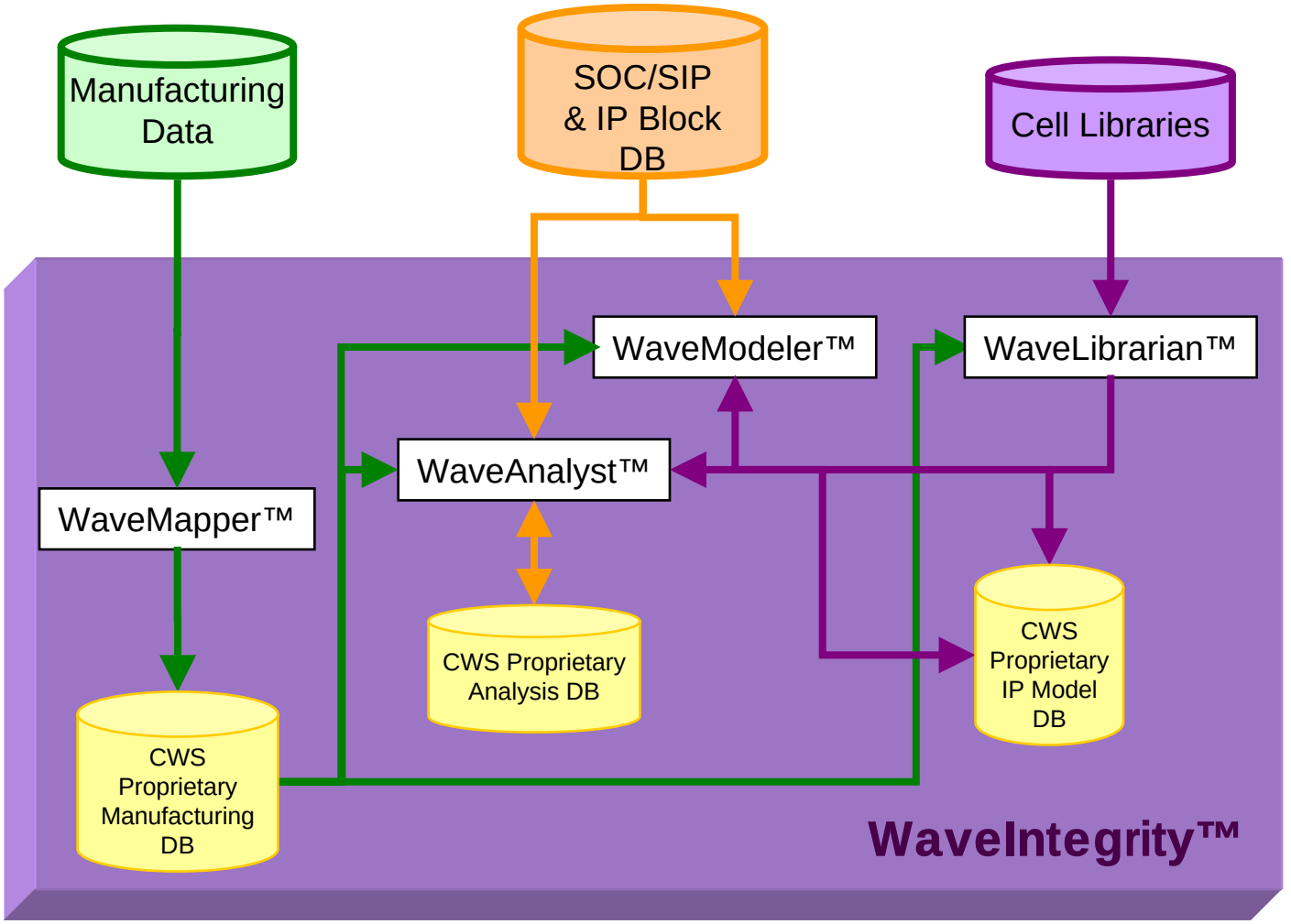
Tuna Tarim
(Tuna@ti.com)

EDA, WTBU,

Texas Instruments

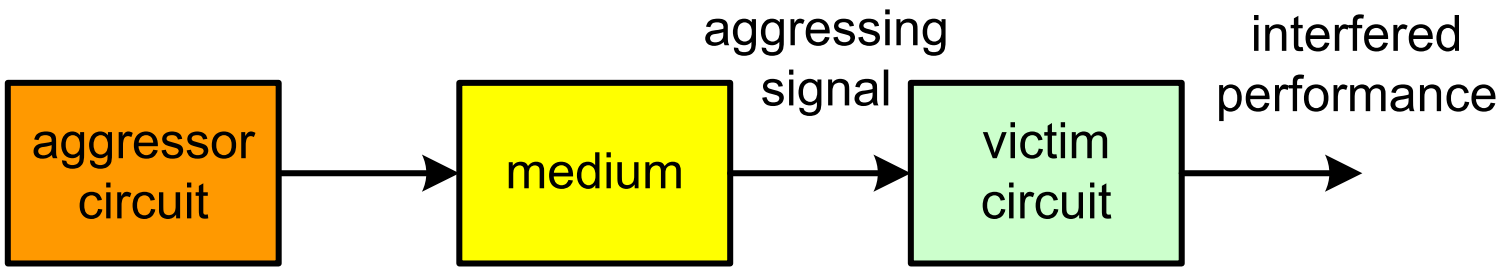
Example for EDA Vendor - CWS

- Coupling Wave Solutions **www.cwseda.com**
- WaveIntegrity™ Platform – ***"Enabling Higher Levels of Integration Complexity"***



Self-Interference in the SoC Environment

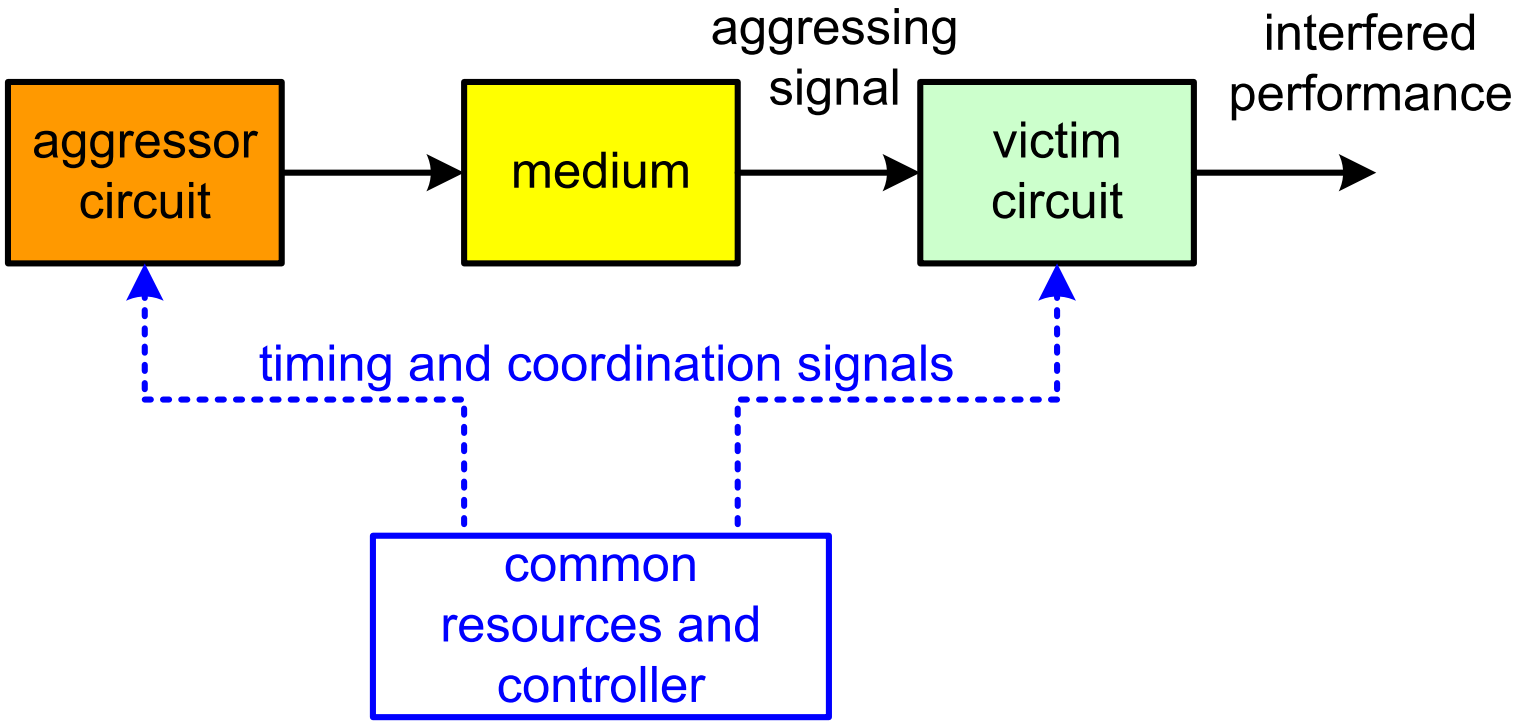
- Definition: self-interference is experienced when the performance of a particular function in the SoC is degraded due to the simultaneous operation of another.
  - may or may not result in the violation of targeted limits
  - may even result in noticeable functional failures



- An interference mechanism involves one *victim*, at least one *aggressor*, and at least one coupling/propagation *medium*.

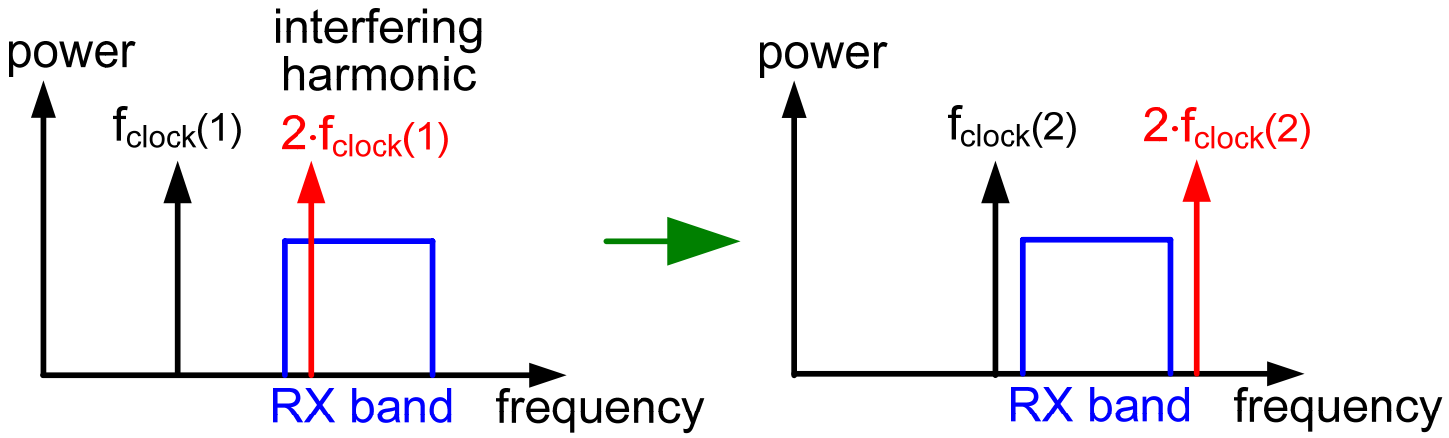
The Potential for Phase/Timing Dependency

- Clock signals used in the victim and/or aggressing functions may be derived form the same source (e.g., RF oscillator that serves as the LO).
- There would typically be a common controller/processor for all functions.
- It may be possible to digitally control the relative timing/phase of aggressing and/or victim signals in the system-on chip (SoC), thereby mitigating the impact of the interference → ***The phase domain approach !***

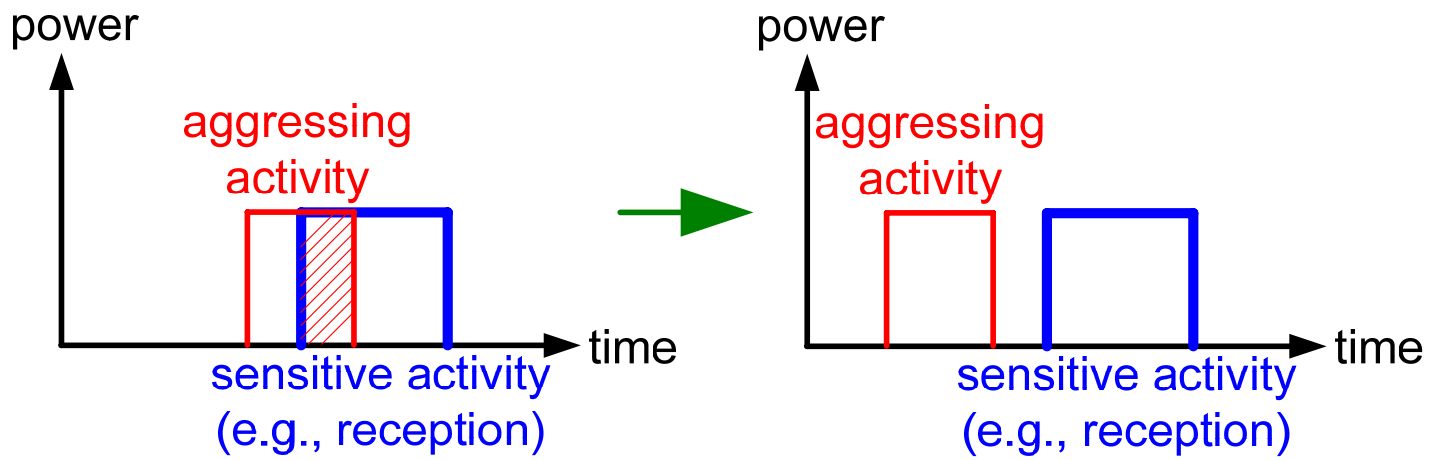


Common Interference Avoidance Techniques (in frequency and time)

- **frequency**-domain avoidance

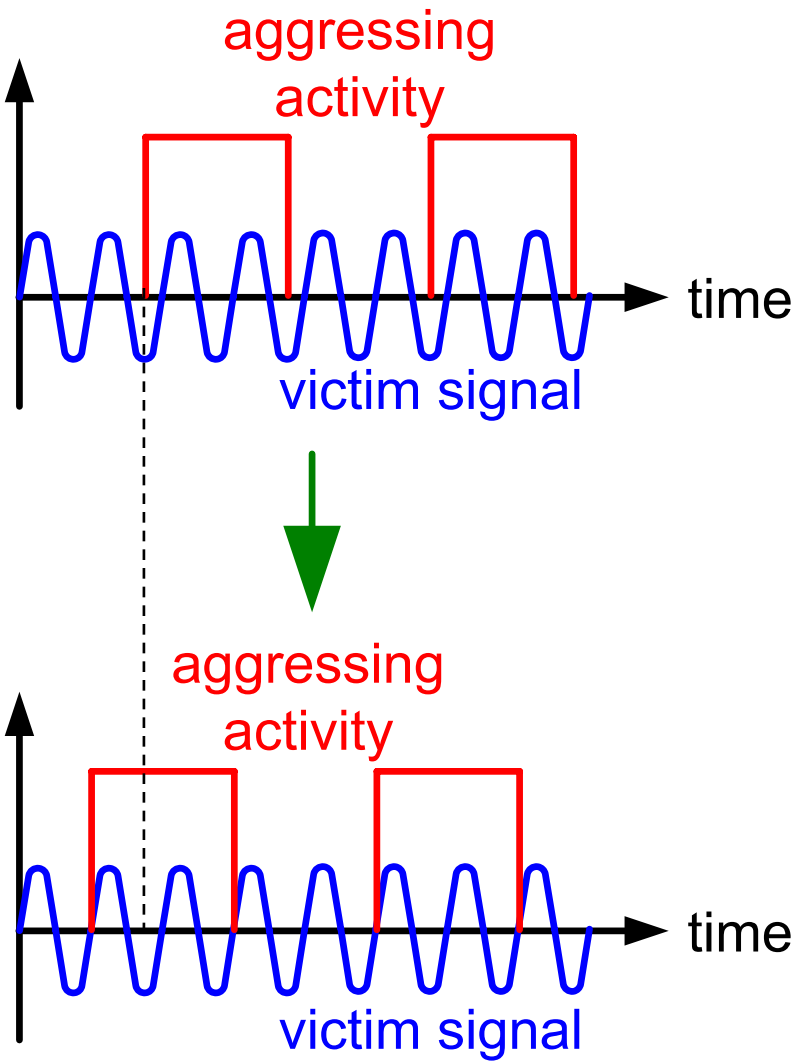


- **time**-domain avoidance



The Novel Phase Domain Approach

- Only the **phase** of an aggressing or victim signal is changed

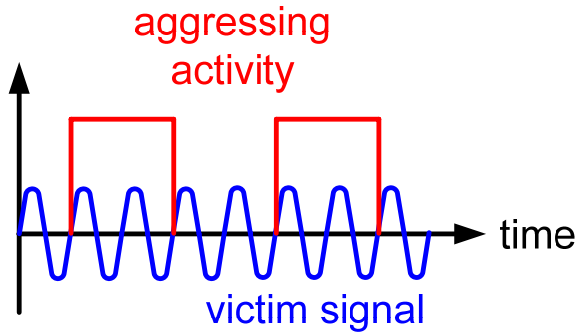


The fundamental frequency of the aggressor in this example is not the same as that of the victim, but we assume that interference is suffered.

Why would this timing/phase relationship between the aggressor and victim be any better?...

Phase-Dependent Interference Scenarios

- The signals involved must be frequency-synchronous, i.e., their fundamental frequencies are:
  - the same frequency, or
  - harmonically related.



- In some cases, one may be frequency-modulated, such that, instantaneously, it may not maintain frequency-synchronicity

- Scenarios where phase-adjustment may be applicable:
  - on-frequency aggressors (destructive/constructive summing)
  - on-frequency AM aggressor (e.g., LO-pulling in polar architecture)
  - frequency synchronous mixing (e.g., leakage of amplitude-modulated harmonic of LO-derived clock into front-end of receiver)
  - synchronous sampling (e.g., sub harmonic sampling of RF by clock slicer, as in the integer-N channel problem)

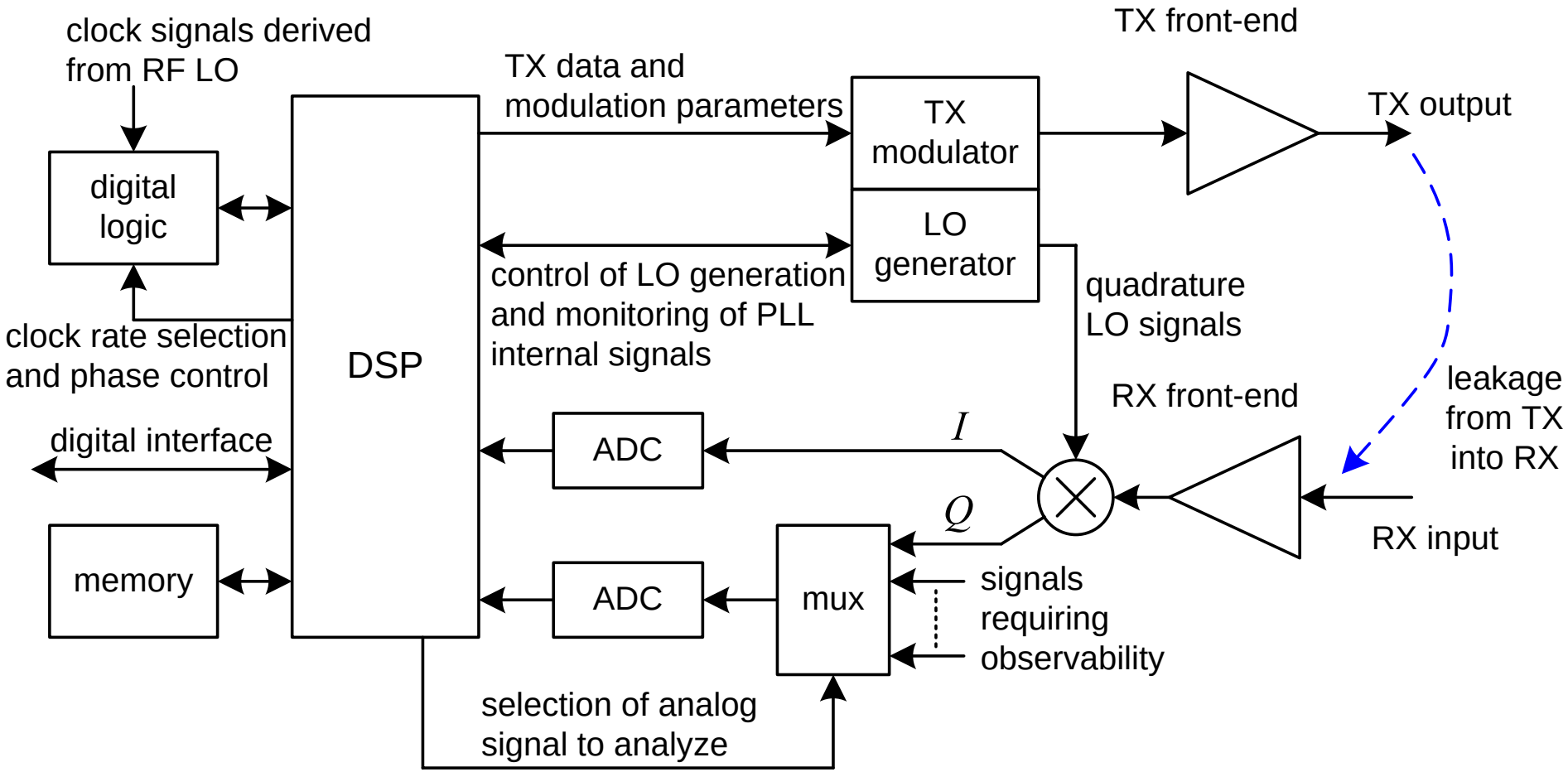
Conditions for Applicability of a Phase-Adjustment Solution

- Frequency-synchronicity
  - the signals must share the same fundamental frequency (one may be phase-modulated while the other isn't), **or**
  - they must be harmonically related
- Limitations on frequency/phase modulation
  - the signals must have the same phase modulation, or
  - if only one is phase-modulated, its modulation is limited to specific constellations that maintain some phase relationship with the carrier
- Phase adjustability
  - it should be possible to control the phase of at least one of the signals
- Phase dependency of interference impact
  - the impact of interference should depend on the phase in a repeatable manner, such that it can be brought from an intolerable to a tolerable level in a predictable way.

General Guidelines for Design-for-Interference-Mitigation (DfIM) to Allow for Phase-Adjustment Solutions

- Make provisions for observability into signals that may need to be digitally analyzed
  - for digital signals this is straightforward (e.g., PHE in ADPLL)
  - analog signal of interest either have a digital proxy or should have a controllable path into one of the ADCs that exists on the SoC
  - same principle as for DfT (Design-for-Testing) and DfD (Debugging)
- Support controllability 'hooks' for clock signals (clock rates, clock phase selection, etc.)
- Support timing/phase adjustments (add hardware if necessary, such as with the flyback delay adjustment)
- Allow for margins in processing power and memory

Design-for-Interference Mitigation (DfIM) in a Transceiver SoC



2 Examples for Dynamic Frequency Avoidance Techniques

1. **Shifting of center-frequency of clock signal using adaptive (digital) pulse swallowing**
2. **Spectral-spreading of harmonic energy via digital phase-modulation**

Related publication:

Yongsam Moon, Deog-Kyoon Jeong and Gyudong Kim,
"Clock dithering for electromagnetic compliance using spread spectrum phase modulation" *IEEE International Solid-State Circuits Conference, Digest of Technical Papers ISSCC 1999,* pp. 186-187

Example 1

Varying the Clock Frequency (Pulse Swallowing)

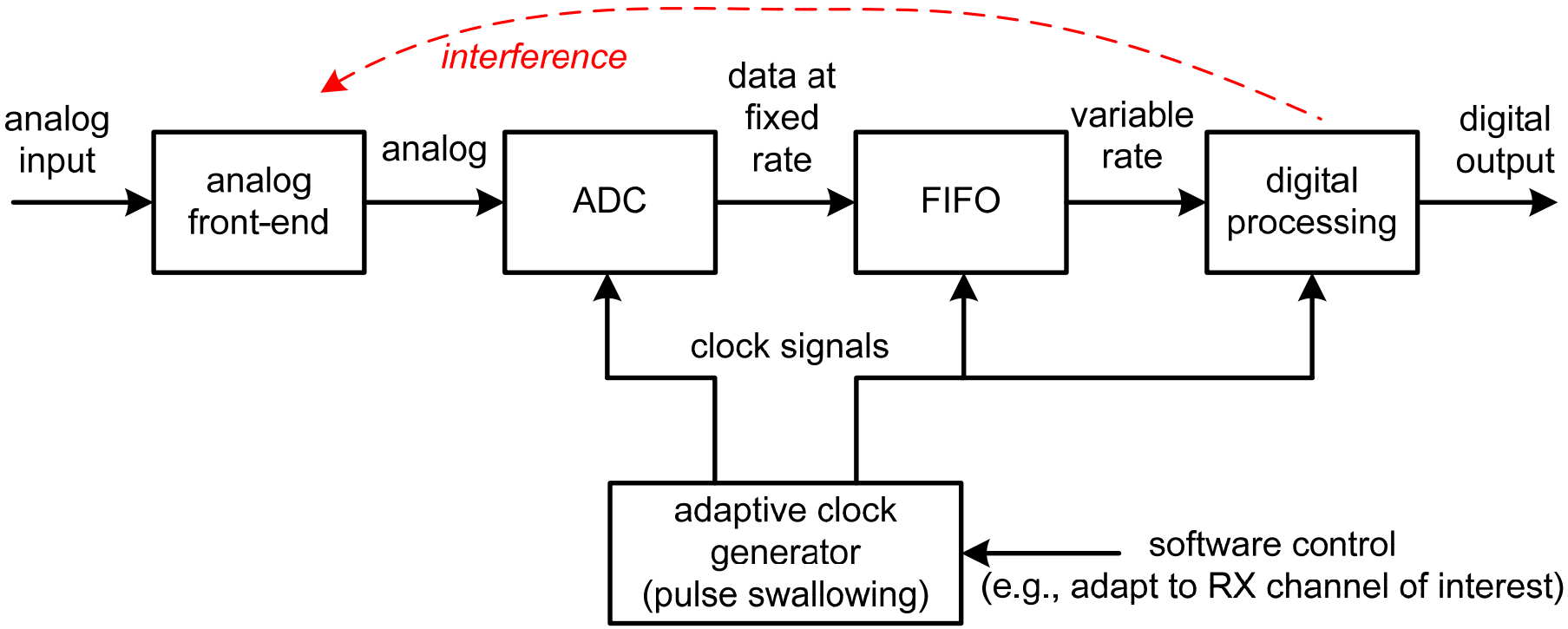
from Nir Tal

WTBU, TI Israel

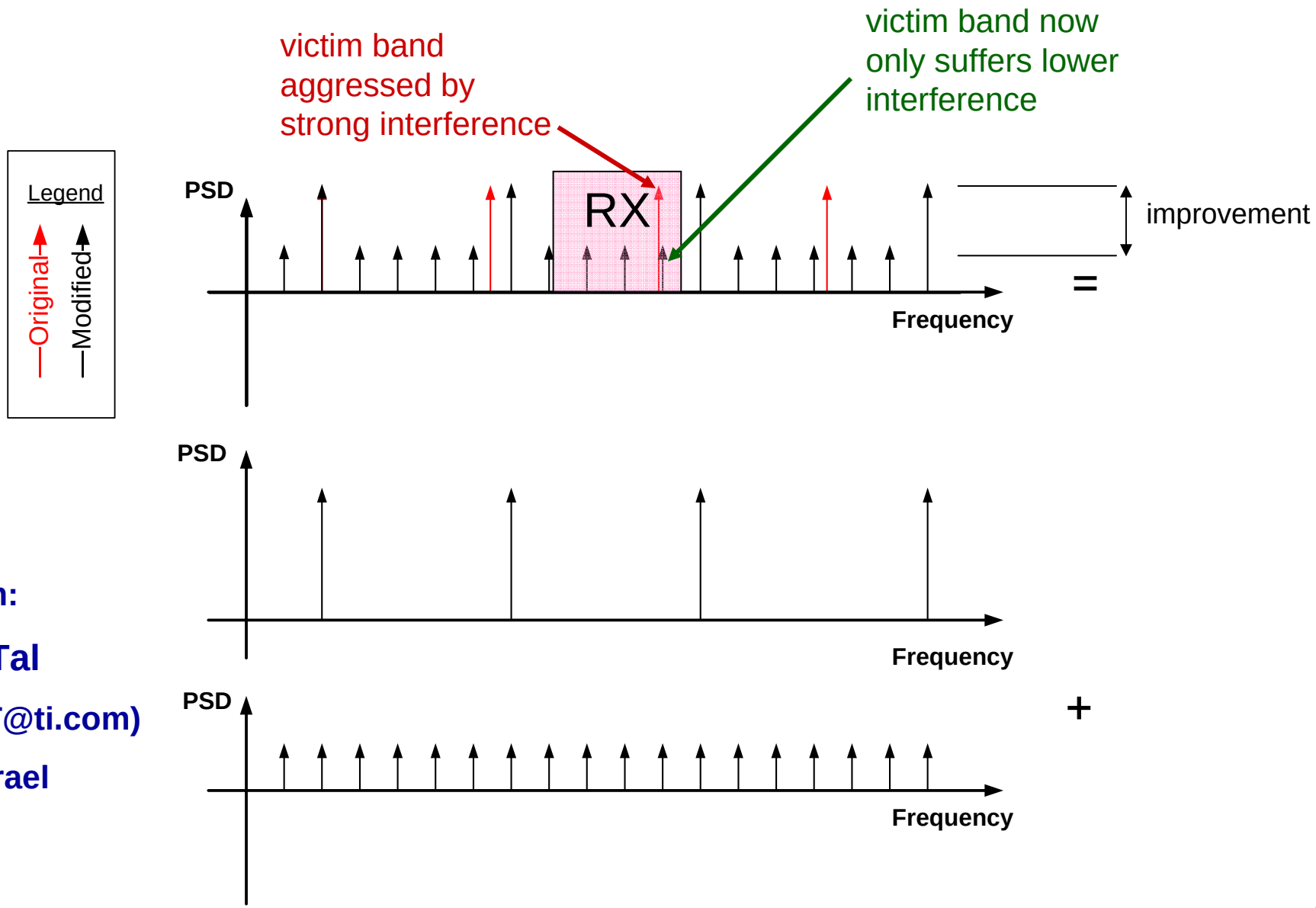
(NirT@ti.com)

Variable Clock (Adaptive Pulse Swallowing)

- Assumptions:
  - digital block creating the aggressing signal can afford to operate at a variable rate having a defined average frequency
  - digital hardware exists to allow dynamic pulse swallowing to control the spectral shaping of the variable-clock
- FIFOs can be used to 'smoothen' transitions between clock domains (e.g., ADC with fixed sampling rate and a digital-processing block)



Frequency Domain Improvement



From:

Nir Tal

(NirT@ti.com)

TI Israel

Example 2

Spectral Spreading of Clock through Randomized Digital Phase Modulation

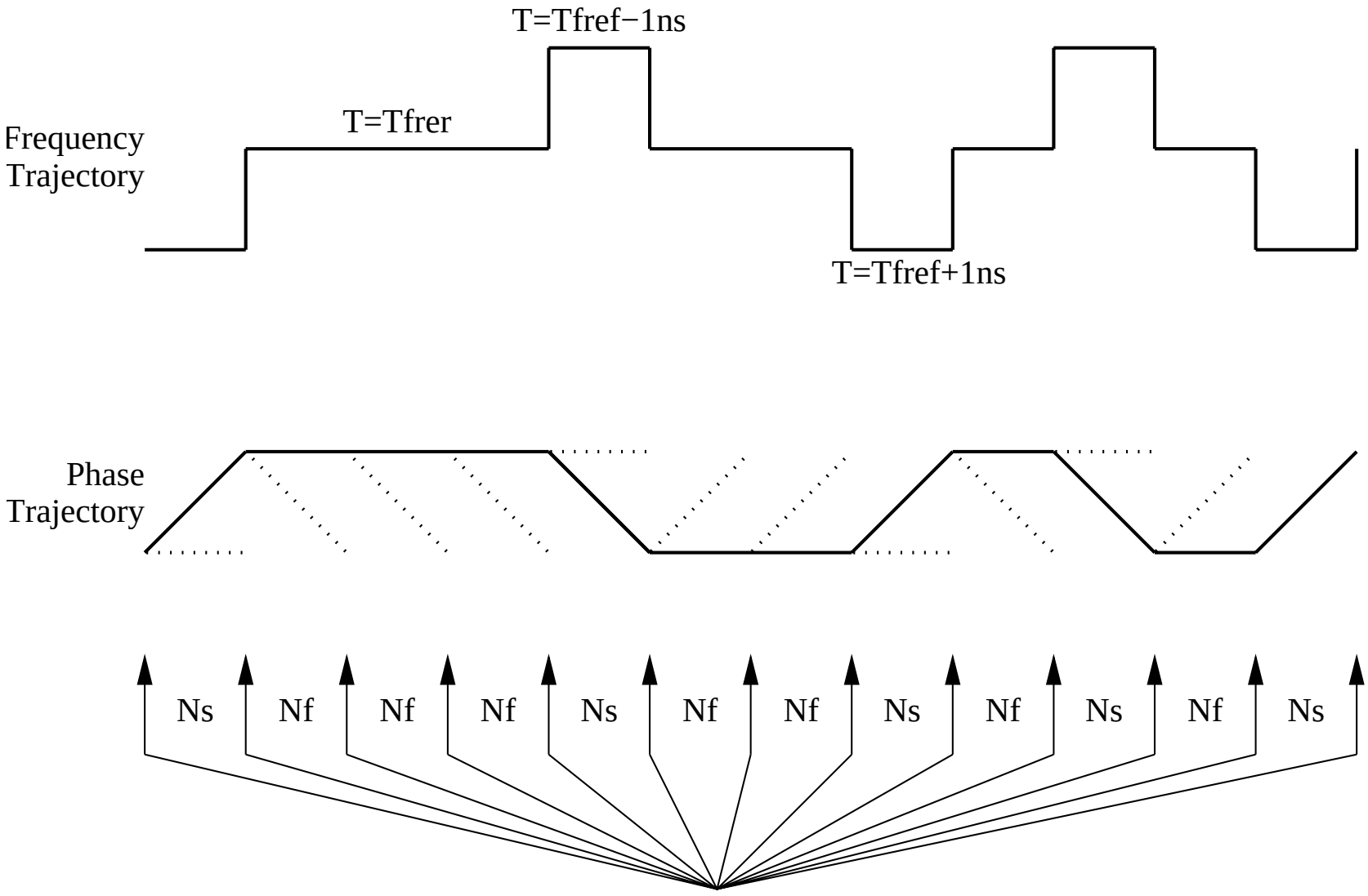
from Gennady Feygin,
WTBU, Texas Instrument,
Dallas, TX

(gfeygin@ti.com)

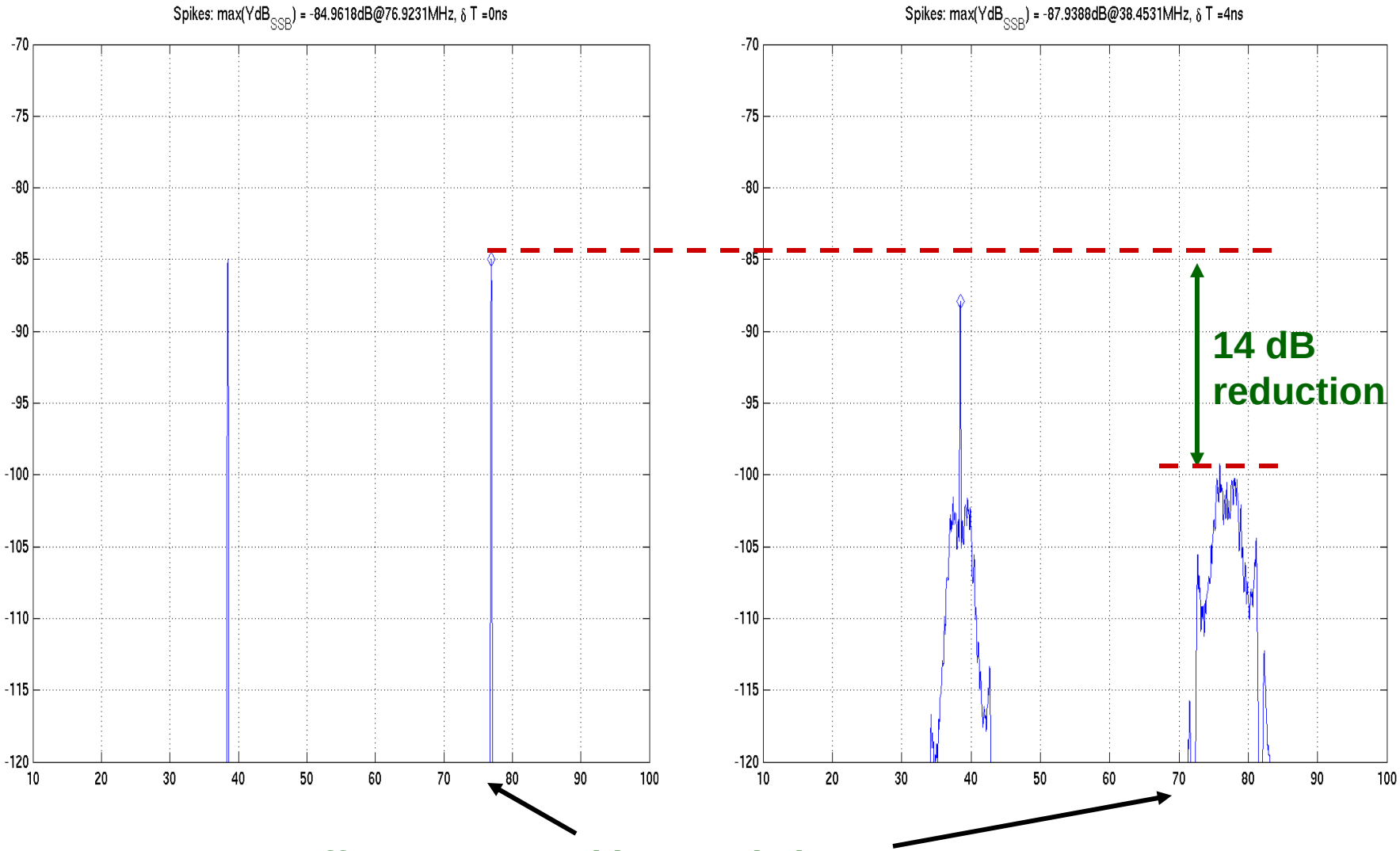
PM Based Clock Spectrum Spreading

- Typically, a large portion of the digital logic operated a common clock, resulting in strong current surges with high harmonic content.
- Clock spreading techniques can be employed to reduce the peak magnitude of specific spurs in the frequency domain, at the cost of creating spectral content elsewhere.
- In the context of incompliant out-of-band spurs in a transmitter, the spectral spreading would be designed to reduce the peak energy to below the allowed limits for the out-of-band emissions.
- In the context of receiver desensitization, the spreading would serve to reduce the spectral density at the channel of interest
- The mechanism is fully digital and is adapted (through tunable digital parameters) according to the frequency of operation (TX carrier or RX frequency)
- Delay elements are cascaded (e.g., inverters) to create delayed versions of the same clock signal, and these are dynamically selected via a mux to create phase-modulation.

Clock Spreading Effects on Clock Frequency and Phase

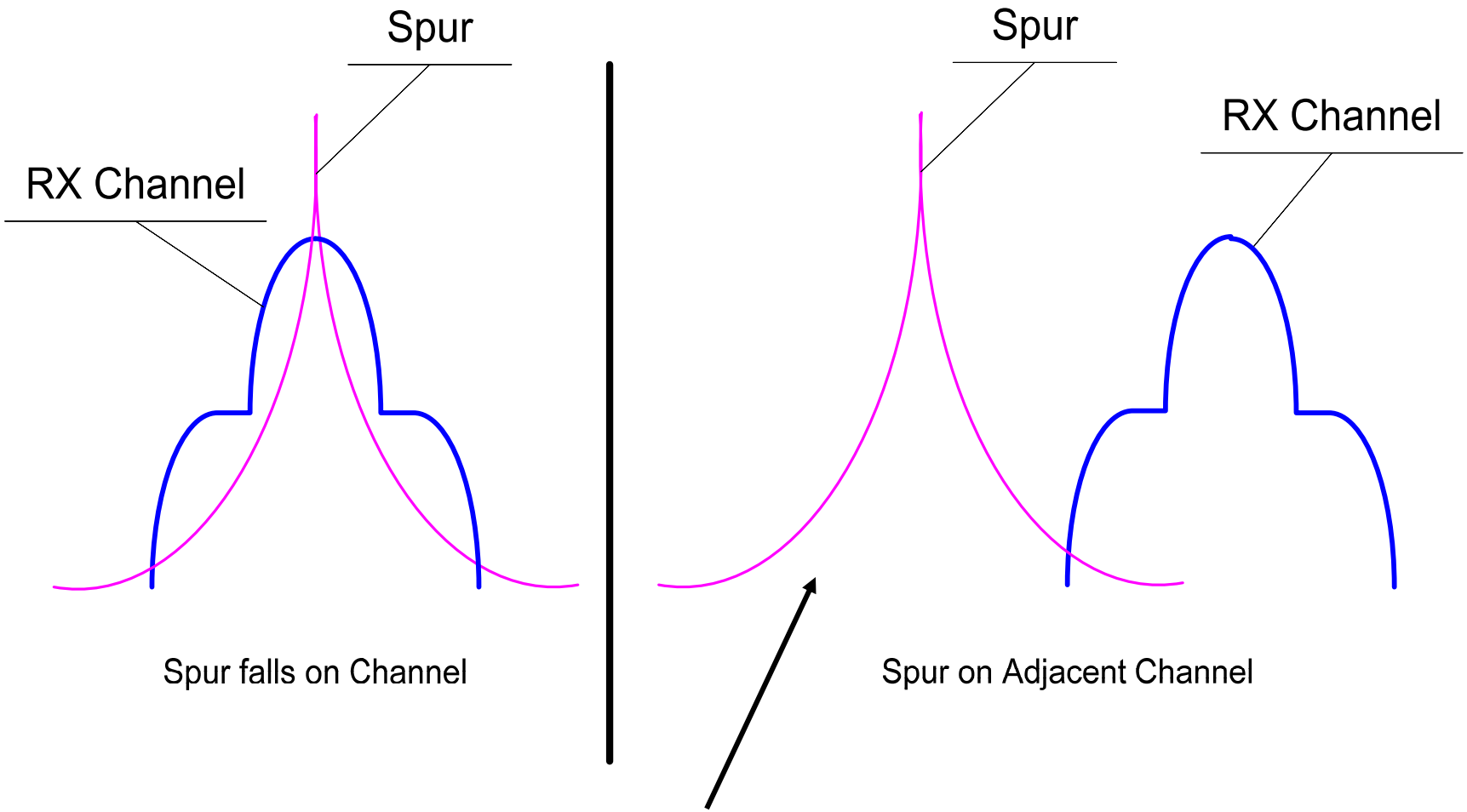


Spectrum of Clock Before and After Spreading (Matlab Simulations)



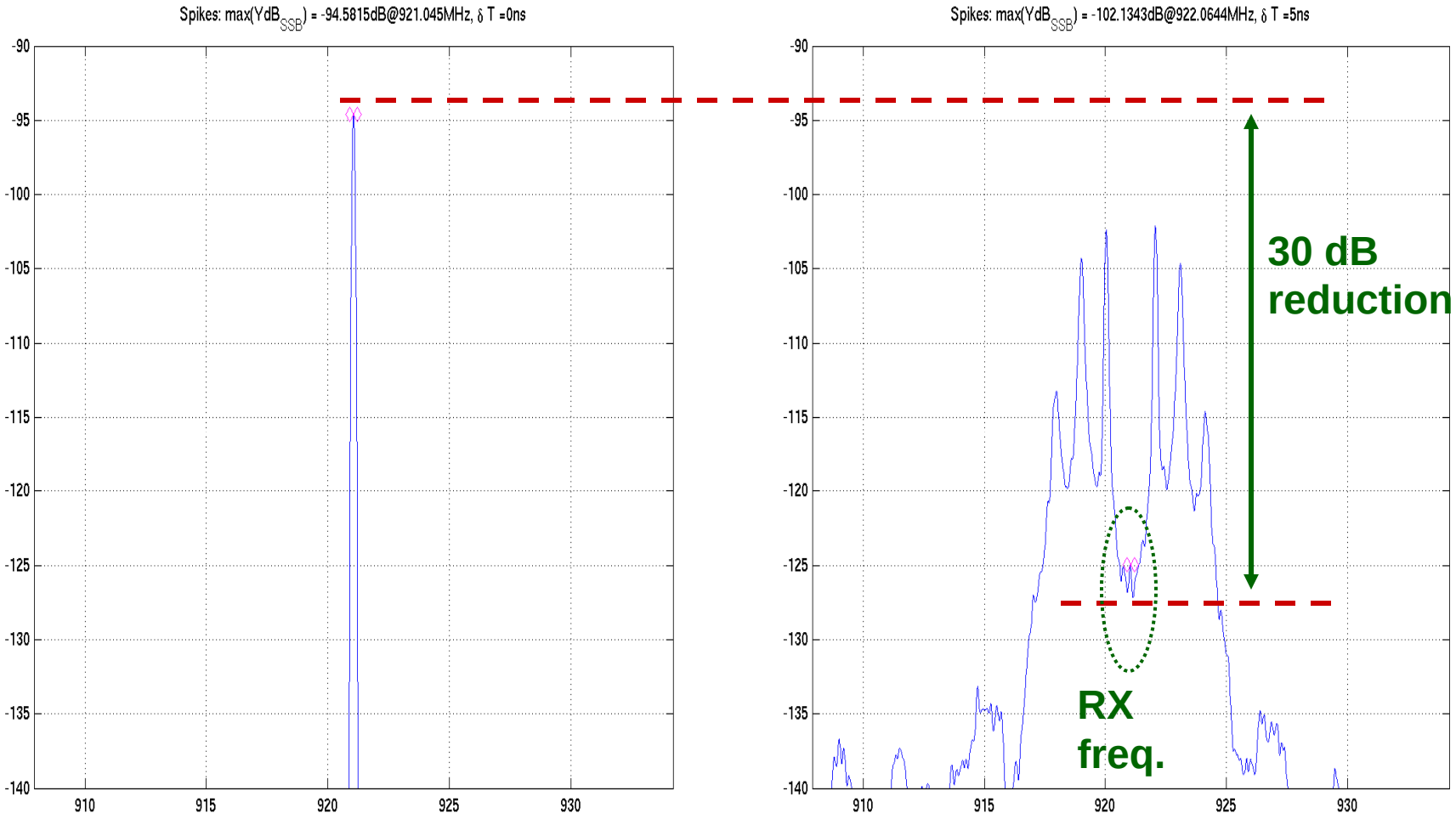
effect on second harmonic is greater

Clock Spreading to Alleviate RX Desensitization



- **The goal is to remove interfering energy from frequency of victim signal**

Spectrum of Clock Before and After Spreading (Matlab Simulations)



Although the interference is still centered at the RX frequency, its spectral density is sufficiently reduced to eliminate desensitization.

3 Examples for Mechanisms of Phase-Dependent Self-Interference in a DRP-Based GSM Transmitter

1. The ‘integer-N channel’ interference problem
2. Interference from SD frequency tuning signal (‘flyback’ setting)
3. Parasitic FM on DCO caused by the AM stage (DCO pulling)

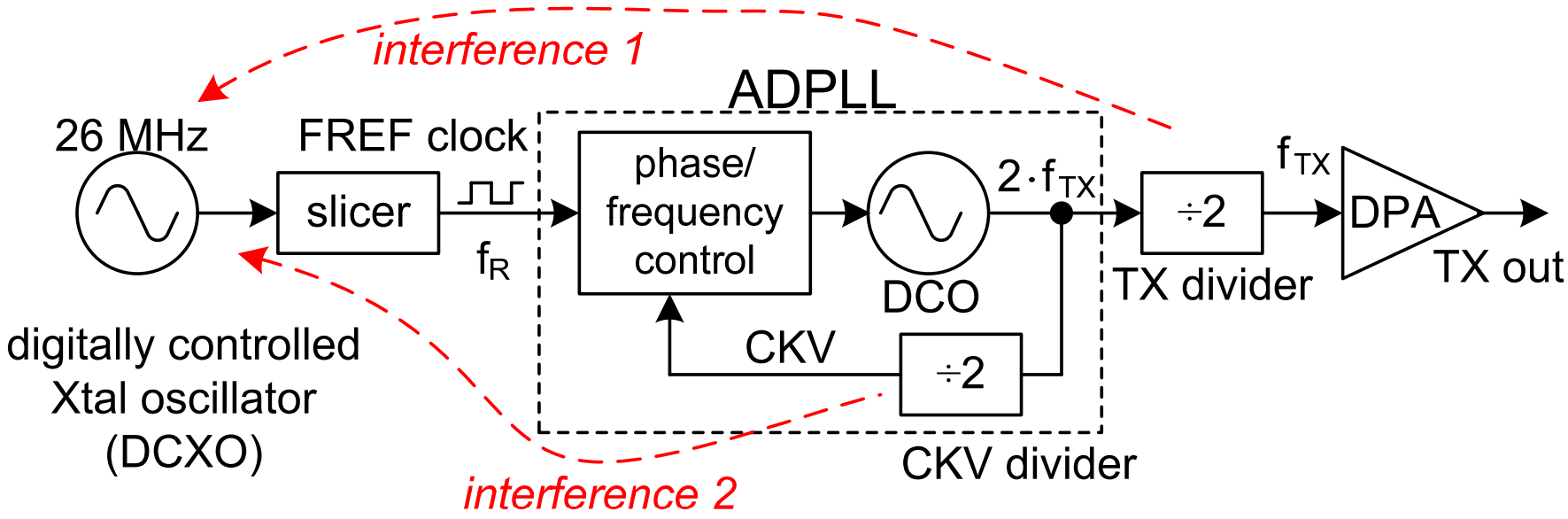
Example 1

The Integer-N Channel Self-Interference Problem (jitter on ADPLL's FREF)

Related publications:

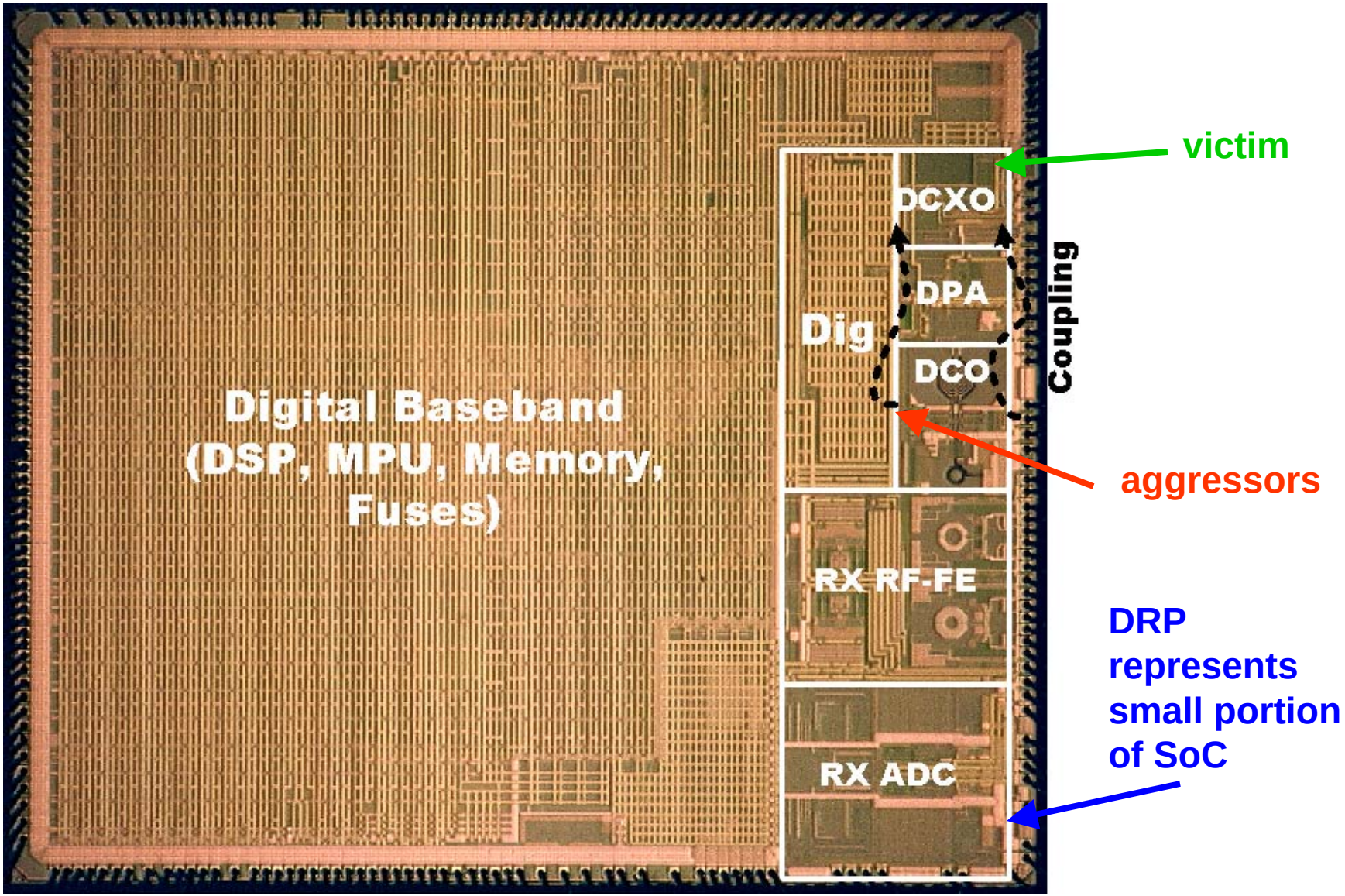
1. **O. Eliezer, B. Staszewski, S. Bhatara, and P.T. Balsara, "Active Mitigation of Induced Phase Distortion in a GSM SoC", Proc. of IEEE RFIC Symposium, pp. 17-20, June 2008.**
2. **O. Eliezer, B. Staszewski, I. Bashir, S. Bhatara, and P. T. Balsara, "A Phase Domain Approach for Mitigation of Self-Interference in Wireless Transceivers", JSSC Special Issue (accepted for publication)**

The ‘Integer-N’ Channel Interference Problem



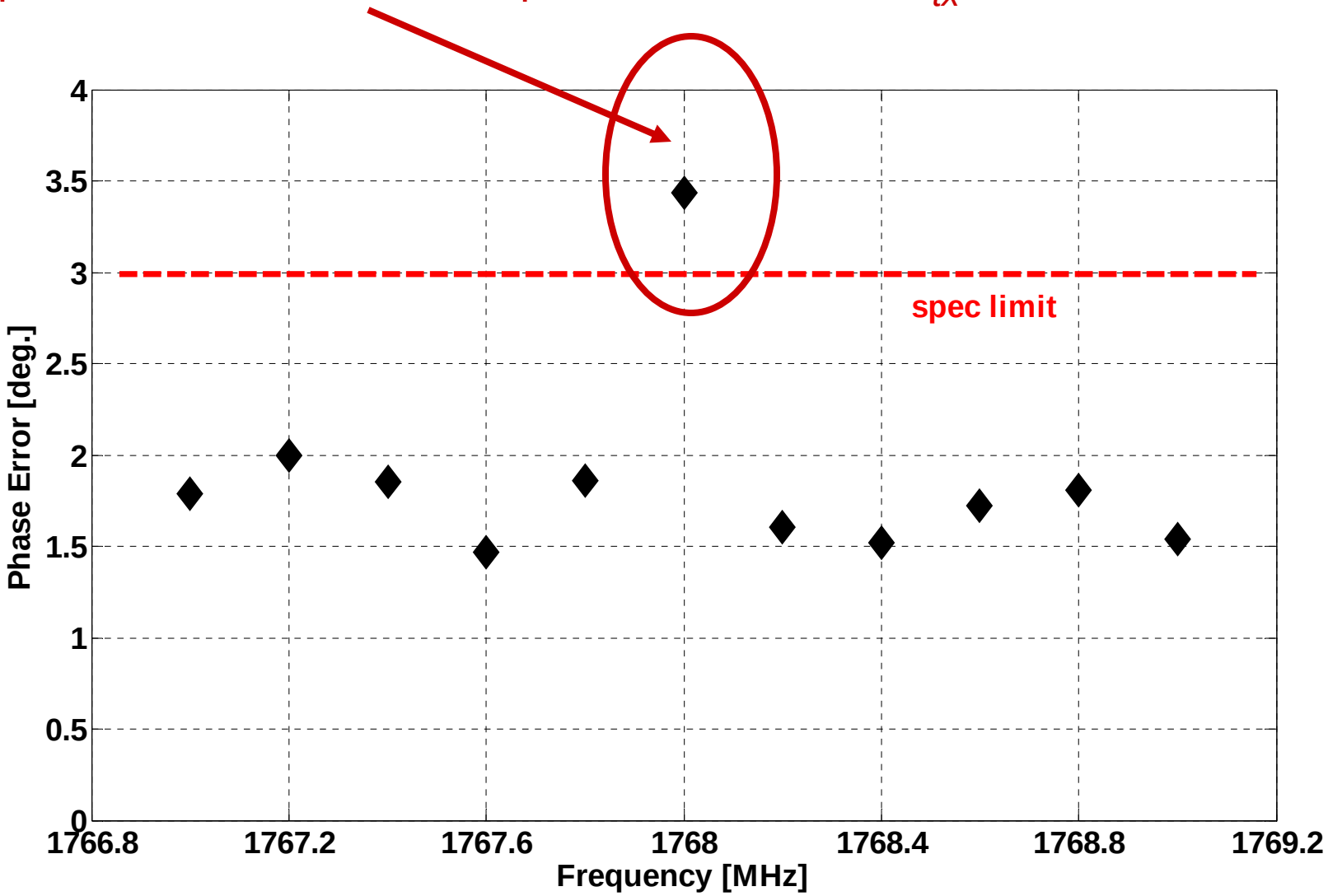
- ADPLL’s FREF clock suffers excessive jitter when TX DCO tuned to “integer channel”: $\boldsymbol{2 \cdot f_{TX} = N \cdot f_R}$
  - Transmitter often fails the phase-trajectory error spec (3° rms)
  - Severity **changes randomly** when ADPLL is relocked
  - Multiple aggressors involved (e.g., turning off the TX path sometimes reduces and sometimes increases the interference)

Die Micrograph of GSM SoC (LoCosto)



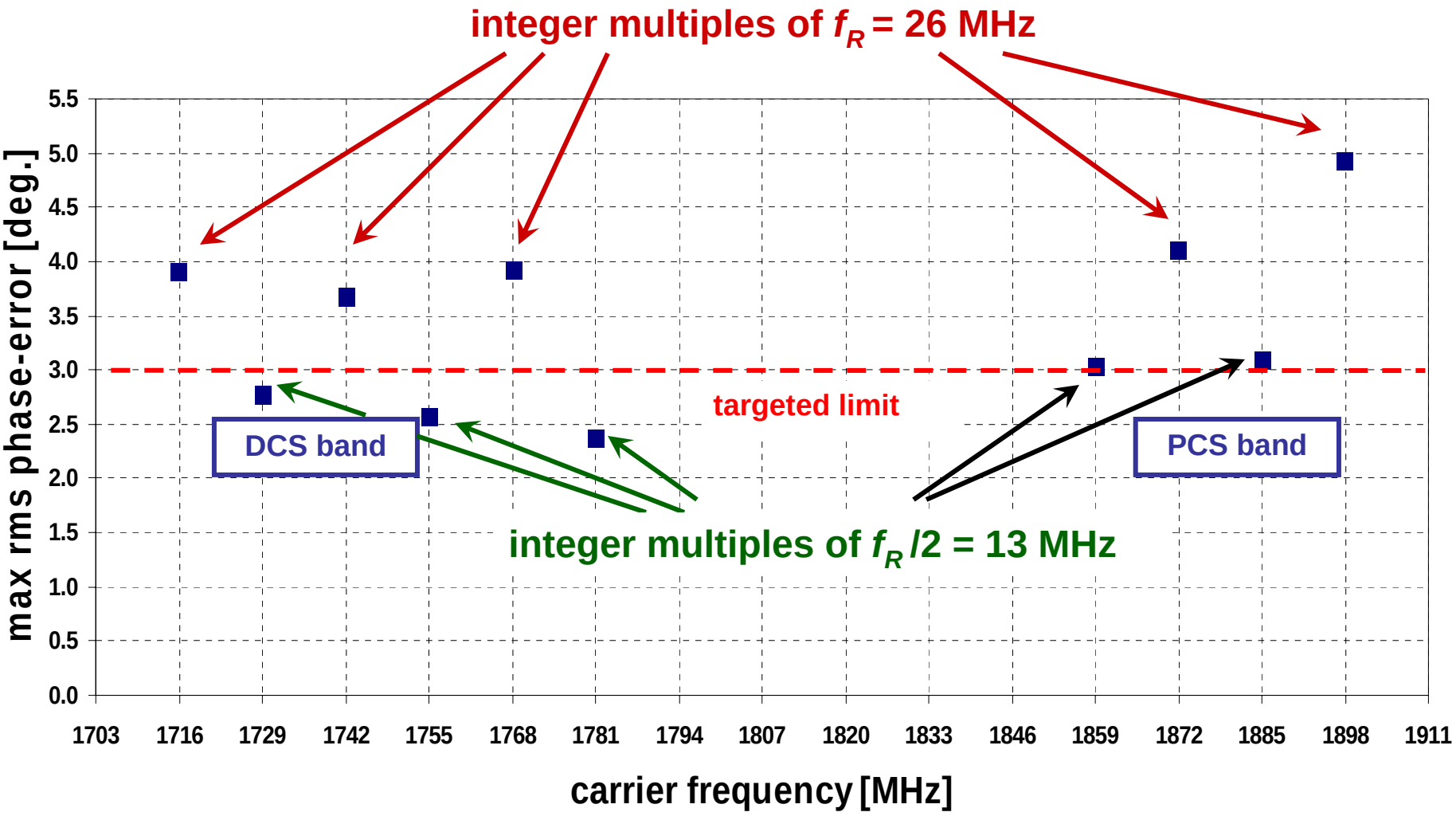
Consequence of this Interference (1/2)

spec violation in “max RMS phase-error” where $F_{tx} = N \cdot 26\ MHz$



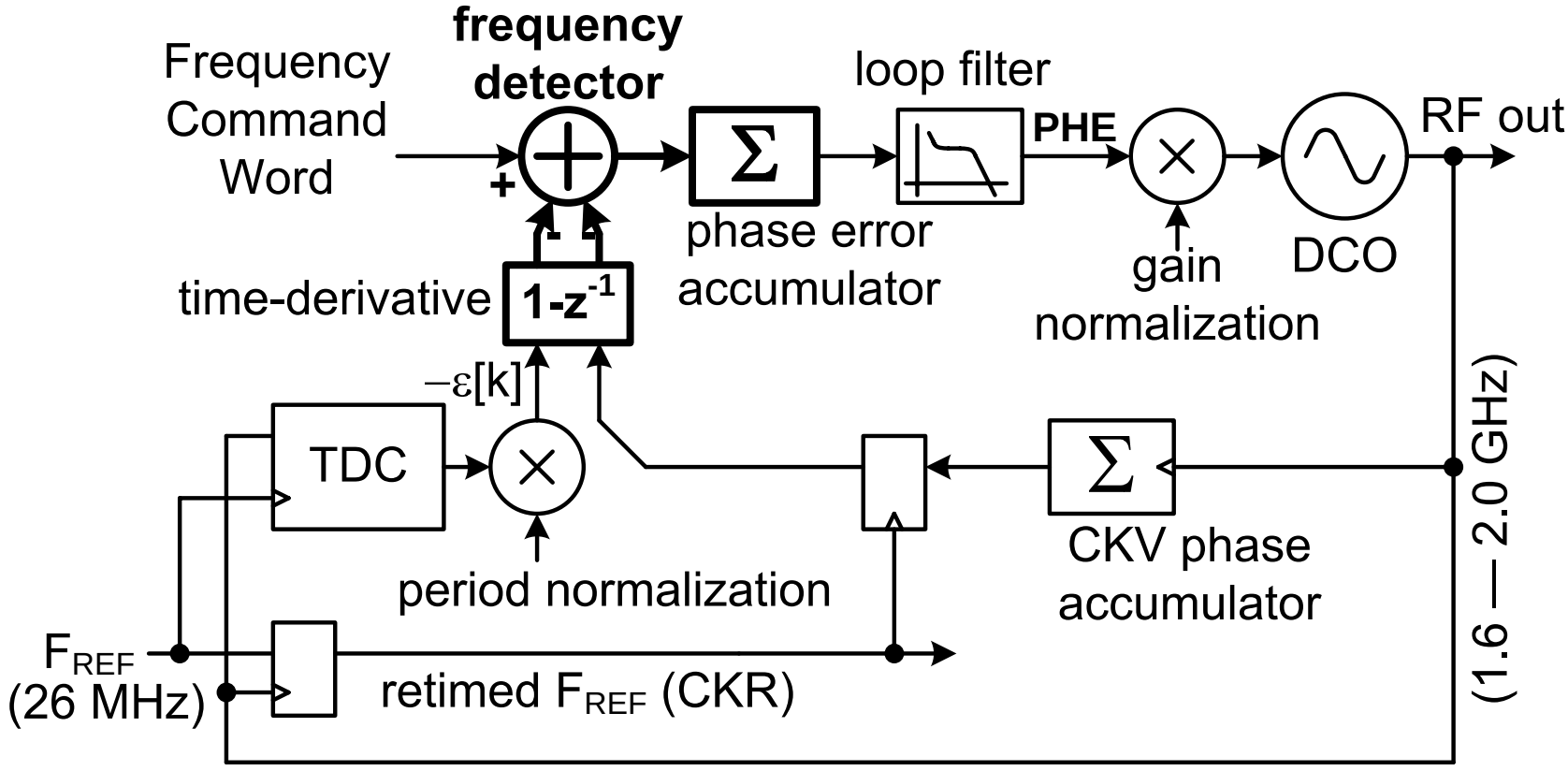
Consequence of this Interference (2/2)

- **integer multiples of FREF=26MHz and FREF/2=13MHz experience interference**



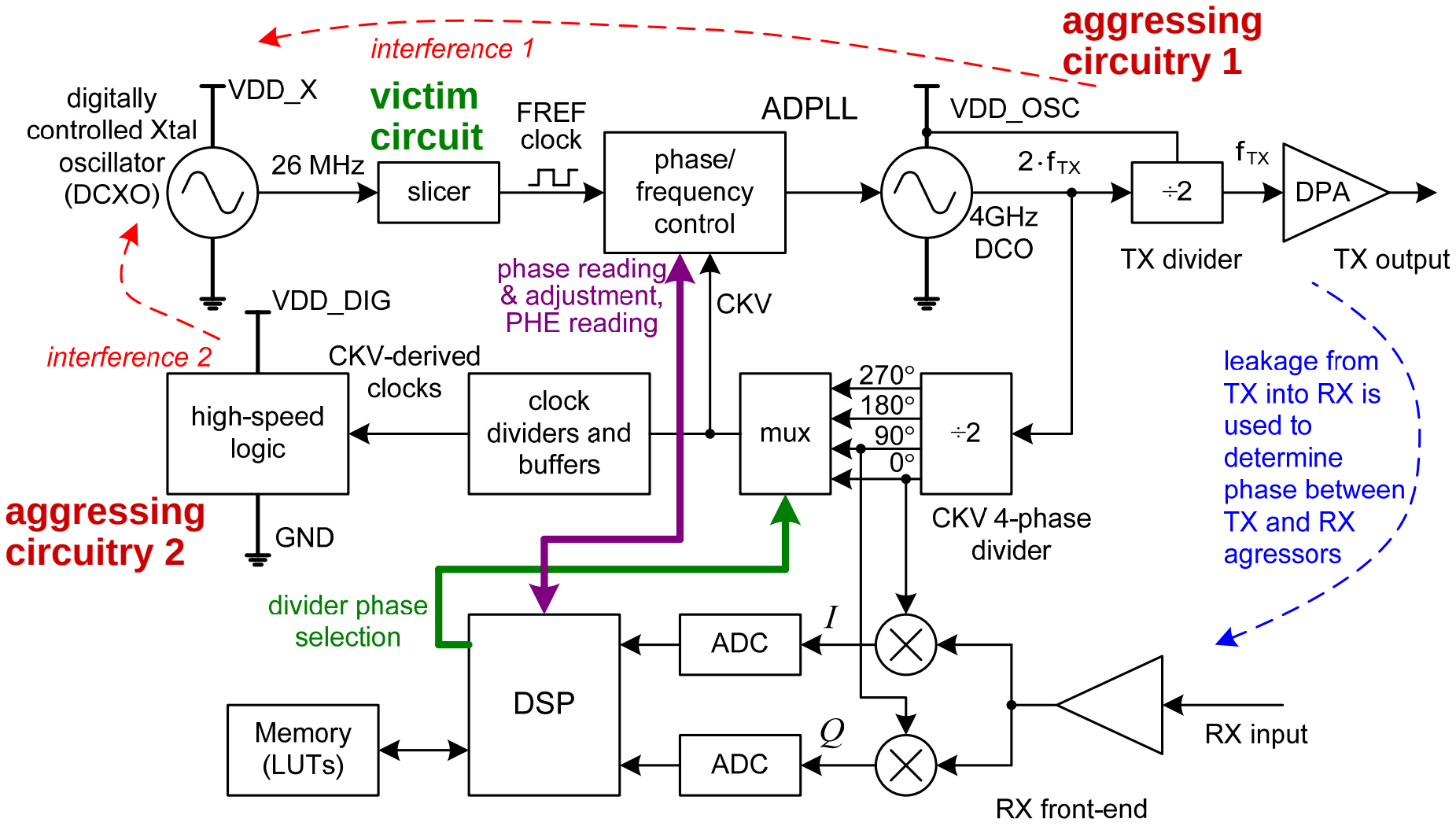
Source for Random CKV-to-FREF Phase

- Frequency (not phase) detector based ADPLL allows for any phase bias to exist between the CKV output signal and the FREF input signal
- Only CKV phase perturbations with respect to the reference phase are 'seen' by the loop as phase errors and are suppressed (within the loop BW)



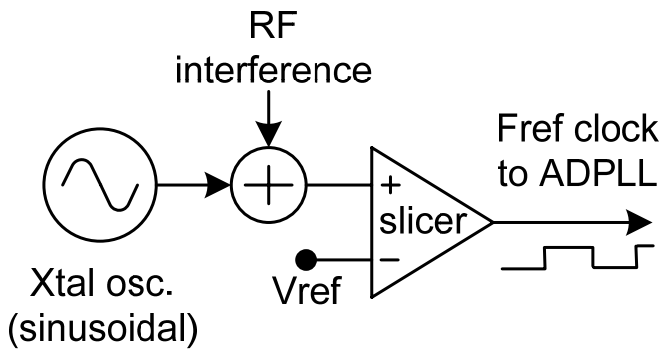
[8] R. B. Staszewski and P. T. Balsara, "All-Digital Frequency Synthesizer in Deep-Submicron CMOS," New Jersey: John Wiley & Sons, 2006.

The Interference Mechanism Components and Environment



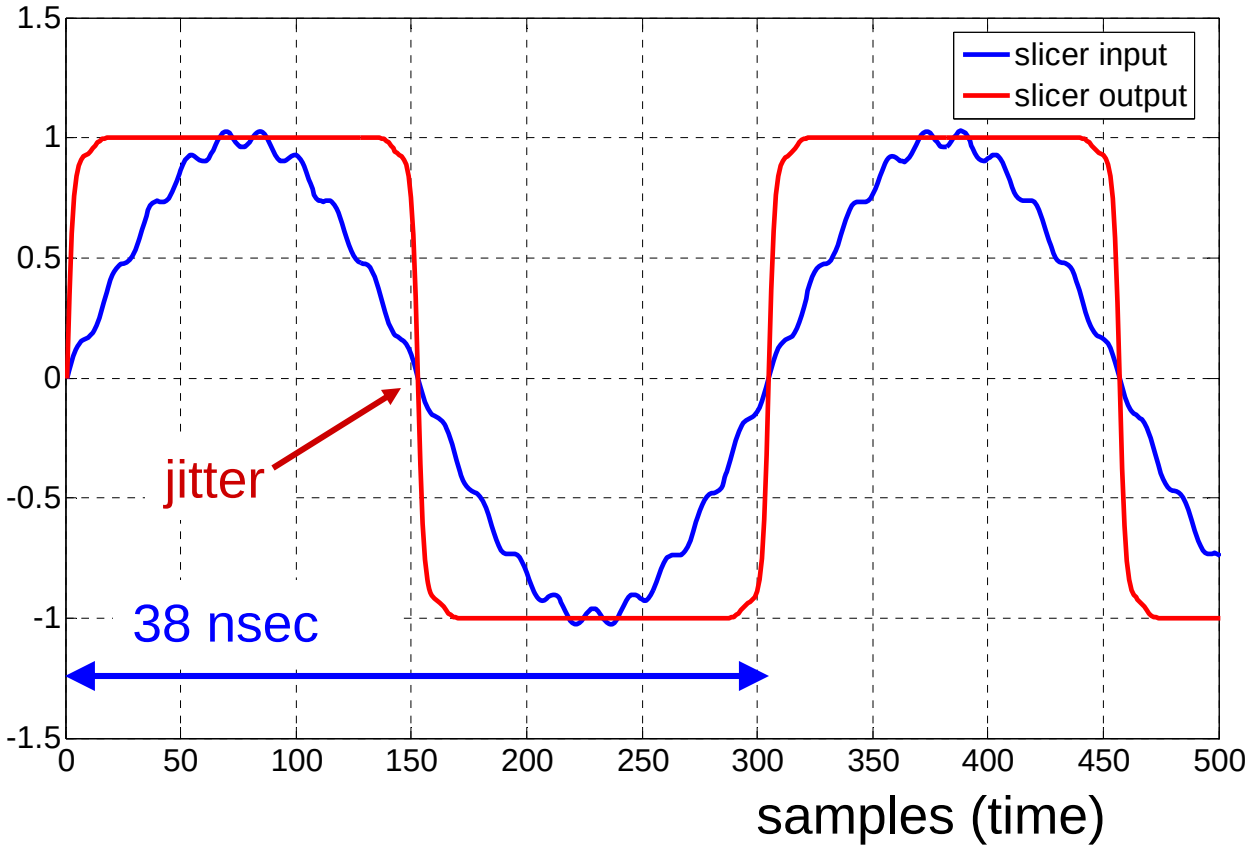
The Victim Signal (FREF Clock for ADPLL)

- The slicer is a non-linear circuit (comparator) that creates a clock signal from a sinusoidal input.

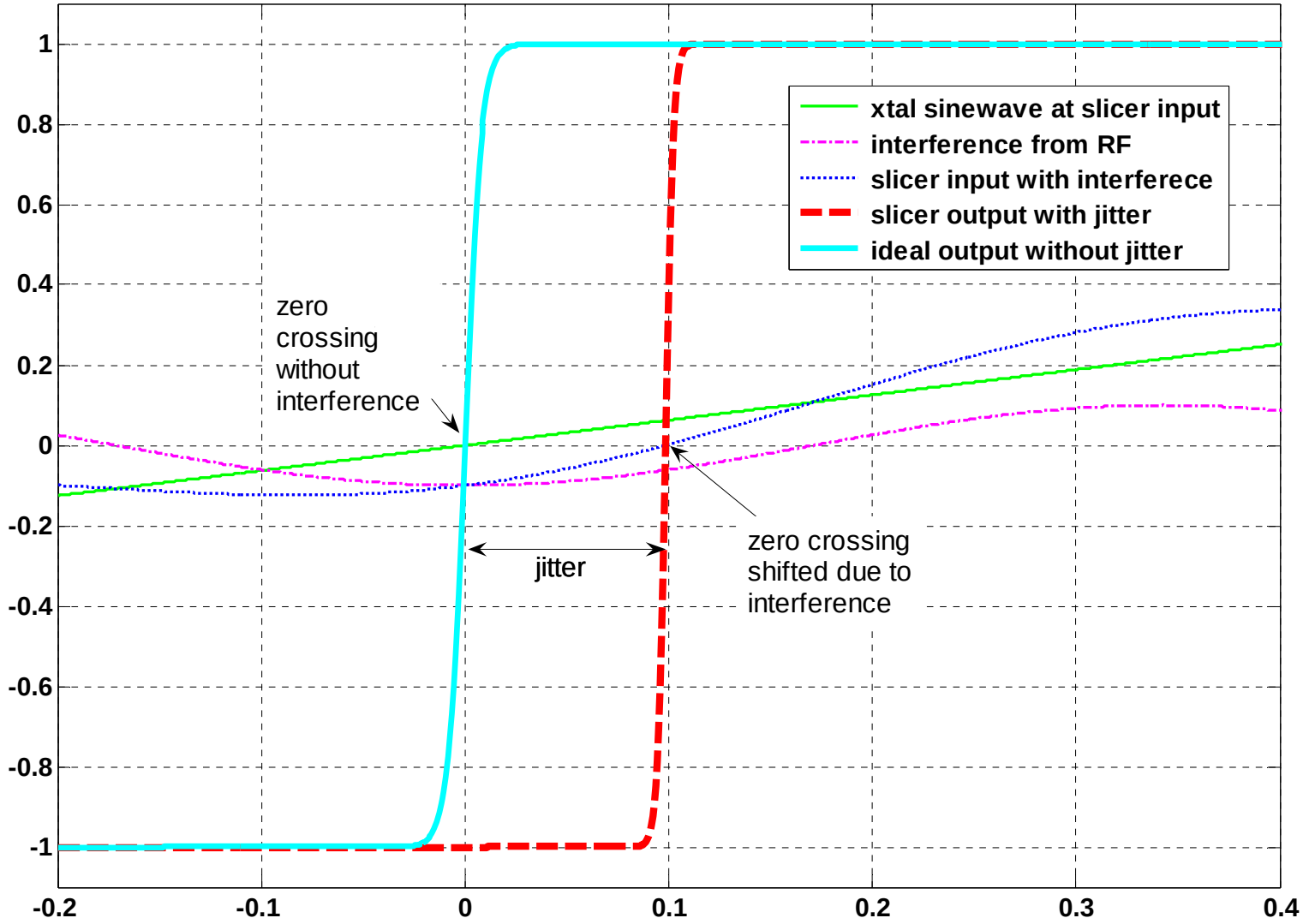


- Additive interference at the slicer's input is translated into jitter at its output.

(26MHz)



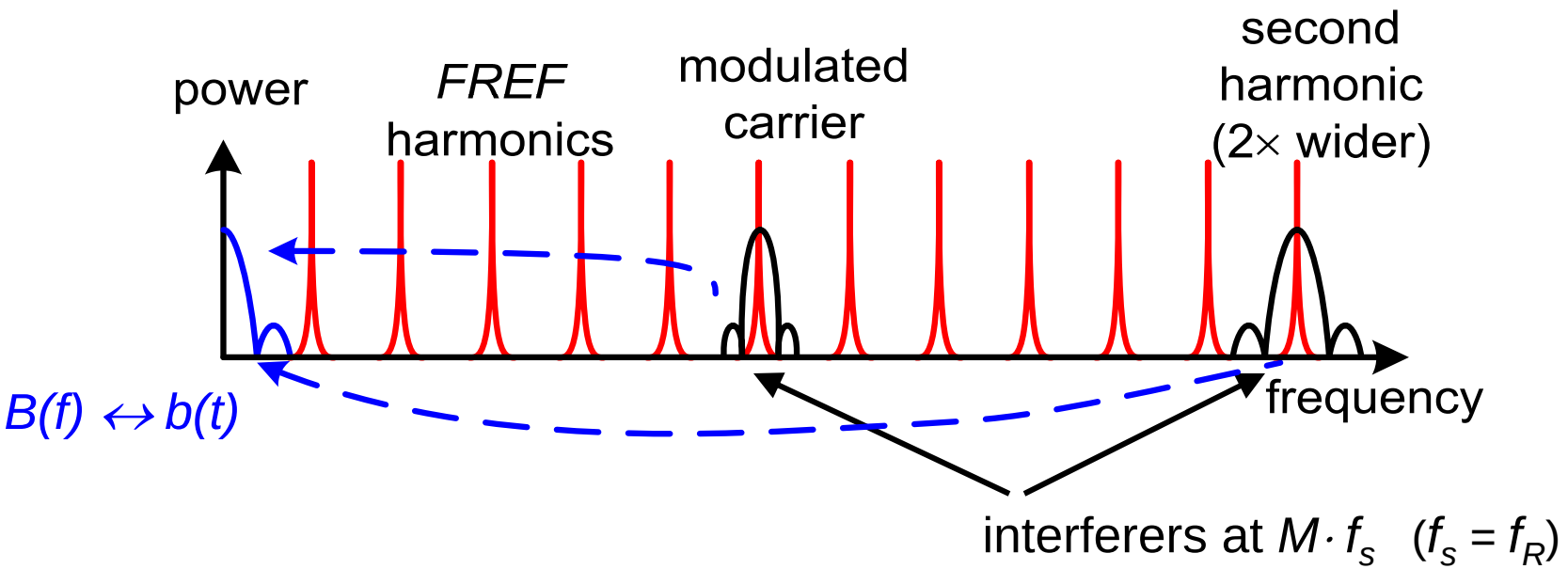
The Creation of Jitter in the FREF Slicer



Mathematical Analysis

- The slicer for the DCXO oscillations effectively samples the aggressor at the threshold-crossing instances, resulting in frequency translation:

$$r(t) = \sum_{n=-\infty}^{\infty} \delta(t - n \cdot \frac{1}{f_S}) \xrightarrow{Fourier} R(f) = \frac{1}{T_S} \sum_{n=-\infty}^{\infty} \delta(f - n \cdot f_S)$$



- The interfering signal at baseband is the sum of all down-converted products:

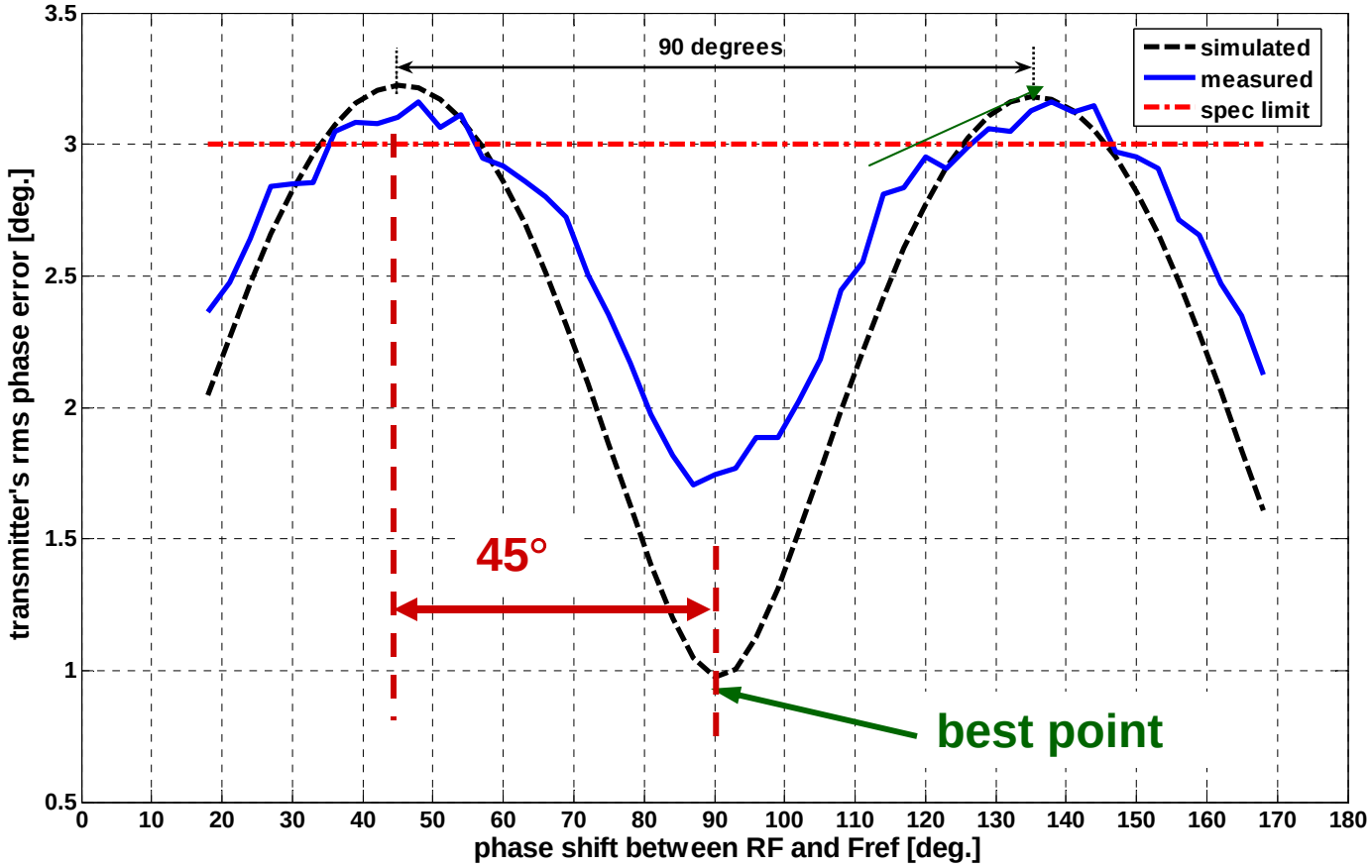
$$b(t) = \sum_{k=1}^{L} \tilde{A}_k \cdot Cos\{\varphi_k(t) + \Phi_k\}$$

no carrier frequency term (zero)

phase between FREF harmonic and interferer k

Measured Performance vs. Phase

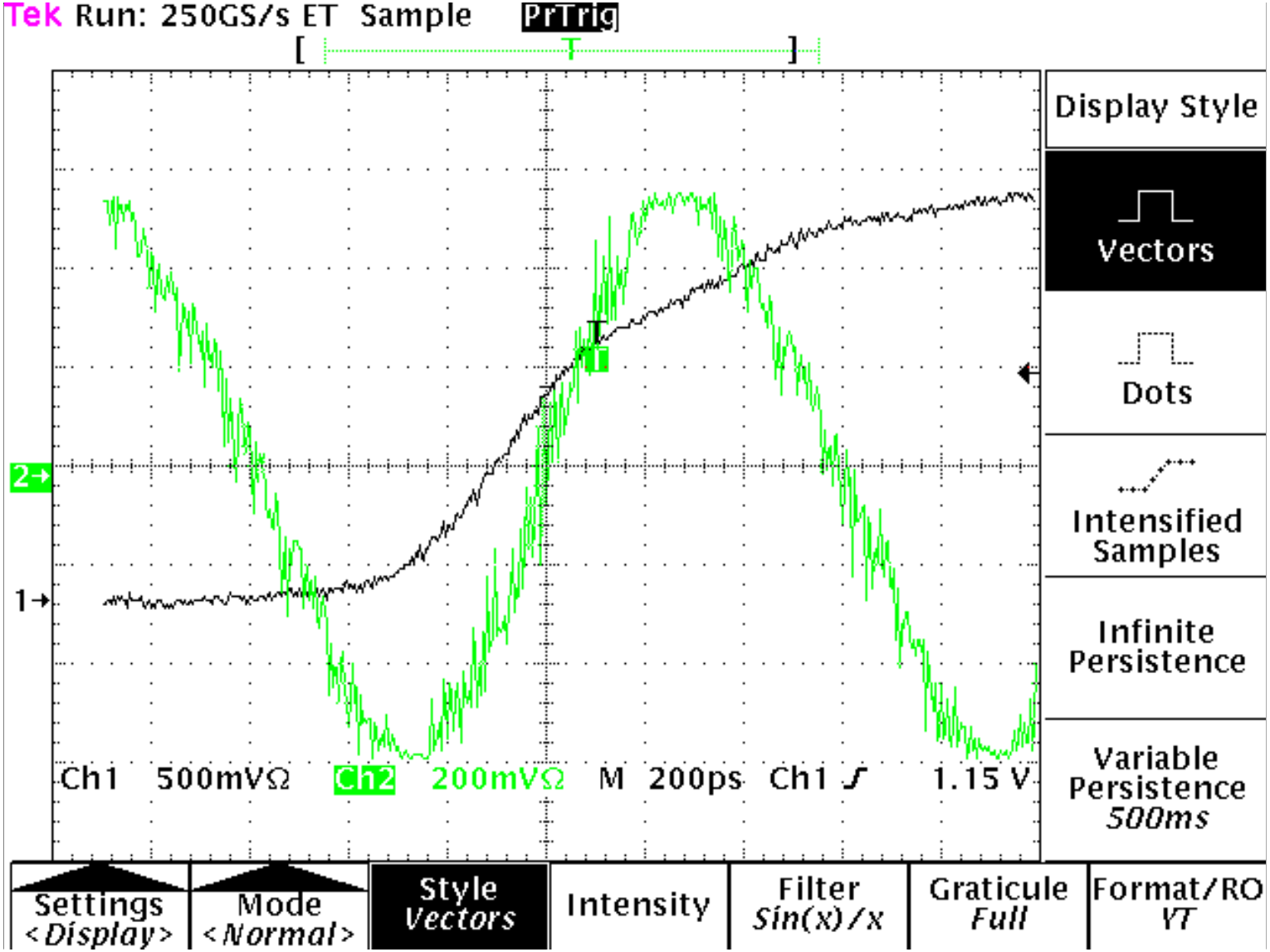
- Periodic performance recorded vs. phase (absolute phase not known)
- This phase shift could not be supported in a typical conventional PLL !
- Distance between best and worst points is 45° and periodicity is **90°**



software controlled phase steps of 3°

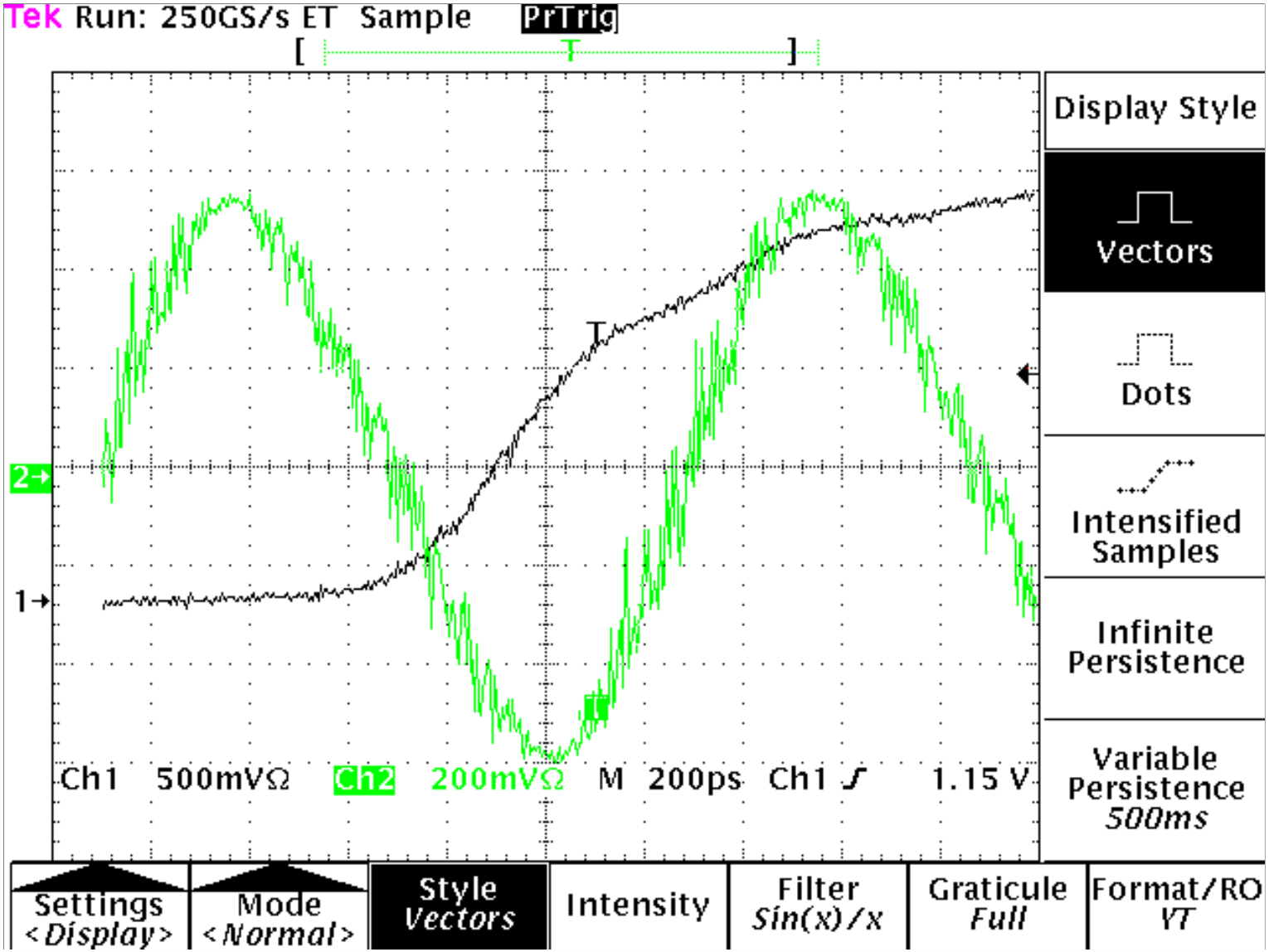
Validation of Phase Shifting Routine (1/2)

- The output RF signal is shown with respect to FREF rising edge (step 0).



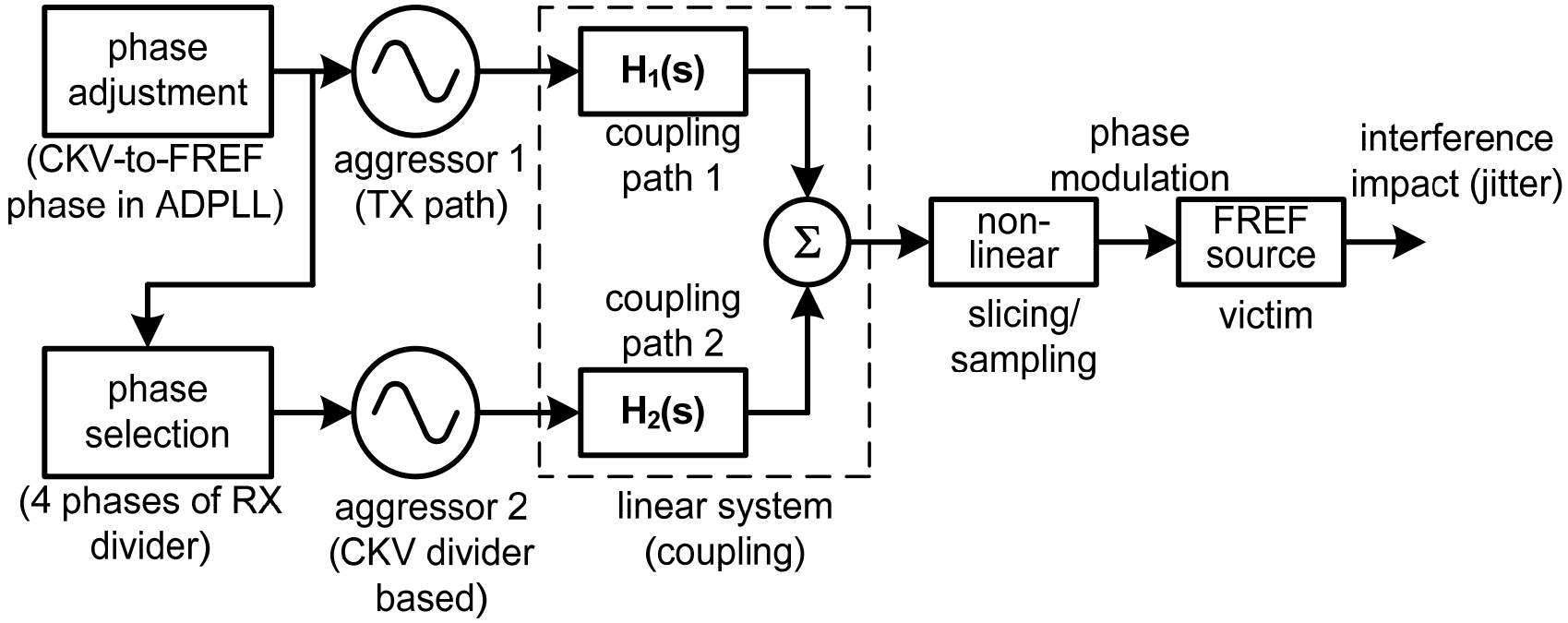
Validation of Phase Shifting Routine (2/2)

- After 30 steps of 3° (90° shifting):



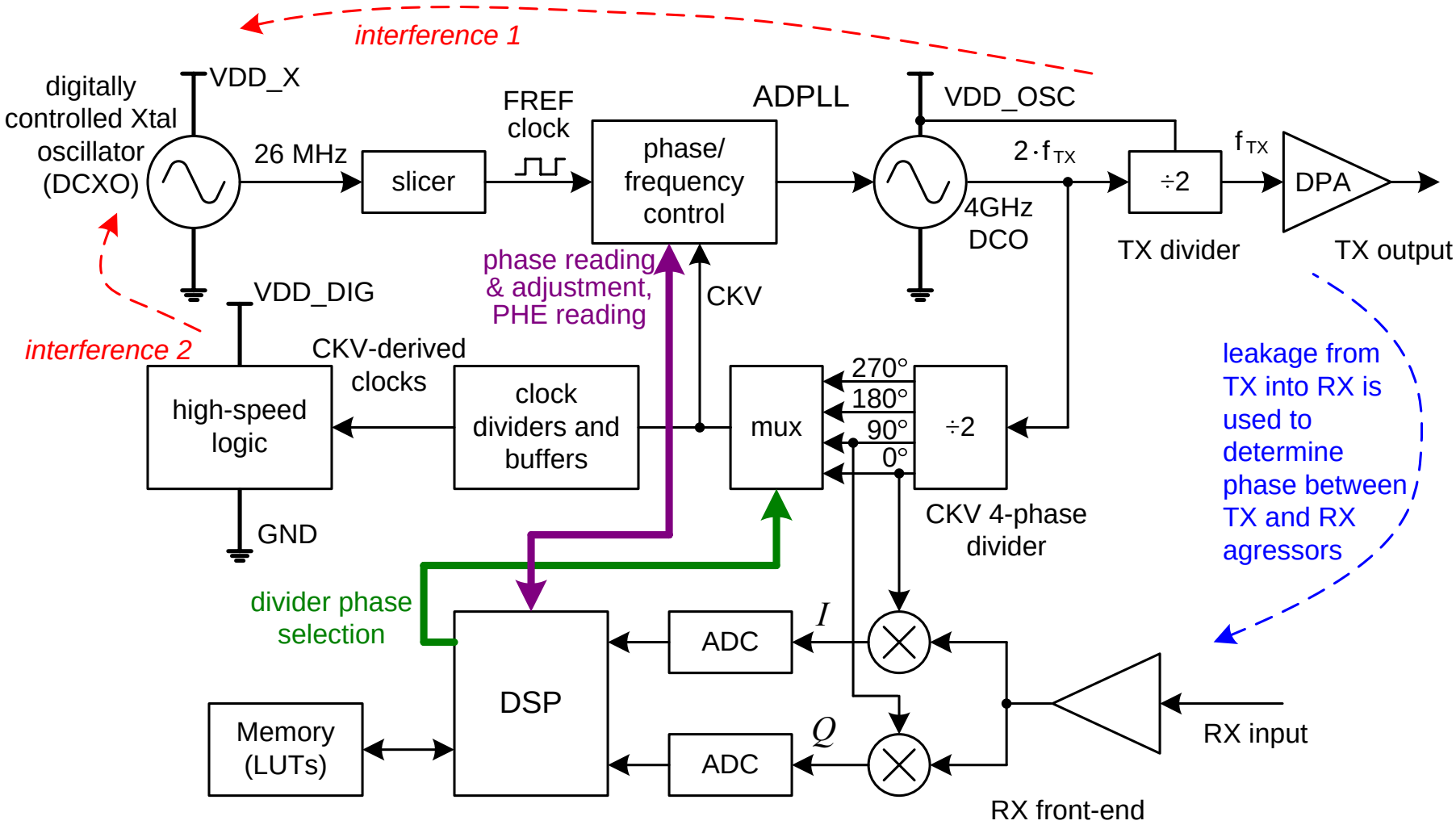
Identification & Isolation of Aggressors

- Each of the aggressing sources (TX path and CKV divider driven) is rich in harmonic content (e.g., fundamental and 2nd harmonic)
- Each aggressor propagates to the victim through a different path defined by a transfer function
- Two independent hooks exist for the control of relative phases



A mathematical model for the addition of the two aggressing sources

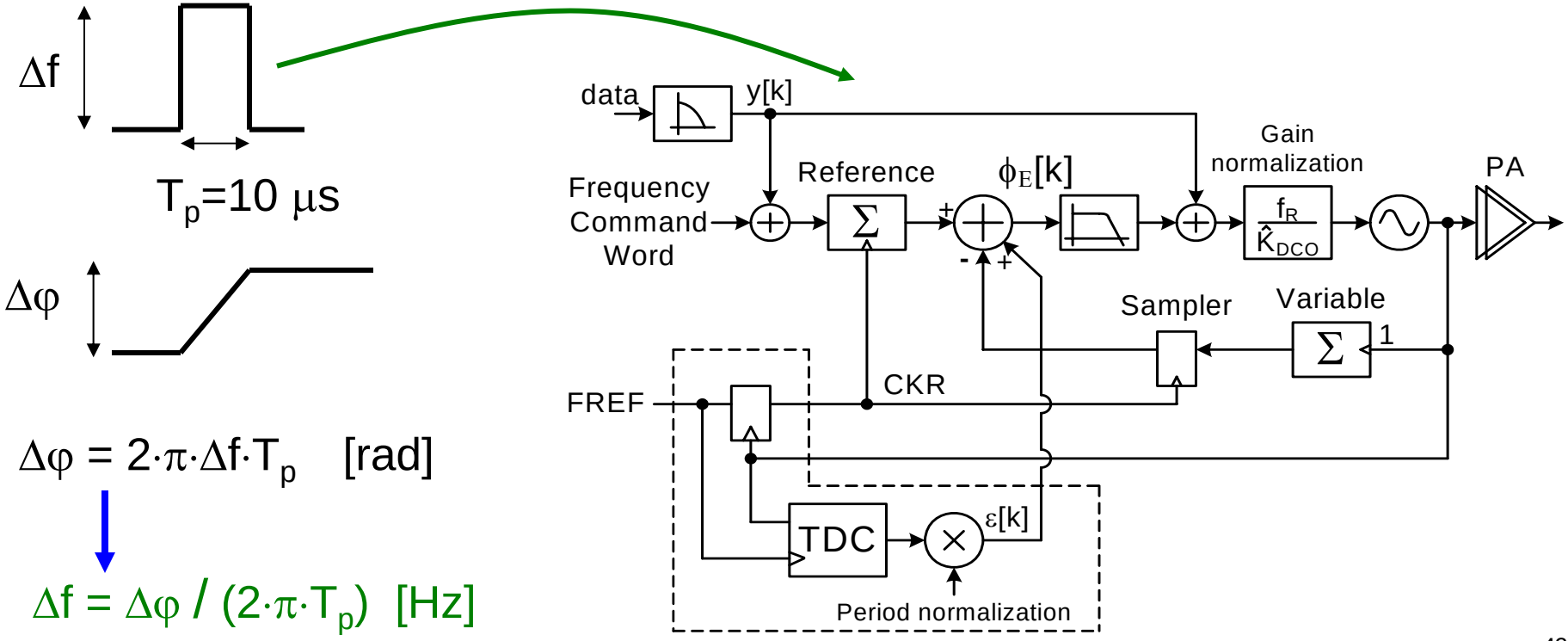
The Phase-Adjustment Solution



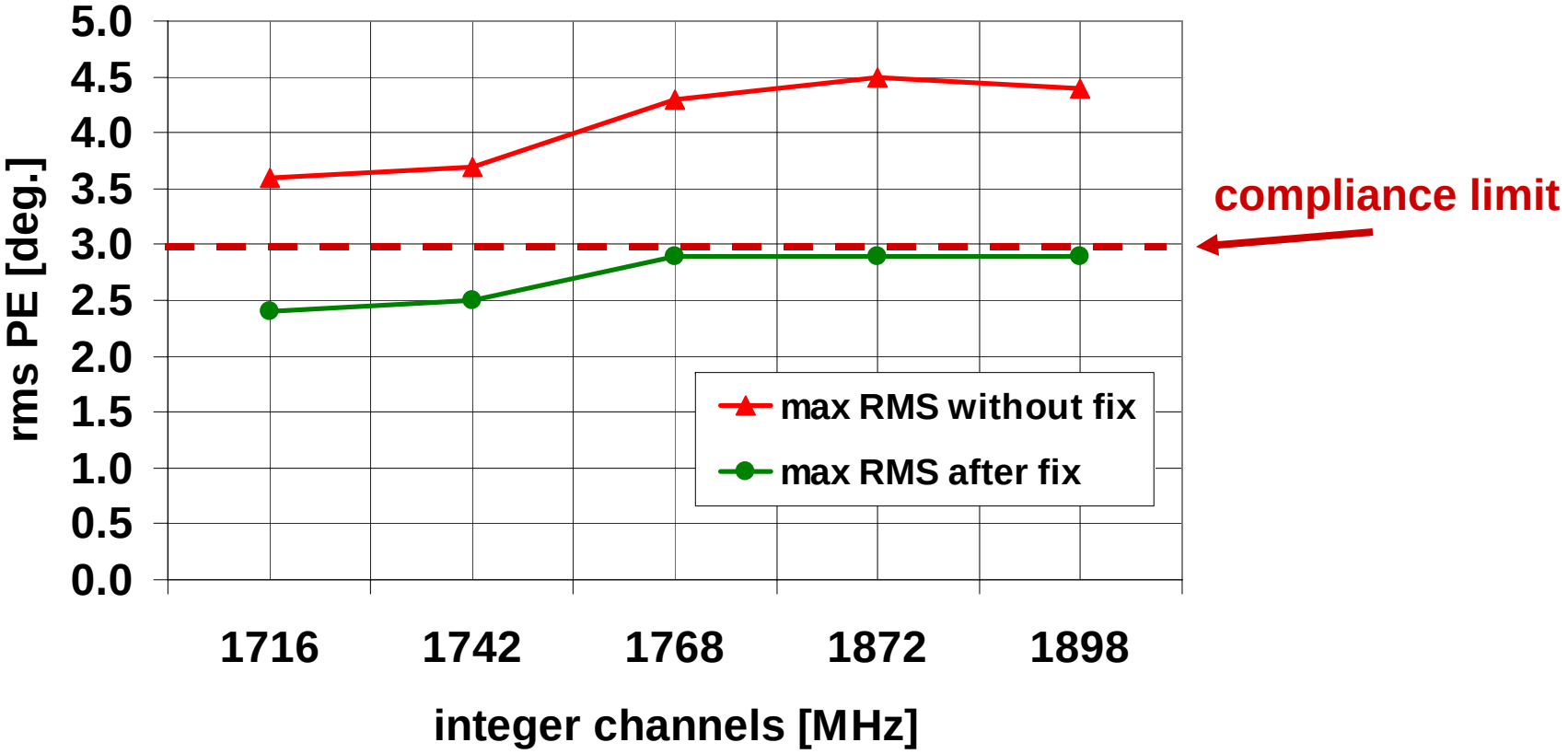
- Software solution implemented based on existing capabilities of the DRP (no hardware changes required)

Calculating and Applying the Compensation

- The necessary phase shift is calculated based on a phase reading from the TDC (time-to-digital-converter) before the data modulation starts.
- Since the performance has a 90° periodicity, the phase-shift is calculated modulo 90° (i.e., limited to ±45°).
- The phase compensation is implemented through a frequency pulse that is applied to the two-point frequency-modulation input of the ADPLL:

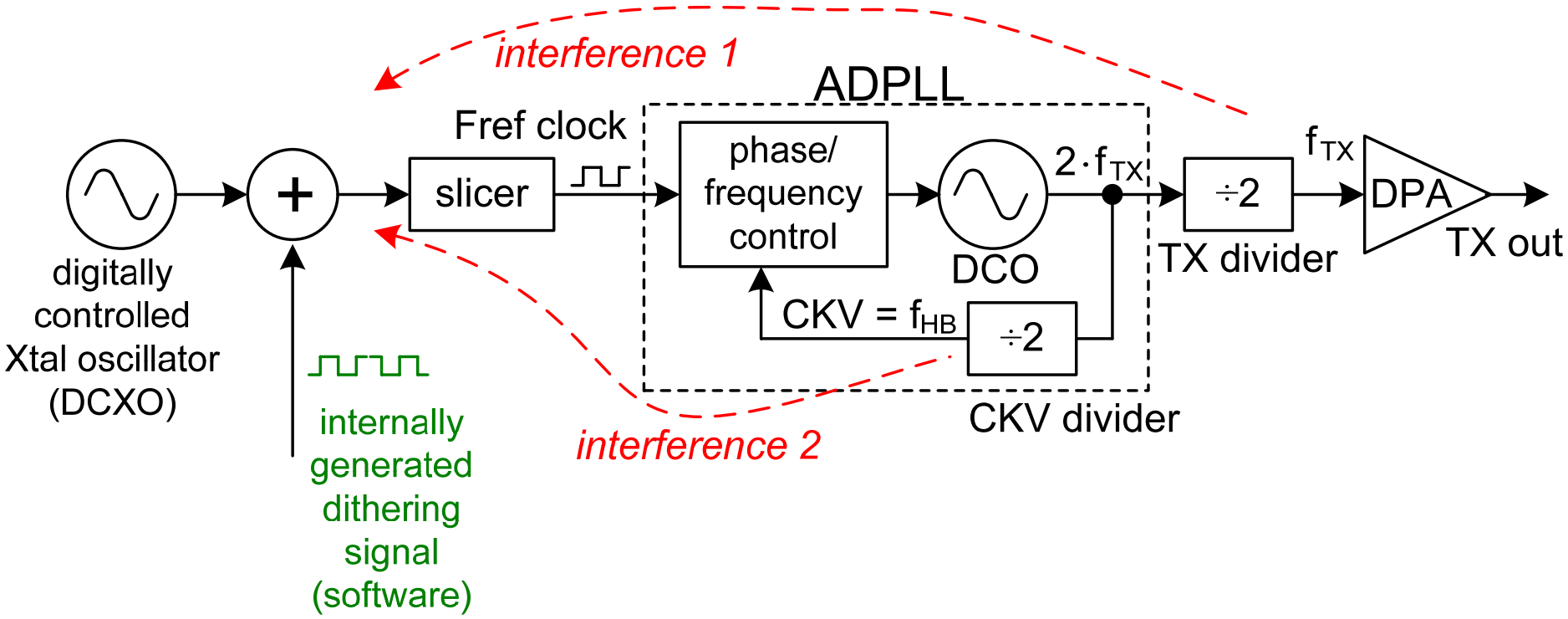


Measured Results Demonstrating the Effectiveness of the Solution



- Performance after employing the software based solution is shown to bring the PTE performance to within compliance!

The Victim-Dithering Based Solution ('Mitch Dither')



- Solution developed entirely in software by Mitch Entezari (patented).
  → no need for hardware redesign!
- Interference energy is effectively spread to higher frequencies, where the ADPLL low-pass can suppress it.

Example 2

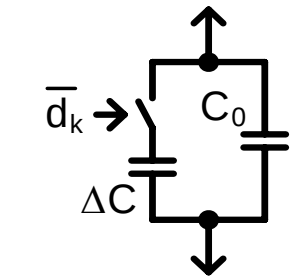
DCO modulation distortion caused by interference from the digital frequency tuning inputs

(the 'flyback' delay effect)

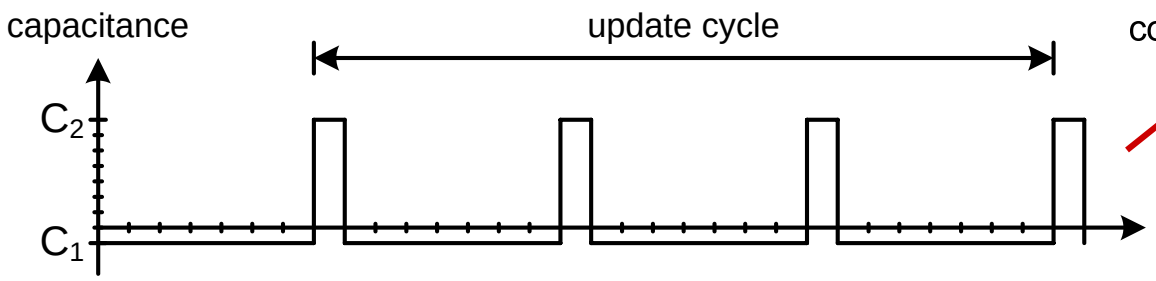
Related publications:

1. **I. Bashir, Robert Bogdan Staszewski, and Oren Eliezer, "Tuning Word Retiming of a Digitally-Controlled Oscillator Using RF Built-In Self Test", Proceedings of IEEE DCAS 2005**
2. **O. Eliezer, I. Bashir, R. B. Staszewski and P. T. Balsara "Built-in Self Testing of a DRP-Based GSM Transmitter", RFIC 2007 RMO4D-2, June 2007**

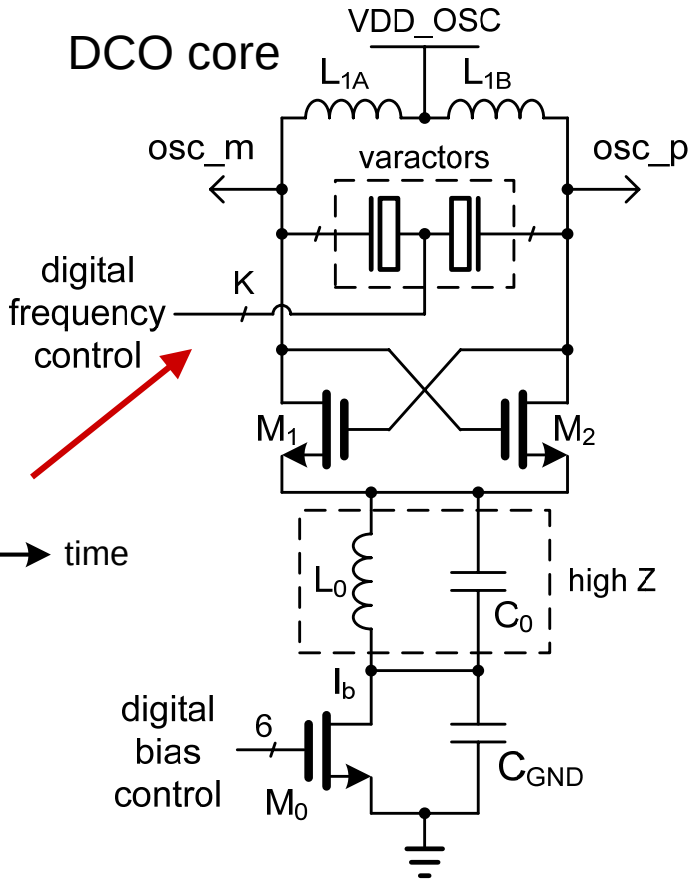
Description of Problem



varactor model



sigma-delta dithering signal for fine-frequency tuning

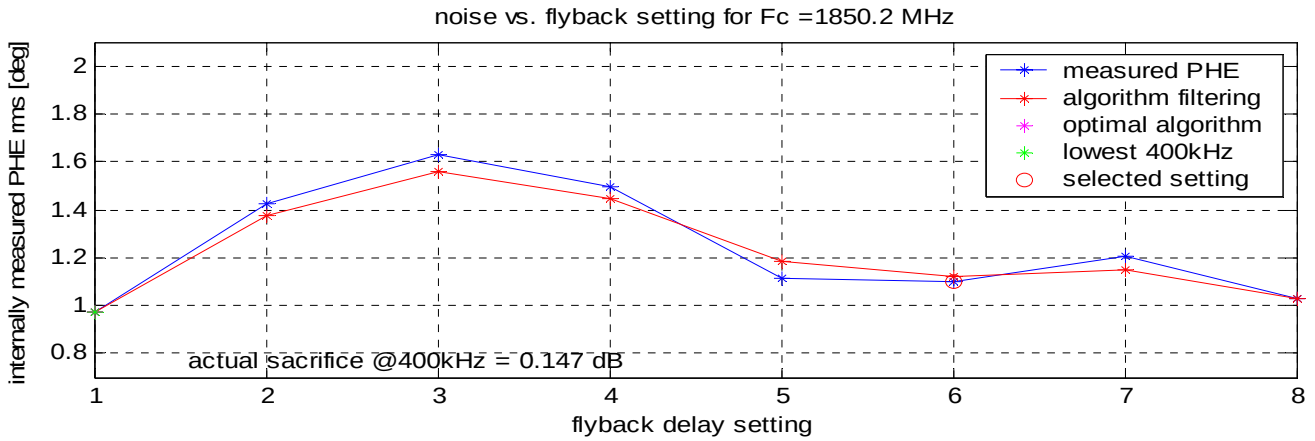


- **TX performance depends on timing of SD signal**
  - **close-in and far-out spectrum impacted (TX mask violations)**
  - **modulation accuracy (phase error in GSM, frequency deviation in Bluetooth)**

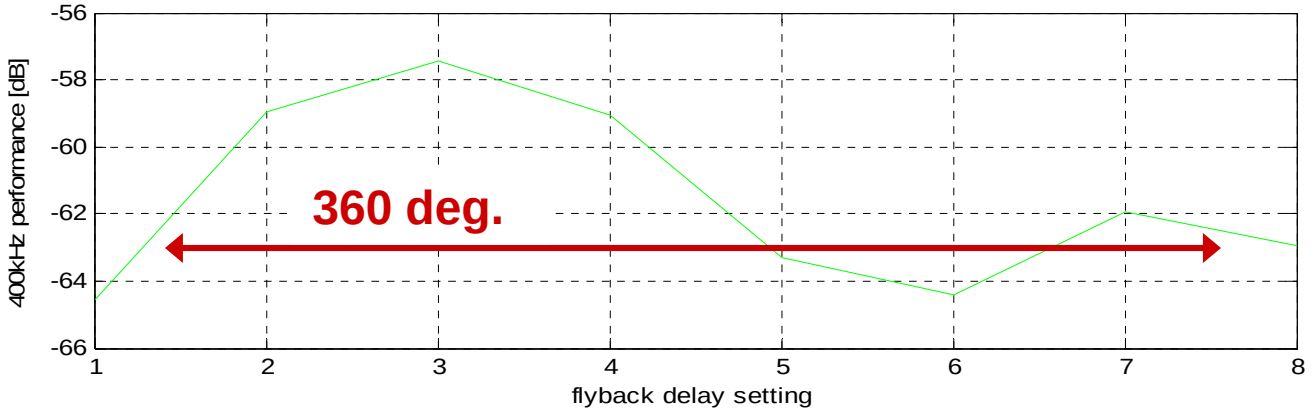
Measured Performance vs. Phase-Shift

Sweeping through 0-360° phase shift between the SD clock and the DCO signal produces a periodic result (**using random data**):

TX phase error

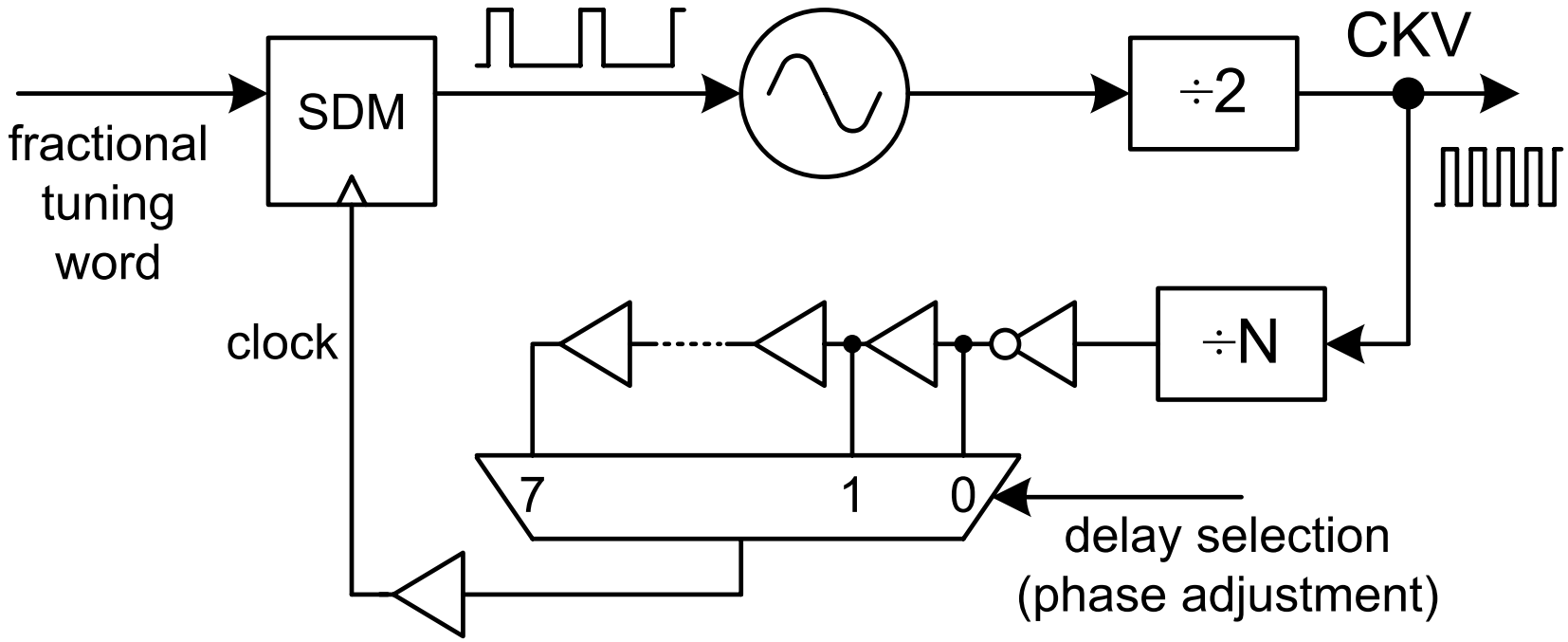


400kHz 'noise'



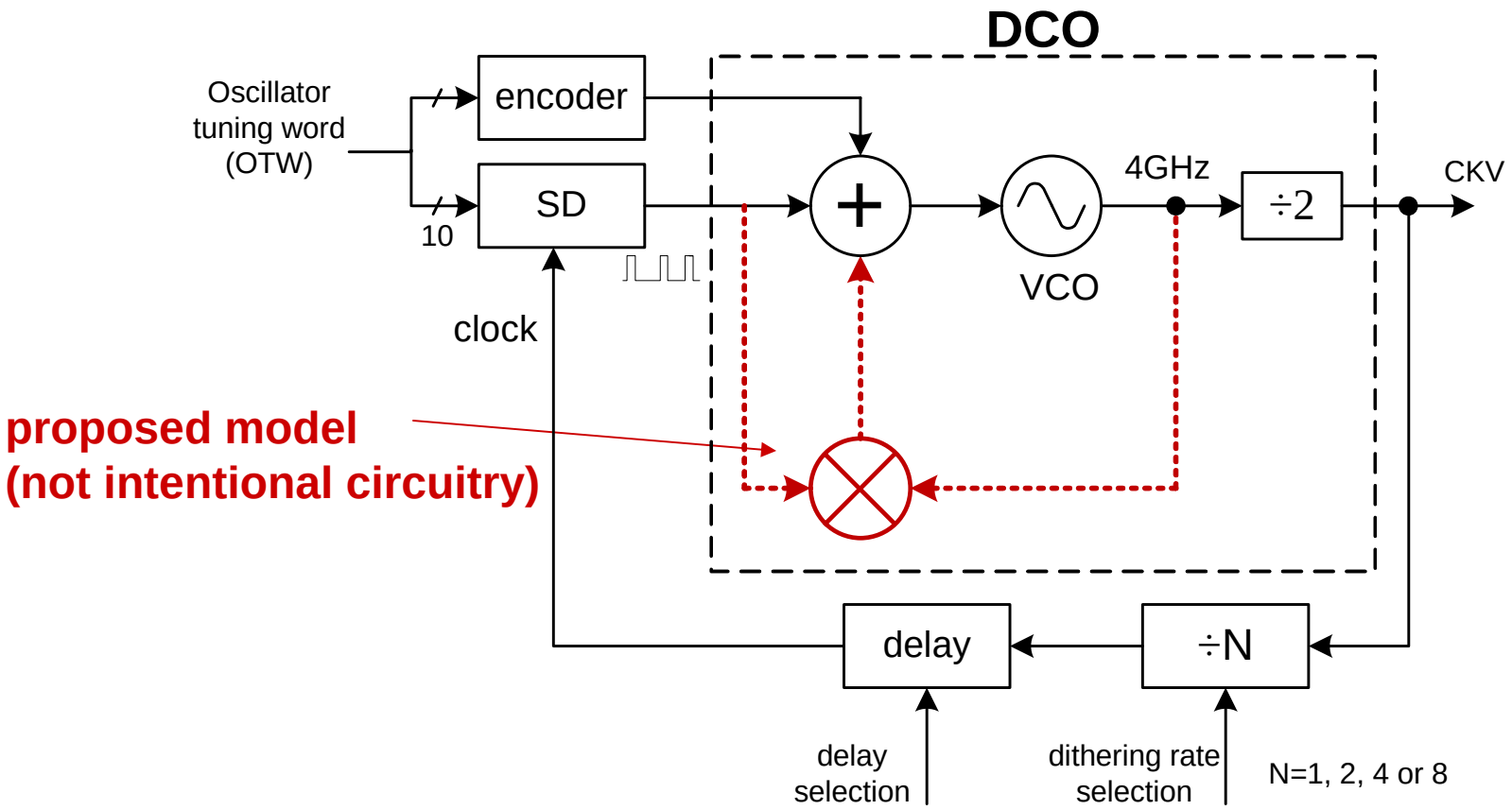
CKV/SD-clock 'flyback' delay setting

The Delay/Phase Adjustment Circuit



- Phase of sigma-delta dithering signal with respect to DCO oscillations is selectable (software controlled)
- Time resolution = buffer's delay = ~40ps = ~50° (depends on frequency)
- Circuit covers over 360° of DCO period

Mathematical Model

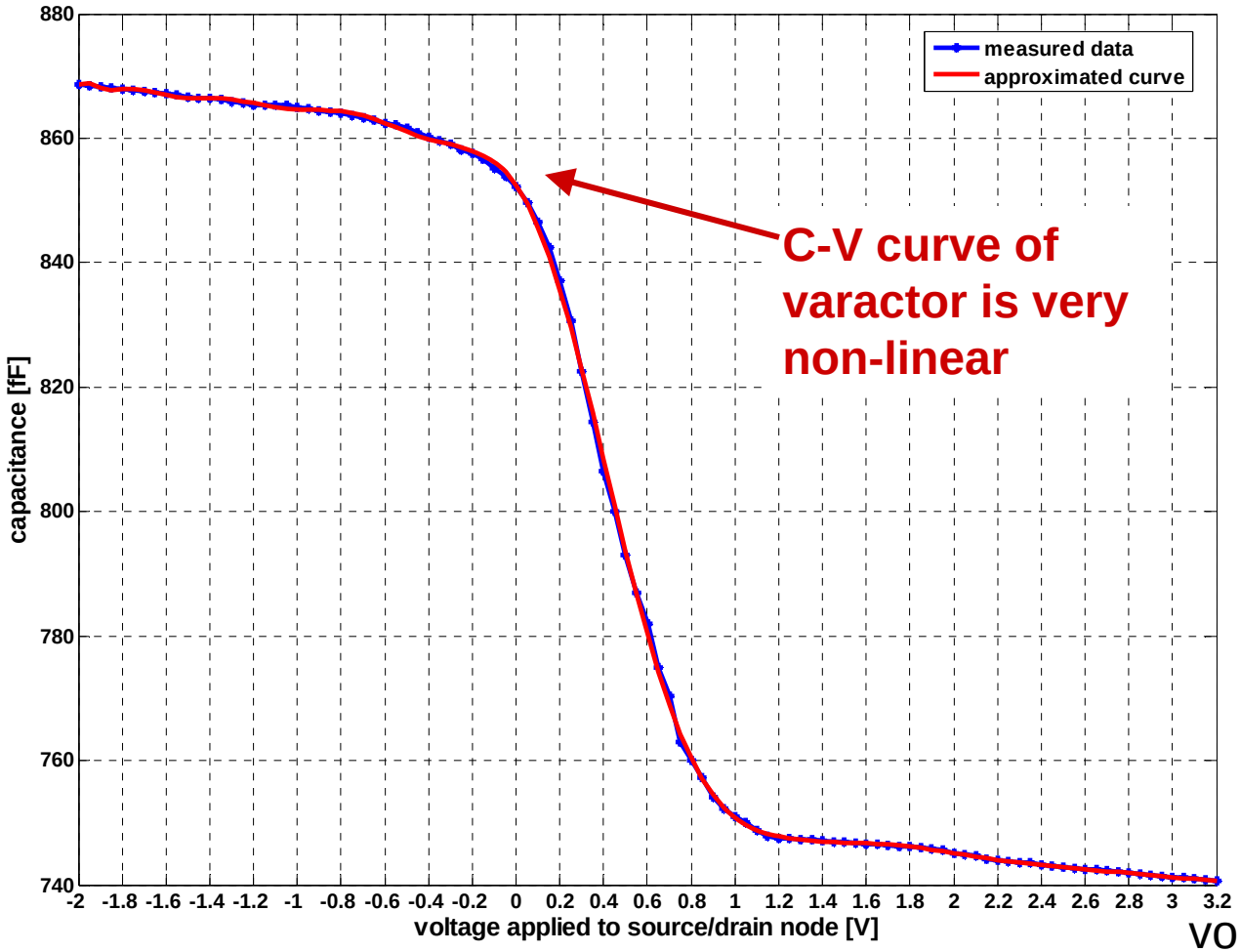


- Multiplication in diagram represents the creation of products due to non-linearity in C-V curve of dithered varactor
  - The products do not have to be in voltage domain (capacitance)
  - The interference products create parasitic analog FM that is added to the desired digital FM

Source for Non-Linearity (Mixing)

- The dithered varactor experiences both a large signal oscillation and a high-speed logic-level (0V/1.5V) dithering signal.
- Superposition cannot be assumed for the sum of these two large signals.

capacitance



voltage

Mathematical Analysis → Phase Dependency

The energy in the SD signal around the DCO frequency may be represented as:

$$SD_o(t) = A(t) \cdot Sin\{2\pi f_o t + \theta_{SD}\}$$

phase with respect to DCO signal

With the oscillations of the DCO represented by:

$$DCO(t) = Sin\{2\pi f_o t\}$$

The mixing of the two would produce the interfering baseband signal:

$$b(t) = \beta \cdot SD_o(t) \cdot DCO(t)$$

not a voltage signal (capacitance)

'conversion gain'

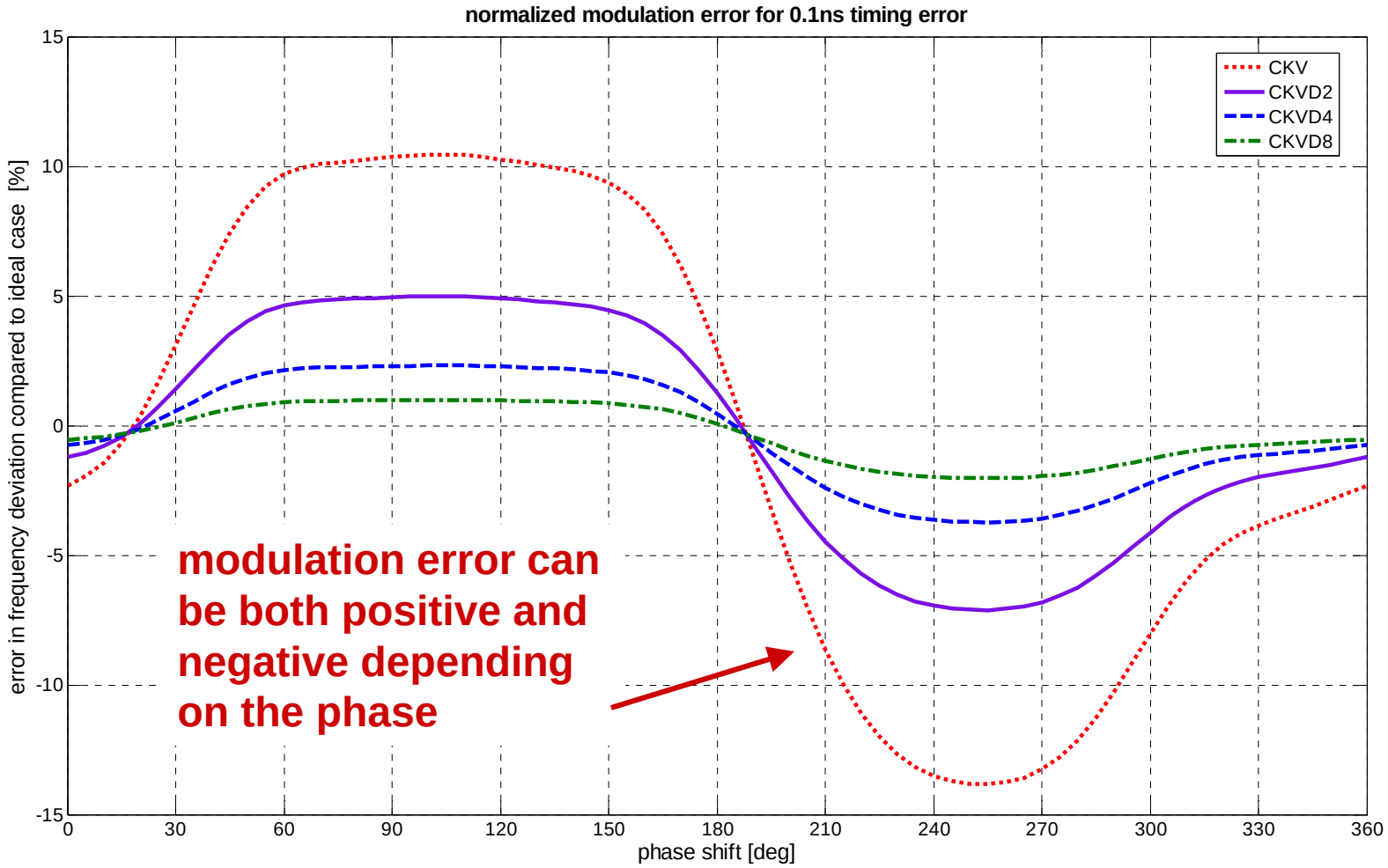
$$b(t) = \beta \cdot A(t) \cdot Sin\{2\pi f_o t + \theta_{SD}\} \cdot Sin\{2\pi f_o t\} =$$

$$= \frac{\beta}{2} \cdot Cos(\theta_{SD}) \cdot A(t)$$

Periodic dependency on phase!

Simulation of Modulation Error vs. Phase

- Actual varactor curve used and specific timing asymmetry assumed in SD
- Phase between SD signal and DCO oscillations swept → 360° period

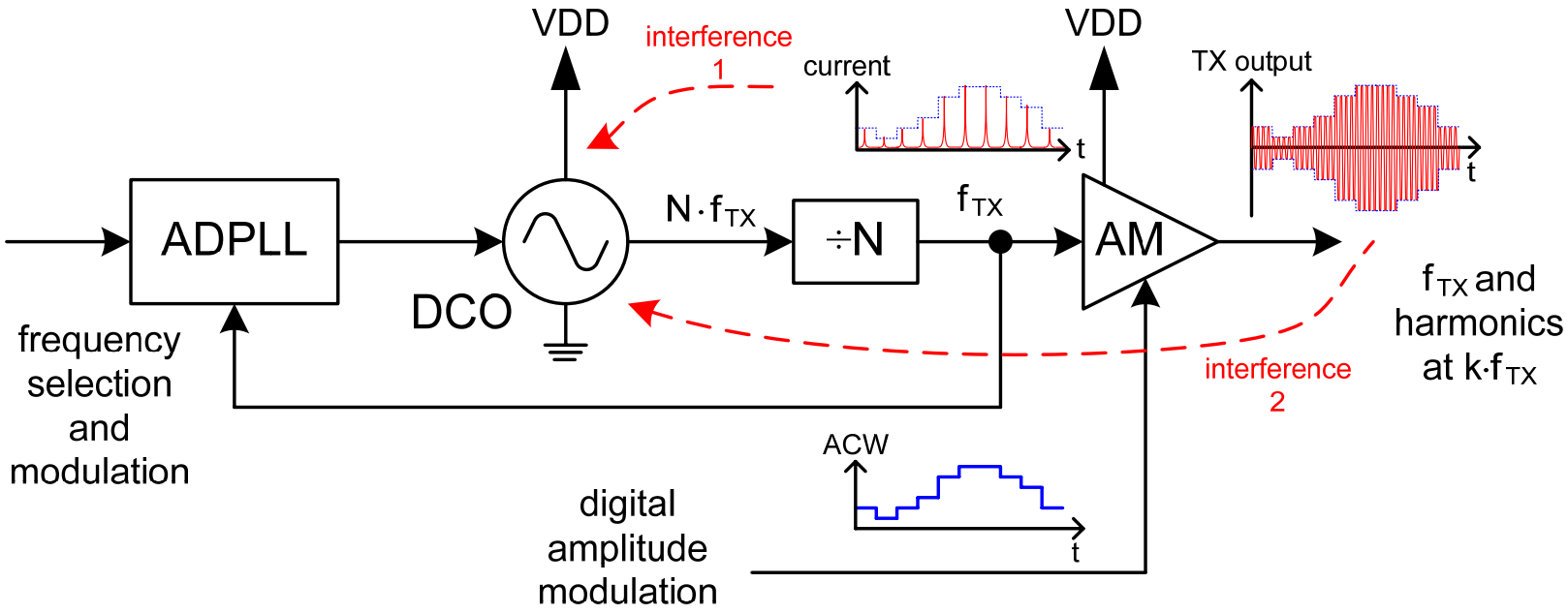


Example 3

Parasitic frequency modulation on DCO caused by AM stage

(‘DCO frequency-pulling’)

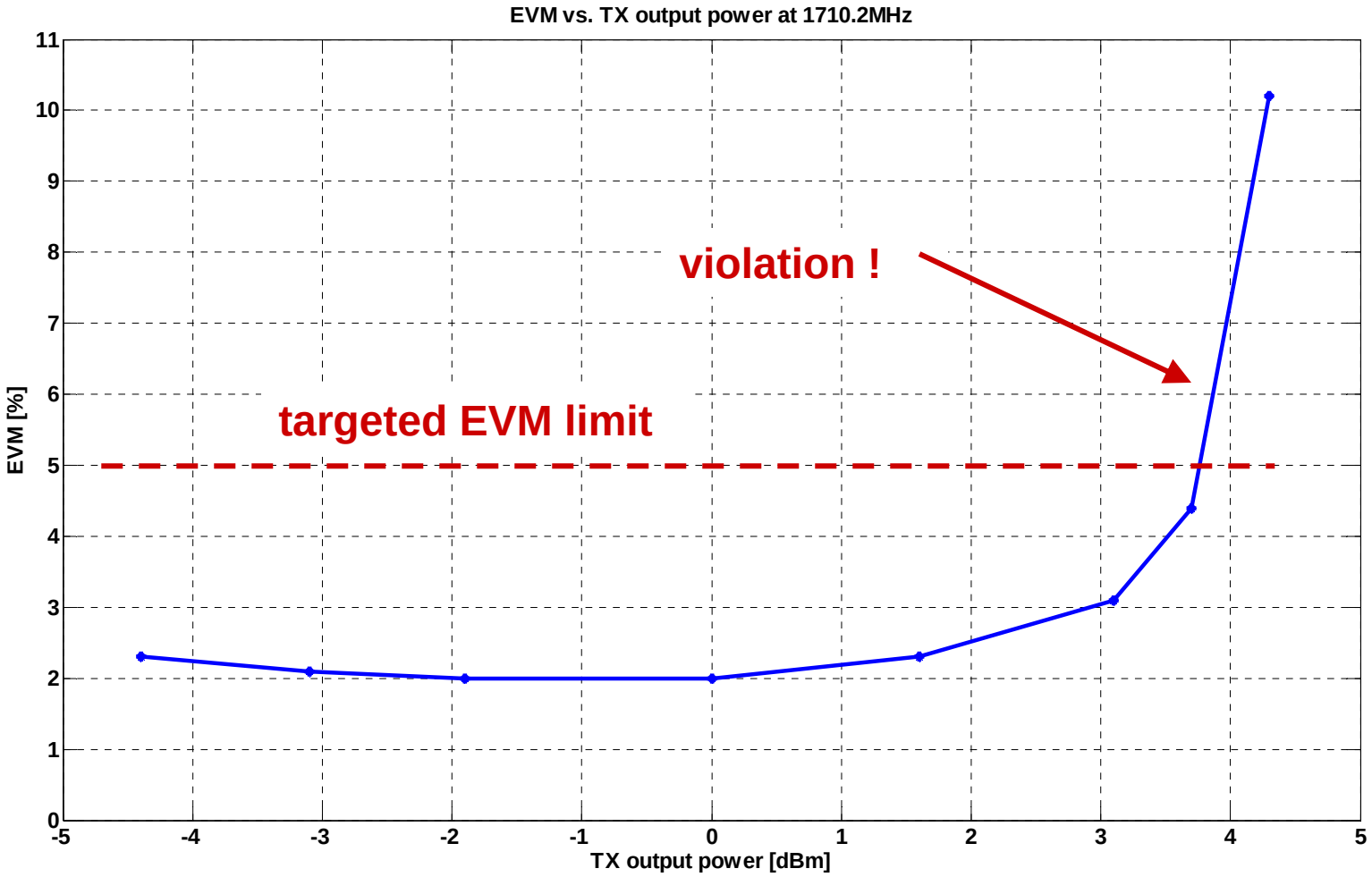
The DCO Frequency-Pulling Problem



- phase/frequency modulation distortion experienced corresponding to the amplitude modulation
  - Worsens with increased output signal level
  - Could be caused by supply fluctuations in addition to the AM RF aggressor
- the aggressor and victim are frequency-synchronous!

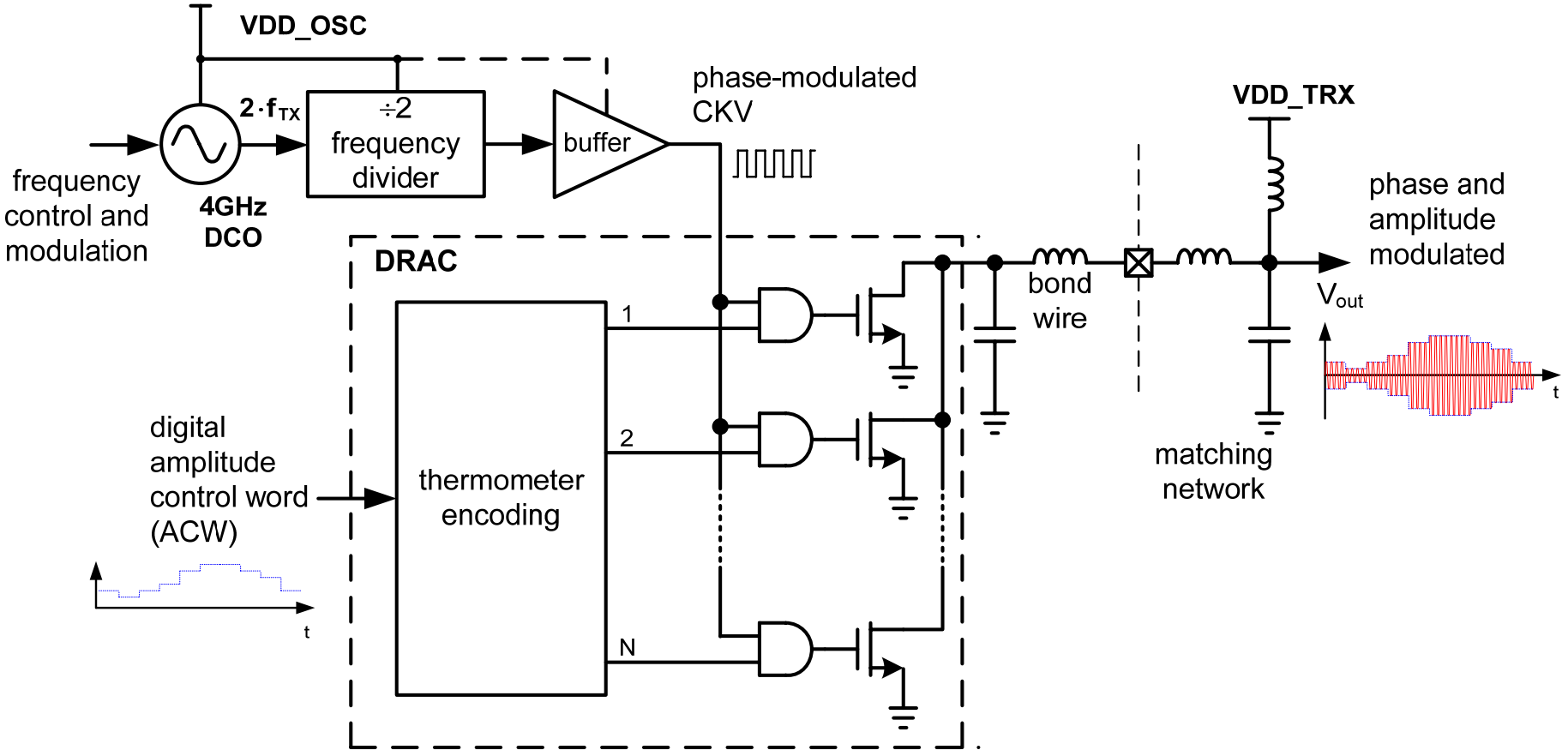
Consequences of the Interference

- EVM worsens as TX power is increased (AM aggressor is stronger)
- TX mask limits are violated due to the distortion in phase

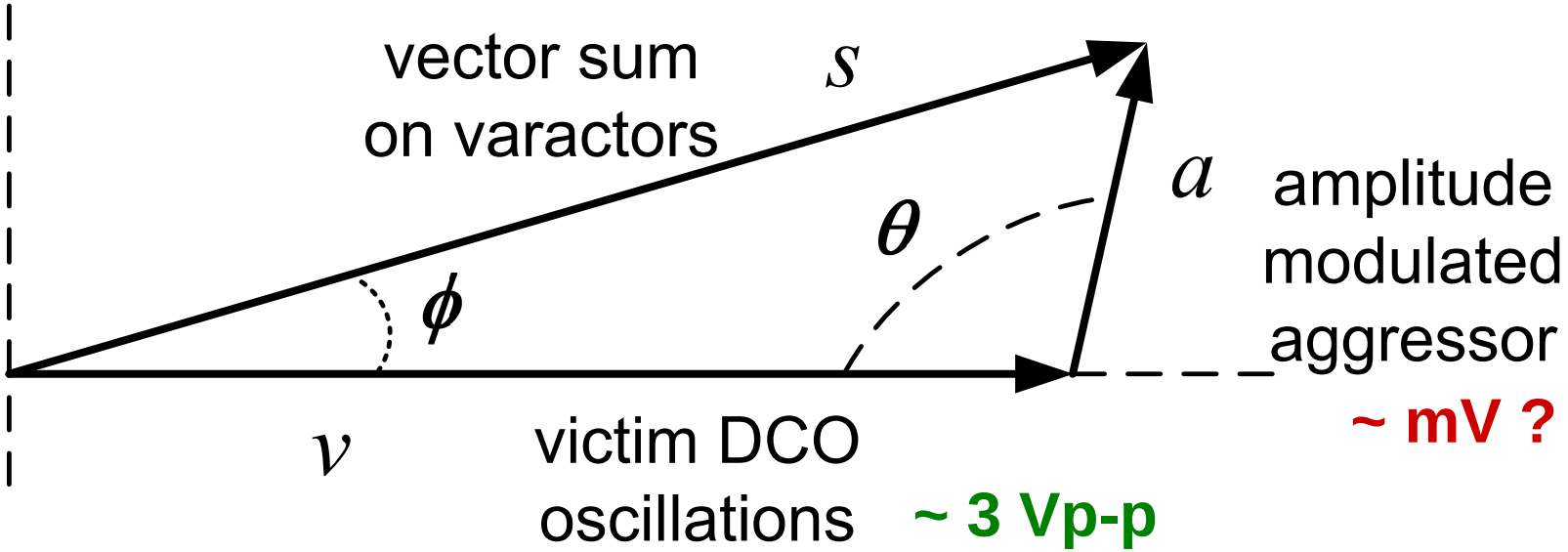


The Principle of Operation of the AM Stage

- The amplitude modulation is fully digital based on a thermometer-code unit weighted digital- to-RF-amplitude-converter (DRAC)
- The instantaneous current into the array is amplitude dependent, potentially representing an additional aggressor



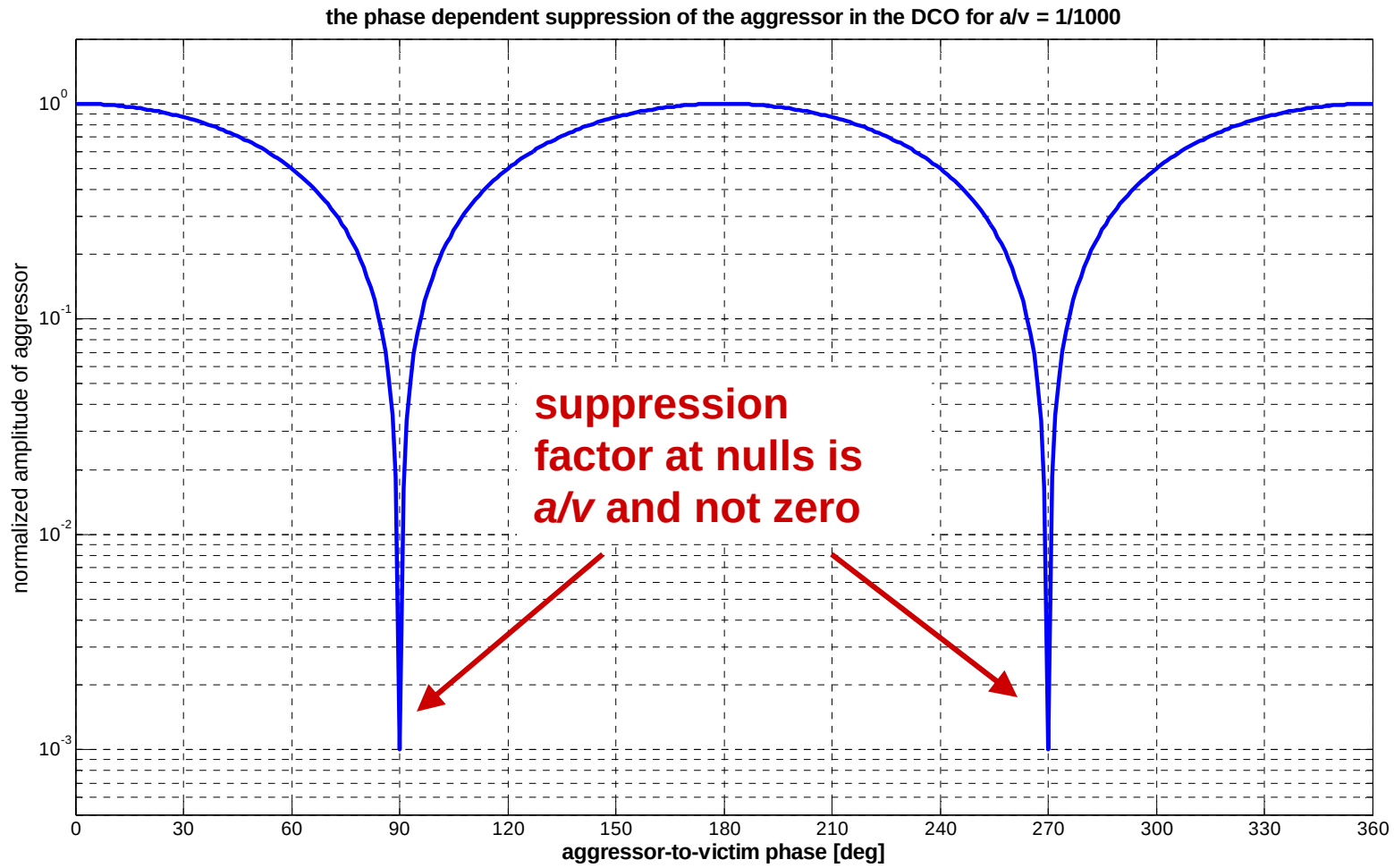
Mathematical Analysis (1/2)



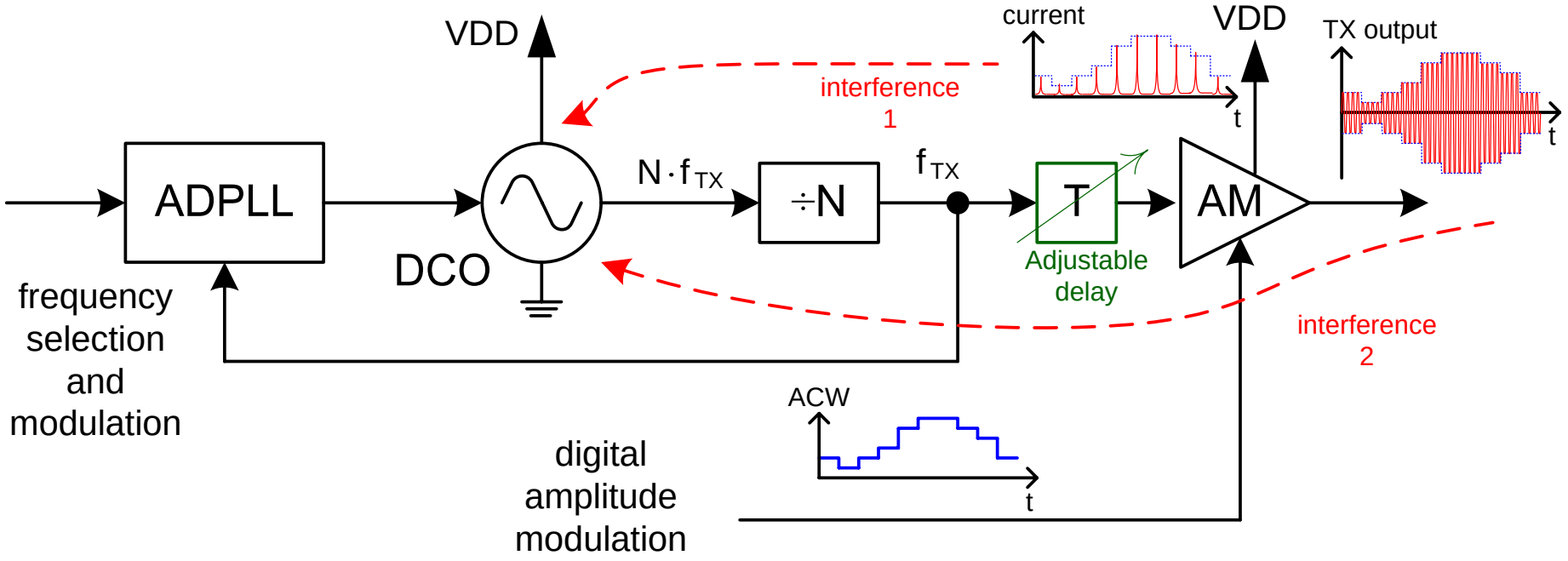
- vector sum on varactors: $s^2 = v^2 + a^2 - 2 \cdot v \cdot a \cdot Cos\,\theta$
- aggressor much weaker than victim: $v^2 >> a^2$
- phase-dependent vector sum: $s = v\sqrt{1 - 2 \cdot \frac{a}{v} \cdot Cos\,\theta}$

Mathematical Analysis (2/2)

- Phase dependency for effective interference magnitude shows 180° periodicity (the maximal suppression is achieved at orthogonality)



Proposed Phase Adjustment Implementation



- Digitally controllable delay circuit to be placed in TX path before AM stage
- Calibration/compensation to be based on internal measurements of the ADPLL PHE signal reflecting the parasitic FM suffered during AM

Summary

- The potential for self-interference is increasing
  - SoCs becoming more complex (often including multiple radios)
  - impractical to model/anticipate all the possible self-interference mechanisms in an SoC at the design stage
- A phase-domain approach for the mitigation of the impact of interference was proposed, which may be applicable in specific scenarios in an SoC.
- To minimize hardware redesign, provisions must be made to allow for digital/software-based interference mitigation at the post-silicon stage – **DfIM** (**D**esign **f**or **I**nterference **M**itigation)
  - allow margins in processing power and memory for the implementation of software algorithms to address interference problems
  - accommodate clock rate selection and dynamic spectral spreading
  - where the phase domain approach may be applicable, allow for phase/delay adjustability on potential aggressors/victims

Thank you! **OrenE@ieee.org**

Additional References (1/2)

1. **A. Hajimiri and T. Lee, "A General Theory of Phase Noise in Electrical Oscillators", *IEEE Journal of Solid State Circuits, Vol. 33, No. 2, Feb. 1998***

2. **R. B. Staszewski, C.-M. Hung, D. Leipold, et al., "A first multigigahertz digitally controlled oscillator for wireless applications," *IEEE Trans. on Microwave Theory and Techniques*, vol. 51, no. 11, pp. 2154–2164, Nov. 2003.**

3. **R. B. Staszewski, D. Leipold, K Muhammad, et al., "Digitally controlled oscillator (DCO)-based architecture for RF frequency synthesis in a deep-submicrometer CMOS process," *IEEE Trans. on Circuits and Systems II*, vol. 50, no. 11, pp. 815–828, Nov. 2003.**

4. **R. B. Staszewski, K. Muhammad, D. Leipold, et al., "All-digital TX frequency synthesizer and discrete-time receiver for Bluetooth radio in 130-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 39, iss. 12, pp. 2278–2291, Dec. 2004.**

5. **R. B. Staszewski and P. T. Balsara, "Phase-domain all-digital phase-locked loop," *IEEE Trans. on Circuits and Systems II*, vol. 52, no. 3, pp. 159–163, Mar. 2005.**

Additional References (2/2)

6. **R. B. Staszewski, C.-M. Hung, N. Barton, M.-C. Lee, and D. Leipold, "A digitally-controlled oscillator in a 90 nm digital CMOS process for mobile phones," IEEE Journal of Solid-State Circuits, vol. 40, no. 11, pp. 2203–2211, Nov. 2005.**

7. **R. B. Staszewski, J. Wallberg, S. Rezeq, et al., "All-digital PLL and transmitter for mobile phones," IEEE Journal of Solid-State Circuits, vol. 40, iss. 12, pp. 2469–2482, Dec. 2005.**

8. **R. B. Staszewski and P. T. Balsara, "All-Digital Frequency Synthesizer in Deep-Submicron CMOS," New Jersey: John Wiley & Sons, 2006.**

9. **O. Eliezer, I. Bashir, R. B. Staszewski and P. T. Balsara "Built-in Self Testing of a DRP-Based GSM Transmitter", RFIC 2007 RMO4D-2, June 2007**

10. **I. Bashir, Robert Bogdan Staszewski, and Oren Eliezer, "Tuning Word Retiming of a Digitally-Controlled Oscillator Using RF Built-In Self Test", Proceedings of IEEE DCAS 2006**

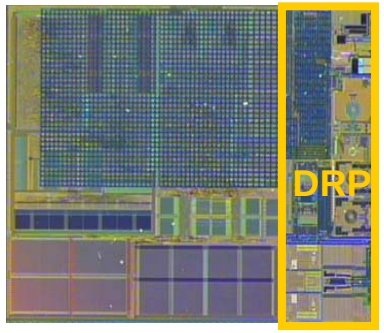
11. **S. Bronckers, G. Vandersteen, L. De Locht, Van Der Plas, G. and Y. Rolain, "Study of the different coupling mechanisms between a 4 GHz PPA and a 5-7 GHz LC-VCO," in 2008 IEEE Radio Frequency Integrated Circuits Symposium, RFIC 2008, 2008, pp. 475-478.**

Background

The DRP Transmitter

Definition/Fundamentals of DRP

- DRP = **D**igital **R**F **P**rocessor
- Radio circuitry suitable for CMOS process of logic/DSP
- Extensive use of digital circuitry to allow integration with digital processor (typically the baseband processor in cellphones) in a single low-cost digital CMOS die (SoC)

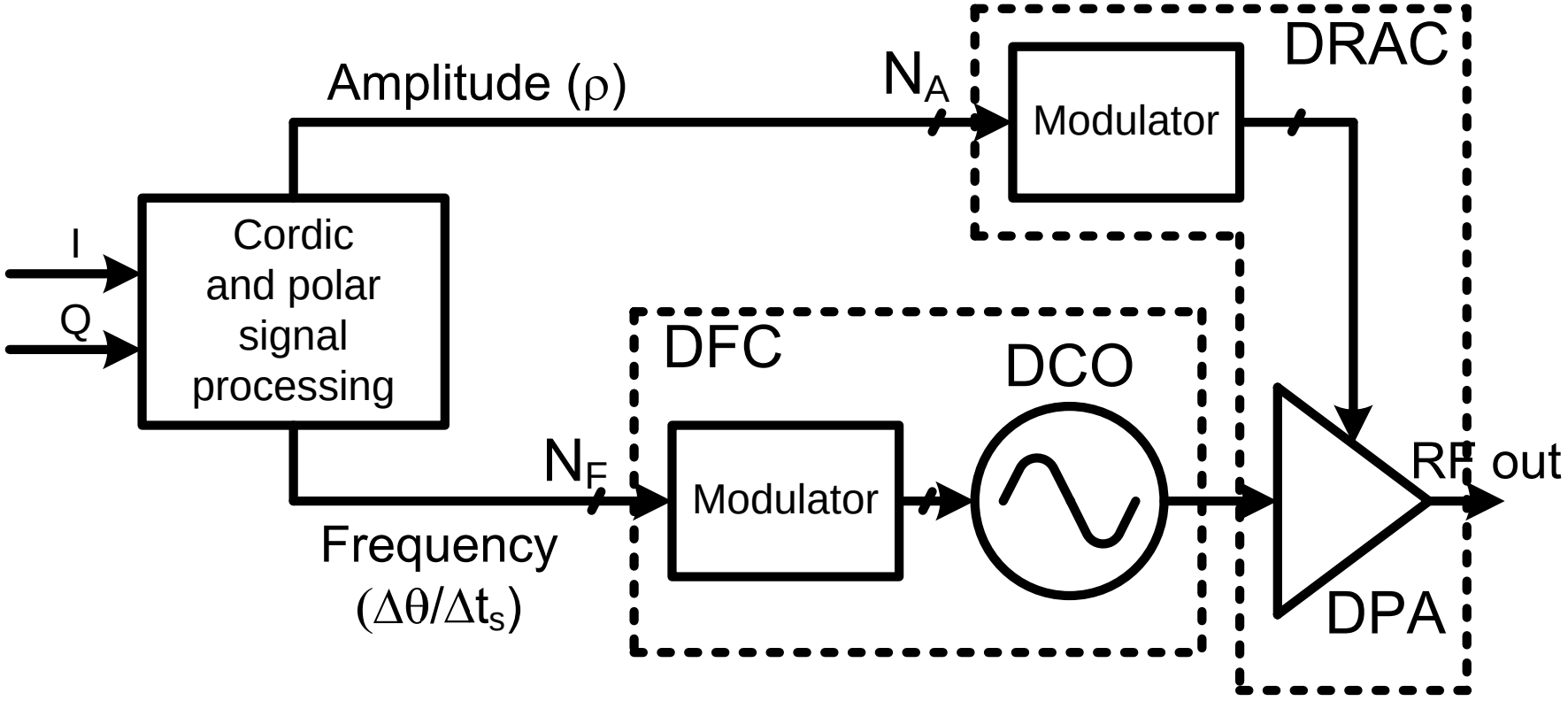


TI's single-chip GSM radio 'Locosto'

- Minimization of the use of problematic analog circuitry
  - does not migrate easily from one process node to the next
  - suffers variances in performance in massproduction
  - problematic and more expensive testing
- Digital design simplifies migration and ensures SoC scalability
- Digital/software compensation for analog impairments

All-Digital Polar TX Architecture

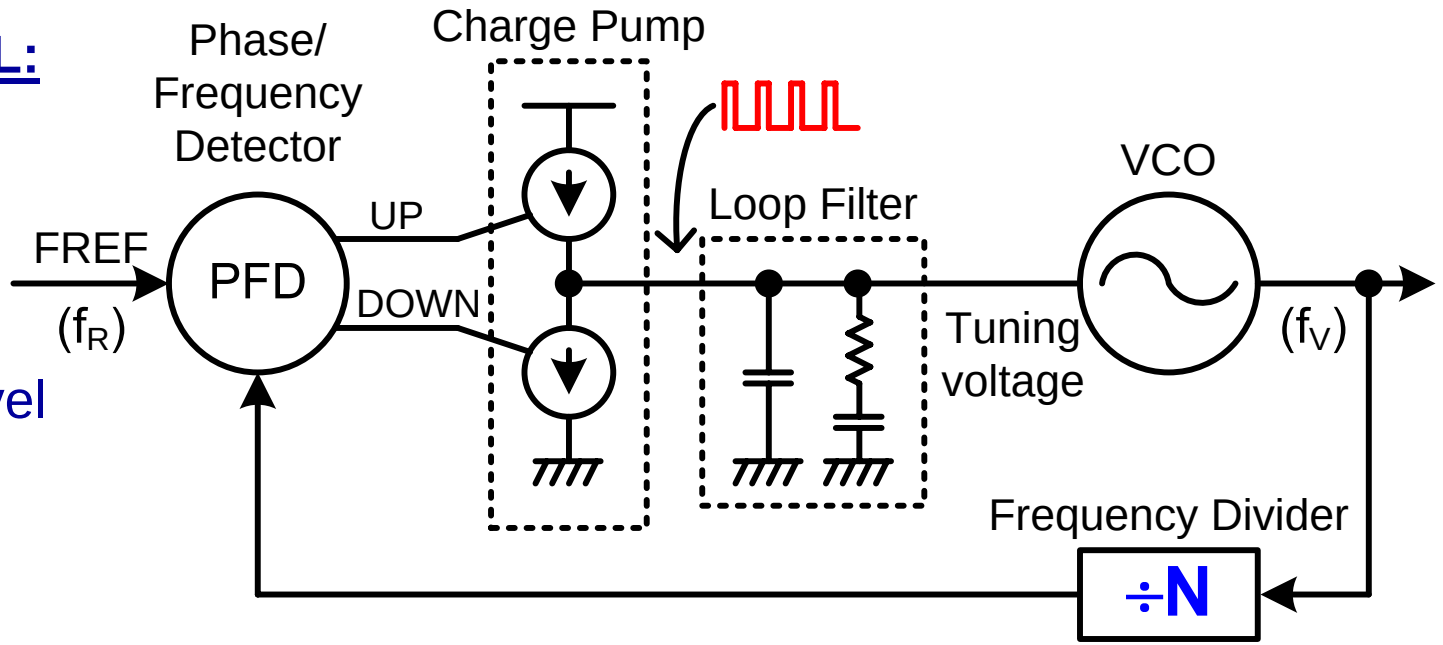
- **Supports constant and non-constant envelope modulation**
- **DCO within ADPLL for digital-to-frequency conversion**
- **DRAC for digital-to-RF-amplitude conversion**
- **Standards addressed: GSM/EDGE, Bluetooth (GFSK, DQPSK)**



All-Digital vs. Conventional PLL

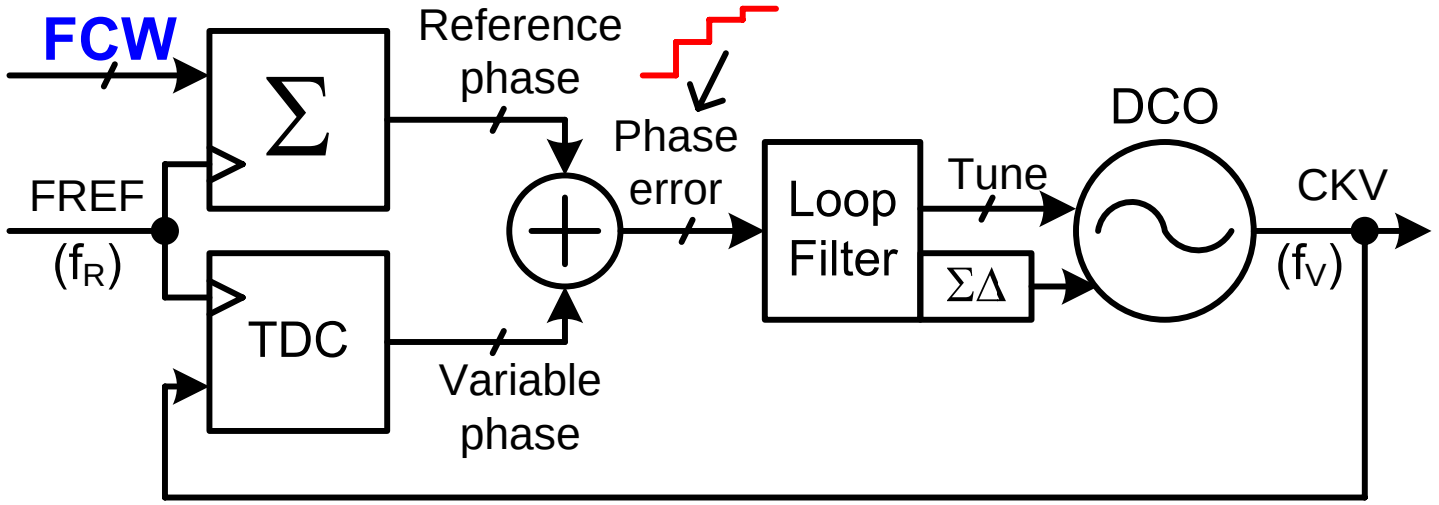
Charge-pump PLL:

- Suffers from f_R spurs
- Tradeoff: bandwidth against spur level
- Requires large capacitors



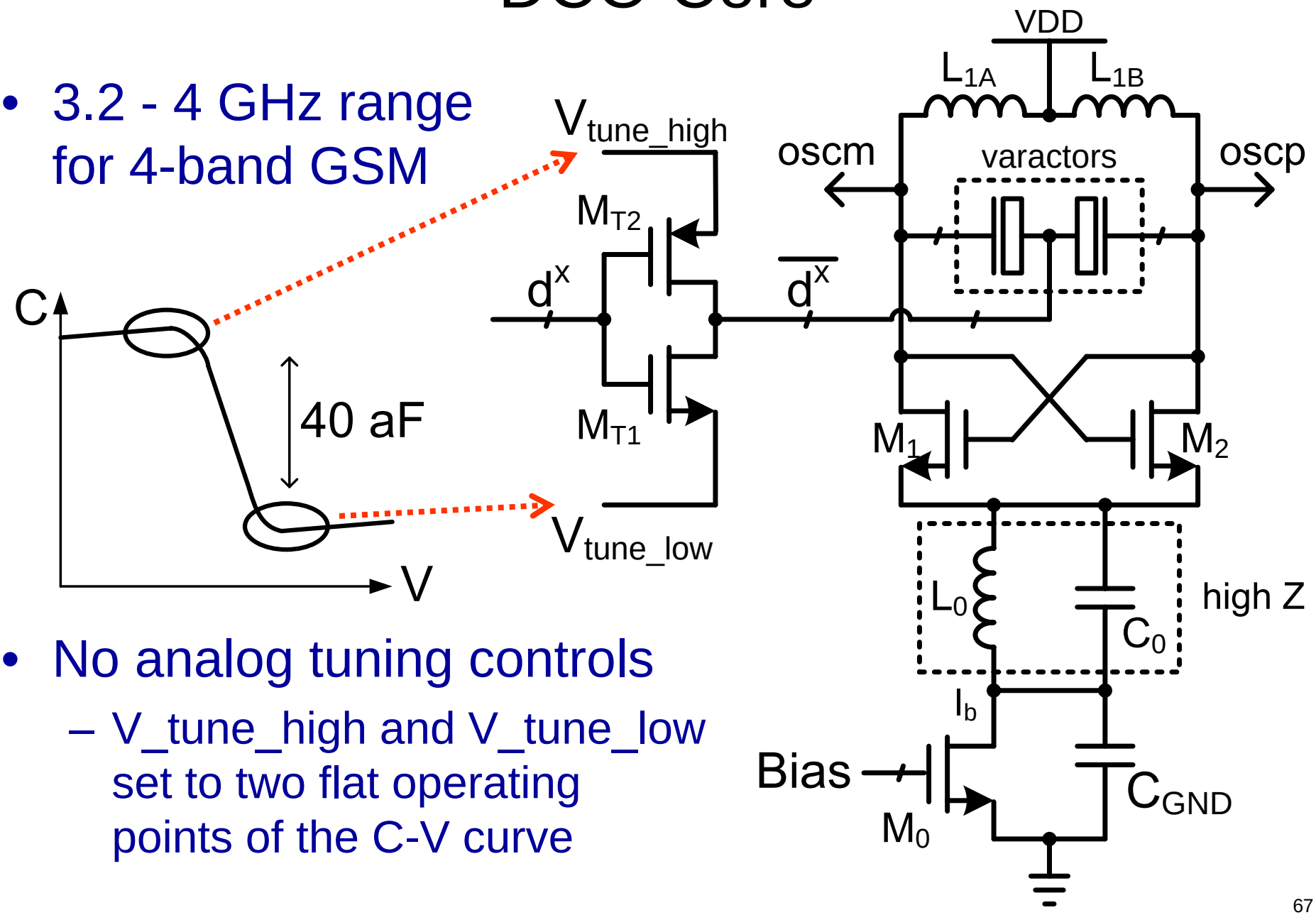
All-digital PLL:

- True phase domain operation
- Digital signal processing
- Noise immunity
- Configurable



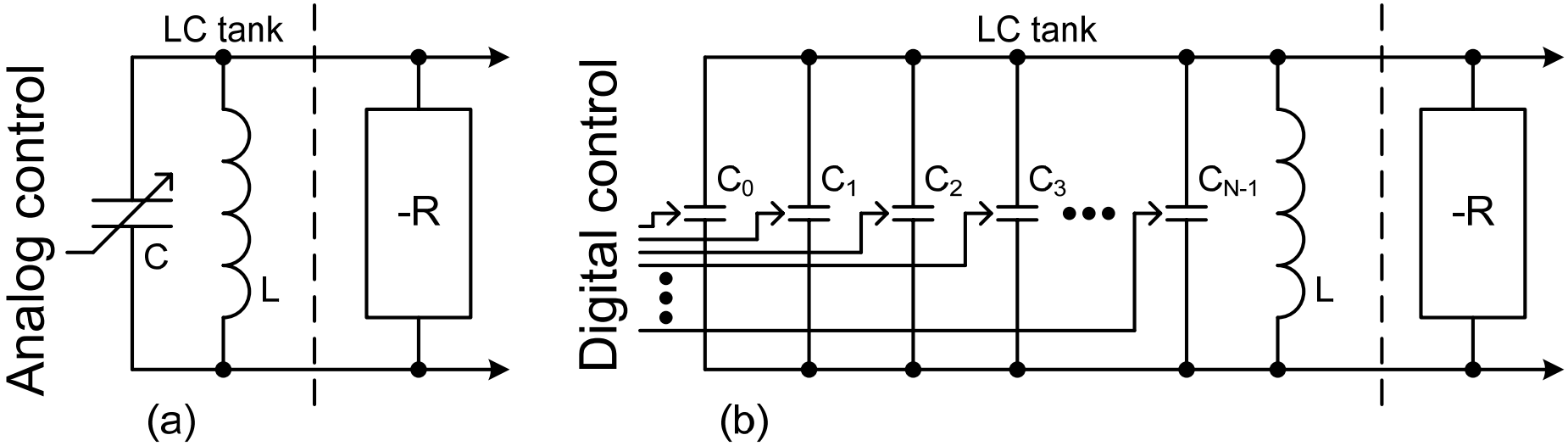
DCO Core

- 3.2 - 4 GHz range for 4-band GSM
- No analog tuning controls
  - V_tune_high and V_tune_low set to two flat operating points of the C-V curve



Digitally Controlled Oscillator (DCO)

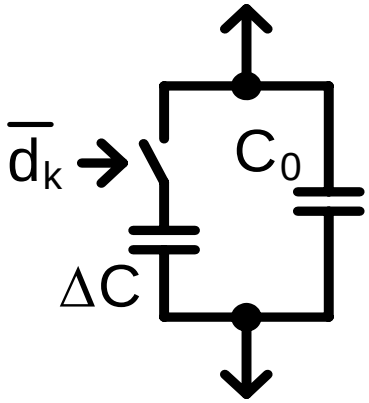
- Linear varactor of conventional VCO replaced with a large number of tiny binary-controlled varactors in a digitally-controlled oscillator (DCO)
  - Smallest varactor size: tens of atto-Farad (aF=10^{-18}F)
- The loop operation is fully digital including the frequency tuning

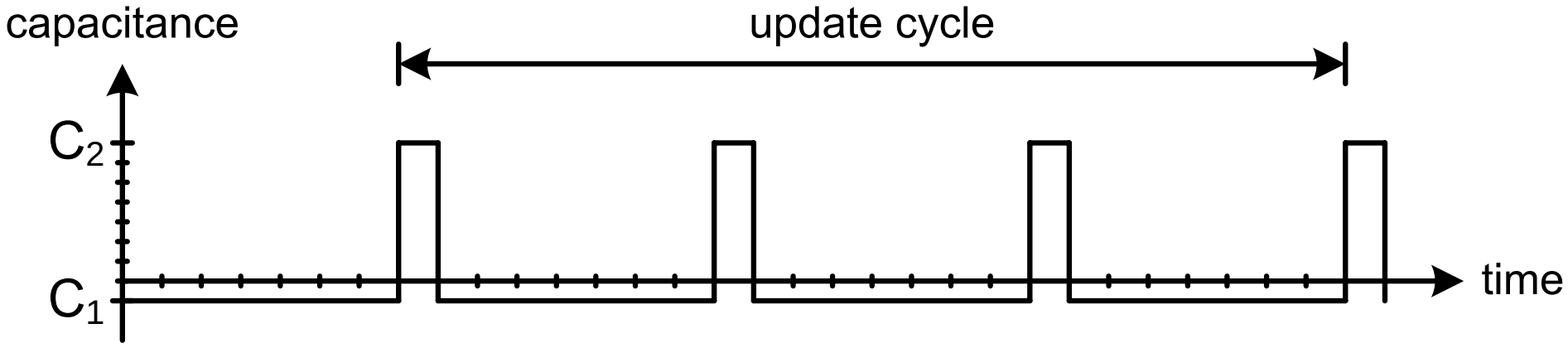


DCO Varactor Dithering Principle

- Frequency resolution enhanced by high-speed dithering of the smallest size varactor
- Sigma-delta dithering rate derived from DCO and therefore frequency synchronous with it (e.g. through divide by 4/8/16…)

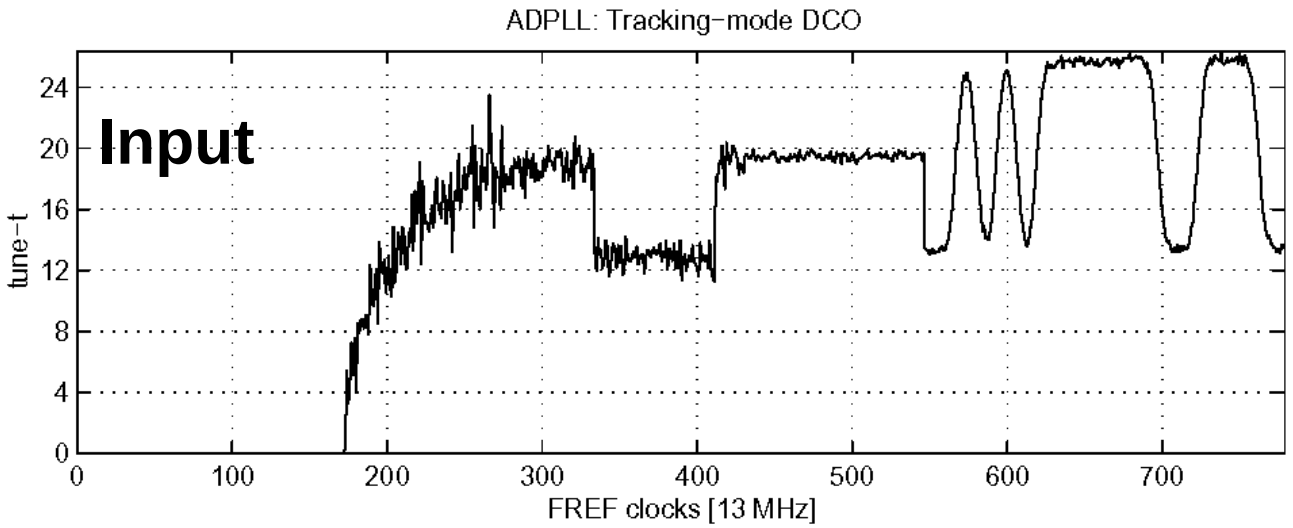
Varactor model:



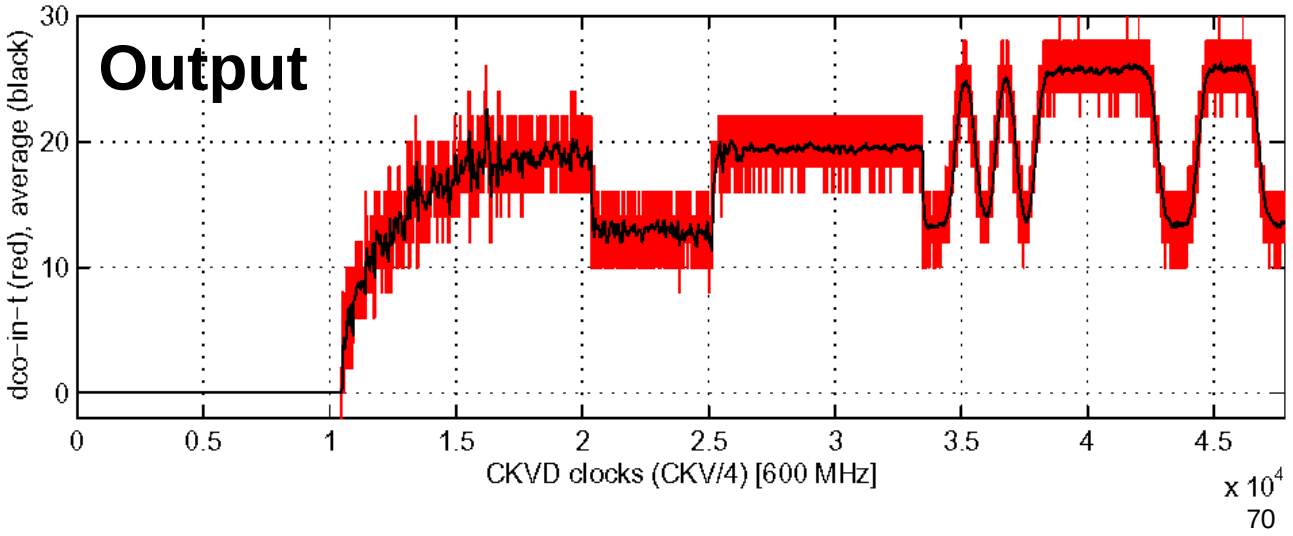


Simulation Example of ΣΔ DCO Dither

- Fixed-point DCO tuning word

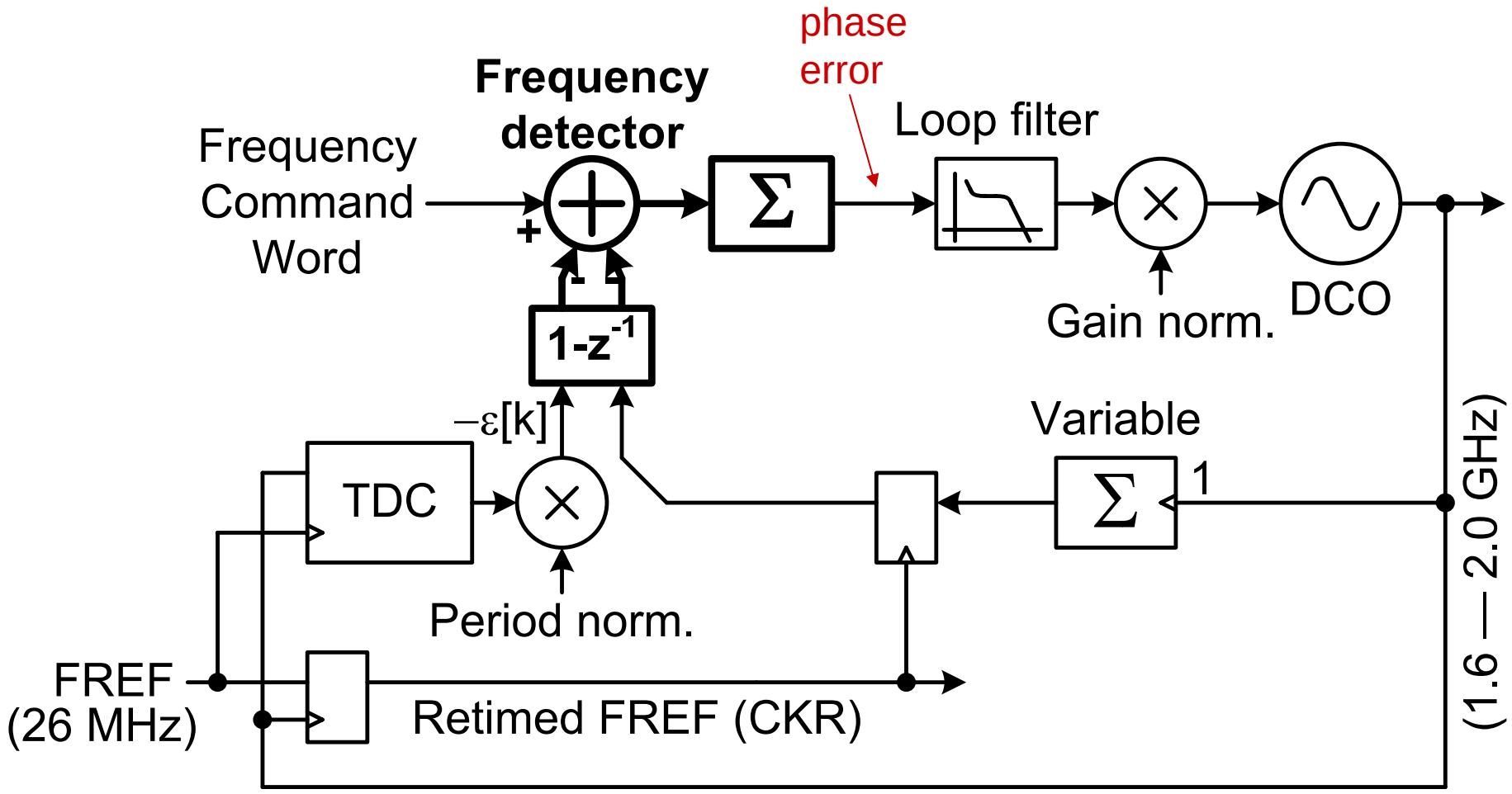


- **Red**: Integer DCO input word
- **Black**: running average



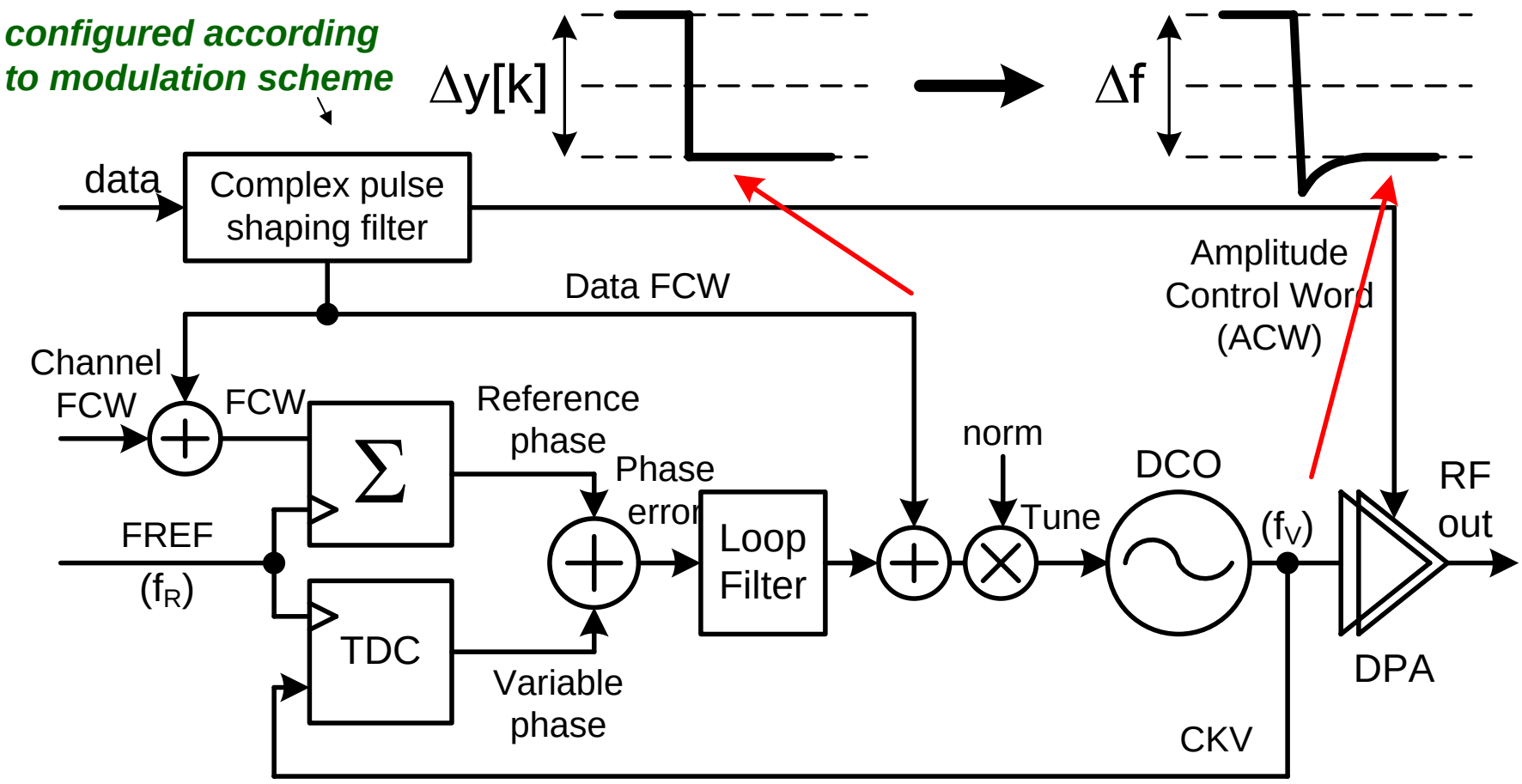
Frequency Detector Based ADPLL

- Phase error is an accumulated frequency error
- Insensitive to arbitrary phase-bias between input and output



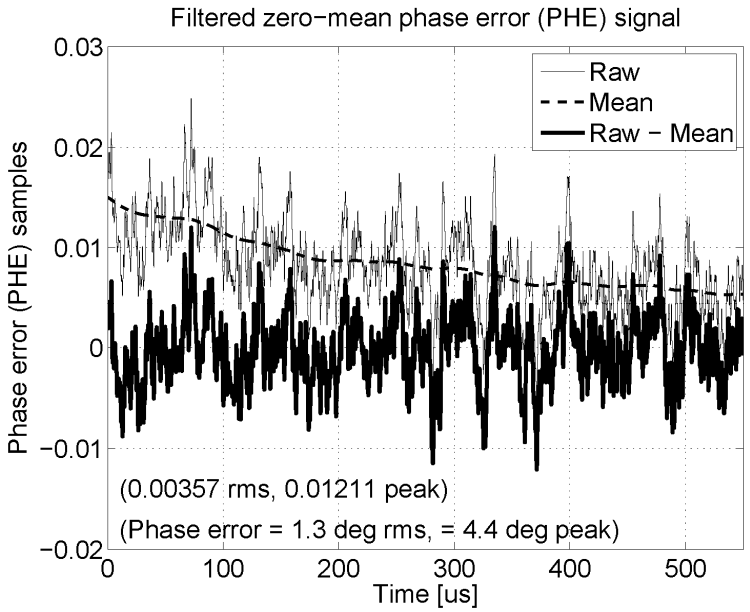
ADPLL with Wideband Modulation

- Two-point frequency modulation
  - Direct feedforward path – y[k] directly drives the DCO
  - Compensating path – y[k] added to the channel frequency control word

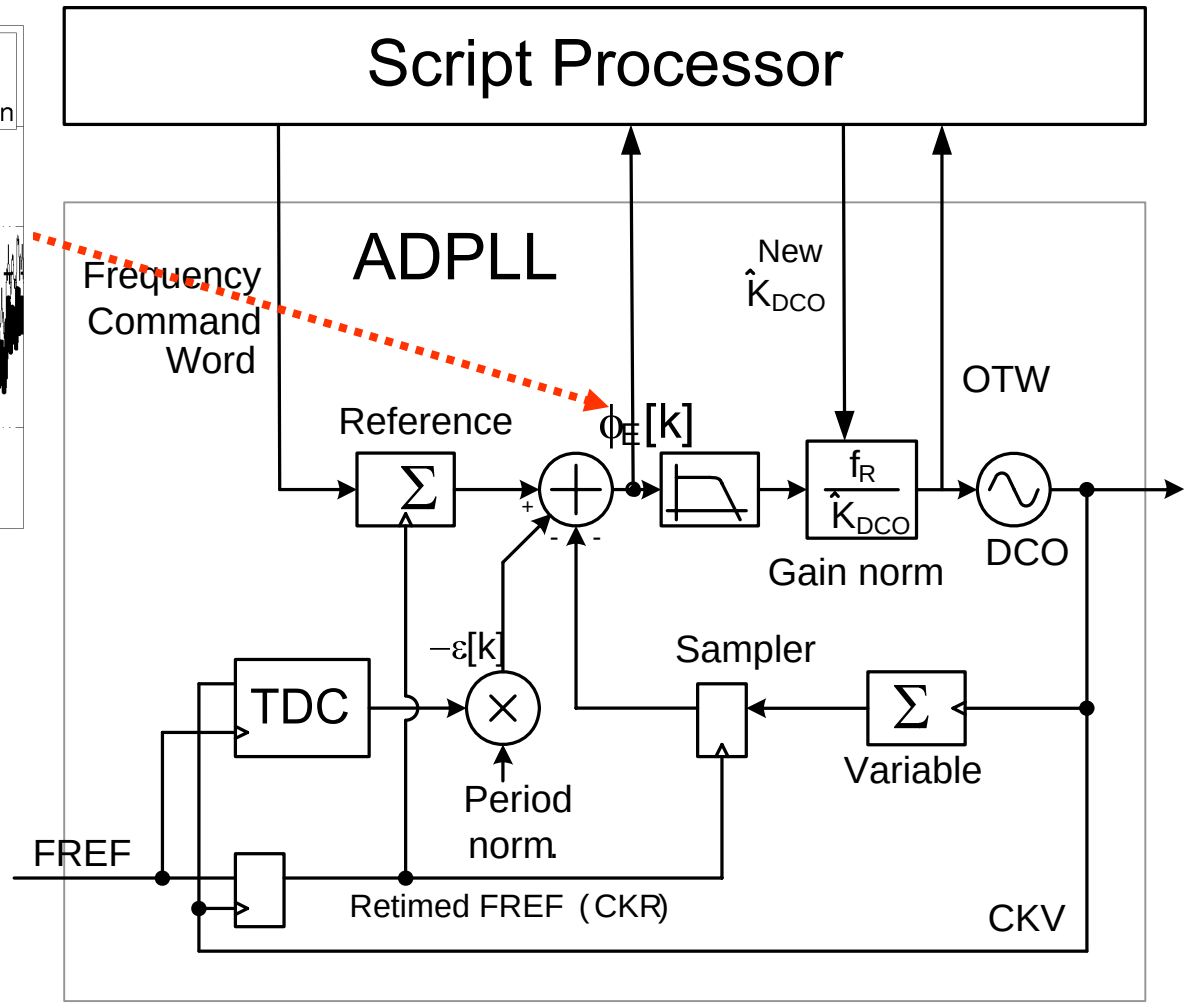


Inherent Built-in Self Test Capability

- Digital processing of phase error is useful in determining DCO noise performance (natural noise and interference)

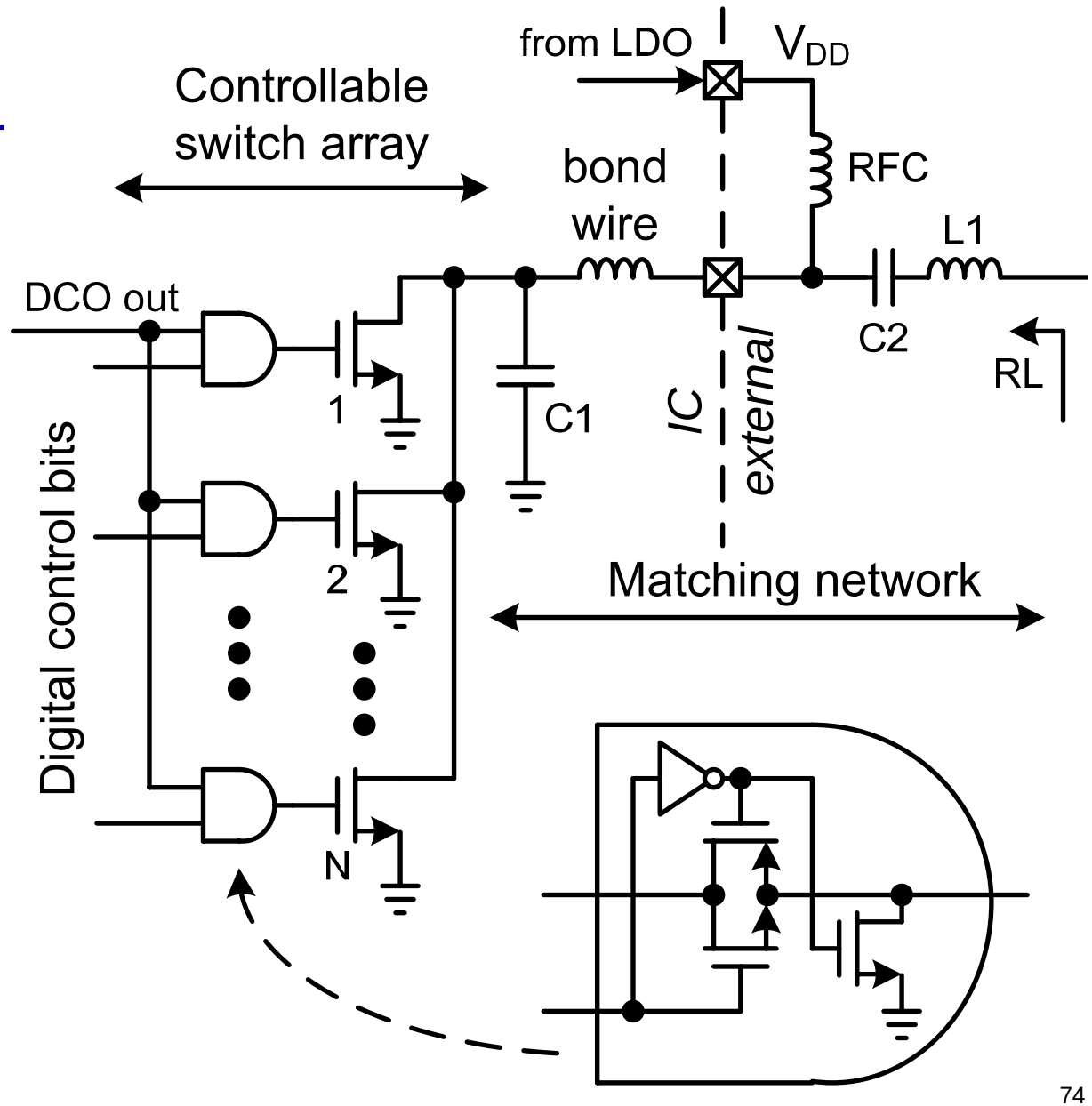


- Processing of phase error also useful for testing of DCO capacitances (RFIC '07 RMO4D-2)



Digitally-Controlled Power Amplifier

- Digital to RF amplitude converter (DRAC) - RFIC '05
- Array of unit-weighted MOS switches
- Each switch contributes a conductance
- Resolution enhanced through $\Sigma\Delta$ modulation

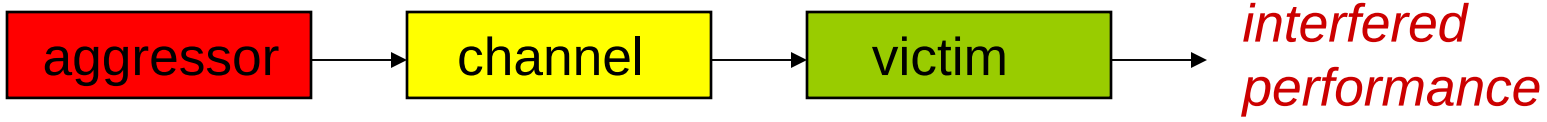


Background

Fundamentals of Interference and Coexistence

Basic Interference Terminology

- Interference mechanisms involve at least one *aggressor*, one *victim* and one coupling/propagation *channel/medium* allowing the aggressing signal to arrive at the victim circuit.
- The *channel/medium* may or may not be parasitic, but must be modeled/estimated sufficiently accurately to determine the level of interference suffered. Typically, it isn't and the interference mechanism is discovered only post-silicon in the lab…
- The consequences of interference may be:
  - Complete malfunctioning (always intolerable)
  - Performance degradation (possibly tolerable)
  - Regulation/standard violation (intolerable but not always noticeable)



Interference Mitigation Approaches (1/2)

(implemented in the victim circuitry)

1. **Suppression of interference within the victim circuitry**
   - Shielding the victim to suppress the level of the arriving aggressor
   - Filtering to suppress arriving aggressing signal
2. **Passive mitigation of interference effects within the victim**
   - Robust biasing (current consumption penalty?)
   - Differential topologies
3. **Active mitigation of interference effects within the victim**
   - Active cancellation of the interfering signal
   - Dithering of threshold in slicing circuits

Interference Mitigation Approaches (2/2)

4. **Reduction in interference power**
   - Proper routing to reduce I·R drop
   - Filtering/shaping of clocks/data (reducing power in specific bands)
5. **Avoidance in frequency domain**
   - Wise/dynamic selection of clock rates to avoid victim sensitivities
   - Spectral spreading of clock/data signals
6. **Avoidance in time domain**
   - Schedule aggressing activity to avoid sensitive instances in victim
   - Shift timing of victim activity to instances clear of interference
7. **Avoidance in phase**
   - Adjust phase of victim signal to minimize its vulnerability to aggressor
   - *Adjust phase of aggressing signal to minimize its impact on victim*