Two Zero Two Pole Active Compensation Replaces a Charge Pump and Regulator in PLLs 6-25-08

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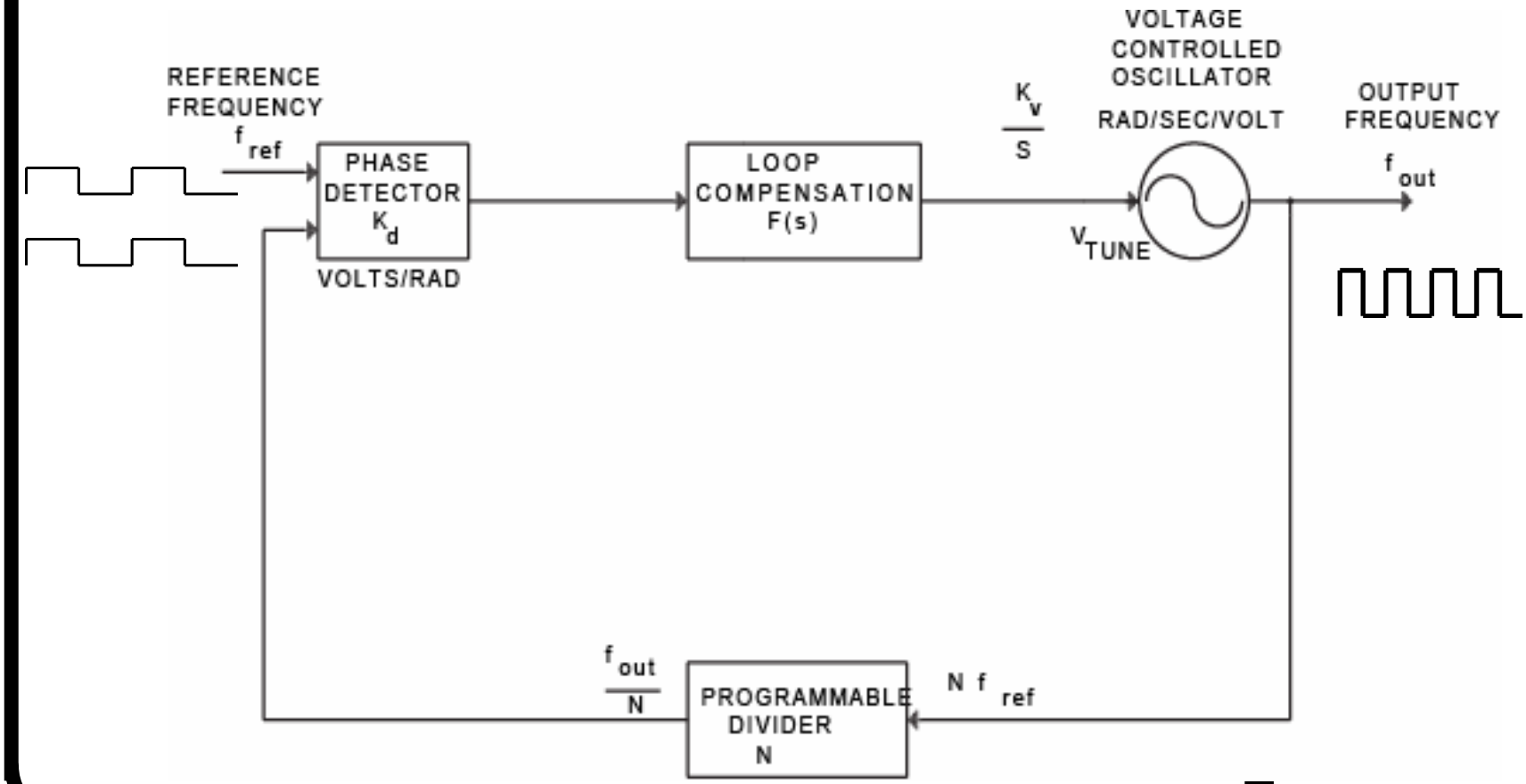
Agenda

- PLL Review
- Various Loop Filters
- 2 Zero 2 Pole Plots and Equations
- 2 Zero 2 Pole Results

PLL Basic Block Diagram

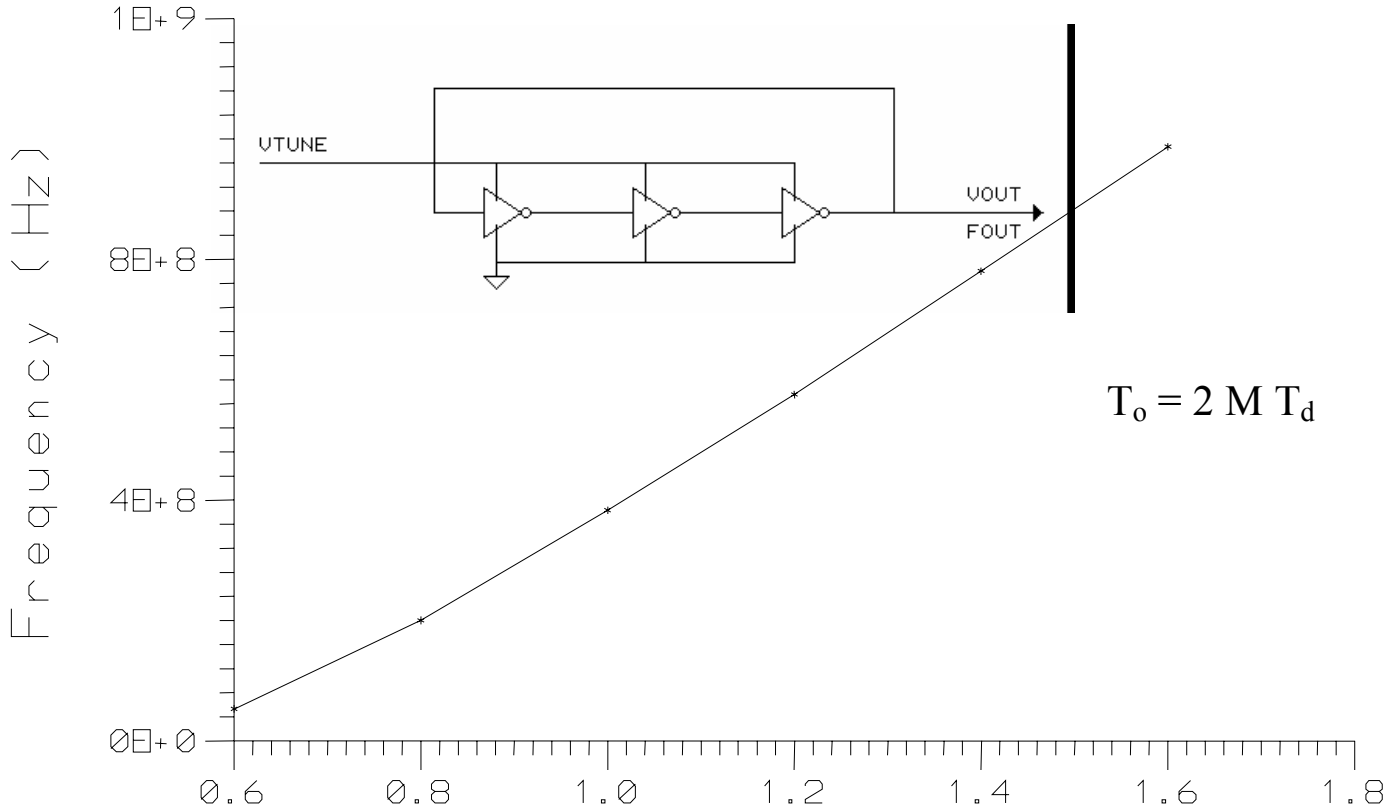
Input Phase Transduced to Voltage and Voltage Transduced to Output Phase



Ideal VCO Transfer Function, Transduces Voltage to Frequency (Edges)

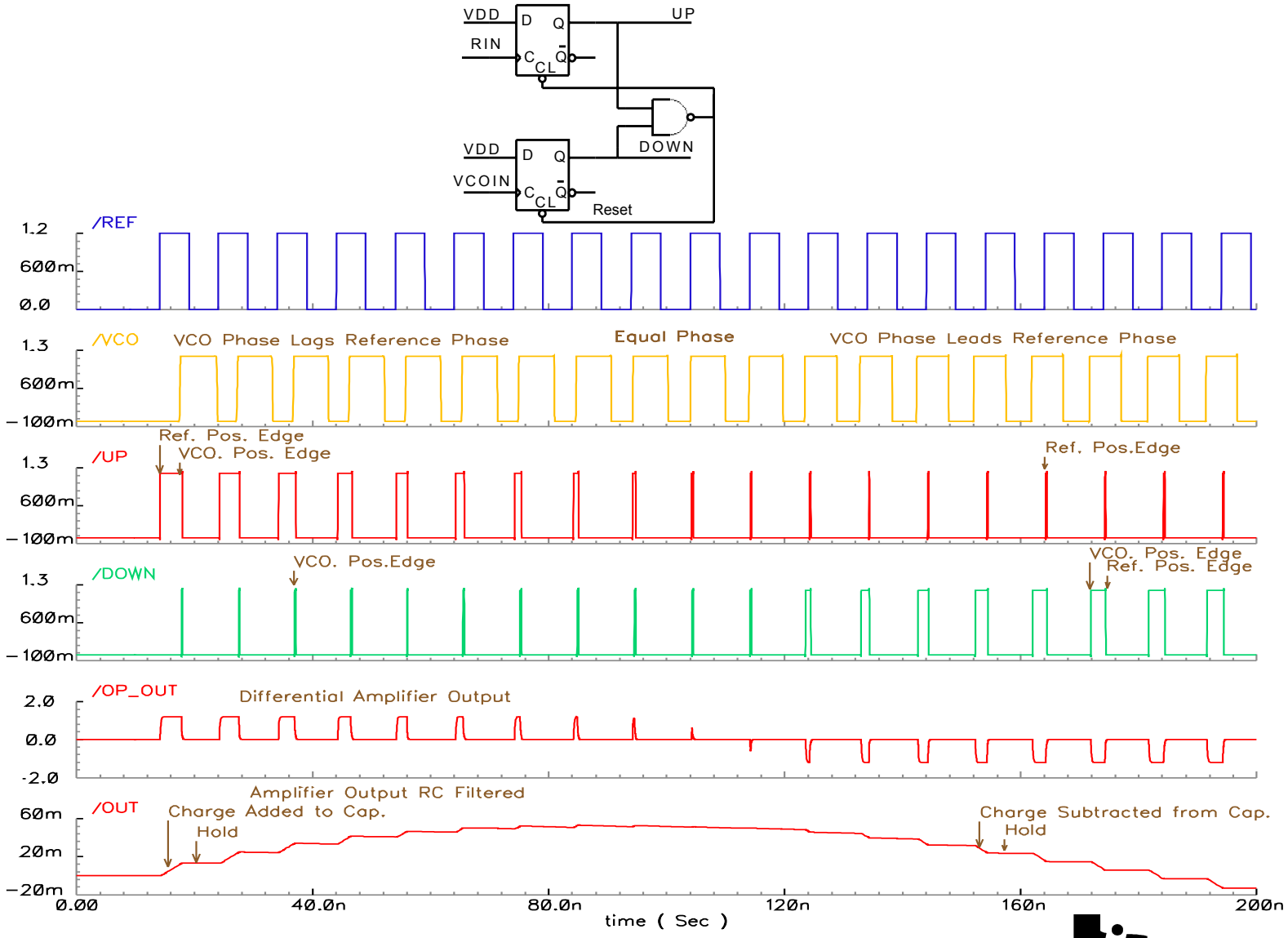
$\omega_{out}=\omega_{off}+K_v V_{tune}$

$\omega_{out}=\Delta\theta_{out}/\Delta t$



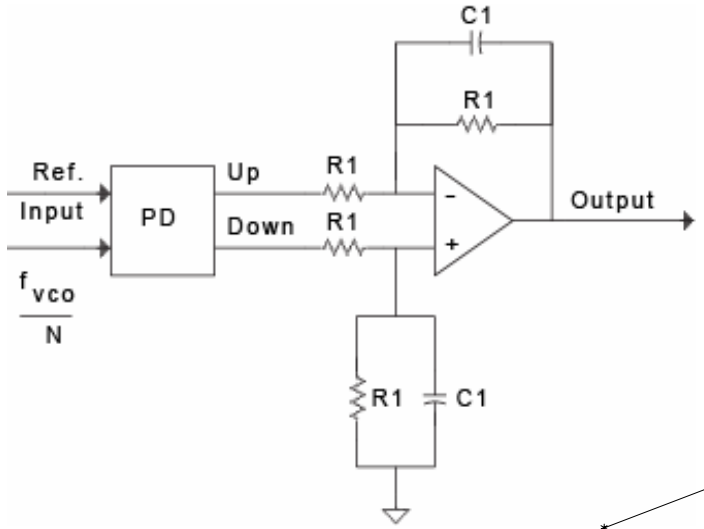
$T_o = 2\ M\ T_d$

Digital Phase Detector Timing and Response to Ramped VCO Phase

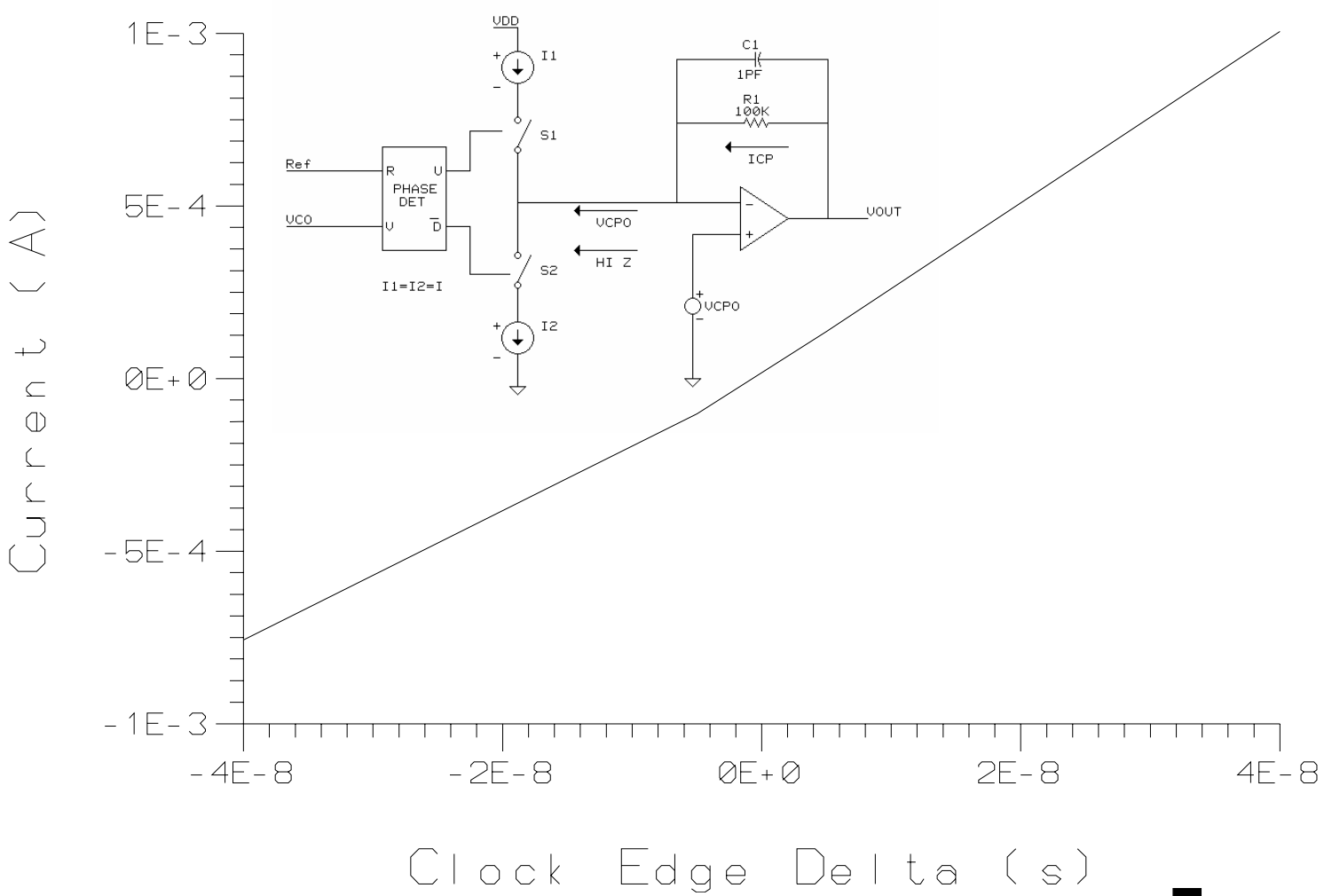


Ideal Phase Detector Transfer Function, Transduces Frequency (Edge) Differences to Voltage

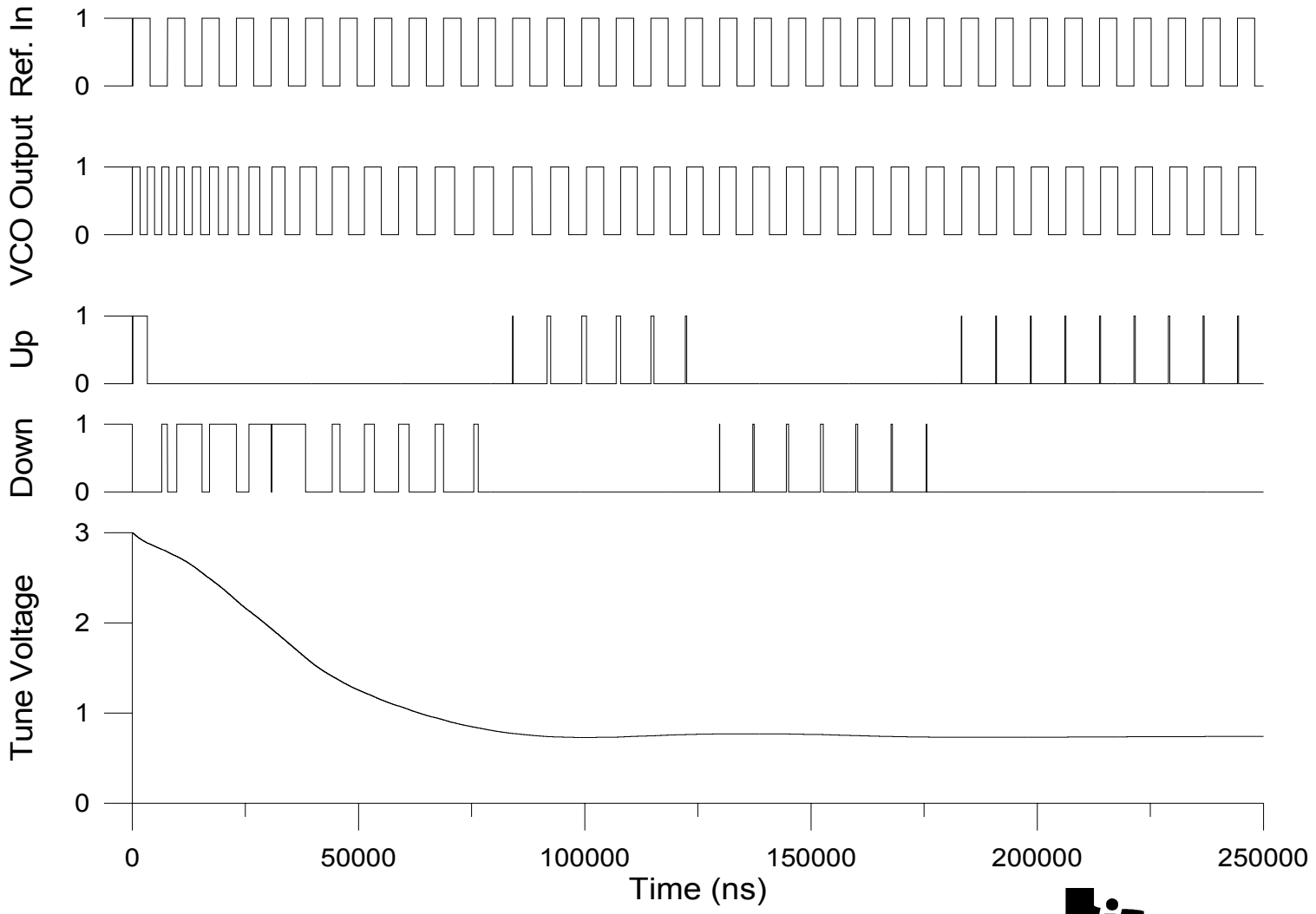
$Vpd_{avg}=K_d\ \theta_e$ (5MHz Ref. Freq.)



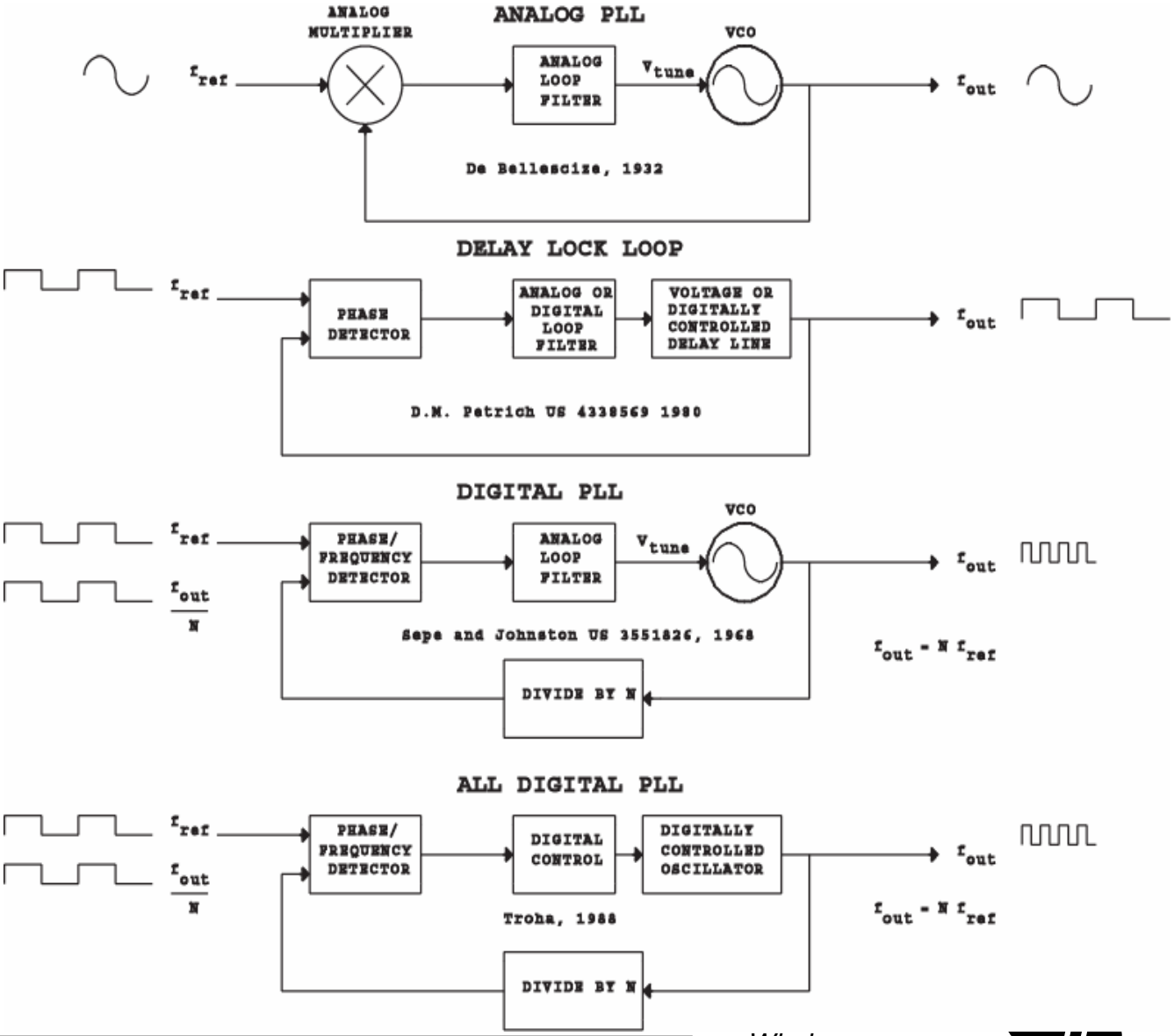
Charge Pump Output Transduces Frequency (Edge) Differences to Current, Kp=I/(2 π)



Example of Lock, Digital Loop
(In Phase)



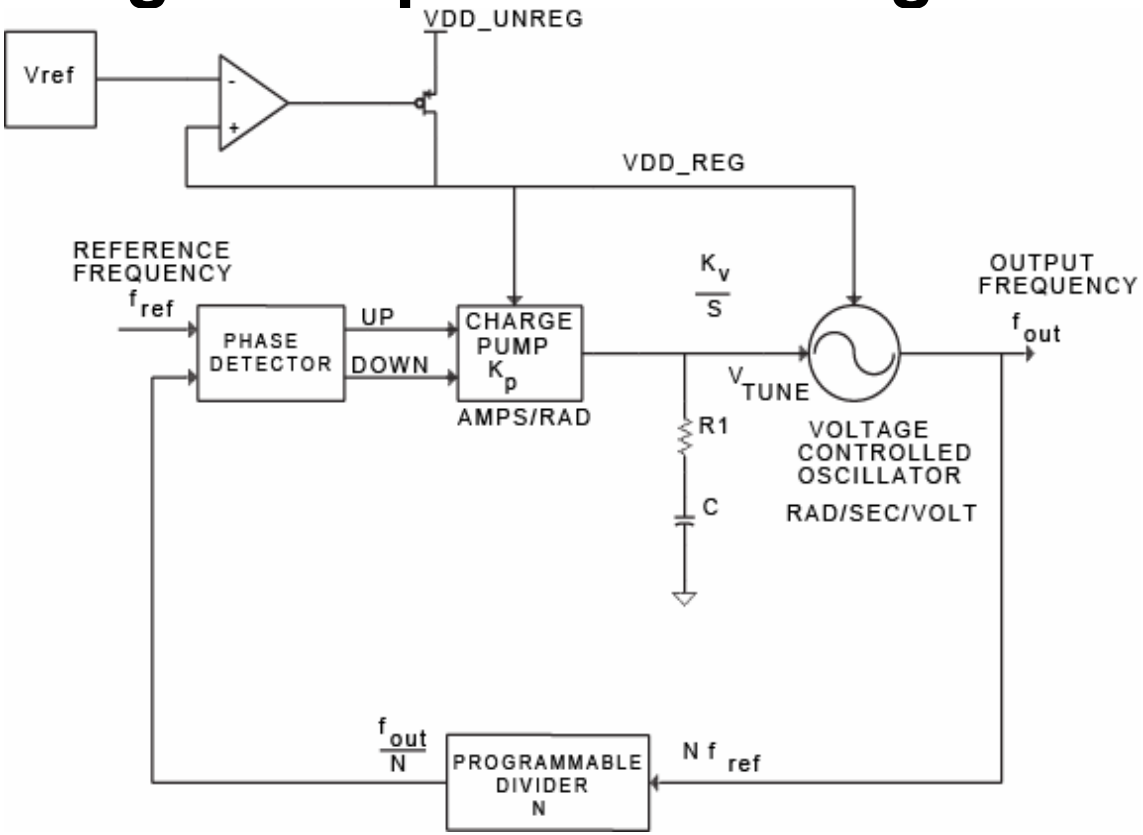
Loop Classifications



Comparison of PLL Loop Filters with Regulators driving VCO

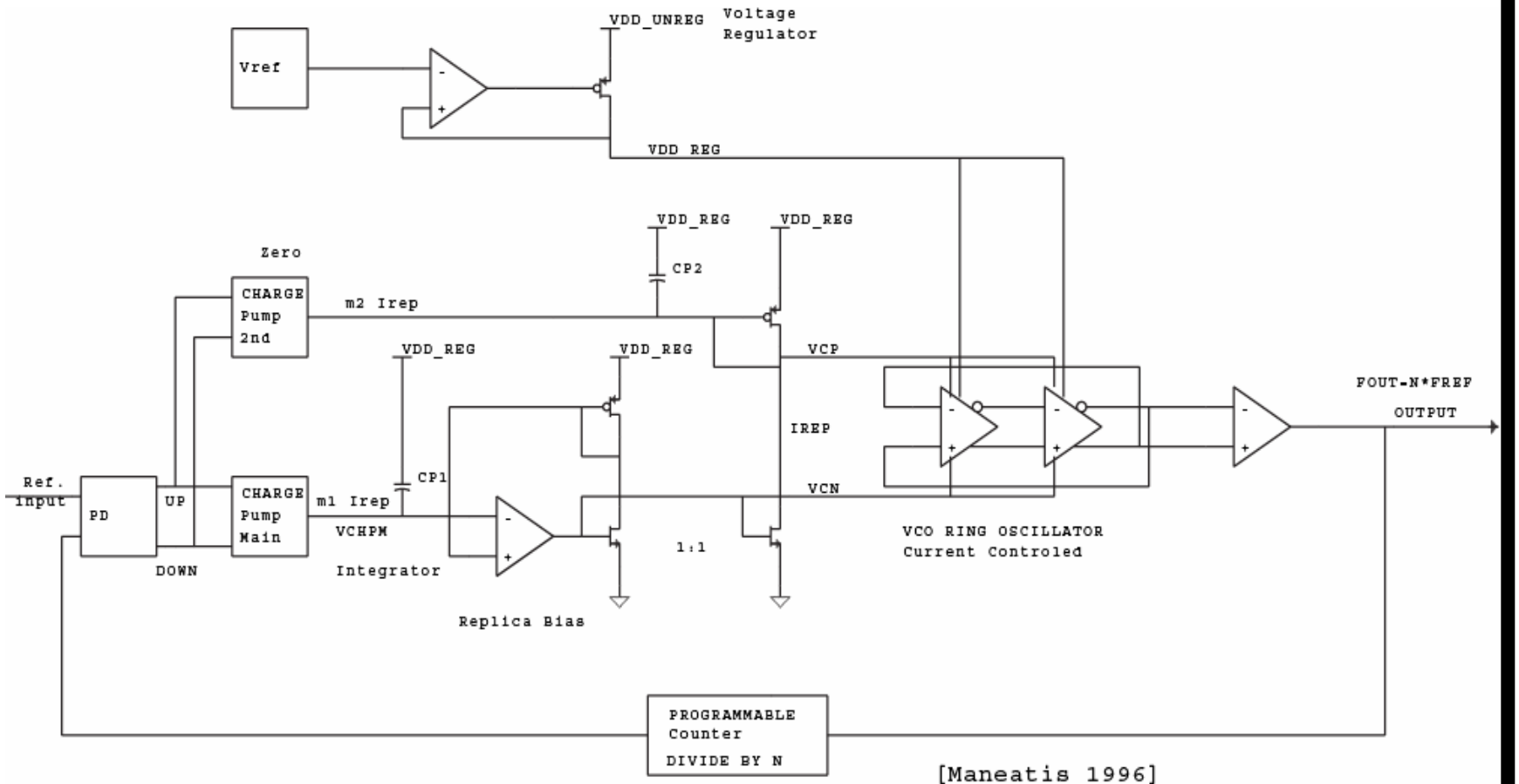
- Charge pump PLL
- Replica Bias PLL
- Digital PLL
- 1 Zero Active PLL

Charge Pump PLL with Regulator



- Charge pump can not drive high current load
- 1 pin for external components

Replica Biased Charge Pump PLL

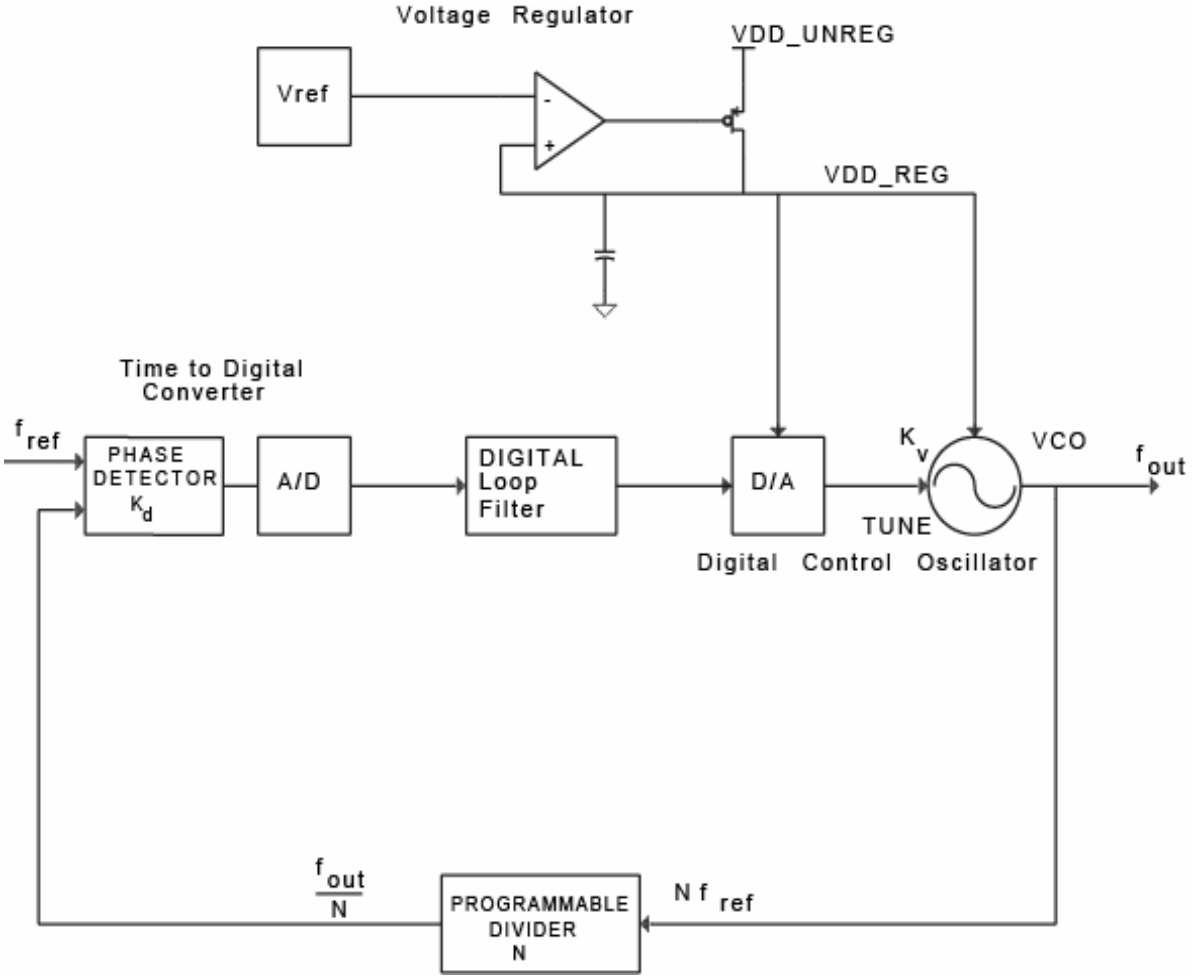


[Maneatis 1996]

Advantages/Disadvantages

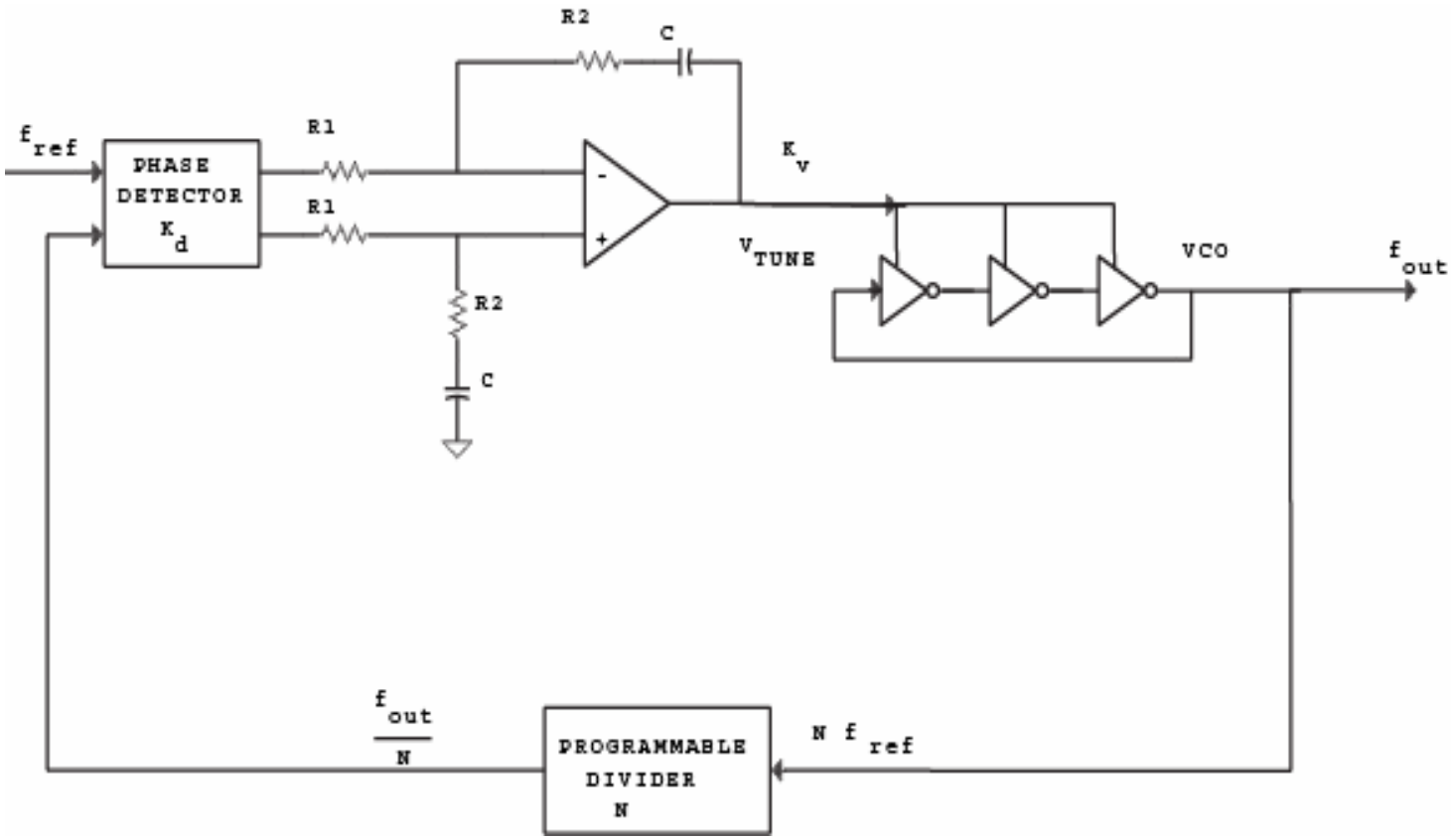
- **Widely used for many years and many designs**
- **High sensitivity to power supply at regulator output**
- **Narrow frequency tuning range (~200mV for nano scaled devices)**
- **Low output voltage swing to differential to single ended converter (50mVpp)**
- **Narrow output voltage range for charge pump (~200mV for nano scaled devices)**
- **Differential ring stops oscillating**

All Digital PLL with Regulator



- **Sensitivity to power supply**
- **Not state of the art performance in power, area, and noise? trade offs**
- **Leakage does not change frequency**

1 Zero Active Compensation



1 Zero, Type 2 Second Order Open Loop Gain Function (Active Filter)

Cascade of Transfer functions for Open Loop Gain

G(s)H(s)= (Phase Detector Gain)(Filter Transfer Function) (VCO Transfer Function)(Divider Transfer Function)

Substitute and Rearrange for Open Loop Gain Expression

$$G(s)\cdot H(s)=\frac{K_d\cdot K_v}{n_{mf}\cdot C\cdot R_1}\cdot\left(\frac{1}{s^2}\right)\cdot\left(s\cdot C\cdot R_2+1\right)$$

Substitute and Rearrange for Closed Loop Gain Expression

$$\frac{G(s)}{1+G(s)\cdot H(s)}=\frac{\frac{K_d\cdot K_v}{C\cdot R_1}\cdot\left[\frac{s}{\left(\frac{1}{C\cdot R_2}\right)}+1\right]}{s^2+s\cdot\left(\frac{K_d\cdot K_v}{n_{mf}}\cdot\frac{R_2}{R_1}\right)+\frac{K_d\cdot K_v}{n_{mf}\cdot C\cdot R_1}}$$

K_d = Phase detector gain (volts/radian),
= VCO transfer function gain constant (radians/second/volt),

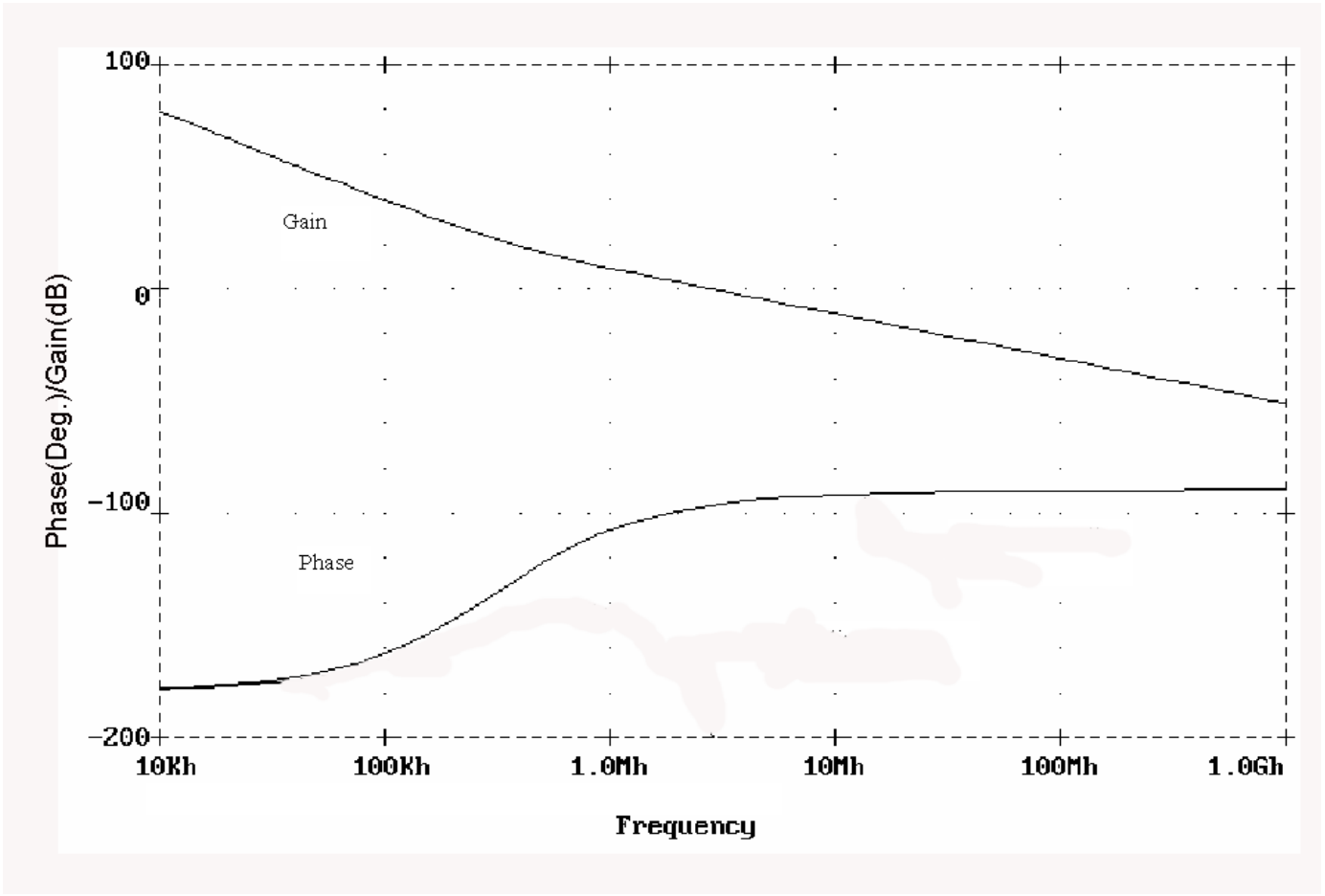
n_{mf} = Integer divider value,
= Loop Frequency Multiplication Factor,
= Output frequency/ input frequency,

C = Capacitor in the operational amplifier's feedback path (F),

R_1 = Resistor in operational amplifier's feedback path (ohms) and,

R_2 = Resistor at the negative input terminal of the operational amplifier (ohms).

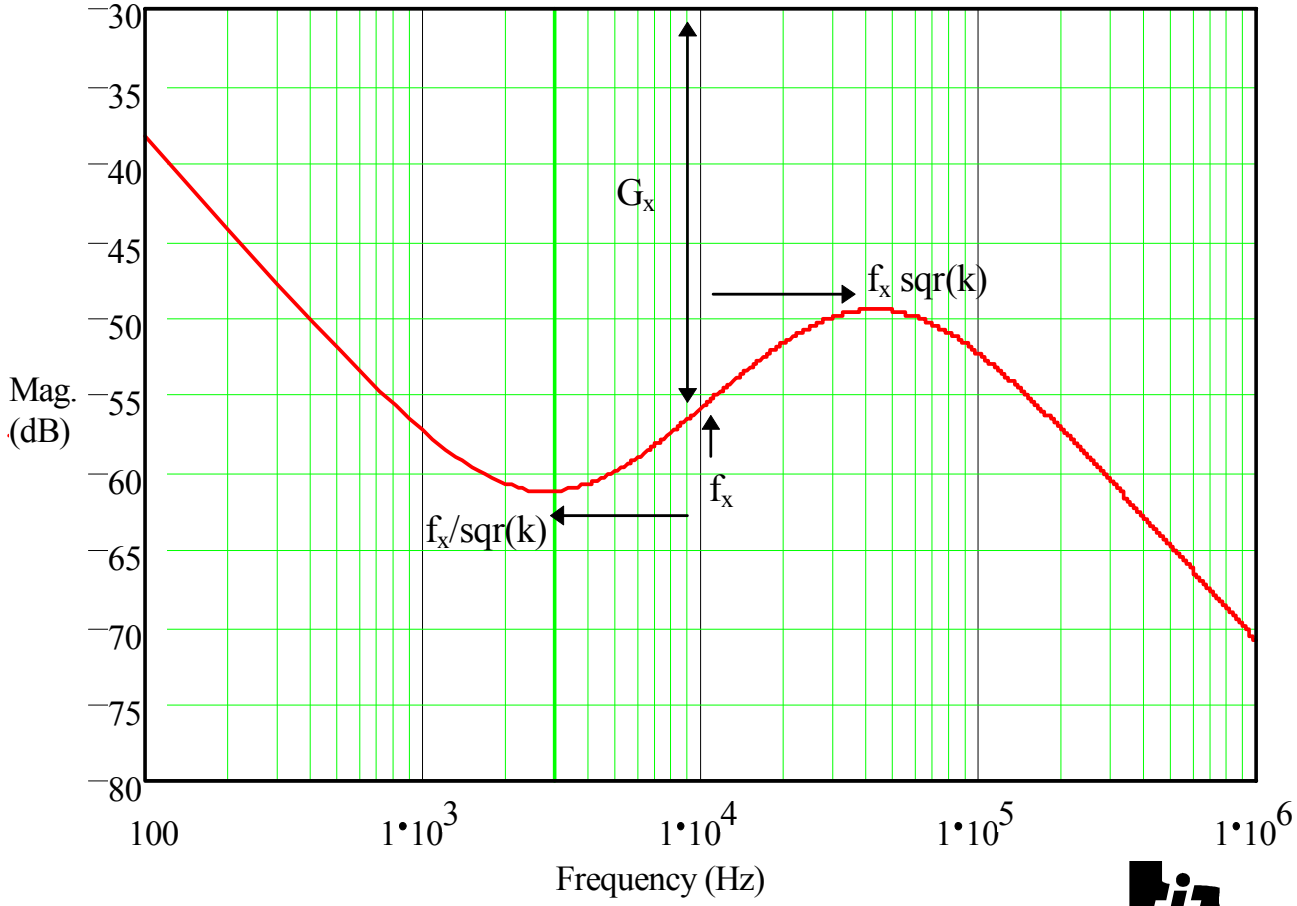
Uncentered Type 2 1 Zero Open Loop Magnitude and Phase, 1MHz Bandwidth example



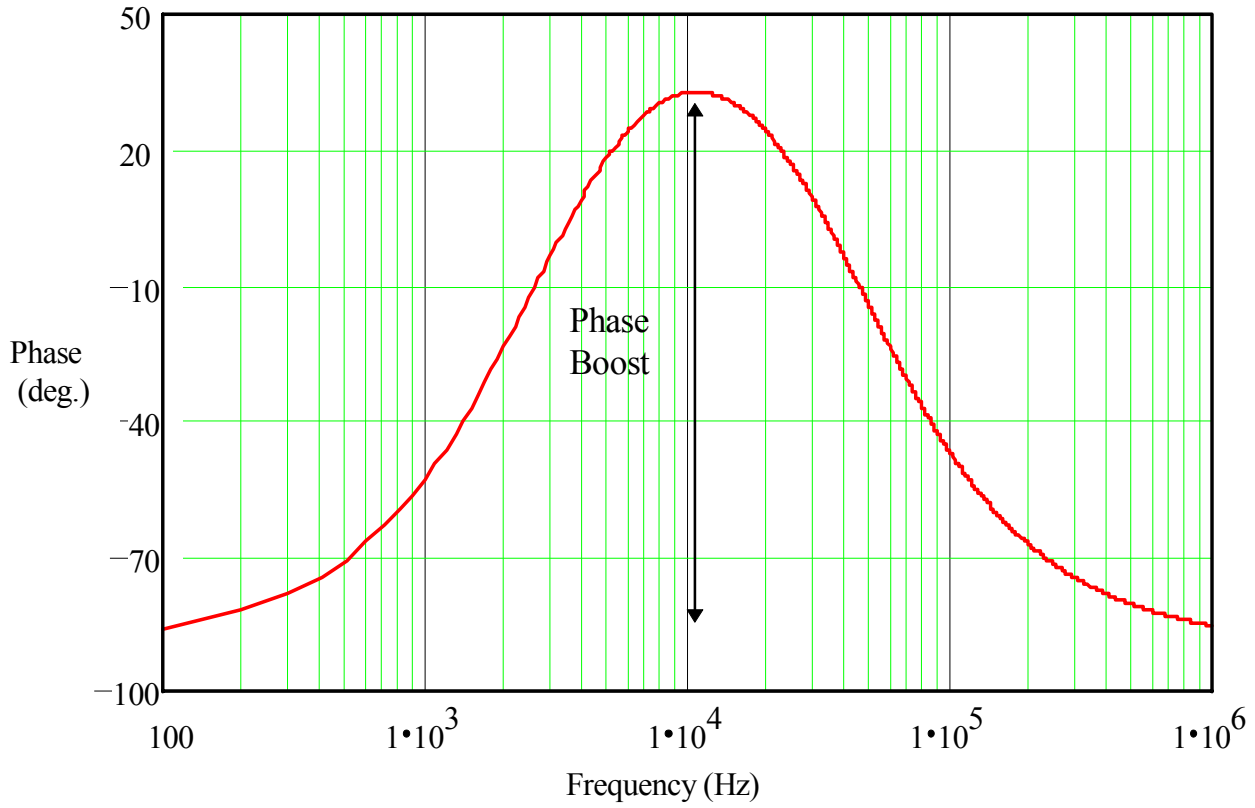
Advantages of 2 Zero 2 Pole Compensation

- OPAMP Replacing a Charge Pump
  - Wider Supply Operating Range, Rail to Rail
  - Lower Voltage drop out
  - Linear Differential to Single Ended Conversion
  - Sources VCOs that draw current
  - No power down resets
  - Acts as voltage regulator to minimize sensitivity to power supply
  - Flexibility in Compensation Polynomials
- 2 Zero 2 Pole Compensation
  - >90 deg. Added to Phase Margin
  - Wider Bandwidth
  - Wider and Optimum Stable Region for less process sensitivity

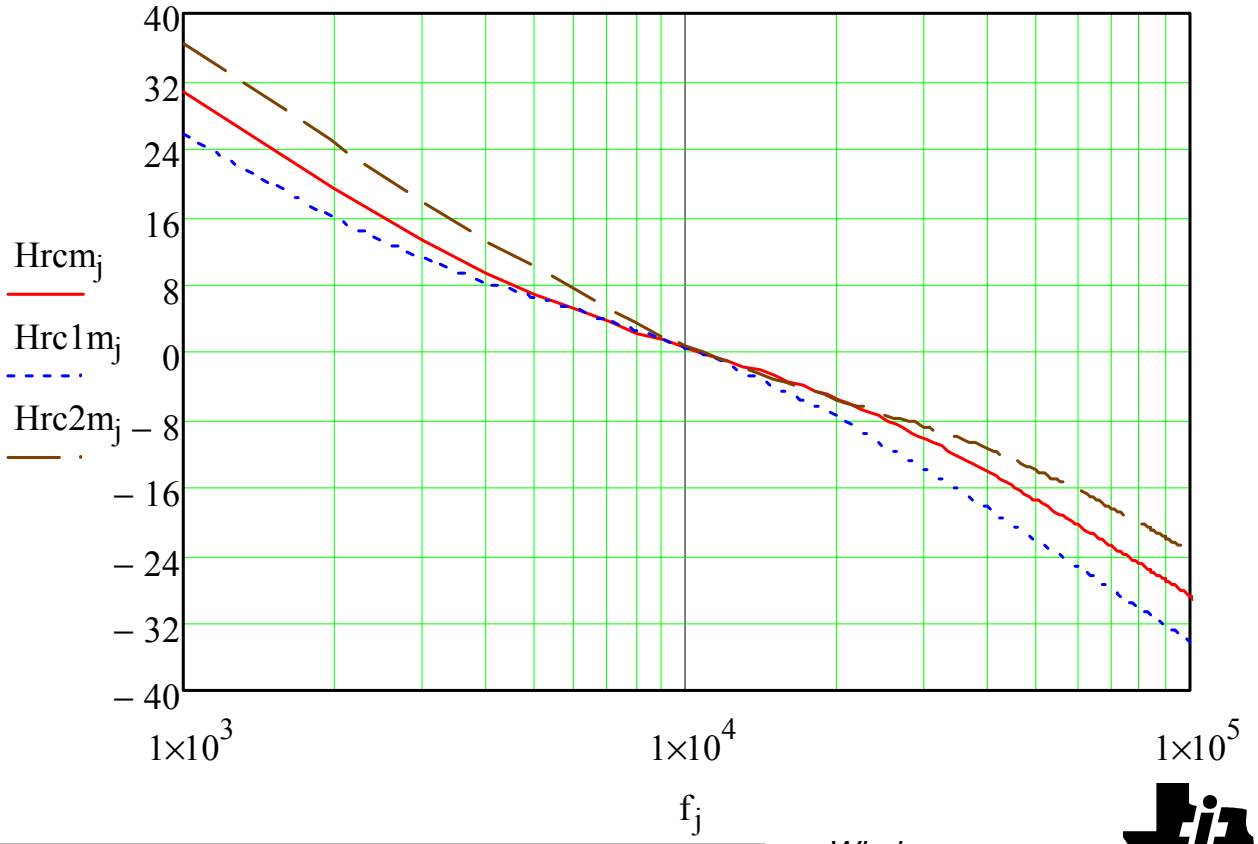
Desired high phase boost example of 2 zero 2 Pole magnitude response for compensation only and phase margin greater than 90 degrees, 10kHz BW Example



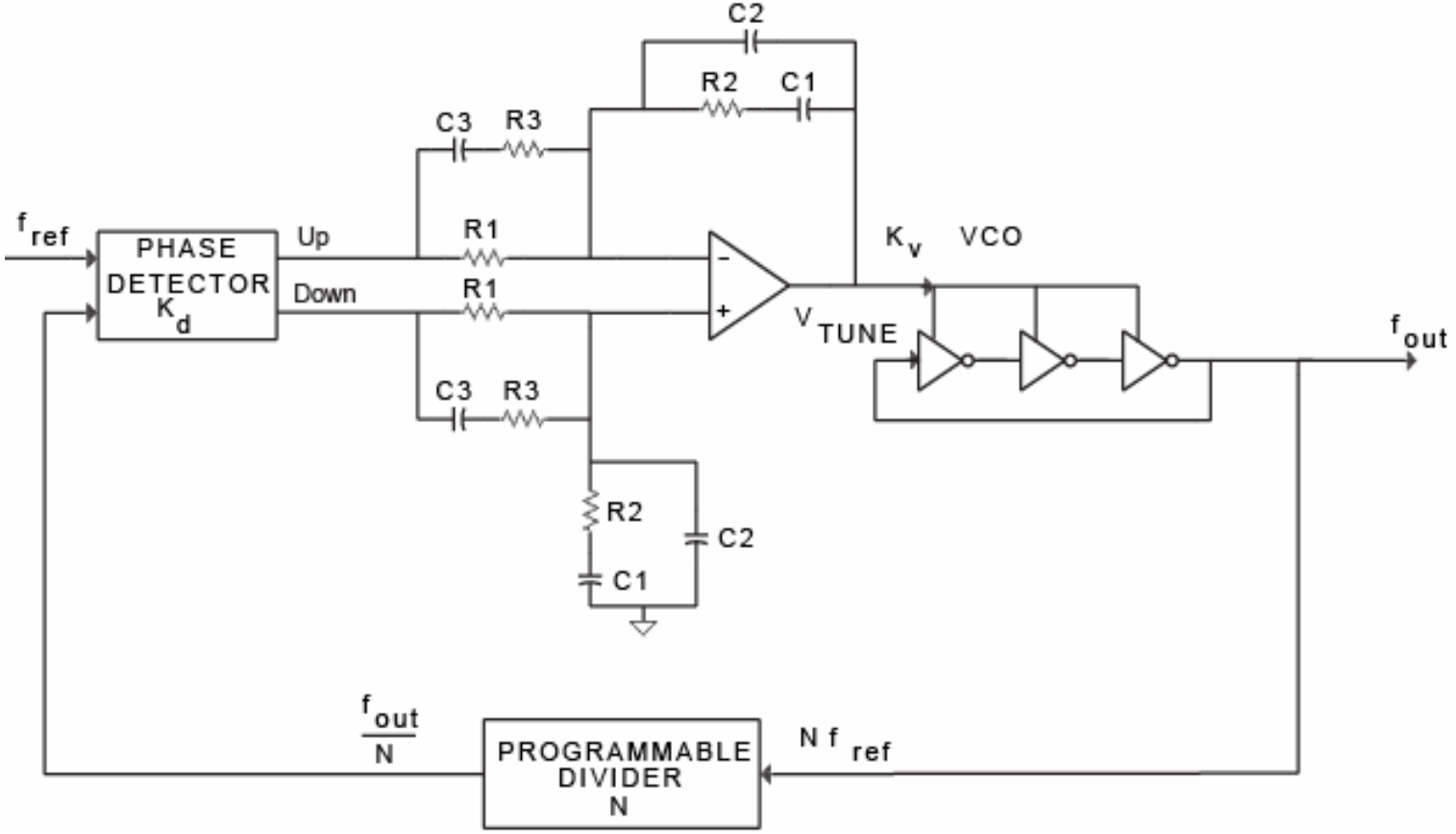
Desired 2 Zero Phase Response for Compensation Only for Phase Margin Greater Than 90 degrees (120 deg), 10kHz BW Example



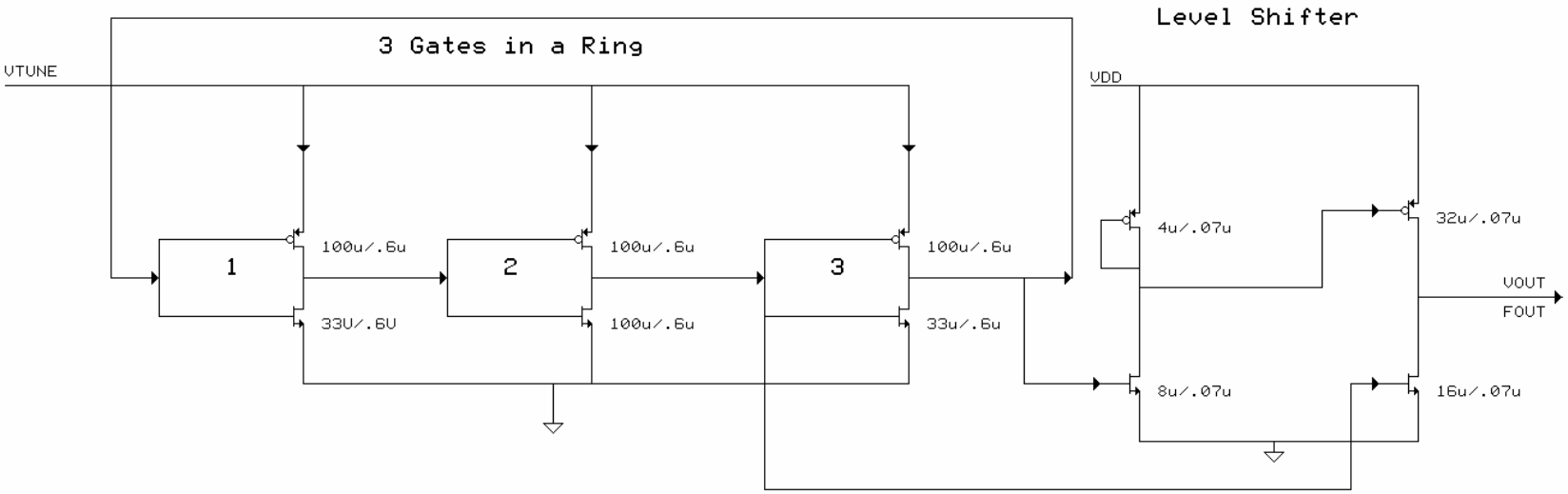
RC +90% and -50% process variation, shows PLL bandwidth insensitivity with 0.7 Damping factor and Symmetric centering of the poles and zeroes



PLL connection for a type 2 and 2 zero loop compensation.



VCO Description



2 Zero 2 Pole Open Loop Transfer Function Equations

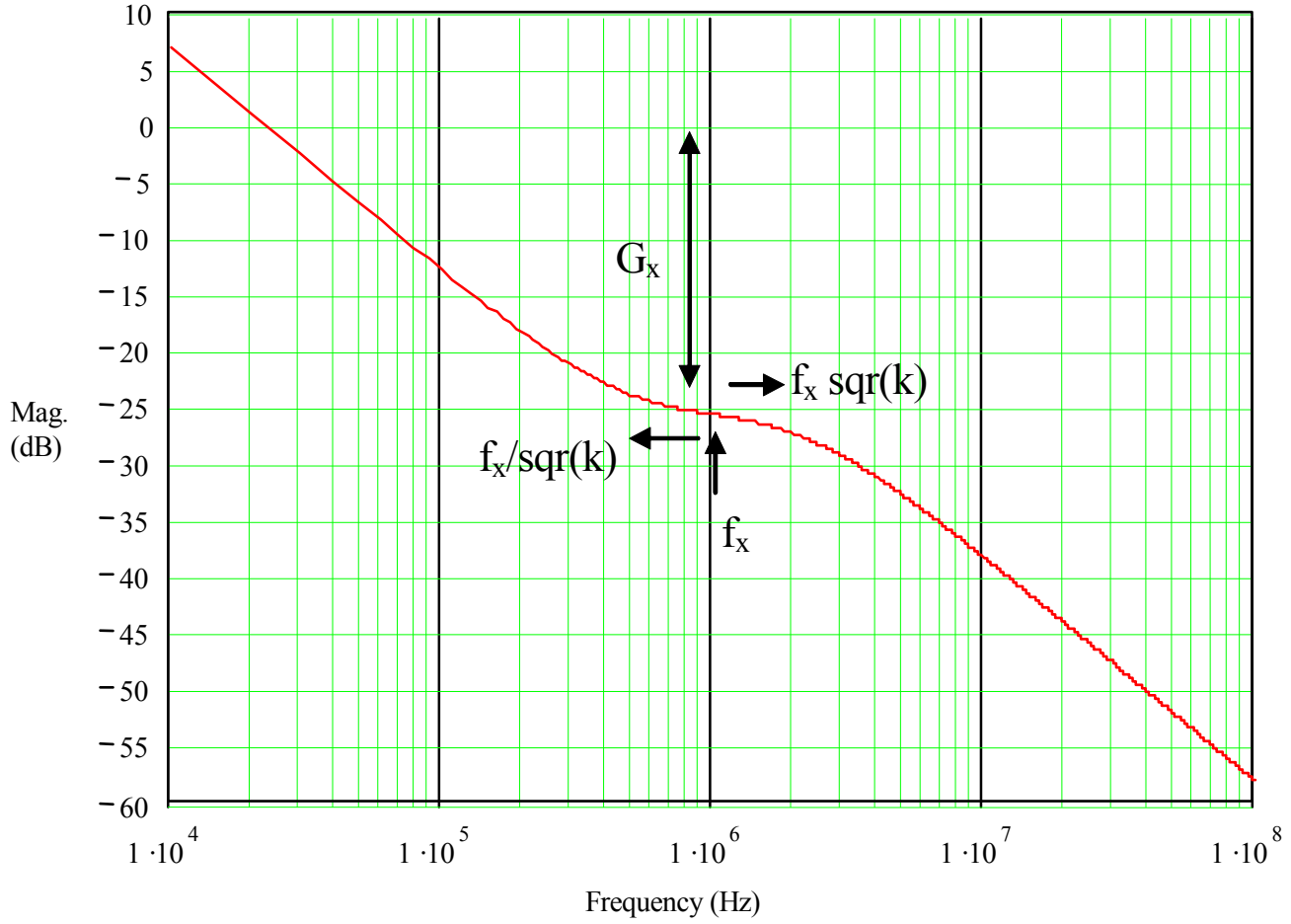
$$\frac{V_o}{V_i} = \frac{1}{s\cdot\left(C_1 + C_2\right)\cdot R_1}\cdot\frac{s\cdot C_1\cdot R_2 + 1}{1 + s\cdot R_2\cdot C_2\cdot\left(\frac{C_1}{C_1 + C_2}\right)}\cdot\frac{s\cdot\left(R_1 + R_3\right)\cdot C_3 + 1}{s\cdot R_3\cdot C_3 + 1}$$

$$k = \tan\left(\frac{\phi_{boost}}{4} + 45\right)^2$$

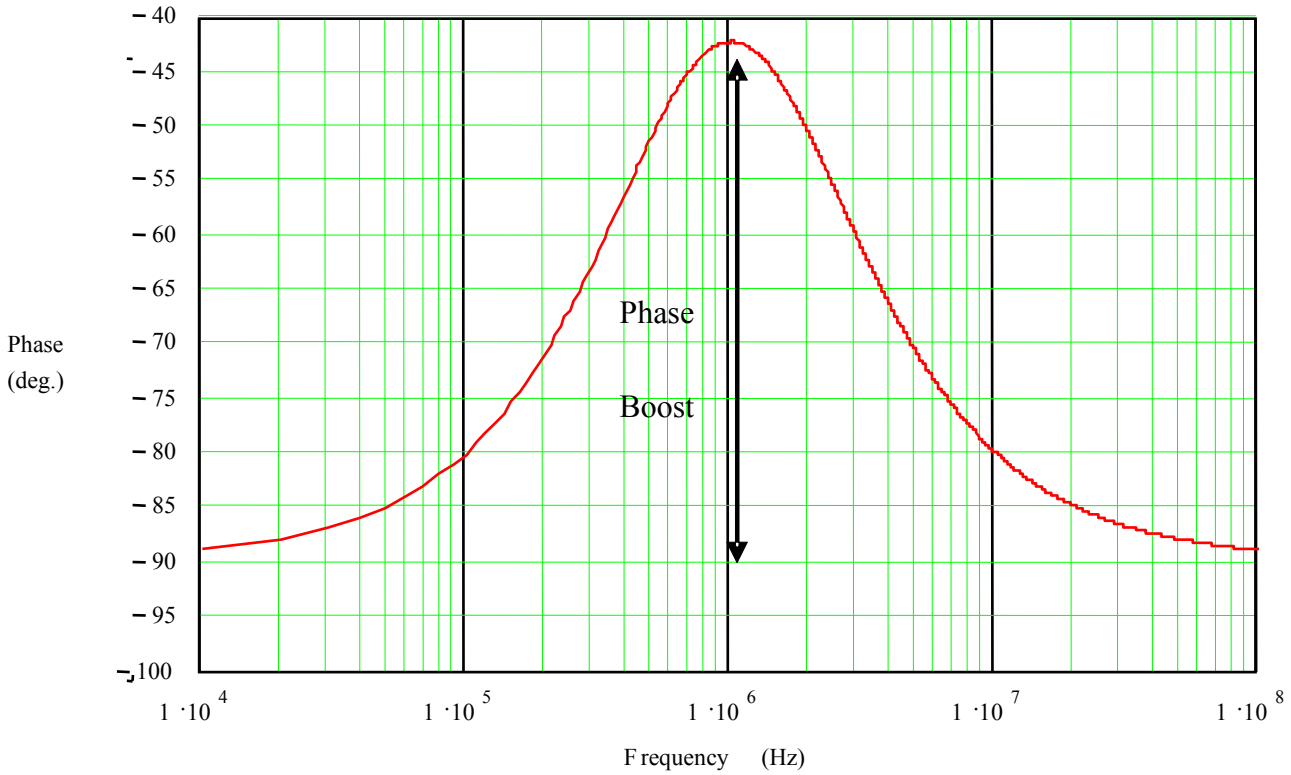
$$\frac{Vo}{Vi} = \frac{1}{\left(\frac{s}{\omega_x\cdot\frac{G_x}{k}}\right)}\cdot\frac{\left[1 + \frac{s}{\frac{\omega_x}{\sqrt{k}}}\right]\cdot\left[1 + \frac{s}{\frac{\omega_x}{\sqrt{k}}}\right]}{\left(1 + \frac{s}{\omega_x\cdot\sqrt{k}}\right)\cdot\left(1 + \frac{s}{\omega_x\cdot\sqrt{k}}\right)}$$

$$G_x = \frac{1}{\left(\frac{K_d\cdot K_v}{N\cdot\omega_x}\right)}$$

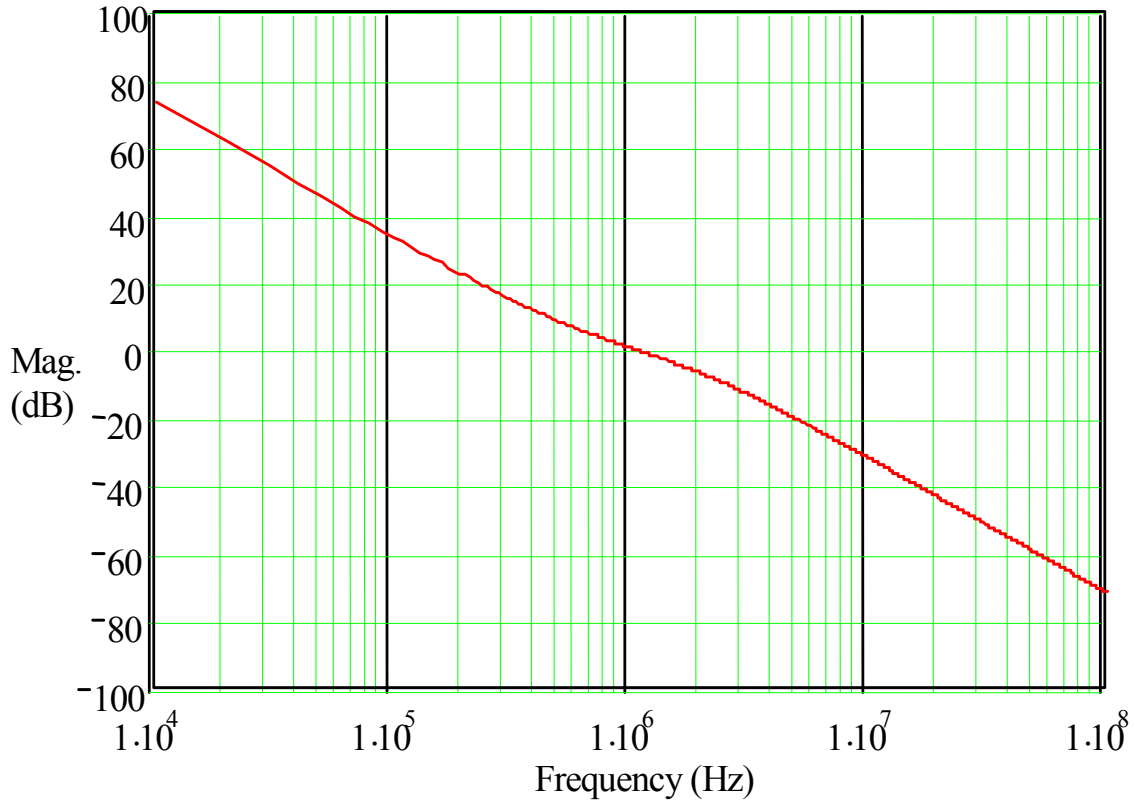
Magnitude response of 2 zero compensation solution to the design



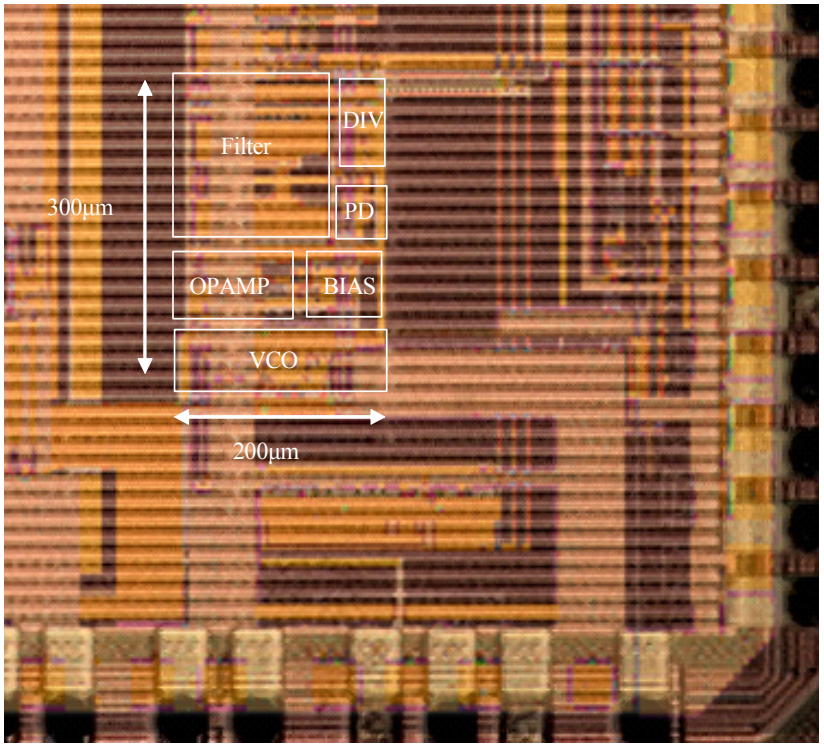
Open loop phase response with type 2 and 2 zero compensation.



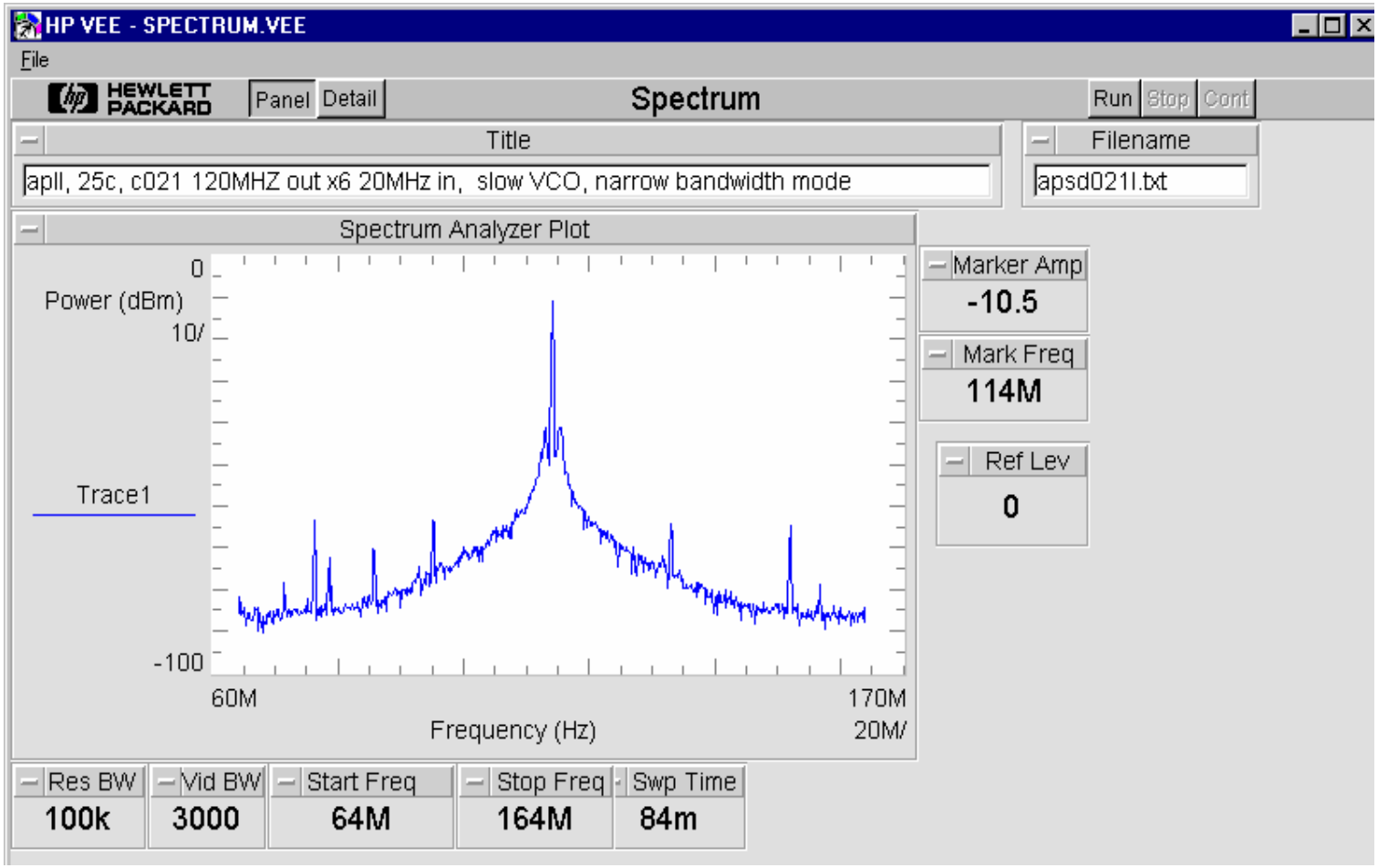
Open loop magnitude response with type 2 and 2 zero compensation



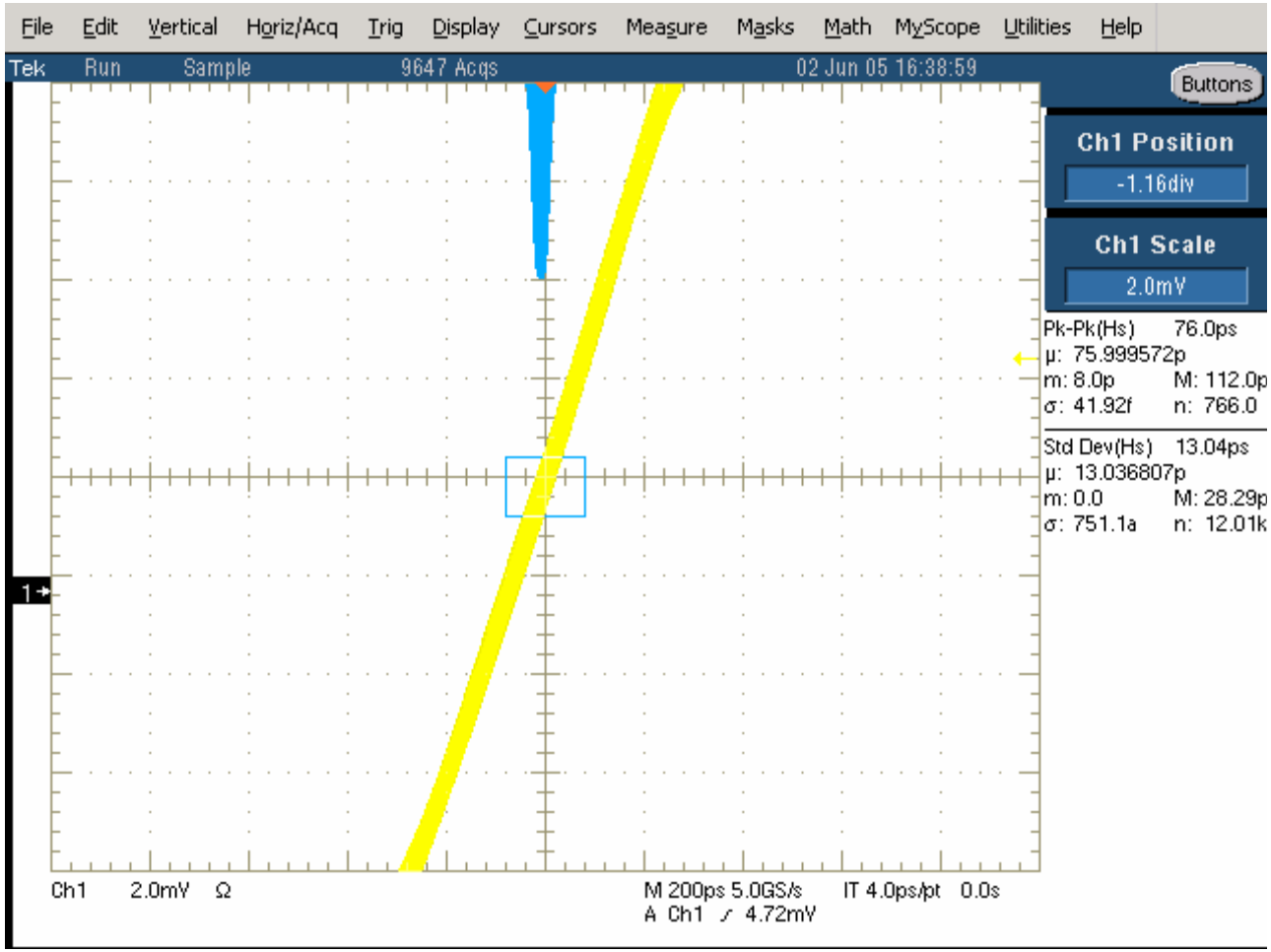
C021 Die photo of the PLL circuit, 300x200um=0.06mm^2



Measured Data Spectrum, Reference Sidebands <-60dBc

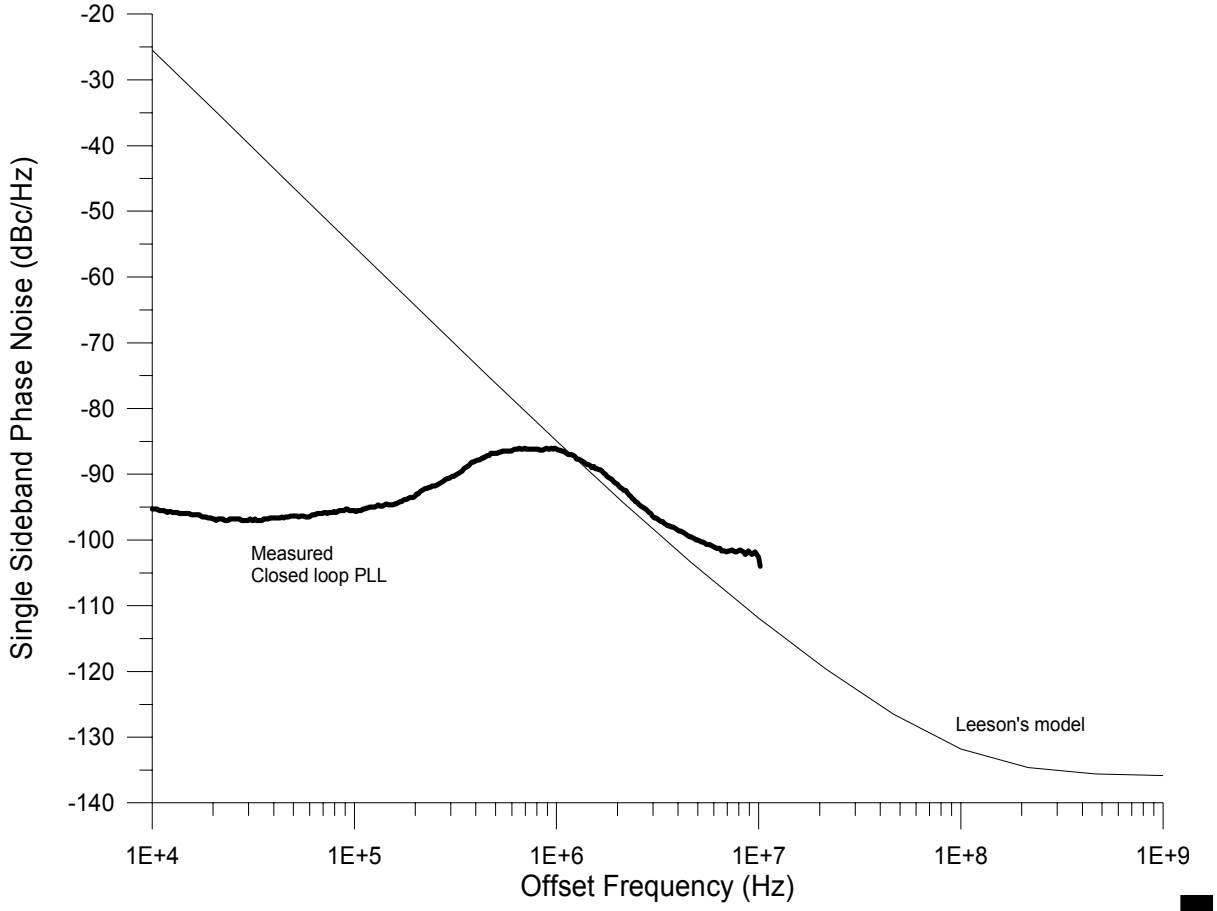


Measured Data Jitter <80ps peak to peak



Measured Phase Noise,

1MHz Bandwidth, -92dBc/Hz Phase Noise at 1MHz, High Phase Margin, Low additive Noise



Comparison Table of Measured Data with Comparable PLL References

Description	Processes	Power	Area (mm^2)	VCO Output Frequency (MHz)	Jitter	power supply sensitivity, %-fvco/%-Vdd	Comments
S. Sidropoulos VLSI '00	.35um 3.3V	21.5mW@500MHz	0.047	30-650		.06%/1%	Simulated, Supply Controled Ring VCO, wide BW
J.M. Ingino ISSCC '01	.15um 3.3V	132mW@4GHz	1.48	600- 4000	44ps p-p at 700MHz	.007%/1%	Regulator included, single ended ring CCO
H. Ahn JSSC '00	.25um 1.9V	25mW@320MHz	0.087	17-1320		.32%/1%	Supply Controled Ring VCO, wide BW, 2.5MHZ BW
K. Minami CICC '01	.1um 1.2V	30mW at 2000MHz	0.15	500-2350	21ps p-p		Single ended ring CCO
Maneatis ISSCC '03	.13um 1.5V	7mW at 240MHz	0.18	30-650	48ps p-p		Differential ring VCO, self biased
Hozer ISSCC '02	.13um 1.5V	7mW at 200MHz	0.16	10-350	155ps p-p 360MHz		Differential ring VCO, VCR
Fahim TCAS '03	.25um 1.9V	3.12mW at 160MHz		30-160	130ps p-p		All Digital PLL, diff. ring VCO
This work APLL	**.065um 1.2V**	**1mW at 240MHz**	**0.06**	**12-600**	**80ps p-p**	**.02%/1%**	

References,

1. Stanley Goldman, *Phase Locked Loop Engineering Handbook,* Artech House, Boston, 2007.
2. Roland Best, *Phase Locked Loops Design Simulation, & Applications,* McGraw Hill, New York, 1997.
3. Behzad Razavi, *Monolithic Phase-Locked Loops and Clock Recovery Circuits,* IEEE Press, New York 1996.
4. William Egan, *Frequency Synthesis by Phase-Lock*, Wiley Interscience, New York, 1981.
5. Floyd Martin Gardner, *Phaselock Techniques*, Wiley Interscience, New York, 1979.

Key Points

- Voltage Regulator can be incorporated into loop compensation (Dual Use)
- Geometrically Centered Zeroes and Poles Reduces sensitivity to R C process variations
- Increasing Resistance can be used to reduce capacitor size and overall loop size.
- Wider loop bandwidths can be achieved with 2 zeros because of the increase in phase margin.
- Widest loops give lowest phase noise for references with lower noise than the VCO
- Further future improvements can be made to reduce power, size, and area.
- Active Compensation gives flexibility in compensation